10Gbit/s error-free DPSK modulation using a push-pull dual-drive silicon modulator

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Abstract: We experimentally demonstrate a high-speed differential phase shift keying (DPSK) modulation using a silicon push-pull operated dual-drive Mach Zehnder modulator (MZM) based on carrier depletion. 5 Gbit/s and 10 Gbit/s error-free modulation is demonstrated by demodulating the generated DPSK modulated signal using a demodulation circuit based on a polarization delay interferometer through the use of a differential group delay (DGD). Furthermore, the potential for higher DPSK modulation speeds up to 20 Gbit/s is also demonstrated. The obtained results validate the potential to achieve higher order modulation formats, such as quadrature phase shift keying (QPSK), by arranging the MZM in a nested configuration.

Keywords: silicon photonics, photonic integrated circuits, phase modulation, waveguide modulators.

1. Introduction

In order to cope with the growing bandwidth demand of next generation communication networks, optical transmission systems with low cost, high spectral efficiency and high per-channel rate are required. Advanced data modulation formats have become quite attractive for optical communication systems because they enable the demanded increase of the optical network capacity [1]. When compared with on-off-keying, phase-shift keying (PSK) modulation format offers several advantages, namely 3-dB receiver sensitivity improvement when combined with balanced detection, enhanced tolerance to fiber nonlinearities and improved spectral efficiency via higher order modulation formats such as quadrature PSK (QPSK) [2].

Silicon-photonics based optoelectronics devices have been shown as the best candidates to provide high-bandwidth communications with low power consumption and low cost due to its compatibility with complementary metal-oxide-semiconductor (CMOS) manufacturing processes. Hence, it is expected that the use of silicon based optical devices will allow large scale integration relieving the existing bandwidth bottleneck.

Silicon modulators based on microring structures have been proposed to achieve phase modulation [3, 4]. Experimental demonstrations of 5 Gbit/s error-free differential PSK (DPSK) modulation [5] and 20 Gbit/s QPSK modulation, but without successful error-free demonstration, have been recently reported [6]. Ring based modulators have unique features in terms of small footprint and low drive voltage. However, the optical bandwidth or range of

useful wavelengths for modulation is much lower than compared to conventional Mach-Zehnder modulators (MZM) that in turn implies that the modulator performance is more sensitive to fabrication tolerances. Thus, some tuning mechanism, which is usually based on the thermo-optic-effect [6], becomes mandatory increasing power consumption and complexity of the transmitter. Very recently, the first works dealing with phase modulation in silicon MZM have also been reported. In principle, a single MZI is capable of covering any phase and amplitude modulation format. However, MZM are typically arranged in a nested configuration to independently modulate in the two quadratures. A silicon based dual-drive nested MZM for QPSK modulation was firstly demonstrated at 20 Gbit/s [7]. However, a poor system constellation was achieved due to the low extinction ratio and unbalanced output optical power at the MZMs. A higher modulation speed, 50 Gbit/s QPSK, has also been demonstrated by using a single-drive nested MZM but no error-free modulation was achieved [8].

In this work, we experimentally demonstrate error-free DPSK modulation up to 10 Gbit/s using a silicon dual-drive MZM. Furthermore, DPSK modulation up to 20 Gbit/s is also achieved.

2. Design and fabrication

Figures 1(a)-(b) show the GDS design and fabricated MZM. Multimode interference couplers (MMI) were used as input/output 3 dB couplers. The silicon waveguide core has a height of 220 nm, a width of 450 nm, and a slab thickness of 100 nm, as illustrated in Fig 1(c). Optical phase modulation is achieved by depleting the majority carriers from a reverse biased pn junction [9] with doping concentrations of $1.6 \cdot 10^{17}$ cm^{-3} in the p-type region and $8 \cdot 10^{17}$ cm^{-3} in the n-type region.
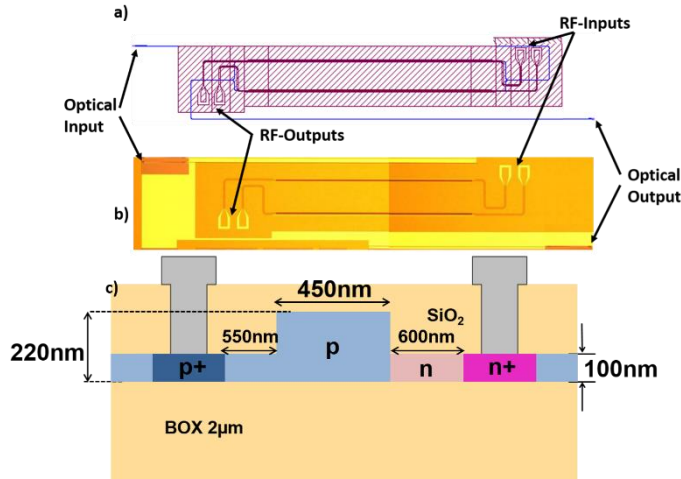
Fig. 1. DPSK modulator. (a) GDS design, (b) optical photograph of fabricated device and (c) cross-section of the pn junction.

The travelling-wave electrodes are formed by depositing a compound AlCu layer on top of highly doped p+ and n+ regions with concentrations of $1 \cdot 10^{20}$ cm^{-3}. A dual-drive electrode configuration was chosen for push-pull operation. Push-pull operation allows producing the required π-phase shift for DPSK modulation when the phase shifters are biased at zero amplitude and driven by digital data signals with opposite polarity and a peak-to-peak voltage of V_π. The two electrodes have the same length to avoid a delay between the non-inverted and inverted digital data signals. Starting from of the transfer function of a MZI and assuming the same propagation losses for both arms, we can obtain the maximum electrical field at the MZI output as:
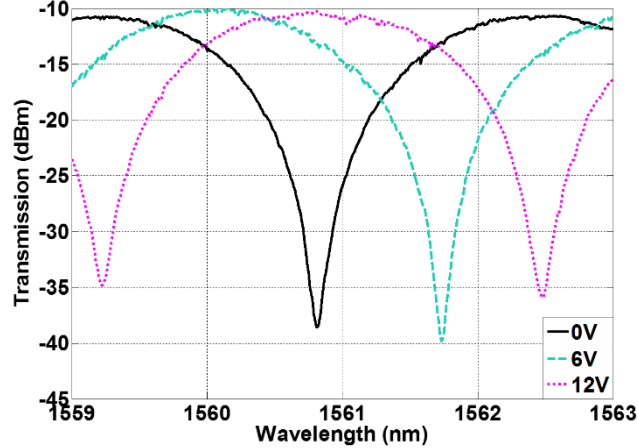
Fig. 2. Normalized transmission spectra of the MZM with different bias voltages.

We first characterized the transmission spectra of the MZM for different applied voltages. Fig. 2 shows the spectra normalized to a reference waveguide. The insertion loss of our DPSK modulator, including phase shifter and MMI losses, is about 10 dB and the free spectral range (FSR) is 3 nm. Different voltages between 0V and 12V were applied to the MZM. The extinction ratios under these DC conditions were close to 30 dB. At 12V the curve was shifted exactly one half FSR, as it can be seen in Fig. 2, marking our V_π value and giving rise to a $V_\pi \cdot L$ product about 3.6 V·cm. Compared to previous works on silicon MZM for PSK modulation, the V_π is only slightly higher than the 10V reported in [8] but in contrast the modulation length is reduced down to 3 mm, half of the length reported in [7, 8], thus significantly reducing the device footprint. Insertion losses are around 5dB higher but they could be reduced via a better optimization of the separation between the high doping regions and the optical waveguide while minimizing the impact on the modulator performance.

3. Experiments and results

Next, we characterized the DPSK modulation using the measurement setup shown in Fig. 3. The input light emitted by an external cavity laser (ECL) is coupled from a standard single mode fiber to the chip via grating couplers. The polarization was optimized and set to a TE polarization using a polarization controller (PC). Before being launched onto the chip, the optical signal was amplified by an erbium-doped fiber amplifier (EDFA), and filtered by a 3nm wide tunable optical filter. Digital data signals were generated from a pseudorandom binary sequence pattern generator with a pattern length of 2^7-1, delivered by a bit pattern generator (BPG) connected to an external clock. The signals were appropriately decorrelated and aligned before being fed to the electrodes with 8 V peak-to-peak voltage. A double RF signal probe with GSGSG configuration was used to drive the MZM, while another double RF signal probe with 50 ohm terminators was applied at the electrode output (see Figs. 1(a)-(b)). A reverse DC bias was applied to the phase shifters for operation in carrier depletion. Separate DC sources were used to adjust the bias level of the phase shifters independently using a bias-tee. The optical modulated DPSK signal was once again amplified after coupling out of the chip, and filtered before being visualized in a digital communication analyzer (DCA) for capturing the modulated eye.
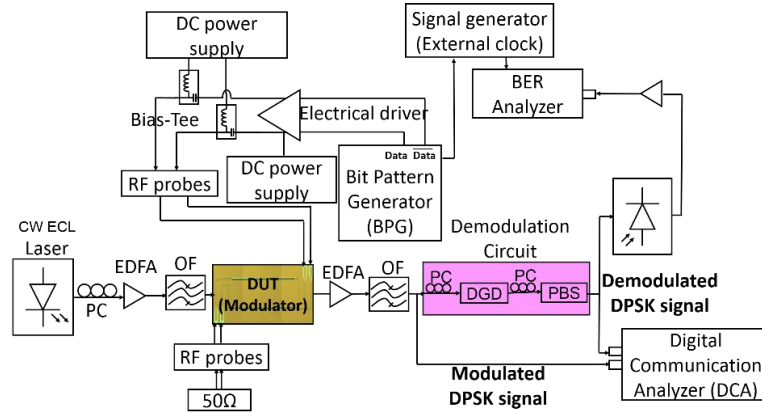
Fig. 3. Schematic of the experimental set-up for evaluating the performance of the DPSK modulator.

In order to measure the bit error rate (BER), the optical DPSK modulated signal was passed through an external demodulation circuit, as depicted in Fig. 3. The demodulation is based on a polarization delay-interferometer [10]. Using a PC, the polarization of the modulated signal is transformed into a linear polarized wave with the same intensity in the TE and the TM axis. The linear signal is then launched into a differential group delay (DGD). The DGD is a birrefrigent crystal that introduces a fixed differential group delay between the TE and TM polarization axes. In our demodulation circuit, the DGD has been used such it introduces a fixed delay between the TE and TM components that is equal or higher than 1-bit period of the modulated signal. Finally, the output signal is again adjusted in polarization with another PC and combined with a polarization beam splitter (PBS). In such a way, the linear polarization is rotated 45 degrees, so the same fraction of the TE and the delayed TM intensities match one of the polarization axis of the PBS. Hence, a combination of the signal with a 1-bit delayed signal is achieved. The demodulated signal is then simultaneously fed to the DCA and BER analyzer, as depicted in Fig. 3.
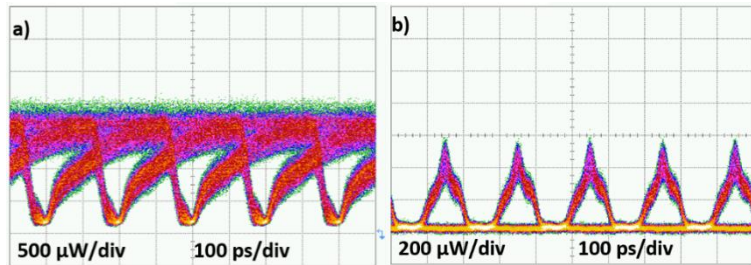

Fig. 4. DPSK (a) modulated and (b) AMI demodulated eye diagrams for 5 Gbit/s.
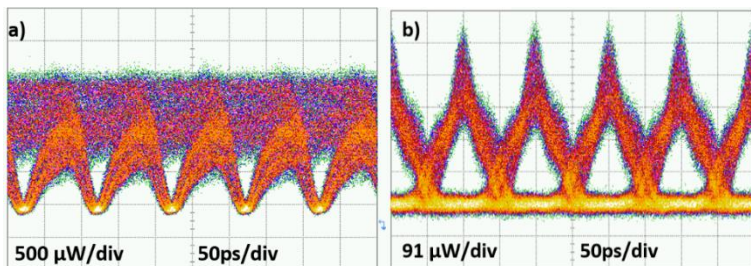

Fig. 5. DPSK (a) modulated and (b) AMI demodulated eye diagrams for 10 Gbit/s.

The measured eye diagrams of the modulated DPSK signal at 5 Gbit/s and 10 Gbit/s are shown in Fig. 4(a) and Fig. 5(a), respectively. The noise is mainly due to the limitation in the drive voltage which is not high enough to achieve V_π in each phase shifter of the MZM (the driver only offers 66.6% of the required V_π). However, clear eye diagrams were obtained for both measured bit rates. Figures 4(b) show the alternate-mark inversion (AMI) demodulated eye diagrams for the 5 Gbit/s modulation, while Fig. 5(b) shows the AMI demodulated eye diagram for the 10 Gbit/s modulation bit rate. As it shown in these figures, very open eye diagrams were measured confirming the correct DPSK modulation for both measured bit rates.
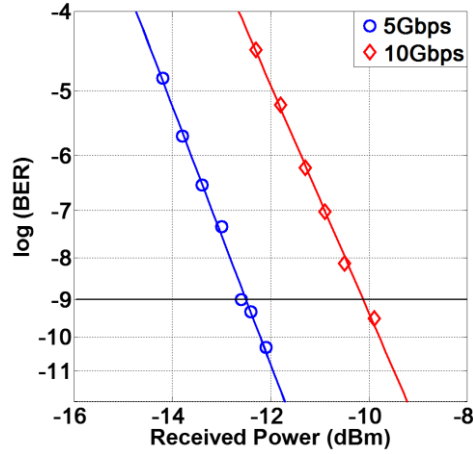

Fig. 6. BER versus received power for 5Gbit/s (○-blue curve) and 10Gbit/s (◊-red curve) DPSK demodulation.

The performance of the silicon DPSK modulator was further evaluated by measuring the BER. As shown in Fig. 6, error-free DPSK modulation, for 5 Gbit/s (○-blue curve) and 10 Gbit/s (◊-red curve), is obtained. Furthermore, no error floor is observed in the results showing that inter-symbol interference (ISI) is not produced in the modulation due to carrier latency effects.
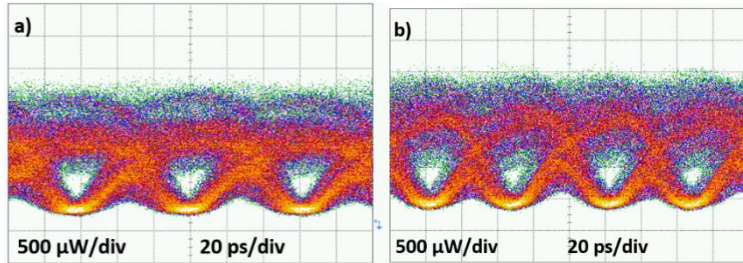

Fig. 7. DPSK modulated eye diagram for (a) 15 Gbit/s (b) 20 Gbit/s.

Modulation at higher bit rates was also tested. DPSK modulated eye diagrams at 15 Gbit/s and 20 Gbit/s are shown in Fig. 7 (a) and Fig. 7 (b) respectively. Unfortunately, the delay introduced by the DGD (τ~90 ps) was too long for correctly demodulating the DPSK signal above 10 Gbit/s and therefore it was not possible to measure the BER for higher speeds. However, it can be clearly seen that the transitions between the different states do not overlap which confirms that ISI would not occur when the right demodulation stage is used and thus the high speed operation of the DPSK modulator.

4. Conclusion

In summary, we have successfully demonstrated error-free DPSK modulation at 5 Gbit/s and 10 Gbit/s using a dual-drive silicon MZM. Furthermore, we have also shown the feasibility of the proposed MZM for 15 Gbit/s and 20 Gbit/s DPSK modulation. The obtained results validate the potential to achieve higher order modulation formats, such as QPSK, by arranging the MZM in a nested configuration. Furthermore, a fully integrated silicon transceiver could be implemented by combining the proposed MZM with an integrated silicon DPSK receiver [11].

Acknowledgments

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