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A Control Scheme without Sensors at the PV Source for Cost and Size Reduction in Two-Stage Grid Connected Inverters

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Abstract: In order to reduce the cost of PV facilities, the market requires low cost and highly reliable PV inverters, which must comply with several regulations. Some research has focused on decreasing the distortion of the current injected into the grid, reducing the size of the DC-link capacitors and removing sensors, while keeping a good performance of the maximum power point tracking (MPPT) algorithms. Although those objectives are different, all of them are linked to the inverter DC-link voltage control loop. Both the reduction of the DC-link capacitance and the use of sensorless MPPT algorithms require a voltage control loop faster than that of conventional implementations in order to perform properly, but the distortion of the current injected into the grid might rise as a result. This research studies a complete solution for two-stage grid-connected PV inverters, based on the features of second-order generalized integrators. The experimental tests show that the proposed implementation has a performance similar to that of the conventional control of two-stage PV inverters but at a much lower cost.

Keywords: photovoltaics; two-stage grid-connected PV inverters; reduced DC-link; sensorless MPPT

1. Introduction

In order to reduce the installation and maintenance costs, the photovoltaic (PV) market requires low cost and reliable systems. Moreover, grid-connected PV inverters must comply with several electromagnetic compatibility (EMC) regulations, some of which limit the distortion of the current injected into the grid (THDi), like IEC EN61000 and IEEE519 [1–4]. Maximum power point tracking (MPPT) algorithms are implemented to optimize the performance of PV systems [5–9]. Conventional MPPT algorithms use current and voltage sensors to calculate the power extracted from the PV source. Several investigations have focused on reducing the number of sensors in PV inverters when implementing MPPT algorithms [10–13], which has a positive impact on cost reduction.

One possible solution to achieve both a good maximum point tracking (MPPT) performance and a reduced THDi is the use of two-stage grid-connected PV inverters, based on a DC-DC converter connected to the PV source, followed by a grid-connected inverter [14–16]. This paper focused on this kind of topologies.

There is a trend to reduce the required capacitance at the DC-link between the DC-DC converter and the inverter stage, which allows replacing electrolytic capacitors by film capacitors, which are more durable [17–22]. Two major effects of the DC-link capacitance reduction are the increase of the voltage ripple at the capacitors and higher transient variations of that voltage under dynamic operation point changes of the inverter. These variations must be bound for the proper operation of the inverter.

In this research, the implementation of control structures based on second-order generalized integrators (SOGI) [23–27] is proposed to support the DC-link capacitance reduction of two-stage

grid-connected PV inverters with a small number of sensors. On the one hand, it will be shown that SOGIs can improve the dynamic response of the DC-link voltage. On the other hand, the frequency adaptability of SOGI structures will help to reduce the THDi in the case of variations of the grid frequency, even under highly distorted grid voltage conditions.

A sensorless MPPT algorithm that does not require sensors of the PV panel electrical variables was developed in this study. It is based on the power balance at the DC-link [11] and the improvement of the PV inverter voltage control loop achieved by the use of SOGIs.

The applied techniques allow both a reduced DC-link and a sensorless MPPT algorithm, keeping the performance similar to that of conventional MPPTs, but at a much lower cost.

2. Two-Stage Grid-Connected PV Inverter

The two-stage grid-connected PV inverter shown in Figure 1 has been used for validating the theoretical study. It is formed by a flyback DC-DC and a single phase inverter. The inverter connects a single 230 W PV panel to the single-phase grid (230 Vrms, 50 Hz).

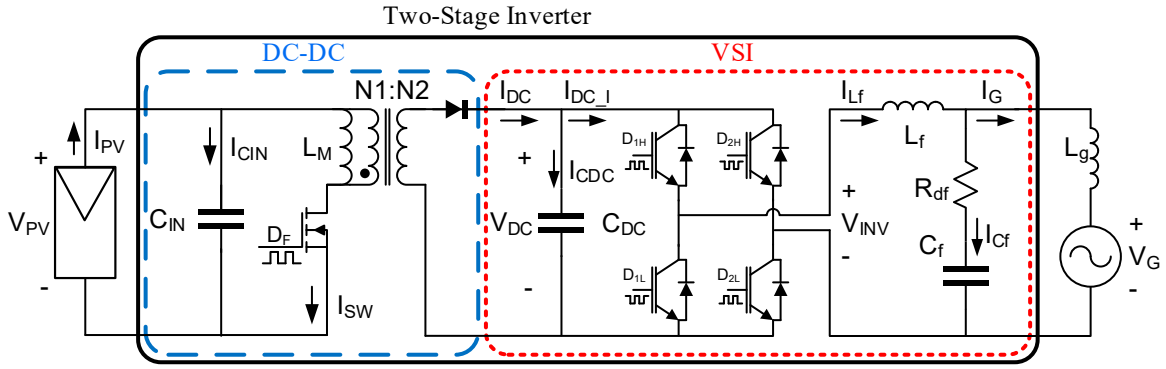


Figure 1. Two-stage grid-connected inverter.

The inverter has a reduced size DC-link. Voltage and current sensors for the measurement of the PV panel voltage, V_{PV}, and current, I_{PV}, are available, in order to compare conventional MPPT algorithms, which make use of those sensors, with sensorless MPPT algorithms under the same conditions.

Costs saving associated with a smaller bulk capacitor and to the absence of MPPT sensors depends on several characteristics, but the estimation done for the implemented prototype is detailed in Table A1 of Appendix A.

2.1. Grid-tied VSI

The voltage source inverter (VSI) is formed by the DC-link capacitance (C_{DC}), a full bridge of IGBTs and an LCL grid filter. The full-bridge is commutated by means of unipolar sinusoidal pulse width modulation (SPWM). The grid filter was designed following the guidelines of Reference [28]. The values of the inverter are shown in Table 1.

The current I_{CDC} has high-frequency current components (I_{DC_SW}) due to the switching of the transistors and a low-frequency current component (I_{DC_AC}). The frequency of I_{DC_AC} is twice the grid frequency and causes a voltage ripple at the DC-link (V_{DC_R}). In Reference [18] it was shown that the minimum value of C_{DC} is determined by the maximum and minimum permissible voltage at the DC-link caused by V_{DC_R}. However, this criterion does not consider the dynamics of the DC-link [19] and transient voltage variations, that are due to changes in the operation point. The proposed value of the capacitance, C_{DC}, to study the effects of a reduced DC-link is designed to limit the peak to peak

value of V_{DC_R} to 10% of V_{DC} at nominal power (P_G = 230 W), thus the value of the capacitance C_{DC} is calculated following Equation (1).

$$C_{DC} \geq \sqrt{2} \cdot \frac{V_{G_{RMS}} \cdot I_{G_{RMS}}}{V_{DC_{AV}} \cdot \pi \cdot F_{RDC} \cdot V_{DC_R\ PP}} = \frac{230V \cdot 1A}{380V \cdot \pi \cdot 100Hz \cdot 38V} = 50.7\ \mu F \approx 50\ \mu F \quad (1)$$

Table 1. Values of the Voltage Source Inverter (VSI) stage.

Item	Value
Topology	Single phase, full-bridge
RMS Grid Voltage: V_G	230 V_{AC}
Grid frequency: F_G	50 Hz
Rated Output Power: P_G	230 W
Max Current: I_G	1 A
Modulation	Unipolar SPWM
Inverter switching Frequency: F_{SW_I}	20 kHz
Sampling Frequency: F_S	40 kHz
Filter Inductance: L_f	38 mH
Filter Capacitance: Cf	330 nF
Damping Resistor: Rf	50 Ω
Grid Inductance estimation: L_g	1.5 mH (strong grid) 3 mH (standard grid) 6 mH (weak grid)
DC-link Voltage: V_{DC}	380 V
DC-link Voltage Ripple: V_{DC_R}	10% of V_{DC} (38 $V_{pk\text{-}pk}$)
DC-link Capacitance: C_{DC}	50 µF

2.2. Step Up DC-DC Converter

The DC-DC stage, shown in Figure 1, is a Flyback converter designed for boosting the voltage from the PV panel (V_{PV}) up to the voltage of the DC-link (V_{DC}) and providing high-frequency galvanic isolation between the PV panel and the grid. The converter is designed to work in discontinuous conduction mode (DCM) because the value of the transformer magnetizing inductance (L_M) and the physical size of the transformer become smaller [15]. The MPPT algorithm establishes the operation point of this stage since the PV panel voltage is at the input of the DC-DC converter. It is worth pointing out that in the two-stage PV inverter structure the output voltage of the DC-DC converter is regulated by the inverter stage, whereas the panel voltage is controlled by the DC-DC converter following the reference value provided by the MPPT algorithm.

The current I_{SW}, through the switch of the DC-DC converter, is composed by Equation (2) an average value equal to the PV panel current, I_{PV}, and a high-frequency component, I_{CIN}, provided by a low voltage input capacitance, C_{IN}, following Equation (2).

$$I_{SW} = I_{PV} - I_{CIN}. \quad (2)$$

The size of C_{IN} depends on the high-frequency current components at the input of the DC-DC converter. Besides, the value of the output capacitance, C_{DC}, has an influence on the MPPT performance, since V_{PV} is susceptible to the low-frequency voltage ripple at the DC-link voltage, V_{DC_R}. It is worth pointing out that the implementation of a peak current control (PCC) is highly desirable for protecting the power switches from transient overcurrents. The values of the DC-DC converter are detailed in Table 2.

Table 2. Values of the DC-DC stage.

Item	Value
Topology	Flyback
DC Input Voltage: V_{PV}	24 V to 35 V at the MPPT
DC Output Voltage: V_{DC}	380 V
Rated Input Power: P_{PV}	230 W
Max Input Current: I_{PV}	8 A
Flyback converter switching Frequency: F_{SW_F}	24 kHz
Input Capacitance: C_{IN}	4 mF
Transformer Turns Ratio: N = N1/N2	1/16
Transformer Magnetizing Inductance: L_M	10 µH
Conduction Mode	Discontinuous (DCM)

3. Control

The control of the two-stage inverter has been implemented digitally in a Texas Instruments TMS320F28335 [29] microcontroller with digital signal processor (DSP) extensions at a sampling frequency (F_S) of 40 kHz. The controllers have been calculated in the continuous domain, having taken into account the digital delays, and then discretized using the bilinear "Tustin" transform. The delay between the sampling and the update of the reference inside the DSP has been done by using a second-order Padé approximation.

It is worth pointing out that the dynamic models used in this control study result from perturbing the averaged variables of the DC-DC converter or of the inverter stage around an operation point, as expressed by Equation (3). In Equation (3), X and $\hat{x}$ denote the operation point value and the small-signal term of the averaged variable, x, respectively. The averaging is done in every cycle of the switching frequency.

$$x = X + \hat{x} \tag{3}$$

3.1. Control Scheme of the VSI Stage

The complete control structure of the VSI is shown in Figure 2.

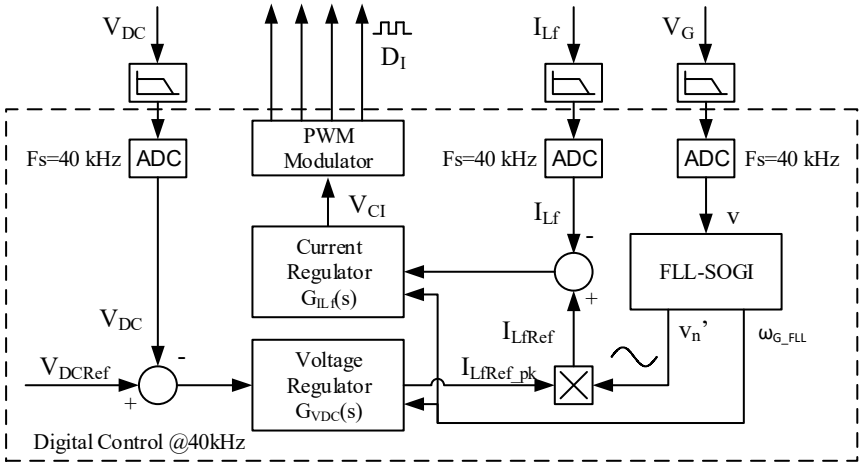


Figure 2. VSI control scheme.

3.1.1. Synchronization with the Grid

The synchronization with the grid voltage (V_G) has been implemented by means of an SOGI based Frequency Locked Loop (FLL-SOGI) [27], which provides the calculation of the grid frequency in rad/s, ω_{G_FLL}, a sinusoidal signal in phase with the grid, v', and a sinusoidal signal in quadrature,

qv′. The amplitude of the fundamental harmonic of V_G, v'_{pk}, is calculated following Equation (4), and a normalized sinusoidal signal in phase with the grid, v'_n, is obtained in Equation (5).

$$v'_{pk} = \sqrt{v'^2 + qv'^2} \tag{4}$$

$$v'_n = \frac{v'}{v'_{pk}} \rightarrow v'_n(t) \equiv \cos(\omega_{G\_FLL} \cdot t) \tag{5}$$

3.1.2. Control of the Current Injected into the Grid

The control of the current injected into the grid, I_G, is indirectly performed by controlling the current through the inductance Lf of the filter, I_{Lf}, because the control of I_{Lf} is less sensitive to grid impedance variations [30].

A proportional + resonant controller + a harmonics compensator (P + R + HC) current regulator, $G_{ILf}(s)$, expressed by Equation (6), has been designed following Reference [26] and References [31–34] for tracking the sinusoidal reference of I_{Lf}, $I_{Lf\,Ref}$. Both the resonant and the harmonics compensator have been implemented by means of second-order generalized integrators (SOGI).

$$G_{ILf}(s) = P_{Lf} + R_{Lf}(s) + HC(s) = K_{PLf} + \sum_{i=1,3,5,7} K_{RLf[i]} \frac{K_{BWRLf[i]} \cdot (\omega_{G\_FLL} \cdot i) \cdot s}{s^2 + K_{BWRLf[i]} \cdot (\omega_{G\_FLL} \cdot i) \cdot s + (\omega_{G\_FLL} \cdot i)^2} \tag{6}$$

Taking into account that the value of ω_{G_FLL} used in Equation (6), provided by the FLL-SOGI, it can be concluded that G_{ILf} is adaptive in frequency, allowing high performance even under large variations of the grid frequency. The index 'i' in Equation (6) represents the corresponding harmonic. The gains of G_{ILf} are shown in Table 3.

Table 3. Constants of the regulator P + R + HC.

Constant	Value
K_{PLf}	0.65
K_{RLf1}	100
K_{BWRLf1}	0.02
K_{RLf3}	100
K_{BWRLf3}	0.02/3
K_{RLf5}	100
K_{BWRLf5}	0.02/5
K_{RLf7}	25
K_{BWRLf7}	0.02/7

3.1.3. Control of the DC-link Voltage (V_{DC})

A reduced DC-link capacitance leads to the fast dynamics of the V_{DC} control loop at the expense of an increase of the THDi of I_G [16,17]. In Reference [16] a notch filter in the DC-link voltage control loop was implemented to reduce the low-frequency harmonics of I_G. In the current study, the notch filter is implemented by means of SOGIs, achieving adaptation to grid frequency variations. This implementation allows an increase of the crossover frequency of the V_{DC} control loop without increasing the distortion of I_G, even with a high low voltage ripple at the DC-link and under large grid frequency variations. The control scheme of V_{DC} is shown in Figure 3.

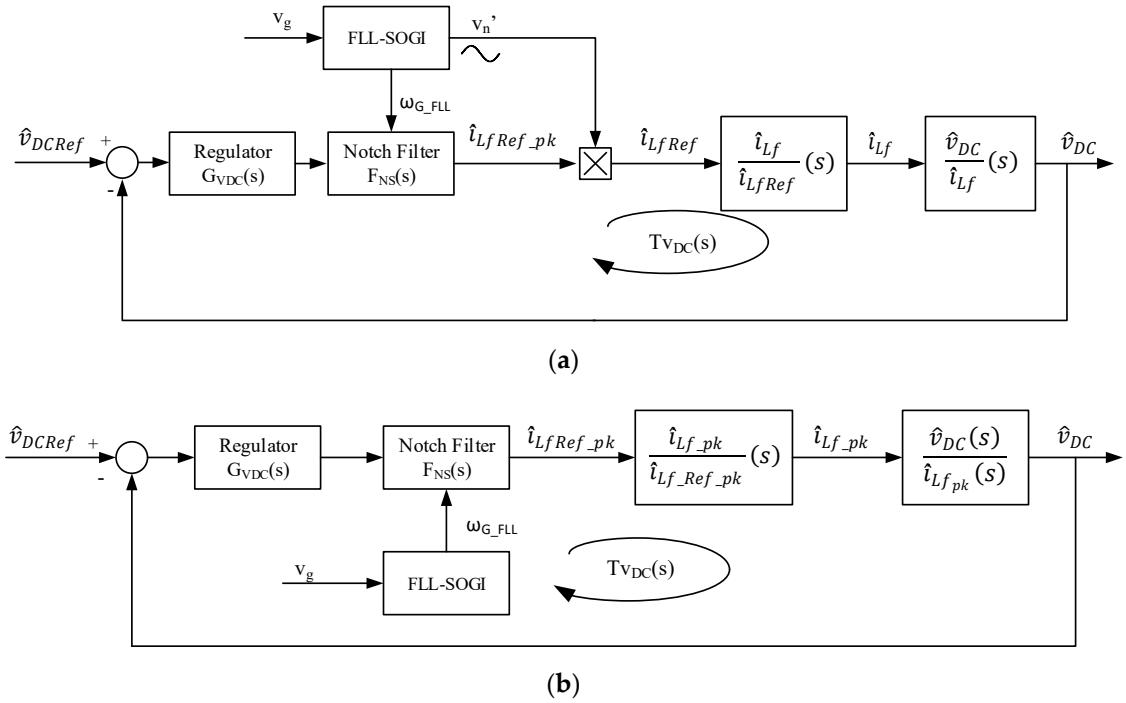


Figure 3. Control loop of the DC-link voltage (V_{DC}) with second order generalized integrator (SOGI) notch filter: (**a**) detailed model, (**b**) equivalent model.

In Figure 3, two small-signal transfer functions play an important role. The first one is the transfer function $\hat{i}_{Lf}/\hat{i}_{LfRef}(s)$ in Figure 3a, which is obtained by closing the control loop of I_{Lf}. This transfer function can be approximated by (7) in Figure 3b, where ω_{Ci} is the crossover frequency of the VSI current loop.

$$\frac{\hat{i}_{Lf\_pk}}{\hat{i}_{Lf\_Ref\_pk}}(s) \approx \frac{1}{1+\frac{s}{\omega_{Ci}}} \tag{7}$$

In the case of a three-phase grid connected inverter, the derivation of the transfer function from the AC side active current to the DC-link voltage and the adjustment of the voltage loop PI regulator can be found in Reference [35], pages 210–219. In the case of the single-phase inverter under study, an analogous Equation (8) can be derived, based on the power balance and the power perturbation at the DC and AC sides. The transfer function from the peak value of the inverter output current at the AC side to the DC-link voltage can be expressed by Equation (8) after some derivation. Note that Equation (8) consists of a first-order transfer function with an (unstable) right half plane (RHP) pole, ω_{P_RHP}, whose value depends on the operation point values V_{DC} and I_{DC}.

$$\frac{\hat{v}_{DC}(s)}{\hat{i}_{Lf\_pk}(s)} = \frac{\frac{V_G}{\sqrt{2}\cdot I_{DC}}}{1-\frac{s}{\left(\frac{I_{DC}}{C_{DC}\cdot V_{DC}}\right)}} = \frac{\frac{V_G}{\sqrt{2}\cdot I_{DC}}}{1-\frac{s}{\omega_{P\_RHP}}};\ \omega_{P\_RHP} = \frac{I_{DC}}{C_{DC}\cdot V_{DC}} \tag{8}$$

The loop gain $T_{VDC}(s)$ of Figure 3 is tuned by means of the PI regulator $G_{VDC}(s)$. Equation (9) provides the crossover frequency, $Fc_{\_VDC}$, one decade higher than $\omega_{P\_RHP}/(2\,\pi)$. Note that an open loop unstable system can be stabilized by feedback only if the loop gain has a gain crossover frequency much higher than the maximum possible value of the unstable open loop pole, $Fc_{\_VDC} >> \omega_{P\_RHP}/(2\,\pi)$ in this case. Besides, the value of $Fc_{\_VDC}$ must be much lower than twice the grid frequency (F_G), to

reduce the effect of the low-frequency voltage ripple at the DC-link (f_{ripple} = 2 $Fc_{\_VDC}$) in the current reference signal i_{Lf_ref}, which could produce an unacceptable distortion of the grid injected current.

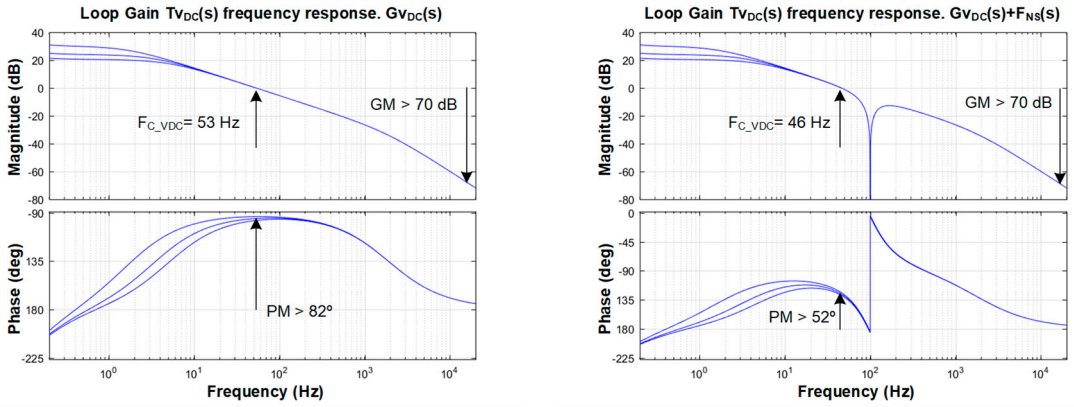
$$Gv_{DC}(s) = -0.03902 \cdot \left(\frac{s + 0.6283}{s} \right) \tag{9}$$

It can be observed from Figure 3 that a notch filter, $F_{NS}(s)$, is placed in series with the PI controller $Gv_{DC}(s)$. The expression of the notch filter transfer function is given by Equation (10). The center frequency of $F_{NS}(s)$ is twice the grid frequency (ω_{NS} = 2 ω_{G_FLL}) in order to filter the ripple at f_{ripple} coming from the sensed DC-link voltage. The tuning of the notch filter is provided by the FLL-SOGI previously described. The constant K_{NS} is used to adjust the bandwidth of the filter, BW_{NS}, as shown in Equation (11). The notch filter allows getting a high enough crossover frequency of the voltage loop with no distortion of the grid injected current. Note that a fast enough DC-link voltage loop is crucial to keep the DC-link voltage within safe values in reduced size DC-links with low capacitance.

$$F_{NS}(s) = \frac{s^2 + {\omega_{NS}}^2}{s^2 + K_{NS} \cdot \omega_{NS} \cdot s + {\omega_{NS}}^2} \tag{10}$$

$$BW_{NS} \cdot 2\pi = K_{NS} \cdot \omega_{NS} \rightarrow K_{NS} = \frac{2\pi \cdot BW_{NS}}{\omega_{NS}} = \frac{100 \cdot 2\pi}{2 \cdot F_G \cdot 2\pi} = 1 \tag{11}$$

The Bode plots of $T_{VDC}(s)$ depicted in Figure 4a are those obtained when the notch filter, $F_{NS}(s)$, placed in series with $Gv_{DC}(s)$ isn´t used. The PI regulator $G_{VDC}(s)$ (9) has been tuned in order to achieve a crossover frequency F_{C_VDC} = 53 Hz, with a phase margin higher than 82° (PM > 82°) and a gain margin higher than 70 dB (GM > 70 dB). The system is stable but the attenuation at 100 Hz is just 5.5 dB. Therefore, the output of the voltage regulator has a remarkable low-frequency voltage ripple due to V_{DC_R}, thus producing a high distortion of the grid current.



(**a**) (**b**)

Figure 4. Loop gain frequency response of $T_{vDC}(s)$ @ I_{DC} = [0.2, 0.4, 0.6] A. C_{DC} = 50 µF: (**a**) without notch SOGI filter, (**b**) with notch SOGI filter.

Figure 4b shows the Bode plots of $T_{VDC}(s)$ when the notch filter is used in series with $G_{VDC}(s)$. In that case the value of F_{C_VDC} has slightly decreased (F_{C_VDC} = 46 Hz), getting high stability margins: PM > 52° and GM > 70 dB. The system is also stable, but the attenuation at 100 Hz is higher than 100 dB.

3.2. Control Scheme of the DC-DC Stage

The control structure of the DC-DC stage is depicted in Figure 5. It is composed by an outer digital voltage loop, regulating V_{PV}, in cascade with an analog peak current control (PCC) circuit, which sets the peak value of the current, I_{SW}, through the Flyback converter power transistor.

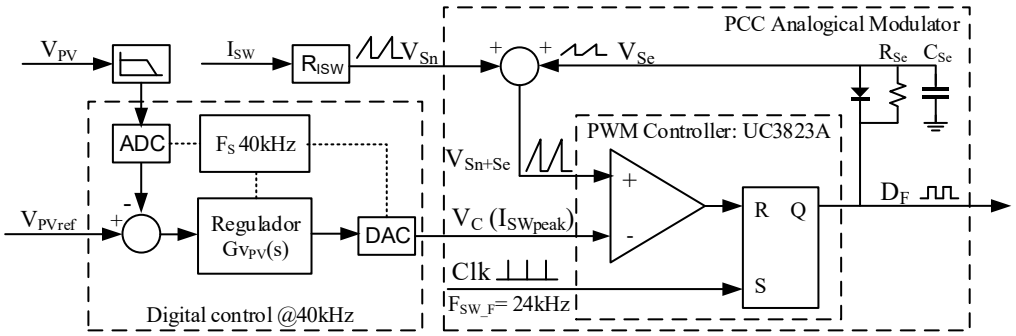


Figure 5. Flyback DC-DC PCC control scheme.

3.2.1. Peak Current Control of DC-DC Stage

The PCC control scheme shown in Figure 5 and has been designed following Reference [15]. This control structure is based on the cycle-by-cycle measurement of the current through the transistor, I_{SW}, of the DC-DC converter. The peak value of I_{SW} is limited by the control signal V_C. An external stabilization ramp signal, V_{Se}, is added to the sensed current signal, V_{Sn}. This method also provides protection for both the HF transformer and the power transistors against an eventual overcurrent.

The modulation index of the PCC, mc = 1 + Se/Sn (Equation (13)), is tuned by means of the slope Se of the external ramp V_{Se}. The value Se = 110 V/ms accomplishes a dynamic behaviour of $\hat{v}_{V_{PV}}/\hat{v}_C(s)$ close to that of a first-order system, as it can be observed from Figure 6a. The high V_{DC_R} ripple value produced by the low size of C_{DC} can change the operation point along the I–V curve of the PV source, degrading the MPPT performance. Therefore, a low susceptibility of V_{PV} to the ripple V_{DC_R} is required. The open loop susceptibility of V_{PV} to variations of V_{DC} (Equation (14)) at 100 Hz is lower than −41.5dB as shown in Figure 6b, therefore V_{DC_R}, that is 10% of V_{DC} (40 Vpp), causes a V_{PV} voltage ripple of 340 mVpp. It can be concluded that the 100 Hz ripple at V_{DC} has a low influence on the PV voltage. Therefore, the sensing of V_{PV} could be avoided and still a good MPPT would be obtained.

$$S_N = R_i \frac{V_{PV}}{L_m} \tag{12}$$

$$F_M = \frac{1}{(S_n + S_e)\cdot T_{SW\_F}} = \frac{1}{m_c \cdot S_n \cdot T_{SW\_F}} \tag{13}$$

$$A(s) = \left.\frac{\hat{v}_{V_{PV}}(s)}{\hat{v}_{DC}(s)}\right|_{\hat{v}_C=0} \tag{14}$$

3.2.2. PV Panel Voltage (V_{PV}) Control Loop in the Conventional MPPT

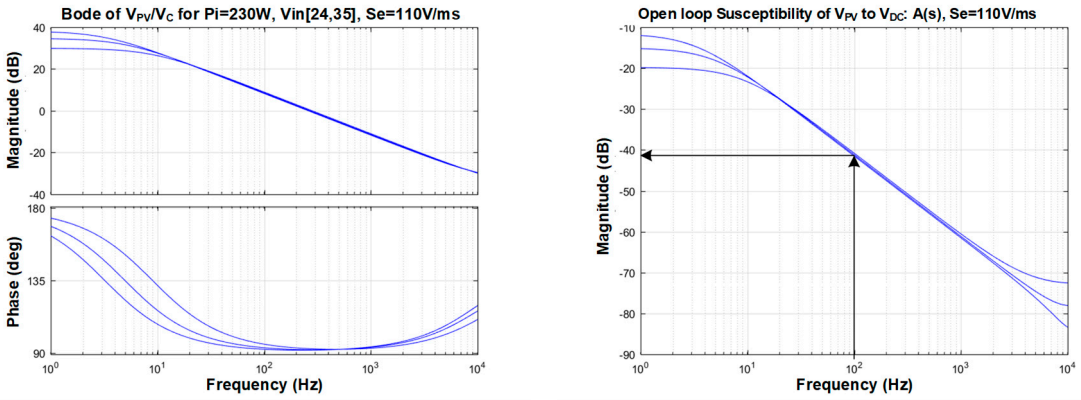
The reference of V_{PV} (V_{PVRef}) is updated at the sampling frequency of the MPPT, F_{MPPT}. The PV panel voltage control loop is implemented digitally and its control scheme is depicted in Figure 7. The sampling frequency of the control loop (Fs) is 40 kHz. This control loop is adjusted by means the PI regulator $G_{VPV}(s)$, whose values are shown by Equation (15). The crossover frequency, Fc_{VPV}, of the loop gain $T_{VPV}(s)$ must be much higher than F_{MPPT} so that V_{PV} can track V_{PVref}. The transfer function $\hat{v}_{V_{PV}}/\hat{v}_C(s)$ is the closed loop of the PCC and $\hat{v}_{V_{PV}}/\hat{v}_C(s)$ is the open loop susceptibility of V_{PV} to the variations of V_{DC}.

As it can be observed from the Bode plots of the loop $T_{VPV}(s)$ in Figure 8a, the crossover frequency Fc_{VPV} achieved by $G_{VPV}(s)$ is higher than 100 Hz. Therefore, an MPPT algorithm running at F_{MPPT} = 10 Hz is suitable Figure 8b shows that the presence of this control loop reduces the susceptibility $\hat{v}_{V_{PV}}/\hat{v}_{DC}(s)$ (16) at 100 Hz down to −55 dB, therefore the voltage ripple in V_{PV} caused by V_{DC_R} is 71 mVpp. Note that the use of a control loop of V_{PV} reduces the sensitivity of V_{PV} to the 100 Hz ripple

in V_{DC} in a factor of around 5: The ripple in V_{PV} is 71 mVpp with voltage loop compared with 340 mVpp with only PCC loop.

$$G_{VPV}(s) = -1.8345\left(\frac{s+350}{s}\right) \tag{15}$$

$$A_{CL}(s) = \left.\frac{\hat{v}_{PV}(s)}{\hat{v}_{DC}(s)}\right|_{\hat{v}_{PVRef}=0} \tag{16}$$



(**a**) (**b**)

Figure 6. Frequency response of the PCC: (**a**) closed loop $\hat{v}_{V_{PV}}/\hat{v}_C(s)$ response and (**b**) open loop susceptibility: A(s). $V_{PV} \in [24, 30, 35]$ V, P_{PV} = 230 W, Se = 110 V/ms.

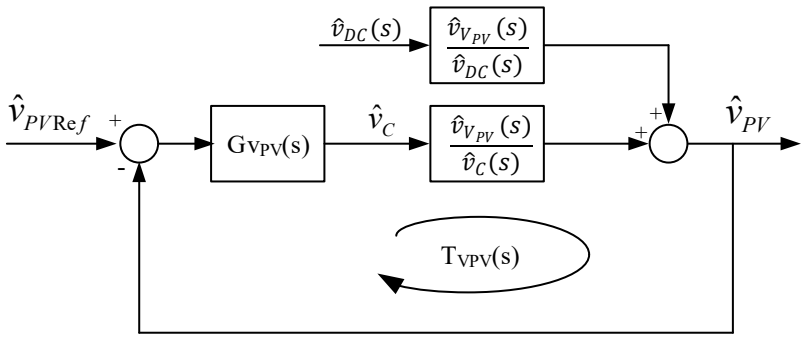
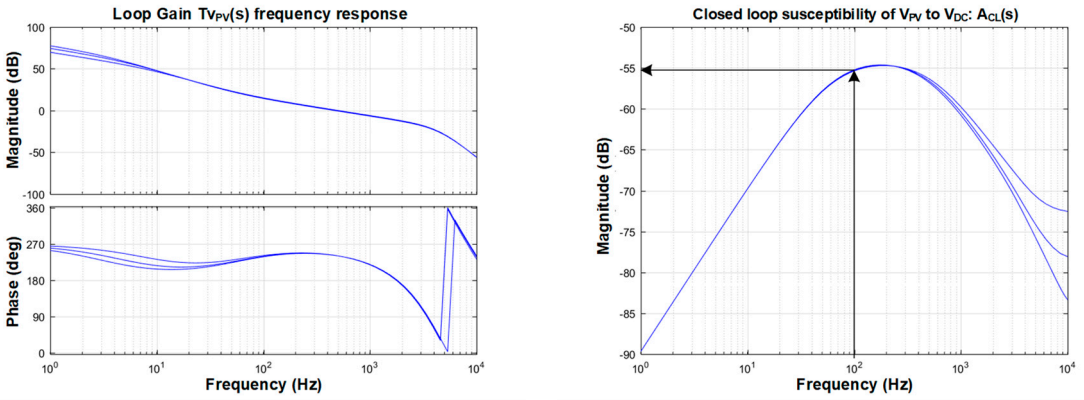


Figure 7. V_{PV} control loop.



(**a**) (**b**)

Figure 8. Frequency response of V_{PV} control loop: (**a**) $T_{VPV}(s)$ loop gain of the V_{PV} control loop and (**b**) closed loop susceptibility, $A_{CL}(s)$. V_{PV} = [24, 30, 35] V, P_{PV} = 230 W, Se = 110 V/ms.

4. MPPT Implementation without V_{PV} and I_{PV} Sensors

The conventional implementations of MMPT algorithms use current and voltage sensors to measure the voltage (V_{PV}) and the current (I_{PV}) of the PV source as it is shown in Figure 9. The use of voltage and current sensors increases the cost of the power converter. Sensorless MPPT algorithms have been developed [10–13] in order to reduce the number of sensors, yielding a cost reduction. In [11] a sensorless MPPT implementation based on the power balance at the DC-link was presented, which relies on the fact that the power injected into the grid (P_G) can be considered almost equal to the power extracted from the PV panels, $P_G \approx P_{PV}$. In that implementation, the reference of the current injected into the grid (I_G) is used as an estimation of P_G. This reference current depends on the control loop of V_{DC} so that the sampling frequency of the MPPT algorithm (F_{MPPT}) is limited by the dynamics of that loop. Besides, the reference of I_G is sensitive to the variations of the grid voltage and has a low-frequency ripple due to V_{DC_R}. Moreover, the method explained in Reference [11] is based on the assumption that the amplitude of the grid voltage is stable.

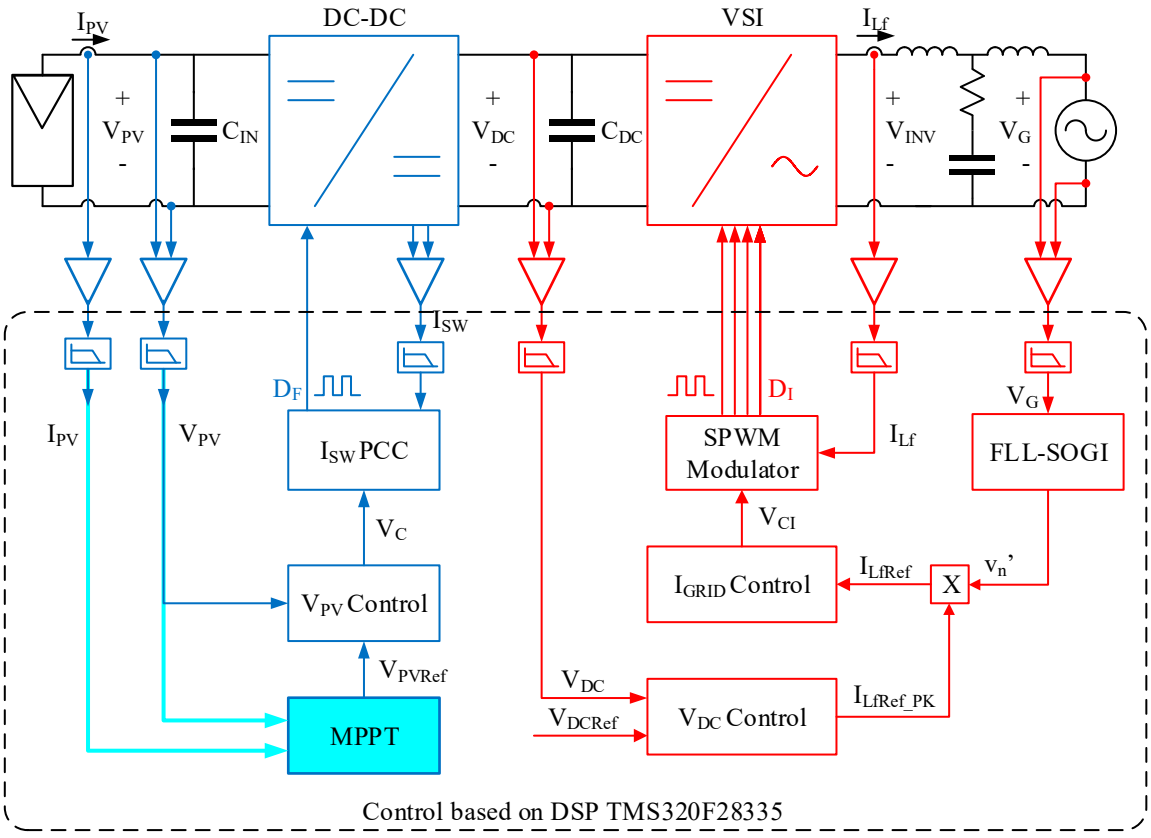


Figure 9. Conventional MPPT implementation.

A sensorless MPPT implementation shown in Figure 10 is proposed in this work. In this implementation, there is neither V_{PV} nor I_{PV} sensors and it is assumed that the power injected into the grid is almost equal to the power extracted from the PV panels, $P_G \approx P_{PV}$, as in Reference [11]. A novelty of this research is that it takes de advantages of the PCC of the DC-DC stage and some SOGI based enhancements applied to the control of the VSI stage to improve the performance of the MPPT implementation.

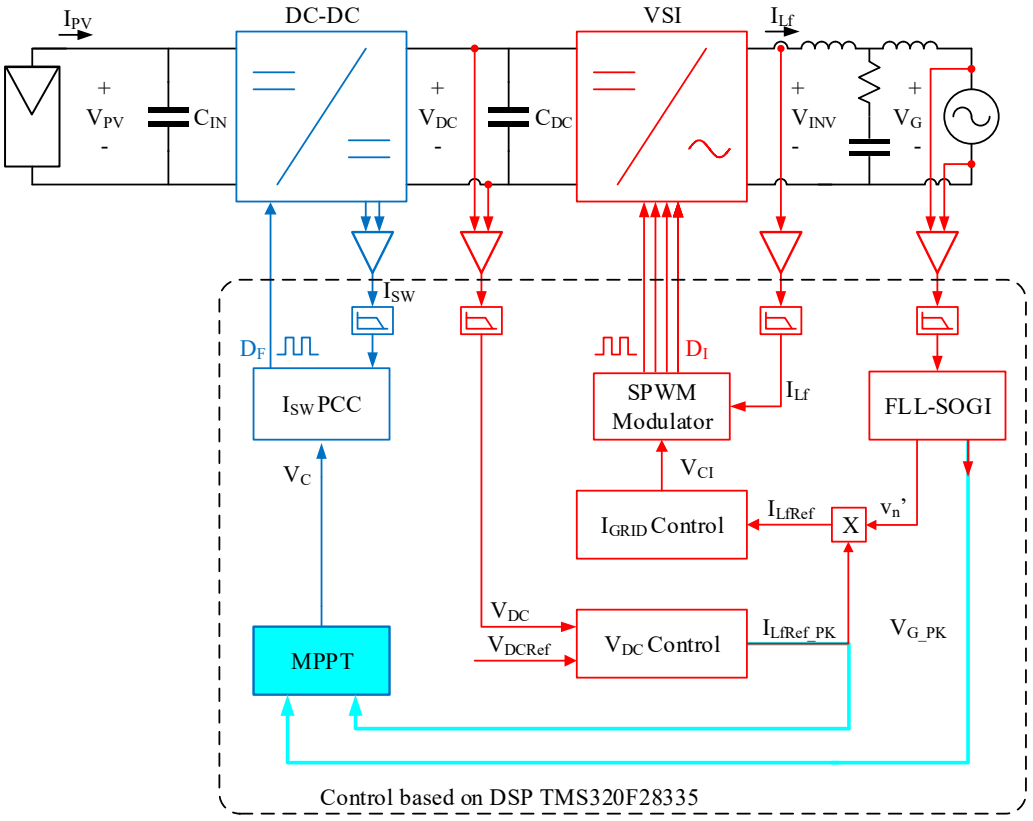


Figure 10. Proposed sensorless MPPT implementation.

A perturb and observe (P and O) algorithm [36] has been programmed in both the conventional (Figure 10) and the proposed sensorless (Figure 11) MPPT algorithms to compare the performance of both implementations. Both implementations use the grid frequency as a time-base to execute the MPPT algorithm. This technique increases the rejection of the disturbances caused by V_{DC_R}. In previous applications of a similar technique [12], the MPPT algorithm was executed at twice the grid frequency, but that sampling frequency is too fast for the control loops implemented in the proposed sensorless algorithm. In the present study, the MPPT algorithm was executed once every five cycles of the grid, yielding F_{MPPT} = 10 Hz.

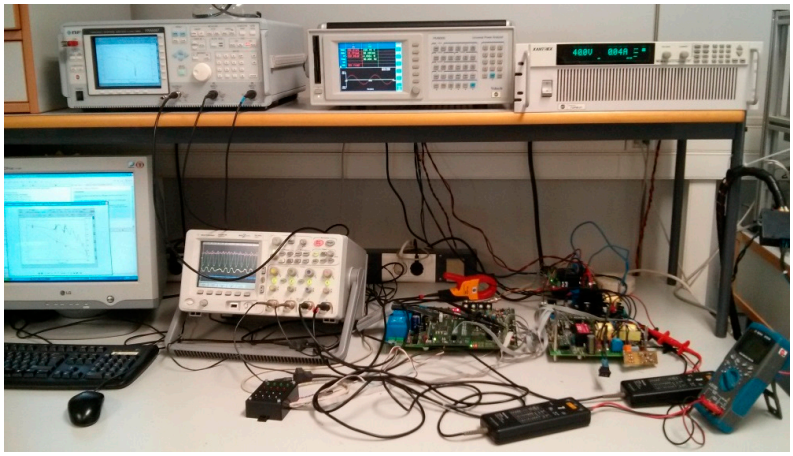


Figure 11. Experimental setup.

In the conventional implementation, the MPPT algorithm provides the reference of V_{PV} (V_{PV_Ref}) to the V_{PV} control loop. In the proposed sensorless MPPT, both the V_{PV} sensor and the V_{PV} control loop have been removed, so that the MPPT provides the reference Vc to the analog PCC.

4.1. Estimation of the Power Injected into the Grid in the Sensorless MPPT

The reference $I_{Lf\_Ref\_PK}$ is the peak value of the current injected into the grid, being proportional to P_G when the amplitude of the grid voltage is a static value. The signal $I_{Lf\_Ref\_PK}$ may have a remarkable low-frequency voltage ripple due to V_{DC_R}, thus producing a high distortion of the grid injected current along with a disturbance in the estimation of P_G. The SOGI based notch filter $F_{NS}(s)$ in series with the regulator $G_{VDC}(s)$ shown in Figure 3 is used to filter out that ripple. The use of the notch filter also enables a high crossover frequency of $T_{VDC}(s)$ without increasing the ripple in $I_{Lf\_Ref\_PK}$, which is useful to implement a fast MPPT algorithm. The crossover frequency of $T_{VDC}(s)$ is F_{C_VDC} = 45 Hz so that an MPPT of F_{MPPT} = 10 Hz can be implemented.

The estimation of P_G, P_{G_est}, depends on I_G and on the grid voltage RMS value (V_G) so that variations of V_G perturb the calculations of P_{G_est}. To overcome this issue, the value of the signal v'_{pk} is used to calculate the estimation of P_G as it is shown in Equation (17). The signal v'_{pk} is the amplitude of the fundamental of V_G and is provided by the FLL-SOGI, not requiring additional computational resources. The signal v'_{pk} has very low sensitivity to the distortion of the grid voltage because it is naturally filtered by the FLL-SOGI.

$$P_{G\_est} = \frac{v'_{pk}}{\sqrt{2}} \cdot \frac{I_{LfRef\_PK}}{\sqrt{2}} = \frac{v'_{pk} \cdot I_{LfRef\_PK}}{2} \approx P_{PV} \tag{17}$$

4.2. Implementation of the Perturb and Observe (P&O) Algorithm

The conventional MPPT algorithm uses the measurements of V_{PV} and I_{PV} to set the operation point of the PV source. The algorithm increases or decreases V_{PV_Ref} in perturbation steps of a value ΔV_{PV_Ref} to move the operation point along the I–V curve. In the sensorless implementation shown in Figure 10, instead of the measurements of V_{PV} and I_{PV}, the value of P_{G_est} expressed by Equation (17) was used. In Reference [11] it was proposed to manage the duty cycle of the switches (D_F) of the DC-DC to move the operation point along the I–V curve. In inverters with a reduced DC-link, the high susceptibility of V_{PV} to the ripple V_{DC_R} disturbs the operation point in the PV panel.

In the proposed sensorless MPPT, the value of I_{PV} is indirectly set by means of the reference signal of the PCC loop, Vc. The use of PCC has two functions: reducing the susceptibility of V_{PV} to the ripple V_{DC_R} and protecting the DC-DC converter from overcurrents.

The variable Vc is increased or decreased in small steps of a value ΔVc. It is worth pointing out that an increase of Vc causes an increase of I_{PV}, moving the PV operation point to the left of the I–V curve, whereas a decrease of Vc moves the PV operation point to the right of the I–V curve.

5. Results

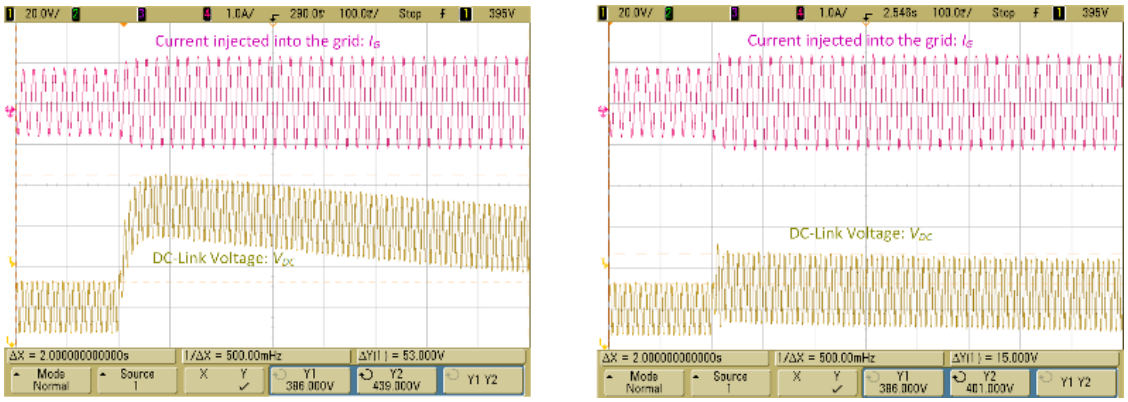
Figure 11 depicts the experimental setup. The laboratory tests have been performed using the two-stage inverter presented in Figure 1. The inverter under test was designed for connecting a single PV panel of 230 W to the single phase grid (230 V_{RMS} @ 50 Hz) and has a DC-link with the capacitance calculated in (1), C_{DC} = 50 μF. The challenge of using such a small value of C_{DC} is to keep a low distortion of the grid current and small transient overvoltages at the DC-link. The control of the two-stage inverter has been implemented digitally in a Texas Instruments TMS320F28335 DSP [30] at a sampling frequency (F_S) of 40 kHz.

The grid was emulated by means of a Cinergia GE&EL 50 grid emulator and electronic load. The voltage waveform was programmed according to the test waveform described in the international standard IEC-61000-4-7 [37], which has a value: THD_V = 1.2%. The PV panel has been emulated by means of an AMETEK TerraSAS ETS1000X10D PV simulator.

5.1. Control of the VSI

5.1.1. Transients of the DC-link Voltage

Figure 12 shows the transient response of the DC-link voltage (V_{DC}) and the current injected into the grid (I_G) when the PV power steps from 150 W up to 200 W. The results shown in Figure 12a were obtained with a crossover frequency $Fc_{\_VDC}$ = 10 Hz, yielding an overvoltage in V_{DC} of 53V from its steady-state value. The response in Figure 12b is obtained with a crossover frequency $Fc_{\_VDC}$ = 45 Hz. The response in Figure 12b was close to five times faster and the overvoltage is only 15 V, which represents a reduction of 72%.

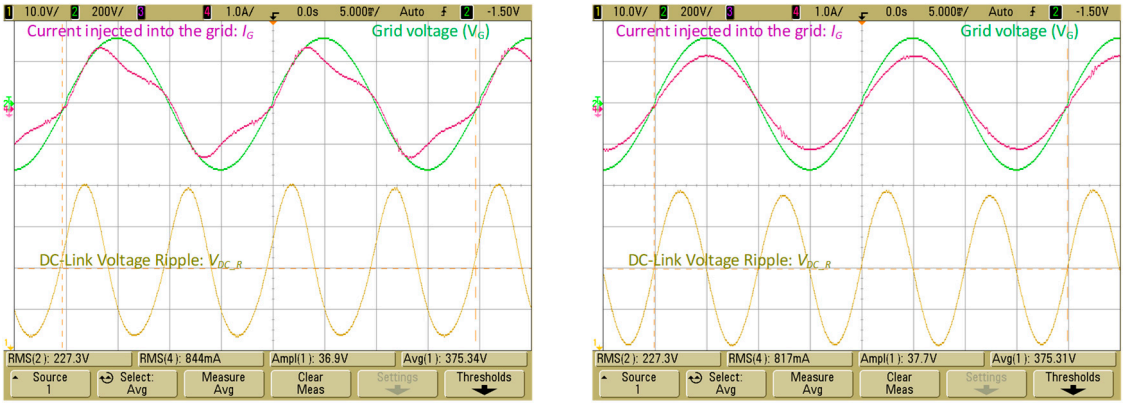


(**a**) (**b**)

Figure 12. Power step from 150 W to 200 W. C_{DC}: 50 µF. (**a**): Fc_{TVDC}: 10 Hz. (**b**): Fc_{TVDC}: 45 Hz.

5.1.2. Influence of the SOGI Notch in the Distortion of the Current Injected to the Grid

The increment of the crossover frequency $Fc_{\_VDC}$ involves a higher susceptibility to V_{DC_R}, which increases the harmonic distortion of the current injected into the grid (THDi). Figure 13 depicts the current injected into the grid (I_G) using two different regulators for controlling V_{DC}. In Figure 13b, the regulator $G_{VDC}(s)$ of the V_{DC} control loop is the PI shown in Equation (9) with a crossover frequency $Fc_{\_VDC}$ = 53 Hz. The waveform of I_G in Figure 13b was obtained using the same PI regulator, but in series with the SOGI notch filter $F_{NS}(s)$ shown in Equation (10), centered at 100 Hz. The crossover frequency has been slightly reduced, $Fc_{\_VDC}$ = 45 Hz, taking into account the addition of $F_{NS}(s)$.



(**a**) (**b**)

Figure 13. THDi of the current injected into the grid at P_G = 200 W. Grid: EN-61000-4-7 (1.2% THDv). $Fc_{\_VDC}$ = 50 Hz. (**a**): PI Reg.: $Gv_{DC}(s)$. (**b**): PI Reg. + Notch filter: $Gv_{DC}(s) + F_{NS}(s)$.

Both tests have been performed injecting 200 W to the grid. The controller of the current injected into the grid (I_G) is formed by the P+R regulator in series with the HC expressed by Equation (6). The resulting values of the THDi are 21.51% and 0.96%, respectively. This result indicates the effectiveness of the notch filter for reducing the THDi in spite of the small DC-link.

The following tests of the THDi have been performed for values of P_G in the range P_G = [40, 180] W. The results are shown in Figure 14. The purple trace represents the values of THDi obtained without the SOGI notch $F_{NS}(s)$ and the green trace represents the values obtained with $F_{NS}(s)$. The THDi without notch varies from 21.51% to 22.43%, clearly exceeding the limits of the IEEE519 standard [4] (5%), shown by the red line. The values of the THDi obtained with $F_{NS}(s)$ vary from 0.96% to 3.14%, widely complying with IEEE519 in the whole range of P_G values. In all the measurements the distortion of the grid voltage is THDv = 1.2%.

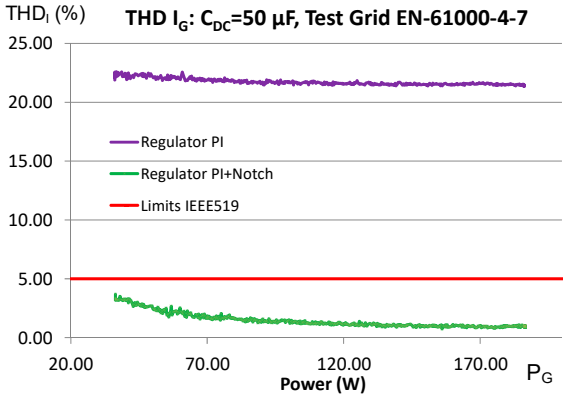


Figure 14. THD of I_G. Grid: EN-61000-4-7 (1.2% THDv). Linear sweep of power injected into the grid (P_G) from 40 W to 180 W at grid frequency F_G = 50 Hz.

5.1.3. Loop Gain Measurement

The loop gain $T_{VDC}(s)$ has been validated by means of loop gain measurement procedures [38–40]. The setup of the test is shown in Figure 15. An NF FRA5097 frequency response analyzer (FRA) is configured to perform an AC sweep from 2 Hz to 20 kHz. The signal generated by the oscillator of the FRA (v_{OSC_A}) is acquired by the DSP, which carries out the control of the inverter through an internal 12-bit ADC. The acquired signal (v_{OSC}) was digitally injected into the control loop as a perturbation. Both, v_{DC} and v_{DC}+v_{OSC} signals were adapted digitally to be loaded into the pulse width modulation (PWM) unit of the DSP. The offset of the signals was removed through digital high pass filters, and then the amplitudes are digitally adjusted to maximize the resolution of the PWM. The PWM signals $(v_{DC})_{PWM}$ and $(v_{DC} + v_{OSC})_{PWM}$ were measured by the FRA. The PWM signals were filtered by the FRA through its internal tracking filter. The loop gain measurement of $T_{VDC}(s)$, shown in Figure 16,was performed at P_G = 230 W. The results show the similarity between the experimental and theoretical Bode plots of $T_{VDC}(s)$.

5.2. MPPT

The performance of the sensorless "perturb and observe" (P and O) MPPT algorithm presented in this study has been compared to a conventional implementation, which uses sensors to measure V_{PV} and I_{PV}. The experimental tests have carried out to measure the start-up time until the maximum power point (MPP) was reached, and the performance at the MPPT under irradiation transients. All the tests were performed with an MPPT sampling frequency, F_{MPPT} = 10 Hz. The perturbation step value programmed in the conventional implementation was ΔV_{PV_Ref} = 300 mV. In the sensorless MPPT the perturbation step was ΔVc = 12.5 mV, which corresponds to a 250 mA step in I_{PV} in the operation region close to the MPP. It is worth pointing out that different values are perturbed in both

MPPTs (either V_{PV_Ref} or ΔVc) and that the DC-DC converter operates in discontinuous conduction mode. Both facts prevent finding an equivalent value of the perturbation step in both MPPTs.

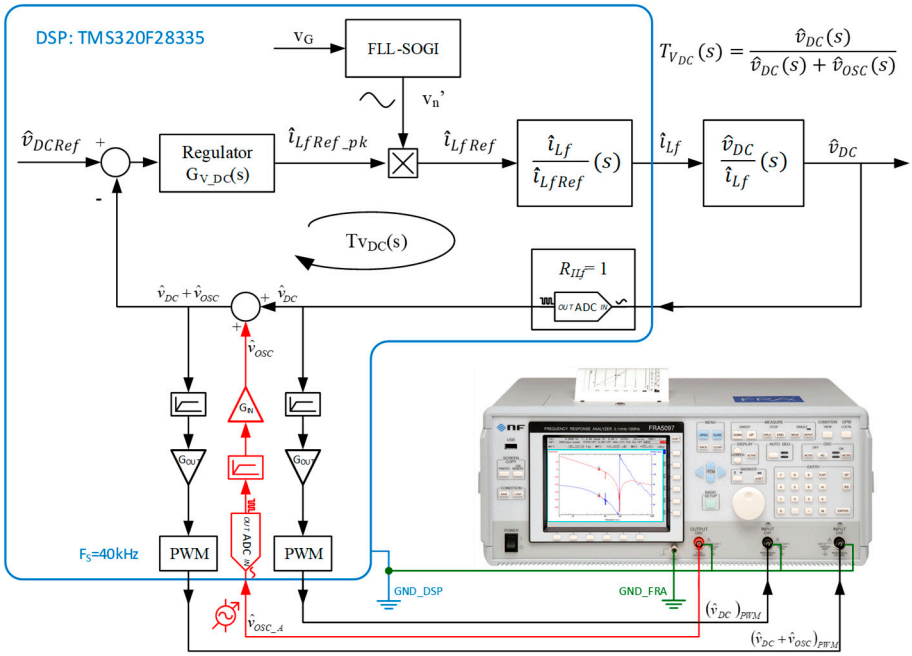


Figure 15. Loop gain measurement setup.

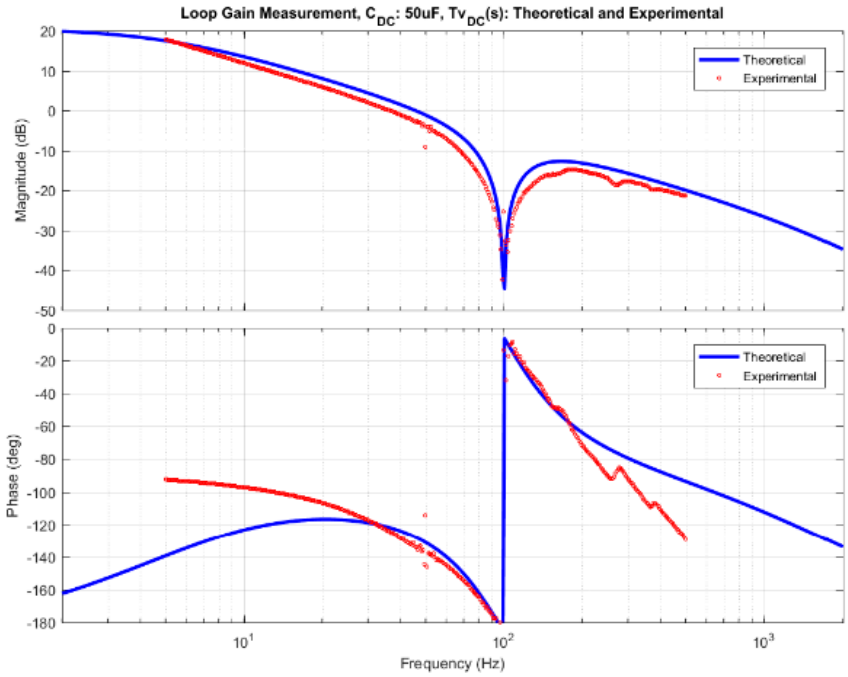


Figure 16. Loop gain frequency response of $Tv_{DC}(s)$. P_G = 230 W, C_{DC} = 50 µF. Blue: theoretical, red: experimental.

5.2.1. Start-up Time to Reach the MPP

Figure 17 shows the evolution of the operation point at the PV source (V_{PV}, I_{PV} and P_{PV}) from the start-up until the MPP was reached. The conventional implementation was faster (2.75 s) than the sensorless (12.6 s) due to the differences in the perturbation step, but once the MPP is achieved, both implementations continue at the MPP.

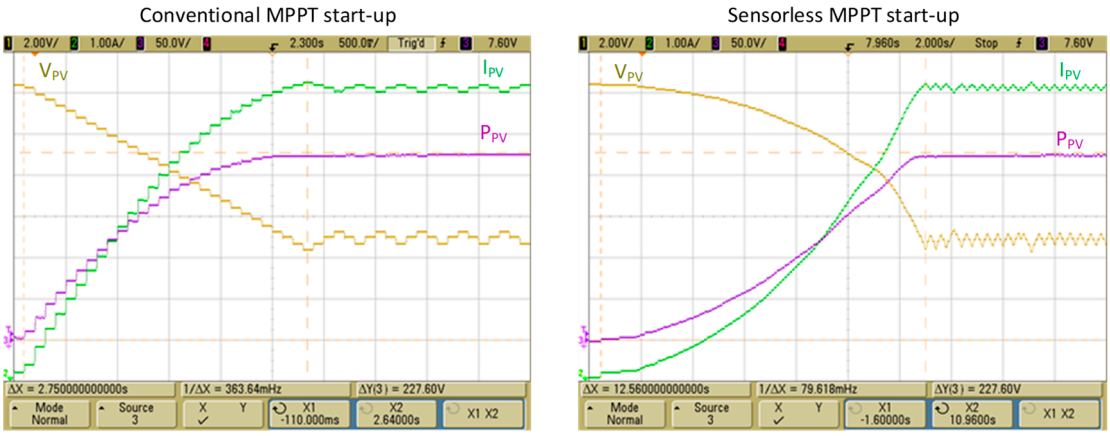


Figure 17. MPPT response from the start-up until the MPP is reached. F_{MPPT}: 10 Hz. (**a**): Conventional, V_{PV} step: ΔV_{PV_Ref} = 300 mV. (**b**): Sensorless, PCC Vc step: ΔVc = 12.5 mV (≈250 mA close to the MPP).

5.2.2. MPPT Performance Close to the MPP

A key factor in the MPPT performance is the accuracy of the PV estimation and the dispersion of the operation point from the MPP along the I–V curve. The results shown in Figure 18 were obtained tracking the MPP of the 230 W PV panel at constant irradiation of 1000 W/m^2 during 50 s. The results in Figure 18a correspond to the conventional MPPT algorithm and the results in Figure 18b correspond to the sensorless algorithm. In both implementations, the operation points are very close to the MPP. The power extracted from the PV panel during the tests is shown in Table 4. In order to calculate the MPP tracking performance, the quotient between the average power and the peak power measured in each experiment has been used as a reference, as it is expressed by Equation (18). Although the sensorless algorithm presents a very slight disadvantage (0.06%) in terms of the tracking efficiency, the performance of both methods is almost the same.

$$\text{Tracking efficiency} = \frac{\text{Average Power}}{\text{Peak Power}}. \tag{18}$$

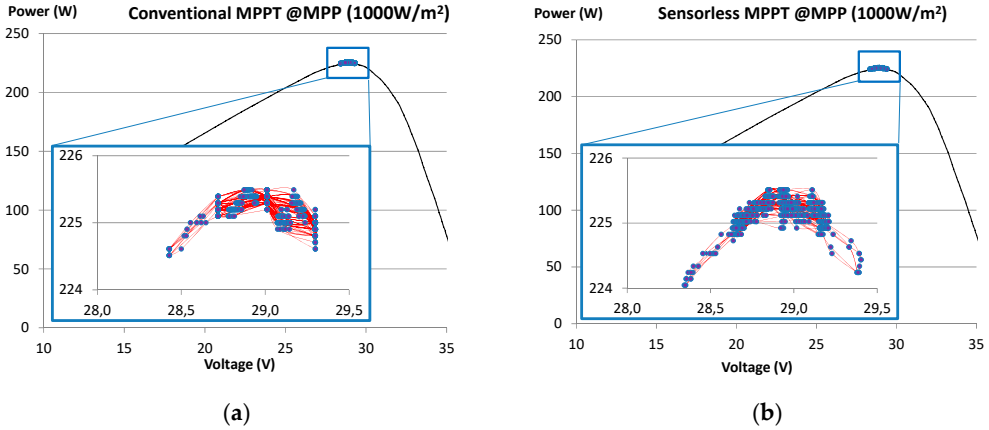
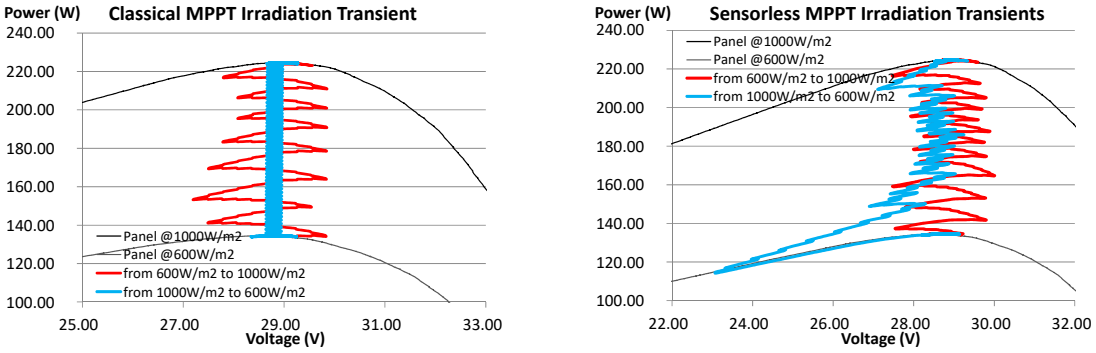


Figure 18. Dispersion of the operation point near the MPP. Total test time: 50 s. F_{MPPT} = 10 Hz. (**a**): Conventional, V_{PV} step: ΔV_{PV_Ref} = 300 mV. (**b**): Sensorless, PCC Vc step: ΔVc = 12.5 mV (≈250 mA near the MPP).

Table 4. Performance of the MPPT algorithms at the MPP under constant irradiation (1000 W/m^2).

MPPT Implementation	Conventional	Sensorless
Average power (W)	225.30	224.80
Peak power (W)	225.49	225.11
Tracking efficiency (%)	99.92	99.86

The tracking of the MPP under heavy irradiation transients is shown in Figure 19. The tests have been performed for 50 s following the stages shown in Table 5. The black traces are the IV curve of the PV panel at 1000 W/m^2 and 600 W/m^2. The blue traces represent the evolution in stage 2, during the reduction of the irradiation, and the red trace represents the evolution in stage 4, during the increase of irradiation.



(**a**) (**b**)

Figure 19. Irradiation transients test. Total time: 50 s. F_{MPPT} = 10 Hz. (**a**) Conventional, V_{PV} step: ΔV_{PV_Re} = 300 mV. (**b**) Sensorless, PCC Vc step: ΔVc = 12.5 mV (≈250 mA near the MPP).

Table 5. Stages of the transient radiation test.

Stage	Irradiation Profile	Duration
1	Constant at 1000 W/m^2	10 s
2	Linear decrease from 1000 W/m^2 to 600 W/m^2	10 s
3	Constant at 600 W/m^2	10 s
4	Linear increase from 600 W/m^2 to 1000 W/m^2	10 s
5	Constant at 1000 W/m^2	10 s
Total	-	50 s

The power extracted from the PV panel during the tests is shown in Table 6. During stages 1, 3 and 5, both MPPTs tracked the MPP as was expected from the results shown in Table 4. During stage 2, the sensorless MPPT was not as accurate as the conventional one, but during stage 4 the sensorless MPPT exhibited a smaller dispersion of the operation point and, thus, a higher accuracy than the conventional one. It can be stated that the MPPT performance of both MPPTs was highly similar. Although the conventional MPPT had a faster start-up and was slightly more accurate in some tests, the performance of the proposed sensorless MPPT near the MPP was almost equal to the conventional implementation, but at a lower cost.

Table 6. Transient radiation test results.

Stage	Conventional MPPT	Sensorless MPPT	%
1	225.30 W	224.80 W	0.998
2	181.27 W	173.51 W	0.957
3	134.90 W	134.41 W	0.996
4	180.82 W	180.36 W	0.997
5	225.30 W	224.80 W	0.998
Average	189.52 W	187.58 W	0.989

6. Conclusions

This paper focused on control techniques which help to reduce the cost of two-stage grid-connected PV inverters. In previous works, sensorless algorithms and techniques to reduce the capacitance of the DC-link have been proposed separately. The present study attempts to integrate both trends in a single implementation. The reduction of the DC-link capacitance requires a faster control loop to keep the DC-link voltage within safe values. However, this practice usually increases the THD of the current injected into the grid. The DC-link can be reduced in a factor of ten compared to standard values of the DC-link capacitance, yet with good values of the THDi, by increasing the speed of the voltage control loop and using a frequency adaptive notch filter tuned at twice the grid frequency.

SOGI structures are an effective way to implement tuned filters both in the inverter voltage loop and in its current loop. It is shown that the crossover frequency of the DC-link voltage control loop can be increased from typical values of 10 Hz to a value around 50 Hz, yet getting a THDi value lower than 1%. The combination of a fast voltage loop with a SOGI notch filter allows the reduction of the DC-link capacitance. An FLL-SOGI is used to get the value of the grid frequency to tune the SOGI controllers in the inverter control loops.

Summing up, this study proposes the implementation of the MPPT with no sensors at the PV source side, which takes advantages of the SOGI based enhancements implemented in the control of the converter. The high dynamics achieved by the inverter controllers yield a performance of the sensorless MPPT very similar to that of conventional MPPT implementations, but at a lower cost.

Author Contributions: R.G.-M., G.G. and E.F. proposed the main idea, performed the investigation and designed the experiments; R.G.-M. and G.G. developed the software, performed the experiments, and wrote the paper. M.L. and S.M. processed the data from the experimental results and reviewed the paper. G.G. and E.F. lead the project, acquired the funds for research.

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Appendix A

Table A1 shows the approximated costs of the prototype built for this study at the present time. It is important to note that a 6% cost saving is estimated.

Table A1. Approximate costs of the prototype.

Implementation	Conventional	Sensorless and Reduced DC-link	
PCB	100 €	100 €	100 €
Common components	400 €	400 €	400 €
DC-link	Electrolytic 500 µF 12 €	Electrolytic 50 µF 5 €	Film 50 µF 7 €
V_{PV} and I_{PV} sensors	25 €	0 €	0 €
Total	537 €	505 € (94%)	507 € (94.4%)

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