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Field-programmable photonic arrays

DANIEL PÉREZ, IVANA GASULLA, AND JOSE CAPMANY*

ITEAM Research Institute, Universitat Politècnica de València, Camino de Vera 46022 Valencia, Spain
**jcapmany@iteam.upv.es*

Abstract: We propose a new programmable integrated photonic device, the Field Programmable Photonic Array, which follows a similar rationale as that of Field Programmable Gate Arrays and Field Programmable Analog Arrays in electronics. This high-level concept, basic photonic building blocks, design principles, and technology and physical implementation are discussed. Experimental evidence of its feasibility is also provided.

1. Introduction

Programmable Multifunctional Photonics (PMP) seeks the design of common integrated optical hardware configurations, which can implement a wide variety of functionalities by suitable programming [1–10]. Several authors [6,7,9,10] have reported theoretical work proposing different configurations and design principles for programmable circuits based on the cascade of either beamsplitters [7,9,10] or integrated Mach Zehnder Interferometers [6] (MZIs). These proposals offer versatile hardware solutions to the implementation of programmable circuits but none of them defines a complete architectural solution of a photonics device that could be programmed for the implementation of arbitrary simple, complex or even simultaneous circuits.

In electronics, this concept is sustained by Field Programmable Gate Arrays (FPGAs) [11,12] and Field Programmable Analog Arrays (FPAAs) [13–16] and following a similar rationale behind the principles of these devices we propose here the implementation of a similar concept in integrated photonics, that can be realized by combining a set of *Programmable Photonics Analog Blocks* (PPABs) and a set of *Reconfigurable Photonic Interconnects* (RPIs) implemented over a photonic chip. This element, which we call Field Programmable Photonic Array (FPPA), can be able of implementing one or various simultaneous photonics circuits and/or linear multiport transformations by the appropriate programming of its resources (i.e. PPABs and RPIs) and the selection of its input and output ports. We first provide in Section 2 the high level description of the FPPA concept and the minimum basic functionalities that both building blocks, PPABs and RPIs need to provide. In Section 3 we provide a general discussion on the design flow and technology mapping of FPPAs. Physical implementation is addressed in section 4 showing that the main FPPA layouts can be implemented using integrated waveguide meshes. Section 5 provides some experimental results to support the proposed concept and finally Section 6 provides a discussion on limiting factors and concludes the paper.

2. High-level concept and building blocks

2.1 High-level concept

The high-level concept of the proposed FPPA is schematically shown in Fig. 1. It consists of a set of PPABs and RPIs implemented through an array of photonic waveguide elements grown on a photonic chip substrate. The waveguide elements that composed the RPIs have programmable features as well and can propagate light in both directions. Note that the layout in Fig. 1 does not presuppose any particular waveguide array geometry and that the square layout depicted there is just for illustration purposes.

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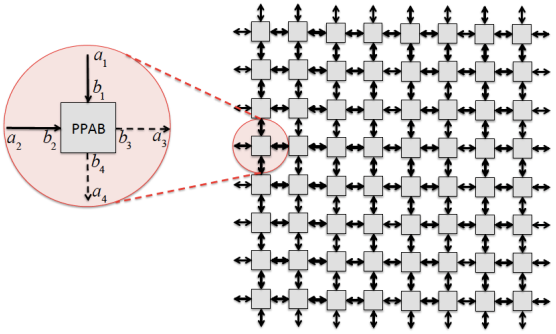

Fig. 1. Schematic diagram example of the proposed FPPA device. The zoom shows a detail of the Programmable Photonic Analog Block as it pertains to the left-up to right-bottom direction of propagation.

2.2 Programmable photonic building blocks

Although several configurations can be considered for the PPAB, here we shall illustrate the concept with a reciprocal, lossless and time reversible 2x2 coupler (2 input ports/2 output ports PPAB units). The scheme of such PPAB is shown in the inset of Fig. 1 for a particular axis orientation and with no internal coupling paths. In general, we will consider 4 options obtained from this configuration by rotating 0°, 90°, 45° and –45° and denote them as type A, B, C, and D, respectively. Figure 2 shows these possible options. The high-level role of the PPAB is to provide tunable independent power coupling ratios and phase shifts as explained below.

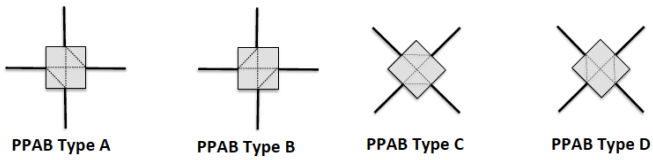

Fig. 2. Four types of 2x2 PPAB units considered and their internal signal coupling layouts shown in broken lines.

The standalone operation of the PPAB is illustrated in Fig. 3 for the Type A case (the description for the other types follows the same line of reasoning). Figure 3 shows the layout of the Type A PPAB with indication of the optical fields at the input and output ports (b_1, b_2, b_3, b_4) and the external fields at the input/output RPI elements enclosing the PPAB (a_1, a_2, a_3, a_4).

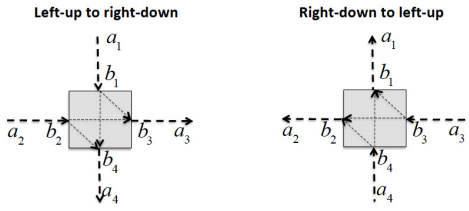

Fig. 3. Type A PPAB unit including the internal and external optical fields at its ports for the two directions of signal propagation.

The PPAB is a 2x2 photonic component that is capable of independently setting a common tunable phase shift Δ_{PPAB} and a tunable optical power splitting ratio K among its input optical waveguide input fields b_1, b_2 and its output optical waveguide output fields b_3, b_4. Two propagation directions are possible as shown in the figure, the first is from the Left

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and up ports to the to Right and down ports and is characterized in the case of implementing the PPAB with a 3-dB tunable coupler by the following transmission matrix:

$$\begin{pmatrix} b_3 \\ b_4 \end{pmatrix} = -je^{j\Delta_{PPAB}} \begin{pmatrix} \sin\theta & \cos\theta \\ \cos\theta & -\sin\theta \end{pmatrix} \begin{pmatrix} b_1 \\ b_2 \end{pmatrix}, \quad (1)$$

where both $K = cos^2\theta$ and Δ_{PPAB} can be changed by means of two external (electronic, mechanic, acoustic) control signals through a linear relationship. Note that other versions of the 2x2 matrix are possible for other implementations of the 2x2 unit, for example, using a tunable directional coupler. The second is from the *Right and down ports to the to Left and up ports* and is characterized by the following transmission matrix:

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = -je^{j\Delta_{PPAB}} \begin{pmatrix} \sin\theta & \cos\theta \\ \cos\theta & -\sin\theta \end{pmatrix} \begin{pmatrix} b_3 \\ b_4 \end{pmatrix}. \quad (2)$$

Figure 4 shows some examples of simple programming of the Type A PPAB leading to very basic operations required in photonic signal processing.

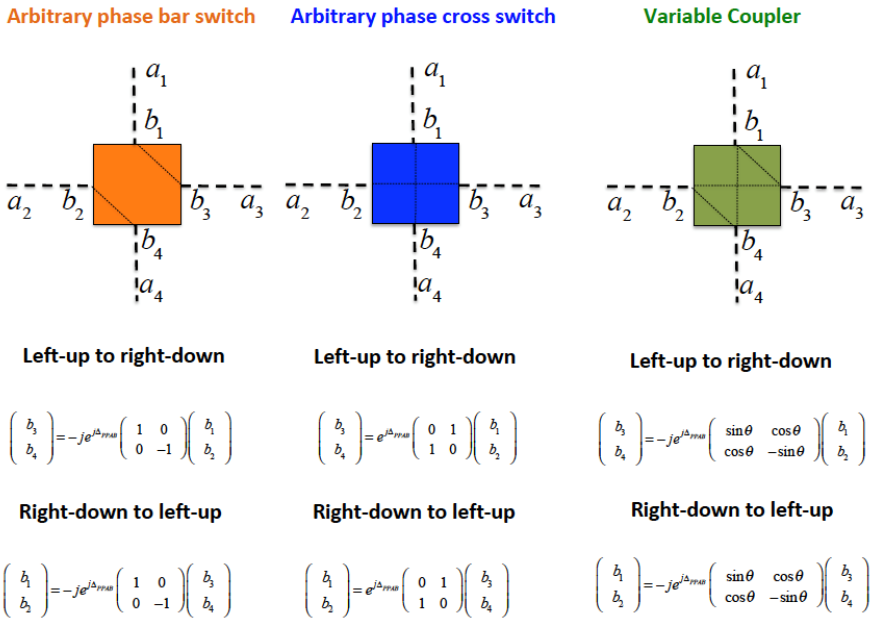

Fig. 4. Different functionality programming, resulting transmission matrices and associated code colors for a Type A PPAB.

Note that in addition to the functionalities displayed, the PPAB can operate in conjunction with an RPI as a phase shifter, as shown in the next section. Similar operation modes and color codes can be defined for type B, C, and D PPABs.

2.3 Reconfigurable photonic interconnects

The RPI elements are assumed to provide a lossless tunable phase shift and their combination with the PPAB elements provide an extra degree of flexibility in the 2x2 transmission matrix. Figure 5 shows this feature for a Type A PPBA element under propagation from Left and up ports to Right and down ports (similar procedure can be established for the reverse propagation direction and for PPBA types B, C and D). The optical waveguide RPI elements can provide independent and tunable differential phase shifting ϕ over a common value Δ_{RPI}

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in the two input and/or output waveguides accessing the PPAB. For instance, and referring to the upper part of Fig. 5:

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} e^{j(\phi+\Delta_{RPI})} & 0 \\ 0 & e^{j\Delta_{RPI}} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} = e^{j\Delta_{RPI}} \begin{pmatrix} e^{j\phi} & 0 \\ 0 & 1 \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}. \tag{3}$$

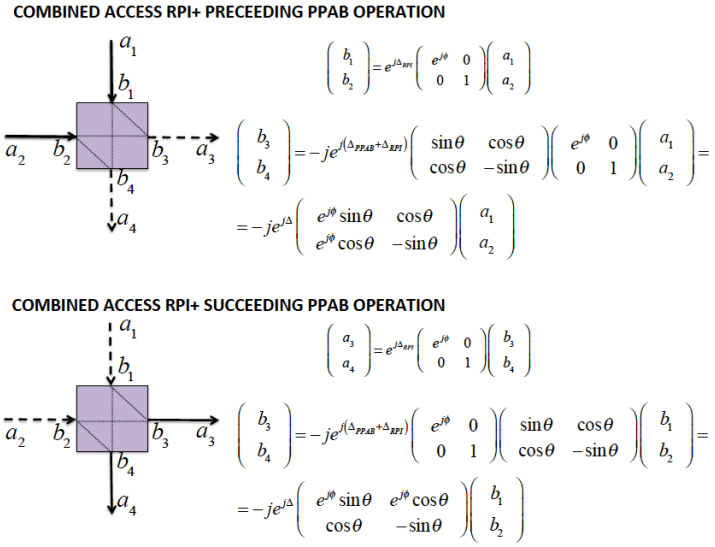

Fig. 5. Combined operation of a PPAB and an RPI for operation as a phase shifter.

The combined action of a PPAB element and its preceding RPI element can then be cast as follows:

$$\begin{pmatrix} b_3 \\ b_4 \end{pmatrix} = -je^{j(\Delta_{PPAB}+\Delta_{RPI})} \begin{pmatrix} \sin\theta & \cos\theta \\ \cos\theta & -\sin\theta \end{pmatrix} \begin{pmatrix} e^{j\phi} & 0 \\ 0 & 1 \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} = \\ = -je^{j\Delta} \begin{pmatrix} e^{j\phi}\sin\theta & \cos\theta \\ e^{j\phi}\cos\theta & -\sin\theta \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}, \tag{4}$$

where the common phase factor is given by $\Delta_{PPA} = \Delta_{RPI} + \Delta_{PPAB}$.

In a similar way, the combined action of a PPAB element and its succeeding RPI element (shown in the lower part of Fig. 5) is given by:

$$\begin{pmatrix} a_3 \\ a_4 \end{pmatrix} = -je^{j(\Delta_{PPAB}+\Delta_{RPI})} \begin{pmatrix} e^{j\phi} & 0 \\ 0 & 1 \end{pmatrix} \begin{pmatrix} \sin\theta & \cos\theta \\ \cos\theta & -\sin\theta \end{pmatrix} \begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \\ = -je^{j\Delta} \begin{pmatrix} e^{j\phi}\sin\theta & e^{j\phi}\cos\theta \\ \cos\theta & -\sin\theta \end{pmatrix} \begin{pmatrix} b_1 \\ b_2 \end{pmatrix}. \tag{5}$$

3. FPPA core architectures, design flow, and technology mapping

It is by adequate concatenation of successive RPI + PPAB and/or PPAB + RPI units into core architectures and subsequent programming that complex standalone and/or parallel photonic circuits and signal processing transformations can be implemented by the FPPA. This process entails a design flow stage and a technology mapping.

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3.1 Core architectures

Figure 6 depicts three generic layouts of FPPA cores built upon assembling RPI + PPAB and/or PPAB + RPI units. Figures 6(a) and 6(b) show the layouts of a square type FPPA design. Here, type A and type B PPAB elements are interleaved in every column and row of the device. We denote this design by class ABAB. A second class is obtained by combining columns of interleaved AB PPABs and columns of type C PPABs, we denote this class, shown in Fig. 6(c), by ABCC. Finally, Fig. 6(d) shows the layout of class ABDD obtained by combining columns of interleaved AB PPABs and columns of type D PPABs. More classes, which are not shown here, lead to non-uniform FPPA design patterns, defined by suitable combinations of different types of PPAB elements. In section 4 on physical implementation, we provide further discussion on these.

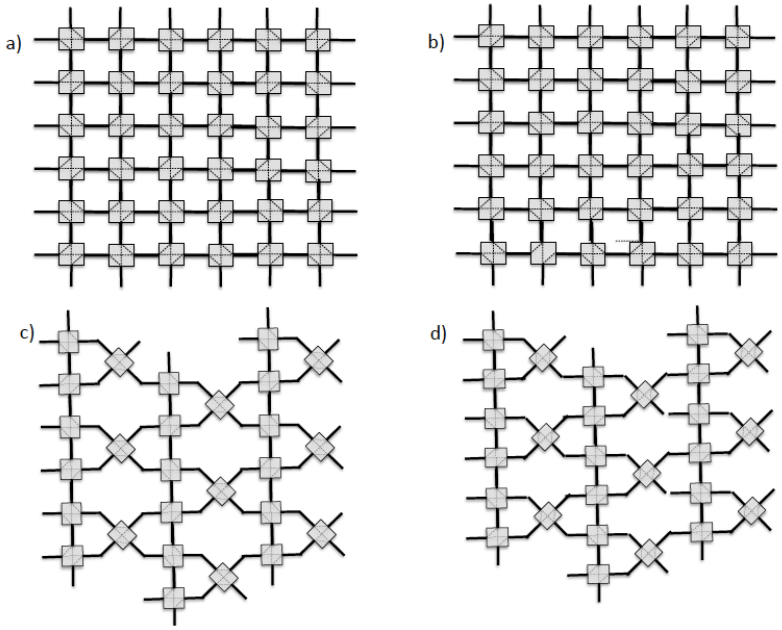

Fig. 6. (a) and (b) Layouts of class ABAB FPPAs. (c) Layout of a class ABCC FPPA. (d) Layout of a class ABDD FPPA.

3.2 Design flow and technology mapping

The most general type of programmable devices consists of an array of uncommitted elements that can be interconnected according to a user's specifications and configured for a wide variety of applications. An FPPA combines the programmability of the most basic reconfigurable photonic integrated circuits in a scalable interconnection structure, allowing programmable circuits with much higher processing density. Thus, processing complexity comes from the interconnectivity.

The left part of Fig. 7 shows the main steps of the design flow process, which we now describe. The starting point for the design flow is the initial application entry or circuit configuration to be implemented. The specifications are then processed to optimize the area and performance of the final circuit. Then, specifications are transformed into a compatible circuit of FPPA processing blocks (technology mapping), optimizing attributes such as delay, performance or number of blocks.

The technology mapping phase transforms the optimized network into a circuit that consists of a restricted set of circuit elements (FPPA processing blocks). This is done selecting a set from the available PPABs and specifying how these will be interconnected.

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This interconnection step implies the setting of several RPI elements physically connecting the selected PPABs. This determines the total number of processing blocks (PPABs and RPIs) to be activated by programming. In a second stage, the processing block configurations (i.e. types of PPABs and RPIs) are chosen and performance calculation and design verification are carried out. This can be done either physically by feeding all the necessary configuration data to the programming units to configure the final chip or, more commonly, by iteratively employing accurate models of the FPPA in the software plane.

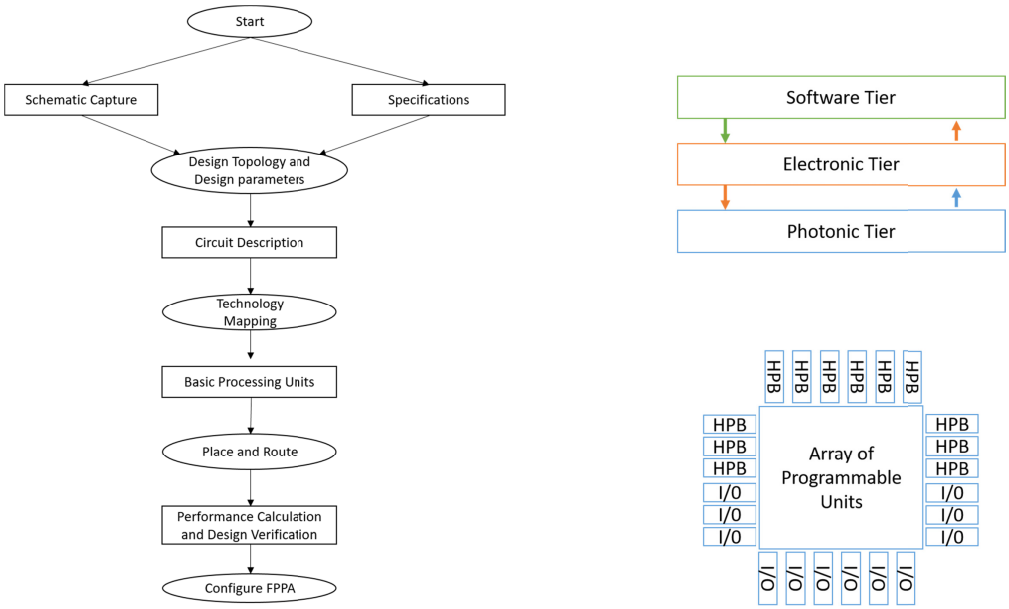

Fig. 7. (Left): main steps involved in the design flow of a FPPA device. (Right): FPPA soft and hard tiers and expanded layout including peripheral high-performance blocks.

The next step assigns each processing block to a specific location in the FPPA core including, as well, the choice of the processing units that route the input signals to the core to the input/s of the programmed circuit and the output/s of the programmed circuit to the core outputs. Note that in contrast to FPGAs [12,13], this structure does not physically differentiate between processing blocks and interconnection resources.

From the aforementioned description, it can be appreciated that the FPPA device involves considering not only the physical hardware of the photonic and control electronic tier, but also a software layer (see upper right part of Fig. 7). The steps contained in the generic design flow can be done automatically either by the software layer, the user, or by a mixture of both, depending on the autonomy and the capabilities of the FPPA. In addition, a failure in any of the steps will require an iterative process till the specifications are accomplished successfully. Additional parallel optimization process (mainly self-winding), enable robust operation, self-healing attributes and additional processing power to the physical device.

Similarly to modern FPGA families, FPPA can include peripheral high-performance blocks (HPB) to expand its capabilities to include higher-level functionality fixed into the chip. This is shown schematically in the lower right part of Fig. 7. Having these common functions embedded into the chip reduces the area required and gives those functions increased performance compared to building them from primitives. Moreover, some of them are impossible to be obtained by a discretized version of basic processing blocks. Examples of these include high-dispersive elements, generic modulation and photo detection subsystems, optical amplifiers and source subsystems and high-performance filtering structures to cite a few.

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3.3 Circuit programming examples

Figures 8, 9 and 10 provide some examples where FPPAs of different types are programmed to emulate and implement simultaneously different photonic circuits. In each case, the figure includes the FPPA layout with colored PPBAs according to the code: orange: bar switch, blue: cross switch, green: variable coupler, and the layouts of the implemented circuits.

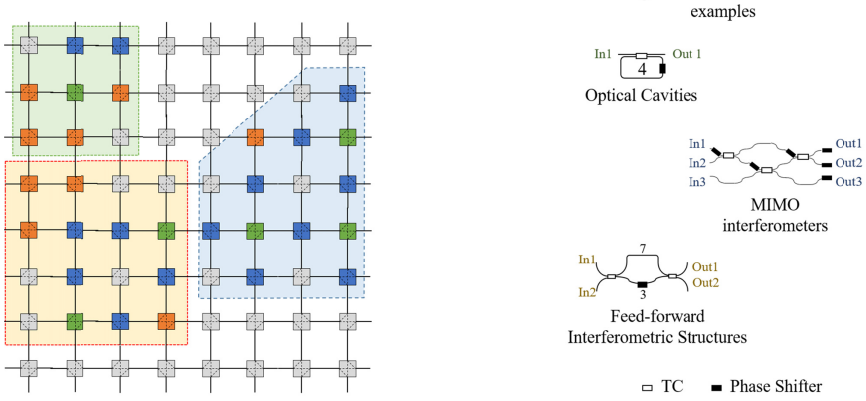

Fig. 8. Simultaneous implementation of a Ring cavity (green shaded area) a Mach-Zehnder Interferometer (orange shaded region) and a 3x3 multiple port interferometer (blue shaded region) using an ABAB FPPA. TC: Tunable Coupler.

In all the cases shown, the FPPA programming is set to implement the same circuits shown in the right parts of the figures. We have chosen a representative example of an Infinite Impulse Response (IIR) filter (i.e. the optical ring cavity), a Finite Input response (FIR) filter (the Mach-Zehnder interferometer) and a multiple input/multiple output (MIMO) interferometer. Colored shading is added to help the reader in the identification of which part of the FPPA is implementing each circuit.

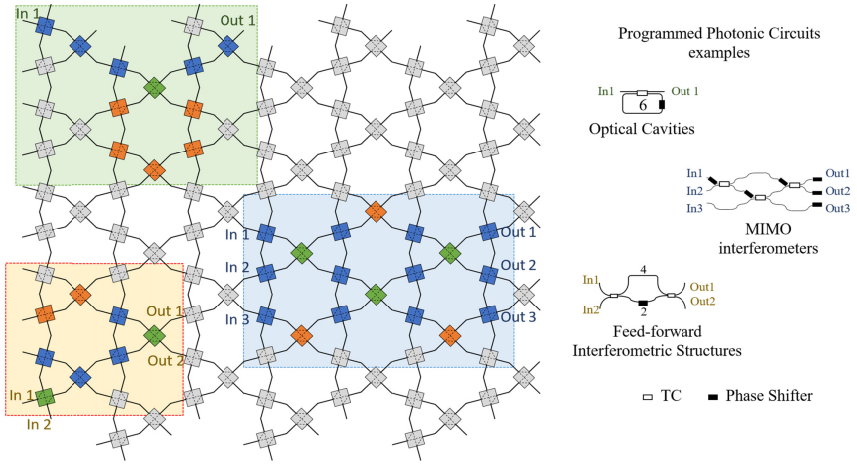

Fig. 9. Simultaneous implementation of a Ring cavity (green shaded area), a Mach-Zehnder Interferometer (orange shaded region) and a 3x3 multiple port interferometer (blue shaded region) using an ABCC FPPA. TC: Tunable Coupler.

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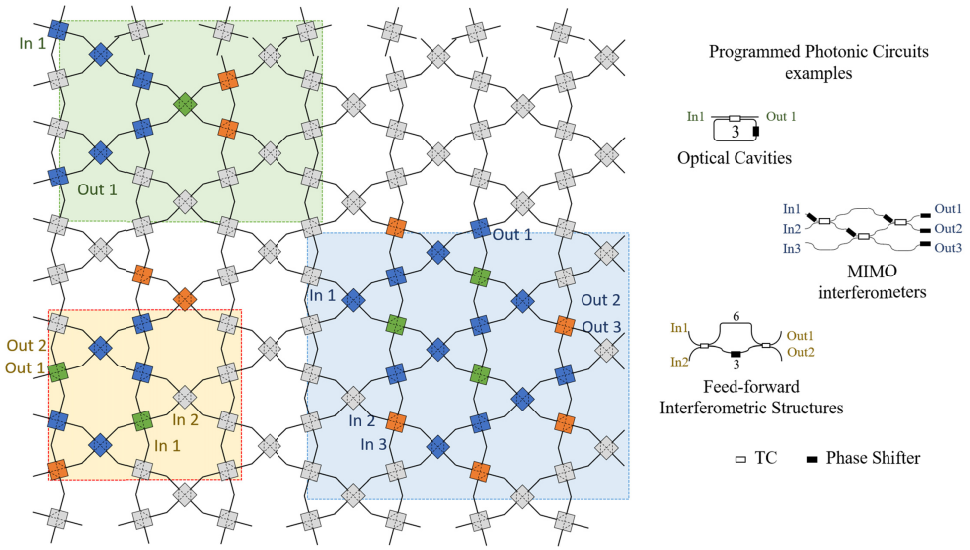

Fig. 10. Simultaneous implementation of a Ring cavity (green shaded area), a Mach-Zehnder Interferometer (orange shaded region) and a 3x3 multiple port interferometer (blue shaded region) using an ABDD FPPA. TC: Tunable Coupler.

Other functionalities are of course possible. For instance, tunable true time delay lines can be implemented by switching different sets of RPIs using the PPABs in crossbar switch mode [17].

4. Physical implementation

The physical implementation of the FPPA device calls for an integrated optics approach, either based on silicon photonics [18,19] or a hybrid/heterogeneous III-V and Silicon photonics platforms [20]. Figure 10 provides some information about the physical options available.

As for the PPBA elements, the currently available photonics technology options are listed in the upper part of Fig. 11. Regarding the implementation of ABAB, ABCC and ABDD FPPA layouts, the intermediate part of Fig. 11 shows the basic replicating blocks. These correspond to the unit blocks of the square, hexagonal and triangular waveguide meshes recently reported, as shown in Fig. 12. Therefore, uniform waveguide meshes provide a natural and compact option for their implementation.

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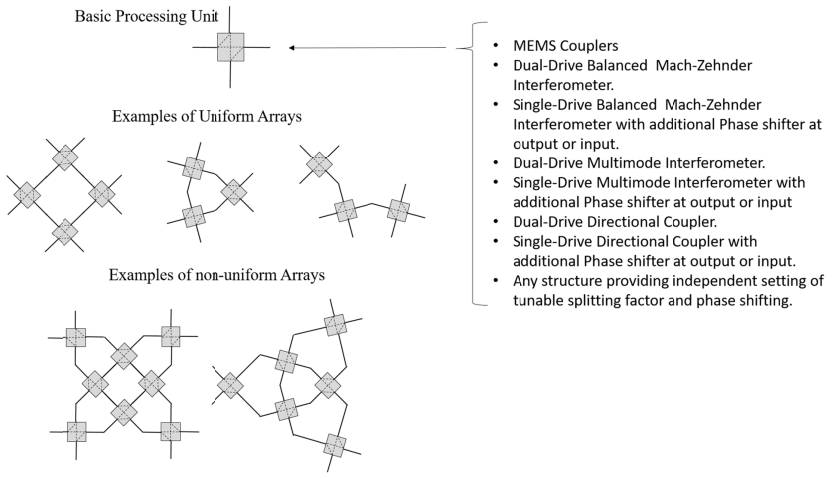

Fig. 11. Technology options for the implementation of the PPBA elements (upper), FPPA layouts (intermediate) and other FPPA possible configurations (lower).

Finally, as mentioned before, more complex FPPA layouts can be designed by interleaving the proposed types of PPBAs, however, in this case, they are implemented by non-uniform waveguide meshes. Some examples are shown in the lower part of Fig. 10.

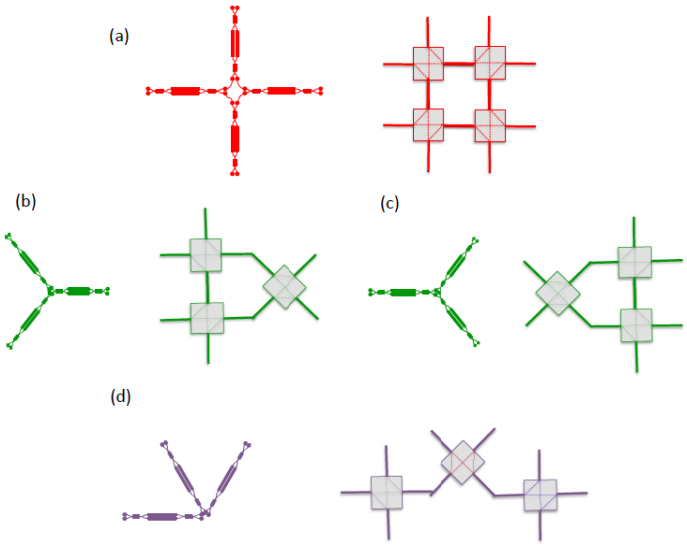

Fig. 12. Identification between the fundamental unit blocks employed to construct integrated waveguide meshes and the main RPI + PPAB blocks studied in this chapter. (a) Square waveguide mesh and ABAB block (b), (c) Hexagonal trilattices and the ABCC block. (d) Triangular waveguide mesh and the ABDD block.

5. Experiment

An ABCC class FPPA has been implemented by means of a silicon photonics hexagonal waveguide mesh composed of seven cells. Figures 13(a) and 13(b) show the equivalence between the waveguide mesh and the FPPA design. To ease the identification, the different building blocks are shown in different colors. Figures 13(c) and 13(d) show two implementations of the FPPA core in silicon photonics and silicon nitride, respectively. The silicon chip occupies a surface of 15 × 20 mm^2, includes 30 3-dB MZIs (featuring a length of

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975 μm), 60 thermal tuners and 120 pads, and features 24 optical input/output ports mounted on a printed circuit board (PCB) that occupies a surface of 60 × 120mm^2. We programmed the FPPA operation by acting over the bias currents of the MZIs. For further details on the chip, the reader is referred to [3]. For details on the measurement and characterization setup, the reader is referred to [4]. The silicon nitride chip occupies a surface of 5.5 x 11 mm^2, and includes 40 3-dB MZIs (featuring a length of 1297 μm) with 80 thermal tuners.

Due to the restricted number of cells in the waveguide mesh design, we did not dispose of enough PPBAs and RPIS to simultaneous implement the three circuits shown in Fig. 9. Here we show the results obtained in the programming of each circuit separately.

Figure 14 shows the programming (a), equivalent circuit (b) as well as measured modulus (c) and phase (d) of the transfer function for an unbalanced (by 4x975 μm) Mach-Zehnder interferometer. Note that two PPABs implement the functionality of tunable couplers K_1 and K_2. In fact, the experimental results show different spectra corresponding to different values of K_1 and K_2. The free spectral range corresponds to the path unbalance.

Figure 15 shows the programming (a), equivalent circuit (b) and measured modulus of the reflected (c) and transmitted (d) signals in a double coupler ring cavity (cavity length = 6x975 μm) resonator. Again, two PPABs implement the functionality of tunable couplers K_1 and K_2 with the experimental results showing different spectra corresponding to different values of K_1 and K_2. The free spectral range corresponds to the path unbalance.

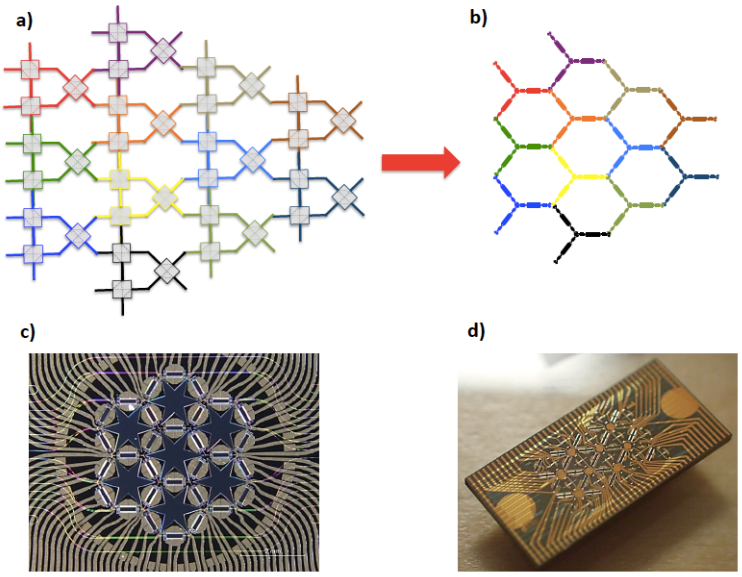

Fig. 13. (a) Layout of the ABCC class FPPA implemented by means of a 7-cell hexagonal waveguide mesh displayed in (b). Silicon (c) and Silicon Nitride (d) chips implementing the 7-cell hexagonal waveguide mesh.

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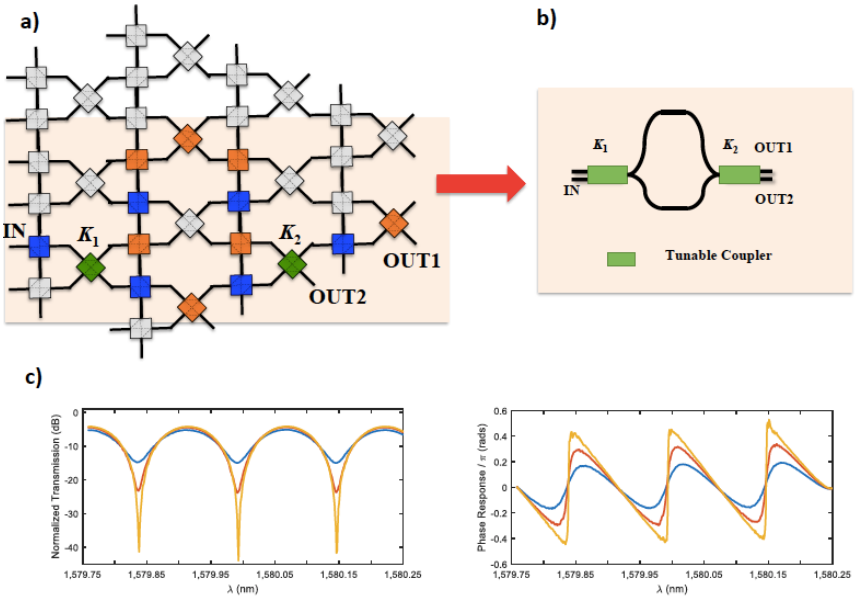

Fig. 14. Programming (a), equivalent circuit (b), as well as measured modulus (c) and phase (d) of the transfer function for an unbalanced (by 4x975 μm) Mach-Zehnder interferometer. The different curves in (c) and (d) correspond to different values of K_1 and K_2.

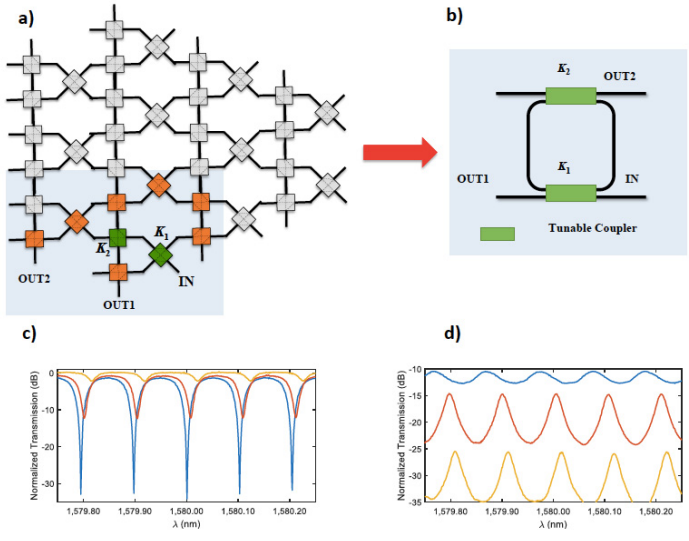

Fig. 15. Programming (a), equivalent circuit (b) and measured modulus of the reflected (c) and transmitted (d) transfer functions for a double coupler ring resonator (cavity length = 6x975 μm). The different curves in (c) and (d) correspond to different values of K_1 and K_2.

Finally, in Fig. 16, we show the results corresponding to a 3x3 MIMO interferometer programmed to implement a 3x3 splitter (tritter) or a DFT. In this case, there is enough room left in the FPPA to accommodate a second circuit (a Hadamard gate), which we also programmed to show simultaneous circuit implementation.

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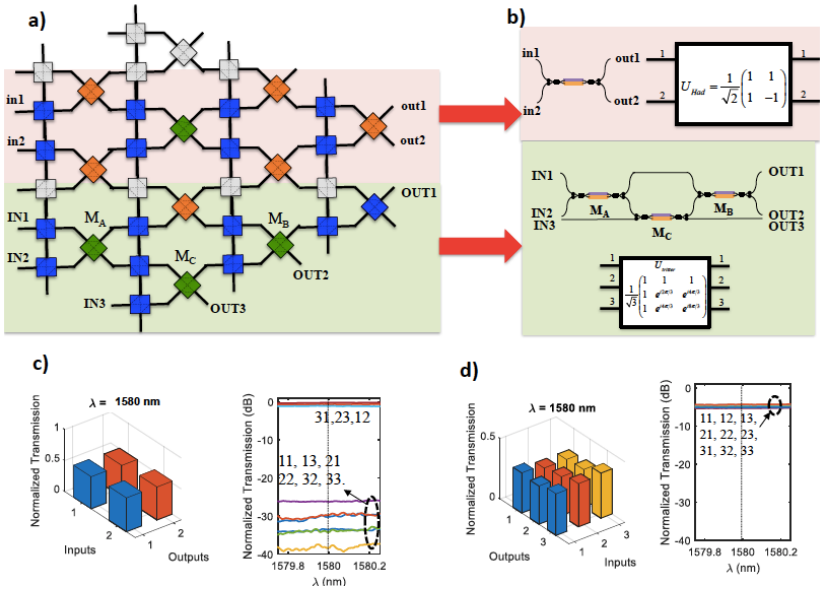

Fig. 16. Programming (a), equivalent circuits (b) and measured bar chart (@1580 nm) and modulus of the transfer functions of a (c) 2x2 MIMO interferometer implementing a Hadamard gate and (d) a 3x3 MIMO interferometer implementing a tritter operation.

The specific transformations are given in this case by:

$$U_{Hadamard} = \frac{1}{\sqrt{2}}\begin{pmatrix}1 & 1\\ 1 & -1\end{pmatrix},$$
$$U_{Tritter} = \frac{1}{\sqrt{3}}\begin{pmatrix}1 & 1 & 1\\ 1 & e^{i\frac{2\pi}{3}} & e^{i\frac{4\pi}{3}}\\ 1 & e^{i\frac{4\pi}{3}} & e^{i\frac{8\pi}{3}}\end{pmatrix}. \quad (6)$$

6. Discussion, summary and conclusions

The versatility of the FPPA is directly proportional to the number of PPABs and RPIs contained in the integrated chip. However, the scalability of these systems is limited by different factors: PPAB and RPI insertion losses, power consumption, optical crosstalk/signal leakage, footprint and the complexity of its control electronics. Of these, the dominant limit is the insertion loss, which is mainly generated by the inner coupling structures and phase-tuning mechanisms. In order to compare them with conventional PICs, we can split the total insertion loss per PPAB and RPIs as the sum of the propagation loss and the additional losses (couplers and tuning mechanism). Even using state-of-the-art tunable couplers and fabrication procedures to implement the PPABs and RPIs, achieving a value below 0.2-dB additional loss unit is a current challenge. With these numbers, we can estimate that a programmed light-path crossing 50 PPABs + RPIs will introduce 10-dB additional loss, setting a scalability limit of the size of the programmed circuits and a miniaturization trade-off [17]. Eventually, these losses may be compensated by the incorporation of semiconductor optical amplifiers (SOAs) as peripheral high-performance blocks (HPB) outside the FPPA core. Regarding the power consumption per PPAB ($P_{\pi,PPAB}$), and RPI ($P_{\pi,RPI}$), exploring tuning mechanism approaches will be fundamental to find power-efficient, low-loss, reduced-size, focalized and low-crosstalk phase shifters. In this sense, thermal tuners have been optimized in the last years to

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open the path for either sub-milliwatts power consumptions [21] or reduced footprint structures [22]. For a FPPA with N active PPABs and M active RPIs, the average power consumption is less than $N{\cdot}P_{\pi,\mathrm{PPAB}} + M{\cdot}P_{\pi,\mathrm{RPI}}$. Additionally, low-loss alternatives enabling the speed increment of the tuners would open the path to a wider range of application in optical/quantum information processing.

An additional concern is the non-desired side effects related to the use of non-ideal components like the optical crosstalk due to the drift in the configured coupling value and to fabrication or design errors. The optical crosstalk produces signal leaking through the FPPA core that causes reflections inside the circuits, creating ripples in the spectral responses and even lasing phenomena. This has been addressed in other kind of complex circuits [3,6]. Here, the unused PPABs and RPIs can be smartly configured to extract the leaked signal to drain optical ports to radically improve the system performance and relax the PPAB specifications to an optical crosstalk less than 20 dB to assure a good circuit performance. If ultra-low-loss, low-power PPABs and RPIs are obtained, future FPPAs will require an increment of the integration densities to further enlarge their performance in a similar way as the number of transistors per chip rate rises in electronic processors. To overcome the PPAB miniaturization trade-offs, three-dimensional Si photonics platforms can be considered [23].

In summary, we have proposed a new programmable integrated photonic device, the Field Programmable Photonic Array. This device is inspired by similar principles of those of Field Programmable Gate Arrays and Field Programmable Analog Arrays in electronics. We have described the main high-level concept of the device, together with a description of its basic constituents or photonic building blocks. These pertain to two different groups, the programmable photonics analog blocks or PPABs, mainly 2x2 tunable photonic components in charge of the basic operations over the amplitude and phase of the optical waveguide modes, and the reconfigurable photonic interconnects or RPIs, in charge of controlling and routing the signal flow between PPABs. We have shown how to assemble the different types of PPABs to form different FPPA classes and discussed general guidelines for design and technology implementation. The physical implementation of the FFPA, which is a key aspect, has also been considered and we have shown that the main FFPA classes can be implemented by means of integrated waveguide meshes. Finally, we have provided a simple experimental proof of concept to support the viability of this concept. The future evolution of this concept requires further investigation to address several issues. A very important one is scalability, which is required to implement FFPAs with enough PPAB and RPI elements to implement complex and simultaneous operations. The interface with electronic control signals is another important topic, together with the link of the latter to reconfiguration software. Last, but not least, the investigation on different alternatives to provide low power consumption PPAB elements should be seriously addressed in order to achieve low-power FFPA devices.

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