IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received November 22, 2021, accepted December 5, 2021, date of publication December 8, 2021,
date of current version December 23, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3134089

Microstrip to Double Ridge Empty Substrate Integrated Waveguide Transitions Based on Exponential and Superelliptical Dielectric Taper

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This work was supported by the Ministerio de Ciencia e Innovación, Spanish Government, under Project PID2019-103982RB-C44 and Project PID2019-103982RB-C41.

ABSTRACT The Empty Substrate Integrated Waveguides (ESIW) maintain the advantages of the Substrate Integrated waveguide (SIW) (i.e. low-volume, low profile, lightweight, easy manufacturing, and integration in a planar circuit board), and present lower losses and higher quality factors in resonators due to the propagation of the fields through air, instead of through lossy dielectric as in SIW. The operational (monomode) bandwidth of the ESIW can be increased with the Single Ridge ESIW (SRESIW). However, the bandwidth can be further increased with the Double Ridge ESIW (DRESIW). In this paper, a brief study of possible DRESIW geometries has been performed, and two transitions from microstrip line (MS) to DRESIW with a dielectric taper geometry based on different equations are proposed. The new wideband transitions present simulated return losses in back-to-back configurations greater than 20 dB in more than a 95% fractional bandwidth. The transition that presents a better compromise between return losses, bandwidth and ease of fabrication is manufactured. The measured return and insertion losses are better than 19.7 dB and 1.5 dB, respectively, in a 96.4% fractional bandwidth.

INDEX TERMS Ridge waveguide, empty substrate integrated waveguide, microstrip line, transition, substrate integrated circuit, tapering structure, wideband communication devices.

I. INTRODUCTION

In the last decade, the trend in RF technology is to increase the operating frequency while, at the same time, demanding microwave components with an excellent behaviour in terms of electric response, low losses, small volume and weight, and reduced manufacturing costs. The traditional communication systems (i.e. high-power applications) are usually developed on waveguide technology, whose components exhibit high performance, are robust and reliable, but also heavy, expensive, bulky and difficult to integrate with other technological solutions. A classical alternative is the planar technology, like microstrip, coplanar or stripline, which provide low-volume, light-weight, and small components with easy integration, but their electrical performance (i.e. attenuation and high-power handling) is not good enough for some high frequency applications.

In order to cover the gap between traditional waveguide and planar technologies, a full suite of novel Substrate Integrated Circuits (SICs) has been object of research in the last two decades. These technologies represent a half-way compromise in terms of performance between traditional waveguides and planar lines.

The first one of these SICs to be proposed was the Substrate Integrated Waveguide (SIW) [1], which mimics a traditional waveguide on a printed circuit board using two lateral rows of metallized via holes. The SIW presents the same advantages than the microstrip technology (low cost, low profile, easy manufacturing), and reduces the losses compared to the microstrip line. However, there is some field leakage

The associate editor coordinating the review of this manuscript and approving it for publication was Yongle Wu.

between the lateral vias, and there are losses due to the fact that the fields propagate through lossy dielectric material. These losses lead to a non-competitive behaviour at high frequencies. Therefore, an empty version of the SIW, called Empty Substrate Integrated Waveguide (ESIW) [2] has been developed. The ESIW removes the dielectric material from the path of the electromagnetic waves, and presents solid metallized lateral walls, so there is no dielectric or radiation loss, thus being suitable for higher frequencies and with better quality factors in resonators. The ESIW is also low cost and easy to manufacture, as the SIW, although it is larger because the wavelength in air is greater than in the dielectric medium.

Multiple microwave components have been designed and manufactured in the ESIW technology, such as filters of different order and type [3]–[5], a phase shifter [6], a hybrid directional coupler 90° [7] and H-plane horns [8], [9]. In order to connect these microwave components with planar technologies, such as microstrip, a transition from microstrip to ESIW is necessary. Several transition design approaches have been proposed, such as a dielectric taper inside the ESIW and a taper in the microstrip line [10], a widened waveguide section at the beginning of the ESIW together with a taper in the microstrip line [11], a through-wire [12], and a tapered artificial dielectric slab matrix [13]. All these transitions present a usable bandwidth limitation, due both to the bandwidth of the fundamental mode in the ESIW, and to the frequency range in which the transition provides a good impedance matching between the microstrip and the ESIW. This results in a practical fractional bandwidth not greater than 66%, which may be small for certain applications.

In order to overcome this limitation, a single ridge ESIW (SRESIW) can be used, since it exhibits a larger mono-mode bandwidth with the same width and height of the cross section. The SRESIW was first proposed in [14]. However, it was not until years later that microstrip to SRESIW transitions were proposed, designed, and manufactured [15], [16]. These transitions present a fractional bandwidth of around 80%. Nevertheless, there is still margin for further frequency bandwidth improvement by using two ridges, in what we can call a Double Ridge ESIW (DRESIW).

Therefore, a good transition from planar lines (usually microstrip) to DRESIW is necessary. This work presents a brief study of possible geometries of a transition from microstrip to DRESIW, with the aim of achieving a good impedance matching in almost all of the available mono-mode bandwidth.

This paper is structured as follows: Section II presents possible DRESIW geometries, as well as their influence on the bandwidth and ease of manufacturing. Section III proposes two geometries for a microstrip to DRESIW transition with its correspondent design procedure. One of these transitions is selected for the manufacture of a back-to-back prototype, and the results are detailed and discussed in Section IV. Finally, the conclusions are presented in Section V.

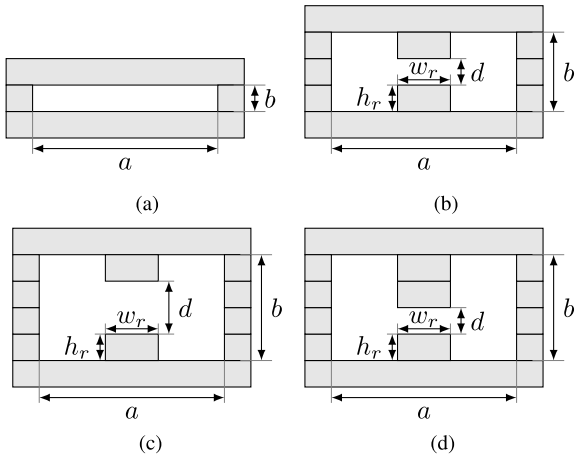


FIGURE 1. ESIW cross-section in (a), and different possible geometries of DRESIW in (b), (c) and (d). $d = h_r$ in (b), $d = 2 \cdot h_r$ in (c), and $d = h_r$ but the upper ridge with height doubled in (d).

II. DRESIW CROSS-SECTION DESIGN

The ridge rectangular waveguide presents one or several metallic ridges attached to the horizontal walls. It is well-known and it has been studied in depth in [17]. The ridges allow a reduction of the cutoff frequency of the first mode (TE_{10}) and an increase in the cutoff frequency of the first higher order mode (TE_{20}), thus providing a higher monomode bandwidth. This is valid for the rectangular waveguide, and also for the ESIW, whose usable bandwidth is also increased by the use of ridges [15].

As mentioned before, we will focus on the double ridge ESIW, or DRESIW. The use of standard techniques used for manufacturing planar circuits allows the creation of the DRESIW simply by piling substrates of the same height, as shown in Fig. 1, where the cross-section of the ESIW is compared with the cross-section of three different possible DRESIW geometries. The use of the same substrate for all layers facilitates the fabrication, but limits the flexibility of design, since the height of the DRESIW (i.e. the dimension b) must be a multiple of the substrate height h_r. So, $b = n \cdot h_r$ where n is the number of layers other that the top and bottom covers. It must be noted that for the DRESIW $n \geq 3$. In order to maximize the usable bandwidth (interval between the cutoff frequencies of the fundamental mode TE_{10} ($f_{c_{10}}$) and the first higher order mode TE_{20} ($f_{c_{20}}$) [17]), and once h_r has been selected, the ridge width w_r and the number of layers n can be optimized. The following transcendental equations can be used in order to compute $f_{c_{10}}$ and $f_{c_{20}}$, and thus estimate and maximize the usable bandwidth:

$$\cot\left(\frac{2\pi f_{c_{10}}\left(\frac{a-w_r}{2}\right)}{c_0}\right) - \frac{b}{d}\tan\left(\frac{\pi w_r f_{c_{10}}}{c_0}\right) - \frac{B}{Y_{01}} = 0 \quad (1)$$

$$\cot\left(\frac{2\pi f_{c_{20}}\left(\frac{a-w_r}{2}\right)}{c_0}\right) + \frac{b}{d}\cot\left(\frac{\pi w_r f_{c_{20}}}{c_0}\right) - \frac{B}{Y_{01}} = 0 \quad (2)$$

In these equations c_0 is the light velocity whereas b, w_r, a, and d are shown in Figure 1, and the susceptance B/Y_{01},

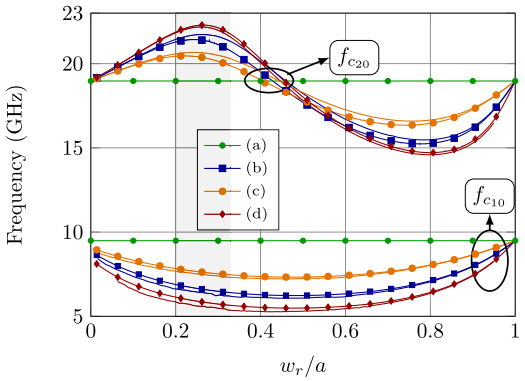


FIGURE 2. Cutoff frequencies $f_{c_{10}}$ and $f_{c_{20}}$ for the four geometries of Figure 1. (Waveguide width $a = 15.7988$ mm and substrate height $h_r = 0.813$ mm).

TABLE 1. Comparison between the four geometries of Figure 1. $f_{c_{10}}$, $f_{c_{20}}$, and BW in GHz.

Fig.	$f_{c_{10}}$	$f_{c_{20}}$	BW	$BW(\%)$	w_r/a
(a)	9.480	18.970	9.490	63.3	-
(b)	6.369	21.723	15.354	102.3	0.2569
(c)	7.537	20.692	13.135	87.6	0.2447
(d)	5.581	22.166	16.585	110.57	0.2695

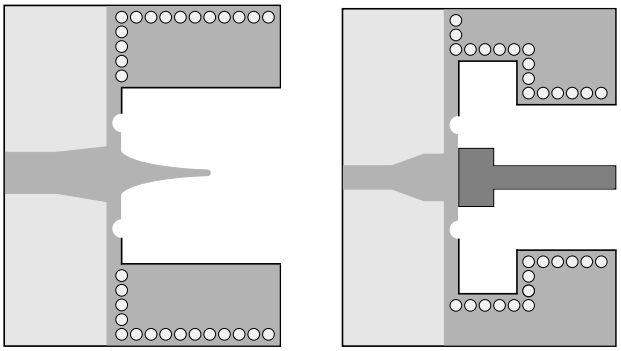
which models the gap in the ridge waveguide, can be approximated (as detailed in [18]) with:

$$\frac{B}{Y_{01}} \approx 2\left(\frac{b}{d}\right)\left(\frac{af_c}{c}\right)\ln\left(\csc\left(\frac{\pi d}{2b}\right)\right) \tag{3}$$

where f_c is $f_{c_{10}}$ for solving (1), and $f_{c_{20}}$ for solving (2).

The dependence of $f_{c_{10}}$ and $f_{c_{20}}$ with the ridge width w_r for the ESIW and the three DRESIW geometries of Figure 1 is shown in Fig. 2. In all four cases, *Rogers* 4003*C* substrates of height $h_r = 0.813$ mm, and the same width as for the WR62 rectangular waveguide ($a = 15.7988$ mm), have been considered. The results using (1), (2), and (3) (plotted with marks) are compared with the results obtained with the commercial simulator CST (plotted in solid lines). In addition, the plot area with values of w_r that provide higher bandwidth has been shadowed. It corresponds to the interval $w_r/a \approx 0.2 - 0.35$. It can be observed that there is a very good coincidence between the results obtained with the analytical formula and the commercial simulator CST.

Table 1 compares the four geometries of Figure 1 in terms of cutoff frequencies, absolute and fractional bandwidth, and the optimum ratio w_r/a that maximizes the bandwidth. It can be observed that a good compromise between minimizing the number of additional layers, ease of manufacturing, cost, and volume, while maximizing the bandwidth, is the topology of Figure 1(b). Therefore, this is the geometry that has been chosen and that is been used for this work. From now on, when we refer to the DRESIW, we are referring to this specific geometry.



(a) Microstrip to ESIW transition with exponential dielectric taper [2].

(b) Microstrip to SRESIW transition with widening of the ridge layer [15].

FIGURE 3. Previous solutions that inspired the transitions presented in this paper.

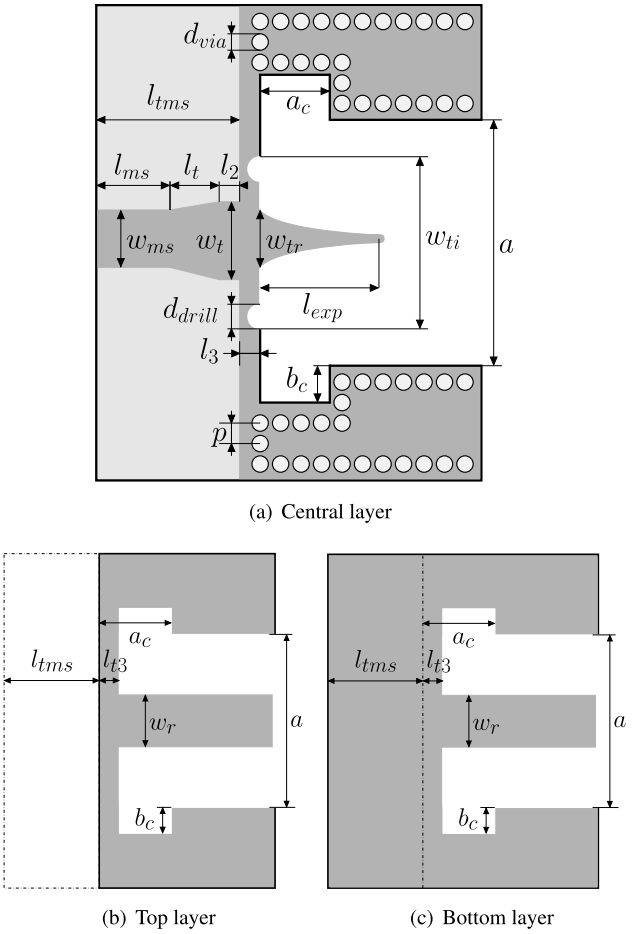
III. DESIGN OF TRANSITIONS FROM MICROSTRIP TO DRESIW

The best known and most used transition from microstrip to ESIW uses a nose-shaped dielectric taper inside the ESIW [2], as shown in Figure 3(a). Usually the function of the dielectric tapers is to perform an impedance gradient matching between the technologies to be connected. However, although a nose-shaped dielectric taper (Fig. 3(a)) in the central layer provides good performance in the transition from microstrip to ESIW, using only this taper provides a poor matching if used to transition from microstrip to DRESIW. Another possible transition would be the solution used in [15] for connecting microstrip to the single ridge ESIW (SRESIW) (Fig. 3(b)). Instead of a nose-shaped taper, this transition uses a widened ridge ESIW section. But again this transition does not provide a competitive behaviour when used to connect microstrip to DRESIW.

In this paper, we propose two possible geometries for the transition from microstrip to DRESIW in order to achieve a good matching in the largest possible fraction of the available bandwidth. The proposed transitions are based on a combination of some features of both the microstrip to ESIW and the microstrip to SRESIW transitions. The DRESIW section is widened, but only in the lateral walls, while, different from the microstrip to SRESIW transition, the ridge width is kept constant. Besides the widening of the lateral walls, a dielectric taper in the central layer is also added. Since the field concentration near the taper is higher in the DRESIW than in the ESIW, due to the presence of the upper and bottom ridges, it might be that a different profile other than the nose-shaped one would be more convenient. For that reason, in this work, besides the nose shape a superellipse shape has also been tested, and their performance have been compared.

A. NOSE-SHAPED DIELECTRIC TAPER TRANSITION

The first transition proposed in this work (see the layout in Figure 4) uses the nose-shaped dielectric taper, which is based on exponential equations as proposed in the first transition



(a) Central layer

(b) Top layer (c) Bottom layer

FIGURE 4. Layout of the microstrip line to DRESIW transition with nose-shaped dielectric taper proposed in this work. White represents empty spaces, light gray represents dielectric body, and dark gray represents copper surfaces.

from microstrip to ESIW (Fig. 3(a)). The lateral walls of the DRESIW are widened, but the ridge width is maintained constant. The equation that controls the taper width $W(x)$ in the nose-shaped taper is,

$$W(x) = \frac{w_{tr}(e^{-c\,l_{exp}} - e^{-c\,x}) + w_{tf}(e^{-c\,x} - 1)}{e^{-c\,l_{exp}} - 1} \tag{4}$$

where l_{exp} controls the length of the taper, and c controls the velocity at which the width decreases. Taking into account the feasibility of the manufacturing process and the mechanical stability, the end of the taper is finished with a semicircle when $W(x)$ is as low as w_{tf} (w_{tf} is fixed to 0.5 mm in this work). In order to simplify the parameters that control the transition, both ridge layers (Fig. 4(b), 4(c)) present the same structure with a widening in the waveguide (controlled by a_c and b_c) and a holder (of length l_{t3}) with the aim of providing greater consistency and stabiity.

In order to accelerate the design process, initial expressions for the design parameters are provided in Table 2. The expressions for the initial values of a_c, l_t, l_2 are extracted from [15], and the initial value of l_{exp} is extracted from [10].

TABLE 2. Initial values for the design parameters in the transition from microstrip line to DRESIW with nose-shaped dielectric taper.

w_{tr}	w_{ti}	l_t	a_c	b_c
$1.2w_r$	$1.5w_{tr}$	$\frac{\lambda_{ms}(f_0)}{4}$	$\frac{\lambda_g(f_0)}{2}$	$\frac{a}{6}$

w_t	l_{exp}	l_2	c
$0.4w_{ti}$	$\frac{\lambda_g(f_0)}{4}$	$\frac{l_t}{3}$	$2/l_{exp}$

TABLE 3. Dimensions of the fixed and design parameters (mm) of the transition from microstrip line to DRESIW with nose-shaped dielectric taper.

Fixed parameters	
p	0.5
d_{via}	0.5
w_r	4.059
d_{drill}	1
w_{ms}	1.813

Design parameters					
	Initial	Final		Initial	Final
w_{ti}	7.306	7.8516	l_{exp}	5.744	6.443
b_c	2.633	2.503	l_2	1.071	1.051
a_c	11.549	10.507	w_t	2.922	2.864
w_{tr}	4.870	4.754	l_t	3.213	3.006
l_{t3}	1.00	0.645	l_3	0.5	0.427

The initial expressions for the other design parameters have been obtained empirically, after designing this transition for several substrates and frequency bands. The value of λ_g used for computing the initial value of a_c and l_{exp} refers to the wavelength in the widened section of the DRESIW of width $a + 2b_c$. These initial values can be used to accelerate the optimization process for a wide range of frequency bands or substrates.

The initial expressions of Table 2 have been applied to design a transition from a 50 Ω microstrip line to a DRESIW of the same width as the standard WR-62 rectangular waveguide ($a = 15.7988$ mm). Both the microstrip lines and the DRESIW are integrated in a Rogers 4003C substrate with height $h_r = 0.813$ mm and $\epsilon_r = 3.55$. Table 3 shows the fixed parameters and the design parameters before and after the optimization process. The Nelder-Mead Simplex algorithm of CST has been used in the optimization process, with the goal of maximizing the return loss in the highest possible bandwidth.

Fig. 5 shows the simulated response (reflection and transmission) of the microstrip to DRESIW back to back transition with the final values of Table 3. The reflection obtained with the initial values of Table 2 has also been plotted. It can be observed that the expressions of Table 2 provide a good approximation to the final optimized values, with return losses above 14 dB in a large bandwidth. The return losses with the optimized final values are greater than 20 dB from 7.2 to 21.7 GHz, and the insertion losses are lower than 0.65 dB in the same frequency range. This corresponds to an absolute bandwidth of 14.5 GHz and a fractional bandwidth of 100.3%, which is almost the maximum usable monomode bandwidth (102.3%).

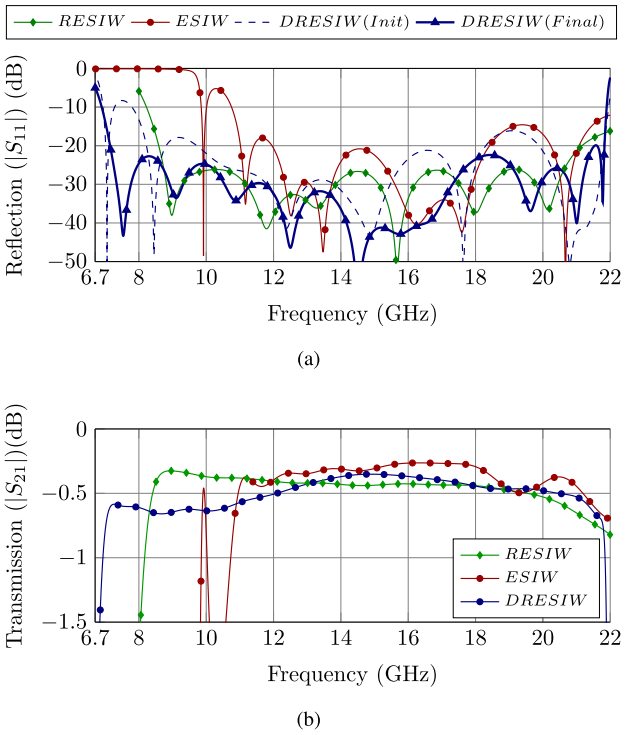


FIGURE 5. Simulated results for reflection (a) and transmission (b) of back-to-back microstrip to DRESIW transition with nose-shape dielectric taper, and comparison with ESIW without a ridge [10] and SRESIW [15].

In order to compare the results with a back-to-back transition from microstrip to ESIW without ridge [10] and to a single ridge ESIW (SRESIW) [15], the return losses of both transitions have also been plotted in Fig. 5 (top). The fractional bandwidth with the return losses over 20 dB for the DRESIW supposes an increment of 144% and 28% in comparison with the fractional bandwidth for ESIW and SRESIW, respectively.

B. SUPERELLIPSE DIELECTRIC TAPER TRANSITION

The other transition proposed uses the equations of the generalized superellipse for shaping the dielectric taper instead of the nose-shape. The superellipse equations are not new in the microwave filed, and they were used for defining impedance matching networks in planar and rectangular technologies [19]. However, it was not until recently that it has been used to match two different technologies, as validated with a transition from microstrip to SRESIW in [16]. A superellipse [20] is a general curve with a single control parameter N. The superellipse is a curve in between a rectangle and an ellipse, and the parameter N controls whether the superellipse is closer to the rectangle or the ellipse. The Cartesian equation of the superellipse is

$$\left(\frac{x}{a}\right)^N + \left(\frac{y}{b}\right)^N = 1 \tag{5}$$

where a and b are the semiaxes of the superellipse and N controls the shape of the superellipse. Multiple shapes

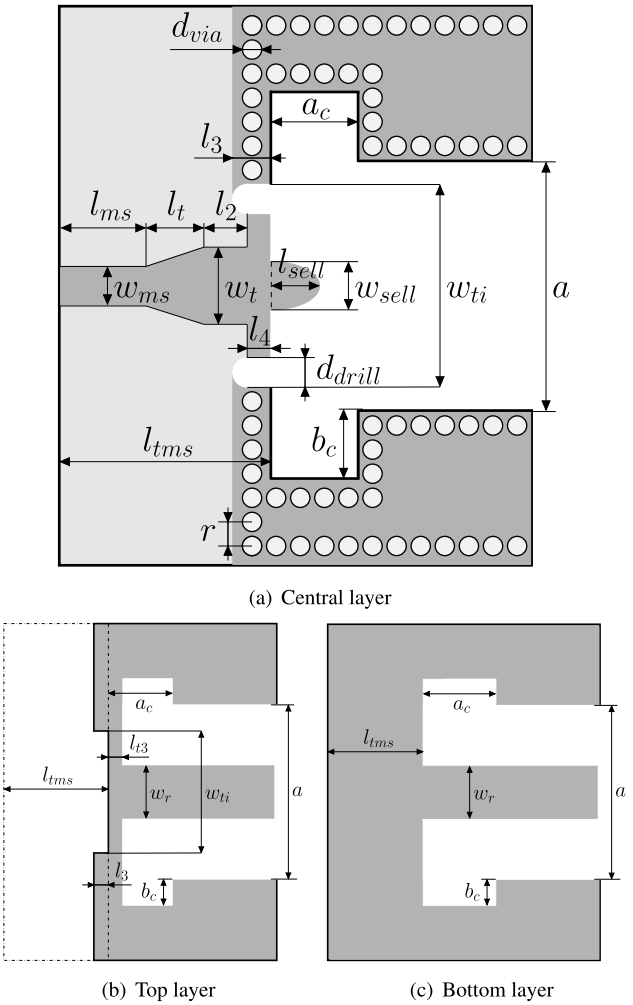


FIGURE 6. Layout of the microstrip line to DRESIW transition with superellipse dielectric taper proposed in this work. White represents empty spaces, light gray represents dielectric body, and dark gray represents copper surfaces.

can be achieved just varying N. However, more flexibility is gained with the generalized superellipse, defined by

$$\left(\frac{x}{a}\right)^p + \left(\frac{y}{b}\right)^q = 1 \tag{6}$$

where p and q control the curvature of the superellipse in the x-axis and y-axis, respectively, and independently. A nose sharp curve or a blunt ellipse can be obtained with extreme values of p or q. (i.e., $p, q = 0$ or $p, q \to \infty$). This curve provides a huge set of possible profiles using only two control parameters. Therefore, the generalized equation of the superellipse will be used to create the dielectric taper shown in Fig. 6, with the following profile:

$$\left(\frac{x}{l_{sell}}\right)^p + \left(\frac{y}{\frac{w_{sell}}{2}}\right)^q = 1 \tag{7}$$

where l_{sell} and $w_{sell}/2$ are the semi-axis of the superellipse. The top and bottom layers of the transition (Figs. 6(b), and 6(c)) are the same ones as in the nose-shaped transitions, with the only difference that in the top layer a cut

TABLE 4. Initial values for the design parameters in the transition from microstrip line to DRESIW with superellipse dielectric taper.

w_{ti}	w_t	l_t	a_c	b_c
$\frac{2}{3}a$	$\frac{w_r+w_{ms}}{2}$	$\frac{\lambda_{ms}(f_0)}{2}$	$\frac{\lambda_g(f_0)}{2}$	$\frac{a}{6}$

w_{sell}	l_{sell}	l_2	p	q
$0.4w_r$	$\frac{\lambda_g(f_0)}{4}$	$\frac{l_t}{8}$	2.5	2.0

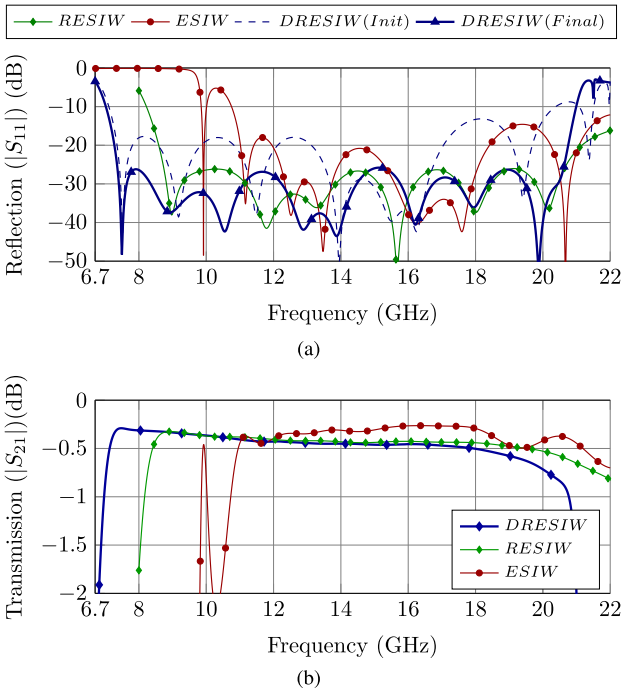


FIGURE 7. Simulated results for reflection (a) and transmission (b) of back-to-back microstrip to DRESIW transition with superellipse dielectric taper, and comparison with ESIW without a ridge [10] and SRESIW [15].

of the same width as the iris w_{ti} has been included, with the aim of providing a better impedance matching.

Table 4 provides initial values for the design parameters of the transitions. The expressions for the initial values of a_c, b_c, w_{sell} are extracted from [16], and l_{sell} is extracted from [10]. As in the previous transition, λ_g refers to the wavelength in the widened section of DRESIW of width $a + 2b_c$. The other expressions have been obtained experimentally after designing the transition for different frequencies and substrates.

The initial expressions summarized in Table 4 have been applied in order to design a transition with the same characteristics as for the previous nose-shaped transition (the same microstrip line impedance, substrate type and height and waveguide width are considered) with the aim to compare both transitions. After fixing the initial values, an optimization is carried out with the help of CST using the Nelder-Mead Simplex optimizer, with the goal of maximizing the return loss at the highest possible bandwidth. Table 5 shows the fixed and design parameters before and after the optimization process.

Fig. 7 shows the performance of the DRESIW back-to-back transition with the optimum values. The reflection with

TABLE 5. Dimmensions of the fixed and design parameters (mm) of the transition from microstrip line to DRESIW with superellipse dielectric taper.

Fixed parameters	
l_3	1.25
d_{via}	0.7
w_r	4.059
d_{drill}, r	1
w_{ms}	1.813
l_{t3}	1.00

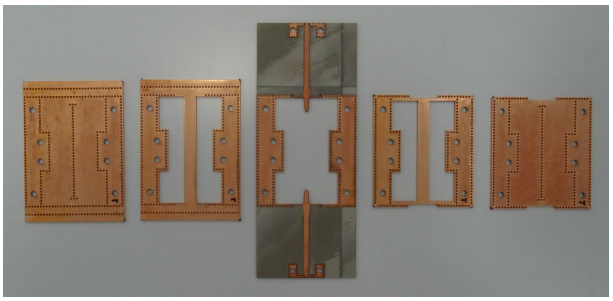
Design parameters					
	Initial	Final		Initial	Final
w_{ti}	10.532	10.190	l_{sell}	5.266	4.945
b_c	2.633	3.121	l_2	0.803	1.002
a_c	11.549	11.328	w_t	2.936	2.656
w_{sell}	1.623	1.710	l_t	6.425	5.006
l_4	0.5	0.488	p	2.5	3.506
q	2.0	2.702			

the initial values has also been plotted. As in the previous transition, the initial values provide a good initial point, with return losses above 15 dB in most of the bandwidth. With the final optimized values, return losses are greater than 26 dB and insertion losses are lower than 0.7 dB between 7.3 and 20.63 GHz. This corresponds to an absolute bandwidth of 13.3 GHz, and a fractional bandwidth of 95.4%, which is almost all the usable frequency band of the DRESIW. The reflection and transmission of the ESIW without ridge [10] and the single ridge ESIW (SRESIW) [15] have also been included. It can be observed that the fractional bandwidth with the return losses over 20 dB for the DRESIW supposes an increment of 123% and 17% in comparison with the fractional bandwidth for ESIW and SRESIW, respectively.

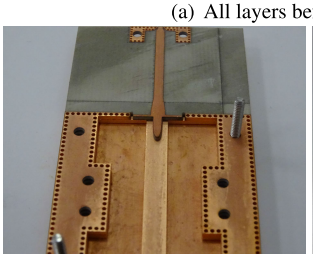
Comparing the nose-shaped and the superellipse transitions, it can be concluded that the superellipse transition presents a shorter fractional bandwidth. However, the return losses are better than in the nose-shaped transition, higher than 26 dB in a very large bandwidth. In addition, it should be taken into account that the nose-shaped dielectric taper is difficult to manufacture, especially for thin substrates that require long and narrow tapers to provide a good impedance matching. Therefore, after an overall assessment, the superellipse transition is preferred, and has been chosen for manufacturing a prototype and measuring its performance.

IV. RESULTS

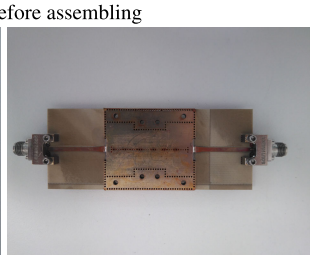
In order to validate the feasibility of the proposed microstrip to DRESIW transition with a superellipse dielectric taper, a back-to-back prototype has been manufactured, with the dimensions of Table 5, and measured. A Rogers 4003C substrate of $h_r = 0.813$ mm height and $\epsilon_r = 3.55$ has been used. Standard PCB processes have been used to mechanize the prototype (cutting, drilling, electrodeposition and copper removal). In the manufacturing process, the tolerance of the laser beam is only 2 μm in the same cut. Nevertheless, the tolerance for the repositioning of the laser beam for non-consecutive cuts and the tolerance in the alignment of the layers is around 50 μm. In order to ensure electrical



(a) All layers before assembling



(b) Detailed view of the transition



(c) Assembled prototype

FIGURE 8. Back-to-back manufactured prototype of the superellipse microstrip to DRESIW transition.

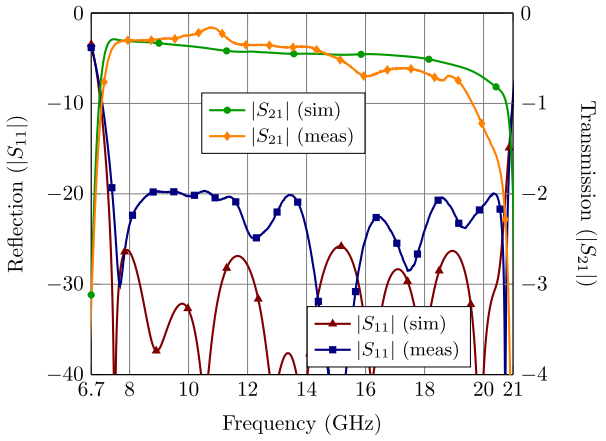


FIGURE 9. Comparison of simulation and measurement of the reflection of the back-to-back transition prototype.

TABLE 6. Performance comparison of the microstrip to DRESIW transition with previous proposals. RL and IL refer to the minimum return loss, and the maximum insertion loss in the bandwidth BW, respectively. FBW refers to the fractional bandwidth.

Transition	Layers	BW (GHz)	FBW	RL (dB)	IL (dB)
MS-SIW [22]	1	17.5-30	52%	15	1.26
MS-ESIW [10]	3	12-18	40%	20	1.2
MS-ESIW [23]	3	6.8-13.6	66%	13.5	1.5
MS-ESIW [11]	3	12-18	40%	21	1
MS-ESIW [12]	3	8.2-12.4	40.7%	12	0.9
MS-SRESIW [15]	4	8-20.5	87.7%	11	1.5
MS-SRESIW [16]	4	9-20.66	83%	14.5	1
This Work	5	7.2-20.6	96.4%	19.7	1.5

contact between the ridges and the top and bottom covers, a new assembly process based on two different tin soldering pastes, with two different melting temperatures, has been used. First, the top ridge layer is soldered to the top layer, and the bottom ridge layer to the bottom layer, and pressed using a tin soldering paste with a high melting temperature ($T_1 = 217°C$). Then, these two ridge plus cover layers are soldered, respectively, in the upper and lower sides of the central layer and pressed using a tin soldering paste with a low melting temperature ($T_2 = 183°C$) that does not melt the first soldering paste. This new procedure provides a better union between all layers, especially between the ridge layers and the covers, where otherwise some air gaps could appear. The back-to-back manufactured prototype is shown in Fig 8.

Fig. 9 plots the simulated and measured transmission and reflection coefficients of the back-to-back prototype. The coaxial to microstrip transitions have been de-embedded from the measurements using a custom Thru-Reflect-Line calibration kit [21]. There is a good agreement between measurement and simulation. The differences are due to manufacturing tolerances. The return and insertion losses are better than 19.7 dB and 1.5 dB between 7.2 and 20.7 GHz, which corresponds to an absolute bandwidth of 13.4 GHz and a fractional bandwidth of 96.4%.

The performance of several previously published transitions are compared in Table 6 with the transition presented in this work. They are compared in terms of insertion and return losses, absolute and fractional bandwidth, and number of layers. All transitions operate in the same or very similar frequency band. It can be observed that this new transition is competitive in terms of return and insertion losses, and it has the highest fractional bandwidth. It is well known that the ridge in rectangular waveguide increases the losses [17]. Coherently, in Table 6 the insertion losses of the SRESIW are greater than in the ESIW without ridge, and the insertion losses in the DRESIW are also greater than in the SRESIW.

V. CONCLUSION

This work proposes and tests the performance of double ridge ESIW topologies formed by piling equal height substrates. A specific topology is chosen as a good compromise between maximizing the bandwidth and minimizing cost and volume. Two possible geometries (a nose-shaped and a superellipse) for designing wideband microstrip line to DRESIW transitions are proposed. A systematic procedure has been presented for designing both transitions, with expressions for setting good initial values for the design parameters. Both transitions are compared in terms of return losses, bandwidth and insertion losses. A back-to-back microstrip to DRESIW transition based on the superellipse geometry, which has shown better performance, has been designed, fabricated and measured. The simulated return losses are above 16 dB in a 96.4% fractional bandwidth. Comparing with several previous transitions from microstrip to ESIW or to SRESIW, the new transition provides a higher bandwidth with good return losses, and paves the way for designing a complete suite of microwave substrate integrated devices for wideband applications.

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