electronics

MDPI

Article

Small-Signal Model of the NPC + GCC Multilevel Transformerless Inverter in Single-Phase Photovoltaic Power Systems

Iván Patrao *, Marian Liberos *, Raúl González-Medina, Enric Torán, Emilio Figueres and Gabriel Garcerá

Grupo de Sistemas Electrónicos Industriales, Departamento de Ingeniería Electrónica, Universitat Politècnica de València, Camino de Vera s/n, 46022 Valencia, Spain
* Correspondence: ivpather@upvnet.upv.es (I.P.); malimas@upv.es (M.L.)

Abstract: Photovoltaic transformerless inverters are very efficient and economical options for solar-power generation. The absence of the isolation transformer improves the converters' efficiency, but high-frequency voltage to ground can appear in the photovoltaic string poles. The high capacitance to ground of the photovoltaic generator leads to undesirable high-leakage currents. Using half-bridge topologies dramatically reduces the leakage to ground, and using a multilevel half-bridge inverters improves the output quality compared with classical inverters. The neutral point clamped + generation control circuit (NPC + GCC) topology is a multilevel single-phase transformerless inverter capable of tracking the maximum power point of two photovoltaic sources at the same time. This paper presents the control structure and the dynamic modeling of the NPC + GCC inverter. The pulse-width modulated (PWM) switch model in continuous conduction mode (CCM) was used to obtain the small-signal model of the two switching converters that make up the inverter. The resulting dynamic model was used to quantify the stability margins of both converters' current and voltage loops.

Keywords: photovoltaic inverter; MPPT; double MPPT; string inverter; photovoltaics; NPC + GCC topology; transformerless

Citation: Patrao, I.; Liberos, M.; González-Medina, R.; Torán, E.; Figueres, E.; Garcerá, G. Small-Signal Model of the NPC + GCC Multilevel Transformerless Inverter in Single-Phase Photovoltaic Power Systems. *Electronics* **2023**, *12*, 3545. https://doi.org/10.3390/electronics12173545

Academic Editor: Elias Stathatos

Received: 3 July 2023
Revised: 26 July 2023
Accepted: 13 August 2023
Published: 22 August 2023

1. Introduction

Grid-connected photovoltaic (PV) inverters may be divided into two categories: PV inverters with isolation transformer and transformerless PV inverters [1–3]. In power converters for renewable energy sources (RES), especially in grid-connected PV inverters, efficiency and cost are vital factors [4,5]. Transformerless inverters present high efficiency and cost less than those with a transformer [6,7]. Hence, many PV transformerless inverter topologies have been presented in the literature [1,8–11].

The main issue PV transformerless inverters must address is the common-mode voltage. The commutation of inverter switches can produce an alternating common-mode voltage between the PV-panel poles and the ground [12–14]. In PV power plants, the parasitic capacitance to ground can reach high values due to the large surface of the PV generator. Typical values vary between 50 and 150 nF/kW for crystalline-silicon cells and reach up to 1 µF/kW for thin-film cells [1]. The alternating component of the common-mode voltage generates a leakage current through these high capacitance values to ground, which may produce serious problems (e.g., the activation of electrical protections, efficiency degradation, and safety problems) [6,15,16]. Figure 1 depicts the parasitic capacitances and the leakage current.

A simple way of reducing the leakage current to ground is the use of half-bridge inverter topologies, in which the midpoint is connected to the neutral point [17]. However, the half-bridge topologies usually present a high level of total harmonic distortion (THD)

in their output. In [18], the NPC + GCC transformerless topology for a single-phase grid-connected PV inverter was presented (Figure 2). In this topology, the midpoint of the dc-link of a multilevel half-bridge neutral point clamped (NPC) inverter is used to reduce the leakage current to ground. Using a multilevel topology improves the THD of the output compared with a conventional half-bridge [19–22]. The more output voltage levels a topology possesses, the lower the level of THD it presents. A variety of topologies, like the cascaded H-bridge (CHB), the flying capacitor (FC), the diode-clamped inverter, the neutral-point clamped (NPC), the Conergy NPC, or the active NPC inverter, were presented in the literature [1]. Due to its cost and simplicity, the NPC is the most widely used topology in low-power systems. Moreover, the use of the midpoint of the input voltage leads to additional benefits in the leakage-current-to-ground reduction [1,21–24].

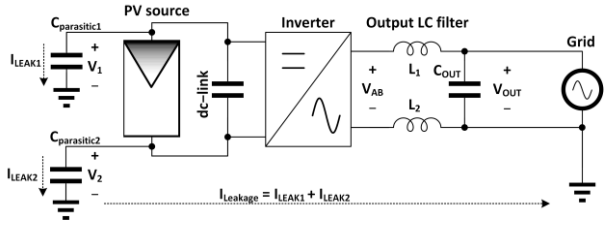

Figure 1. Parasitic capacitances and leakage current to ground in a PV transformerless inverter.

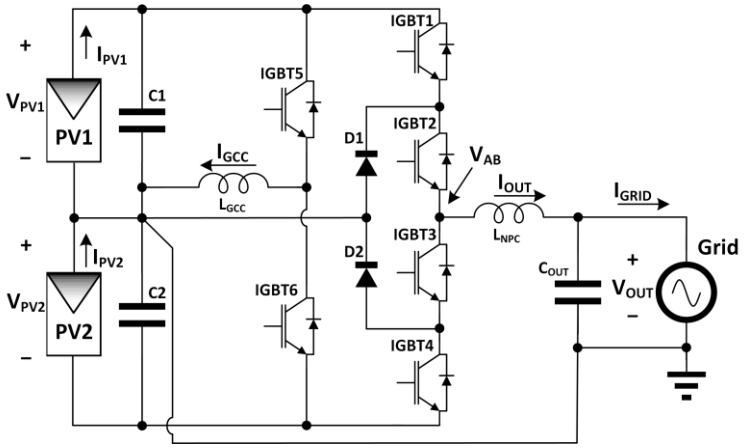

Figure 2. The NPC + GCC topology.

Furthermore the generation control circuit (GCC) converter uses the midpoint to provide the highly efficient double-maximum-power-point tracking of two series-connected PV sources, improving the power generation under partial shadowing in PV modules. In fact, the voltage control provided by the GCC converter solves the midpoint voltage balancing, the main drawback of the NPC inverter [25,26]. Partial shadowing is problematic in PV power plants, since a small shadow can dramatically reduce the overall power of a large group of PV modules [27,28], and the GCC circuit improves the partial-shadowing performance of the converter.

The NPC + GCC transformerless topology is formed by two parallel converters: the NPC multilevel inverter (IGBT1 to IGBT4 and D1 to D2), which manages the current injected over the grid; and the GCC DC/DC converter (IGBT5 and IGBT6), which adjusts the midpoint voltage of the dc-link. This pair of converters tracks two different maximum power points (MPP) in the converter's input (V_{PV1} and V_{PV2}). Compared with a double-stage PV inverter (boost + inverter), the NPC + GCC has better efficiency [18] since the GCC only manages the power difference between the strings and not the full power.

NPC and GCC converters share the input dc-link series-connected capacitors and are connected to the total input voltage. The midpoint is connected to the NPC's free-wheeling diodes and the GCC's inductance output port. This paper proposes a control

structure and presents the procedure to obtain a small signal dynamic model to control both converters independently. The objective is to control the input voltage in each dc-link independently while the NPC injects a sinusoidal current into the mains grid. Hence, a dual maximum-power-point tracking (MPPT) algorithm will run over the two inputs.

This paper is based on a 5 kW NPC + GCC photovoltaic inverter fed by a pair of PV strings of 3 kW each. Section 2 describes the control structure of the whole system in depth. Sections 2.1 and 2.2 detail the models of the NPC and the GCC converters. Then, Sections 3 and 4 detail how the models obtained are used to adjust the current and voltage regulators.

2. Transformerless PV Inverter Control Structure

Figure 3 shows the control structure of the NPC + GCC topology. It consists of a double maximum-power-point tracking (MPPT) perturb and observe (P&O) algorithm and independent control loops for the NPC and the GCC, organized as follows.

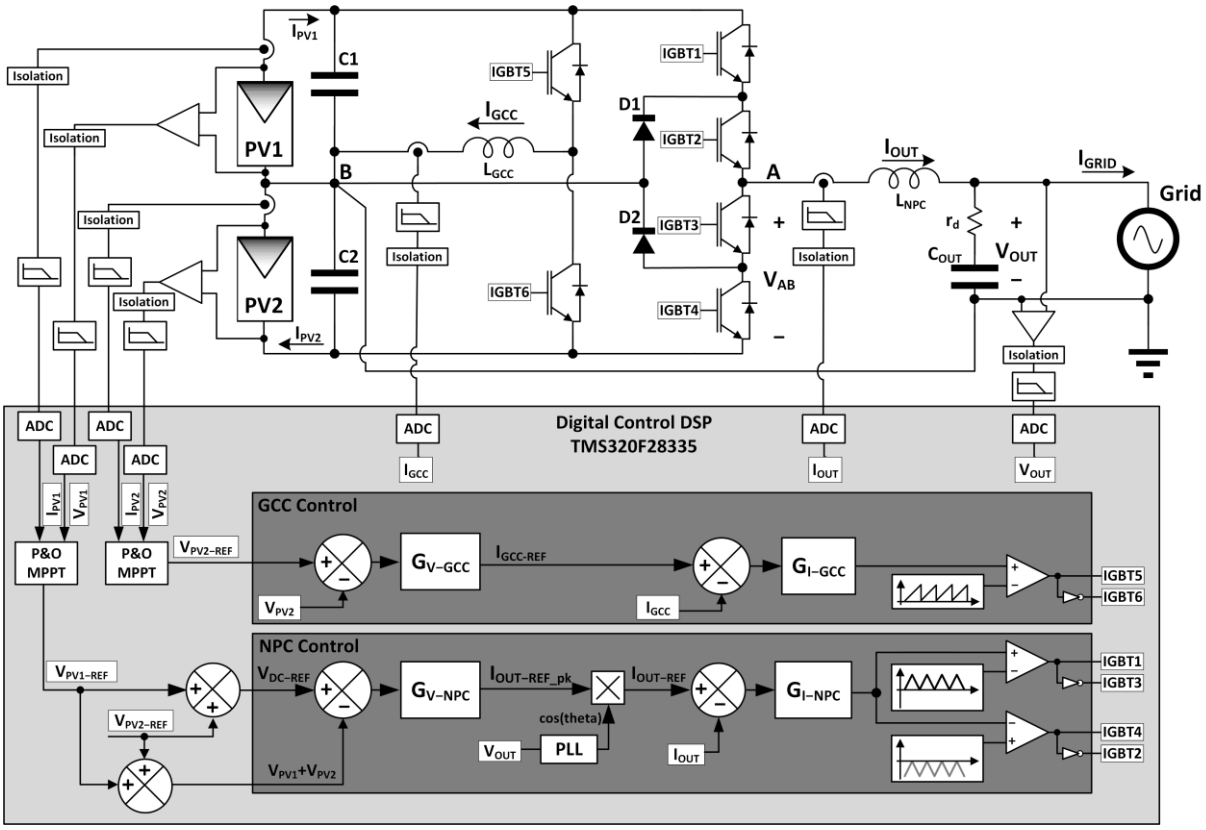

Figure 3. NPC + GCC topology control structure.

The GCC control block consists of a PWM modulator generating the switching signals for IGBT5 and IGBT6, fed by a current compensator ($G_{I\text{-}GCC}$), adjusting the inductance current. The current reference ($I_{GCC\text{-}REF}$) is generated by an input voltage compensator ($G_{V\text{-}GCC}$), which adjusts the voltage of the PV string number 2 (V_{PV2}).

The NPC control block consists of an in-phase disposition (IPD) PWM modulator, but other modulation multilevel techniques can be considered [29], generating the switching signals for IGBT1 to IGBT4, fed by a current compensator ($G_{I\text{-}NPC}$), adjusting the current injection into the mains grid. The phase-locked loop (PLL) generates the sinusoidal shape of the current reference ($I_{NPC\text{-}REF}$) to ensure unity power factor injection. The $I_{NPC\text{-}REF}$ magnitude is generated by the voltage compensator ($G_{V\text{-}NPC}$), which adjusts the total input voltage of the PV strings PV1 + PV2 ($V_{DC\text{-}REF}$). Hence, the voltage of PV1 (V_{PV1}) is indirectly controlled.

The current and control loops are digitally programmed in a Texas Instruments DSP TMS320F28335. All the signals are fed to the DSP controller through analog low-pass filters (LPF) and acquired through a 12-bit ADC running at 32 ksps. The two independent MPPT algorithms are based on the classical perturb and observe (P&O) technique and run by employing the PV input voltage and current values (V_{PV1}, I_{PV1} and V_{PV2}, I_{PV2}).

Table 1 summarizes the most critical parameters of the power converter under study. Regarding the voltage rating of the components, it must be noted that the MPP nominal input voltage of each input is 408.8 V. Hence, since the worst-case open circuit voltage in typical PV modules is usually 30% higher, the maximum input voltage is around 530 V. The switches of the GCC must withstand a voltage twice this value. Hence, 1200 V IGBTs are used. The switches in the NPC must withstand 530 V; therefore, a 950 V device is sufficient. However, the limited commercial offer in NPC half-bridge modules leads to the 1200 V device.

Table 1. Main parameters of the NPC + GCC PV inverter.

Parameter	Value
Input voltage at MPP (V_{PV-MPP})	2 × 408.8 V
Input current at MPP (I_{MPP})	7.54 A_{DC}
Maximum PV power (P_{PV-MAX})	2 × 3.08 kW
GCC switching frequency (f_{SW-GCC})	16 kHz
NPC switching frequency (f_{SW-NPC})	16 kHz
Input capacitance (C1 and C2)	2 × 3 mF
GCC inductance (L_{GCC})	15 mH
NPC inductance (L_{NPC})	2 mH
LC filter capacitance (C_{OUT})	9.4 µF
Damping resistor (r_d)	1 Ω
GCC IGBT switches	IRG4PH40KDPBF (1200 V/15 A)
NPC IGBT switches	APTGL60TL120T3G (1200 V/60 A)
RMS nominal grid voltage ($V_{GRID-RMS}$)	230 V_{RMS}
Nominal grid frequency (f_{GRID})	50 Hz
Anti-aliasing filters crossover frequency	16 kHz
ADC sampling frequency	32 kHz
Digital voltage regulators update frequency	32 kHz
Digital current regulators update frequency	32 kHz
MPPT update period	300 ms

In this work, the NPC inverter regulates the total dc-link voltage (V_{PV1} + V_{PV2}), whereas the GCC regulates the voltage V_{PV2}. Many MPPT methods have been presented in the literature, among which the perturb and observe (P&O) method is a simple but robust MPPT one, being the preferred option in low-to-medium power converters [30]. A double-MPPT P&O algorithm generates the voltage references $V_{PV1-REF}$ and $V_{PV2-REF}$. Figure 4 shows the flowchart algorithm of the implemented double MPPT algorithm. This algorithm is based on the classic P&O with a fixed step size [30,31].

The GCC voltage regulator (G_{V-GCC}) adjusts the current reference in the inductor ($I_{GCC-REF}$) to set the voltage V_{PV2} at the desired level. The voltage regulator of the NPC inverter (G_{V-NPC}) modifies the reference of the output current amplitude, $I_{OUT-REF}$, to regulate the total input voltage (V_{DC} = V_{PV1} + V_{PV2}) at the desired level. Since the GCC regulates V_{PV2}, this algorithm indirectly regulates the voltage V_{PV1}.

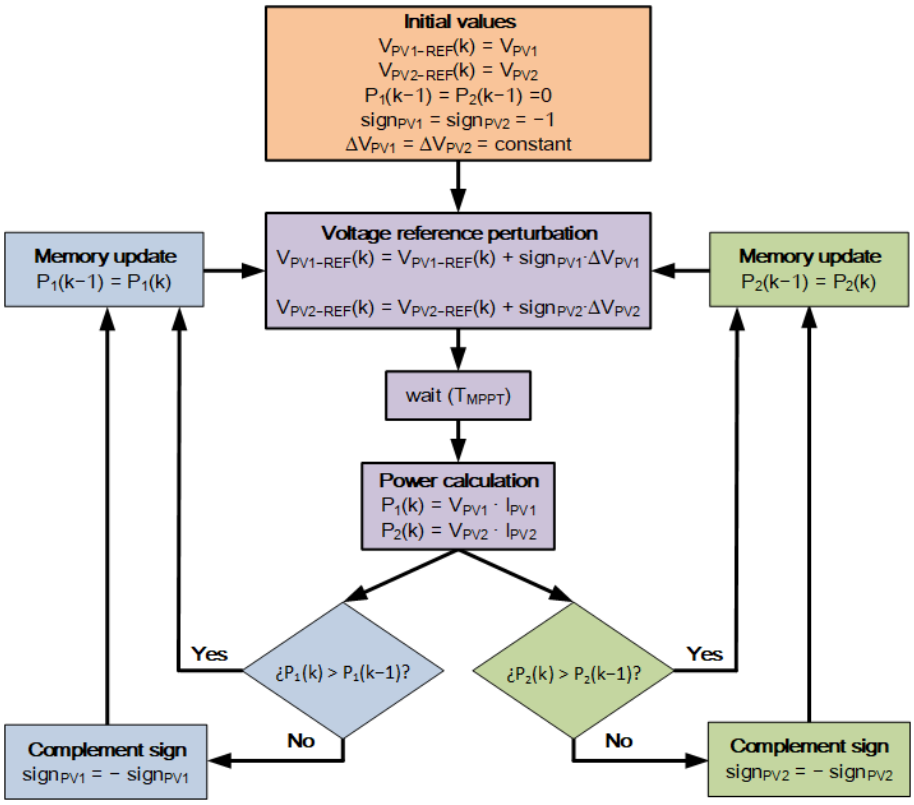

Figure 4. Double P&O MPPT algorithm.

2.1. Model and Control Structure of the Multilevel Half-Bridge NPC PWM Inverter

In this section, the model and the control structure of the multilevel NPC PWM inverter are described. Figure 3 introduces the NPC PWM inverter control structure. It comprises an MPPT P&O algorithm, an output current control loop, and an input voltage control loop.

The MPPT P&O algorithm (Figure 4) perturbs the voltage reference for V_{PV1} ($V_{PV1\text{-}REF}$). If the power obtained from string PV1 (P_{PV1}) increases, the next step value of $V_{PV1\text{-}REF}$ will be applied in the same direction. However, if the power decreases, the next step value of $V_{PV1\text{-}REF}$ will be in the opposite direction.

The voltage references ($V_{PV1\text{-}REF}$, $V_{PV2\text{-}REF}$) generated by the MPPT algorithms are added to create $V_{DC\text{-}REF}$, the input voltage reference for the NPC inverter voltage control loop. The voltage regulator ($G_{V\text{-}NPC}$) adjusts the input voltage to match that reference value. Thus, the output of $G_{V\text{-}NPC}$ is the peak value of the output inductor reference current ($I_{OUT\text{-}REF\_PK}$).

The phase-locked loop (PLL) module ensures that the output current is aligned with the grid voltage phase based on an SRF-PLL [32]. It provides information about the phase angle of the grid. The magnitude $I_{OUT\text{-}REF\_PK}$ multiplied by the cosine of the phase angle provides the instantaneous reference value for the output inductor current ($I_{OUT\text{-}REF}$). The current regulator ($G_{I\text{-}NPC}$) adjusts the output current (I_{OUT}) to match the reference. Furthermore, the current regulator of the NPC inverter must provide a high-quality output waveform, even under distorted grid voltages [33].

The modulator employed In the multilevel NPC inverter uses in-phase disposition (IPD) carrier signals [34]. Figure 5 depicts the IPD modulator concept. The IPD modulator drives the switches IGBT1 to IGBT4 to provide the required inverter output voltage (V_{AB}). Note that the output voltage waveform has three levels (V_{PV1}, 0, and $-V_{PV2}$).

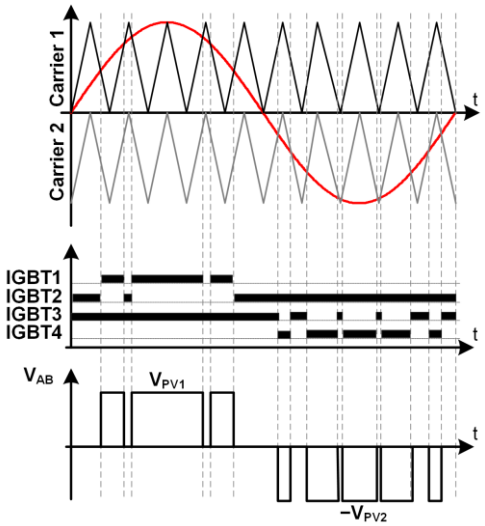

Figure 5. IPD multilevel modulator: three output voltage levels.

Different approaches have been published in the literature to obtain a switching converter's linear model and adjust its control loops. The equivalent matrix structure and mixed logical dynamic (MLD) approaches are specially indicated for NPC inverters with a high number of output voltage levels [35]. Model predictive control (MPC) has fewer bandwidth limitations and a fast dynamic behavior but a variable switching frequency [36]. The modulated model predictive control (MMPC) combines the advantages of the MPC with a constant switching frequency [37]. Fuzzy logic and neural networks controllers can work from imprecise inputs and do not require a precise model [38], but their complexity can be high. Fractional order PID and modulated hysteresis provide very fast transient performance and are easy to implement [39]. The AC small-signal modeling applied to multilevel converters [40] is a powerful technique to obtain a linear model of a switching converter. In this technique, deciding the appropriate control loop structure and determining the variables to be perturbed are essential.

However, when a reduced number of output voltage levels are used, and a constant frequency is desired, the PWM switch model proposed by V.Vorperian for continuous conduction mode (CCM) [41] is a widely used approach. It is a simple and robust method to obtain a linear model of the switching converter, is easy to use and requires a reduced number of equations, thus limiting the mathematical complexity of the model. Additionally, it is unusual to require an ultra-fast dynamic response in PV applications; therefore, Vorperian's model suits most PV applications well.

In this model of the NPC + GCC inverter, the averaged variables are composed of their operating point (OP) value, X, and their small-signal perturbation around the OP, $\hat{x}$, as shown in Equation (1). Note that, in a PWM inverter, some of the OP values have a sinusoidal variation with time at a fundamental frequency much lower than the switching frequency.

$$x = X + \hat{x} \tag{1}$$

Figure 6 depicts the output current path during a switching period to be studied to identify the active (Act), passive (Pas), and common (Com) terminals of Vorperian's model. Thus, the active, common and passive terminals are identified, as shown in Figure 7. The inverter can be replaced during the positive half-cycle of the output voltage, V_{AB}, by the switching cell shown in Figure 7. The study of the negative cycle leads to a circuit equivalent to that presented in this section; thus, only the positive cycle is studied.

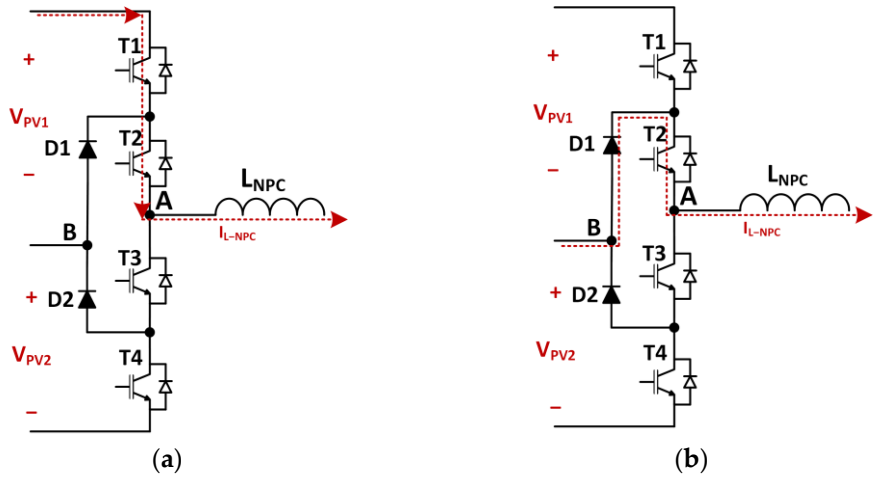

Figure 6. Current path in the positive period of the grid voltage; (**a**) $V_{AB} = +V_{PV1}$; (**b**) $V_{AB} = 0$.

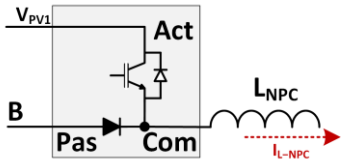

Figure 7. Switching cell during positive half-cycle of the output voltage (Act: active, Pas: passive, Com: common).

The impedance of the electrical grid, L_{GRID}, must be considered for the dynamic study of the inverter. The ratio between the short-circuit current (I_{CC}) and the nominal current of the grid (I_N) permits the grid impedance to be estimated. This impedance, assumed to be inductive, is then calculated in the range of 84 µH (strong electrical grid, $I_{CC} = 20 \cdot I_N$) to 337 µH (weak electrical grid, $I_{CC} = 5 \cdot I_N$).

Thus, by replacing the inverter with the PWM switch cell model and considering the grid impedance, the model shown in Figure 8 is obtained. The model comprises the operating point circuit (OP) and the small-signal circuit (AC). The previous figures' points labeled A and B are kept for clarity. In this model, the diodes and switches are considered ideal devices with no voltage drop.

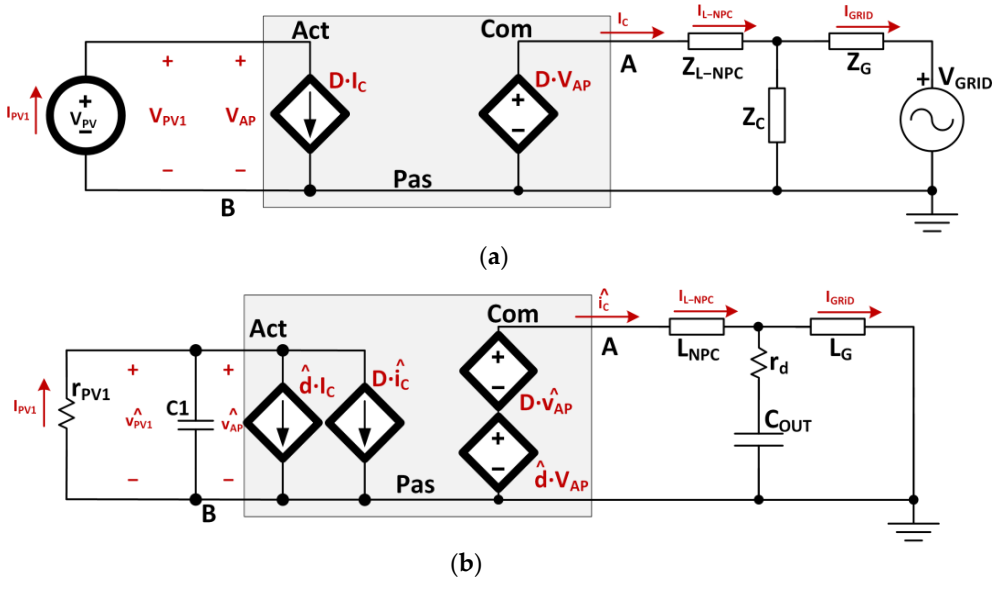

Figure 8. NPC (**a**) operating point circuit (OP); (**b**) small signal circuit (AC).

The values of the parameters of the OP circuit are expressed in (2)–(12), and the small-signal transfer functions are shown in (13)–(16), where 's' is the variable of the Laplace transform. The OP circuit provides the value for the parameters V_{AP}, I_C, and D to be used in the small-signal equations.

The value of V_{AP} is constant (2) since it is the DC value of the input voltage.

$$V_{AP} = V_{PV1} \tag{2}$$

The I_C value is a 50 Hz sinusoidal alternating value. Thus, (3) calculates its precise phasor value. Since the capacitor current in the LCL filter is designed to consume a low current at 50 Hz, the I_C current instantaneous value is almost equal to that injected into the grid and, therefore, is commonly approximated as (4), with a minimum error in most cases. Note that θ is the instantaneous phase value of the grid voltage.

$$\vec{I_C} = \frac{\vec{V_{GRID}}}{\vec{Z_C}} + \left(1 + \frac{\vec{Z_{GRID}}}{\vec{Z_C}}\right) \cdot \vec{I_{GRID}} \tag{3}$$

$$I_C(\theta) \approx \sqrt{2} \cdot I_{GRID-RMS} \cdot \cos(\theta) \tag{4}$$

Solving Figure 8a circuit, the precise phasor value for the duty cycle (D) is calculated through (5). Assuming a pure inductive NPC inductor ($Z_{L\text{-}NPC} = L_{NPC}$) and grid impedance ($Z_G = L_{GRID}$), the real and imaginary parts of D are easily calculated as in (6) and (7). Thus, its magnitude is determined as (8) and its phase value as (9). Hence, the instantaneous value of D is calculated as (10). Note that θ represents the phase value of the grid voltage, and θ_D the phase delay between the duty cycle phasor and the grid voltage one. However, if the phase delay introduced by the LCL filter at 50 Hz is neglected, the instantaneous value of D can be estimated as in (11), with a minimum error in most cases. Note that θ is the instantaneous phase value of the grid voltage.

$$\vec{D} = \frac{\vec{V_{GRID}} + \vec{I_C} \cdot \left[\vec{Z_{L1}} + \vec{Z_{GRID}} \cdot \left(1 + \frac{\vec{Z_{L1}}}{\vec{Z_C}}\right)\right]}{V_{AP} \cdot \left(1 + \frac{\vec{Z_{GRID}}}{\vec{Z_C}}\right)} \tag{5}$$

$$\Re e(D) = \frac{\sqrt{2} \cdot V_{GRID-RMS}}{V_{AP} \cdot (1 - \omega^2 \cdot L_{GRID} \cdot C_{OUT})} \tag{6}$$

$$\mathbb{I}m(D) = \frac{\sqrt{2} \cdot I_{C-RMS} \cdot [\omega \cdot (L_1 + L_{GRID}) - \omega^3 \cdot L_1 \cdot L_{GRID} \cdot C_{OUT}]}{V_{AP} \cdot (1 - \omega^2 \cdot L_{GRID} \cdot C_{OUT})} \tag{7}$$

$$\left|\vec{D}\right| = \sqrt{(\Re e(D))^2 + (\mathbb{I}m(D))^2} \tag{8}$$

$$\theta_D = \tan^{-1}\left(\frac{I_{C-RMS} \cdot [\omega \cdot (L_1 + L_{GRID}) - \omega^3 \cdot L_1 \cdot L_{GRID} \cdot C_{OUT}]}{V_{GRID-RMS}}\right) \tag{9}$$

$$D(\theta) = \sqrt{2} \cdot \left|\vec{D}\right| \cdot \cos(\theta + \theta_D) \tag{10}$$

$$D(\theta) \approx \frac{\sqrt{2} \cdot V_{GRID-RMS} \cdot \cos(\theta)}{V_{AP}} \tag{11}$$

Once the OP parameters are obtained, the small-signal model is obtained by solving the circuit of Figure 8b. First, the small-signal characteristic of the PV modules is determined. It is modeled as a dynamic resistor, according to (12).

$$r_{PV} = \frac{V_{MPP}}{I_{MPP}} \tag{12}$$

From Figure 8b, the duty cycle-to-inductor current transfer function is obtained (15). Additionally, the inductor current-to-input voltage transfer function is of interest (16). The parameters defined in (13) and (14) help to simplify the mathematical functions' transcription.

$$A(s) = \frac{\frac{L_{GRID}}{s} + r_d \cdot L_{GRID} \cdot C_{OUT}}{1 + r_d \cdot C_{OUT} \cdot s + L_{GRID} \cdot C_{OUT} \cdot s^2} \tag{13}$$

$$B(s) = \frac{r_{PV}}{1 + r_{PV} \cdot C_{PV} \cdot s} \tag{14}$$

$$\frac{\hat{i}_C}{\hat{d}}(s) = \frac{V_{AP} - B(s) \cdot I_C \cdot D}{A(s) \cdot s^2 + L_1 \cdot s + D^2 \cdot B(s)} \tag{15}$$

$$\frac{\hat{v}_{PV}}{\hat{i}_C}(s) = B \cdot \frac{I_C \cdot \left(A(s) \cdot s^2 + L_1 \cdot s + 2 \cdot D^2 \cdot B\right) - D \cdot V_{AP}}{V_{AP} - B \cdot I_C \cdot D} \tag{16}$$

Figures 9 and 10 depict the Bode plots of the mathematical model presented in (2)–(17). Figure 9 shows the Bode diagram of the duty-cycle to inductor current ($\hat{i}_C/\hat{d}$) transfer function, the power being 5 kW and the grid inductance L_{GRID} = 337 µH. Figure 10 depicts the Bode plots of the inductor current to PV-input voltage ($\hat{v}_{PV}/\hat{i_C}$) transfer function. In both cases, the grid phase, θ, is a running parameter.

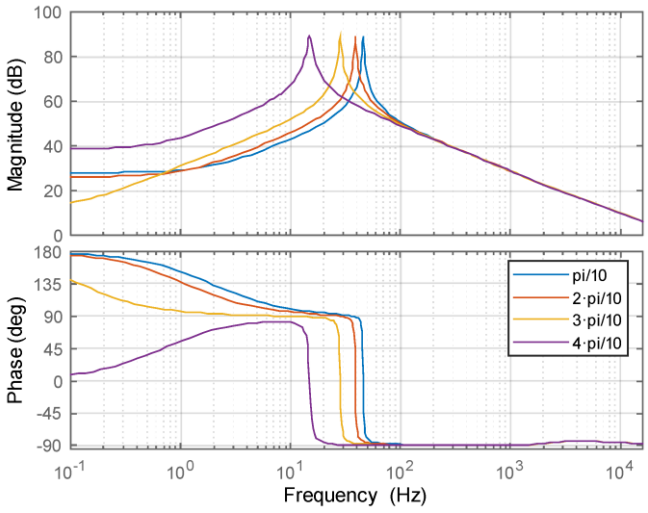

Figure 9. Bode diagram of the transfer function $\hat{i}_C/\hat{d}$. P_{OUT} = 5 kW, L_{GRID} = 337 µH. Grid phase value (θ) as a running parameter. Note: pi = 3.14159.

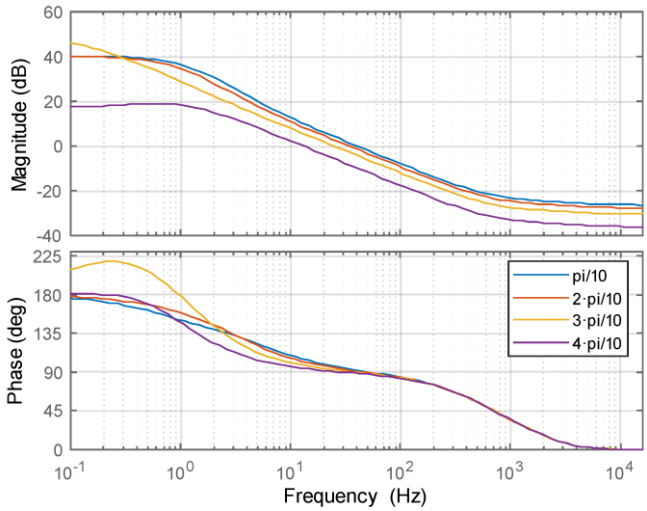

Figure 10. Bode diagram of the transfer function $\hat{v}_{PV}/\hat{i}_C$. P_{OUT} = 5 kW, L_{GRID} = 337 µH. Grid phase value (θ) as a running parameter. Note: pi = 3.14159.

2.2. Model and Control Structure of the GCC DC/DC Converter

Figure 3 shows the GCC DC/DC converter [42] and its control loops (current loop, input voltage loop, and MPPT P&O algorithm). The MPPT P&O algorithm, shown in Figure 4, perturbs the voltage reference for V_{PV2} ($V_{PV2\text{-}REF}$). Similarly, as in the case of $V_{PV1\text{-}REF}$, if the power obtained from string PV2 (P_{PV2}) increases, the next step in the value of $V_{PV2\text{-}REF}$ will be applied in the same direction. If the power decreases, the sign of the next step will be changed.

The voltage regulator ($G_{V\text{-}GCC}$) adjusts the voltage V_{PV2} to match its reference value ($V_{PV2\text{-}REF}$). Then, the output of $G_{V\text{-}GCC}$ is the reference value of the inductor current ($I_{GCC\text{-}REF}$). The voltage of string 2 is adjusted by changing the value of $I_{GCC\text{-}REF}$. The current regulator, $G_{I\text{-}GCC}$, must be able to regulate both positive and negative values of I_{GCC} to provide bidirectional power flow between strings.

Figure 11 shows the modulator used in the GCC converter. The converter switches between the rails of the input voltage; therefore, the voltage at the inductor of the GCC ($V_{L\text{-}GCC}$) ranges between two voltage levels (V_{PV1} and $-V_{PV2}$).

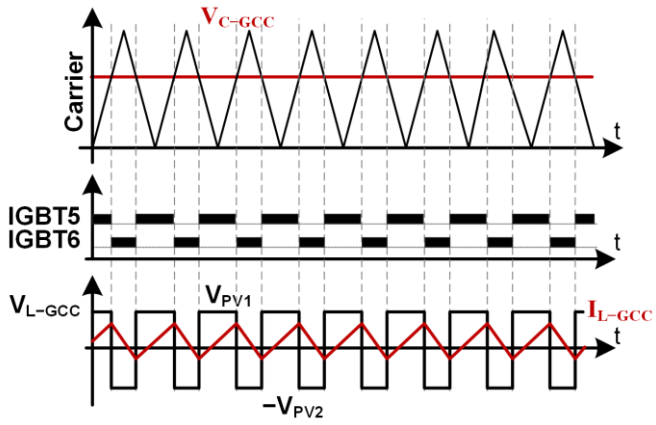

Figure 11. GCC modulator.

The GCC PWM DC/DC converter is modeled using the PWM switch model proposed by V. Vorperian for continuous conduction mode (CCM). To identify the Active (Act), Passive (Pas) and Common (Com) terminals of the Vorperian's model, the path of the output current is studied (Figure 12) during a switching period (positive current in L_{GCC} is

assumed). Thus, the Act-Com-Pas terminals are identified, as shown in Figure 13, and the DC/DC converter is replaced by the switching cell shown in Figure 13.

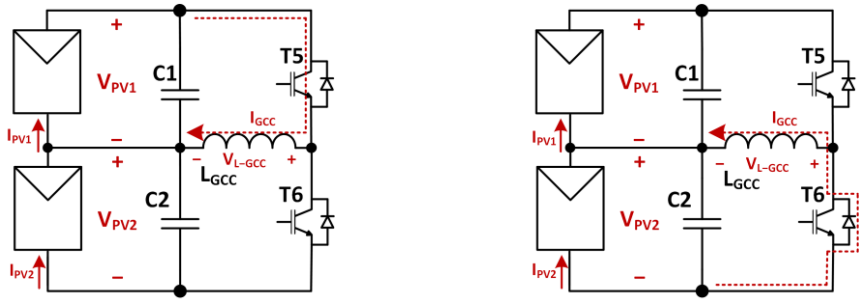

Figure 12. Current path for positive current in L_{GCC}; (**a**) $V_{L\text{-}GCC} = +V_{PV1}$; (**b**) $V_{L\text{-}GCC} = -V_{PV2}$.

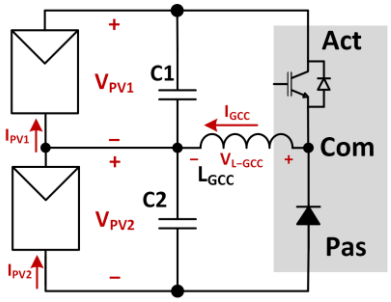

Figure 13. Switching cell for positive current in L_{GCC}.

Thus, by replacing the GCC converter with the switching cell model, the GCC model shown in Figure 14 is obtained. The model is formed by the operating point circuit (DC) and the small-signal circuit (AC). The values for parameters of the operating point circuit are presented in (17)–(19), whereas (20)–(23) show the small-signal transfer functions.

$$\mathrm{V_{AP}} = V_{PV1} + V_{PV2} \tag{17}$$

$$\mathrm{I_C} = I_{PV1} - I_{PV2} \tag{18}$$

$$\mathrm{D} = \frac{V_{PV2}}{V_{PV1} + V_{PV2}} \tag{19}$$

$$\left.\frac{\hat{i}_C}{\hat{d}}(s)\right|_{\hat{i}_{npc}=0} = \frac{\frac{r_{PV}}{1+r_{PV}\cdot C_{PV}\cdot s}\cdot I_C\cdot(2\cdot D-1) - V_{AP}}{\frac{r_{PV}}{1+r_{PV}\cdot C_{PV}\cdot s}\cdot(1-2\cdot D+2\cdot D^2) - L_{GCC}\cdot s} \tag{20}$$

$$\left.\frac{\hat{i}_C}{\hat{i}_{NPC}}(s)\right|_{\hat{d}=0} = \frac{D\cdot\frac{r_{PV}}{1+r_{PV}\cdot C_{PV}\cdot s}}{\frac{r_{PV}}{1+r_{PV}\cdot C_{PV}\cdot s}\cdot(-1+2\cdot D-2\cdot D^2) - L_{GCC}\cdot s} \tag{21}$$

$$\mathrm{A} = \frac{r_{PV}}{1 + r_{PV}\cdot C_{PV}\cdot s} \tag{22}$$

$$\left.\frac{\hat{v}_{PV2}}{\hat{i}_C}(s)\right|_{\hat{i}_{npc}=0} = \frac{A\cdot\left[(V_{AP} - A\cdot D\cdot I_C)\cdot(1-D) - I_C\cdot\left(L_{GCC}\cdot s + A\cdot D^2\right)\right]}{V_{AP} + A\cdot(1-D)} \tag{23}$$

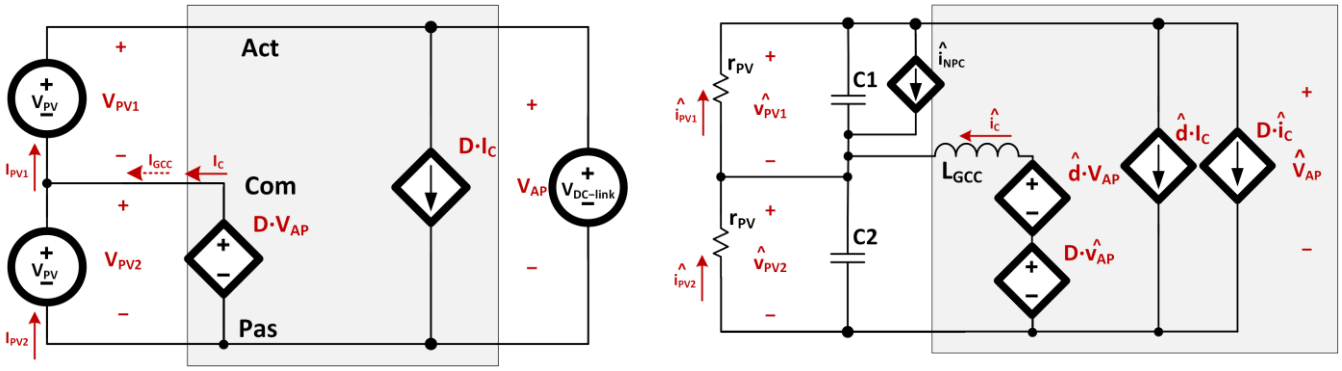

Figure 14. GCC (**a**) operating point circuit (OP); (**b**) small-signal circuit (AC).

Figure 15 shows the Bode plots for the duty-cycle to inductor current ($\hat{i}_C/\hat{d}$) transfer function. Figure 16 depicts the Bode plots for the inductor current to input PV voltage ($\hat{v}_{PV}/\hat{i}_c$) transfer function. In both cases, the dynamic resistance of the photovoltaic string, r_{PV}, is considered a running parameter. These Bode diagrams are obtained using the mathematical model presented in (17)–(23).

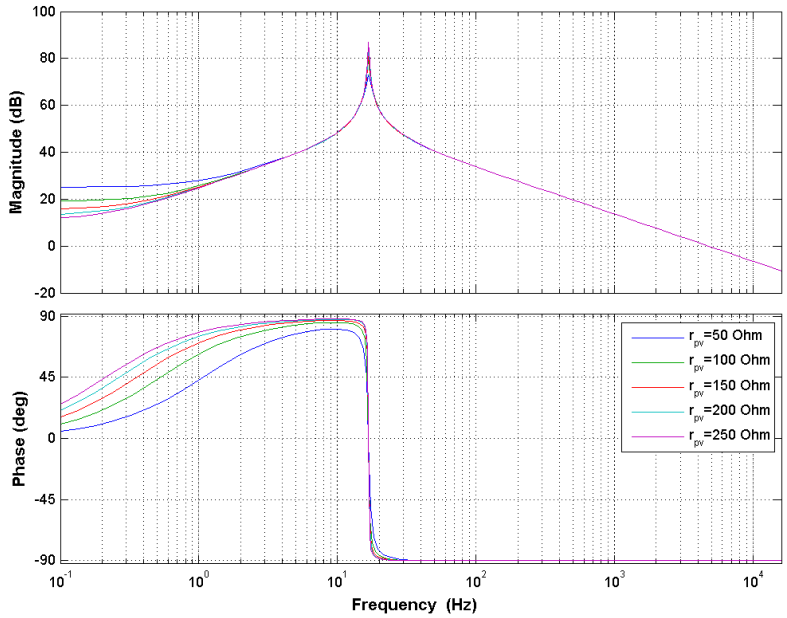

Figure 15. Bode diagram of the transfer function $\hat{i}_C/\hat{d}$. Dynamic resistance of the PV string (r_{PV}) as a running parameter.

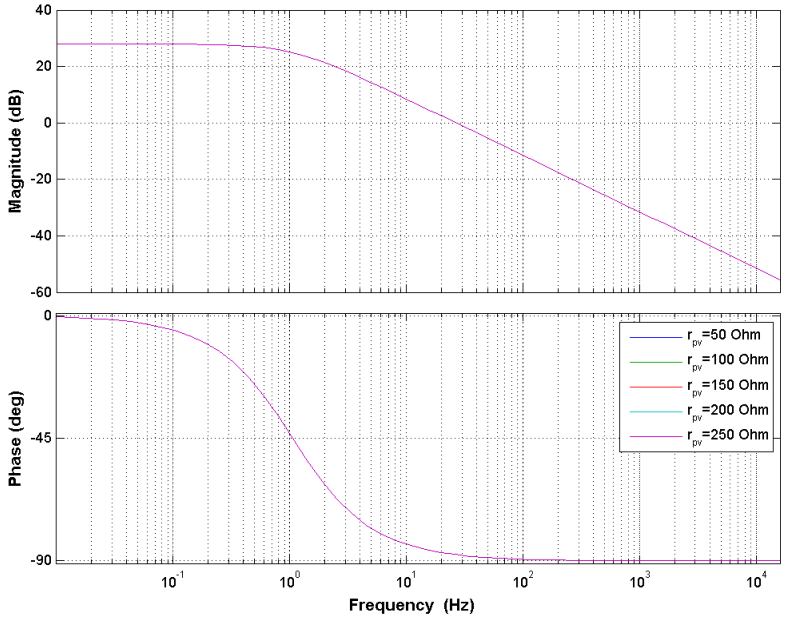

Figure 16. Bode diagram of the transfer function $\hat{v}_{PV}/\hat{i}_C$. Dynamic resistance of the PV string (r_{PV}) as a running parameter (the traces are overlapped).

3. Control Design of NPC PWM Inverter

Figure 17 shows the closed-loop control structure designed using the small-signal model of the NPC inverter. In this figure, several transfer functions blocks appear, which are detailed as follows: $G_{V\text{-}NPC}$ represents the input voltage compensator and $G_{I\text{-}NPC}$ the output current compensator for the NPC inverter; del(s) represents the PWM delay; F_m the PWM modulator gain; $\hat{i}_L/\hat{d}$ stands for the duty cycle-to-output current transfer function and $\hat{v_{PV}}/\hat{i_L}$ for the output current-to-input voltage one; Ri represents the current sensor gain (unitary, due to the digital conversion gain); β represents the voltage sensor gain (unitary, due to the digital conversion gain); and Ant(s) represents the anti-aliasing ADC filters. Table 2 defines several transfer functions of interest.

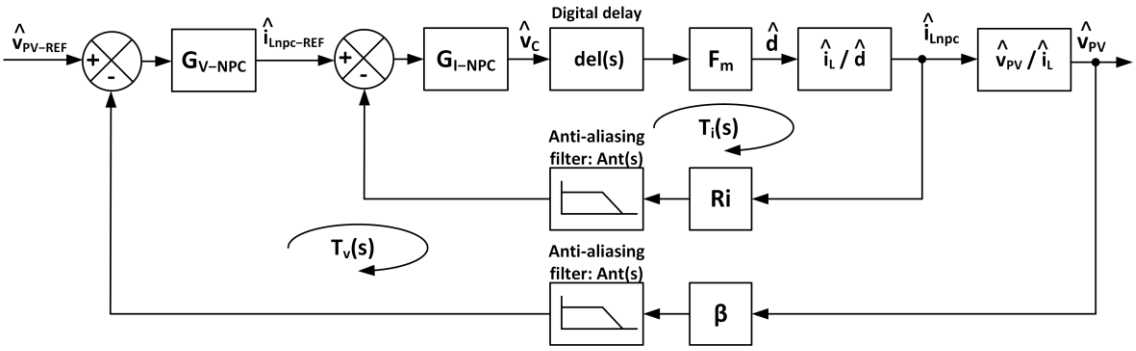

Figure 17. Voltage and current loops for the NPC inverter.

The current regulator, $G_{I\text{-}NPC}$, must provide a high gain at the grid frequency and its harmonics, along with enough attenuation at the switching frequency and proper stability margins. $G_{I\text{-}NPC}$ is based on a P + Resonant structure, implemented in a Texas Instruments TMS320F28335 DSP processor. $G_{I\text{-}NPC}$ has been adjusted to obtain an open loop gain of the current loop, whose Bode plots are shown in Figure 18. In the figure, $T_i(s)$ presents a high gain at the grid frequency and its 3rd, 5th, and 7th harmonics, and a low gain at the switching frequency (16 kHz). The stability of the current loop is guaranteed by the stability margins: 0 dB crossover frequency f_{Ci} = 1.6 kHz, phase margin 50°, and gain margin 10 dB.

Table 2. Gains and transfer functions of the NPC inverter.

Name	Value/Expression
Digital delay of one sampling period (T_S = 31.25 µs), del(s)	$e^{-s \cdot T_S} \approx \frac{1-\frac{s \cdot T_S}{2}+\frac{(s \cdot T_S)^2}{12}}{1+\frac{s \cdot T_S}{2}+\frac{(s \cdot T_S)^2}{12}}$
Modulator gain, F_m	1
Current sensor gain, Ri	1
Voltage sensor gain, β	1
Anti − aliasing filter, Ant(s) ($\omega_0 = 2 \cdot \pi \cdot 8\text{kHz}$)	$Ant(s) = \frac{1}{1+\frac{s}{Q \cdot \omega_0}+\frac{s^2}{\omega_0^2}}$ $Q = \frac{1}{\sqrt{2}}$
Current regulator, $G_{I\text{-}NPC}(s)$	$G_{I-NPC}(s) = 0.05 + \frac{10 \cdot s}{s^2+7 \cdot s+(100 \cdot \pi)^2} + \frac{25 \cdot s}{s^2+21 \cdot s+(300 \cdot \pi)^2} + \frac{30 \cdot s}{s^2+35 \cdot s+(500 \cdot \pi)^2} + \frac{35 \cdot s}{s^2+49 \cdot s+(700 \cdot \pi)^2}$
Closed loop response of the output current to its reference	$T_{i-lc}(s) = \frac{\hat{i}_L(s)}{\hat{i}_{L-REF}(s)} = \frac{1}{R_i} \cdot \frac{T_i(s)}{1+T_i(s)}$
Voltage regulator, $G_{V\text{-}NPC}(s)$	$G_{V-NPC}(s) = \frac{-4 \cdot (1+s/20)}{s}$
Loop gain of the voltage loop, $T_V(s)$	$T_V(s) = G_{V-NPC}(s) \cdot T_{i-lc}(s) \cdot \frac{\hat{v}_{PV}(s)}{\hat{i}_C(s)} \cdot \beta$
Closed loop response of the output current to its reference	$\frac{\hat{v_{PV}}(s)}{\hat{v}_{PV-REF}(s)} = \frac{1}{\beta} \cdot \frac{T_V(s)}{1+T_V(s)}$

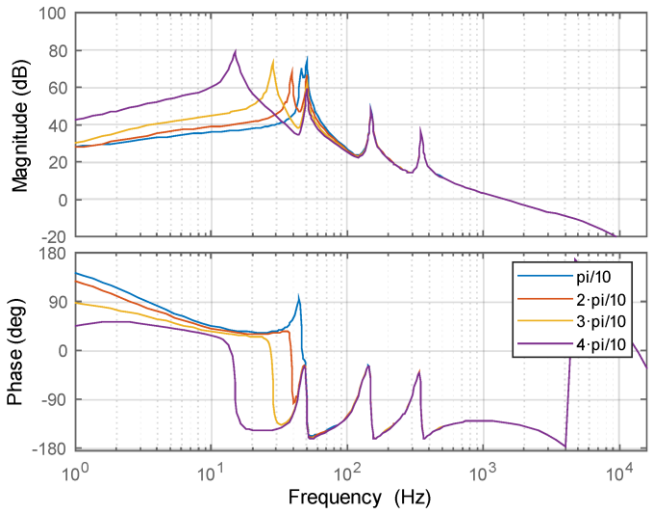

Figure 18. NPC control: Bode diagram of $T_i(s)$. P_{OUT} = 5 kW, L_{GRID} = 337 µH. Grid phase value (ω·t) in the legend. Note: pi = 3.14159.

The voltage regulator, $G_{V\text{-}NPC}$, must provide a high gain at DC and a low gain at the grid frequency to minimize the distortion in the output current due to the low-frequency voltage ripple at the DC link, whose frequency agrees with the grid frequency in an NPC half-bridge inverter. The proposed structure for the voltage regulator is a proportional integrator (PI). $G_{V\text{-}NPC}$ is adjusted to obtain the open loop gain (T_V) shown in Figure 19. The stability of the voltage loop is guaranteed by the stability margins: crossover frequency f_{CV} = 3.4 Hz to 9 Hz, phase margin > 65°, and gain margin > 35 dB. The gain at 50 Hz is −16 dB, thus attenuating the influence of the input voltage ripple in the output current.

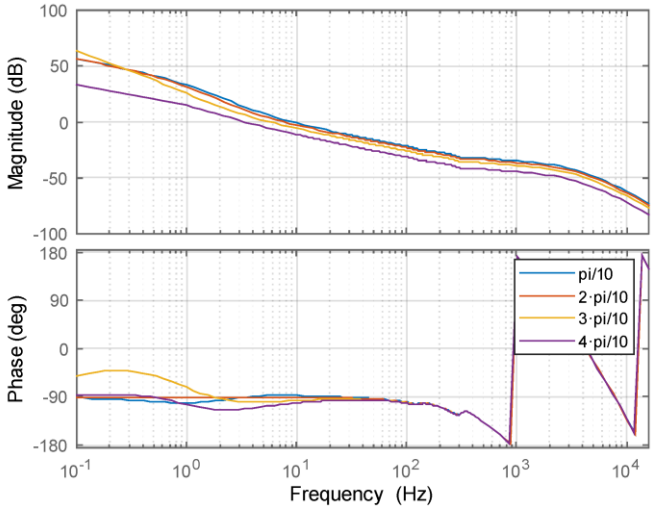

Figure 19. NPC control: Bode diagram of $T_V(s)$. P_{OUT} = 5 kW, L_{GRID} = 337 µH. Grid phase value ($\omega \cdot t$) as a running parameter. Note: pi = 3.14159.

4. Control Design of GCC DC/DC Converter

Figure 20 shows the closed-loop control structure using the small-signal model of the GCC converter, where several transfer functions of interest, defined in Table 3, can be identified.

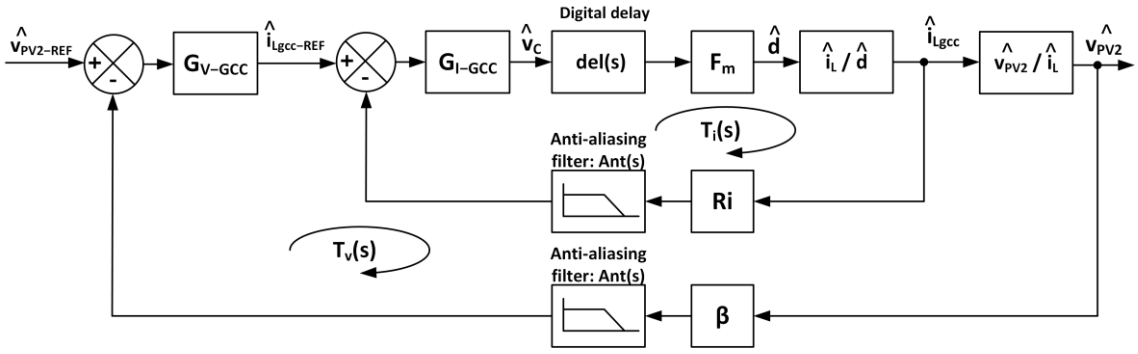

Figure 20. Voltage and current loops for the GCC converter.

Table 3. Gains and transfer functions of the GCC converter.

Name	Value/Expression
Digital delay of one sampling period (T_S = 31.25 µs), del(s)	$e^{-s \cdot T_S} \approx \frac{1-\frac{s \cdot T_S}{2}+\frac{(s \cdot T_S)^2}{12}}{1+\frac{s \cdot T_S}{2}+\frac{(s \cdot T_S)^2}{12}}$
Modulator gain, F_m	1
Current sensor gain, Ri	1
Voltage sensor gain, β	1
Anti − aliasing filter, Ant(s) ($\omega_0 = 2 \cdot \pi \cdot 8$kHz)	$Ant(s) = \frac{1}{1+\frac{s}{Q \cdot \omega_0}+\frac{s^2}{\omega_0^2}}$ $Q = \frac{1}{\sqrt{2}}$
Current regulator, $G_{I\text{-}GCC}(s)$	$G_{I-GCC}(s) = \frac{15}{s} \cdot \frac{1+\frac{s}{200}}{1+\frac{s}{30000}}$

Table 3. *Cont.*

Name	Value/Expression
Loop gain of the current loop, $T_i(s)$	$T_i(s) = G_{I-GCC}(s) \cdot del(s) \cdot Fm \cdot \frac{\hat{i}_L(s)}{\hat{d}(s)} \cdot Ri \cdot Ant(s)$
Closed loop response of the output current to its reference	$\frac{\hat{i}_L(s)}{\hat{i}_{L-REF}(s)} = \frac{1}{R_i} \cdot \frac{T_i(s)}{1+T_i(s)}$
Voltage regulator, $G_{V\text{-}GCC}(s)$	$G_{V-GCC}(s) = \frac{1+\frac{s}{5}}{s}$
Loop gain of the voltage loop, $T_V(s)$	$T_V(s) = G_{V-NPC}(s) \cdot T_{i-lc}(s) \cdot \frac{\hat{v}_{PV2}(s)}{\hat{i}_C(s)} \cdot \beta$
Closed loop response of the output current to its reference	$\frac{\hat{v}_{PV2}(s)}{\hat{v}_{PV2-REF}(s)} = \frac{1}{\beta} \cdot \frac{T_V(s)}{1+T_V(s)}$

In this case, the current regulator, G_{I_GCC}, must provide a high gain at DC, enough attenuation at the switching frequency, and proper stability margins. G_{I_GCC} is a PI regulator implemented in the digital controller and adjusted to obtain the open loop gain, $T_i(s)$, shown in Figure 21. The main stability margins observed from this figure are as follows: crossover frequency 350–40 Hz, phase margin > 75°, and gain margin > 20 dB.

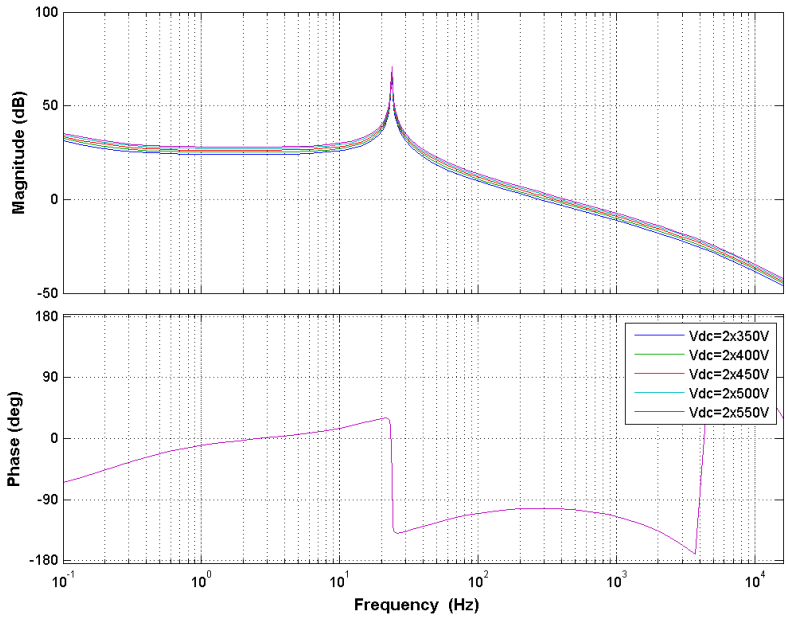

Figure 21. GCC control: Bode diagram of $T_i(s)$. DC link voltage as a running parameter.

The voltage regulator, $G_{V\text{-}GCC}$, adjusts the voltage V_{PV2} to match the reference value, $V_{PV2\text{-}REF}$. $G_{V\text{-}GCC}$ must provide a high gain at DC to guarantee a null error in tracking the steady state reference current. $G_{V\text{-}GCC}$ is adjusted to obtain the open loop gain (T_V) of Figure 22. The stability margins guarantee the stability of the voltage loop: crossover frequency 6 Hz, phase margin 85°, and gain margin 45 dB.

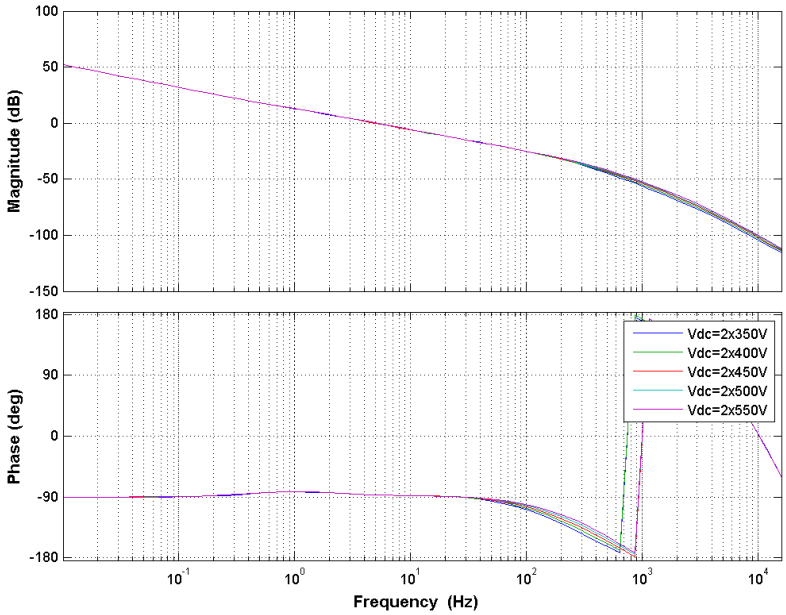

Figure 22. GCC control: Bode diagram of $T_V(s)$. DC input voltage in the legend.

5. Conclusions

In this paper, the modeling of the NPC + GCC topology is presented. OP (operating point) and AC (small-signal) equivalent circuits for the NPC inverter and GCC DC/DC converter have been obtained. The NPC + GCC topology has a pair of converters working in parallel. As a result, both PV input voltages can be controlled independently. Additionally, its model and stability study are carried out independently as well.

By using the small-signal model presented, both converters' current and voltage controllers have been designed in the frequency domain. Moreover, the stability margins are obtained and evaluated to ensure the designed control's robustness.

The low-frequency ripple in the input capacitors, inherent in the half-bridge topologies, is addressed here in the control loops. The designed voltage compensators have a very low gain at the grid frequency. Hence, they do not respond to that ripple.

Author Contributions: Conceptualization, I.P., E.F. and G.G.; methodology I.P. and M.L.; validation I.P., M.L. and R.G.-M.; software I.P. and E.T.; formal analysis, I.P., M.L. and G.G.; writing—original draft preparation, I.P., M.L. and G.G.; supervision, G.G. and E.F.; project administration, G.G. and E.F.; funding acquisition G.G. and E.F. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the Spanish "Ministerio de Asuntos Económicos y Transformación Digital" and the European Regional Development Fund (ERDF), under grant PID2021-122835OB-C22.

Data Availability Statement: No data were created.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Patrao, I.; Figueres, E.; González-Espín, F.; Garcerá, G. Transformerless topologies for grid-connected single-phase photovoltaic inverters. *Renew. Sustain. Energy Rev.* **2011**, *15*, 3423–3431. [CrossRef]
2. Liberos, M.; González-Medina, R.; Garcerá, G.; Figueres, E. A Method to Enhance the Global Efficiency of High-Power Photovoltaic Inverters Connected in Parallel. *Energies* **2019**, *12*, 2219. [CrossRef]
3. Vo, D.-V.; Nguyen, K.M.; Lim, Y.-C.; Choi, J.-H. A Single-Stage Bimodal Transformerless Inverter with Common-Ground and Buck-Boost Features. *Electronics* **2023**, *12*, 221. [CrossRef]
4. Amoiralis, E.I.; Tsili, M.A.; Kladas, A.G. Power Transformer Economic Evaluation in Decentralized Electricity Markets. *IEEE Trans. Ind. Electron.* **2011**, *59*, 2329–2341. [CrossRef]

5. Kefalas, T.D.; Kladas, A.G. Analysis of Transformers Working Under Heavily Saturated Conditions in Grid-Connected Renewable-Energy Systems. *IEEE Trans. Ind. Electron.* **2011**, *59*, 2342–2350. [CrossRef]
6. Araujo, S.; Zacharias, P.; Sahan, B. Novel grid-connected non-isolated converters for photovoltaic systems with grounded generator. In Proceedings of the 2008 IEEE Power Electronics Specialists Conference, Rhodes, Greece, 15–19 June 2008; pp. 58–65. [CrossRef]
7. Li, W.; Gu, Y.; Luo, H.; Cui, W.; He, X.; Xia, C. Topology Review and Derivation Methodology of Single-Phase Transformerless Photovoltaic Inverters for Leakage Current Suppression. *IEEE Trans. Ind. Electron.* **2015**, *62*, 4537–4551. [CrossRef]
8. Wang, L.; Chen, L.; Ye, W.; Ma, W. Phase-Shifted Energy Balance Control for Multilevel Inverters in Grid-Connected PV Systems. *Electronics* **2023**, *12*, 2582. [CrossRef]
9. Chen, B.; Gu, B.; Zhang, L.; Zahid, Z.U.; Lai, J.-S.; Liao, Z.; Hao, R. A High-Efficiency MOSFET Transformerless Inverter for Nonisolated Microinverter Applications. *IEEE Trans. Power Electron.* **2014**, *30*, 3610–3622. [CrossRef]
10. Kerekes, T.; Teodorescu, R.; Rodriguez, P.; Vazquez, G.; Aldabas, E. A New High-Efficiency Single-Phase Transformerless PV Inverter Topology. *IEEE Trans. Ind. Electron.* **2009**, *58*, 184–191. [CrossRef]
11. Salas, V.; Olías, E. Overview of the state of technique for PV inverters used in low voltage grid-connected PV systems: Inverters below 10kW. *Renew. Sustain. Energy Rev.* **2009**, *13*, 1541–1550. [CrossRef]
12. Xiao, H.F.; Lan, K.; Zhang, L. A Quasi-Unipolar SPWM Full-Bridge Transformerless PV Grid-Connected Inverter with Constant Common-Mode Voltage. *IEEE Trans. Power Electron.* **2014**, *30*, 3122–3132. [CrossRef]
13. López, Ó.; Freijedo, F.D.; Yepes, A.G.; Fernández-Comesaña, P.; Malvar, J.; Teodorescu, R.; Doval-Gandoy, J. Eliminating Ground Current in a Transformerless Photovoltaic Application. *IEEE Trans. Energy Convers.* **2010**, *25*, 140–147. [CrossRef]
14. Gonzalez, R.; Gubia, E.; Lopez, J.; Marroyo, L. Transformerless Single-Phase Multilevel-Based Photovoltaic Inverter. *IEEE Trans. Ind. Electron.* **2008**, *55*, 2694–2702. [CrossRef]
15. Tang, Y.; Yao, W.; Loh, P.C.; Blaabjerg, F. Highly Reliable Transformerless Photovoltaic Inverters with Leakage Current and Pulsating Power Elimination. *IEEE Trans. Ind. Electron.* **2015**, *63*, 1016–1026. [CrossRef]
16. Vazquez, N.; Rosas, M.; Hernandez, C.; Vazquez, E.; Perez-Pinal, F.J. A New Common-Mode Transformerless Photovoltaic Inverter. *IEEE Trans. Ind. Electron.* **2015**, *62*, 6381–6391. [CrossRef]
17. Zhou, L.; Gao, F. Low leakage current single-phase PV inverters with universal neutral-point-clamping method. In Proceedings of the 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 20–24 March 2016; pp. 410–416. [CrossRef]
18. Patrao, I.; Garcerá, G.; Figueres, E.; González-Medina, R. Grid-tie inverter topology with maximum power extraction from two photovoltaic arrays. *IET Renew. Power Gener.* **2014**, *8*, 638–648. [CrossRef]
19. Zhang, Q.; Sun, X.; Zhong, Y.; Matsui, M. A Novel Topology for Solving the Partial Shading Problem in Photovoltaic Power Generation System. In Proceedings of the 2009 IEEE 6th International Power Electronics and Motion Control Conference, Wuhan, China, 17–20 May 2009; pp. 2130–2135.
20. Daher, S.; Schmid, J.; Antunes, F.L.M. Multilevel Inverter Topologies for Stand-Alone PV Systems. *IEEE Trans. Ind. Electron.* **2008**, *55*, 2703–2712. [CrossRef]
21. Kjaer, S.; Pedersen, J.; Blaabjerg, F. A Review of Single-Phase Grid-Connected Inverters for Photovoltaic Modules. *IEEE Trans. Ind. Appl.* **2005**, *41*, 1292–1306. [CrossRef]
22. Memon, R.; Mahar, M.A.; Larik, A.S.; Shah, S.A.A. Design and Performance Analysis of New Multilevel Inverter for PV System. *Sustainability* **2023**, *15*, 10629. [CrossRef]
23. Debdouche, N.; Deffaf, B.; Benbouhenni, H.; Laid, Z.; Mosaad, M.I. Direct Power Control for Three-Level Multifunctional Voltage Source Inverter of PV Systems Using a Simplified Super-Twisting Algorithm. *Energies* **2023**, *16*, 4103. [CrossRef]
24. Zaid, S.A.; Bakeer, A.; Albalawi, H.; Alatwi, A.M.; Abdeldaim, H.; Manqarah, B. Model-Free Predictive Current Control of a 3-φ Grid-Connected Neutral-Point-Clamped Transformerless Inverter. *Energies* **2023**, *16*, 3141. [CrossRef]
25. Alghamdi, T.A.; Anayi, F.; Packianather, M. Modelling and Control Development of a Cascaded NPC-Based MVDC Converter for Harmonic Analysis Studies in Power Distribution Network. *Energies* **2022**, *15*, 4867. [CrossRef]
26. Serban, E.; Ordonez, M.; Pondiche, C.; Hulea, D. Voltage and Power Balancing in Solar and Energy Storage Converters. In Proceedings of the 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA, 29 September–3 October 2019; pp. 5832–5839. [CrossRef]
27. Ji, Y.-H.; Jung, D.-Y.; Kim, J.-G.; Kim, J.-H.; Lee, T.-W.; Won, C.-Y. A Real Maximum Power Point Tracking Method for Mismatching Compensation in PV Array Under Partially Shaded Conditions. *IEEE Trans. Power Electron.* **2010**, *26*, 1001–1009. [CrossRef]
28. De Brito, M.A.G.; Galotto, L.; Sampaio, L.P.; Melo, G.D.A.E.; Canesin, C.A. Evaluation of the Main MPPT Techniques for Photovoltaic Applications. *IEEE Trans. Ind. Electron.* **2013**, *60*, 1156–1167. [CrossRef]
29. Lim, Z.; Tafti, H.D.; Pinkymol, H.R. Multilevel Modulation Methods. In *Advanced Multilevel Converters and Applications in Grid Integration*; Maswood, A.I., Tafti, H.D., Eds.; John Wiley & Sons: Chichester, UK, 2018. [CrossRef]
30. Ram, J.P.; Babu, T.S.; Rajasekar, N. A comprehensive review on solar PV maximum power point tracking techniques. *Renew. Sustain. Energy Rev.* **2017**, *67*, 826–847. [CrossRef]
31. Mastromauro, R.A.; Liserre, M.; Dell'Aquila, A. Control Issues in Single-Stage Photovoltaic Systems: MPPT, Current and Voltage Control. *IEEE Trans. Ind. Inform.* **2012**, *8*, 241–254. [CrossRef]

32. Golestan, S.; Monfared, M.; Freijedo, F.D. Design-Oriented Study of Advanced Synchronous Reference Frame Phase-Locked Loops. *IEEE Trans. Power Electron.* **2012**, *28*, 765–778. [CrossRef]
33. Gazoli, J.R.; Villalva, M.G.; Siqueira, T.G.; Ruppert, E. Micro-Inverter for Integrated Grid-Tie PV Module Using Resonant Controller. In Proceedings of the 2012 IEEE Power and Energy Society General Meeting, San Diego, CA, USA, 22–26 July 2012; pp. 1–8.
34. Lan, Z.; Li, Y.; Li, C.; Zhu, C.; Wang, C. Investigation on IGCT-Based NPC/H-Bridge Large Power Converter. In Proceedings of the 2012 IEEE Energy Conversion Congress and Exposition (ECCE), Raleigh, NC, USA, 15–20 September 2012; pp. 726–730.
35. Feng, T.; Chen, C.; Li, J.; Zhang, H.; Wang, K. Research on the modeling method of NPC three-phase three-level inverter. In Proceedings of the 2020 Chinese Automation Congress (CAC), Shanghai, China, 6–8 November 2020; pp. 3808–3813. [CrossRef]
36. Kong, D.; Zhang, Z.; Liu, C.; Tian, W.; Gao, X.; Kennel, R. Modulated Model Predictive Control of Power Electronics Transformer Based on Isolated Modular Multilevel Converter. In Proceedings of the 2021 IEEE International Conference on Predictive Control of Electrical Drives and Power Electronics (PRECEDE), Jinan, China, 20–22 November 2021; pp. 831–835. [CrossRef]
37. Yoon, H.; Cho, Y. Modulated Model Predictive Current Control for Three-Phase NPC Inverter with an LC Filter. In Proceedings of the 2022 5th International Conference on Power Engineering and Renewable Energy (ICPERE), Bandung, Indonesia, 22–23 November 2022; Volume 1, pp. 1–5. [CrossRef]
38. Boumaaraf, H.; Talha, A.; Bouhali, O. A three-phase NPC grid-connected inverter for photovoltaic applications using neural network MPPT. *Renew. Sustain. Energy Rev.* **2015**, *49*, 1171–1179. [CrossRef]
39. Rasoanarivo, I.; Arab-Tehrani, K.; Sargos, F.-M. Fractional Order PID and Modulated Hysteresis for high performance current control in multilevel inverters. In Proceedings of the 2011 IEEE Industry Applications Society Annual Meeting, Orlando, FL, USA, 9–13 October 2011; pp. 1–7. [CrossRef]
40. Pimentel, S.P.; Husev, O.; Stepenko, S.; Vinnikov, D.; Roncero-Clemente, C.; Makovenko, E. Voltage Control Tuning of a Single-Phase Grid-Connected 3L qZS-Based Inverter for PV Application. In Proceedings of the 2018 IEEE 38th International Conference on Electronics and Nanotechnology (ELNANO), Kyiv, Ukraine, 24–26 April 2018; pp. 692–698. [CrossRef]
41. Vorperian, V. Simplified analysis of PWM converters using model of PWM switch. Continuous conduction mode. *IEEE Trans. Aerosp. Electron. Syst.* **1990**, *26*, 490–496. [CrossRef]
42. Shimizu, T.; Hirakata, M.; Kamezawa, T.; Watanabe, H. Generation control circuit for photovoltaic modules. *IEEE Trans. Power Electron.* **2001**, *16*, 293–300. [CrossRef]