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Performance Evaluation of the B4 Topology for Implementing Grid-Connected Inverters in Microgrids

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Abstract: The B4 topology is an interesting alternative to the conventional B6 inverter due to its reduced number of parts and lower cost. Although it has been widely used in the past, especially in low-power motor drive applications, its application as a grid-connected inverter is an open area of research. In this regard, this paper analyses the feasibility of the B4 inverter topology for grid-connected applications. A versatile 7 kW inverter prototype, which may be configured as B4 and B6, was built, allowing for a comprehensive evaluation of the performance of both topologies. Through an analytical study and experimental tests, the performance of the B4 and B6 topologies was comparatively evaluated in terms of efficiency, total harmonic distortion of line currents, current unbalance, cost, and mean time between failures. The study was carried out in the context of microgrid systems, highlighting their role in the integration of renewable energy and distributed generation.

Keywords: four-switch inverter; microgrid; performance evaluation; cost estimation; reliability analysis

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1. Introduction

In the pursuit of a more sustainable and resilient energy future, the concepts of microgrids, decentralised production of energy, and renewable energy sources are viewed as transformative forces in the global energy landscape [1,2]. Traditional centralised power generation and distribution systems, usually characterised by large-scale power plants and extensive transmission networks, face challenges related to environmental impact, reliability, and adaptability to rapidly evolving technological advancements [3,4]. In response to these challenges, there has been a major shift towards decentralised energy production through microgrids, coupled with the utilisation of renewable energy sources.

In this aspect, microgrids offer a localised and more flexible approach to power generation and consumption. These self-contained systems integrate various distributed energy resources, such as solar panels, wind turbines, and energy storage systems, creating resilient and adaptive energy networks. The decentralisation of energy production not only enhances energy security [5], but also reduces the dependence on centralised grids and mitigates transmission losses [6].

With the appearance of small photovoltaic solar energy producers, many types of power converters have appeared that make use of this energy source [7], from standalone systems to grid-connected ones [8,9]. The more traditional grid-connected inverters fed all the available energy into the grid, while more advanced ones use batteries to accumulate excess energy at off-peak hours [10]. Some topologies have been proposed to feed critical loads during times of blackout [11]. Others solutions have been proved to be able to compensate for current harmonics [12]. Finally, some topologies are capable of accumulating surpluses of solar energy in electric vehicles [13]. Furthermore, this allows its use when the grid has a greater demand, increasing grid stability [14,15].

In this landscape, the B4 converter may be an alternative to classic inverters. The B4 is a type of inverter where one of its legs is replaced by a capacitor bank and the third

phase is obtained from its midpoint. This topology has been previously used in low-power motor-drive applications, mainly due to its reduced number of parts and lower cost [16]. Figure 1 shows the B4 inverter topology.

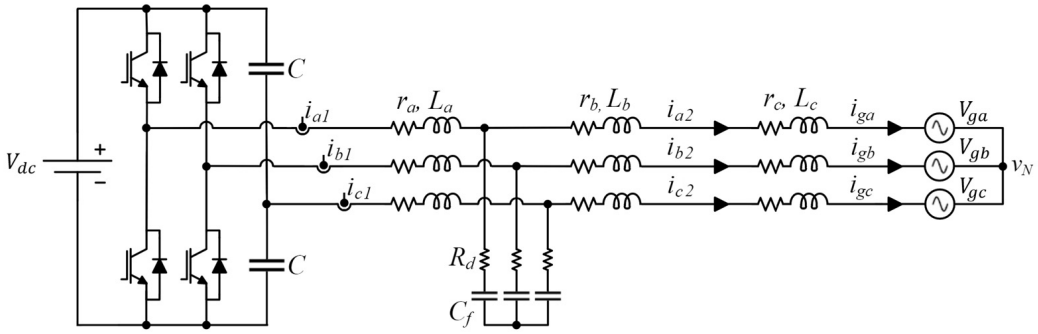

Figure 1. B4 inverter topology.

In Figure 1, the B4 inverter is connected to the grid via an LCL filter, formed by {r_a, L_a}, {r_b, L_b}, and {r_d, C_f}. The {r_c, L_c} set represents the grid impedance. Although three current sensors are depicted in Figure 1, they are not necessary. Two sensors would suffice, as the sum of the currents in each line is 0. The same principle applies to the voltage sensors shown in later figures.

However, this topology has two main drawbacks. Firstly, as one of the currents of the three lines flows through the capacitor bank, a voltage ripple is generated which limits the maximum power that the converter can process. Secondly, under the same operating conditions, a DC voltage $\sqrt{3}$ times higher is required for the inverter to operate at the same operating point of the PWM modulator.

This work aims to carry out a suitability evaluation of the B4 topology for grid-connected operation. The figures of merit chosen for this study are the efficiency, the total harmonic distortion of the current in the grid (THD_I), the unbalance of the grid currents, the cost, and the mean time between failures. To conduct the comparative analysis, a 7 kW inverter has been built. This inverter can be configured as either B4 or B6 and it has been connected to an experimental low power microgrid available in the laboratory. A power analyser is used to quantify efficiency, THD, and current unbalance.

The outline of the work is as follows. After the introduction section, the fundamentals of the B4 topology are presented in Section 2, followed by an analysis of the control algorithm for a B4 inverter in Section 3. Subsequently, Section 4 explains the experimental setup, while Section 5 presents the obtained experimental results, including a comparison of both B4 and B6 topologies, in terms of performance, costs and reliability. Finally, the conclusions drawn from the study are presented in Section 6.

2. Fundamentals of the B4 Topology

2.1. Analysis of the Equivalent Circuit at Fundamental Frequency

In the B4 topology, only four gate signals are needed, as there are only four switches to be controlled. As explained in [17], Fortescue's theorem is applied to analyse this topology. The midpoint of the capacitor bank has been taken as the voltage reference (point 0), as shown in Figure 2a. The fundamental voltages generated by the two active phases are V_{A0} and V_{B0}, while the voltage in the third phase is $V_{C0} = 0$. Applying Fortescue's theorem yields the circuit depicted in Figure 2b, where the generated voltages establish an unbalanced system with V_{A0} and V_{B0} shifted by 60°, as explained in [18].

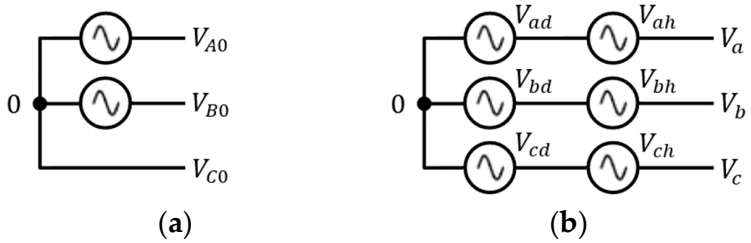

Figure 2. Fortescue's theorem application. (**a**) B4 inverter and (**b**) equivalent circuit.

Equations (1)–(3) are derived from Figure 2b, which show that the fundamental of the inverter phase voltages can be decomposed into a system of positive sequence voltages and a zero-sequence component. The zero-sequence components disappear in the phase-to-phase voltages.

$$V_{A0} = V_{ad} + V_{ah} \tag{1}$$

$$V_{B0} = V_{bd} + V_{bh} \tag{2}$$

$$V_{C0} = V_{cd} + V_{ch} = 0 \tag{3}$$

In Equations (1)–(3), V_{ad}, V_{bd}, and V_{cd} are the positive sequence voltages, while V_{ah}, V_{bh}, V_{ch} are the zero sequence voltages of phases A, B, and C, respectively. Considering that the homopolar phasors have the same magnitude, Equation (1) can be rewritten as:

$$V_{ah} = V_{bh} = V_{ch} \tag{4}$$

$$V_{A0} = V_{ad} + V_{ch} \tag{5}$$

$$V_{A0} = V_{ad} - V_{cd} \tag{6}$$

Figure 3 shows the vector composition used to obtain V_{A0}.

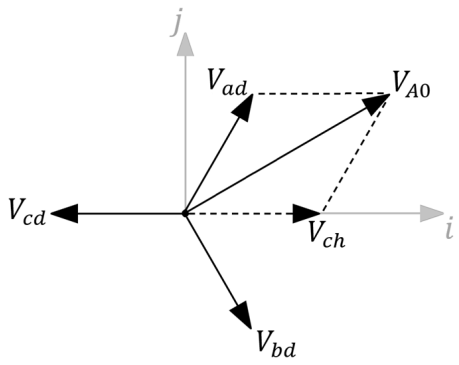

Figure 3. Phasor V_{A0}.

From Equation (6) the gate signals can be calculated as Equations (7) and (8), where v_a, v_b, and v_c are the control signals obtained after performing the inverse DQ0 transformation [17] and $v_{\hat{a}}$ and $v_{\hat{b}}$ are the actual signals that the modulator uses to generate the PWM for the two active phases.

$$v_{\hat{a}} = v_a - v_c \tag{7}$$

$$v_{\hat{b}} = v_b - v_c \tag{8}$$

2.2. Power Transfer Capability

As the positive-sequence phasors V_{ad}, V_{bd}, and V_{cd} have the same magnitude and are shifted 120° degrees apart, the phasor V_{A0} from Equation (6) can expressed as Equation (9) and its module as Equation (10).

$$V_{A0} = V_{ad}i + V_{ad} \cdot \cos(60^\circ)i + V_{ad} \cdot \sin(60^\circ)j \tag{9}$$

$$|V_{A0}| = |V_{ad}| \cdot \sqrt{3} \tag{10}$$

As a result, the fundamental voltages generated by the two remaining active phases in the B4 inverter must be $\sqrt{3}$ times higher to connect to the same voltage grid as B6. Therefore, a $\sqrt{3}$ times higher DC bus voltage is needed to work at the same operating point of the PWM modulator. This issue is probably the major drawback of the B4 topology.

2.3. Capacitor Current and Voltage Ripples

As stated before, the other drawback of the B4 topology is the voltage ripple that appears at the midpoint of the capacitor bank. This ripple appears due to the internal impedance of the capacitors and the current flowing through them. The presence of ripple in the system modifies the voltage of the non-active phase, thereby changing the operating point of the PWM modulator. Consequently, the power transfer capability of the inverter must be limited, preventing operation within the overmodulation zone.

The third, non-active phase can be modelled as a capacitor with an equivalent value of 2C, along with a current source in parallel [18], as Figure 4 shows. Note that C is the value of the capacitors that are connected in series to create the midpoint 0, as shown in Figure 1. The current source in the model is the current of the non-active phase, i_{c1}, while ΔV_C is the voltage ripple.

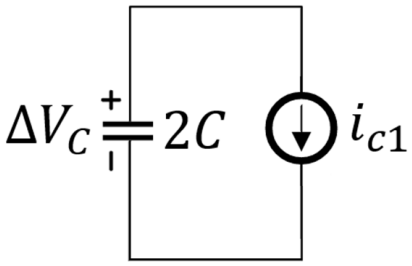

Figure 4. Third leg equivalent circuit.

The RMS value of the ripple is given through Equation (11):

$$\Delta V_C = I_C \cdot Z_C = \frac{S}{\sqrt{3} \cdot V_{ac}} \cdot \frac{1}{\omega \cdot 2 \cdot C} \tag{11}$$

where S is the power of the converter and ω is the grid frequency in radians per second. By assuming that the voltage ripple at 0 point is negligible, the minimum DC voltage required to operate in the linear range of the B4 inverter can be expressed as Equation (12), where V_{LCL} is the voltage drop across the LCL grid filter.

$$V_{dc,min} = \sqrt{3} \cdot \left[\sqrt{2} \cdot V_{ac} + V_{LCL}\right] \tag{12}$$

From Equation (11), and taking into account that the voltage ripple at the midpoint of the capacitors, the actual needed DC voltage is given through Equation (13):

$$V_{dc} \geq V_{dc,min} + \sqrt{2} \cdot \Delta V_C \tag{13}$$

Figure 5 shows the minimum needed capacity, C, as a function of the inverter power for three different values of voltage ripples at the midpoint of the capacitor bank. The grid voltage is $230V_{RMS}$ in all cases.

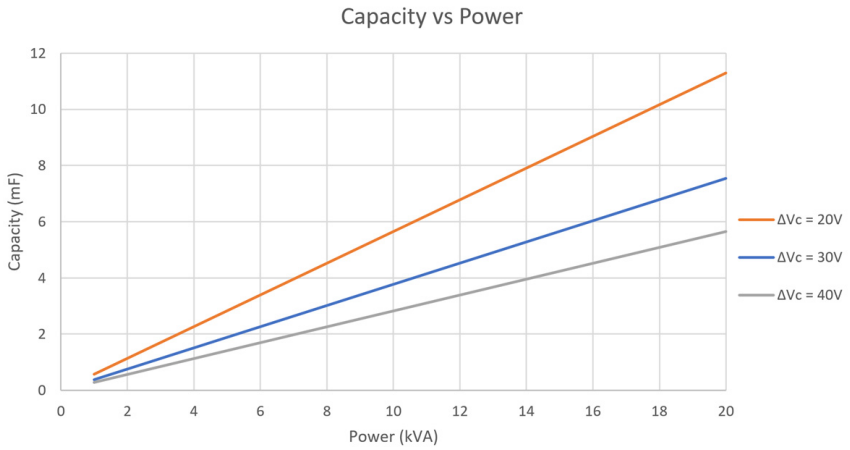

Figure 5. Relationship between capacity and inverter power for three different allowed voltage ripples at the midpoint of the capacitor bank.

3. Description of the Control Algorithms

3.1. B6 Inverter

One of the usual control strategies for B6 grid-connected inverters is to carry out the control in a rotating synchronous reference frame, also known as 'DQ control', allowing independent control of the direct (D) and quadrature (Q) components of the current, as shown in Figure 6.

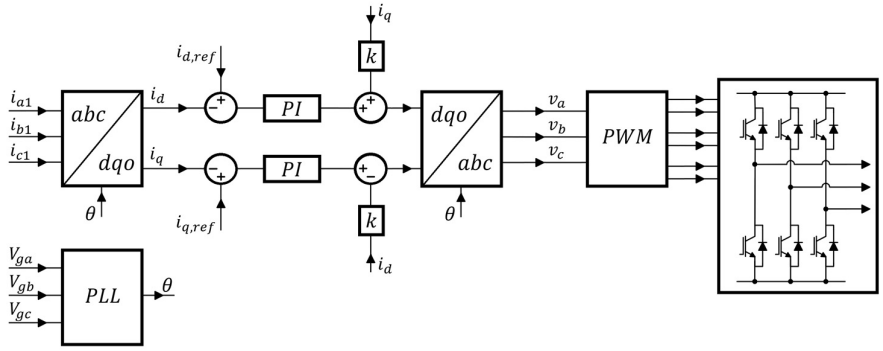

Figure 6. Current control loop of a classic B6 inverter.

When using this control technique, the current of the three lines is converted using the DQ0 transformation [17], represented in Figure 6 as the 'abc-to-dqo' block. The angular position, θ, is obtained from the grid. After that, the actual control is performed. In this case, there are two PI controllers as there are only two current control loops. Each control loop also has a decoupling block [19], as shown in Figure 6, where k is defined through Equation (14):

$$k = \frac{2 \cdot \pi \cdot f \cdot L}{V_{dc}} \tag{14}$$

where f is the grid frequency, L is the total inductance of the LCL output filter, and V_{dc} is the actual DC voltage of the converter. The signals are then returned to the abc frame using the inverse DQ0 transform. Finally, these are sent to the modulator to generate the six gate signals for the three-phase bridge.

3.2. B4 Inverter

As stated before, in the B4 topology only four gate signals are needed. Figure 7 shows the DQ control strategy applied to a B4 inverter.

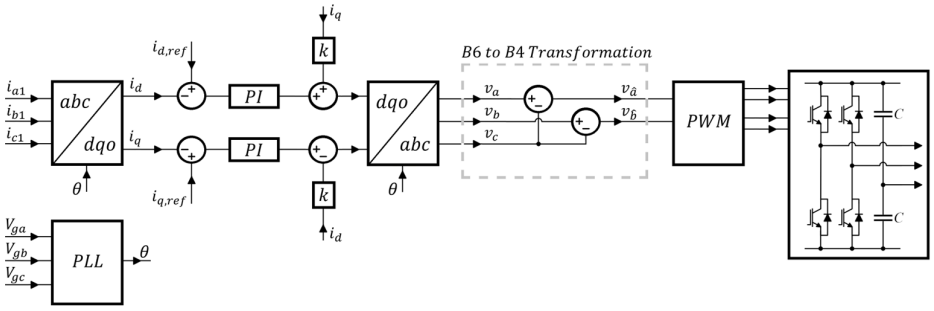

Figure 7. Current control loop of a B4 inverter.

After the two PI controllers are executed and the signals have been converted back to the abc frame, Equations (7) and (8) are applied, obtaining $v_{\hat{a}}$ and $v_{\hat{b}}$. These signals are sent to the PWM modulator, obtaining the four gate signals. As shown in Figures 6 and 7, the control is carried out in a rotating frame which is in sync with the grid. Therefore, grid synchronisation is mandatory.

There are several techniques for synchronising with a three-phase grid. The three most important ones are probably the Synchronous Reference Frame PLL (SRF-PLL), the Decoupled Double Synchronous Reference Frame PLL (DDSRF-PLL), and the Double Second-Order Generalised Integrator FLL (DSOGI-FLL) [20].

The SRF-PLL operates by converting the grid voltages, V_{ga}, V_{gb}, and V_{gc}, into the dq frame using the DQ0 transformation, obtaining the direct (V_d) and in-quadrature (V_q) signals. Subsequently, a low-pass filter is applied to V_q to remove high-frequency noise. The filtered V_q signal is then sent to a PI controller, the output of which is fed into an integrator simulating a voltage-controlled oscillator. This oscillator determines the angular position of the dq reference frame. The resulting angular position is fed back to the DQ0 transformation block, forming a feedback loop which regulates the V_q component to zero and keeps track of the grid frequency and phase.

The DDSRF-PLL represents an enhanced version of the SRF-PLL. Its notable feature lies in the utilisation of two synchronous reference frames, one rotating positively and the other negatively. This configuration enables the isolation of the negative sequence voltage effects on the V_d and V_q values derived from the positively rotating system, and vice versa. Following this decoupling process, the V_q signal from the positively rotating system is directed to a phase-locked loop (PLL) to obtain the grid frequency and phase.

The DSOGI-FLL is an alternative method that estimates the grid frequency rather than the grid phase angle. It operates by transforming the grid voltages into the αβ reference frame. Subsequently, two SOGIs generate the direct and in-quadrature signals, which are then processed by the positive-negative sequence calculation block. The resulting signals are utilised by the frequency-locked loop (FLL) to determine the grid frequency and phase.

As this paper does not aim to compare synchronisation techniques, the SRF-PLL has been selected for grid synchronisation. Figure 8 shows the diagram of the phase-locked loop used for grid synchronisation.

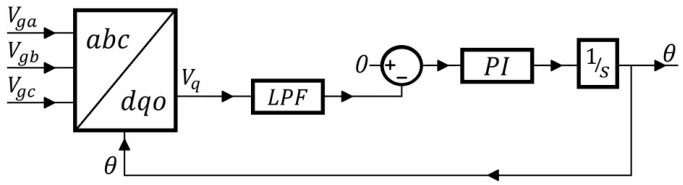

Figure 8. Phase-locked loop.

All these control loops are programmed in a DSP, as shown in Figure 9. The main routine is executed at twice the switching frequency in order minimise the time delay and increase the phase margin.

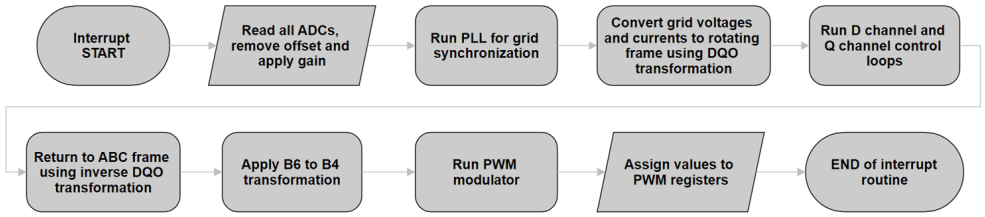

Figure 9. Inverter control routine.

Figure 10 provides an overview of the 2-leg, current source inverter, with its closed-loop control.

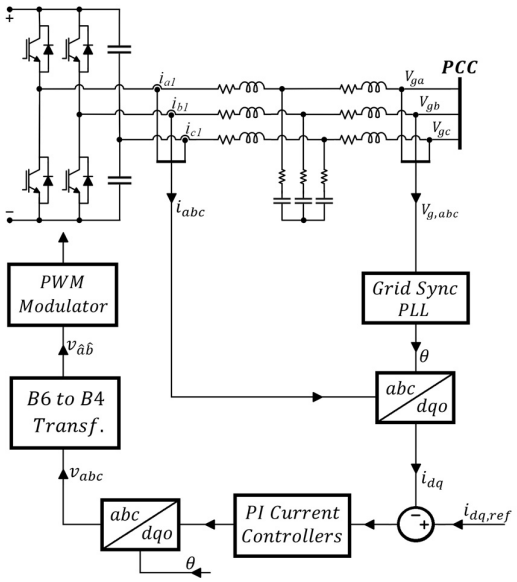

Figure 10. Closed control loop of the 2-leg inverter.

4. Experimental Setup

The experimental B4 inverter used to validate the simulation results is shown in Figure 11. It has been designed and built in the Grupo de Sistemas Electrónicos Industriales of the Universitat Politècnica de València. The inverter has a nominal power P_n = 10 kW and a switching frequency f_{sw} = 10 kHz with a 500 ns dead time. The DC-Link is formed by 10 electrolytic capacitors, five branches of two capacitors in series, with their midpoints interconnected (C = 2.35 mF). The control has been implemented on a Texas Instruments DSP F28379D and runs at 20 kHz.

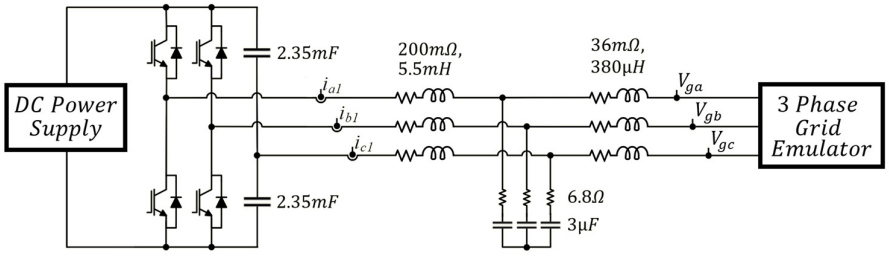

Figure 11. Experimental B4 inverter setup.

The inverter is connected to the experimental microgrid that the GSEI has [21] via an LCL grid filter. The grid inductance, which is estimated as ~300 μH/km [22], has been omitted as it is several orders of magnitude smaller than the output inductance of the

LCL filter due to the short length of the microgrid. Figure 11 also shows the values of the implemented LCL filter.

Although the converter is rated for 10 kW in a B6 configuration, a nominal power of only 7 kW has been achieved in tests. This is because the maximum power that can be transferred in the B4 topology is limited by the maximum current ripple supported by the DC-Link capacitors. Figure 12 shows the laboratory setup.

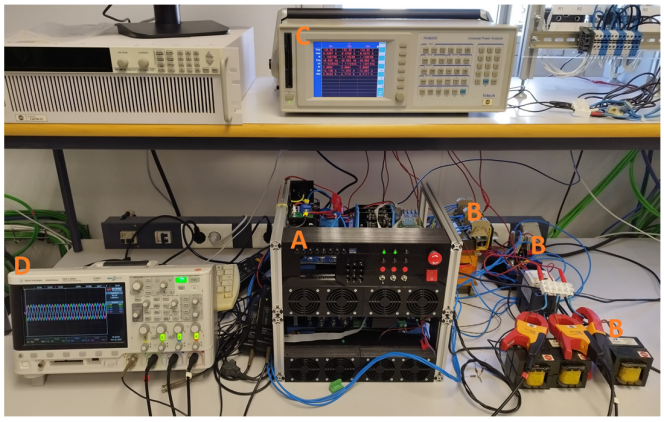

Figure 12. Experimental setup: (A) inverter; (B) LCL filter; (C) power analyser; and (D) oscilloscope.

A power analyser was used to measure the input and output power, current and voltage distortion, and current and voltage unbalance. The current and voltage unbalance (CU and VU, respectively) have been defined as the maximum deviation of any phase current/voltage (I_n, V_n) from the average value of the three phases (AV_I, AV_V), divided by the average value (i.e., $CU = \frac{\max|I_n - AV_I|}{AV_I}\%$ and $VU = \frac{\max|V_n - AV_V|}{AV_V}\%$) [23]. An oscilloscope has also been used to measure the output currents and the voltage at the midpoint of the capacitor bank in the B4 topology. Table 1 shows the laboratory equipment used in the experimental tests.

Table 1. Laboratory equipment.

Description	Model
AC Grid Emulator	Cinergia GE&EL-50
DC Voltage Source	AMREL HPS-800
Power Analyser	Voltech PM6000
Oscilloscope	Agilent DSO-X 2004
Differential voltage probes	Tektronix P5200
Current probes	Fluke i400s

The power analyser features four wattmeter-type channels, each for voltage and current measurement. Three channels are used for the AC output, while one is utilised for the DC input. The oscilloscope measures the output currents after the LCL filter using three current clamps, while the voltage at the midpoint of the capacitor bank is measured via an isolated differential voltage probe.

To verify that the conclusions obtained from the simulations in [24] are correct, two tests have been carried out with the same inverter. In the first one, the inverter has been configured as a B6 topology, while in the second one it has been changed to a B4 topology. This is achieved through disabling its third leg and obtaining the third phase from the midpoint of the capacitor bank which forms the DC-Link. Table 2 shows the parameters of the converter under study.

Table 2. Parameters of the converter.

Parameter	Nominal Value	Parameter	Nominal Value
V_{dc}	700 V	r_a	200 mΩ
V_{ac}	230 V_{rms}	r_b	36 mΩ
f_{ac}	50 Hz	r_d	6.8 Ω
C	2.35 mF	L_a	5.5 mH
f_{sw}	10 kHz	L_b	380 µH
P_n	7 kW	C_f	3 µF

5. Experimental Results

5.1. B4 Waveforms

Figure 13 shows the output current of the inverter. In all the following figures, the green trace represents line A current, the blue trace represents line B current, and the pink trace represents line C current (the one obtained from the midpoint of the capacitor bank).

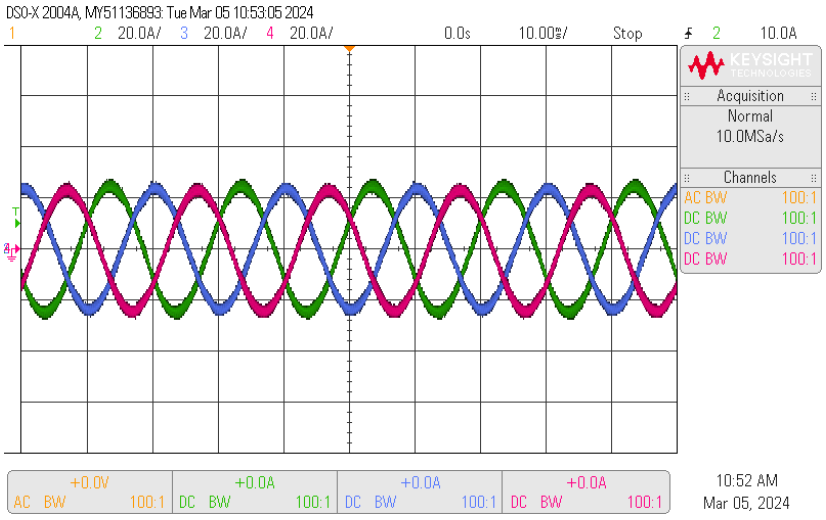

Figure 13. B4: Grid current at 7 kW.

The currents have a sinusoidal waveform and there is a 1.1% current unbalance among phases due to the voltage ripple at the mid-point of the capacitor bank.

Figure 14 shows this ripple during a transient from 50% to 100% of the rated power, while Figure 15 shows the output current.

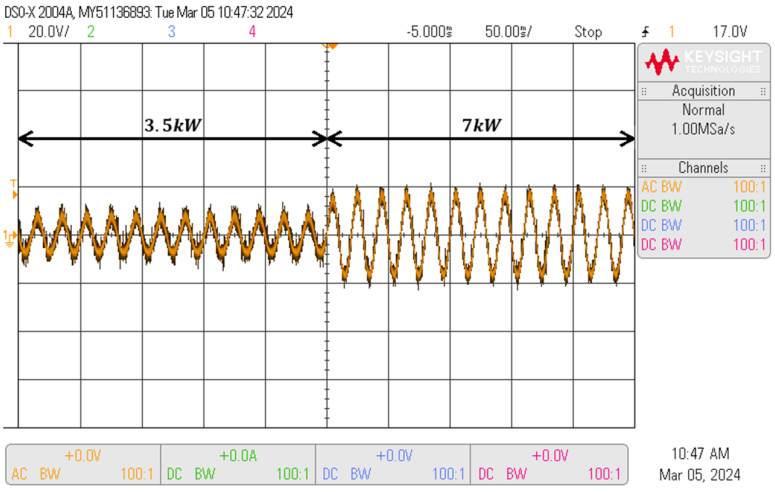

Figure 14. Voltage ripple at the midpoint of capacitors, with a load step from 3.5 to 7 kW.

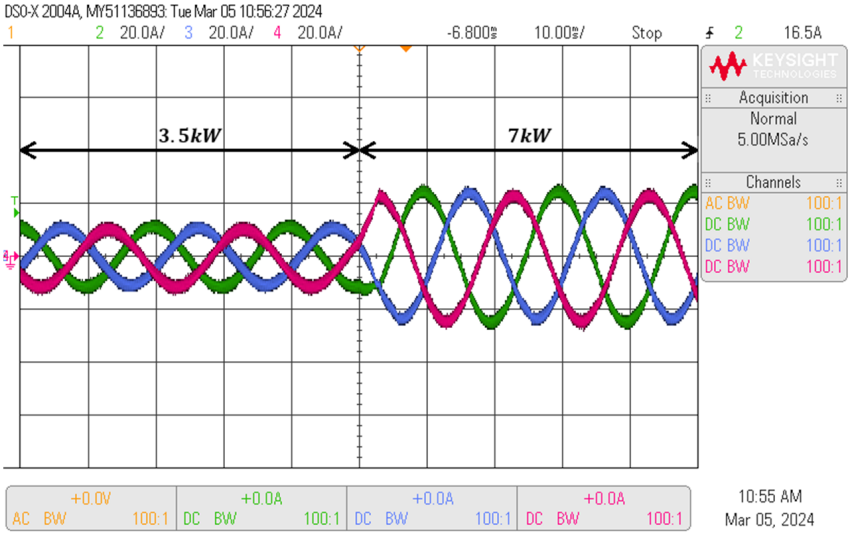

Figure 15. Grid current during a load step from 3.5 to 7 kW.

As expected, there is an increase in the voltage ripple at the midpoint of the DC-Link. At 7 kW the ripple increases to a maximum of 37.9 V_{pp}.

As it may be seen in Figure 15, the output current remains sinusoidal independently of the output power and the voltage ripple. The total harmonic distortion increases to 1.8% at 7 kW. Figure 16 displays the measured voltage ripple at the midpoint of the capacitor bank, alongside the corresponding theoretical values across various power levels.

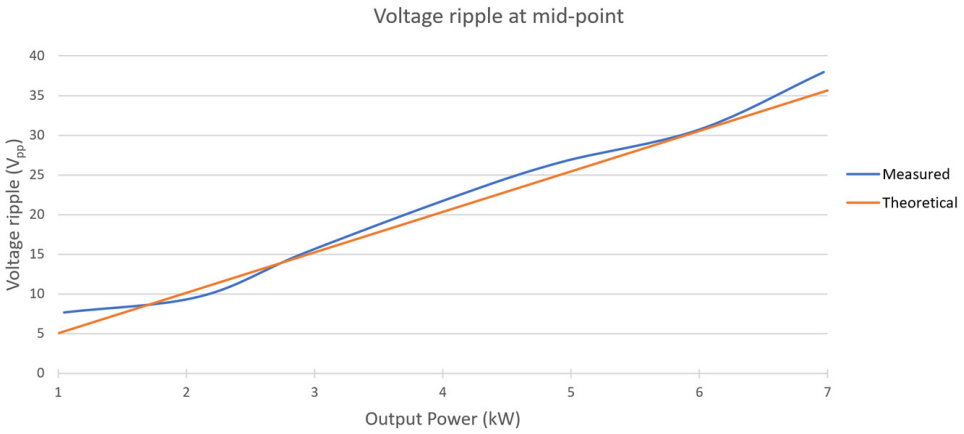

Figure 16. Measured and theoretical voltage ripple.

Both traces exhibit almost identical positive slopes, with a maximum deviation of 2.6 V, which corresponds to a 0.75% error relative to the nominal voltage.

The Cinergia GE&EL-50 programmable grid emulator can be configured to produce distortions and unbalances in the grid voltage. In this case, it has been configured to emulate a balanced and non-distorted three-phase grid, as Figure 17 shows. Despite this, small values of distortion and unbalance have been measured at the grid voltages, as Figure 18 shows.

Figure 18 shows the measured total harmonic distortion (THD_V) and the voltage unbalance on the emulated grid, for different power levels.

The THD_V does not exceed 0.5% while the unbalance does not reach 0.8%, for the entire power range.

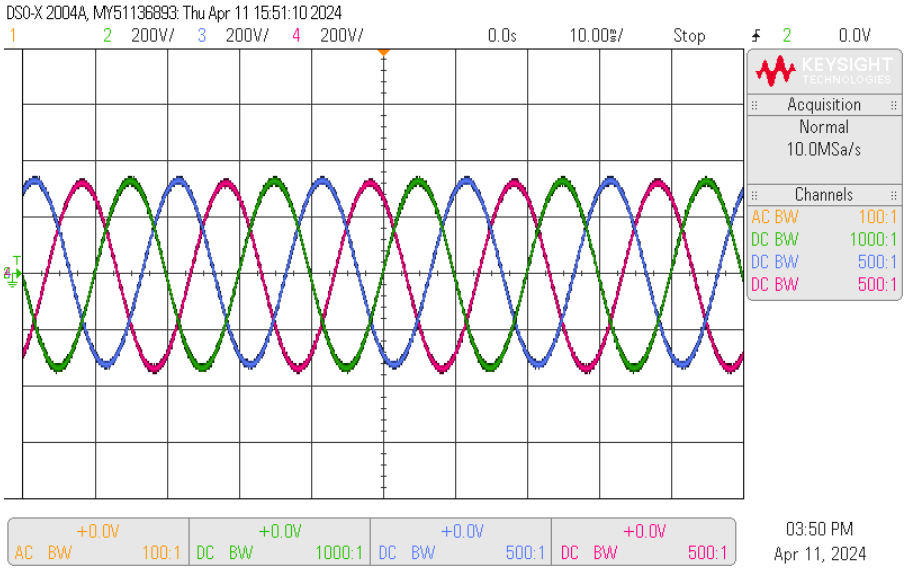

Figure 17. Measured grid voltages at 7 kW.

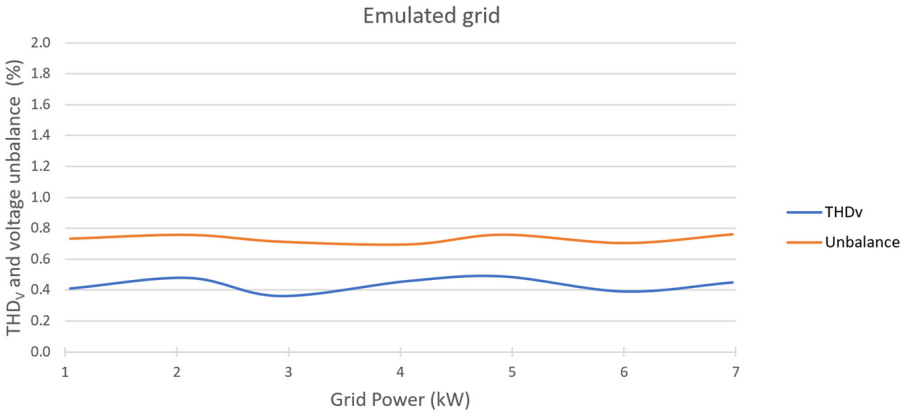

Figure 18. Measured THD_V and unbalance of the phase voltages.

5.2. Comparative Analysis of the Experimental Results

This section offers a comparative analysis of experimental findings between the two topologies, examining efficiency, total harmonic distortion, and current unbalance. The following figures present the test results, covering the power range from 1 to 7 kW.

The best efficiency (95.7%) is achieved by the B4 topology. There is a 3.3% efficiency difference between both topologies at high load and a 4.5% difference at low load. At 3 kW, where the efficiency curves are closest, B4 outperforms B6 by 2.5%. The B4 topology exhibits better efficiency over the whole power range. This is motivated by the lower conduction and switching losses in the B4 topology, as it employs two fewer transistors compared to B6. Figure 19 shows the efficiency measured for both tests.

The efficiency achieved by the tested B6 topology is relatively low compared to commercial three-phase inverters [9]. Regarding this issue, it's worth to point out that the goal of this paper is to compare, in equivalent conditions, the performance of both B4 and B6 topologies to implement grid-connected inverters. Since the main source of losses in the power stage are the conduction and switching losses of transistors, the efficiency of both topologies could be improved by reducing the switching frequency or by choosing other devices to implement the power stage.

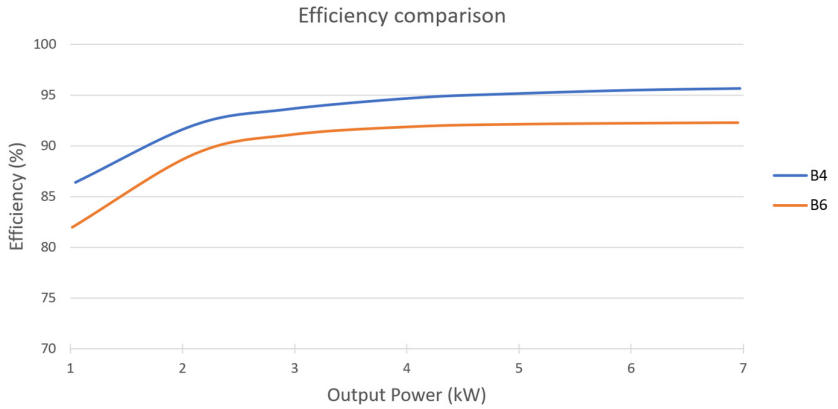

Figure 19. Measured efficiency.

Figure 20 shows the measured THD_I of the grid currents for both tests. Both topologies have a similar THD_I in the low-power range. In the high-power range, the B6 topology has a lower distortion than the B4 topology. Specifically, the THD_I at the corresponding rated power of each topology is 0.98% for B6 and 1.83% for B4.

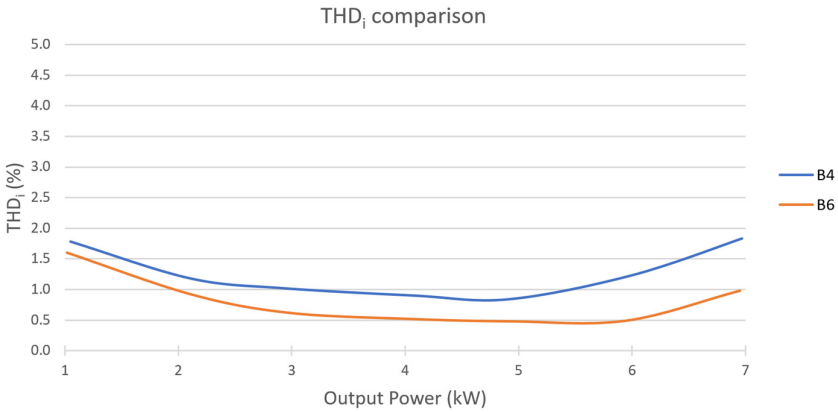

Figure 20. Measured THD_I of the line currents.

Figures 21 and 22 display the current harmonics from the 3rd to the 13th order for B4 and B6 topologies, respectively. The harmonics are represented as a percentage of the fundamental harmonic. As well as for the oscilloscope captures, the green trace corresponds to line A and the blue trace to line B. In B4 topology the pink trace, line C, is the one obtained from the midpoint of the DC-Link. In both cases, the inverter is operating at 7 kW.

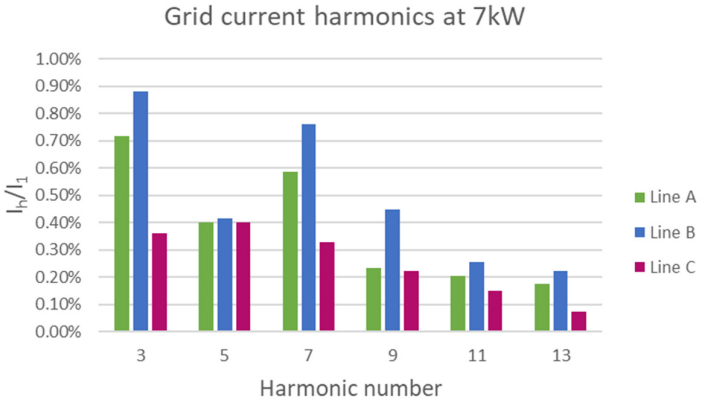

Figure 21. Grid current harmonics for B4 inverter at 7 kW.

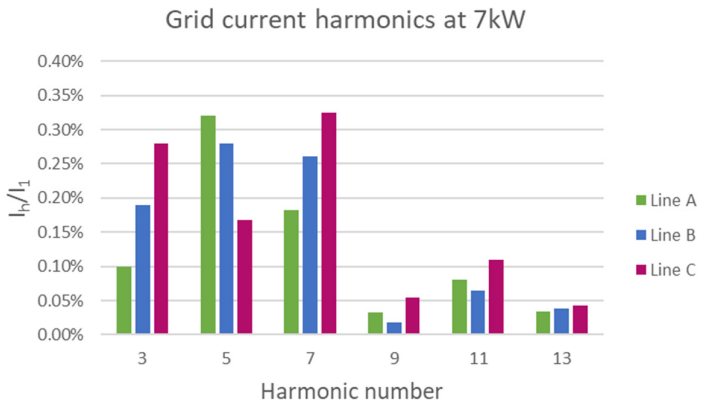

Figure 22. Grid current harmonics for B6 inverter at 7 kW.

As expected, the harmonics are greater in the B4 topology, being harmonics 3 to 7 the predominant in both cases, as Figures 21 and 22 show.

Figure 23 shows the measured unbalance of the grid currents for both topologies. While theoretically the unbalance should be zero in the case of the B6 topology, a 0.4% unbalance has been measured at full load.

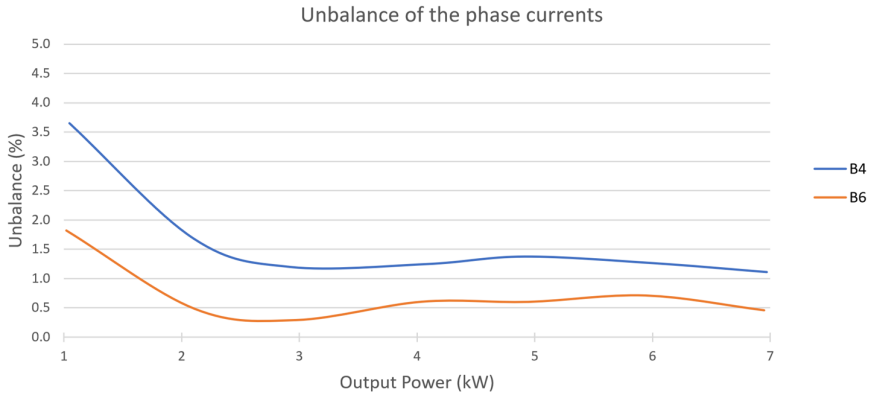

Figure 23. Measured unbalance of the grid currents.

The B4 converter achieves a higher performance, while the B6 topology presents a lower harmonic distortion of the output currents and a lower unbalance between them.

5.3. Cost Comparison of the B4 and the B6 Topology

Next, a comparison has been made regarding the economic cost of each topology. The difference between the B4 and B6 inverters lies mainly in the power stage. The sensing circuits, acquisition, control and output filters are the same in both inverters and therefore they have not been taken into account. Regarding capacitors and transistors, the price of each component and their quantity have been considered. For the gate drivers, it has been taken into account that they are mounted on a removable printed circuit board. Therefore, the cost of the gate driver, the printed circuit board, and the isolated DC-DC converter that powers up the gate driver IC have been included in the cost calculation. The capacitors are model B43544A6477M000, while the transistors are SK75GB12T4T. The selected gate driver is the HCPL-316J IC and the isolated DC-DC converter is XP-ISA0515. Table 3 summarises the resulting cost for each alternative.

The B4 topology is the cheapest one, although there is only a 1.48 EUR/kW difference between the two topologies. To determine the factors contributing to the increased costs of the B6 topology, Figure 24 illustrates the breakdown of expenses for each topology. Note that this metric is an approximation and does not account for factors such as shipping and handling costs, among others.

Table 3. Estimated cost of each topology.

Topology	Cost
B6	35.43 EUR/kW
B4	33.95 EUR/kW

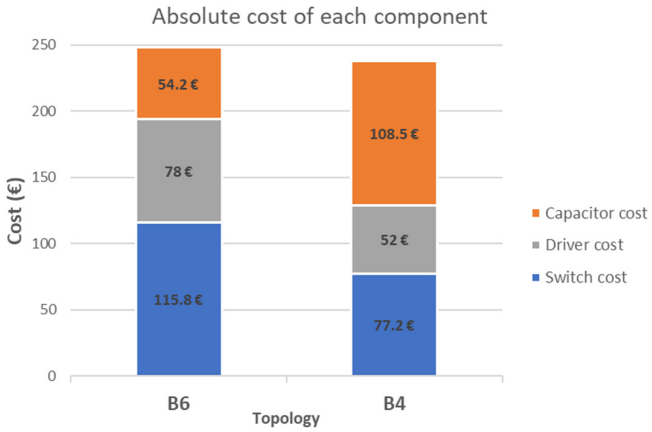

Figure 24. Absolute cost of each component for each topology.

According to this figure, the B4 topology is notably affected by the costs associated with constructing the DC link. This is due to the expenses related with the increase in the number of capacitors which result from the higher current circulating through them. In the B6 topology, the cost of capacitors is EUR 54.20 (21.9%), while in B4 it increases to EUR 108.50 (45.6%). However, in B6, the cost of drivers is EUR 78.00 (31.4%) and the cost of switches is EUR 115.80 (46.7%), while in B4 these decrease to EUR 52.00 (21.9%) and EUR 77.20 (32.5%), respectively.

5.4. Reliability Analysis of the B4 and the B6 Topology

To analyse the impact of varying component quantities on the lifetime of the inverters (e.g., B6 having more transistors but B4 having more capacitors), a reliability analysis has been conducted. The Mean Time Between Failures (MTFB) has been chosen as figure of merit. The MTBF is a measure of the reliability of a system or a component. It refers to the average time that elapses between one failure and the next and under normal operating conditions. In other words, MTBF is a statistical estimate of the expected time that a device or component will operate without experiencing a failure.

The following components have been taken into account for the analysis: IGBTs, DC-Link capacitors, gate drivers, main LC filter, grid contactor, current sensors, voltage sensors, auxiliary power supplies, and main control board. The MTBF data for the analysis has been obtained from the datasheets provided by the manufacturers, including those for the gate drivers [25] and auxiliary power supplies [26,27].

Where manufacturer-provided data was unavailable, an estimation of the MTBF has been conducted in accordance with MIL-HDBK-217F [28]. This handbook contains failure rate models for different electronic components, such as transistors, capacitors, and resistors [29]. The guide offers an estimate of the failures in time (FIT) for each component, derived from empirical data. The FIT is a dimensionless unit of measurement also used to express the failure rate of a component. It represents the number of failures expected to occur, usually in 10^9 h of operation. Calculating the FIT requires several initial data points, including the device's operating environment (ground, naval, airborne or space), ambient temperature, voltage stress compared to nominal voltage, among other factors. A ground-fixed environment and a 60 °C ambient temperature have been assumed for the FIT calculation. However, this guide lacks a specific failure rate calculation methodology for IGBTs. Given that an IGBT consists of both a BJT and a MOSFET, the MTBF has been determined by combining the MTBF values of both components [30,31].

As an example, Equation (15) is the one used to calculate the number of failures per 10^6 h of operation for an aluminium electrolytic capacitor.

$$\lambda_p = \lambda_b \pi_{CV} \pi_Q \pi_E \tag{15}$$

There are several equations that determine the value of λ_b, depending on the maximum operating temperature of the capacitor. In this case, as the capacitor is rated for 105 °C, it is given by Equation (16):

$$\lambda_b = 0.00254 \left[\left(\frac{S}{0.5} \right)^3 + 1 \right] exp \left(5.09 \left(\frac{T+273}{378} \right)^5 \right) \tag{16}$$

T is the ambient temperature in Celsius degrees and S is the ratio between the operating voltage and the maximum voltage of the capacitor. Equation (16) yields to $\lambda_b = 0.14$.

The value of π_{CV} depends on the capacity and is given by Equation (17):

$$\pi_{CV} = 0.34 C^{0.18} \tag{17}$$

where C is the capacity in μF. In this case, Equation (17) results in $\pi_{CV} = 1.029$.

The value of π_Q depends on the quality grade of the capacitor. In this case, quality M [28], results in $\pi_Q = 1$.

The value of π_E depends on the environment in which the component will be installed. In this case, ground-fixed [28], results in $\pi_E = 2$.

Finally, the failure rate for every 10^6 h of operation is obtained:

$$\lambda_p = 0.14 \cdot 1.029 \cdot 1 \cdot 2 = 0.28812 \tag{18}$$

The equivalent *FIT*, per 10^9 h of operation is:

$$FIT \approx 288 \tag{19}$$

After obtaining the *FIT* of each component, it has been multiplied by the quantity of that component, and the results have been summed to obtain the overall *FIT*.

Equation (20) has been used to obtain the *MTBF*.

$$MTBF = \frac{10^9}{FIT} \tag{20}$$

Table 4 shows the results of the reliability analysis, both in hours and failures in time [32].

Table 4. Results of the reliability analysis.

Topology	FIT (per 10^9 h)	MTBF (Hours)
B6	7385	135,410
B4	7115	140,557

The B4 topology shows a better MTFB, with a total of 140,557 h while the B6 topology achieves 135,410 h. To determine the reason why the B6 topology presents a lower MTBF, Figure 25 disaggregates the FIT for both topologies.

The reason why the B6 topology has a higher number of failures in time, despite having fewer capacitors, is due to the increase in transistors and driving circuits. While it is true that the FIT of capacitors in B4 is 2240 (31%) and only 1120 in B6 (15%), the FIT of IGBTs in B4 is 1145 (16%) while in B6 it increases to 1717 (23%). Furthermore, the FIT of the gate drivers in B4 is only 1636 (23%), while in B6 it reaches 2454 (33%).

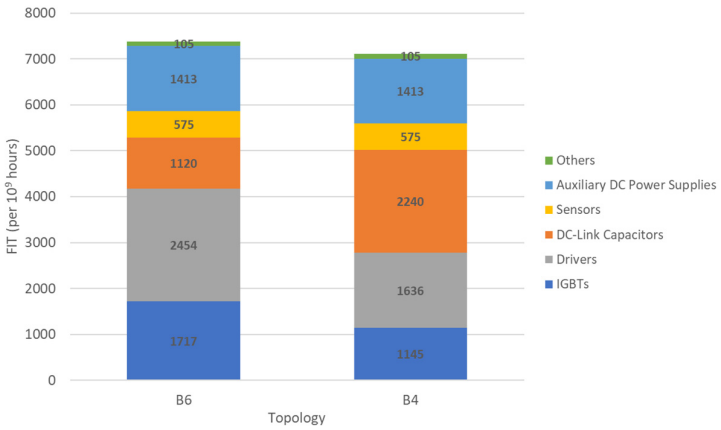

Figure 25. Contribution of each component to the FIT.

To include the long-term implications in the comparative study, a new indicator called Equivalent Cost per Year (ECY) has been defined. It takes into account both the cost of the converter and the time before the first failure, as Equation (21) shows:

$$ECY = \frac{Cost}{MTBF} \tag{21}$$

This indicator may be useful for comparing the cost-effectiveness of various alternatives with different lifespans. The results obtained with this new metric are shown in Table 5.

Table 5. Equivalent cost per year for both topologies.

Topology	ECY (EUR per 10,000 h)
B6	18.3
B4	16.9

The B4 topology shows a better ECY, with a total of 16.9 EUR/10,000 h, while the B6 topology stands at 18.3 EUR/10,000 h (8% higher). The reason for this improvement is that the B4 topology has a lower cost and a higher MTBF.

6. Conclusions

This paper presents a suitability evaluation of the B4 inverter operating in grid-connected mode. Tests have been carried out which show how the B4 topology demonstrates superior efficiency compared to the B6 topology across the entire power range. The maximum increase in efficiency is observed at low loads, where the difference amounts to approximately 4.5%. At high load the B4 topology outperforms the B6 one by 3.3%. At 3 kW load, where the efficiency curves are closest, B4 achieves a 2.5% higher efficiency than B6.

Furthermore, although harmonic distortion is similar in both, B6 has a lower THD. The difference is more significant at high loads, where in B4 it reaches a 1.83% while in B6 it remains at 0.98%. Current harmonics 3 to 7 are the predominant in both topologies. Similar trends are observed with the current unbalance, with B6 exhibiting a slightly lower level. At high loads, the current unbalance in B6 reaches 0.4%, whereas in B4 it stabilises at 1.1%.

The B4 topology stands out as the more cost-effective option, mainly due to the reduced number of transistors and gate drivers it requires. Despite the higher number of capacitors in B4, its cost stands at 33.95 EUR/kW, with capacitors accounting for 45.6% of the total. In contrast, the B6 topology, with a cost of 35.43 EUR/kW, has capacitors representing a smaller proportion, at 21.9%. In B6 the cost of gate drivers is 31.4% and the cost of switches is 46.7%, while in B4 these decrease to 21.9% and 32.5%, respectively.

Lastly, the B4 topology exhibits superior MTFB of 140,557 h compared to the B6 topology of 135,410 h. Despite fewer capacitors, B6 experiences more failures due to an increased number of transistors and driver circuits. Capacitor FIT rates are 31% in B4 and 15% in B6. In respect to the total FIT, the combined IGBT and gate driver FIT rates are 39% in B4 and increase to 56% in B6.

As the B4 topology has a lower cost and a higher MTBF, it presents a better ECY of 16.9 EUR/10,000 h. Topology B6 has an 8% higher ECY at 18.3 EUR/10,000 h.

The B4 inverter has proven to be a good candidate for use as a grid-tied inverter, achieving a higher efficiency, a slightly reduced cost, and a greater MTFB relative to a B6 inverter, while maintaining low THD_I and current unbalance.

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Conflicts of Interest: The authors declare no conflicts of interest.

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