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# Readout electronics for the SiPM tracking plane in the NEXT-1 prototype

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NEXT is a new experiment to search for neutrinoless double beta decay using a 100 kg radio-pure high-pressure gaseous xenon TPC with electroluminescence readout. A large-scale prototype with a SiPM tracking plane has been built. The primary electron paths can be reconstructed from time-resolved measurements of the light that arrives to the SiPM plane. Our approach is to measure how many photons have reached each SiPM sensor each microsecond with a gated integrator. We have designed and tested a 16-channel front-end board that includes the analog paths and a digital section. Each analog path consists of three different stages: a transimpedance amplifier, a gated integrator and an offset and gain control stage. Measurements show good linearity and the ability to detect single photoelectrons.

## 1. Introduction

### 1.1. The NEXT experiment

NEXT (Neutrino Experiment with a Xenon TPC) is a new experiment designed to search for neutrino-less double beta decay using a 100 kg radio-pure, 90% enriched ($^{136}$Xe isotope) high-pressure gaseous xenon TPC with electroluminescence readout. The experiment will be located in the Canfranc Underground Laboratory (LSC) in Spain [1-2].

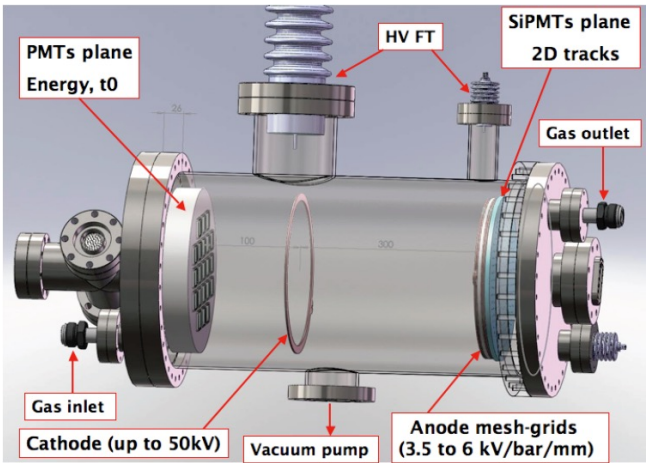



Fig. 1. The NEXT-1 EL TPC. The anode is equipped with a SiPM plane used for pattern recognition.

NEXT-1 EL is a large-scale prototype (Fig. 1) equipped with two sensor planes in opposite sides of the detector vessel. One plane will measure event energy with PMTs and will also detect the primary scintillation light [3-4]. The other plane will use a SiPM array to follow the primary electron paths and to help in the discrimination of interesting events from the background.

Primary electrons that result from background events and double-beta decays in the TPC active volume follow random paths due to multiple scattering (Fig. 2), ionizing the gas in their movement.

The secondary electrons produced by this ionization drift towards the anode following the electric field lines in the TPC. Electroluminiscence is then used at the anode to amplify these weak signals and produce photons that are registered by the SiPM plane array. About 1,000 photons are produced per drift electron.

The uniformity of the SiPM noise pulses and the large intensities of tracking signals allow setting a digital threshold at about five photoelectrons, high enough to eliminate almost all noise but without degrading the spatial resolution [1]. This value sets a relaxed design parameter for the front-end electronics. Nevertheless, with the aim to study the resolution limits in the NEXT-1 EL tracking plane, single-photoelectron resolution is taken as a design goal for the front-end electronics described in this paper.

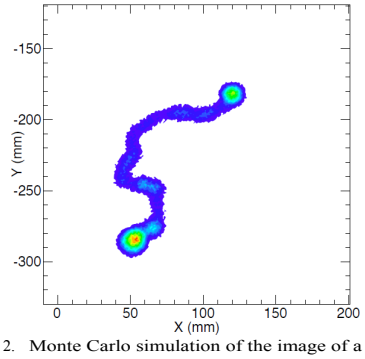



Fig. 2. Monte Carlo simulation of the image of a neutrino-less double beta decay in the SiPM plane

### 1.2. The SiPM tracking plane

The SiPM plane contains 248 sensor elements (Hamamatsu MPPC, 1mm$^2$ active area, SMD type model S10362-11-050C) mounted on 18 daughter boards (Fig. 3, top left). The daughter boards are in turn mounted on a 238-mm diameter mother board for mechanical support and electrical connections (Fig. 3, top right). Sensors on the same daughter board share a common bias voltage provided by a high-voltage DC supply module from ISEG (APS series). The gain dispersion in each daughter board is better than 4% while the average gain of each board is in (2,27−2,50)10$^5$. This ensures a uniform plane response.

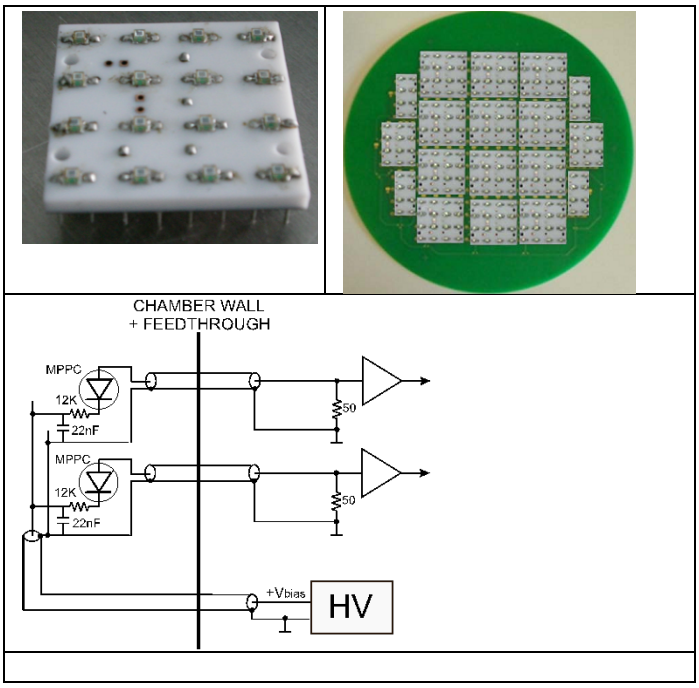



Fig 3. A 16-ch daughter board (top left), plane array mounted on top of the motherboard (top right), and SiPM bias scheme (bottom).

1.3. Cabling scheme and crosstalk

For 32 ADC counts per photoelectron in a 10-bit ADC (see Section 4, Fig. 7), our signal has a dynamic range of 30 dB. In order to keep the crosstalk level below one photoelectron, the total crosstalk should be ten times smaller. This gives a maximum admissible crosstalk of -50 dB.

From the mechanical point of view ribbon cables are easier to handle and connect than coaxial cables. As the crosstalk is additive, the induced crosstalk in a ribbon cable tends to be large due to the contribution of the neighbouring wires. Several configurations of ribbon cables and signal mapping have been tested: twisted and untwisted wires, single ended and differential, common ground and individual grounds. Single-ended, untwisted, common ground configuration showed the worst performance; with approx. -20 dB crosstalk. The best results were measured on a twisted-pair, differential transmission configuration. Yet even in this case the measured crosstalk was larger than the required -50dB. As a result it was decided to use coaxial cables to minimise this problem, following the connection scheme shown in Fig. 3 (bottom).

2. The analog front-end

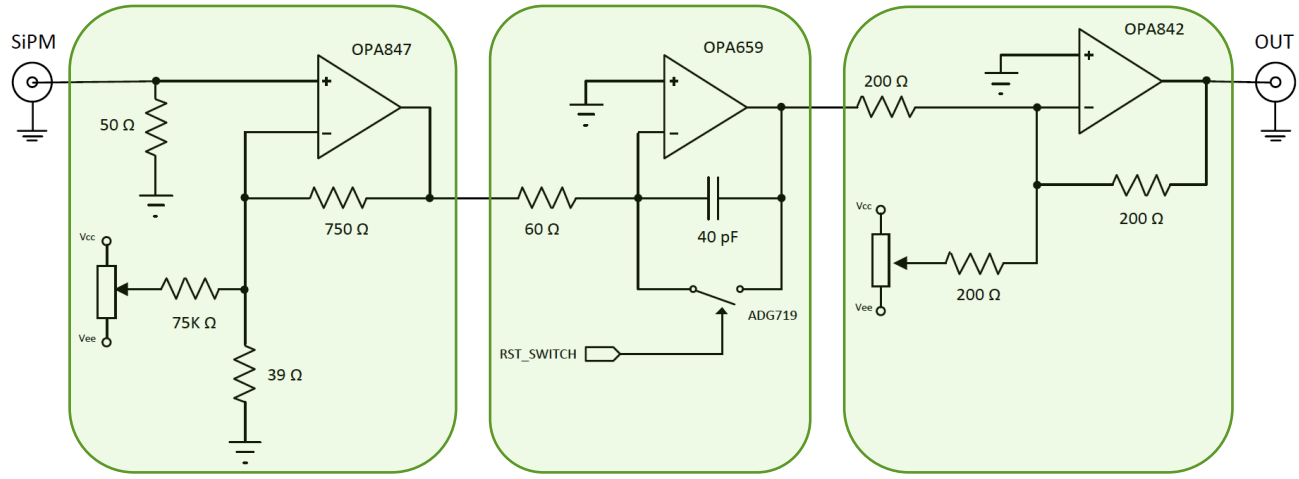
The primary electron paths can be reconstructed from time-resolved measurements of the light that arrives to the SiPM sensor plane (Fig. 2). Our approach is to estimate how many photons have reached each SiPM sensor per time bucket by integrating the SiPM output current in a gated integrator. Sensors are spaced 1 cm (this defines the x-y resolution) and the time bucket is 1 us (for 1 mm resolution in z as the drift velocity is 1 mm/us).

Although an integrating front-end is more vulnerable to thermal and induced noise [5], it also provides higher signal levels necessary to read very low light events. Most of the induced noise is due to capacitive/inductive coupling from switching digital lines in the PCB and charge sharing effects in the integrator. As a consequence, most of the integrated induced noise turns out to be deterministic which allows an easy calibration procedure. Signals obtained at the front-end output are converted to digital domain using a 10-bit 1-MHz ADC.

The analog path consists of three different stages (Fig 4). The first stage is a transimpedance preamplifier with constant input impedance for line adaptation. Final bandwidth (45 MHz) is limited by terminal impedance (50 Ohm) and SiPM parasitic capacitance (70 pF). However OPA847 extended GBP (Gain-Bandwidth Product) provides a preamplifier intrinsic bandwidth over 100 MHz, which guarantees an efficient line adaptation over the final bandwidth. An offset control optimizes the integrator dynamic range. First stage gain including line impedance adaptation is 1000 Ohm.

The second stage is a gated integrator with a variable integration time. The nominal value of this integration interval (1 us) is related to the desired spatial resolution of the whole detector and the minimum will be limited by the maximum data rate of the uplink. Since we are using a positive bias voltage (Fig. 3 bottom), first stage output is also positive, which in turn produces a negative voltage at the integrator output. In order to discharge the integrating capacitor, ADG719 has been chosen since it is the fastest integrated switch available in a discrete implementation. It provides a discharge time of 10 ns which is only 1% of the nominal integration time.

The third stage is an inverter with G = -1, required to produce a



positive signal at the ADC input. An offset correction is included since the integrator introduces an output offset: the switch control signal introduces a small quantity of charge into the feedback capacitor, producing a constant offset after every reset.

The gains in every stage have been defined to obtain output precision which could resolve up to a single photo-electron (pe). The output voltage step obtained from a single photoelectron should be higher than the equivalent output noise so that the system may have the desired resolution. Although preamplifier noise response is extremely good (OPA847 datasheet shows 0.85nV/√Hz) it takes the largest part of the equivalent output noise budget (7 mVrms). The rest of the front-end shows lower noise levels. Finally the total equivalent output noise theoretically calculated and checked through simulation is below 13 mVrms. In order to provide a sufficient dynamic range and stay above the noise floor, gain values have been adjusted to obtain about 18 mV/pe.

## 3. The SiPM front-end board

We have designed and tested a 16-channel board that includes 16 analog paths and a digital section (Fig. 5). The analog path circuit is described in the previous section.

### 3.1. On-board data processing

The digital section is based on a small, low-power Xilinx Spartan-3 FPGA that reads sixteen 10-bit ADCs (AD7277), controls the switches in the gated integrators, builds a frame with the digitized data and communicates with the upstream readout stage using LVDS signals over standard RJ-45 connector and CAT6 cable. Careful PCB layout techniques ensure that the digital parts introduce very little noise in the analog section.

The FPGA has enough logic resources to implement some basic data processing, like zero suppression or a buffer to operate in triggered mode. Nevertheless, the readout is operated in raw continuous acquisition. A data packet containing the sixteen digitized values is sent to the DAQ each microsecond.

### 3.2. Interface to the DAQ

The upper stage in the readout chain is the Front-End Concentrator (FEC) card [6], designed as a joint collaboration between CERN and NEXT in the framework of the RD51 Collaboration readout system [7-8]. Up to 16 front-end cards can be connected the FEC, allowing for up to 256 SiPM channels, enough for NEXT-1. This readout system can be scaled up by simple addition of FEC cards. Data are sent to the DAQ PC via gigabit Ethernet links.

The SiPM front-end board and the FEC card are connected by means of a high-speed full duplex link consisting of two LVDS pairs in each direction over a standard CAT-6 network cable. The FEC card sends a master clock to the front-end board FPGA over one of the LVDS pairs, thus providing system-level synchronization among the different front-end boards. A second downstream pair is used to send trigger and configuration commands to the front-end board.

The front-end FPGA sends the acquired data from the sixteen SiPM channels through the remaining two LVDS pairs (eight SiPM channels per pair). The bit rate of each serial link is 200 Mbps. Each data frame is composed of a 16-bit start of frame (SOF) header, a 16-bit identifier word, eight 16-bit words for the raw data and a 16-bit end of frame (EOF) trailer. The system sends a new frame each microsecond, resulting in an aggregated upstream data throughput of 352 Mb/s. A data recovery algorithm is used in the destination (FEC card) in order to avoid clock forwarding from the front-end [9].

The described link was validated in a test setup composed of one front-end board, one FEC card and a 15-meter CAT-6 network cable. No error in the link occurred during three consecutive days at the nominal 352 Mb/s load with PRBS data [10]. The estimated BER is then lower than 1e-13 with a 99.99% confidence level. This result confirms the goodness of the link implementation.

Fig. 4. The amplifier and integrating circuit

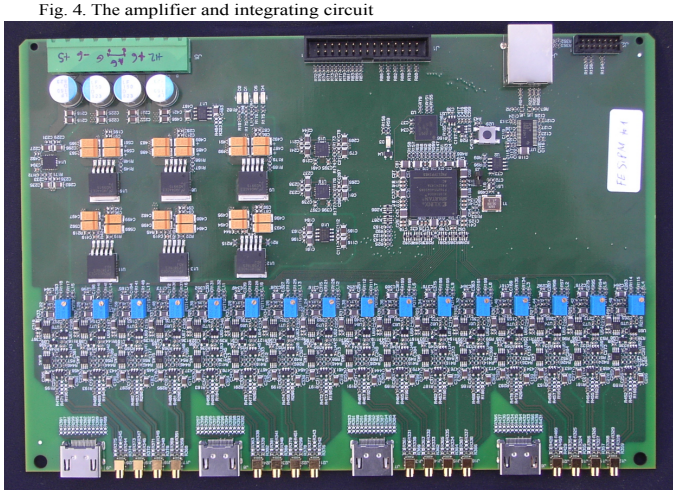


Fig. 5. The FE-SiPM card. The digital section (top right) includes the FPGA and the RJ-45 socket. Voltage regulators are located at the top left corner. The bottom half of the board contains the 16 analog paths and the input connectors. Input signal options are miniature coax (single ended) or HDMI (differential).

## 4. Measurements

Our test setup consists of one daughter board, which comprises 16 channels (16 SiPMs), mounted on top of the motherboard. The 16 SiPM devices have been selected to have a uniform response, and are biased from a single voltage (71,14 V). The sensors were introduced inside a black box in order to reduce external noise.

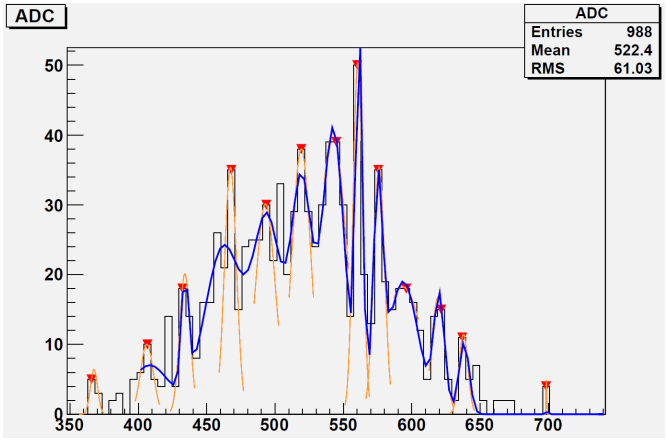



Fig.6 Gaussian fit to the number of ADC counts produced by different photoelectrons

A 400-nm LED was used to illuminate the daughter board at low intensity inside the black box. A suitable pulse generator was required to synchronize the emission of light with the trigger signal for the readout electronics. In each acquisition (384 us), 10 pulses of light of 1 us each were produced.

Light pulses produce a variable number of detected photoelectrons, which are processed by the electronic chain, giving

a response in ADC counts. Fig. 6 shows the typical response in ADC counts for a single channel. The different gaussian fits shown identify the different numbers of photoelectrons produced in the device with each pulse.

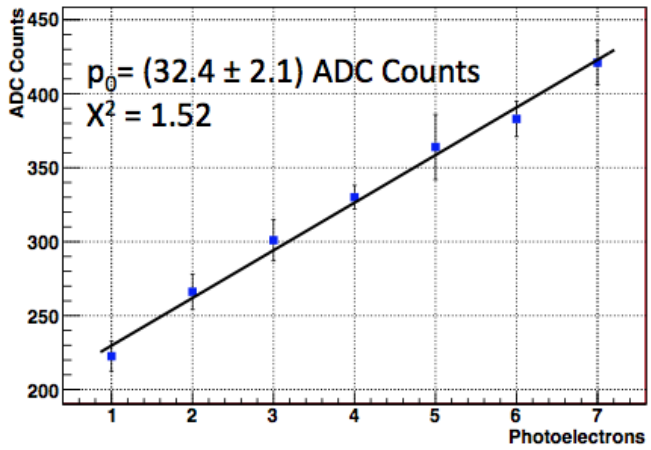



Fig.7 Linearity in the ADC dynamic range (1024 counts)

From this analysis we can easily obtain the linearity of our system. In fact, as can be seen from Fig 7, the behaviour of the system with the number of photoelectrons produced in the device is linear in the dynamic range (1024 counts), where the fit slope gives the conversion factor between ADC counts and photoelectrons.

## 5. Conclusions

In this paper we have described the readout electronics for the SiPM plane in the NEXT-1 prototype. The readout is based on a gated integrator circuit that produces an output proportional to the number of photons that impinge on the SiPM sensor each microsecond. Data are then digitized and transmitted to the DAQ using RD51 electronics, developed jointly by the NEXT Collaboration and CERN for the RD51 Collaboration.

Performance tests show single photoelectron detection, good linearity and superb data transmission quality to the DAQ PC, resulting in a valid solution for NEXT-1 purposes.

Nevertheless, there are still a couple issues that still need to be addressed in a coming design revision:

(1) Channel-by-channel offset voltage adjustment by hand turned out to be critical to obtain the reported performance. So, the offset voltage drift with temperature and aging needs to be studied.

(2) Power dissipation in the operational amplifiers is high and requires the use of forced air cooling and/or heathsinks. The use of alternative, low-power amplifiers must be evaluated.

Scalability to 248 channels is straightforward, requiring sixteen front-end boards, two FEC cards (serving only 8 front-end cards each for a reduced load in the gigabit Ethernet link), two DAQ PCs and one trigger card to fan out clock and commands.

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