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Additional Information

The front-end electronics for the 1.8-kchannel SiPM tracking plane in the NEW detector

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ABSTRACT: NEW is the first phase of NEXT-100 experiment, an experiment aimed at searching for neutrinoless double-beta decay. NEXT technology combines an excellent energy resolution with tracking capabilities thanks to a combination of optical sensors, PMTs for the energy measurement and SiPMs for topology reconstruction. Those two tools result in one of the highest background rejection potentials in the field. This work describes the tracking plane that will be constructed for the NEW detector which consists of close to 1800 sensors with a 1-cm pitch arranged in twenty-eight 64-SiPM boards. Then it focuses in the development of the electronics needed to read the 1800 channels with a front-end board that includes per-channel differential transimpedance input amplifier, gated integrator, automatic offset voltage compensation and 12-bit ADC. Finally, a description of how the FPGA buffers data, carries out zero suppression and sends data to the DAQ interface using CERN RD-51 SRS's DTCC link specification complements the description of the electronics of the NEW detector tracking plane.

KEYWORDS: Analogue electronic circuits; Data acquisition circuits; Front-end electronics for detector readout; Digital electronic circuits

1 The NEXT experiment

The NEXT experiment will use a high-pressure gas electroluminescent Time Projection Chamber (TPC) to search for neutrinoless double beta decay $bb0n$ using ^{136}Xe . Two sensor planes, one at each end cap, will allow to measure both the event energy and its path inside the gas. The energy is measured using PMTs while the electron path is reconstructed using the information recorded by a SiPM tracking plane. The combination of these two measurements gives the experiment the power to efficiently reject background while maintaining efficient reconstruction of the signal with good energy resolution.

The primary goal of the project is the construction, commissioning and operation of the NEXT-100 detector, filled with 100 kg of xenon enriched at 90% by the isotope ^{136}Xe . The experiment will operate at the Canfranc Underground Laboratory (LSC), starting in 2016. The NEXT collaboration includes institutions from Spain, Portugal, USA, Russia and Colombia. As a first step towards the construction and operation of NEXT-100, the NEW detector will be built and operated in 2015 to allow the validation of the technological solutions proposed for the NEXT experiment. NEW would permit, in a 10-kg scale ^{136}Xe detector, a measurement of the energy resolution at high energy, and the characterization of the two-electron topological signature, by measuring the $bb2n$ mode. Finally, NEW will permit a realistic assessment of the NEXT background model before the construction of the NEXT-100 detector, checking that the chosen materials satisfy the radiopurity requirements, specially in the energy region around Q_{bb} (2458 keV), mainly from ^{214}Bi and ^{208}Tl .

1.1 NEXT-DEMO detector

One of the first prototypes operated by the NEXT Collaboration is NEXT-DEMO. The NEXTDEMO detector is a 1:3 scale of NEXT-100 that has been running at IFIC for the last 3 years. It allowed for a full demonstration of the capabilities of the SOFT concept [1] and NEXT technology [2]. The tracking plane of the DEMO detector was instrumented with SiPMs at a sensor pitch of 1 cm. The plane consists of 256 Hamamatsu S10362-11-050P SiPMs distributed between 4 boards, each with 64 sensors coated with tetraphenyl butadiene (TPB) to improve the light detection efficiency. The detection process is as follows: First the gamma coming from an external source interacts with an electron in the Xenon media. This primary electron moves in the gas losing its energy through ionization and excitation of Xenon atoms. The moderate electric field in the active volume of the field cage prevents the recombination of those ionized electrons (secondary) drifting them towards the electroluminescent (EL) region. At this time, detection of the primary scintillation in the PMTs plane coming from the de-excitation of the atoms sets the initial time of the event that will be also needed for positioning the event along the z-axis. Finally, when the secondary electrons reach the EL region, the signal is amplified and around 1100 photons per secondary electron are produced. Those photons are detected both in the energy plane where the total number of photons detected gives a measurement of the energy, and in the SiPM plane that provides the necessary information for the topology reconstruction.

In order to reconstruct the primary electron paths, time-resolved measurements of the light that arrives to the SiPM plane are required. Our approach is to measure how many photons reach each SiPM sensor each microsecond using a gated integrator. This provides enough resolution, as the electron drift speed in the Xe gas is approximately 1 mm/ms. A 16-channel front-end board that includes the analog paths and a digital section was designed. A detailed description of the board can be found in

[3]. Each analog path consists of three different stages: a transimpedance amplifier, a gated integrator and an offset and gain control stage.

The digital section consists of sixteen 12-bit 1-MHz ADCs and an FPGA for data formatting and communication with the upper readout stage.

The development of this electronics has played a crucial role in the reconstruction of electrons produced by ^{22}Na and ^{137}Cs [4]. The NEXT-DEMO detector has achieved an energy resolution of 1.62% FWHM at the 511 keV photoelectric peak of ^{22}Na [5] that extrapolates to better than 1% FWHM at Q_{bb} energies. Furthermore, the NEXT-DEMO prototype has demonstrated the capability of a SiPM array for topology reconstruction.

Nevertheless, there were a number of issues that need to be addressed for a larger-scale detector:

(1) more channels per front-end board are required, (2) channel-by-channel offset voltage adjustment by hand would be impractical and (3) power dissipation in the operational amplifiers was too high. Moreover, a single-ended readout scheme could not suppress the detector-coupled noise, which was much higher than expected. As a result, the noise amplitude was equivalent to 3-to-4 photoelectrons, which did not harm tracking at all but made it difficult to calibrate the tracking plane solely on the SiPM noise.

2 The tracking plane in the NEW detector

The NEW tracking plane is made of 28 Kapton Dice-Boards (KDBs), shown in figure 1. Each KDB has an 8x8 SiPM array placed with 1-cm pitch, a NTC temperature sensor and four LEDs for calibration. The KDBs over-cover the fiducial region with 1800 SiPMs, ensuring that there are no dead regions. The connector is located at the end of a long tail, and is screened from the gas, in the fiducial volume, by a 120 mm thick copper shield. The Dice-Boards (DBs) for NEXT-DEMO were made of multi-layer CuFlon, and their measured radioactivity was moderately high, due to the adhesive needed to glue the layers. Two additional problems with the DBs were the need to solder SiPMs by hand (since CuFlon does not tolerate the temperatures of an oven) and the need to use connectors (all of which are known to be non radiopure). The new KDBs for NEW solve all the above issues. The material is kapton, and the measured radioactivity budget (only upper limits) is one order of magnitude less than in the old DBs. The connector is located at the end of a long tail, and is screened from the gas by a thick copper layer. In addition, TPB was coated directly on top of the DEMO DBs. Instead, the design of the electroluminescent region with a quartz plate allows for a direct coating of the plate instead of the individual Dice-Boards.

2.1 Design considerations for the front-end cabling and electronics in the NEW tracking Plane

The design parameters, in terms of dynamic range and resolution are equivalent to those of NEXTDEMO. According to the NEXT simulation models we can expect up to 250 photoelectrons per microsecond in a SiPM sensor. A 1-ms integration time provides an adequate 1-mm resolution in the Z direction in the TPC.

Due to radiopurity requirements, electronics (including passive elements such as capacitors and resistors) must be placed behind the lead shield that surrounds the detector vessel. As a result, a gated-integrator approach is a better match for NEXT than a shaping circuit followed by a fast sampling. This is due to the fact that the total cable length from the SiPM sensor to the amplifier in the front end is approximately 5 meters, which has two main effects on the SiPM signal: (1) low signal-to-noise ratio as a result of pulse amplitude reduction and a potentially large and broadband noise

coupling from the environment, and (2) reflections due to high frequency components in the SiPM pulse. An integrator overcomes the low signal-to-noise ratio by attenuating high frequency noise and recovering pulse charge. Moreover, it is insensitive to high-frequency signal reflections in the line. This is more difficult to achieve with a fast sampling approach, unless a costly cabling solution is used to prevent noise coupling and signal reflections. As a lesson learned from NEXT-DEMO, both the cabling and the front-end amplifier must be balanced to allow common-mode noise reduction.



Figure 1. Left: Drawing of the Dice-Board, with the pigtail passing through the copper shield. Right: Picture of the kapton Dice-Board.

3 The front-end cabling

3.1 Kapton Dice-Boards (KDBs) and in-vessel cabling

The Dice-Board and the inner cable operate with a differential signal output in a broadside coupled traces scheme, connected directly to the anode and the cathode of the SiPM. That achieves a better reduction of the noise during signal acquisition. This scheme provides also a small parasitic capacitance which is enough to provide the SiPM fast current pulses, so there is no need of additional components inside the detector. The stackup consists in a 25 mm thick two-layer kapton core with a kapton coverlay bonded on each side (to minimize adhesives that would increase radioactive background). As shown in figure 1, the Dice-Board is a flexible kapton circuit which contains a 8 x 8 SiPM array. The design has a \sim 40 cm pigtail, which crosses the copper shielding and connects to the inner cable. The traces are 100 mm width with 0.5 mm pitch, which is a compromise solution for crosstalk, size and trace resistance. The inner cable has the same materials, stackup and trace geometry as the Dice-Board. The connectors used are the FX11LA series from Hirose, which are low profile high density board-to-board connectors. This cables are \sim 80 cm long, and connect the end of the Dice-Boards to a high density custom feedthrough.

3.2 External cabling

In order to keep background events to a minimum, front-end electronics are placed nearby the detector but beyond the lead castle that surrounds the TPC, with a total cable length of \sim 5 m from the sensor to the electronics. This poses a challenge in the design of a cabling solution that (1) is radio-clean enough to be inside the detector, (2) keeps enough signal-to-noise ratio in the relevant signal bandwidth for the gated integrator with a 5 m cable, (3) is cost-effective, (4) includes SiPM biasing voltage wires and (5) is also valid for the final NEXT phase (NEXT-100). Finally, differential transmission lines on fine-pitch FFC (flat flexible cable) cables outside the

detector were chosen as a good trade off between performance and cost. As shown in figure 2, the cables are 0.5 mm pitch with 280 x 76 mm traces; all embedded in a thin polyester layer. As said before, we take the anode and the cathode of each SiPM, which are connected to the signal and bias

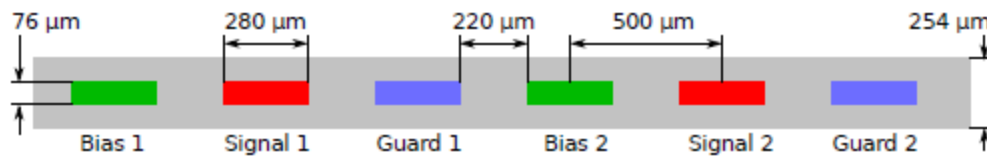


Figure 2. Cross-section of the external cable (just two channels are shown).



Figure 3. The FEB64 board.

lines respectively. Channels are separated by a guard trace connected to the analog ground in the front-end; so we need three lines for each SiPM channel plus the additional signals (temperature sensor and LEDs).

As we could not find commercial cables with that density of traces, we decided to split into four FFC cables. This way, the signals of a whole Dice-Board are distributed in four cables of 51 wires each. This distribution is done just at the output of the feedthrough, using a kapton adapter board. This board has the same stackup as the Dice-Board or the inner cable, and splits the signals in four DF9 Hirose connectors for the long cables. In order to further reduce the noise coupled to the external cables, they are wrapped with a 1 mm aperture mesh, also connected to the analog ground at the front-end. This mesh has its maximum attenuation rated at 1 MHz, which covers the range of frequencies we want to attenuate.

4 The front-end electronics board

4.1 Board layout

The FEB64 is a 3U x 220 mm module (figure 3). A 19" Eurocard chassis without backplane can accommodate up to 14 boards. Both front and rear ends are used for power and I/O. The front panel houses a 6-pin power connector, a JTAG connector to program the FPGA, a selectable HDMI (top) or RJ-45 (bottom) connector to the DAQ interface and up to 5 LEDs (only one is shown in the picture). The rear of the module houses the four (two on each side) connectors to the tracking plane, as described in

sections 3.1 and 3.2, as well as a 4-pin LEMO connector that brings the SiPM bias from a dedicated voltage source and forwards the remote temperature sensor wires to the same source for gain compensation [10]. The digital circuitry (FPGA, LVDS buffers, flash memories and voltage regulators for the digital ICs) reside on the left side of the card. The 64 analog channels (consisting each of two

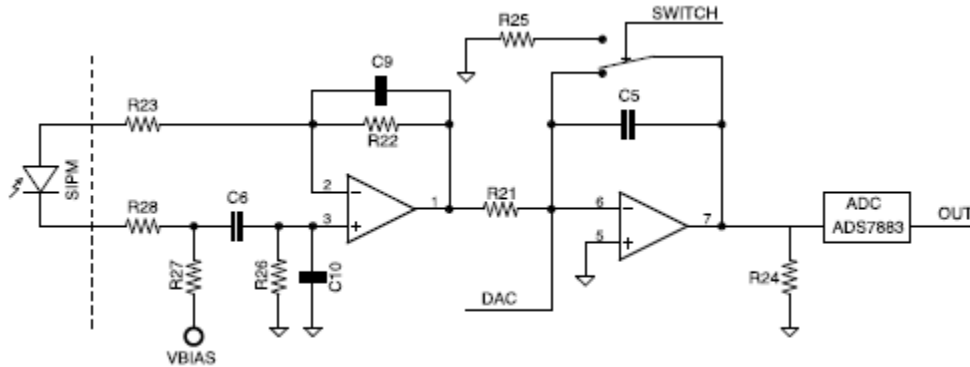


Figure 4. The analog channel circuit.

operational amplifiers, ADC and switch, as described in section 4.2) are located on the right side, in an 8-by-8 matrix. At the left of the matrix, a column with eight 8-channel DACs provide the voltages for the per-channel offset compensation.

4.2 The analog section: amplification and integration

The SiPM is biased at the front end board. Anode and cathode lines run to the SiPM sensors in a balanced configuration, as described in sections 3.1 and 3.2. As shown in figure 4, two resistors at the front-end input limit the current in the case of a SiPM short circuit and keep line balance. A differential-input transimpedance amplifier based on the low-power low-cost AD8055 operational amplifier reduces common mode noise and amplifies the SiPM current by approximately 1400 with a 10-MHz bandwidth. A per-channel automatic offset voltage compensation is implemented thanks to the on-board FPGA, which reads the ADC values, calculates the baseline and provides a DC compensation voltage via a DAC at the input of the integrating stage. The gated integrator, also based on the AD8055, provides the required gain (15 ADC counts per photoelectron, as the expected dynamic range is 250 photoelectrons in a microsecond and the ADC resolution is 12 bits). The switch is controlled by the FPGA at a 1 MHz rate. A few tens of nanoseconds are used to discharge the integrating capacitor, leaving the rest of the microsecond for integration.

Compared to the previous NEXT-DEMO front-end electronics [3], an amplification stage has been eliminated, the analog channel power (including the ADC) has been reduced by a factor of 3.5 to maximum 150 mW, cost is one third, the number of channels per front-end board has been increased by a factor of 4 and the signal-to-noise ratio has been improved by a factor of 4 thanks to the differential input stage. As a result, the FEB64 board is a valid solution for tracking planes in the scale of NEW and NEXT-100 (1800 and 7000 channels, respectively).

4.3 Digitization, data handling and interface to the DAQ electronics

An on-board FPGA Virtex-6 XC6VLX130T reads out data from up to 64 1-MHz ADCs, formats data, time-stamps and stores them in a reconfigurable-length dual-event circular buffer to avoid dead time. When a trigger is received, zero-suppressed data are read out and sent to the upper stage. The circular buffer is implemented with the internal resources of the FPGA and is able to store two complete events in raw mode,

whose maximum size corresponds to approximately twice the maximum detector drift time (up to 3.2 ms). Baseline adjustment and zero-suppression parameters (baseline reference, value over the baseline, pre- and post-samples, minimum number of samples to consider a pulse) are configurable through a set of commands. In zero-suppression

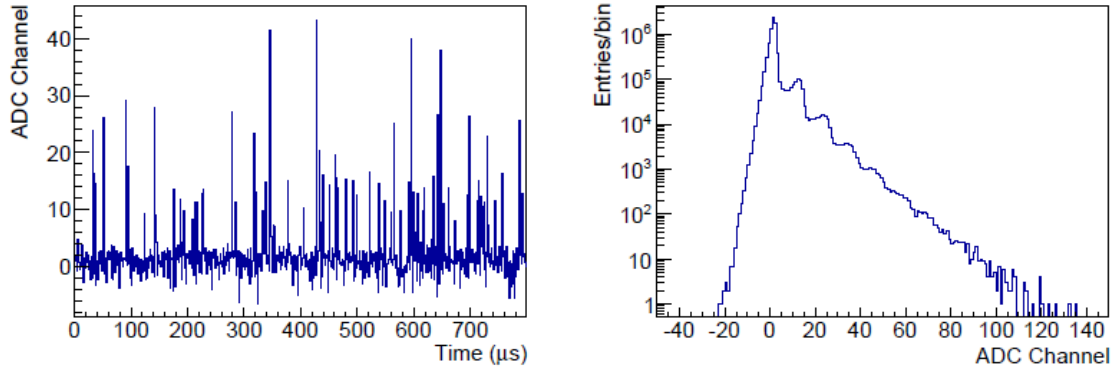


Figure 5. Left: Typical dark count waveform of the S10362-11-050P with an integration time of 1 ms. Right: Typical single photon spectrum (SPS) of the S10362-11-050P recorded in a sample time of 1 ms with dark count events (first peak is the pedestal noise)

mode, the system triggers when the signal exceeds the value over the baseline fixed during at least the minimum number of samples to consider a pulse. Then, this signal is sent with its pre- and post-samples. Raw data mode of operation, where no zero suppression occurs, is also supported for testing purposes.

Front-end cards interface the Scalable Readout System's (SRS) DAQ interface modules [7] (tested on both FECv3 and the new FECv6) through the SRS' DTCC (Data, Trigger, Clock and Control) link specification over copper [8]. In this link, data, trigger, clock and slow controls flow on the same RJ-45 or HDMI connector over 4 LVDS pairs. ALICE's DATE is used as DAQ software environment. As a result, the front-end electronics are fully compatible with CERN RD-51 SRS electronics. The DTCC configuration used is the basic one. The link has been fully tested up to 250 Mbps over the two data pairs using 1 meter SFTP 6A copper cables.

5 Results

A complete readout slice consisting of a KDB with 64 Hamamatsu S10362-11-050P SiPMs, a 5 m cable, a FEB64 front-end card, a DAQ interface module and a DAQ PC running the DATE environment has been tested. Signals generated by dark counts events have been used to produce their Single Photon Spectrum (SPS). The different intensities in the generated signals correspond to different numbers of fired pixels in the sensors during the electronic sample time (1 ms) (see figure 5-left). As observed in the most left peak in figure 5-right, the SPS indicates good photon counting capability, allowing to identify different peaks which are used to produce the absolute calibration of the channels (G), in number of ADC Counts per single photoelectron.

These results have been verified by using the Photon Transfer Curve (PTC) method with a LED source. From a very basic point of view, a read out channel, composed by a SiPM plus its associated electronics, is a system block with light as an input, and digital data as an output. The only noise introduced at the input is due to the nature of photons themselves, which is inherent to the light and it is known as shot noise [11]. A

random noise can be associated to the read out channel and its processing electronics, and represents the baseline noise in total darkness. Illuminating the SiPM,

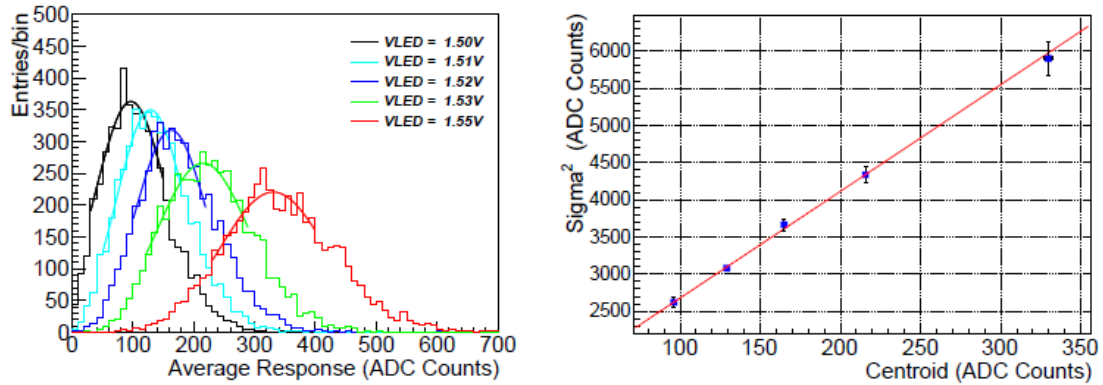


Figure 6. Left: Average response of the SiPM at different illumination levels of the LED and gaussian fit to the mean value. Right: Photon Transfer Curve of a SiPM and linear fit in the shot noise region obtaining the absolute gain of the system.

as the input light level increases in amplitude, the noise at the system output rises out of the baseline noise and becomes dominated by shot noise. Shot noise is directly related to the input illumination I , satisfies Poisson statistics and is therefore proportional to the square root of that signal:

$$s_I = \sqrt{I} \quad (5.1)$$

During the PTC measurements, SiPMs are exposed to a blue LED producing an uniform illumination and pulsed at different reverse bias voltage. The digital SiPM response (S_{ADC}) at different intensities is represented in figure 6-left. For an increase in illumination I , the digital SiPM response will change by $S_{ADC} = G \cdot I$, while $s_{ADC} = G \cdot s_I$. Using the anterior assumption of equation 5.1:

$$s_{ADC}^2 = (G \cdot s_I)^2 = G^2 \cdot I$$

$$s_{ADC}^2 = G \cdot S_{ADC} \quad (5.2)$$

Therefore, the absolute gain value of the system can be extracted from equation 5.2 as the slope of the linear fit between the digital SiPM response (S_{ADC}), and the square shot noise of the signal (see figure 6-right). The gains obtained, match perfectly with the ones calculated using dark counts events, ensuring the reliability of the results. In addition, the PTC method allows to study the linearity of the system, demonstrating to be linear in the range of low intensities (<40 pes), ~15% of the electronics dynamic range.

6 Conclusions and outlook

The front-end cabling and electronics requirements for NEW and NEXT-100 pose harder design constraints than those in NEXT-DEMO. Lessons learned with the front-end in NEXT-DEMO allowed the new solutions presented in this paper. A complete slice of the NEW tracking plane readout has been tested. Measurements based on dark count events and also with a LED source show good performance for the NEXT experiment and a correct behaviour of the full readout chain. Nevertheless, the front-end board is undergoing a minor design revision in late 2014 to correct some mechanical aspects as well as to reduce the noise produced by the on-board DC/DC

converter that powers the FPGA core. The construction and operation of NEW in 2015 will be a challenge, though good tracking results obtained with NEXT-DEMO and the measured performance of the NEW readout slice give cause for optimism. Beyond NEXT, the present work shows the feasibility of tracking applications based on SiPMs and discrete electronics in medium-scale detectors.

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