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Effects of the PWM carrier signals synchronization on the DC-Link current in Back-to-Back Converters

L.G. González [a], G. Garcerá [b], E. Figueres [b], R. Gonzalez[b].

[a] Departamento de Electrónica y Comunicaciones, Universidad de los Andes, núcleo la Hechicera, 5101, Mérida-Venezuela.
[b] Grupo de Sistemas Electrónicos Industriales del Departamento de Ingeniería Electrónica, Universidad Politécnica de Valencia, Camino de Vera s/n, 46022, Valencia-España.

Abstract: This paper presents a study about the synchronization effects of the PWM carrier signals of a back-to-back converter for grid connection of Wind Energy Conversion Systems based on Permanent Magnet Synchronous Generators. It is demonstrated by means of a spectral analysis that, with the proper synchronization of the carrier signals of both the rectifier and inverter stages, the *rms* value of the current through the DC-Link capacitors is greatly reduced. As a result, the number of capacitors needed to build the back-to-back converter decreases, whereas its life cycle is expanded, so that the Wind Energy Conversion System becomes more cost effective. It is shown that the worst case occurs when the phase difference between both carrier signals is $\pm\pi/2$, yielding the highest *rms* value of the DC-link capacitors current. In that case the harmonic with the highest *rms* value is located at twice the switching frequency. The theoretical analysis is compared with experimental results from a *10kW* back-to-back converter in order to validate the effects of the carrier signals phase shift on the DC-link capacitors current.

Keywords: Back-to-Back Converter, PWM modulator, Synchronization of carrier signal, ripple current.

1.- Introduction

Back-to-back power converters are extensively used in wind energy conversion systems. Recent studies show that the back-to-back topology has a better performance than other topologies for low and medium power applications [1]. This topology is also used in other variable frequency applications, like motor drives with an active front-end [2]. Fig. 1 shows a back-to-back converter working from a permanent magnet synchronous generator (PMSG), a typical low and medium power Wind Energy Conversion System (WECS). In this case the PMSG is operated at variable speed, whereas its position and speed are estimated using sensorless techniques [3]. Due to the unpredictable and variable nature of the wind, a Maximum Power Point Tracking (MPPT) algorithm varies the turbine speed, by acting on the rectifier stage control, in order to extract as much energy as possible from the wind [referencias MPPT, incluida la nuestra]. The back-to back converter is composed by a three-phase PWM rectifier and an inverter, linked by a capacitive DC-Bus or DC-link.

It´s well known that reliability and efficiency are important elements in power converters design [4]. Several studies point out the importance of the ripple current reduction in the DC-link capacitors [5-8]. This reduction implies the reduction of converter losses, expanding the capacitors life while decreasing their size. Besides, the reduction of the capacitors size has a positive influence on the size and cost of the power converter, whereas the expansion of the capacitors life increases the exploitation benefits of the WECS, being operative during a longer time.

This work shows the synchronization effects of the PWM carrier signals of the rectifier and of the inverter on the DC-link capacitors current. The synchronization conditions that minimize the ripple current of the DC-link capacitors are determined. The theoretical analysis is performed by means of the Fast Fourier Transform (FFT) and experimentally validated.

This paper is organized as follows. Section 2 presents the ripple current effects on the DC-link capacitor. Section 3 expresses analytically the current through the DC-link capacitance as a function of the phase shift between the PWM carrier signals of the rectifier and of the inverter. Section 4 describes the control structure of the back-to-back converter, taking into account the synchronization of the PWM carrier signals. Section 5 shows the analytical and experimental results of the DC-link capacitors currents, both in the time and in the frequency domains. Finally, in section 6 the conclusions from this study are presented.

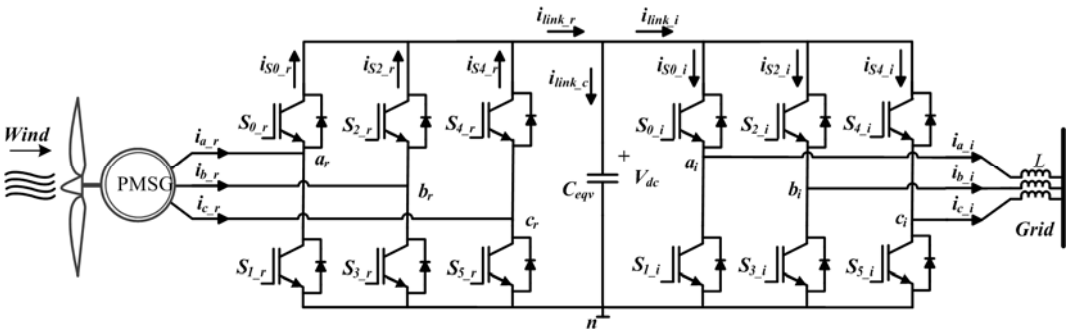


Fig.1, General scheme of a wind energy conversion system based on a back-to-back converter.

2.- Effects of the current ripple on the DC-link capacitors

The electrolytic capacitors main faults are caused by several factors such as overvoltages, temperature and vibrations, as well as reverse voltage or excessive charge and discharge cycles. Besides these physical variables, the ripple currents reduce capacitors life, because they are responsible for electrical losses, increasing the capacitors temperature and causing vaporization of the electrode. This behavior yields a capacitance reduction and an increase of the equivalent series resistance (ESR) associated to the capacitor [9]. Eq. (1) shows the calculation of the estimated useful life of a capacitor (L_x)

$$L_x = L_0 \cdot K_{Temp} \cdot K_{Voltage} \cdot K_{Ripple} \quad (1)$$

, where L_0 represents the maximum useful life. K_{Temp}, $K_{Voltage,}$ K_{Ripple} stand for the temperature, voltage and ripple current coefficients, respectively. The ripple coefficient decreases as the ripple current increases, thus reducing the capacitor useful life. Another important consequence of the ripple current increase in the capacitor is the electrical losses rise. Those losses are represented by equation (2)

$$P_{loss} = \sum_{i=1}^{n} I_i^2 \cdot ESR(i) \quad (2)$$

, where I_i represents the *i-th* harmonic current *rms value*, and *ESR(i)* represents the equivalent series resistance at the frequency of the current harmonic under consideration. Fig. 2 represents the variation of the capacitor *ESR* with frequency for an ALS31A331DF500 electrolytic capacitor (500V, 330µF), from the company BHC, for an ambient temperature of 55ºC [10].

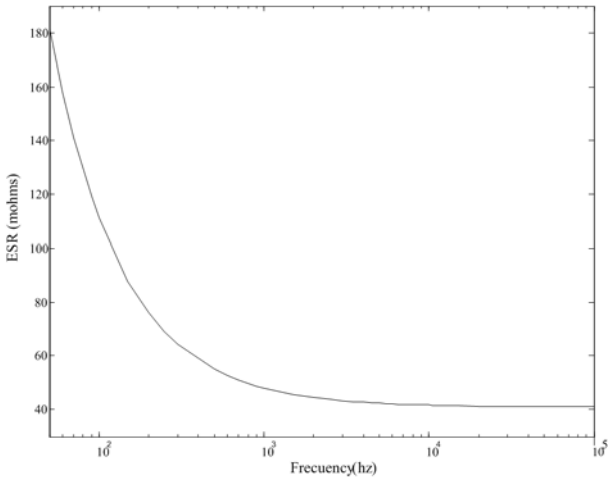


Fig. 2, Equivalent series resistance (ESR) of ALS31A331DF500 electrolytic capacitors @ 55°C.

3.- Analysis of the DC-Link Current in a Back-to-Back Converter

The analytical method for determining the capacitor current is obtained from [11] and [12], where a voltage switching function is used [12], applying an asymmetrical regular sampled modulation. The DC-link current is calculated as the difference between the rectifier and inverter currents, following equation (3), see Fig.1. The rectifier and inverter currents are calculated as the sum of the individual phase currents multiplied by their corresponding switching function, equations (4) and (5). Subscript *r* stands for the rectifier stage, whereas subscript *i* stands for the inverter stage. Table A-1 in Appendix A explains the nomenclature used in this section.

$$i_{link_C}(t) = i_{link_r}(t) - i_{link_i}(t) \tag{3}$$

$$i_{link_r}(t) = \sum_{\eta=1,2,3} \hat{I}_{a_{1_r}} \cdot \cos\left(\omega_{1_r} t + \varphi_{\eta_r} - \varphi_{0_r}\right) \cdot S_{\eta_r}\left(t, \omega_{1_r}, \omega_{sw}, \varphi_{\eta_r}, \varphi_{PWM_r}\right) \tag{4}$$

$$i_{link_i}(t) = \sum_{\eta=1,2,3} \hat{I}_{a_{1_i}} \cdot \cos\left(\omega_{1_i} t + \varphi_{\eta_i} + \varphi_{0_i}\right) \cdot S_{\eta_i}\left(t, \omega_{1_i}, \omega_{sw}, \varphi_{\eta_i}, \varphi_{PWM_i}\right) \tag{5}$$

In (4) and (5), the switching functions $S_{\eta r}$ (rectifier) and $S_{\eta i}$ (inverter) of the converter legs associated to phase η (η=*1*,*2*, and *3* for phases *a*, *b* and *c*, respectively) are obtained from the voltages between the midpoints of each converter leg and point n of the DC-link: v_{ar_n}, v_{br_n}, v_{cr_n} for the rectifier, and v_{ai_n}, v_{bi_n}, v_{ci_n} for the inverter [12]. For instance, the switching function of the rectifier leg associated to phase *a* is defined by (6), in terms of the Fourier transform of voltage v_{ar_n} expressed by (7).

$$S_{1_r}\left(t, \omega_{1_r}, \omega_{sw}, \varphi_{1_r}, \varphi_{PWM_r}\right) = \frac{v_{a_r n}\left(t, \omega_{1_r}, \omega_{sw}, \varphi_{1_r}, \varphi_{PWM_r}\right)}{V_{dc}} \tag{6}$$

$$v_{a_r n}\left(t, \omega_{1_r}, \omega_{sw}, \varphi_{1_r}, \varphi_{PWM_r}\right) = \frac{V_{dc}}{2} + \frac{2V_{dc}}{\pi} \sum_{n=1}^{+\infty} \frac{1}{n\left(\frac{\omega_{1_r}}{\omega_{sw}}\right)} J_n\left(n\left(\frac{\omega_{1_r}}{\omega_{sw}}\right)\frac{\pi}{2} m_{a_r}\right) \sin\left(n\frac{\pi}{2}\right) \cos\left(n\left(\omega_{1_r} t + \right.\right. \tag{7}$$

In (8) the variable *q* is defined as:

$$q = m + n \cdot \left(\frac{\omega_{1_r}}{\omega_{sw}}\right) \tag{8}$$

The DC-link capacitors current expression (9) is obtained by the substitution of equations (4) and (5) into equation (3),

$$i_{1}(\left[link\right]_{1}C)(t) = \Sigma_{1}(\eta = 1,2,3)^{1}3 \left[i^{\wedge}{}_{1}(a_{1}(1_{1}r))\right) \cdot \cos(\omega_{1}(1_{1}r)\, t + \varphi_{1}(\eta_{1}r) - \varphi_{1}(0_{1}r))\right) \cdot [1/2$$

(9)

Note from (9) that the phase values of both PWM carrier signals (φ_{PWMr} for the rectifier, and φ_{PWMi} for the inverter) determine the current through the DC-link capacitance, and thus its *rms* value. Other studies [13] and [15] have determined an approximate expression of the *rms* current through the DC-link capacitance, without taking into account

the phase difference between the PWM carrier signals of the rectifier and of the inverter, $\Delta\varphi_{PWM}$, represented by equation (10). For the case $\Delta\varphi_{PWM}=0$, it results an approximate *rms* value of the DC-link capacitor current, $i_{tnkc_{rms}}(t)$, given by equation (11):

$$\Delta\varphi_{PWM} = \varphi_{PWM_r} - \varphi_{PWM_i} \tag{10}$$

$$i_{tnkc_{rms}}\Big|_{\Delta\varphi_{PWM}=0} = \hat{i}_{a_r}\sqrt{m_{a_r}\left(\frac{\sqrt{3}}{4\pi}+\left(\frac{\sqrt{3}}{\pi}-\frac{9m_{a_R}}{16}\right)\cdot\cos^2(\varphi_{0_r})\right)} \tag{11}$$

Both the rectifier and the inverter DC side instantaneous value currents, $i_{tnk_r}(t)$ and $i_{tnk_i}(t)$, can be calculated as the sum of a DC component and a switching harmonics component. For instance, equation (12) represents $i_{tnk_r}(t)$, where I_{tnk_r} is the DC value and $\tilde{i}_{tnk_r}(t)$ is the switching harmonics component. The DC component of the rectifier DC side current is represented by equation (13) [14].

$$i_{tnk_r}(t) = I_{tnk_r} + \tilde{i}_{tnk_r}(t) \tag{12}$$

$$I_{tnk_r} = \frac{3}{4}m_{a_r}\hat{i}_{a_{1_r}}\cos(\varphi_{0_r}) \tag{13}$$

From [14] it results that the DC component of the inverter DC side current is shown by equation (14).

$$I_{tnk_i} = \frac{3}{4}m_{a_i}\hat{i}_{a_{1_i}}\cos(\varphi_{0_i}) \tag{14}$$

Note that, neglecting the losses in the DC-link capacitors, the DC values of the DC side currents of the rectifier (13) and of the inverter (14) agree in steady state, because the steady state DC current of the DC-link capacitance is null.

4.- Description of the control structure and measurement setup.

This section describes the control structure and measurement setup for the study of the PWM carriers synchronization effect on the DC-link capacitors current. The power converter general diagram control is shown in Fig. 3. This control framework includes a current control loop in the synchronous reference frame with classic PI controllers and a vectorial control technique with $I_d=0$ [16]. The controller of the rectifier stage uses a Kalman observer to estimate the speed and angular position of the PMSG [17], and a classical perturb and observe algorithm for the maximum power point tracker (MPPT) [18].

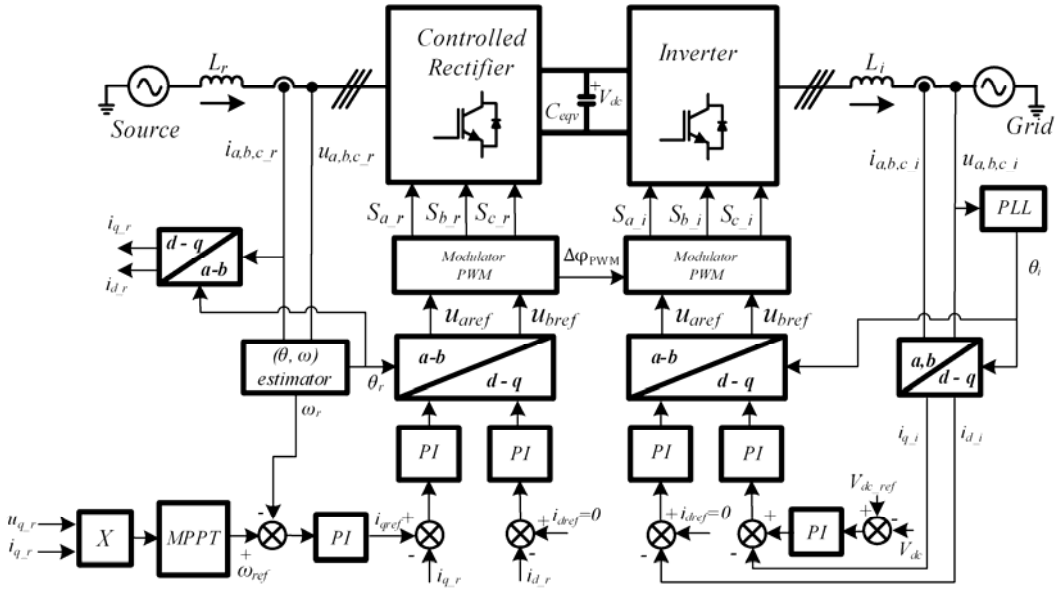


Fig. 3, General control scheme of the Back-to-Back Converter

In this application the energy source is a PMSG working at variable speed, which implies that the fundamental frequency of the rectifier input voltage and current, f_{1r}, is variable. Nevertheless, the fundamental frequency of the inverter output, f_{1i}, is constant and agrees with the grid frequency. The goal in the rectifier stage is to extract the maximum power from the wind generator using an MPPT algorithm. The MPPT defines the PMSG operation speed. The objective of the inverter stage is to extract the available energy from the DC-link, maintaining the DC-link voltage constant. In this application, both the rectifier and the three phase inverter have the corresponding control loops for the respective line currents: the currents in inductors L_r are controlled by the rectifier, whereas the currents in inductors L_i are controlled by the inverter. The current control is implemented in the synchronous reference *d-q* frame [16-19], using PI controllers tuned by means of zero-pole assignment [20]. In the experimental tests, the total DC-link current capacitance is calculated starting from the measurement of the current through one of the DC-link capacitors (C_8), see Fig. 4.

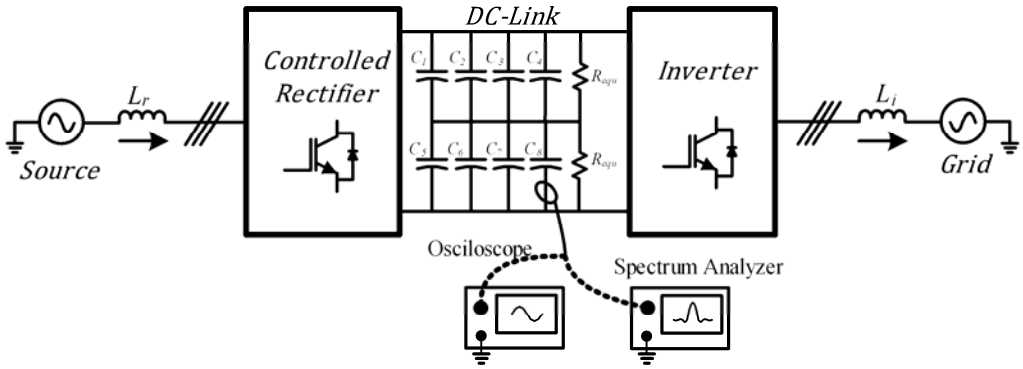


Fig. 4, General scheme for the measurement of the DC-link current of the Back-to-Back Converter

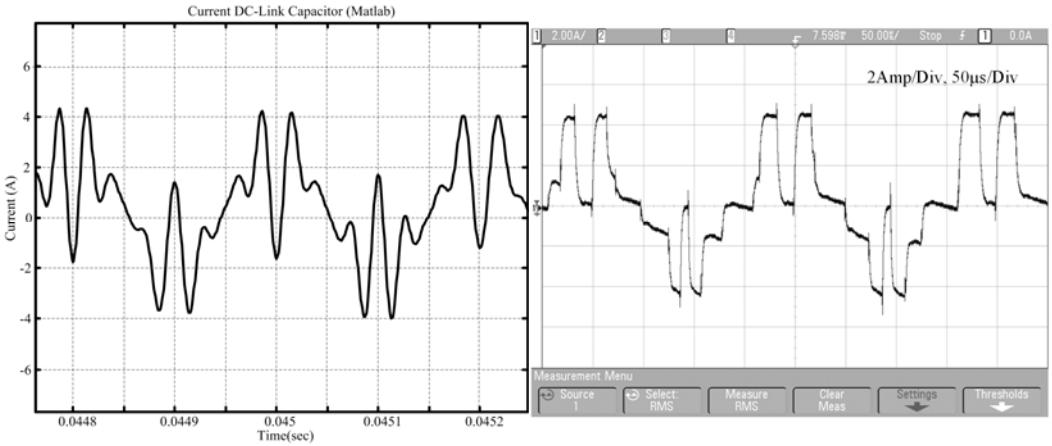
5.- Analytical and experimental results.

A photograph of the experimental setup is shown in Fig. 5. The rated power of the experimental back-to-back converter is *10kW*. In all the measurements the operating power is *10kW* and the DC current obtained from the rectifier stage is $I_{link_r} = 12.5 Amp.$ The power semiconductors of both the rectifier and the inverter stage are BSM 50 GB 120 DN2 IGBTs from EUPEC, working at a switching frequency of $f_{SW}=5kHz$. The DC-link is composed by eight equal electrolytic capacitors of 330µF and 500V model ALS31A331DF500 from BHC, making up a total DC-link capacitance of 660µF (see Fig. 4). The control algorithms are running on a DSP model TMS320F2812 of Texas Instruments. Further prototype characteristics are shown in table A-2 in appendix A. The current in one DC-link capacitor current is measured using a high frequency current probe and the Agilent oscilloscope model MSO6014A. The reason of measuring only one capacitor current is not to increase the parasitic inductance of the DC-link when separating from it capacitors by means of cables (see Fig. 4). The total DC-link current is calculated as four times the measured capacitor current. The spectral measurements have been carried out by means of an Agilent 4395A Spectrum Analyzer. For the spectral analysis the current harmonics are represented in dB: $I(dB)=20\cdot log(\hat{I}_i)$, where $\hat{I}_i$ represents the peak value of the *i-th* current harmonic.

Fig. 5, Experimental Setup.

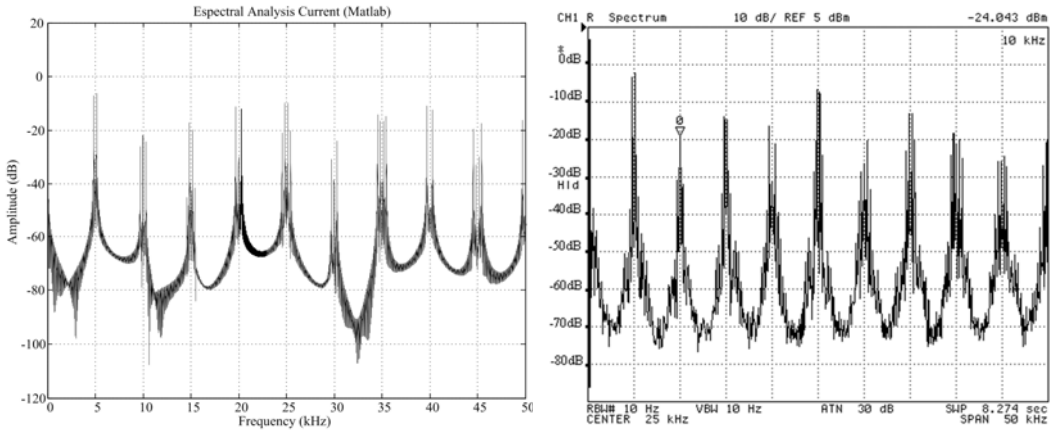
Using the equations of the DC-link current studied in section 3, the system parameters shown in Table A-2 in Appendix A and the experimental setup in Fig. 5, it is possible to determine the theoretical DC-link capacitor current using the first ten harmonics of the switching frequency (*n=10).* Fig. 6 shows the theoretical and experimental capacitor current in the time domain for the case: $\Delta\varphi_{PWM}=0°$. The *rms* values of the analytical and experimental capacitor currents agree, being *1.31A*. Note from Fig. 6 that the waveforms of both capacitor currents are similar, with a peak value of around *4A* in both cases.

Fig. 7 shows the frequency spectrum of the analytical and experimental capacitor current for $\Delta\varphi_{PWM}=0°$. The theoretical spectral analysis has been performed using the *MATLAB*® built-in Fast Fourier Transform [21], as it is shown in figures 7a and 9a, and also in figures 10a to 15a. From those figures, it is observed that the main harmonics are located at sidebands centered at multiples of the switching frequency. It is worth pointing out that, due to the high frequency modulation ratio ($m_f>20$), it is not possible to notice all the harmonics of each sideband in the theoretical *MATLAB*® frequency spectra of the measured DC-link current. On the contrary, the resolution bandwidth of the 4395A Spectrum Analyzer (*RBW=10Hz*) allows for a good discrimination of all the experimental harmonics. It can be observed from experimental Figure 7b that the main two harmonics (at *4950Hz* and *5050Hz*) of the capacitor current are located around the switching frequency, having an equal amplitude of *XXX A (YYY dB)*. Analytical Fig. 7a corroborates the predominance of those harmonics for $\Delta\varphi_{PWM}=0°$.



(6a) *(6b)*

Fig. 6, DC-Link capacitor current in the time domain @ $\Delta\varphi_{pwm}=0°$, (6a Analytical result, 6b Experimental results with a scale 2A/div, 50µs/div).

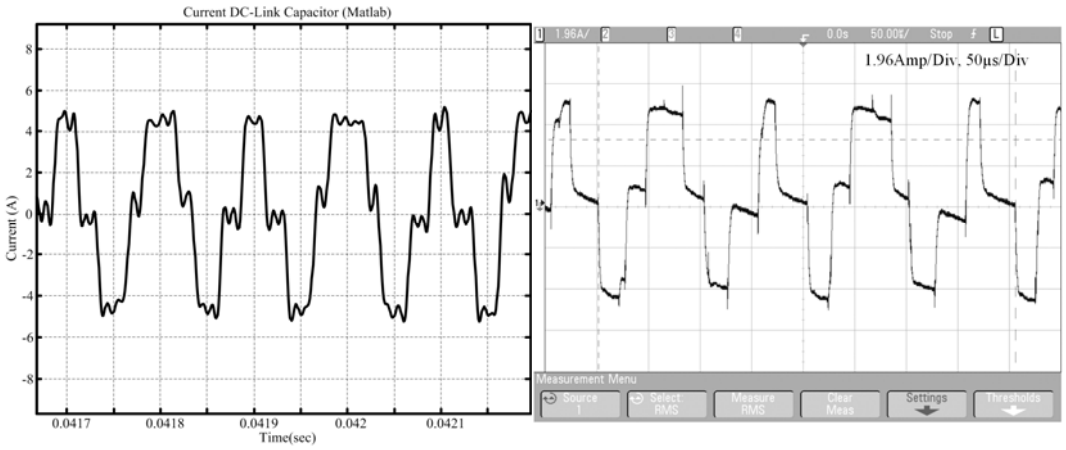


(7a) *(7b)*

Fig. 7, Spectral analysis of the DC-Link capacitor current @ $\Delta\varphi_{pwm}=0°$, (7a Analytical results, 7b Experimental results with a scale 10dB/div, 5kHz/div).

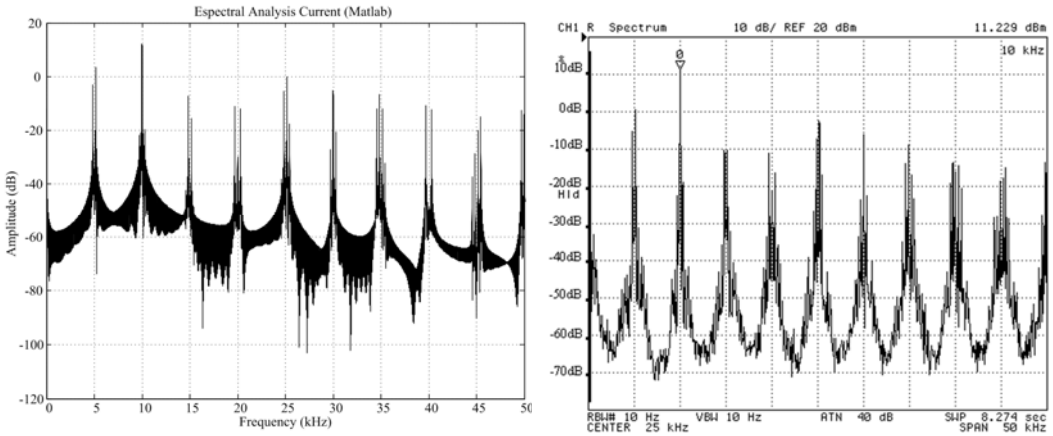
Fig. 8 shows the DC-link capacitor current in the time domain for the maximum current ripple case, i.e. when $\Delta\varphi_{pwm}=\pm 90°$. In that case both the analytical and the experimental capacitor current have an *rms* value of *4.01A*. Note from Fig. 8 that the waveforms of both capacitor currents are similar, with a peak value of around *5A* in both cases.

Fig. 9 shows the analytical and experimental frequency spectrum of the DC-link capacitor current for $\Delta\varphi_{pwm}=\pm 90°$. It can be observed from this figure that the main harmonic is located at twice the switching frequency ($2f_{sw}=10kHz$), having an experimental amplitude of XXX A (YYY dB) and a theoretical amplitude of XXX A (YYY dB). Note the great agreement between both values.



(8a) *(8b)*

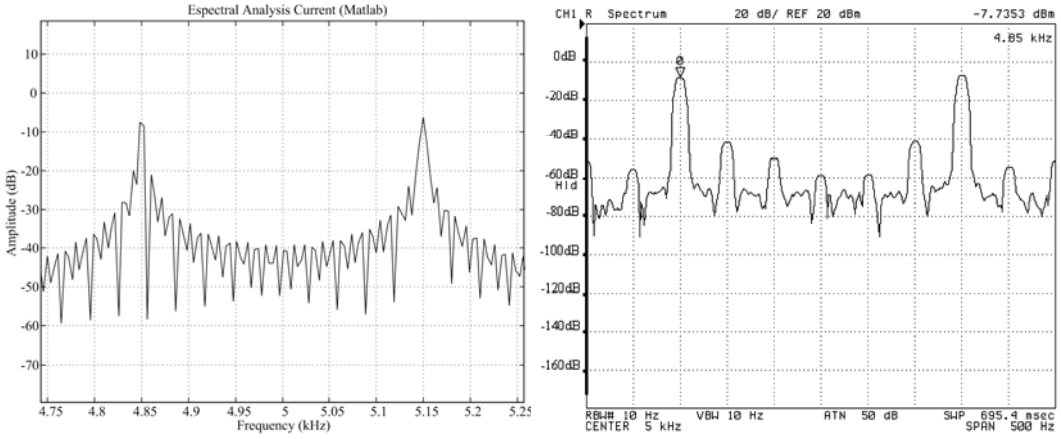
Fig. 8, DC-Link capacitor current in the time domain @ $\Delta\varphi_{pwm}=90°$, (*8a* Analytical result *8b* Experimental results with a scale 1.96A/div, 50µs/div).



(9a) *(9b)*

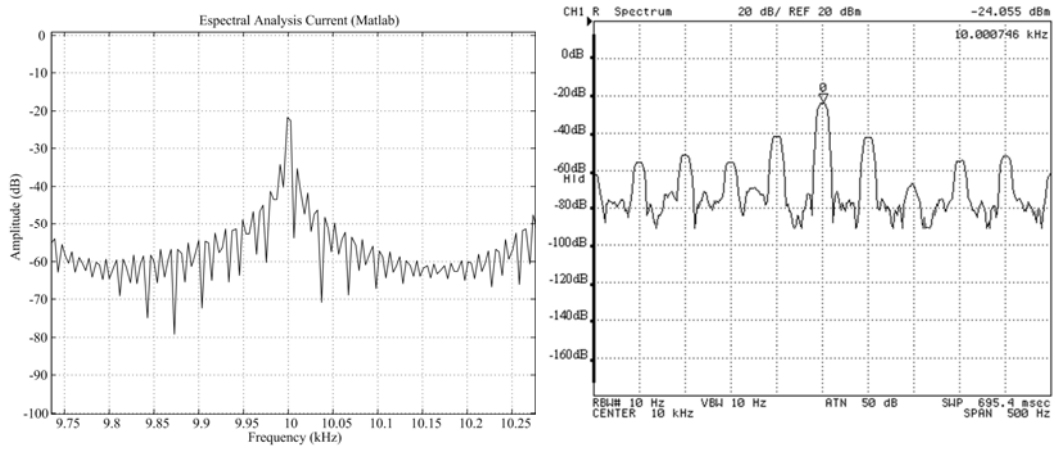
Fig. 9, Spectral analysis of the DC-Link capacitor current @ $\Delta\varphi_{pwm}=90°$, (9*a* Analytical results, *9b* Experimental results with a scale: 10dB/div 5kHz/div).

Fig. 10 to 15 show the detailed analytical and experimental frequency spectra of the first three sidebands, centered at *5 kHz, 10 kHz* and *15 kHz*, for the cases $\Delta\varphi_{pwm}=0°$ *and* $\Delta\varphi_{pwm}=90°$. Note that the dominant harmonics of the experimental spectra agree with the theoretical ones in an important degree.



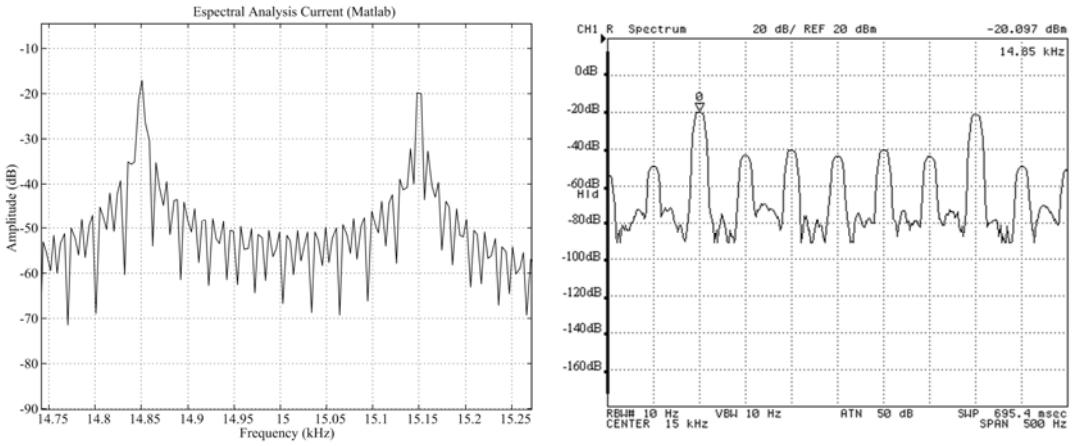
(10a) *(10b)*

Fig. 10, Spectral analysis of the DC-Link capacitor current: Sideband around 5kHz @ $\Delta\varphi_{pwm}=0°$, (10*a* Analytical result, *10b* Experimental results with a scale 20dB/div 50Hz/div).



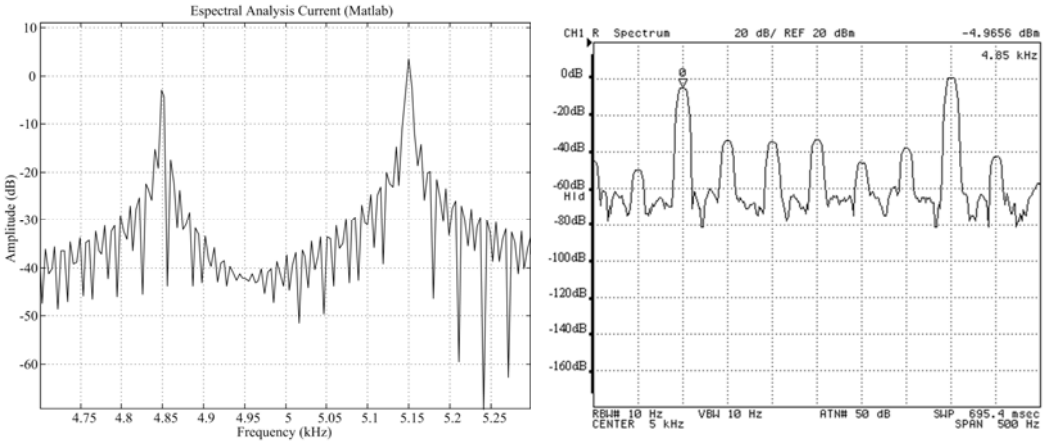
(11a) *(11b)*

Fig.11, Spectral analysis of the DC-Link capacitor current: Sideband around 10kHz @ $\Delta\varphi_{pwm}=0°$, (*11a* Analytical result, *11b* Experimental results with a scale 20dB/div 50Hz/div).



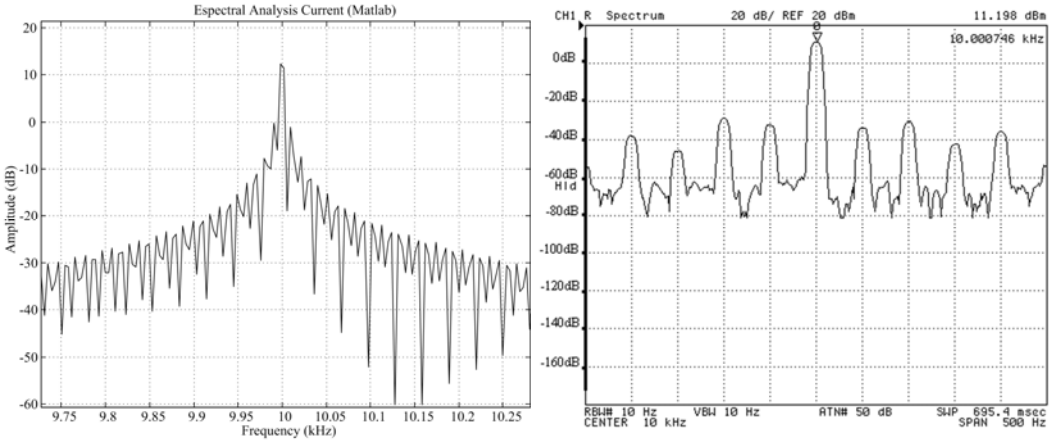
(12a) *(12b)*

Fig.12, Spectral analysis of the DC-Link capacitor current: Sideband around 15kHz @ $\Delta\varphi_{pwm}=0°$, (12*a* Analytical result, *12b* Experimental results with a scale 20dB/div 50Hz/div).



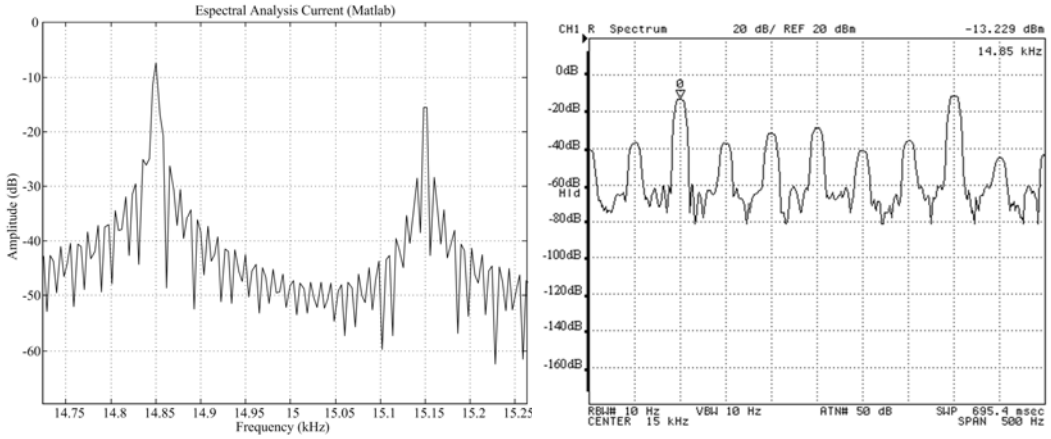
(13a) *(13b)*

Fig. 13, Spectral analysis of the DC-Link capacitor current: Sideband around 5kHz @ $\Delta\varphi_{pwm}=90°$, (13*a* Analytical result, *13b* Experimental results with a scale 20dB/div 50Hz/div).



(14a) *(14b)*

Fig. 14, Spectral analysis of the DC-Link capacitor current: Sideband around 10kHz @ $\Delta\varphi_{pwm}=90°$, (14*a* Analytical result, *14b* Experimental results with a scale 20dB/div 50Hz/div).



(15a) *(15b)*

Fig. 15, Spectral analysis of the DC-Link capacitor current: Sideband around 15kHz @ $\Delta\varphi_{pwm}=90°$, (*15a* Analytical result, *15b* Experimental results with a scale 20dB/div 50Hz/div).

Table 1, shows the value of the *rms* current of each DC-link capacitor, both in the experimental and analytical case, for several angles of the PWM carriers phase difference, $\Delta\varphi_{pwm}$. In the same table it is represented the power dissipated in each capacitor and its life expectancy for each $\Delta\varphi_{pwm}$ value, using the calculation formulae of [10]. An ambient temperature of *55ºC* and an operation voltage of *400V???* have been assumed. It is observed that both the theoretical and the experimental *rms* capacitor currents increase in a factor around 3 when $\Delta\varphi_{pwm}$ changes from *0°* to *90°*. The associated capacitor losses increase in a factor around 9, with the resulting capacitor life reduction from *205.58 kHours* to *136.95 kHours*.

Table 1. *RMS* values of the current measured in one DC-Link capacitor as a function of $\Delta\varphi_{pwm}$

$\Delta\varphi_{pwm}$ (°)	±180, 0	±165, ±15	±150, ±30	±135, ±45	±120, ±60	±105, ±75	±90
Capacitor *RMS* current (*A*) (Experimental.)	**1.31**	**2.01**	**2.69**	**3.32**	**3.78**	**3.92**	**4.01**
Capacitor *RMS* current (*A*) (Theoretical)	**1.02**	**1.74**	**2.56**	**3.08**	**3.39**	**3.60**	**3.75**
Capacitor losses (*W*)	**0.57**	**1.34**	**2.40**	**3.66**	**4.75**	**5.11**	**5.35**
Capacitor Life (*kHours*)	**204.58**	**191.72**	**175.63**	**157.73**	**143.98**	**139.70**	**136.95**

The *rms* current through the whole DC-link capacitance related to the DC current provided by the rectifier (13), $i_{linkr_{RMS}}/I_{linkr}$, is shown in Fig. 16. This figure shows that the minimum value of the *rms* capacitors current occurs when $\Delta\varphi_{pwm}=0°$ and $\pm180°$, whereas the worst case occurs when $\Delta\varphi_{pwm}=\pm90°$. The analytical and the experimental curves in Fig. 16 show a high agreement. On one hand, the minimum theoretical *rms* value of the DC-link capacitance current is $0.35\cdot I_{linkr}$, whereas its experimental value is $0.4\cdot I_{linkr}$. On the other hand, the maximum theoretical *rms* value of the DC-link capacitance current is $1.15\cdot I_{linkr}$, whereas its experimental value is $1.22\cdot I_{linkr}$. As it is also observed from table 1, the capacitors *rms* current increases in a factor 3 when $\Delta\varphi_{pwm}$ changes from *0°* to *90°*.

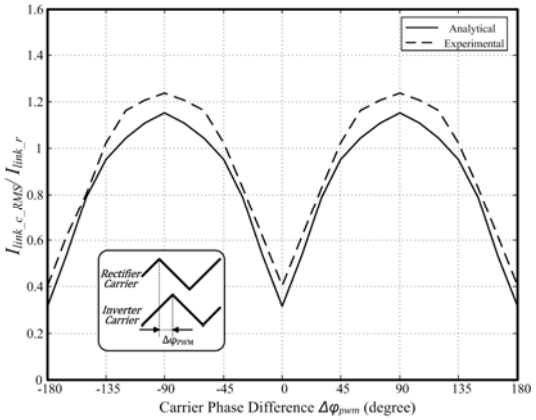


Fig.16, *RMS* current through the whole DC-link capacitance as a function of the PWM carrier phase difference, $\Delta\varphi_{pwm}$.

6.- Conclusion

In back to back converters the synchronization of the PWM carrier signals of the rectifier and of the inverter has an effect on the DC-link capacitance current. The analytical and experimental results on a *10kW* converter show that the PWM carriers phase difference, $\Delta\varphi_{pwm}$, determines the *rms* value and the harmonics of the DC-link capacitance current, which are minimized for $\Delta\varphi_{pwm}=0^0$ and 180^0, and maximized for $\Delta\varphi_{pwm}=90^0$. Taking into account this effect it is possible to both minimize the DC-link losses, increasing the converter efficiency, and to extend the DC-link capacitors useful life.

In the experimental prototype under study the *rms* DC-link capacitance current decreases in a factor around 3 when $\Delta\varphi_{pwm}$ changes from *90°* to *0°*. Therefore, the associated capacitor losses decrease in a factor around 9, achieving a capacitor life cycle extension from *136.95 kHours to 205.58 kHours*. Taking into account that the capacitors life is a factor that strongly limits the life cycle of the whole system, the exploitation benefits of a WECS can be increased by properly synchronizing the PWM carrier signals of the back-to-back converter.

Besides, the reduction of the DC-link capacitors current ripple allows for a smaller DC-link capacitance, decreasing the size and cost of back-to-back converters.

From the practical point of view, if the control of the rectifier and of the inverter is not performed by the same digital processor, synchronization between the carriers of both processors should be implemented in order to minimize the DC-link currents.

Appendix A.

Table A-1. Nomenclature

L_x	Estimated useful life of a capacitor.
L_o	Base useful life base of a capacitor.
$\hat{i}_{a_{1r}}$	Peak current (per phase) in the controlled rectifier stage.
f_{1_r}	Fundamental frequency of the rectifier stage.
$\hat{i}_{a_{1i}}$	Peak current (per phase) in the inverter stage.
f_{1_i}	Fundamental frequency of the inverter stage.
f_{sw}	Switching frequency
m_{a_r}	Amplitude modulation index of sinusoidal PWM.
$J_k(x)$	First kind Bessel function of order k.
φ_{0_r}	Phase shift between the fundamental ac voltage and current: rectifier stage.
φ_{η_r}	$\varphi_{\eta_r} = (1 \quad \eta) \times \frac{2\pi}{3}$; Where η *=1, 2* and *3,* for phase a, b and c. respectively: rectifier stage.
φ_{0_i}	Phase shift between the fundamental ac voltage and current: inverter stage.

φ_{η_i}	$\varphi_{\eta_i} = (1-\eta) \times \frac{2\pi}{3}$; Where η =*1, 2* and *3,* for phase a, b and c. respectively: inverter stage.
φ_{PWM_r}	Phase of the Rectifier PWM carrier signal
φ_{PWM_i}	Phase of the Inverter PWM carrier signal

Table A-2. Parameters of the experimental setup

Power converter parameters		***Grid Parameters (inverter and rectifier side)***	
DC-Link capacitance	*660 μF*	*RMS line voltage*	*400 V*
DC-Link voltage	*800 V*	*Line inductances (L_r, L_i)*	*5 mH*
Switching frequency $\omega_{sw} = 2\pi f_{sw}$	*5 kHz*	*Fundamental frequency (f_{1r}=f_{1i})*	*50 Hz*

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