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Measurement of the Loop Gain Frequency Response of Digitally Controlled Power Converters

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Abstract—The study of the loop gains frequency response in a power converter is a powerful tool commonly used for the design of the controllers used in the control stage. As the control of medium and high power electronic converters is usually performed digitally, it is useful to find a method to measure the digital loop gains. The purpose of this paper is to present a method for properly measuring the loop gain frequency response of digitally controlled power converters by means of an analog Frequency Response Analyzer (FRA). An analog sinusoidal reference signal generated by the FRA is injected through an Analog to Digital Converter (ADC) into the digital controller, and added to the discrete feedback signal. To obtain the frequency response of the open loop gain, both feedback and disturbed feedback signals are sent back to the FRA by using the Pulse Width Modulation (PWM) peripherals of the controller.

Index Terms— Pulse width modulated power converters, Power system measurement, Power system control, Digital signal processors (DSP).

I. INTRODUCTION

I t is well known that the analysis of the open loop gain frequency response of a closed loop controller allows the designers to study the dynamic response as well as the stability of the system [1,2]; for that reason, the loop gain is usually measured in the design procedure of the controllers, obtaining Nyquist plots [3,4] or their equivalent Bode plots [5-9]. Both of them allow measuring the phase and gain margins, which in turn gives information about the bandwidth and the stability of the process, among other important parameters.

Once the controllers have been designed and implemented, it is possible to obtain an experimental measurement of the open loop gain by disturbing the closed loop system [10], allowing the designer to adjust the parameters of the regulators

to obtain the desired dynamic response of a prototype. It is worth pointing out that the method presented in [10] was developed for analog feedback systems, and it is common to find commercial frequency response analyzers based on it. Those equipments are capable of performing the open loop gain measurement in an accurate way, thus allowing the adjustment of the critical parameters related to the control of electronic power converters. Nevertheless, it should be pointed out that nowadays the control of most medium and high power converters is based on digital controllers implemented on DSP or FPGA; therefore the method presented in [10] should be modified to be used in the digital domain.

Although different methods to measure the frequency response of digitally controlled power converters have been proposed [11-13], all of them use a considerable amount of resources that in some cases could make impossible for the programmer to fit the code in the processor. Besides, these methods are complex and need the software of the controllers to be modified far away from the original one, incrementing the time-to-market time. Nevertheless, in [11] this fact is justified by the reason that the gain-phase margin monitor is designed to be used in an on-line monitoring system, where one of the main goals is a cost-competitive solution; in this scenario, it is worth designing a frequency response analyzer embedded in the DSP, thus avoiding the use of a stand-alone FRA. However, special care should be taken if the control strategy of the power converter takes a considerable amount of resources from the DSP, as it could be not possible to fit the code of the embedded FRA in the processor. In [12], the proposed method is intended to be used along with a PC. In this case, as real time communication is needed between the processor and the PC, real time control reliability problems could arise. Finally, in [13] the frequency response analysis is used for system identification purposes, making the overall process too complex.

The purpose of this paper is to design a simple method based on [10] to measure open loop gains in digitally controlled electronic power converters, by means of a stand-alone Frequency Response Analyzer (FRA). An analog variable frequency sinusoidal reference signal generated by the FRA is injected through an Analog-to-Digital Converter (ADC) [14] into the digital controller, and added to the discrete feedback signal. In order to obtain the frequency response of the open loop gain, both feedback and perturbed

feedback are sent to the FRA by using the Digital Pulse Width Modulation (DPWM) peripheral of the controller; this implies that the DPWM performs the task of a Digital-to-Analog Converter (DAC). The proposed method does not require many computational resources, and allows using standard measurement equipments, with no need of complex additional code in the control software. Besides, it allows to measure the control loop gains of variables that are not physical but mathematical, e.g. dq control of three phase power converters [15], as the discretized reference signal can be injected in any place inside the discrete loop.

It is important to consider that the quantization effect as well as the resolution of the ADC and the DPWM could introduce limit-cycle oscillation problems and a poor Signal-to-Noise Ratio (SNR) [16,17] due to the digital nature of the proposed method. This implies discrepancies between measured and actual loop gain that could lead to errors in the design process. For that reason, a method is presented in this paper that takes into account both the SNR and the quantization effect of the ADC and the DPWM, so that measurement errors are minimized.

The paper is organized as follows. In section II, an overview of the proposed measurement technique along with its operation principle is shown. In section III, a more detailed study of the measurement stages is presented, focusing on the gain adjustment of the important signals used to measure the loop gain. Additionally, a suitable small signal model based on the principles of PWM [18], is used to study the dynamics, error and noise introduced by the ADC and DPWM stages in the measurement [19-21]. Section IV presents the modeling and digital current control [22-25] of a 10 kW voltage source rectifier by means of a Texas Instruments DSP TMS320F2812. This rectifier has been used to test the proposed loop gain measurement method by means of a FRA NF Corp. FRA5097. Finally, experimental results of the prototype described in section IV are shown in section V.

II. MEASUREMENT OF THE LOOP GAIN FREQUENCY RESPONSE

Electronic power converters are usually operated by means of closed loop control of the most relevant space state variables of the system. Fig. 1 shows a simplified block diagram of a typical converter where several signals are sensed in order to make the space state variables of interest to follow the desired references by means of closed loop control strategies. Therefore, several loop gains (T_1, T_2, ... ,T_n) should be analyzed in order to assure the system stability along with the desired dynamic performance, by adjusting the respective gain and phase margins by means of properly designed regulators [1].
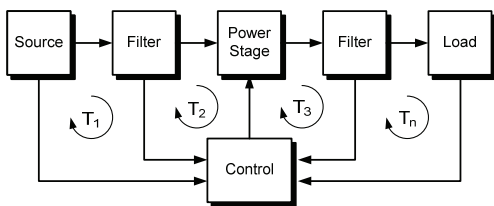

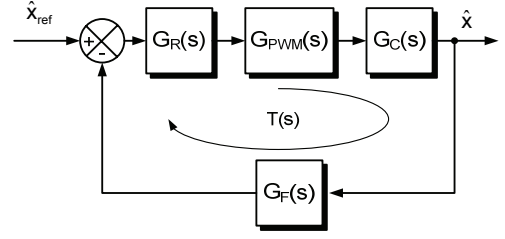Fig. 1. Basic block diagram of a closed loop controlled power converter.

Fig. 2. Closed loop control of the small signal variable $\hat{x}$.

Once the power converter, including filters and load, has been modeled, the classic control structure shown in Fig. 2 could be obtained for each of the small signal variables to be controlled, where the open loop gain $T(s)$ can be calculated according to (1), where $G_R(s)$, $G_{PWM}(s)$, $G_C(s)$ and $G_F(s)$ are the transfer functions in Laplace domain of the regulator, the PWM modulator, the power converter and the sensing gain and filters, respectively.

$$T(s) = G_R(s)G_{PWM}(s)G_C(s)G_F(s) \qquad (1)$$

A. Analog modulation scheme

Although the closed loop could be broken for the open loop gain, $T(s)$, to be measured, it is advisable to keep the loop closed, so that the converter operation point is kept.

A method to measure $T(s)$ based on the injection of an *ac* signal into the closed loop has been presented in [10]. Fig. 3 shows the suggested injection point in the original circuit, which satisfies the condition described in [10] and [26] to avoid measurement distortion, being expressed by (2), where Z_o is the output impedance of $G_F(s)$ and Z_i is the input impedance of $G_R(s)$.

$$\left| \frac{Z_o}{Z_i} \right| \ll 1 \qquad (2)$$

Furthermore, it should be noted that the *ac* signal has to be injected at a point of the loop where the waveform is smooth and well-behaved [14].

Fig. 4 shows the disturbed closed loop small signal equivalent block diagram of the system, where $\hat{x}_d$ and $\hat{x}_f$ are the disturbed and the feedback signal respectively, and $X(s)$ is the Laplace transform of the sinusoidal disturbance signal, as shown in (3).
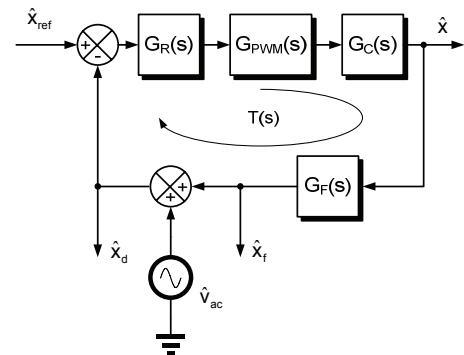

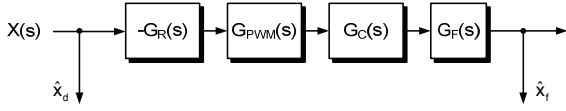Fig. 3. AC signal injection point in closed loop.

Fig. 4. Disturbed closed loop small signal equivalent block diagram.

Measurement of both signals $\hat{x}_d$ and $\hat{x}_f$, allows for the analysis of *T(s)* according to (4). It should be noted that the measurement is 180 degrees out of phase, so that the measured loop gain should be inverted in order to obtain the actual loop gain frequency response. Commercial FRAs are usually capable of performing the proposed measurement by generating a small *ac* signal whose frequency ω_i is swept along the desired bandwidth and injected into the analog control loop. The FRA is also capable of sensing the disturbance and feedback signals, obtaining the Bode plots of *T(s)*. Nevertheless, if a digital signal processor is chosen for the control of the power converter, a new approach has to be taken into account in order to measure the discrete open loop gain.

$$X(s) = V_{ac} \frac{\omega_i^2}{s^2 + \omega_i^2} \tag{3}$$

$$-\frac{\hat{x}_f}{\hat{x}_d} = \frac{X(s) \cdot T(s)}{X(s)} = T(s) \tag{4}$$

B. Proposed method for digitally controlled power converters

In order to perform the digital control of the power converter, some of the space state variables have to be discretized by means of the ADCs usually integrated in the digital processor. Hence, Fig. 2 should be modified according to Fig. 5. It is worth pointing out that the digital regulator $G_R(z)$ is the discretized version of the analog controller $G_R(s)$ [19] and that the DPWM gain has to be chosen according to the type of modulation implemented [20]. Although the design of the discrete regulator is beyond the scope of this paper, it is important to take into account that the discrete loop gain, T_d, has a different Bode plot to that of the analog loop gain, *T(s)*, as the discretization process modifies the dynamic response of the control system.

In order to measure the discrete loop gain T_d by using the method described in previous sections, both points A and B in Fig. 5 could be used to inject the *ac* signal. Despite the fact
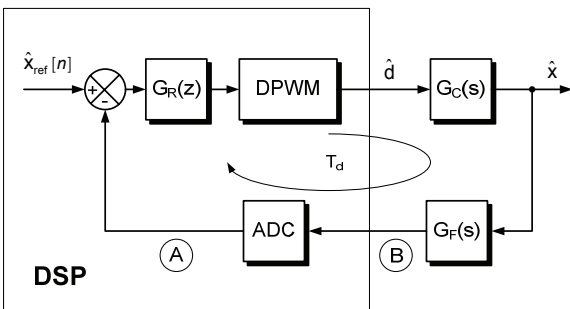
that point B offers the advantage of measuring discrete loop gain by means of the analog modulation scheme with an analog FRA, point A is the preferred injection point, mainly because once the perturbation has been discretized, it could be used to measure several transfer functions other than the open loop gain [23]. Besides, there are some digital control schemes where the optimal injection point is the one defined by point A in Fig. 5, e.g. *dq* control of three phase power converters. This is due to the fact that the controlled variables are the projection of the measured variables in a Synchronous Reference Frame (SRF) [15]. Therefore, the disturbance of the measured variables and not of the projected ones doesn't allow the measurement of the loop gains in the *dq* frame. This issue will be discussed in more detail in section IV.

A simplified scheme of the proposed method to measure the discrete loop gain T_d is depicted in Fig. 6, where an FRA from NF Corp. (FRA5097), has been used to generate the disturbance $\hat{v}_{ac}$ and to obtain the loop gain frequency response according to (4). The output of the built-in oscillator of the FRA $\hat{v}_{osc}$ is filtered out by means of $G_{osc}(s)$. This stage is composed by the anti-aliasing filter, $H_{AA}(s)$, and the *dc* gain, G_{osc}, as shown in (5), and allows to avoid aliasing problems and to extend the effective number of bits used for the internal representation of the discretized signal $\hat{v}_{ac}$, as it is discussed later on.

$$G_{osc}(s) = G_{osc} \cdot H_{AA}(s) \tag{5}$$

For the bipolar signal $\hat{v}_{ac}$ to be discretized, a voltage level shift circuit, *LS↑↑*, must be used to center the signal in the middle of the ADC Full Scale Range (FSR). Finally, $\hat{v}_{ac}$ is discretized by means of an ADC included in the processor.

As the disturbed signal $\hat{x}_d$ and the feedback signal $\hat{x}_f$ are measured by the FRA to obtain the loop gain frequency response, they have to be converted from discrete to analog.
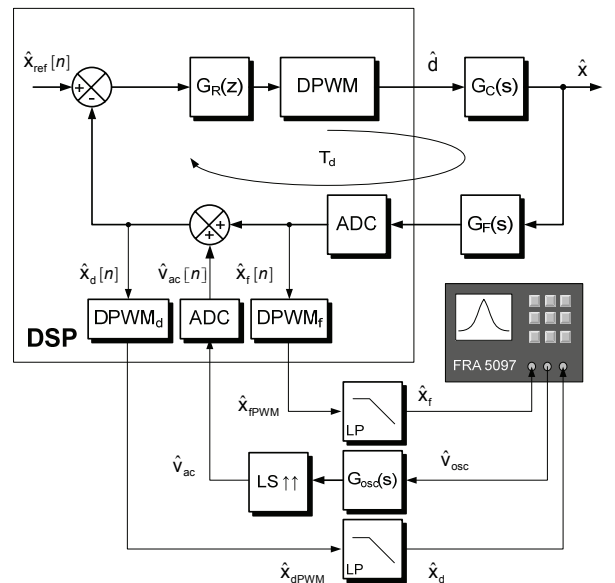

Fig. 5. Digital control of the small signal variable $\hat{x}$.

Fig. 6. Proposed method to measure the discrete loop gain *Td*.

Although the straightforward solution could be to make the conversion by using a DAC, commercial DSP's used to control electronic power converters, as the widely used C2000 family from Texas Instruments, usually don't include this functionality. However, PWM outputs driven by built-in digital comparators are a common feature that can be exploited to obtain an analog version of the discrete signals, as it can be seen in Fig. 6, where the disturbed and the feedback signals are modulated by the PWM peripheral of the DSP, and then low-pass filtered in order to eliminate the PWM harmonics, obtaining $\hat{x}_d$ and $\hat{x}_f$. These signals are the inputs fed to the FRA to compute the loop gain frequency response. It should be noted that the low pass filter used to remove PWM harmonics is not always mandatory, as the FRA uses a selective notch filter in the measuring process. Nevertheless, if the FRA includes an automatic gain adjustment input stage, it is advisable to use the low pass filter for the correct operation of this stage. This ensures that the automatic gain is adjusted with the amplitude of fundamental harmonic and not with the amplitude of the PWM pattern.

III. PRACTICAL IMPLEMENTATION

The conditioning, ADC and PWM modulation stages influence the measurement of the loop gain frequency response. Therefore they have to be modeled and included in the block diagram of the overall system. Besides, quantization errors as well as limitations in the SNR will appear because the measurement process implies the use of analog-to-digital conversion and PWM modulation. Hence, the design process described next should be carried out to minimize these effects.

A. Modeling of the disturbance signal conditioning and discretization process

Fig. 7 shows the proposed disturbance signal conditioning and discretization process, where G_{osc} is the gain applied to the FRA oscillator output, $H_{AA}(s)$ is an anti-aliasing filter, $LS\uparrow\uparrow$ is a level shifter and G_{ac} is a discrete gain.

Due to the fact that the sampling rate is generally low in high power conversion applications, interferences caused by the power semiconductors switching could be aliased into the low-frequency band as a result of sampling, therefore an anti-aliasing filter $H_{AA}(s)$ must be used [21]. Typical filters includes 4th order filters based on the cascade connection of two 2nd order filter as the one shown in (6), where the cut-off frequency, ω_c, is designed to be less than half of the sampling frequency and Q is chosen to obtain a butterworth response, hence $\omega_c \leq 4\pi/T_s$ and $Q=0.7$, where T_s is the sampling period.

$$H_{AA}(s) = \frac{\omega_c^2}{s^2 + \dfrac{\omega_c}{Q}s + \omega_c^2} \qquad (6)$$

The ADC can be modeled as an ideal Sample and Hold circuit (S/H) followed by a quantizer [19,21], as depicted in Fig. 7. On one hand, it is usual to model the S/H circuit as a Zero Order Hold (ZOH), so that the discretization process adds a delay according to the mathematical model presented in (7).
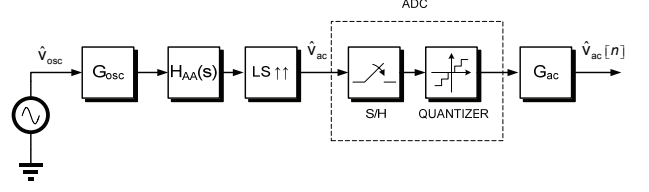

Fig. 7. Block diagram of the disturbance signal conditioning.

$$ZOH(s) = \frac{1 - e^{-sT_s}}{s} \qquad (7)$$

On the other hand, the quantizer limits the SNR according to (8), where N_e is the effective number of bits used to code the input signal, and could be calculated according to (9), n is the ADC number of bits, FSR is the ADC full scale range in volts and $V_{acpk\text{-}pk)}$ is the peak to peak voltage of the ADC input signal in volts.

$$SNR = 6.02 \cdot N_e + 1.76 \; (dB) \qquad (8)$$

$$N_e = n - floor\left(\frac{\log_{10}\left(\dfrac{FSR}{V_{ac(pk-pk)}} \right)}{\log_{10} 2} \right) \qquad (9)$$

In order to achieve a good SNR, N_e should be chosen as high as possible, so that $V_{ac(pk-pk)}$ has to be designed in order to make $N_e=n$, i.e., the maximum possible value for N_e. It is worth adding that sinusoidal signals are bipolar, whereas the conversion range of the ADC only supports positive values, so that some offset must be applied to the signal to be discretized.

Taking both the SNR improvement and the offset concerns into account, G_{osc} and $LS\uparrow\uparrow$ stages should condition the FRA output signal according to Fig. 8. Hence, the gain G_{osc} described by (10) should be applied, where the peak voltage of the FRA output signal in volts, $V_{osc(peak)}$, and FSR, are known design parameters. Besides, the level-shift stage should add an $FSR/2$ offset.

$$G_{osc} = \frac{FSR}{2 \cdot V_{osc(peak)}} \qquad (10)$$

The last gain used to condition the disturbance signal is G_{ac}, which is included to experimentally adjust the level of the injected signal, so that its level is high enough to excite the loop producing measurable signals, but low enough to keep the system around its operating point.

Once the different gains included in the conditioning process of the disturbance signal have been described, it is advisable to study their influence on the system dynamics, because it is desirable that the conditioning and discretization processes don't modify the loop gain measurement. For this reason, the gain $G_{ADC}(s)$ is defined as the product of the signal conditioning transfer functions depicted in Fig. 7, whose expression is shown in (11).

$$G_{ADC}(s) = G_{osc} \cdot H_{AA}(s) \cdot ZOH(s) \cdot G_{ac} \qquad (11)$$
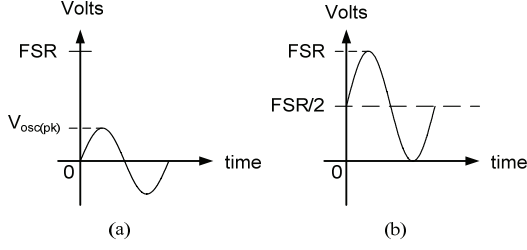
Fig. 8. Oscillator output conditioning by means of level shift and gain G_{osc}. (a) Original signal. (b) Conditioned signal.

Fig. 9. Perturbed closed loop small signal equivalent block diagram.

By obtaining the continuous domain transfer functions of the discrete regulator $G_R(z)$ and the DPWM, $G_R(s)$ and $G_{DPWM}(s)$ respectively, and taking into account the delay, $ZOH(s)$ (7), introduced by the ADC at the output of $G_F(s)$, it is possible to obtain the continuous equivalent block diagram of the digital control shown in Fig. 5 [19] depicted in Fig. 9. This allows studying the effect of including $G_{ADC}(s)$ in the measurement of the loop gain T_d.

From Fig. 9 it is possible to deduce the analog equivalent loop gain frequency response $T_d(s)$ by applying (12) and (13).

$$T_d(s) = G_R(s) G_{DPWM}(s) G_C(s) G_F(s) ZOH(s) \quad (12)$$

$$-\frac{\hat{x}_f}{\hat{x}_d} = \frac{X(s) \cdot G_{ADC}(s) \cdot T_d(s)}{X(s) \cdot G_{ADC}(s)} = T_d(s) \quad (13)$$

As expression (13) matches with (4), it is possible to conclude that the measurement of the loop gain frequency response is not affected by the conditioning and discretization process carried out on the disturbance signal.

Nevertheless, it is worth pointing out that the measurement bandwidth is limited by the Nyquist frequency; therefore the sampling rate has to be chosen to be higher than twice the loop gain upper frequency of interest. By taking into account that the small-signal model of the power converter is only valid up to half the switching frequency, the sampling frequency can be chosen double of the switching frequency. This assures a correct measurement of the open loop gain in the frequency range where the small-signal model of the power converter is valid.

B. Modeling of the disturbed and feedback signals conditioning and modulation process

In order to convert both disturbed and feedback signals from discrete to analog, the use of the DSP integrated PWM peripherals is proposed. PWM effects in the loop gain measurement are discussed in this section, taking into account both quantization and dynamic issues.

Fig. 10 shows the typical double-update DPWM used in the control stage of a power converter, where $\hat{x}_c[n]$ is the controller output, along with the single-update DPWM of the disturbed discrete variable $\hat{x}_d[n]$, $\hat{x}_{dPWM}$. Besides, T_{PWM} is the period of the DPWM modulator of the control stage, T_s is the sampling period, and T_{clk} is the period of the counter used to implement the DPWM ramp of both, the control stage and the loop measurement stage. In the control stage, the controller
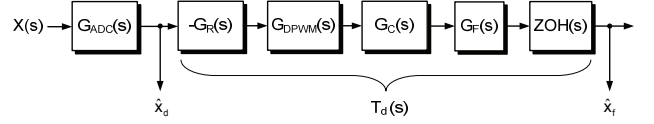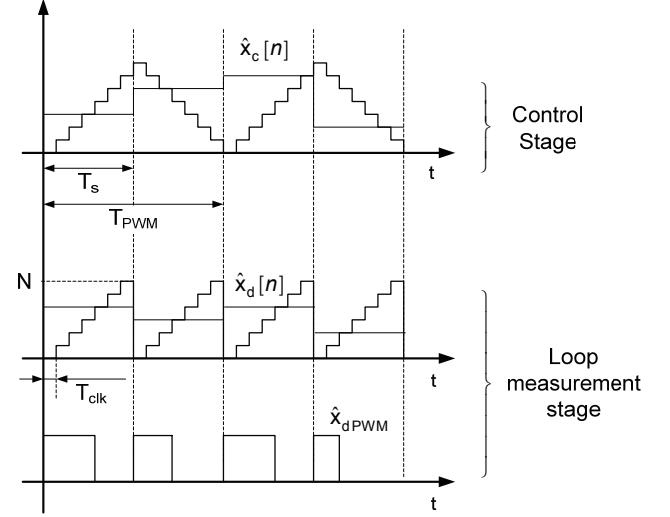

Fig. 10. 3 bit double-update DPWM used in control stage and single-update DPWM used in loop measurement stage.

output, $\hat{x}_c[n]$, is compared with a triangular carrier wave, producing the variable duty cycle square wave that controls the power semiconductors commutation, whereas in the loop measurement stage, the disturbed signal $\hat{x}_d[n]$ is compared with a sawtooth carrier wave in order to obtain the pulse width modulated signal, $\hat{x}_{dPWM}$. By filtering this signal with the low pass filter shown in Fig. 6, $\hat{x}_d$ is obtained. This method is also applied to the signal $\hat{x}_f[n]$ in order to obtain $\hat{x}_f$, so that (13) can be used to measure T_d. It should be noted that the period of the DPWM used to convert discrete signals into analog ones, should be equal to the sampling period, T_s. This allows for the Nyquist-Shannon theorem to be met, making possible the measurement of T_d from DC up to half the sampling frequency.

In order to analyze the effect of the DPWM in the measurement of the loop gain T_d, a model of this stage is needed. Fig. 11 shows a widely accepted block diagram of the uniformly-sampled or digital PWM [16,17,20] of the discrete variables $\hat{x}_d[n]$ and $\hat{x}_f[n]$, where the quantization error as well as a certain delay, $G_{DPWM}(s)$, associated to the ZOH effect due to the digital nature of DPWM have been considered. A discrete gain, G_x, as well as a low-pass filter, $LP(s)$, have been included to condition the signals before modulation and to filter out the modulation high frequency harmonics, respectively. As it will be explained later, G_x and $G_{DPWM}(s)$ must be equal in both $\hat{x}_d[n]$ and $\hat{x}_f[n]$ DPWM stages.

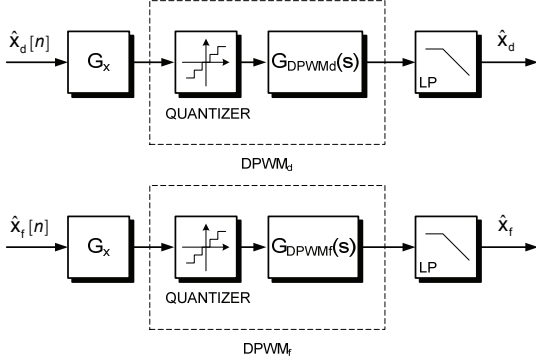The quantization effect of the DPWM modulation has been

Fig. 11. Block diagram of the digital PWM stage used to convert disturbed and feedback signals into analog.

studied in [16], showing that there is a limit-cycle oscillation problem associated with the resolution of both, the DPWM and the ADC used to discretize the control and disturbance variables. The conclusions of these papers point out that the limit-cycle oscillation can be avoided if the DPWM resolution is higher than that of the ADC. Moreover, the SNR depends only on the ADC resolution if the aforementioned condition is met.

From Fig. 10 it is possible to deduce (14), where N is the counts number from the loop measurement stage counter reset to the loop measurement stage counter overflow. Operating from (14), (15) can be obtained. By substituting (15) into (16), (17) is obtained, which allows to determine the minimum single-update DPWM resolution in bits, m, needed to accomplished the desired sampling frequency f_s.

$$T_s = N \cdot T_{clk} \tag{14}$$

$$N = \frac{f_{clk}}{f_s} \tag{15}$$

$$2^m = N \tag{16}$$

$$m = ceiling\left(\log_2\left(\frac{f_{clk}}{f_s}\right)\right) \tag{17}$$

Taking (9) into account, and making FSR=1, it is possible to find a relationship between the maximum DPWM duty cycle, D_{max}, and the effective number of bits of the digital modulator, M_e, as shown in (18).

$$M_e = m - floor\left(\frac{\log_{10}\left(\dfrac{1}{D_{max}}\right)}{\log_{10}(2)}\right) \tag{18}$$

As stated previously, it is possible to avoid limit-cycle oscillations as well as to limit the SNR to that of the ADC by allowing the DPWM resolution to be higher than the ADC resolution, meeting condition (19).

$$M_e > N_e \tag{19}$$

From (18) it is quite obvious that by maximizing m and D_{max}, M_e can be increased, whereas f_{clk} could be chosen from (17); therefore, a method to adjust D_{max}, thus obtaining the desired value for M_e, has to be devised. For that reason, the disturbed and feedback signals have been defined as shown in (20) and (21), where $\bar{X}_d[n]$ and $\bar{X}_f[n]$ are the disturbed and feedback steady-state signals, respectively, whereas $\hat{x}_d[n]$ and $\hat{x}_f[n]$ are the disturbed and feedback small-signal terms, respectively. Taking into account that the injected disturbance is adjusted to keep the system working around the operation point, (22) can be applied.

$$X_d[n] = \bar{X}_d[n] + \hat{x}_d[n] \tag{20}$$

$$X_f[n] = \bar{X}_f[n] + \hat{x}_f[n] \tag{21}$$

$$\bar{X}_d[n] = \bar{X}_f[n] \tag{22}$$

Steady-state and small-signal components of the feedback signal ($\bar{X}_f[n]$ and $\hat{x}_f[n]$ respectively) along with the DPWM ramp, are shown in Fig. 12 (a). A similar figure could be obtained for the disturbed signal.

In order to achieve the desired maximum duty cycle, D_{max}, the signals in Fig. 12 (a) have to be modified according to Fig. 12 (b). By applying the gain G_x and adding a level-shifter offset $N/2$, the original signals in Fig. 12 (a) become those of Fig. 12 (b), where D_{max} is the desired maximum duty-cycle according to (18) and (19). It is important to realize that both $X_d[n]$ and $X_f[n]$ could adopt either positive or negative values. This implies that a level-shifter stage has to be included, so that the signals could be modulated by means of the DPWM.

In order to obtain the correct value of the gain G_x, (23) is derived, where $X_{f\,max}[n]$ is the maximum value of the feedback signal, whose expression is shown in (24) and (25).

$$G_x = \frac{\left(D_{max} - \dfrac{1}{2}\right)}{X_{f\,max}[n]} \cdot N \tag{23}$$

$$X_{f\,max}[n] = \bar{X}_f[n] + \hat{x}_{f\,max}[n] \tag{24}$$

$$\hat{x}_{f\,max}[n] = |T_d|_{max} \cdot \hat{v}_{ac}[n] \tag{25}$$
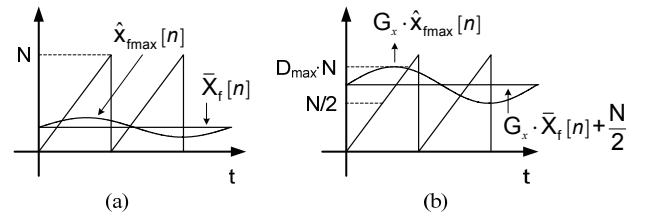

Fig. 12. Steady-state and disturbance components of the feedback signal and N bits DPWM ramp (a) without *Dmax* adjustment and (b) with *Dmax* adjustment.

It should be noted that $\bar{X}_f[n]$ is the steady-state value of the feedback signal, which can be calculated or measured previous to the loop gain measurement. Besides, $|T_d|_{max}$ is the expected maximum absolute value of the loop gain, whose value could be previously obtained by means of simulation or analytical methods. Finally, it could be derived from Fig. 6 that the effect of the loop gain, T_d, is applied to the discretized disturbance signal, $\hat{v}_{ac}[n]$, so that expression (25) can be used.

Once the quantizer effect of DPWM has been studied, it is important to take into account the dynamic behavior of the digital modulator, $G_{DPWM}(s)$. In order to achieve an as high as possible resolution in bits, m, it is advisable to use single-update DPWM for the modulation of $\hat{x}_d[n]$ and $\hat{x}_f[n]$. The use of double-update DPWM will reduce m by a half, as half of counts of the DPWM counter, N, are needed to obtain the same switching frequency f_s. In [17,20], a small-signal laplace-domain transfer function of this type of modulation has been derived, whose mathematical expression is shown in (26).

$$G_{DPWM}(s) = e^{-sDT_s} \qquad (26)$$

From (26) it is possible to affirm that single-update DPWM adds a delay which depends on the sampling rate T_s as well as on the duty cycle D. Taking into account (26), Fig. 9 could be modified as depicted in Fig. 13, where the delays in each of the channels are expressed by (27) and (28).

$$G_{DPWMf}(s) = e^{-sD_f T_s} \qquad (27)$$

$$G_{DPWMd}(s) = e^{-sD_d T_s} \qquad (28)$$

Assuming that injected perturbation is much lower than the steady-state signals, so that the operation point remains unchanged, it is possible to affirm that the duty-cycle depends exclusively on $\bar{X}_d[n]$ and $\bar{X}_f[n]$, hence from (22) it is possible to derive (29).
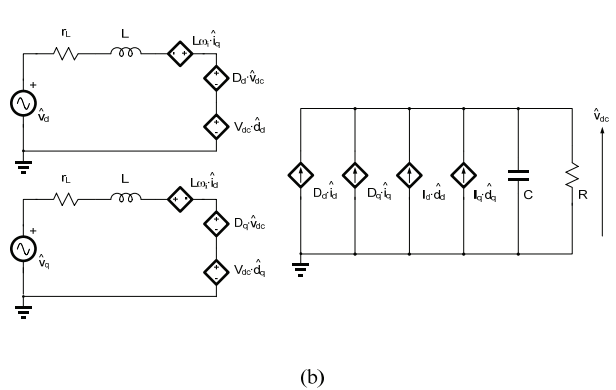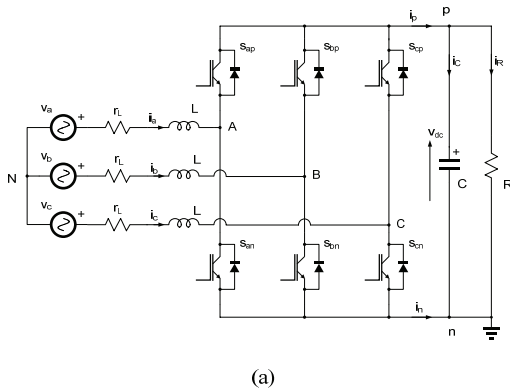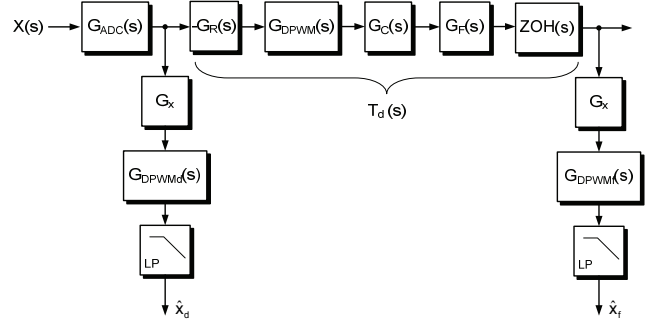
$$D_d = D_f = D \qquad (29)$$

Fig. 13. Disturbed closed loop small signal equivalent block diagram with DPWM laplace model of the measured variables.

Therefore (27) and (28) could be expressed by (30).

$$G_{DPWMf}(s) = G_{DPWMd}(s) = e^{-sDT_s} \qquad (30)$$

By applying the analog modulation scheme at Fig. 13, the analytical expression (31) can be derived to obtain $T_d(s)$.

$$-\frac{\hat{x}_f}{\hat{x}_d} = \frac{X(s) \cdot G_{ADC}(s) \cdot G_x \cdot LP(s) \cdot e^{-sDT_s} \cdot T_d(s)}{X(s) \cdot G_{ADC}(s) \cdot G_x \cdot LP(s) \cdot e^{-sDT_s}} = T_d(s) \quad (31)$$

It is quite obvious that assuming (29) and taking into account that the low-pass filter and G_x are the same in both channels, the DPWM doesn't modify the measurement of the gain loop frequency response.

IV. MEASUREMENT OF THE DIGITAL CURRENT CONTROL LOOP GAINS OF A THREE-PHASE VOLTAGE SOURCE RECTIFIER

In order to test the proposed measurement method, a 10 kW three-phase voltage source rectifier (VSR) has been designed and implemented. In the next sections, the modeling and digital control of the VSR, along with the measurement scheme of the several loop gains are presented.

A. Modeling and Digital Control of the three-phase VSR

In Fig. 14 (a) it is depicted the power stage of a conventional three-phase VSR with resistive load, where a first order grid filter (L), a three-phase IGBT bridge and a DC-link (C), along with a load (R) are shown. Besides, the parasitic resistance of the inductor, r_L, has been taken into

(a)

(b)

Fig. 14 (a) Power stage of the three-phase VSR and (b) Electrical small-signal equivalent model of the three-phase VSR

Fig. 16. Synchronous Reference Frame PLL small-signal closed loop control block diagram

account. The electrical small-signal model of the power converter in a synchronous reference frame depicted in Fig. 14(b) can be derived from Fig. 14(a) [23,27]. This model is widely used for the linear control of the power converter [15,28,29] due to several advantages which include:

- The operation point variables are DC magnitudes.
- It is theoretically possible to obtain infinite gain at the grid frequency by using conventional proportional-integral (PI) controllers.
- Active and reactive power control can be carried out by means of the control of the projected *abc* variables into the *d* and *q* axis.

In order to control the dc-link voltage of the VSR, V_{dc}, as well as the *d* and *q* projections of the grid currents i_a, i_b and i_c (i_d and i_q respectively), the closed loop control scheme shown in Fig. 15 is usually performed [22], where conventional PI controllers are used. It is worth pointing out that the transfer functions $\hat{i}_d(s)/\hat{d}_d(s)$, $\hat{i}_q(s)/\hat{d}_q(s)$ and $\hat{v}_{dc}(s)/\hat{i}_d(s)$ model the small-signal VSR behavior, and that they could be obtained from the electrical small signal model shown in Fig. 14(b); besides, the term K_d is included to decouple space state variables $\hat{i}_d$ and $\hat{i}_q$ modulator dynamic behavior. The study of the loop gains frequency response of the voltage loop (T_{vdc}), the current loop in the *d* channel (T_{id}), and the current loop in the *q* channel (T_{iq}), allows the designer to know about the stability of the VSR as well as the bandwidth for each of the control loops, so that the PI controllers can be adjusted by means of analytical methods. The proposed measurement method can be used to validate the designed controllers by means of the measured loop gains frequency response.

In order to properly synchronize the VSR with the grid frequency, a Synchronous Reference Frame PLL (SRF-PLL) [30,31] has been used. Fig. 16 shows the small-signal model of the SRF-PLL, where a PI controller, PI_{PLL}, has been used. The correct design of this controller allows making the SRF-PLL stable as well as obtaining the desired bandwidth for the system.
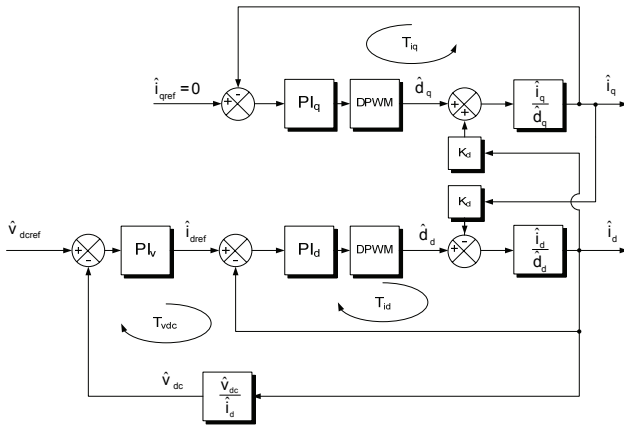
By applying the aforementioned method for the design of the PI controller, the loop gain frequency response, T_{PLL}, can be studied. The proposed measurement method could be used as a final step in the design process, so that experimental results are obtained to validate analytical results.

B. Measurement of the Loop Gains

In order to measure the loop gains frequency response T_{vdc}, T_{id}, T_{iq} and T_{PLL} by applying the measurement method described in this paper, the scheme presented in Fig. 6 has to be implemented in each of the loops to be measured. Fig. 17 shows the correct connection of the FRA to carry out the loop gain frequency response analysis of T_{id}, where anti-aliasing filters as well as level shifter stage and decoupling terms have been omitted in the scheme to make the presentation simpler; however, these stages should be included in the measurement process, as stated thereinafter.

For the measurement of the other loop gains to be made, a similar arrangement should be applied for each of the control loops, taking into account the important issues presented in section III. The measured loops gains should agree with the analytical expressions shown in (32), (33), (34) and (35). It is worth pointing out that for (32) to be true, the control loop bandwidth of the variable $\hat{i}_d$ has to be wider than that for the

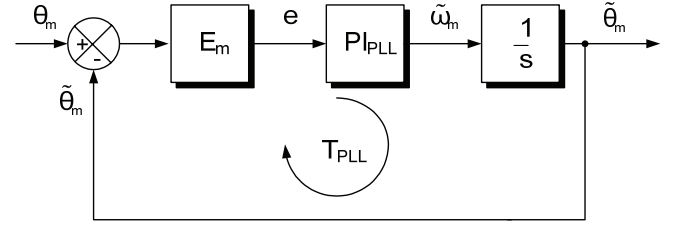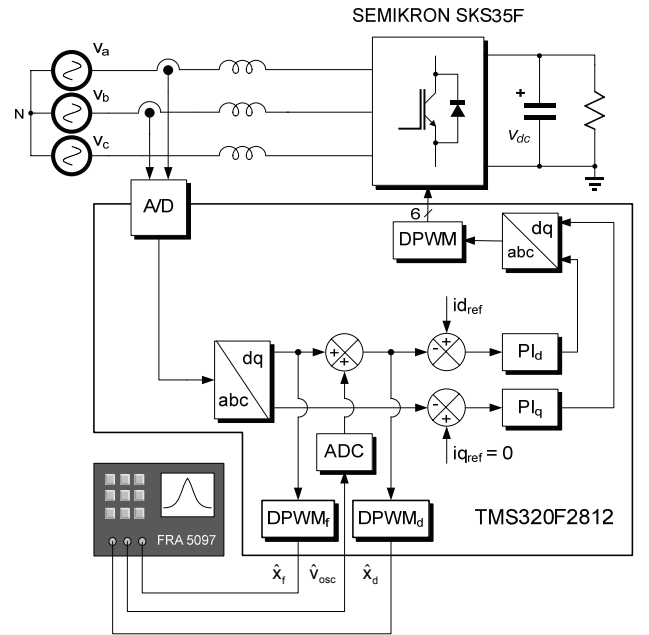Fig. 15. Closed loop control block diagram of $\hat{v}_{dc}$, $\hat{i}_d$ and $\hat{i}_q$ with decoupling term K_d.

Fig. 17. Measurement of the loop gain T_{id}.

variable $\hat{v}_{dc}$, which in turn is a design constraint that has to be taken into account in the controller design [22].

$$T_{Vdc} = PI_V \cdot \frac{\hat{v}_{dc}}{\hat{i}_d} \tag{32}$$

$$T_{id} = PI_d \cdot DPWM \cdot \frac{\hat{i}_d}{\hat{d}_d} \tag{33}$$

$$T_{iq} = PI_q \cdot DPWM \cdot \frac{\hat{i}_q}{\hat{d}_q} \tag{34}$$

$$T_{PLL} = E_m \cdot PI_{PLL} \cdot \frac{1}{s} \tag{35}$$

The additional resources needed to measure the open loop gain are a single ADC channel and a PWM port, usually included in the DSP. In addition, the original control software has to be modified by adding three multipliers and three adders. It should be noted that, for typical applications, the overhead of the original control software and hardware could be considered negligible. In Fig. 18 it is depicted a simplified version of the modified control software of the DC-link voltage, $\hat{v}_{dc}$, where the additional code needed to measure the open loop gain T_{vdc} has been written in bold. Note that only five additional lines of code have been added.

```
// Read from ADC channels
vab=ADC_CHANNEL1;
vbc=ADC_CHANNEL2;
ia=ADC_CHANNEL3;
ib=ADC_CHANNEL4;
vdc=ADC_CHANNEL5;

// Added code. Read ac disturbance.
Vosc=ADC_CHANNEL6

// Additional code. Write duty cicle for scaled
// feedback and disturbed signals in DSP registers.
xf=vdc;
xd=vdc+Gac*Vosc;
PWMd=Gx*xf+N/2;
PWMf=Gx*xd+N/2;

// COMPUTE dq control
dq_control(vab, vbc, ia, ib, xd);

// Write duty cicle for each power converter leg in
// DSP registers
PWM1=PWM1_controller;
PWM2=PWM2_controller;
PWM3=PWM3_controller;
```

Fig. 18. Modified control software of the power converter.

TABLE I
PARAMETERS OF THE THREE-PHASE VSR UNDER STUDY

Parameter	Nominal value
Va_{RMS}, Vb_{RMS}, Vc_{RMS}	230 V phase to neutral
Vdc	750 V
L	10 mH
r_L	1 mΩ
C	2.04 mF
f_{PWM}	5 kHz
fs	10 kHz
R	75 Ω

TABLE II
T_{ID} MEASUREMENT PARAMETERS

Parameter	Nominal value
$Gosc$	1
$Vosc(peak)$	1.2 V
FSR	3 V
n	12 bits
Ne	12 bits
Gac	0.005291
Ts	100 μs
$Tclk$	6.67 ns
N	15000
D_{MAX}	0.8
m	14 bits
Me	14 bits
Gx	12000

V. EXPERIMENTAL RESULTS

A 10 kW three-phase VSR prototype has been implemented by taking into account the measurement system described in section IV. The power stage consists of a SEMIKRON SKS 35F IGBT power module, digitally controlled by means of a Texas Instruments DSP TMS320F2812. The measurement has been carried out by means of the FRA NF Corp. FRA5097.

Table I shows the parameters of the three-phase VSR and in Table II it is depicted the parameters used for the measurement of the loop gain T_{id}.

Fig. 19 to Fig. 22 show a comparison between analytical (solid line) and experimental (dotted line) loop gain frequency response of T_{vdc}, T_{id}, T_{iq} and T_{PLL} respectively, from which it is possible to conclude that the measured loop gains agree with the analytical results, mainly in the crossover region.

It should be noted that the measured open loop gain frequency response differs from the analytical one in the high-frequency range, mainly due to imperfections in the small-signal model of the electronic power converter. Nevertheless, it agrees with the analytical one in the frequency range of interest, i.e. in the crossover frequency region, which in turn allows the designer to know about the actual phase and gain margin of the loop gain.

VI. CONCLUSIONS

A method to measure the loop gains frequency response of digitally controlled power converters by means of a
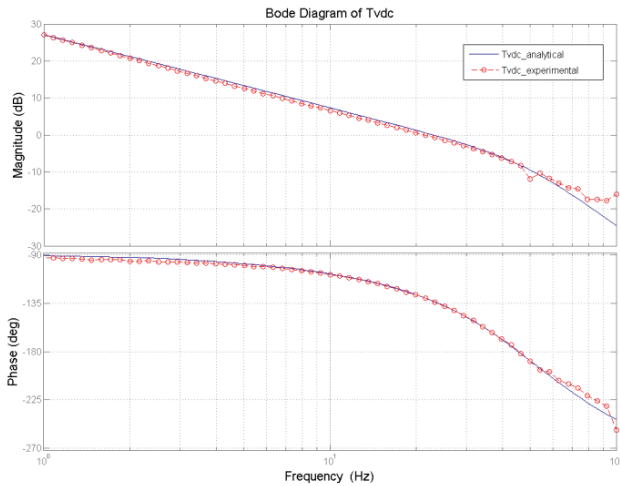
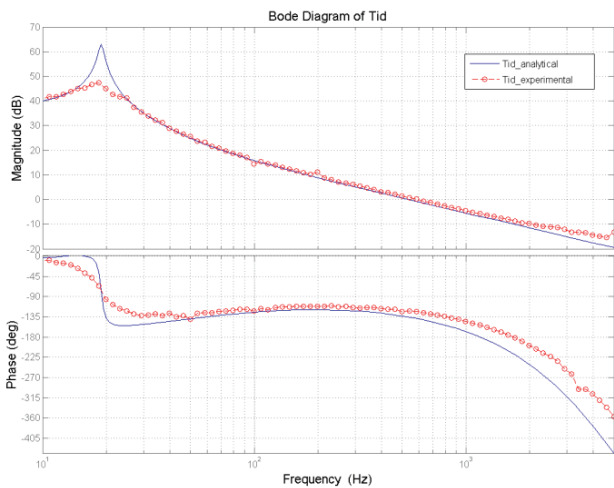Fig. 19. Analytical (solid) and experimental (dotted) loop gain frequency response of T_{vdc}.

Fig. 20. Analytical (solid) and experimental (dotted) loop gain frequency response of T_{id}.
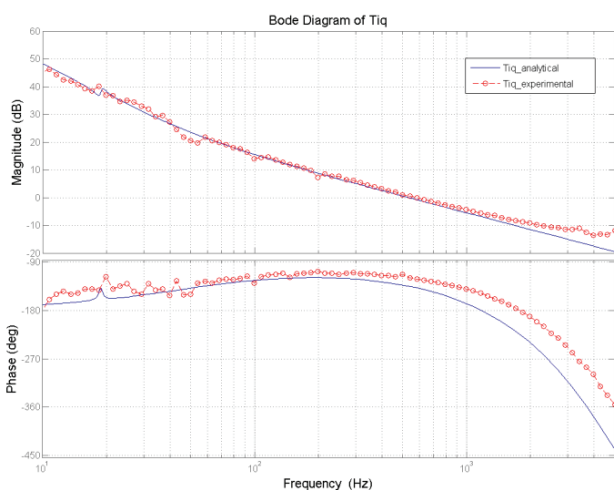

Fig. 21. Analytical (solid) and experimental (dotted) loop gain frequency response of T_{iq}.
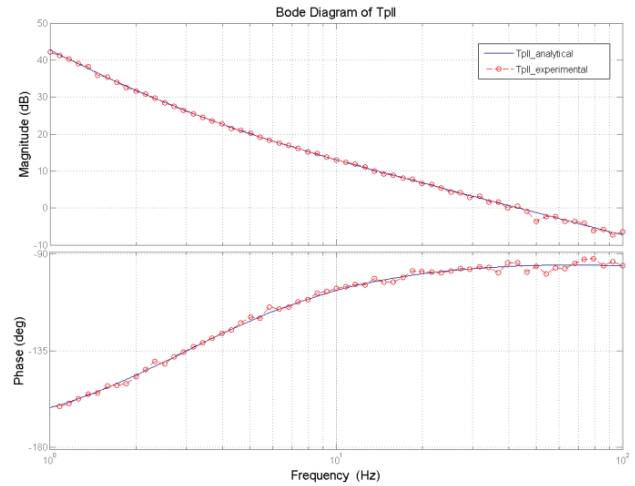

Fig. 22. Analytical (solid) and experimental (dotted) loop gain frequency response of T_{pll}.

conventional FRA has been proposed. The method is based on the analog modulation scheme, and uses the common resources offered by the DSP, as DPWM peripherals and integrated ADCs, to disturb the closed loop in order to obtain the loop gain frequency response.

The study of the method has shown that the measured loop gain is not affected by the measurement process if some design constraints are taken into account. Besides, limit-cycle oscillation phenomena due to the resolution of the DPWM and the ADC can be avoided by properly selecting the resolution of both stages.

The proposed measurement method can be used in both simple and more complex electronic power converters to measure not only the loop gain frequency response but any other transfer functions of interest. Besides, the method described in this paper allows to measure loop gains that use intermediate variables that are a mathematical combination of physical variables.

The experimental results carried out by means of an FRA NF Corp. FRA5097 and a 10 kW VSR controlled by a Texas Instruments DSP TMS320F2812, have shown that the measured loop gain frequency response agrees with the analytical one, mainly in the crossover region and in the low frequency range, where the small-signal model of the converter is more accurate.

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