UNIVERSITY OF ZAGREB

FACULTY OF ELECTRICAL ENGINEERING AND COMPUTING

MASTER THESIS no. 1755

IMPACT OF THE CIRCUIT PARAMETERS ON THE ELECTROMAGNETIC COMPATIBILITY OF A RESONANT SWITCHED-MODE POWER CONVERTER

Alejandro Cerro Martínez

Zagreb, July 2018.

Contents

1. Introduction 3
2. Electromagnetic compatibility 4
2.1. Radiated Emissions 5
2.2. Conduced emissions 7
3. Design of Printed Circuit Boards 9
3.1. Schematic Design 10
3.2. Circuit Parameters 11
3.3. Simulations 13
3.4. Board Design 22
4. Measurements 25
4.1. Validation 25
4.2. Radiated Emissions 34
4.3. Conducted Emissions 47
5. Conclusion 51
References 52
Abstract 53
Sažetak 54

1. Introduction

The power converters are divided into two groups, switched mode power converters and linear converters. The advantages of linear converters are the simplicity, low cost and the low generation of electromagnetic interference, while the main disadvantage of these kind of converters is low efficiency [1].

Switched mode converters have a wide range of applications. Their principal advantage is they can have efficiency higher than 90% [1]. Switching mode convertors dissipate energy only in the switching transistor and this quantity of energy is low, so heat sinks are not needed. Due to these facts, the dimensions and weight of the boards are lower. However, the main disadvantage of this kind of converters is that they produce a level of electromagnetic noise which can be higher than the limits established by the different committees like CISPR (International Special Committee on Radio Interference). Furthermore, switched mode converters show a slow response to load changes and they have a high complexity.

One type of switched mode converters is the resonant switched mode converter. The main advantage of this converter is that it can work at a frequency between 10 to 100 times higher than a pulse-width modulated (PWM) switched mode converter. This allows obtaining faster changes of the output with load. Moreover, the passive components can be smaller which allows to use a higher frequency and for this reason, the price and dimensions of the board are reduced.

In this thesis, resonant switched mode converters and the impact of their circuit parameters on the electromagnetic compatibility are studied. In Section 2 the electromagnetic compatibility is described, Section 3 analyses the four designed boards, their efficiency and their time domain waveforms, the Section 4 describes the validation of all four printed circuit boards, and it shows the measurements of the radiated and conducted emissions. Finally, conclusion about the electromagnetic compatibility of the boards is given.

2. Electromagnetic compatibility

Electromagnetic compatibility (EMC) is the field of electrical engineering that studies the generation, propagation and reception of electromagnetic energy. The goal of EMC is the correct operation of different equipment in a common electromagnetic environment [2].

EMC is based on three parameters. The emission, which is generated by some source and released into the environment. The susceptibility of the device to malfunction or break down in the presence of these emissions, which are known as Radio Frequency Interference (RFI). Finally the coupling, which is the mechanism by which emitted interference reaches the victim.

The requirements of EMC are imposed by governmental agencies. The requirements are mandatory and they must not be ignored or discarded. These constraints ensure reducing the disturbances due to the device, i.e. reducing the electromagnetic contamination. Moreover, all devices must comply with these regulations to be put on the market, independently of its operation.

Some committees carry out the studies about electromagnetic compatibility such as CISPR (International Special Committee on Radio Interferences), FCC (Federal Communications Commission) and BSI (British Standards Institution). The majority of European countries have accepted the regulations of CISPR in relation to electromagnetic compatibility. In fact, standard CISPR 22 says that there are two classes of devices, class A and class B. Class A is about devices for commercial purposes and industry, while class B is related to devices intended for home. Class B devices have more strict restrictions than class A because disturbances in the industrial environment are easier reduced than those in a household where the source of disturbance and the sensitive device are close to each other.

EMC limits required by CISPR 22 are about two types of emissions; radiated emissions and conduced emissions.

2.1. Radiated Emissions

Radiated emissions refer to the electric and magnetic fields, which are emitted by the device and which can be received by other devices, which causes interference. The frequency range of radiated emissions is between 30 MHz and 1 GHz [2]. The measurement of the irradiated electric fields created by the device is carried out by means of measurement aids placed in vertical and horizontal position. According to CISPR 22, the emission standard is measured at a distance of 10 meters for Class A and Class B devices [2]. The emission limits for Class B, according to the CISPR standard, are given in Table 2. The analysed converters are included in class B. The visualization of limits according to CISPR 22 is shown in Figure 1.

Frequency [MHz]	μV/m	dBμV/m
30-230	31.6	40
230-1000	70.8	47

Table 1 Limit emissions class B devices [2].

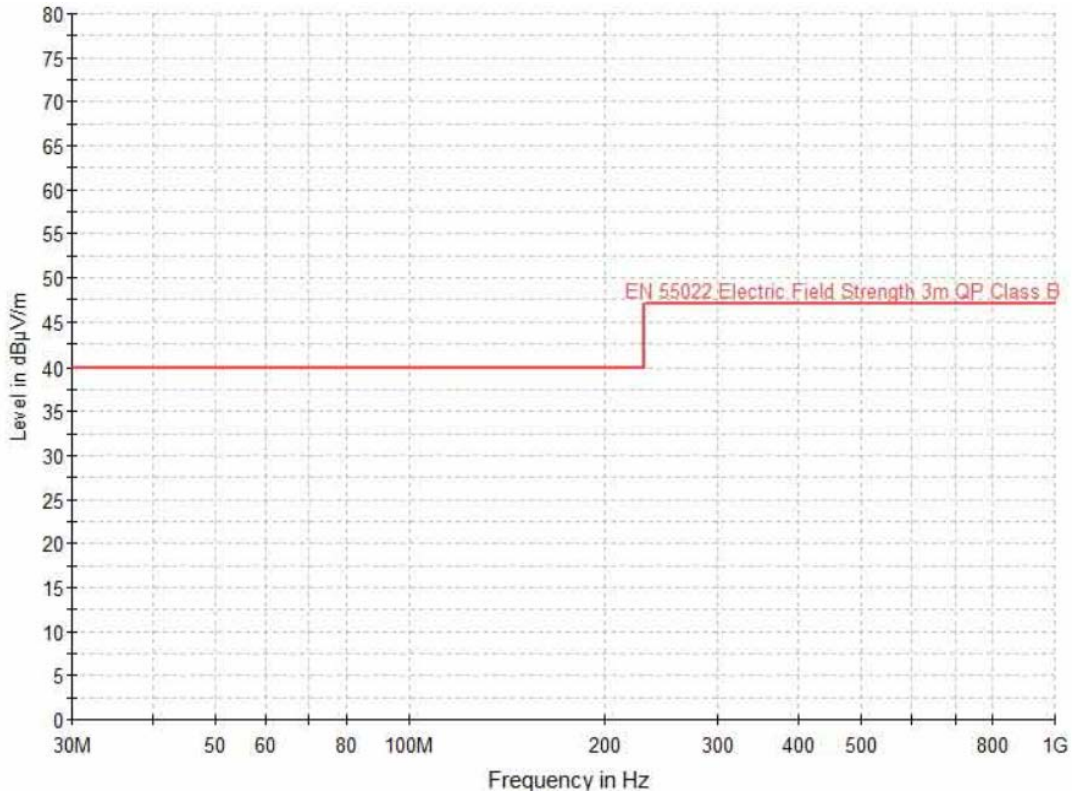


Figure 1 Visualization of limits class B devices according to CISPR 22 [2].

To do the measurements of radiated emissions an anechoic chamber is used with the objective to isolate the other electromagnetic disturbances like environment disturbances, which can affect the measurements. Figure 2 shows the set up of an anechoic chamber.

Alternatively, the measurements can be done in a TEM (Transverse electromagnetic) cell. It has the same function as an anechoic chamber, stabilise the electromagnetic fields in a closed space but it is simpler and cheaper than an anechoic chamber. The figure 3 shows a TEM cell.

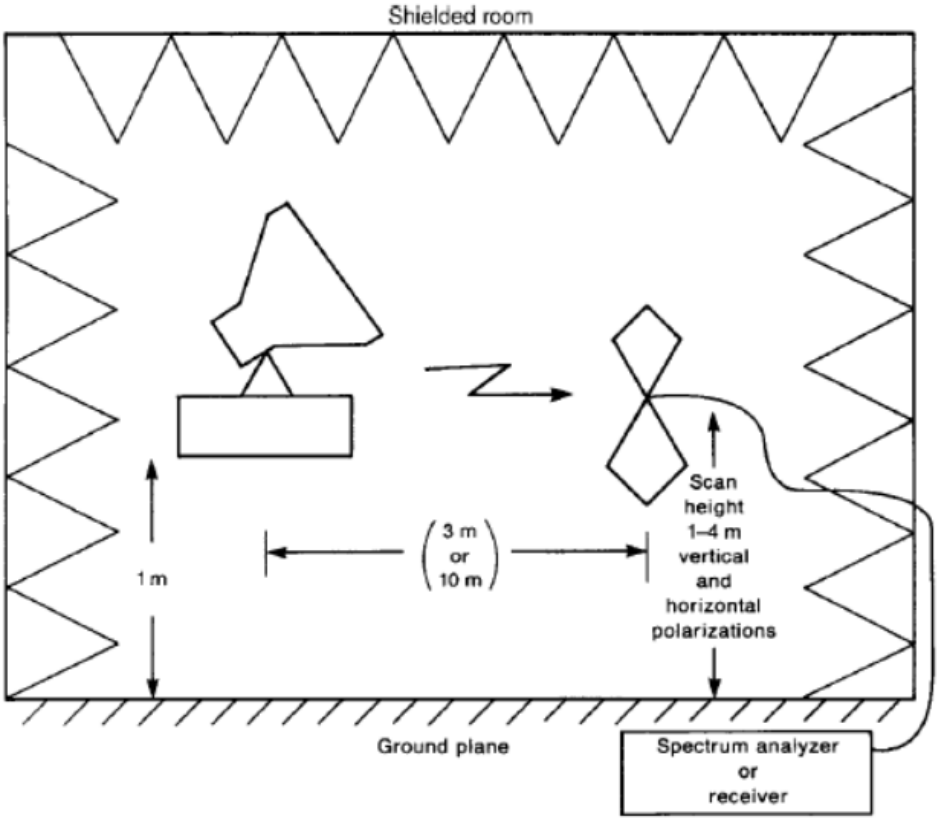


Figure 2 Measurement of radiated emissions in anechoic chamber [2].

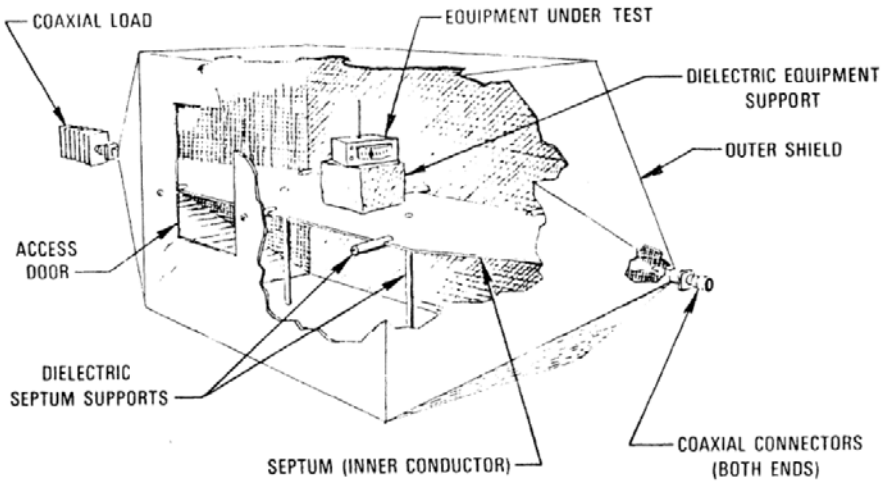


Figure 3 TEM cell [3].

2.2. Conduced emissions

Conduced emissions are currents that pass through the power supply, signal or ground wires. Theses currents have a range of frequencies between 150 kHz and 30 MHz and it causes interferences in the devices [2]. The measurements of these emissions is done with a LISN (Lime Impedance Stabilization Network) connected between the device under test and the power supply system. The perturbation limits for class B are shown in the table 2.

Frequency [MHz]	µV QP (AV)	dBµV QP (AV)
0,15	1995 (631)	66 (56)
0,5	631 (199.5)	56 (46)
0.5-5	631 (199.5)	56 (46)
5-30	1000 (316)	60 (50)

Table 2 Perturbation limit to class B [2].

The LISN network has two proposes: first, to avoid the external interferences in the measurement and ensure that only the device interferences are measured and the second reason is to get the same impedance to the measurement output through all frequency bands. The LISN includes two capacitors to reduce the external noise and avoid the continuous current. Moreover, the function of the inductor of 50 uH is to reduce this noise. Finally, resistors are used to discharge the capacitors when these are not connected to an external load [2].

Figure 3 shown a LISN of 50 uH.

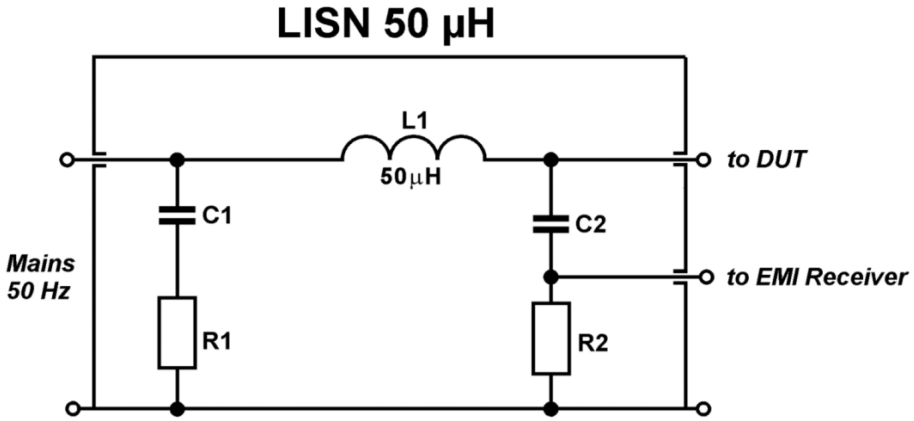


Figure 4 LISN 50 uH [2].

3. Design of Printed Circuit Boards

This section describes how to design the schematic, board, considerations taken into account to improve the EMC and the components for the design of resonant class E DC-DC converter.

The thesis is based on the study of a resonant class E converter. This kind of converters is interesting to study because they can work at higher frequencies and with this characteristic the dimensions and components are smaller. Figure 5 shows a typical isolated class E dc-dc converter [4].

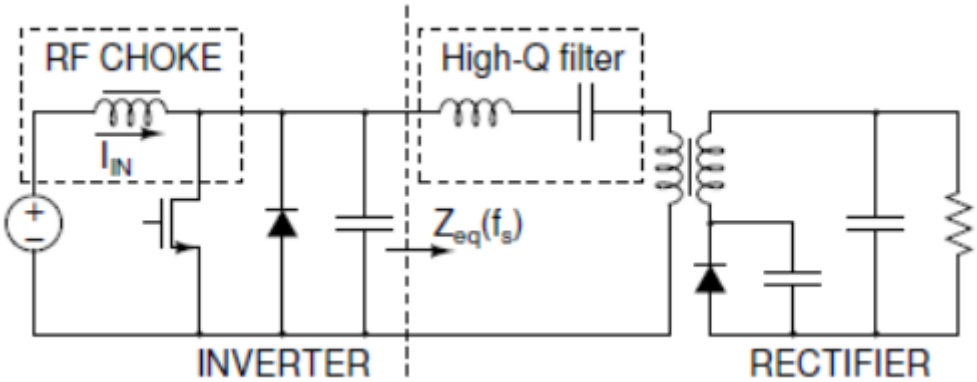


Figure 5 Typical class E dc-dc converter [4].

A class E DC-DC converter is based on two fundamental building blocks, a class- E inverter, and a rectifying stage, connected together by an LC filter. The inverter stage is a class E amplifier working at frequency f_s, and loaded with a non-resistive network design to properly shape the voltage across the transistor and to achieve optimal operation. The resonant rectifier makes the final ac/dc conversion [4].

The schematic of the converter considerer in this thesis is shown in Figure 6. It is a non-isolated topology of a resonant class E dc-dc converter. The circuit can be separated into an inverter and a rectifier stage, connected together by paring inductance L_{pair}. The input and output voltage is denoted by V_{in} and V_{out}. Finally, the current through the load is $I_{out} = V_{out}/ R_{load}$.

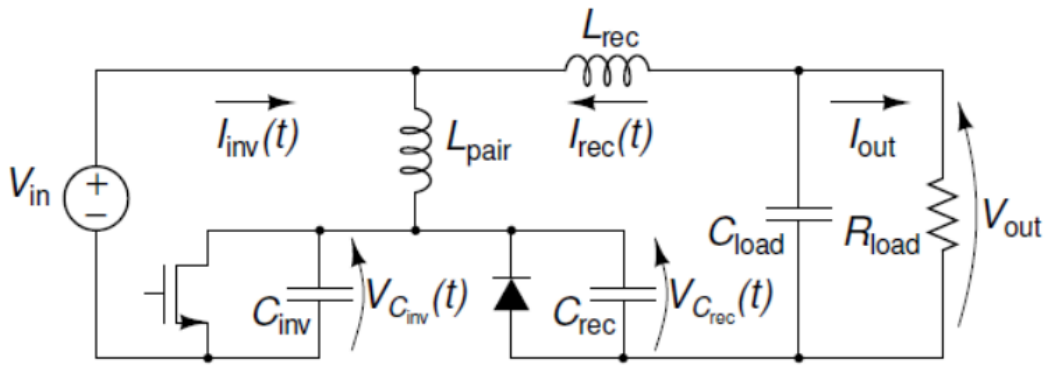


Figure 6 Non-isolated topology [4].

Four boards are designed to study the impact of the circuit parameters on the electromagnetic compatibility. All four converters convert the input voltage of 12 V into the output voltage of 5 V, at the output current 1 A and at the switching frequency of 1 MHz. The duty cycles is the only difference between the boards, it is 30% for the first one, 40% for the second, 50% for the third and 60% the fourth. These changes in the duty cycle lead to the difference in the circuit parameters and in the generated electromagnetic emissions.

3.1. Schematic Design

The circuit is designed by taking into account the “proposed circuit description” and “nonidealities modelling” of [4].

The capacitor C3 is added to reduce the impedance and noise, just as in the output part with the capacitor C8 (Figure 7). This capacitor reduces the output voltage ripple. In the inverter part, a driver is added to assure that the PWM controls the N-MOSFET. It should be noted that the inductor L1 has been put in the inverter side to get a symmetry of the design. It is not used and it is replaced by 0-Ohm resistor. At last, the connector is added to the board to provide the input, output and PWM signals.

The values of the inductors, inverter and rectifier capacitors are obtained by the mathematical formulations described in [4].

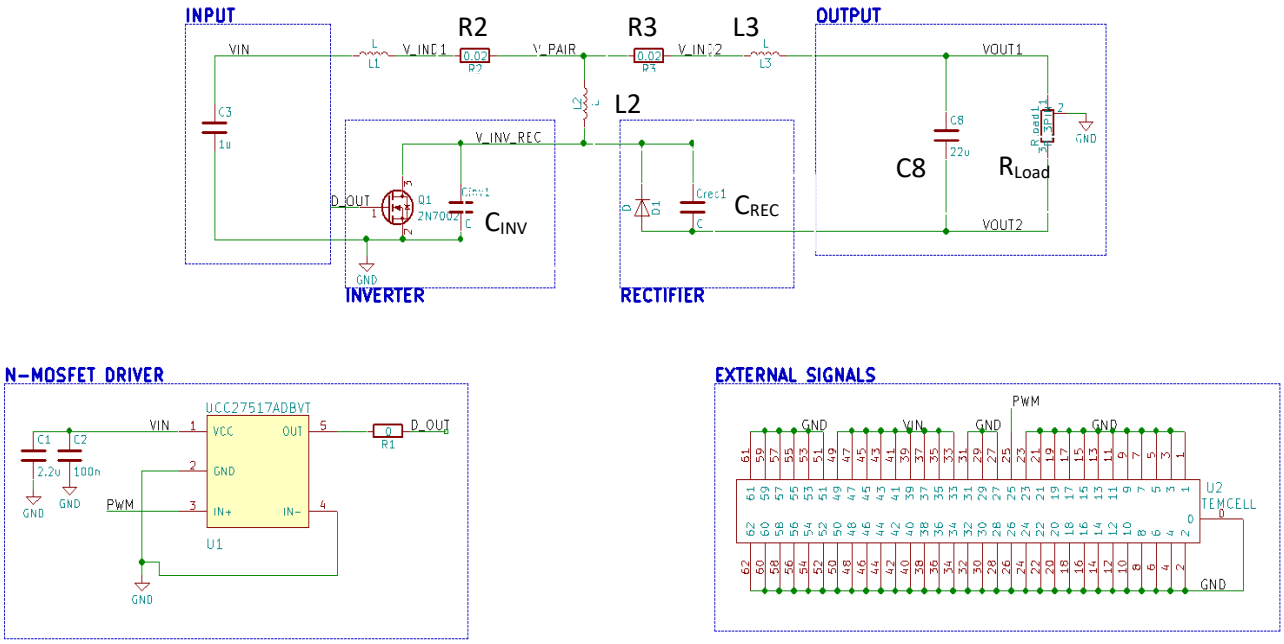


Figure 7 Schematic design.

3.2. Circuit Parameters

To finish the schematic design it is needed to calculate the parameters for each board. To do this, the equations that appear in the “appendix” of [4] have to be solved. These equations have been modelled in Matlab.

The following values have been obtained by the equations:

Duty Cycle	L1	L2	L3	C_{inv}	C_{rec}
30%	0 H	2.79 µH	2.79 µH	15.42 nF	6.55 nF
40%	0 H	2.93 µH	2.93 µH	11.82 nF	4.40 nF
50%	0 H	2.80 µH	2.80 µH	10.90 nF	5.03 nF
60%	0 H	3.06 µH	3.06 µH	7.03 nF	2.80 nF

Table 3 Circuit Parameters.

The majority of values will be difficult to find due to the non-standard values. In the presence of this issue, the values are standardized. This fact modifies the optimal operation, therefore it has to be analysed in the simulations to prove that the boards have a similar performance.

According to the standardized components, the requirements of the circuit and trying to reduce the costs, the new values are:

Duty Cycle	L1	L2	L3	C_{inv}	C_{rec}
30%	0 H	2.70 µH	2.70 µH	15.47 nF	6.60 nF
40%	0 H	3.00 µH	3.00 µH	11.00 nF	5.00 nF
50%	0 H	2.70 µH	2.70 µH	11.00 nF	4.70 nF
60%	0 H	3.00 µH	3.00 µH	6.80 nF	2.80 nF

Table 4 Standard circuit parameters.

The other selected components are given in Table 5, which shows the Bill of Materials developed for these boards.

Designator	Description	Case Style
C3, C6	SMD Multilayer Ceramic Capacitor, 0805 [2012 Metric], 1 µF, 25 V, ± 10%, X7R	0805
C4, C5, C7	SMD Multilayer Ceramic Capacitor, 0805 [2012 Metric], 10 µF, 25 V, ± 10%, X5R	1206
C8	SMD Multilayer Ceramic Capacitor, 0805 [2012 Metric], 22 µF, 25 V, ± 20%, X5R	1205
C2	SMD Multilayer Ceramic Capacitor, General Purpose, 0603 [1608 Metric], 0.15 µF, 25 V, ± 10%, X7R	0603
C1	SMD Multilayer Ceramic Capacitor, 0603 [1608 Metric], 2.2 µF, 25 V, ± 10%, X5R	0603
L2A, L3A	Power Inductor (SMD), 2.7 µH, 4 A, Shielded, 2.2 A, SRR4828A Series, 4.8mm x 4.8mm x 2.8mm	Inductor_custom
L2B, L3B	Power Inductor (SMD), 3 µH, 8 A, Shielded, 2.2 A, XFL4030 Series, 4mm x 4mm x 3.1mm	Inductor_custom
L1	SMD Chip Resistor, 0 ohm, RC Series, 200 V, Thick Film, 2010 [5025 Metric], 750 mW	2010
R2, R3	SMD Current Sense Resistor, 0.02 ohm, TLM Series, 1206 [3216 Metric], 500 mW, ± 1%	1206
R1	SMD Chip Resistor, 3.3 kohm, RC Series, 75 V, Thick Film, 0603 [1608 Metric], 100 mW	0603
Rload1	SMD Chip Resistor, 5 ohm, PWR163 Series, 250 V, Thick Film, TO-252 (DPAK), 25 W	DPACK
Q1	MOSFET Transistor, N Channel, 3.1 A, 100 V, 0.102 ohm, 10 V, 3 V	SOT-23
D1	Schottky Rectifier, 100 V, 3 A, Single, SOD-128FL, 2 Pins, 840 mV	SOD-128FL
Cinv1A	SMD Multilayer Ceramic Capacitor, AEC-	0603

	Q200, 0603 [1608 Metric], 0.015 µF, 100 V, ± 10%, X7R	
Cinv1B	SMD Multilayer Ceramic Capacitor, 0603 [1608 Metric], 470 pF, 100 V, ± 5%, X7R	0603
Crec1B	SMD Multilayer Ceramic Capacitor, 0603 [1608 Metric], 5600 pF, 100 V, ± 10%, X7R	0603
Cinv2A, Cinv3A	SMD Multilayer Ceramic Capacitor, 0603 [1608 Metric], 0.01 µF, 100 V, ± 5%, X7R	0603
Crec2B	SMD Multilayer Ceramic Capacitor, 0603 [1608 Metric], 330 pF, 100 V, ± 10%, X7R	0603
Cinv3B, Crec4A, Crec1A, Cinv2B	SMD Multilayer Ceramic Capacitor, 0603 [1608 Metric], 1000 pF, 100 V, ± 5%, X7R	0603
Cinv4A	SMD Multilayer Ceramic Capacitor, 0603 [1608 Metric], 2200 pF, 100 V, ± 5%, X7R	0603
Cinv4B, Crec3A, Crec2A	SMD Multilayer Ceramic Capacitor, 0603 [1608 Metric], 4700 pF, 100 V, ± 5%, X7R	0603
Crec4B	SMD Multilayer Ceramic Capacitor, 0603 [1608 Metric], 1800 pF, 100 V, ± 5%, X7R	0603
U1	IGBT/MOSFET IC, Low Side, 4.5V-18V Supply, 4A Out, 13ns Delay, SOT-23-5	SOT 23-5

Table 5 Bill of Materials.

3.3. Simulations

Using the values obtained by the equations mentioned before, the circuit is implemented in LTspice tool to simulate how it works. Each board has been simulated with the ideal and optimized values and the results are plotted.

Simulation for duty cycle 30%

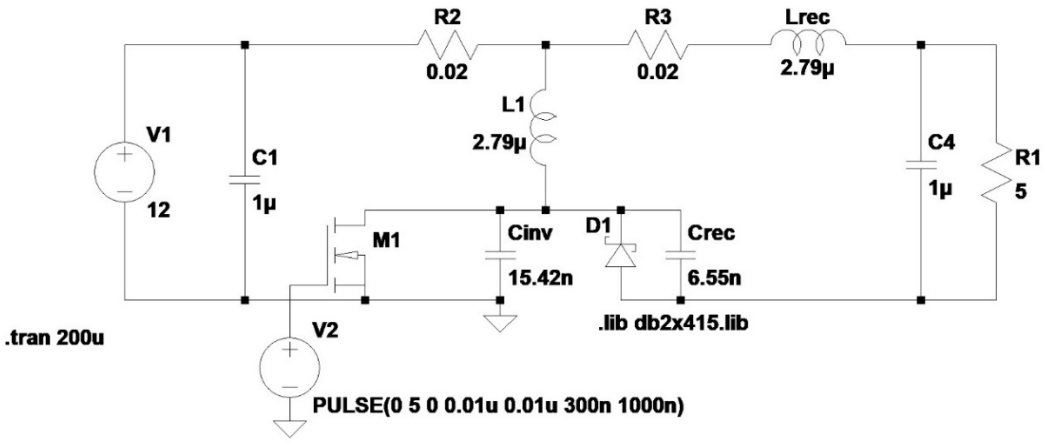


Figure 8 Schematic for a duty cycle of 30%.

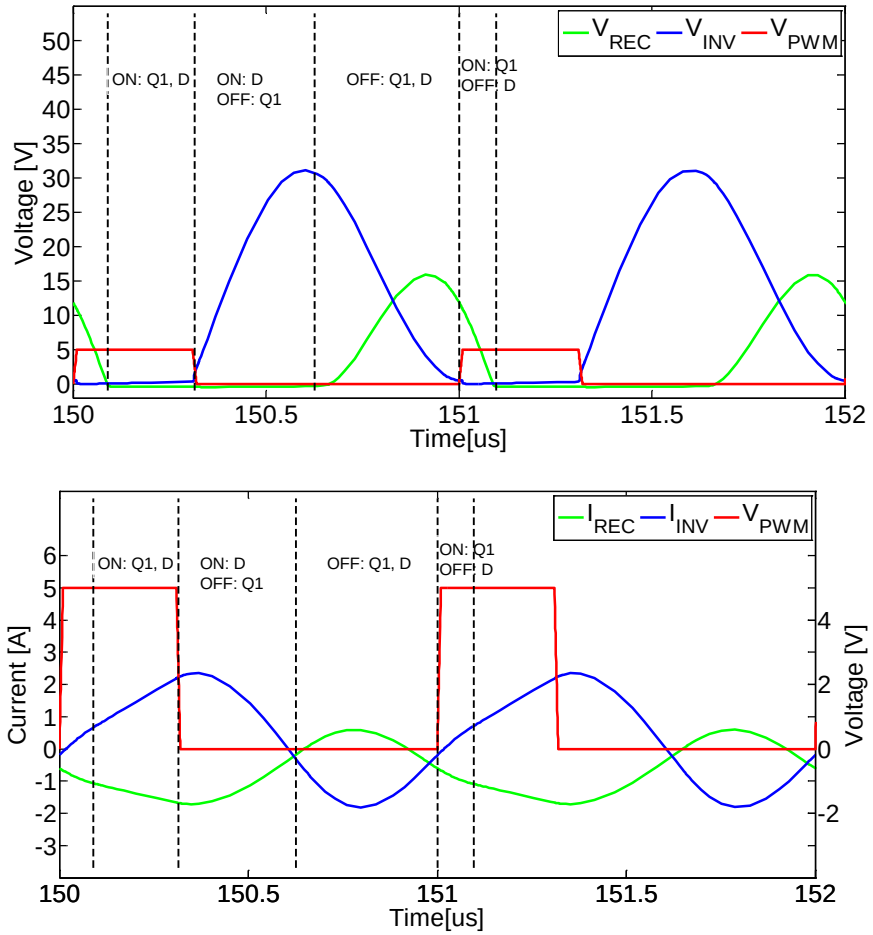


Figure 9 Simulation for a 30% duty cycle.

After simulating the ideal values, the schematic is analysed according to the values of Table 5.

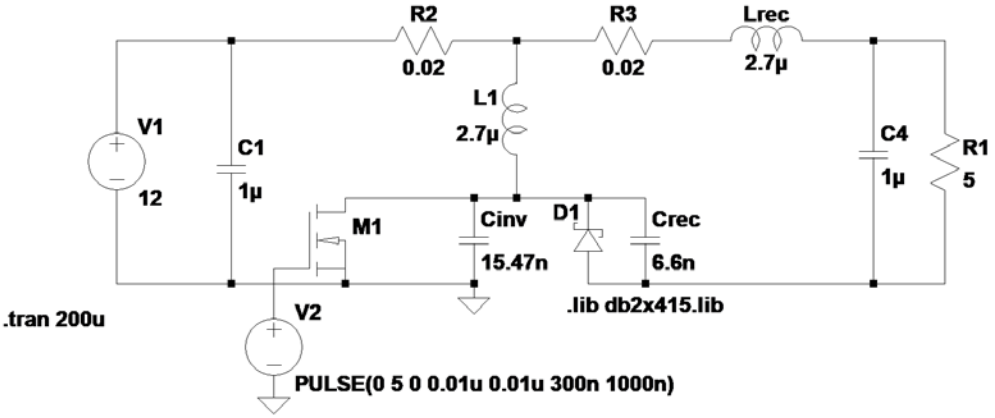


Figure 10 Schematic for a duty cycle of 30% with standard components.

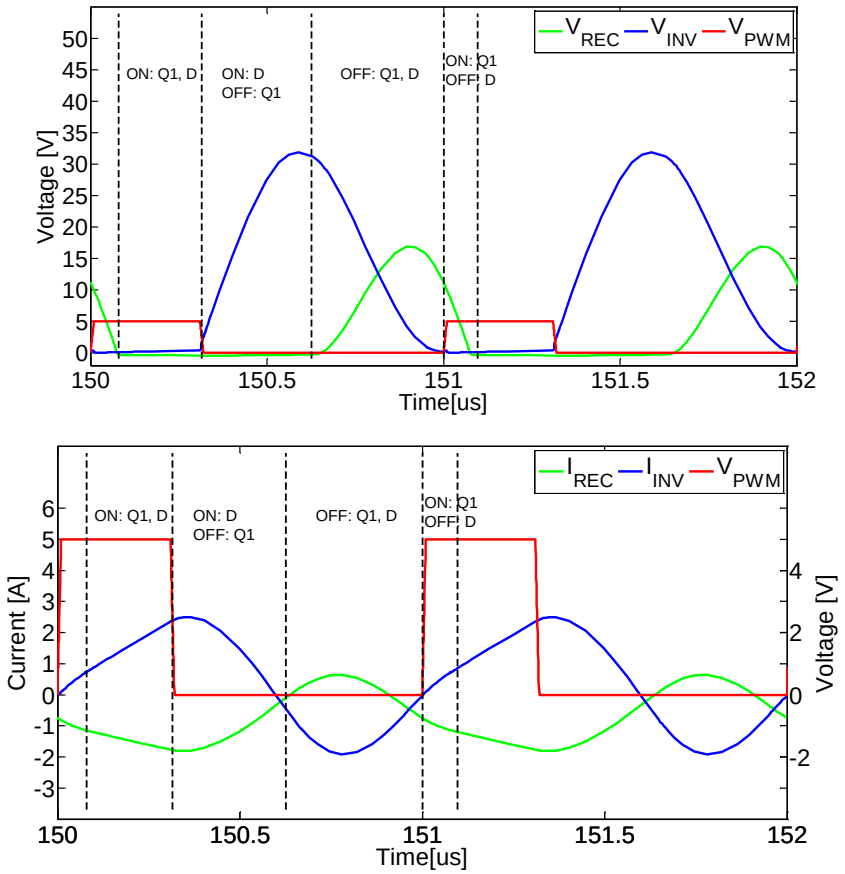


Figure 11 Simulation for a 30% duty cycle with standard components.

Simulation for duty cycle 40%

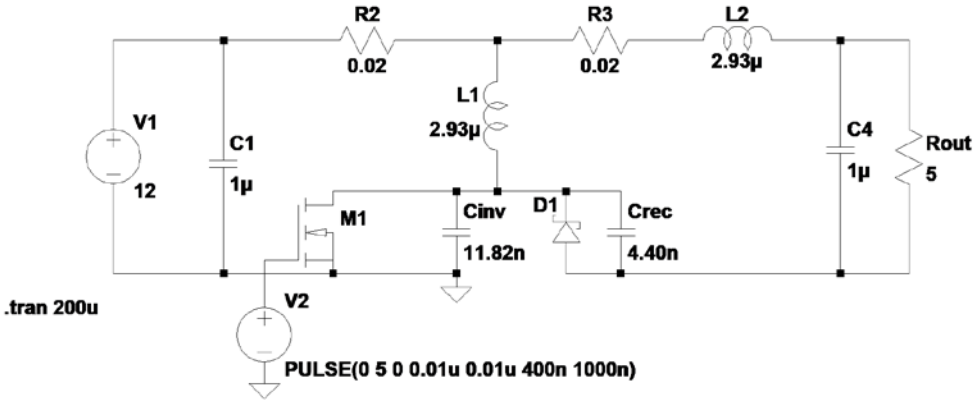


Figure 12 Schematic for a duty cycle of 40%.

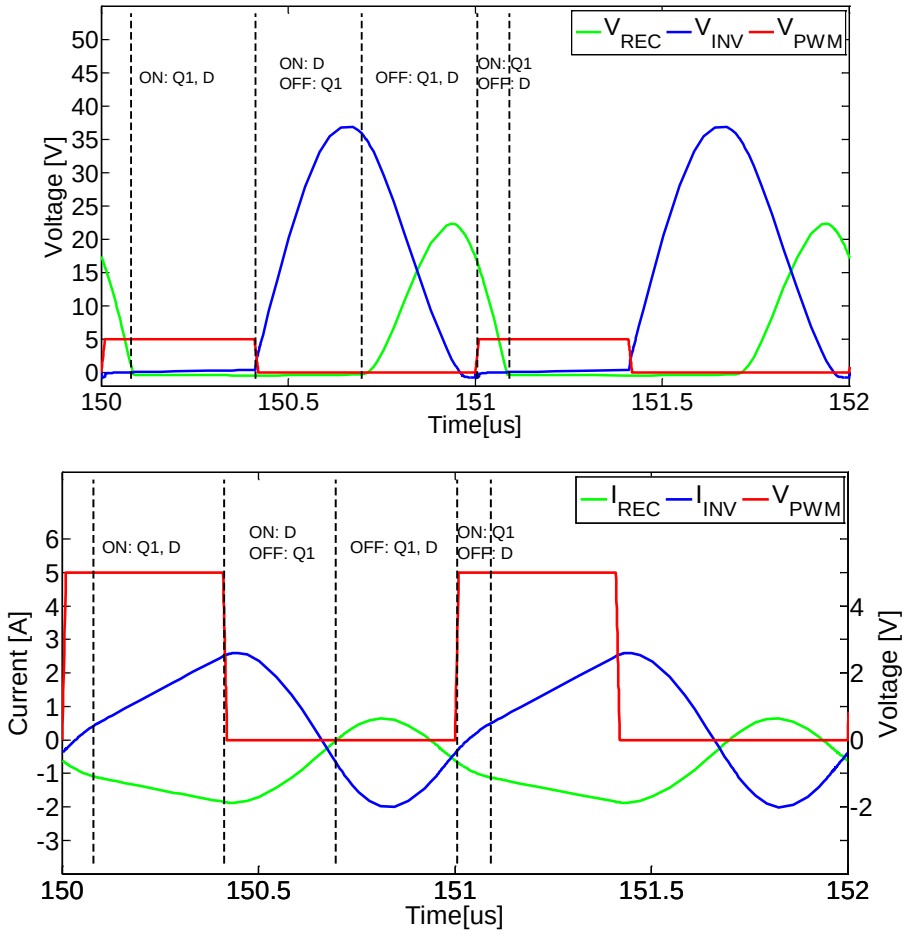


Figure 13 Simulation for a 40% duty cycle.

After simulating the ideal values, the schematic is analysed according to the values of table 5.

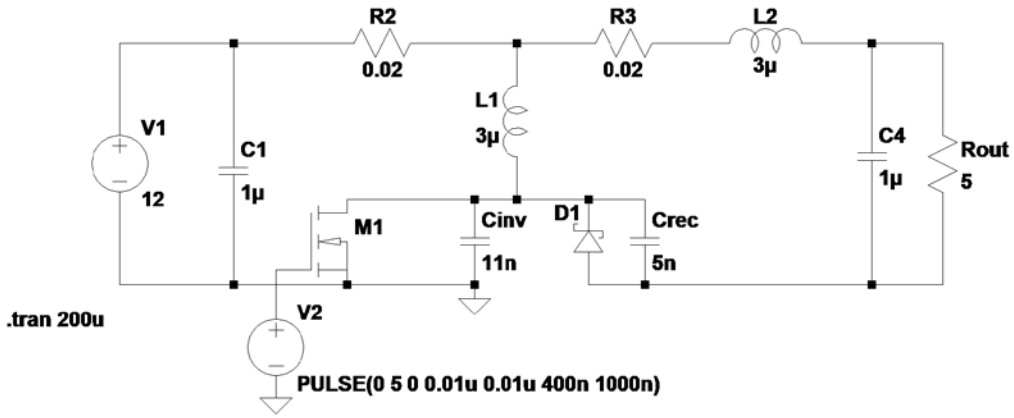


Figure 14 Schematic for a duty cycle of 40% with standard components.

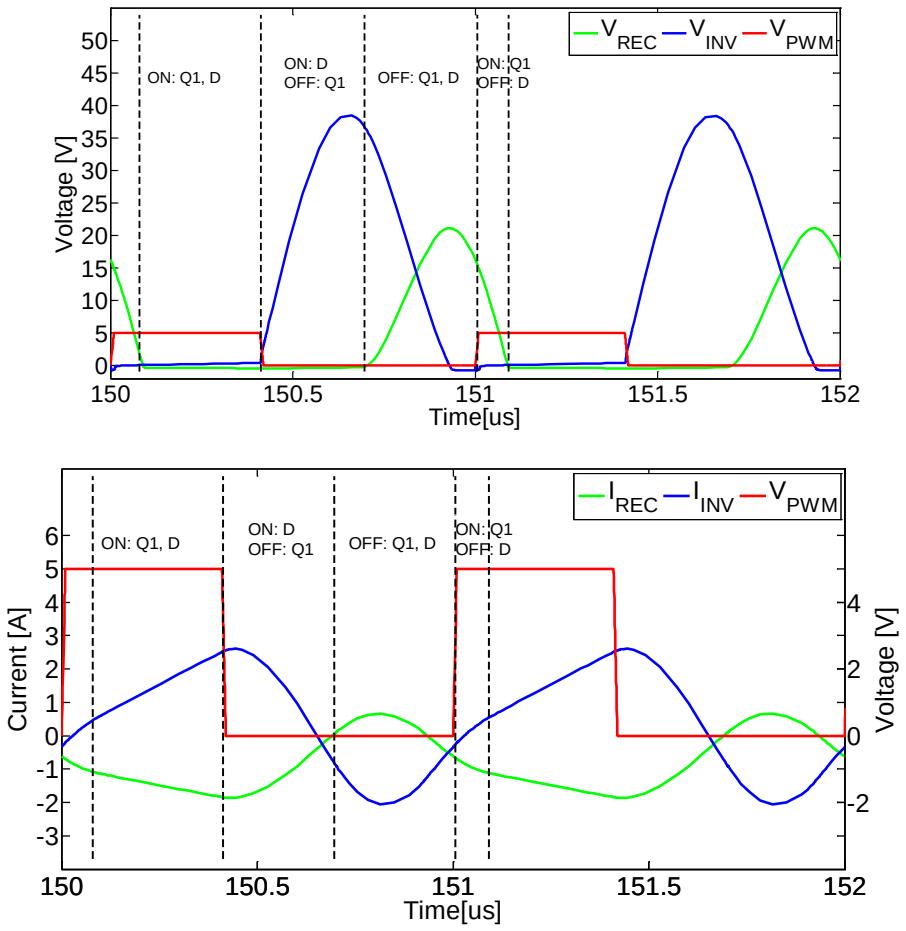


Figure 15 Simulation for a 40% duty cycle with standard components.

Simulation for duty cycle 50%

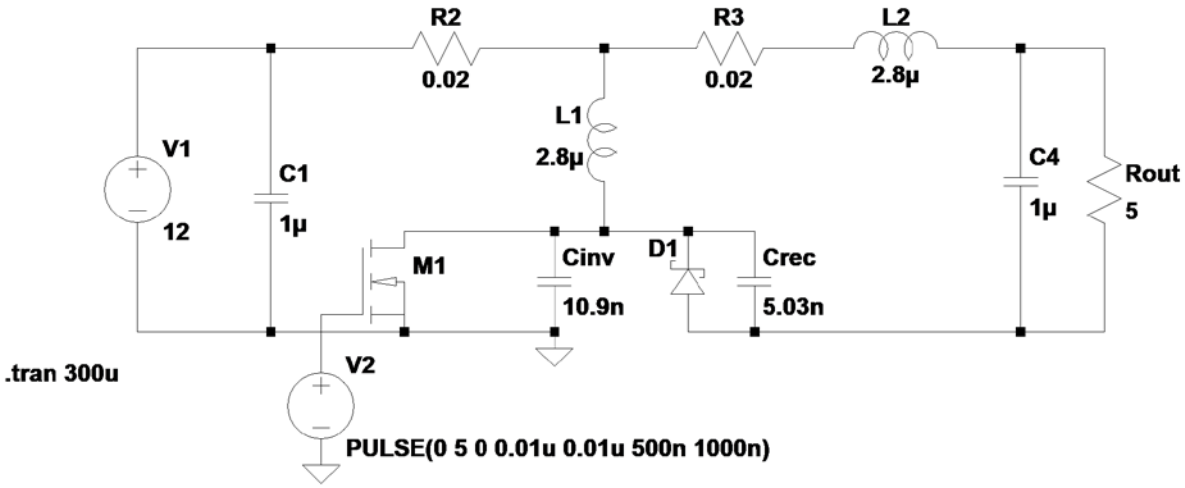


Figure 16 Schematic for a duty cycle of 50%.

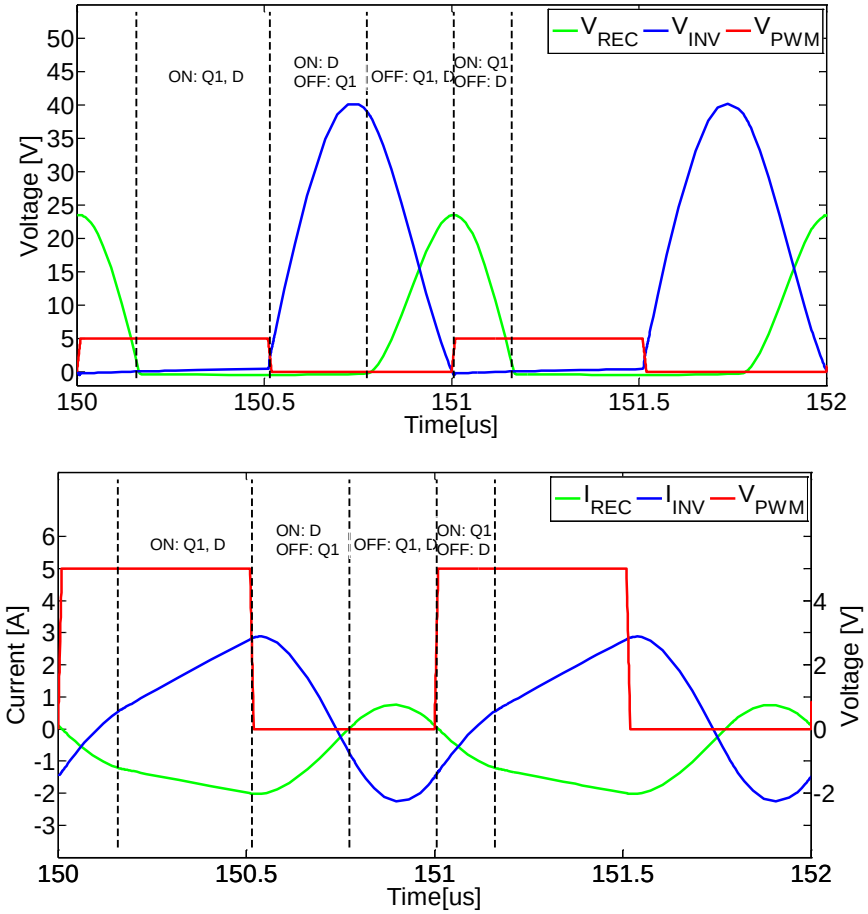


Figure 17 Simulation for a 50% duty cycle.

After simulating the ideal values, the schematic is analysed according to the values of table 5.

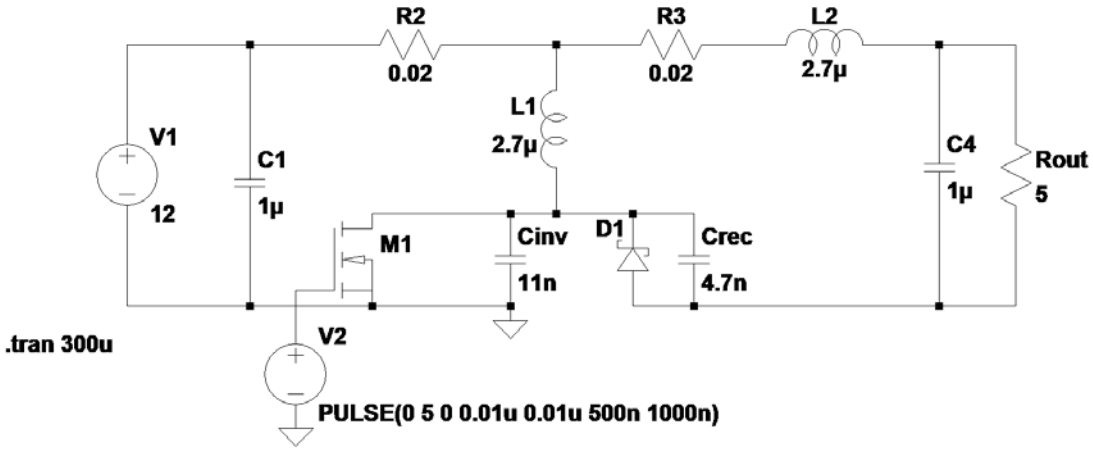


Figure 18 Schematic for a duty cycle of 50% with standard components.

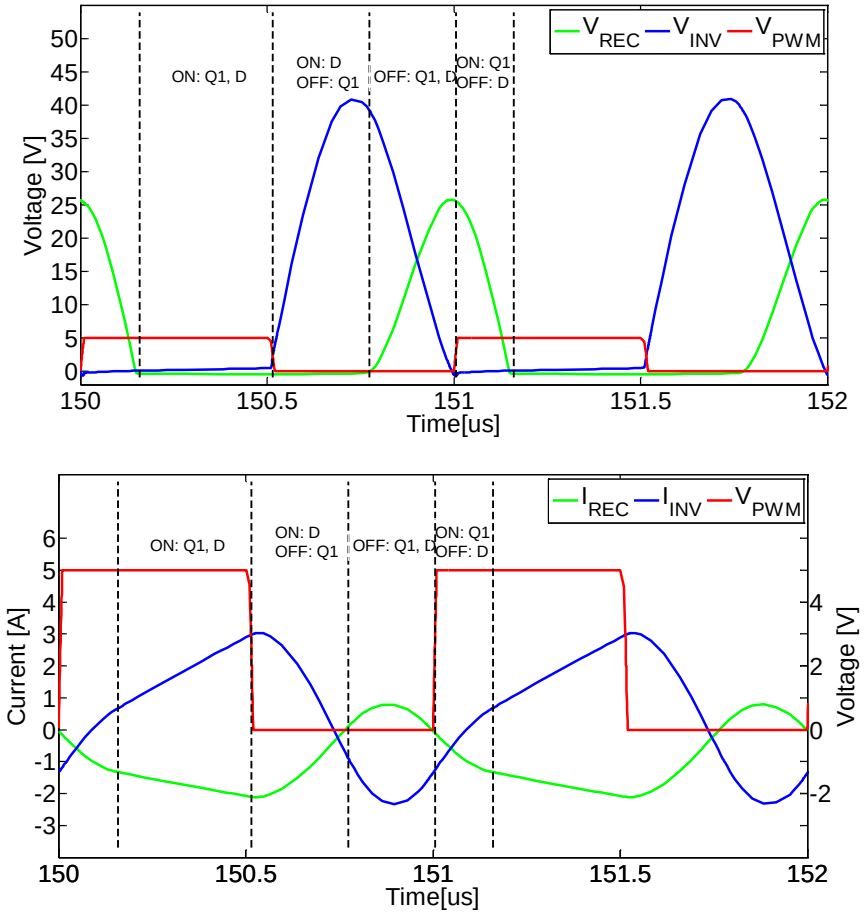


Figure 19 Simulation for a 50% duty cycle with standard components.

Simulation for duty cycle 60%

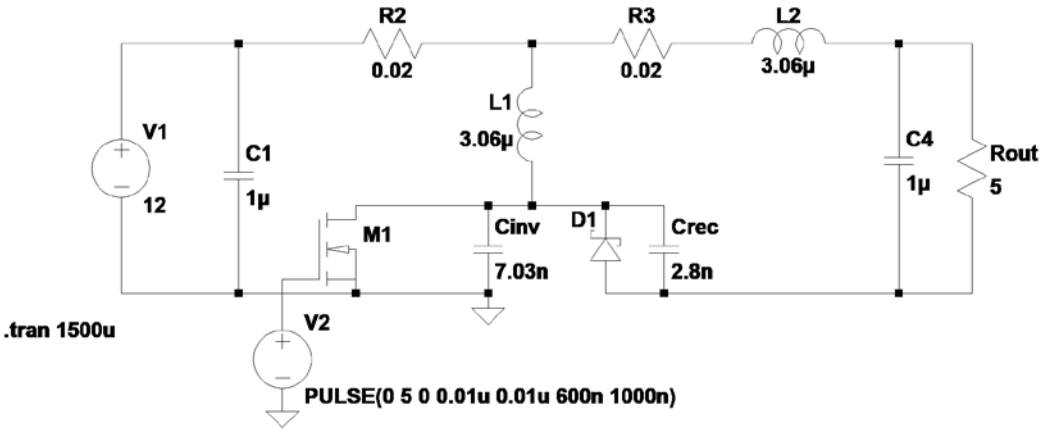


Figure 20 Schematic for a duty cycle of 60%.

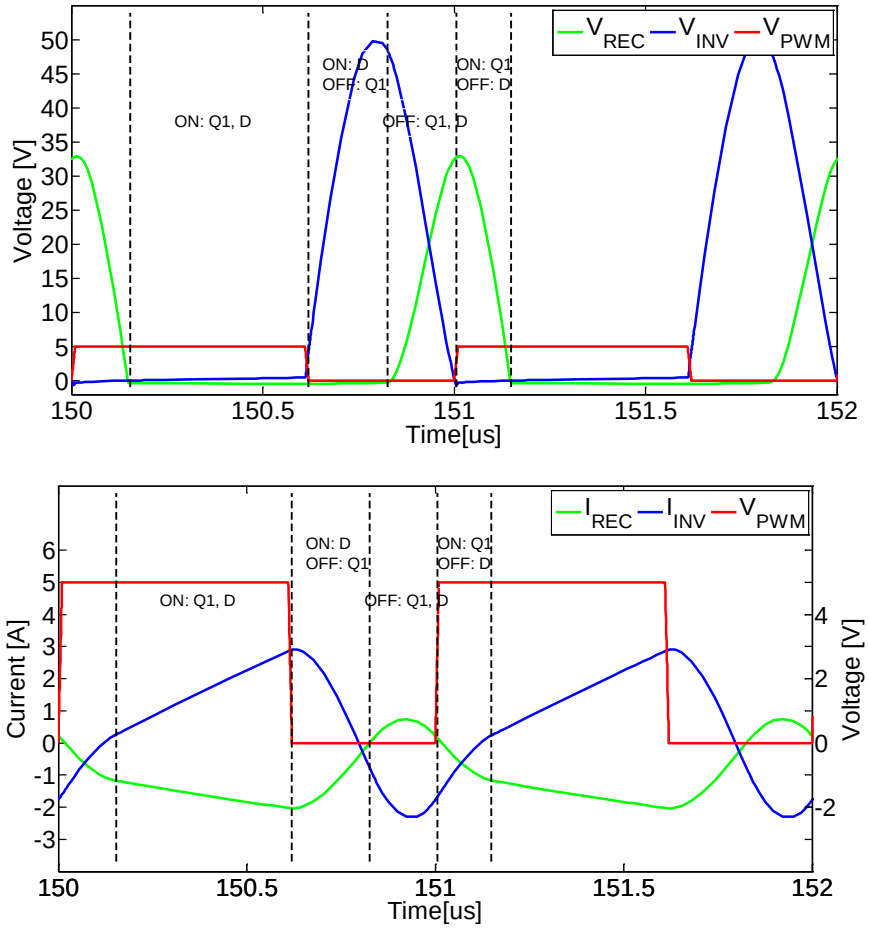


Figure 21 Simulation for a 60% duty cycle.

AS it is done before, the schematic is analysed according to the values of table 5.

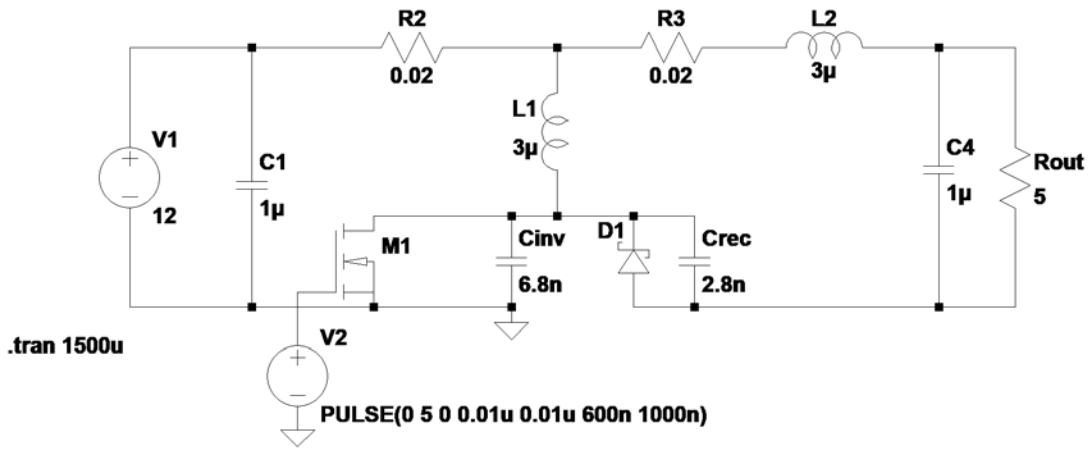


Figure 22 Schematic for a duty cycle of 60% with standards components.

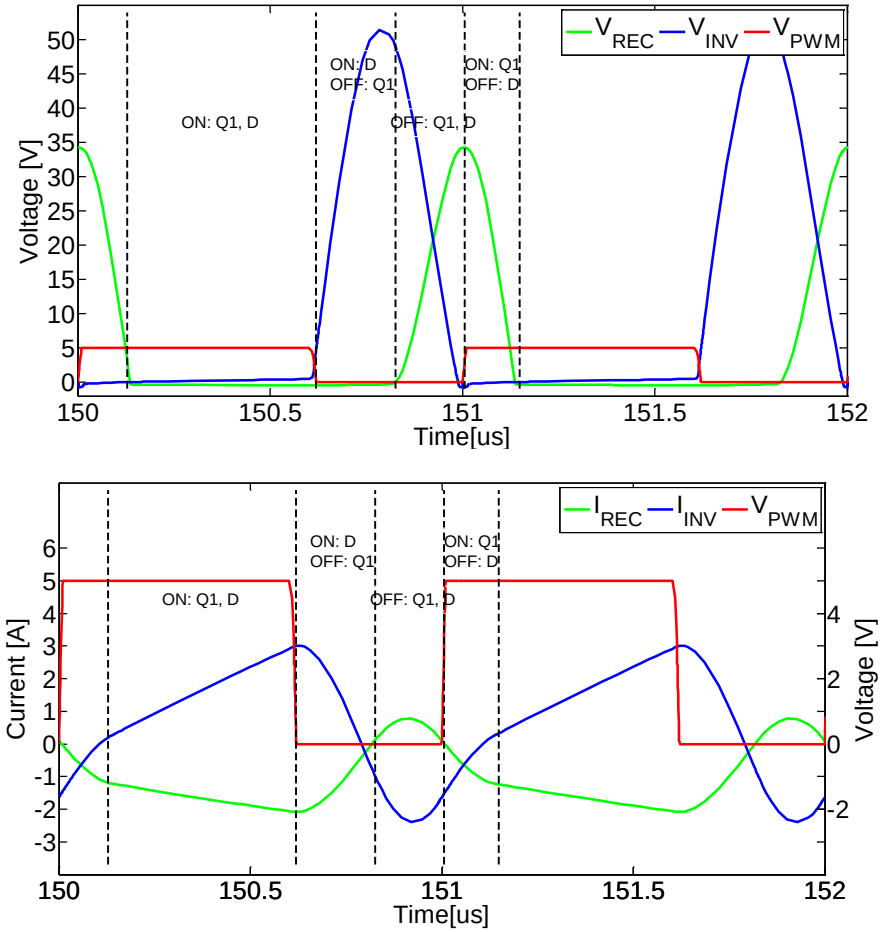


Figure 23 Simulation for a 60% duty cycle with standard components.

The simulation of the schematics with standard components are a bit more abrupt than the schematics with the ideal parameters. Taking into account the limitations, the results are acceptable and they meet the conditions imposed,

therefore the schematics can be implemented on a board. The switching frequency of 1 MHz is the same for optimal and standard simulations.

Table 6 shows the output voltage and the efficiency for each board.

Duty Cycle	Voltage input	Current input	Voltage output	Current output	Simulated efficiency
30%	12,00 V	0,37 A	3,74 V	0,75 A	63%
40%	12,00 V	0,42 A	4,04 V	0,81 A	65%
50%	12,00 V	0,57 A	4,76 V	0,95 A	66%
60%	12,00 V	0,63 A	5,25 V	1,05 A	73%

Table 6 Efficiency of simulated boards.

The board for 60% duty cycle is the only which generates the expected values, it is due to calculated values of the schematics are not entirely correct so it should be calculated again doing some changes in the Matlab script, it is a step that will be done in a future investigations.

Table 7 shows the output ripple.

Duty Cycle	Output Ripple
30%	0,38 V
40%	0,36 V
50%	0,42 V
60%	0,39 V

Table 7 Simulated output ripple.

After analysing the simulations, the components are selected according to the correct limits stipulate by the simulations and the dimensions of the boards.

3.4. Board Design

The schematic is implemented in four different boards. The process has been standardized by using some custom footprints for the components that change depending on the duty cycles implemented. These components are inverter and rectifier capacitors, input and output decoupling capacitors and the inductors.

As described in Section 2, to accomplish the EMC requirements imposed by the agencies and government, some considerations have to be taken into account

in the board design. These considerations are: the placements of the components as close as possible, placement of all components in only one layer and a ground layer in the bottom size. Thanks to this, the current loops and susceptibility of the device to malfunction or break down are reduced. Finally, vias have been added to ensure a low-impedance connection between the top and bottom ground plane.

The board design with the pertinent considerations to reduce the EMC is shown in figure 24.

The PCB without components and with them is shown in Figures 25 and 26. Four boards have been produced as shown in the Figure 25, each one for a different duty cycle.

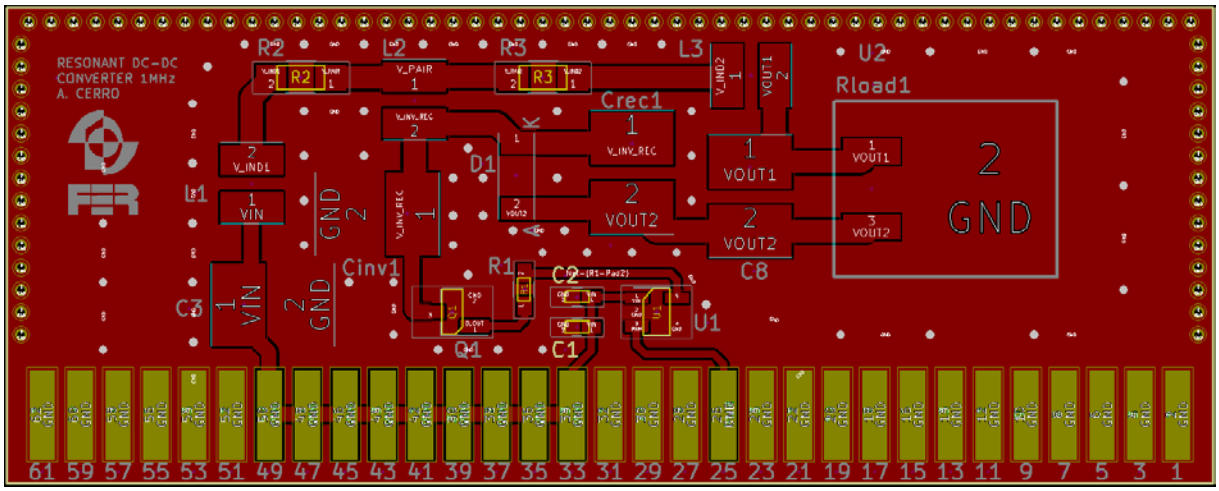


Figure 24 Board Design.

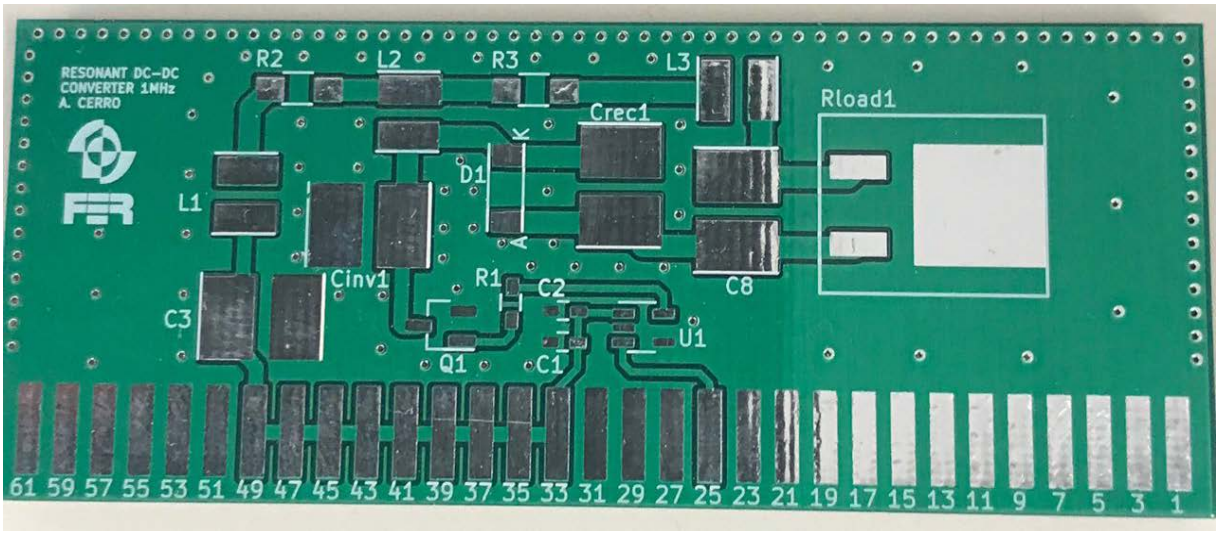


Figure 25 PCB without components.

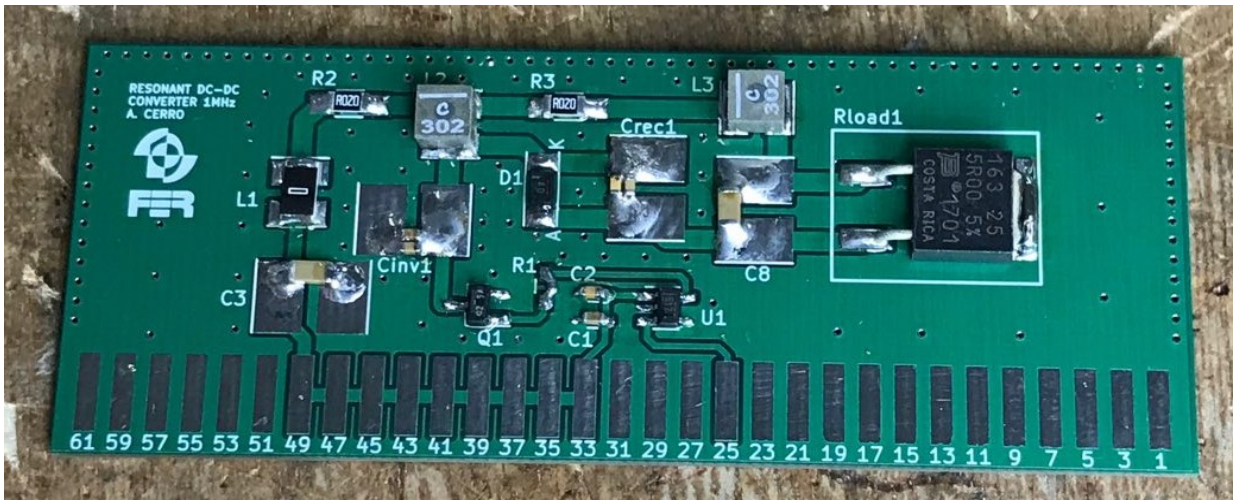


Figure 26 Board welded with components soldered.

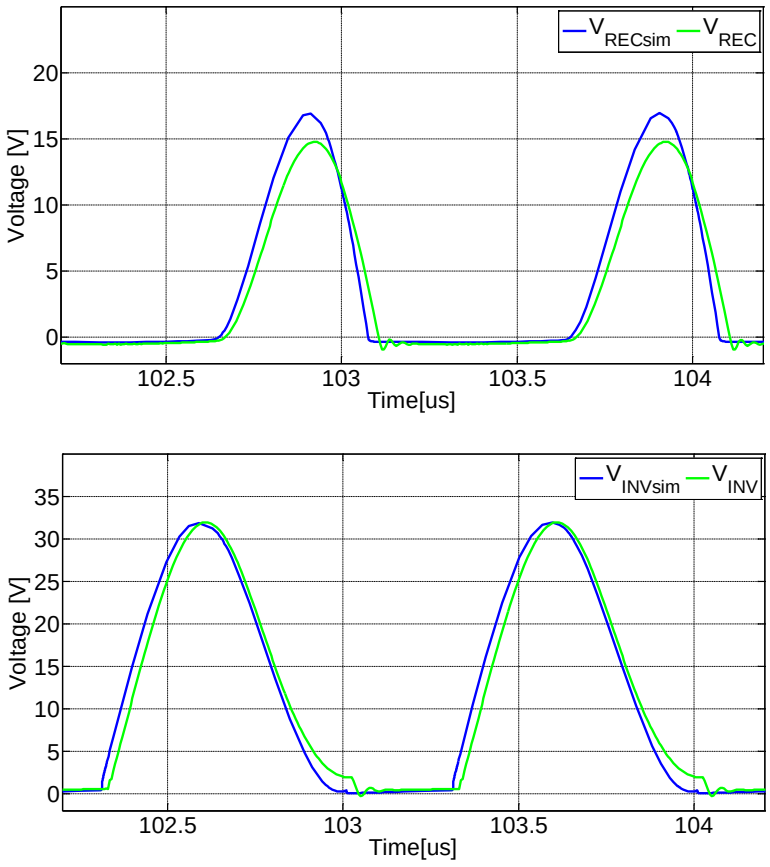
4. Measurements

4.1. Validation

Once the design has been carried out, it is verified that it complies with the previously fixed conditions, so once the boards have been soldered, the measurements are compared to the simulations. To carry out this verification, the power supply, oscilloscope and function generator are used.

The comparison between the signals simulated in LTspice and the measurements acquired from boards previously designed are shown below. This validation is done for each one of the PCBs designed with their corresponding duty cycle.

Validation of 30% duty cycle



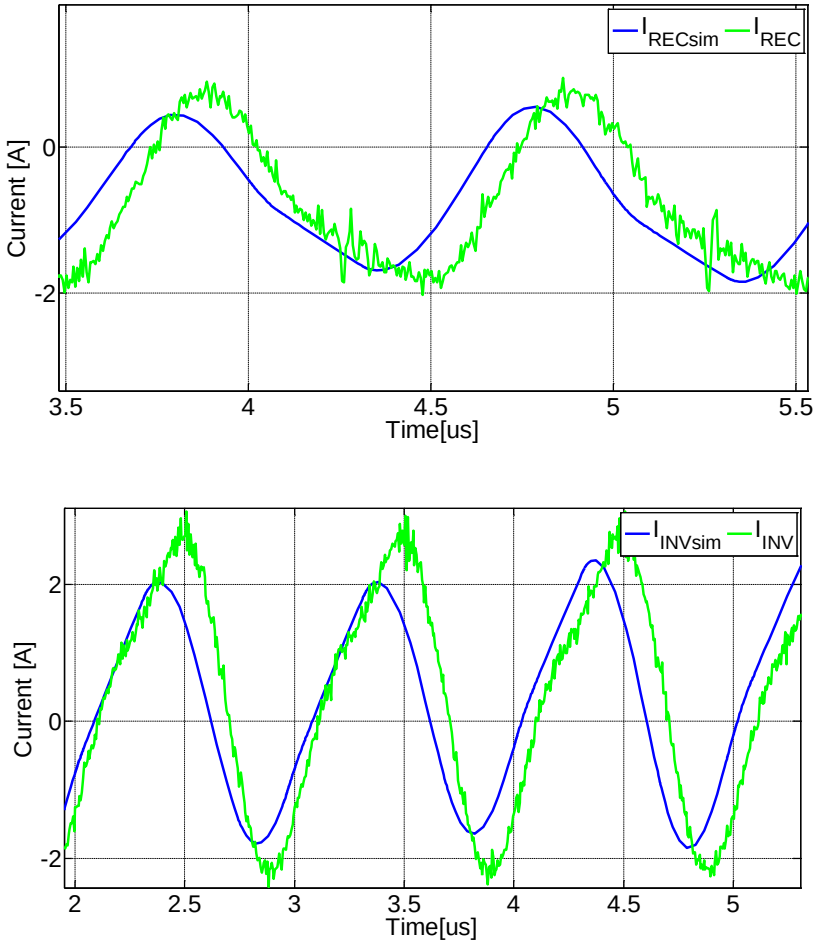
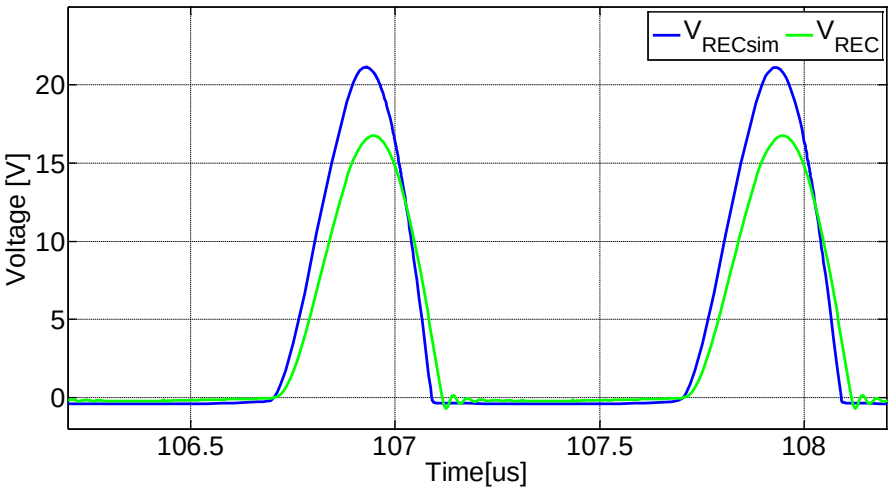
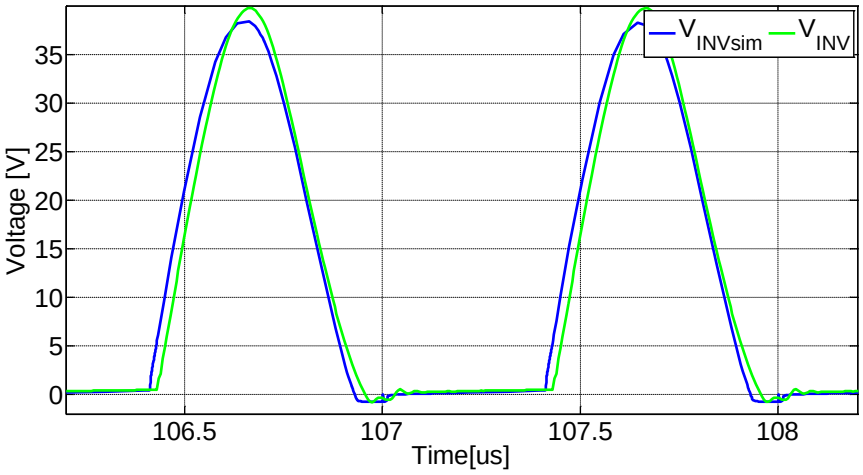


Figure 27 Validation DC-DC converter for 30% of duty cycle; comparison of measurements (green) and simulations (blue).

After verifying the simulations of the board for 30% duty cycle, it is observed how the measured voltages in the rectifier and inverter are very similar to those simulated; there is only a small offset of the signal. In relation to the currents, there is a greater difference with respect to the simulations, as well as, a greater amount of noise in the signal. This noise can be due to induced interference in the measurement cables and the noise produced by the current loops present on the board.

Validation of 40% duty cycle





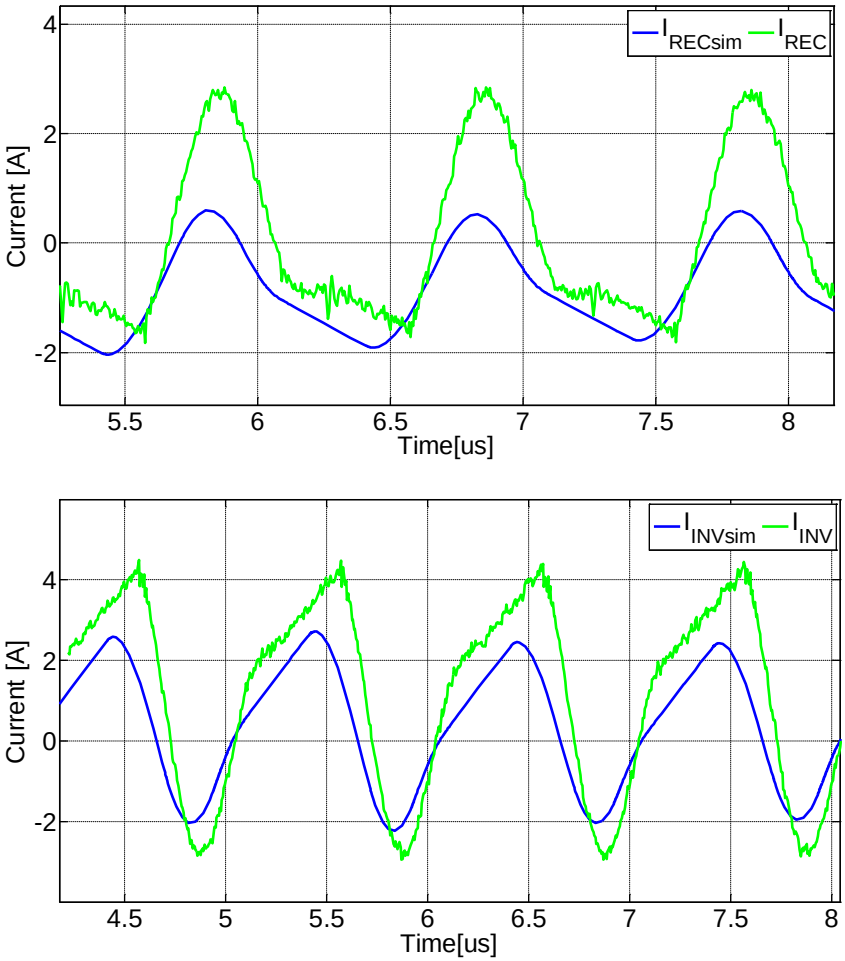
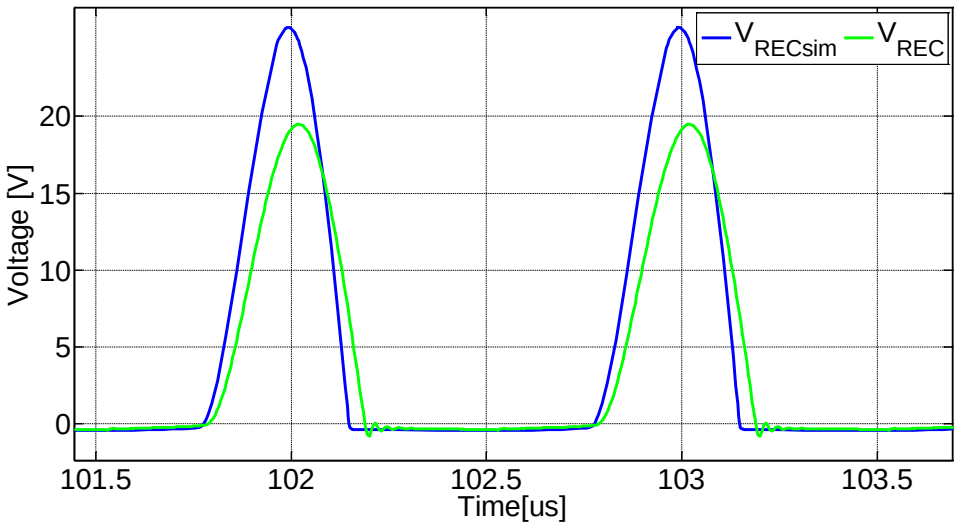


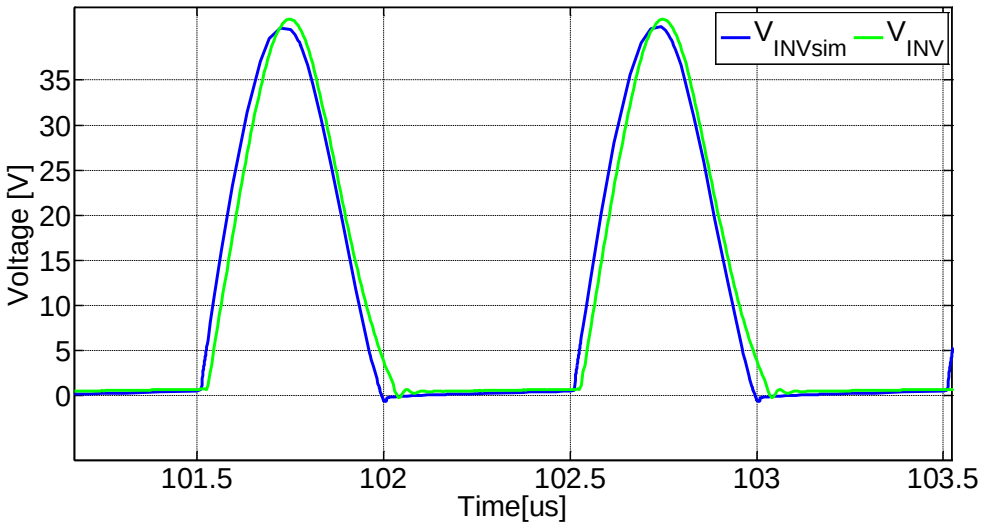
Figure 28 Validation DC-DC of 40% duty cycle; comparison of measurements (green) and simulations (blue).

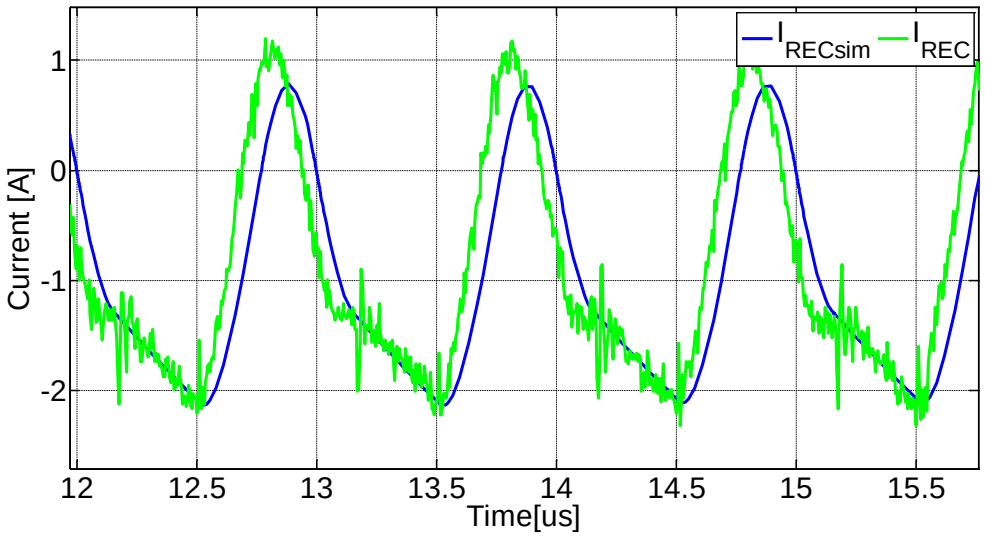
After verifying the simulations of the board for 40% duty cycle, it is observed how the rectifier voltage is slower than simulation and a bit higher in the inverter side. However, the results are similar to the results predicted by simulations.

Talking about the current, as it happened for the 30% duty cycle, the waveforms are similar to the simulated waveforms, but the values are a bit higher than the predicted. It should be pointed out that the noise is lower in this case.

Validation of 50% duty cycle







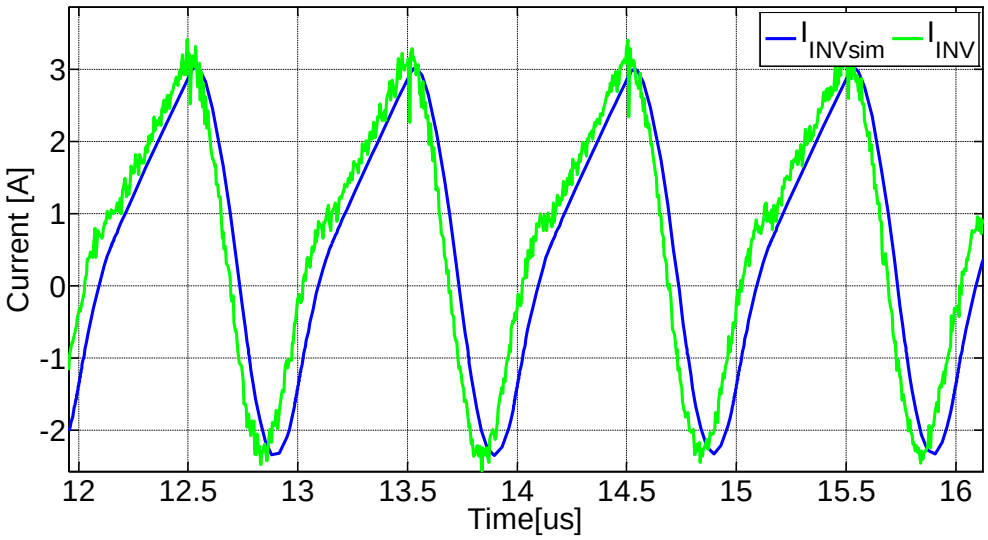
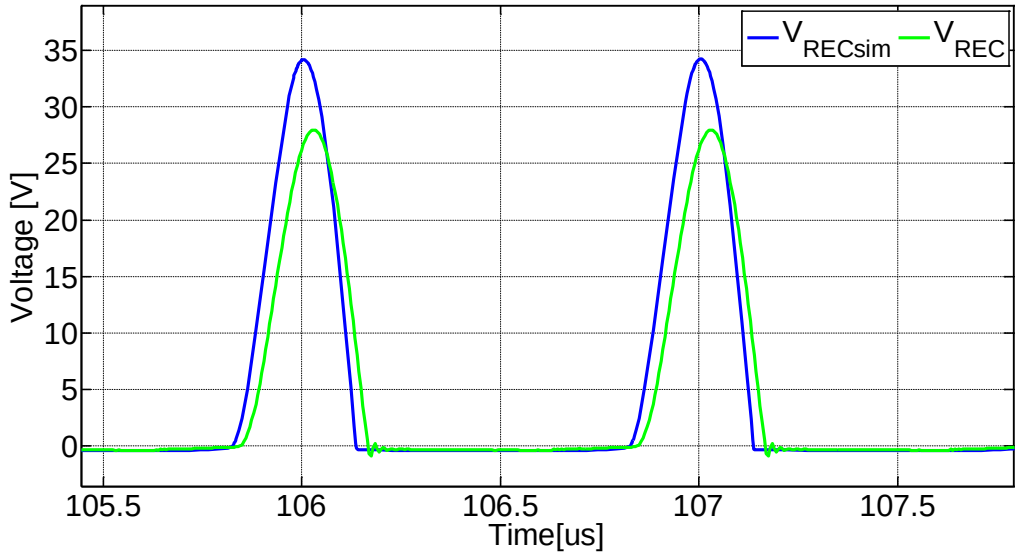


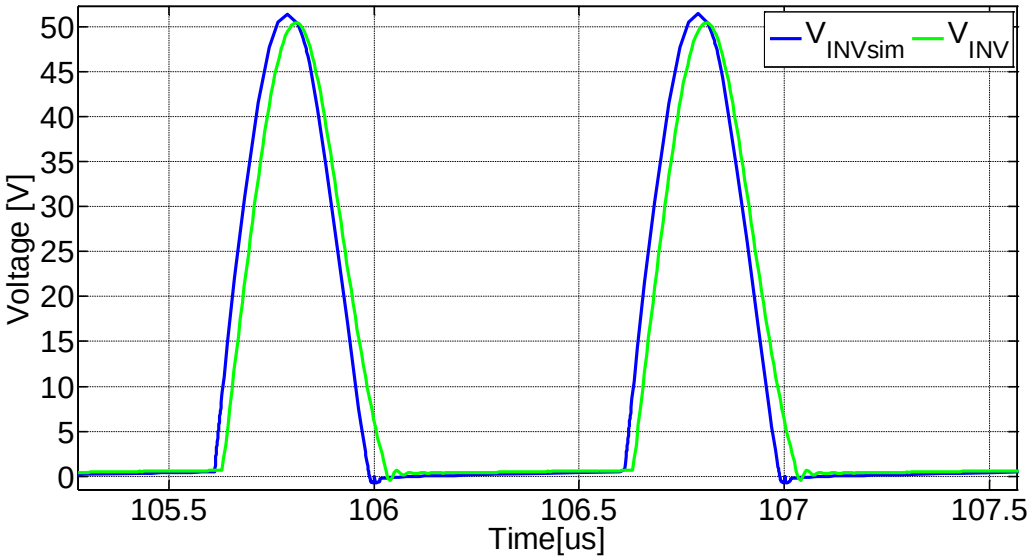
Figure 29 Validation DC-DC of 50% duty cycle; comparison of measurements (green) and simulations (blue).

After verifying the simulations of the board with 50% duty cycle, it is observed how the rectifier voltage is slower than simulated one and almost the same in the inverter side so the results are similar to the results predicted in simulations.

About the current, the results are similar to obtained in simulations, as it can be seen the current in the inverter side is a bit higher and with more noise than it is expected. This noise is due to interferences produced by the measurement cables. However, the current in the inverter side is almost identical to the simulated current.

Validation of 60% duty cycle





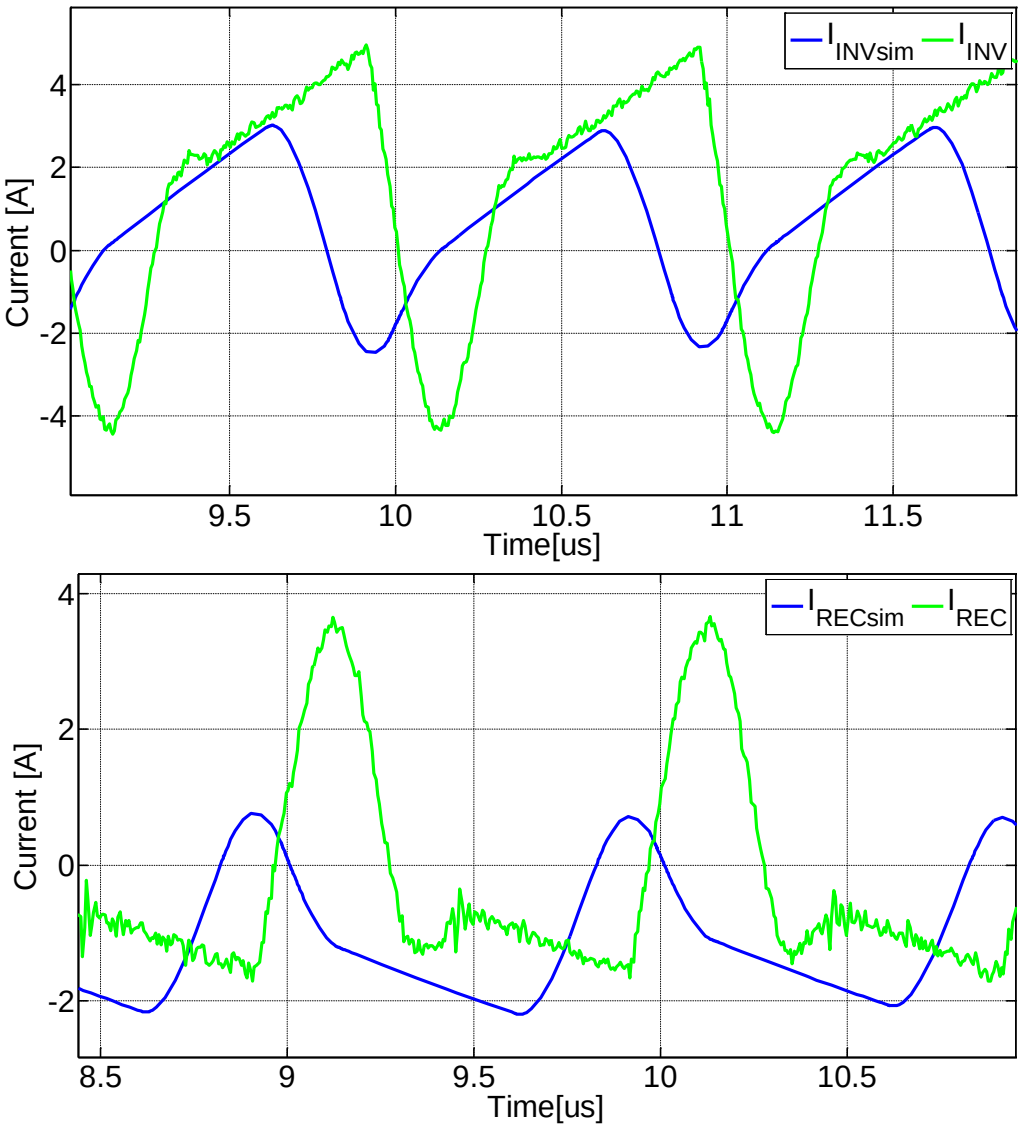


Figure 30 Validation DC-DC of 60% duty cycle; comparison of measurements (green) and simulations (blue).

In the simulations of the board with 60% duty cycle it is observed that in the rectifier the voltage is a bit slower than in simulations, as it happened with the rest of convertors. However, the inverter side has almost the same value.

Talking about the current, as it happened with the other duty cycles the waveforms are similar to the simulate ones, but the values are different from the predicted values, in this case both currents are around 2A higher. It should be pointed out that the noise is lower in the voltages and inverter current. However, rectifier current has zones where the noise is higher than the rest of simulations. This noise is due to parasitic impedance of the current sense resistors and the differential probe, which is used to measure the current. The differential probe

has the problem of the wire lengths; these are too long so some interference is induced in the measurements.

The efficiency obtained by measurements of the boards is shown in table 8.

Duty Cycle	Voltage input	Voltage output	Current input	Current output	Measured efficiency
30%	12,00 V	3,55 V	0,44 A	0,71 A	48%
40%	12,00 V	3,74 V	0,44 A	0,75 A	53%
50%	12,00 V	4,23 V	0,58 A	0,85 A	51%
60%	12,00 V	4,76 V	0,66 A	0,95 A	57%

Table 8 Efficiency DC-DC converters obtained by the measurements.

The values of the efficiency are low for the designed boards. It is due to the equivalent series resistors of capacitors, which modify the efficiency of the class E resonant DC-DC converter.

To prove the impact of the equivalent series resistors (ESR) in the efficiency, these resistances have been studied. Table 9 shows the values of the equivalent series resistors for the components in the circuit.

D = 30%						
$C_{INVERTOR}$		**$C_{RECTIFIER}$**		**MOSFET**	**INDUCTOR**	**CAPCITOR**
0,015uF	470pF	1000pF	5600pF	Rds_{ON}	2,7uH	1uF
0,575 Ω	6,37 Ω	3,45 Ω	1,102 Ω	0,18 Ω	0,034 Ω	0,013 Ω
D = 40%						
$C_{INVERTOR}$		**$C_{RECTIFIER}$**		**MOSFET**	**INDUCTOR**	**CAPCITOR**
0,01uF	1000pF	4700pF	470pF	Rds_{ON}	3uH	1uF
0,753 Ω	3,45 Ω	1,09 Ω	6,37 Ω	0,18 Ω	0,004 Ω	0,013 Ω
D = 50%						
$C_{INVERTOR}$		**$C_{RECTIFIER}$**		**MOSFET**	**INDUCTOR**	**CAPCITOR**
0,01 uF	1000 pF	4700 pF	330 pF	Rds_{ON}	2,7uH	1uF
0,753 Ω	3,45 Ω	1,09 Ω	12,02 Ω	0,18 Ω	0,034 Ω	0,013 Ω
D = 60%						
$C_{INVERTOR}$		**$C_{RECTIFIER}$**		**MOSFET**	**INDUCTOR**	**CAPCITOR**
2200 pF	4700 pF	1000 pF	1800 pF	Rds_{ON}	3uH	1uF
1,85 Ω	1,09 Ω	3,45 Ω	2,09 Ω	0,18 Ω	0,004 Ω	0,013 Ω

Table 9 Equivalent Series Resistances.

The table shows how in the rectifier and inverter side the equivalent series resistance is higher than for the rest of parameters in the circuit. It produces more losses and as a consequence, the efficiency decreases.

The schematic is simulated with a lower ESR (0.01 Ω) in the parasitic elements to prove how the efficiency increases. The results are shown in Table 10.

Duty Cycle	Voltage input	Current input	Voltage output	Current output	Simulated efficiency
30%	12,00 V	0,31 A	3,92 V	0,78 A	83%
40%	12,00 V	0,34 A	4,15 V	0,83 A	85%
50%	12,00 V	0,47 A	4,90 V	0,98 A	85%
60%	12,00 V	0,55 A	5,37 V	1,08 A	88%

Table 10 Efficiency DC-DC converters with low ESR.

As a consequence of reducing the ESR the efficiency increases considerable, it even reaches values around 90%. The reduction of the ESR is an issue to take into account to improve the design of converters.

4.2. Radiated Emissions

The analysis of the radiated emissions (RE) is done with a TEM cell. To do these measurements a power supply of 12 V and a waveform generator to generate the PWM of 5V are used. In addition, to acquire the radiated emissions data, an EMI test receiver is used. This set up can be seen in Figure 31.

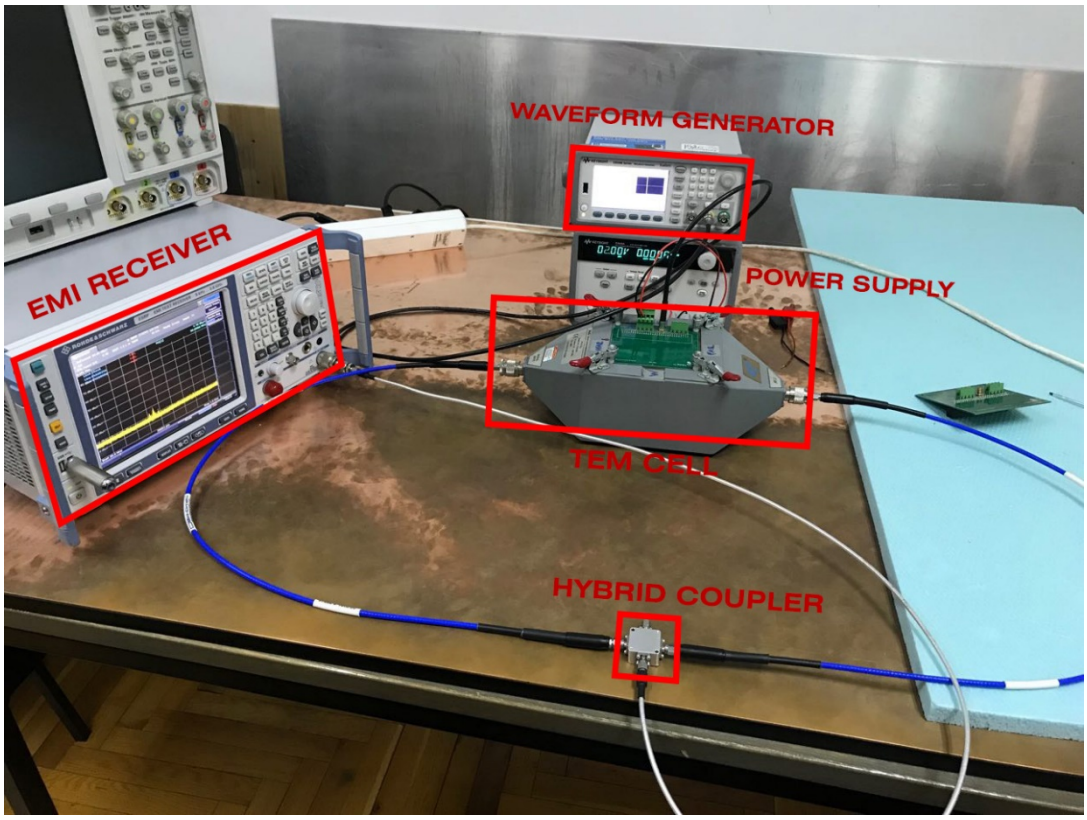


Figure 31 TEM cell measurement.

A hybrid coupler connected to TEM cell is used to acquire the data. The hybrid coupler is a device that has two inputs and two outputs, one of the inputs has a phase of 0º and the other has 180º. The sum of both signals or the difference between them can be obtained by this setup.

The measurements of radiated emissions for each board is done with the sum and differential output at different times. When using an output, the other one is terminated by an impedance of 50 Ω. This load is used because it provides a match at lower frequencies and an absorber wall to suppress reflections at higher frequencies. Moreover, with each measurement of the hybrid coupler, the board is fixed in horizontal position, vertical position and the interpose in which the board is placed is rotated 90º for each one. In his way all different possibilities are tested. Overall, there are five measurements of each board:

1. The board in horizontal position with the interpose in the initial position and using the sum output (A1SUM).
2. The board in horizontal position with the interpose turned 90º and using the differential output (A2ISO).

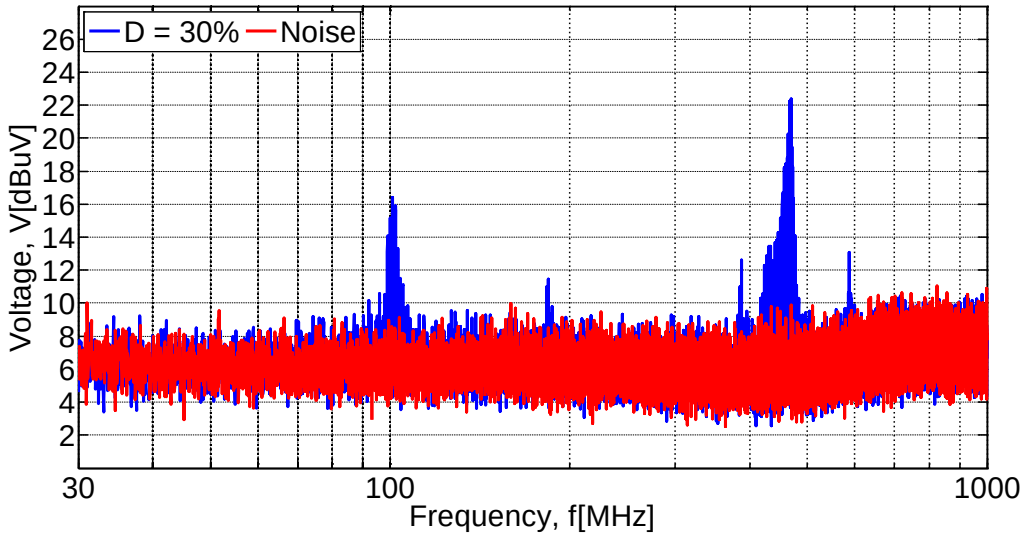
3. The board in horizontal position with the interpose turned 90º and using the sum output (A2SUM).
4. The board in vertical position with the interpose turned 90º and using the sum output (S2SUM).
5. The board in vertical position with the interpose turned 90º and using the differential output (S2ISO).

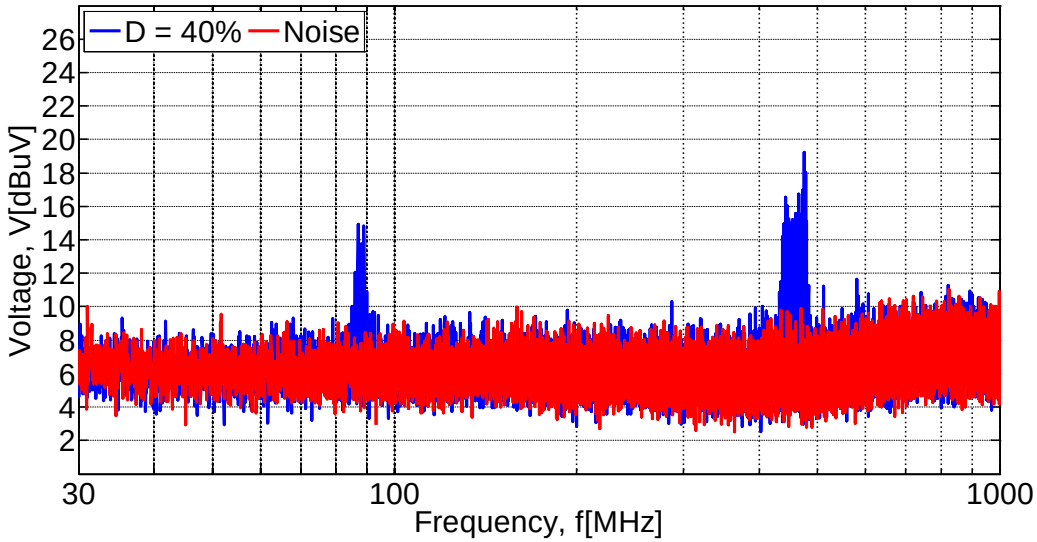
The easiest way to measure radiated emissions is to model the DUT as a group of dipoles (magnetic and electrical) and use the TEM cell to measure the magnitude of these. So according to [4] a minimum of six measurements are needed when the type of source is unknown (electric or magnetic).

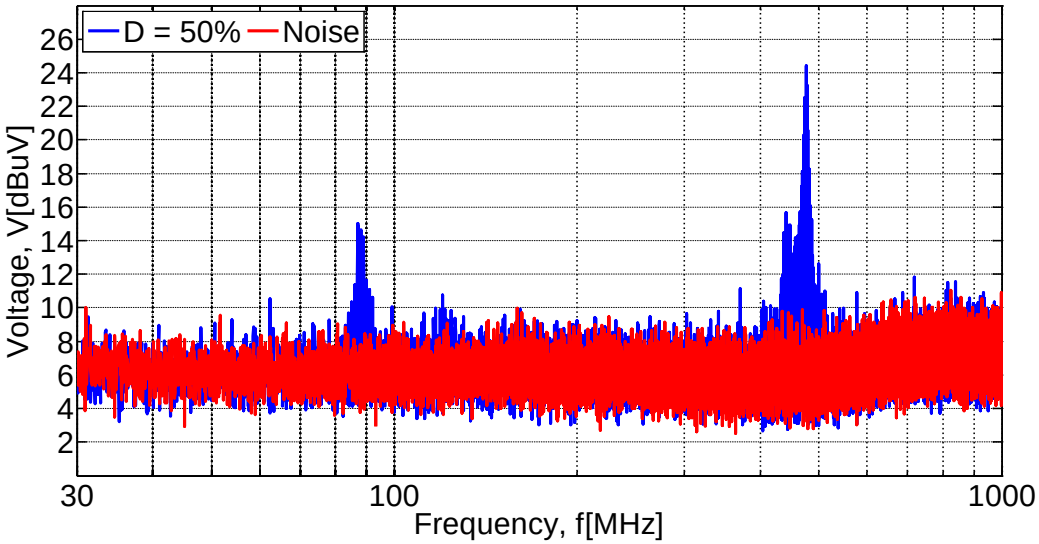
The electric dipoles are obtained through the sum of the two signals acquired from the TEM cell. These correspond to the measurements obtained through the differential output of the hybrid coupler, one of the signals of input has a phase of 180º so it corresponds to the sum of both signals. These measurements are A2ISO and S2ISO.

With respect to the magnetic dipoles, these are obtained through the difference of the two signals, corresponding to the measurements: A1SUM, A2SUM and S2SUM. It has to be noted that only five of the six measures have been taken, because one of them (A1ISO) is coupled with the electric field as indicated in [4], making impossible to measure it. To measure this dipole another measurement would have to be done which is impossible due to the dimensions of the TEM cell.

The measurements obtained by this configuration are shown as it follows.


D = 30%
Noise
Voltage, V[dBuV]
Frequency, f[MHz]
30
100
1000


D = 40%
Noise
Voltage, V[dBuV]
Frequency, f[MHz]
30
100
1000


D = 50%
Noise
Voltage, V[dBuV]
Frequency, f[MHz]
30
100
1000

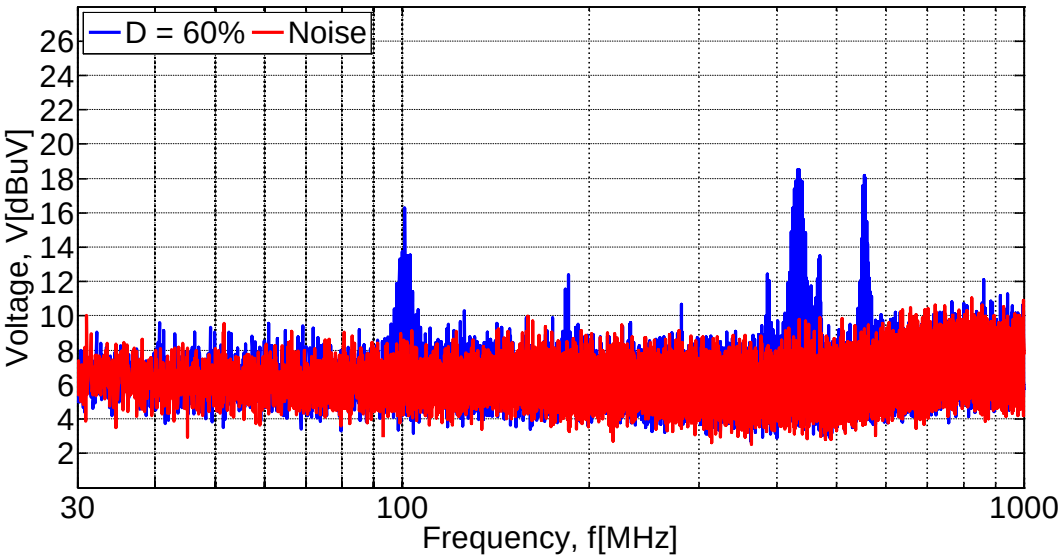
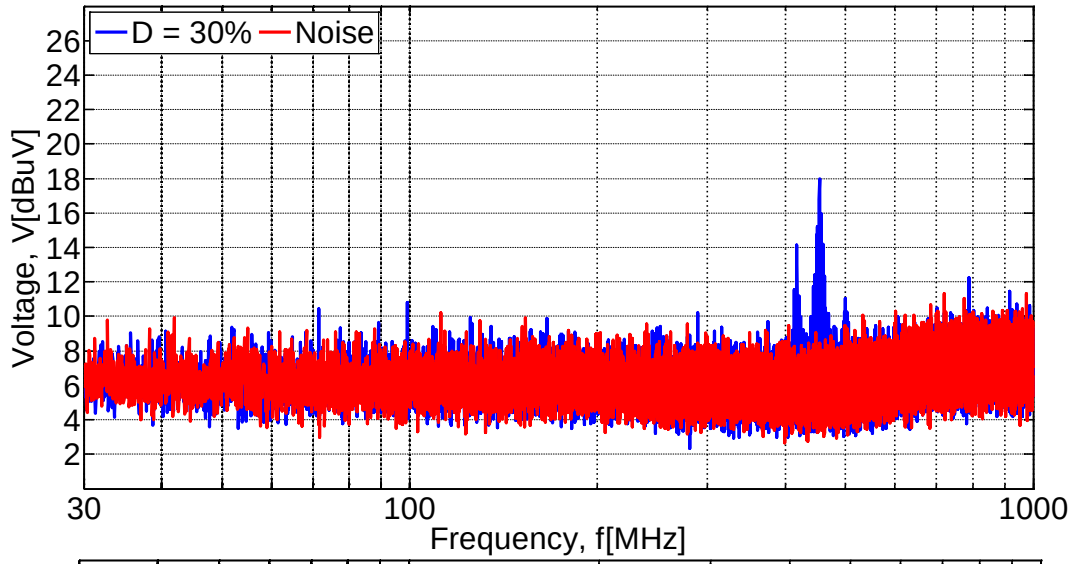
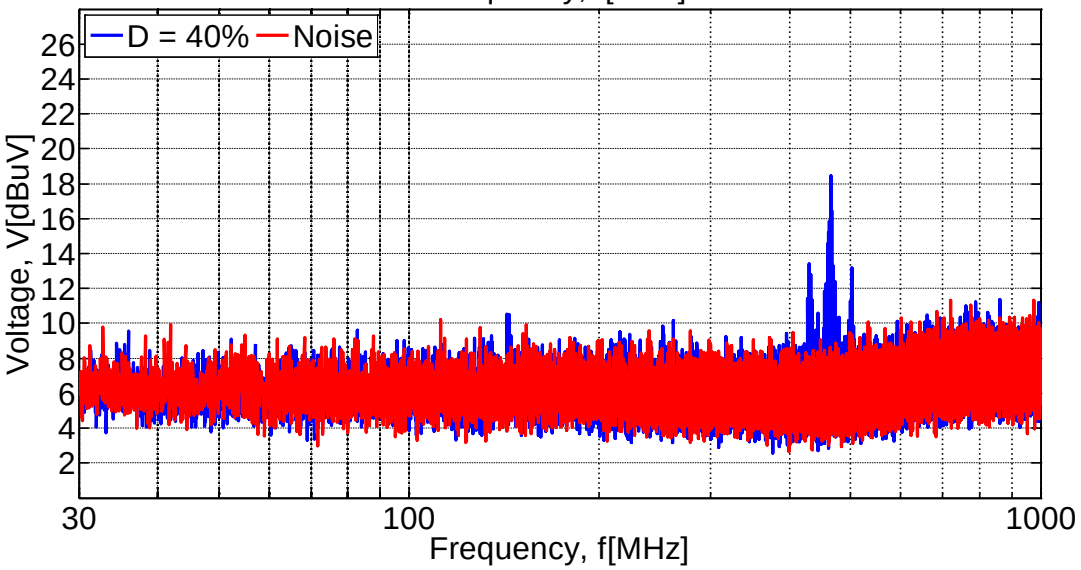


Figure 32 Radiated emissions with horizontal position and sum output.


D = 30%
Noise
Voltage, V[dBuV]
26
24
22
20
18
16
14
12
10
8
6
4
2
30
100
1000
Frequency, f[MHz]


D = 40%
Noise
Voltage, V[dBuV]
26
24
22
20
18
16
14
12
10
8
6
4
2
30
100
1000
Frequency, f[MHz]

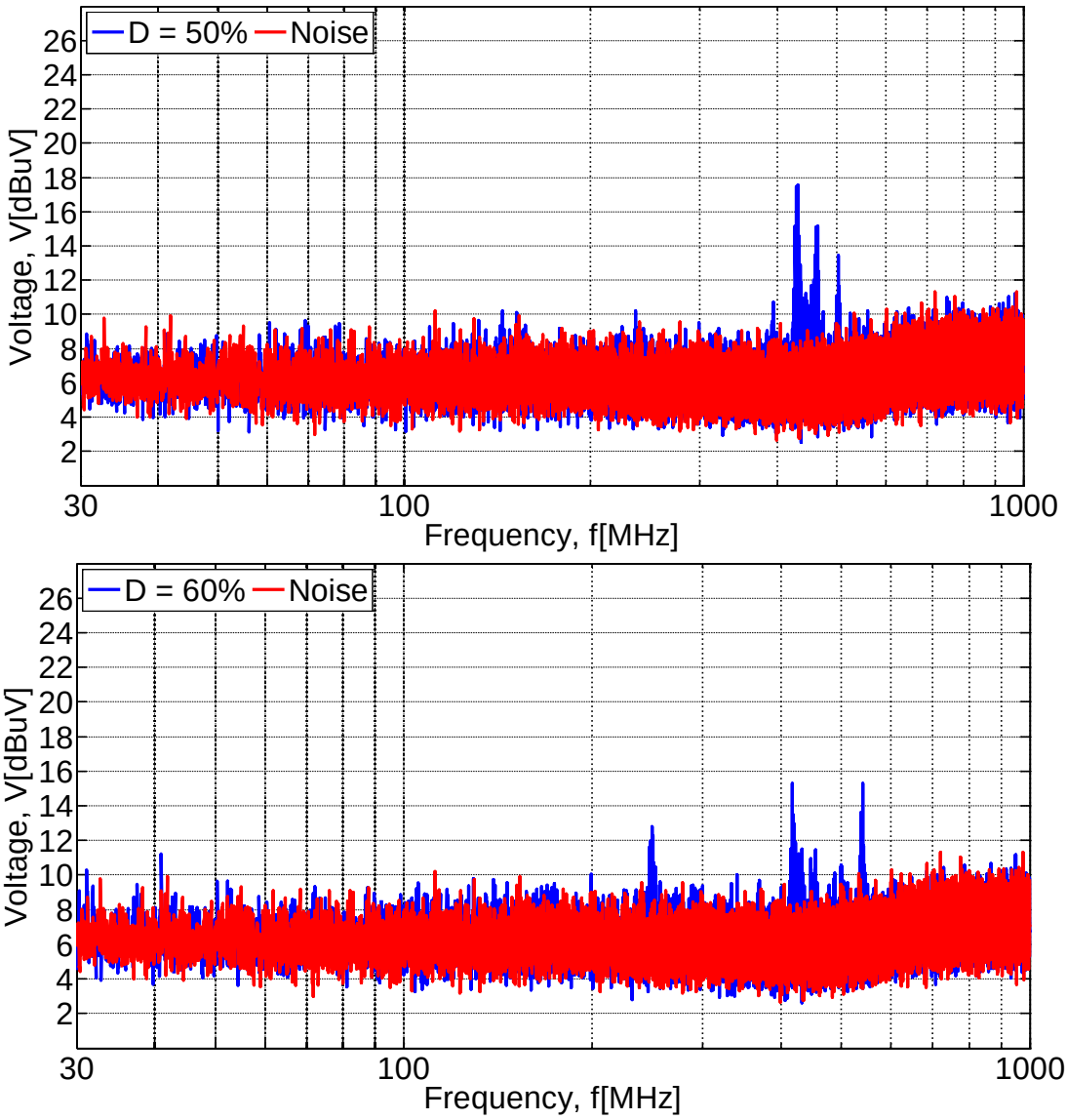
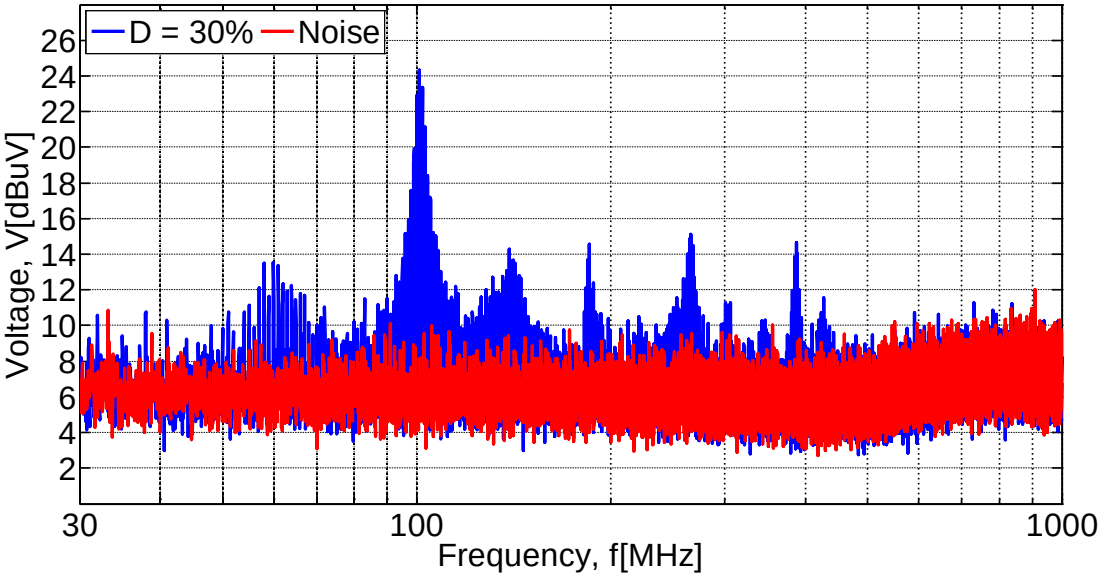
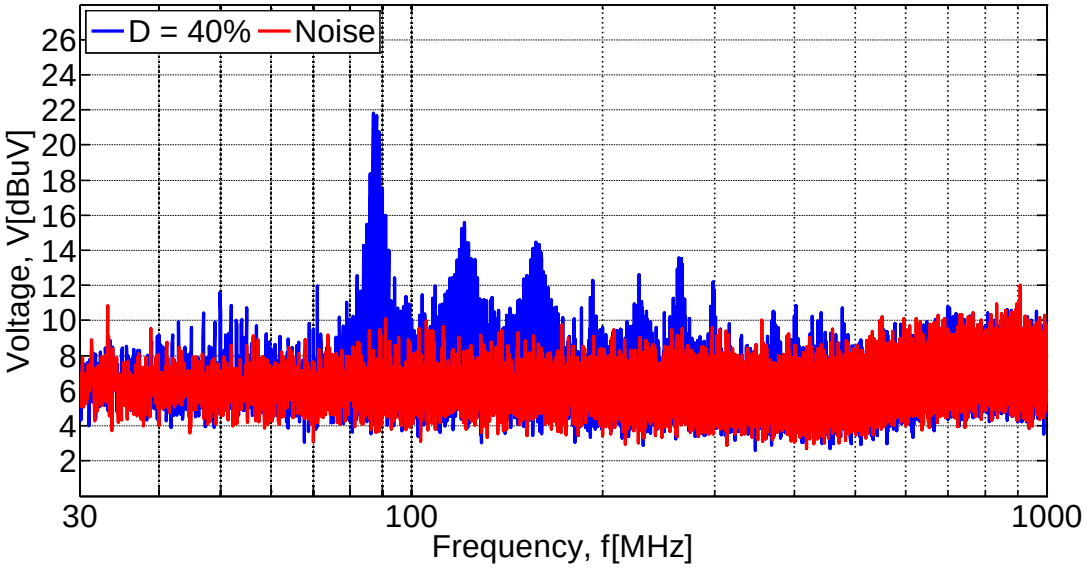
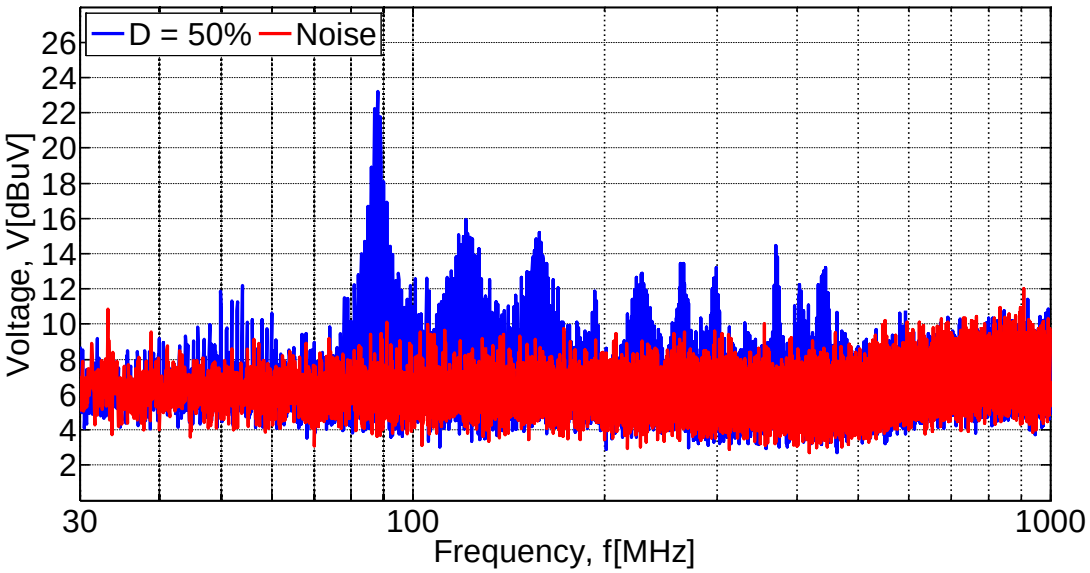


Figure 33 Radiated emissions with horizontal position, turned 90º and differential output.


D = 30%
Noise
Voltage, V[dBuV]
Frequency, f[MHz]
30
100
1000


D = 40%
Noise
Voltage, V[dBuV]
Frequency, f[MHz]
30
100
1000


D = 50%
Noise
Voltage, V[dBuV]
Frequency, f[MHz]
30
100
1000

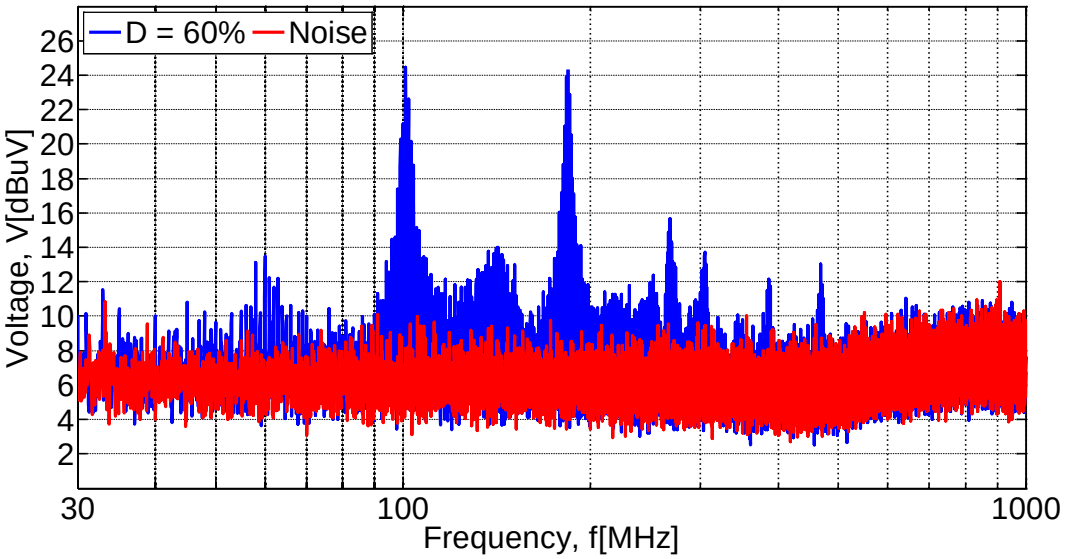
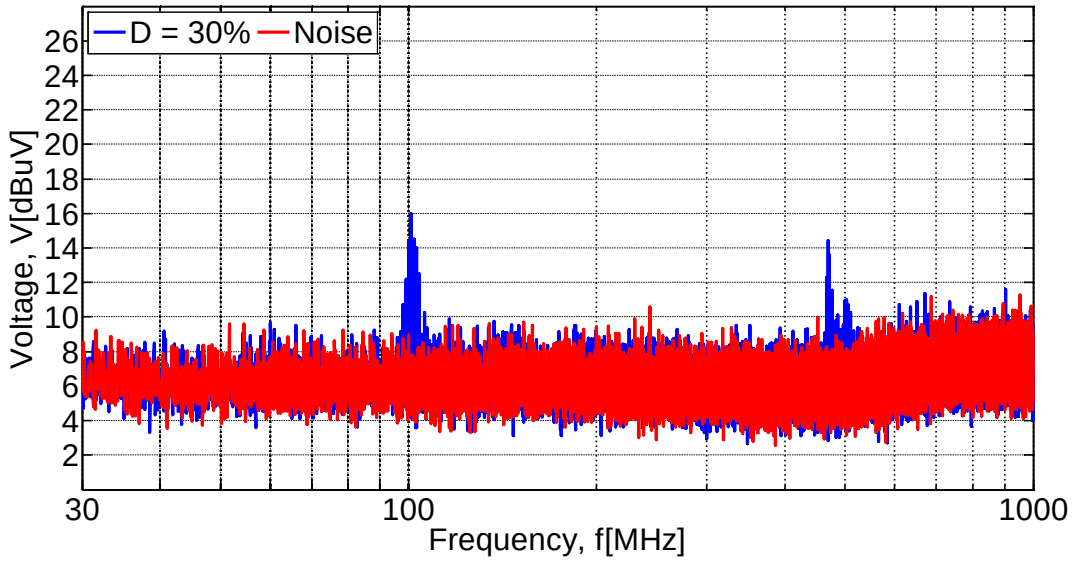
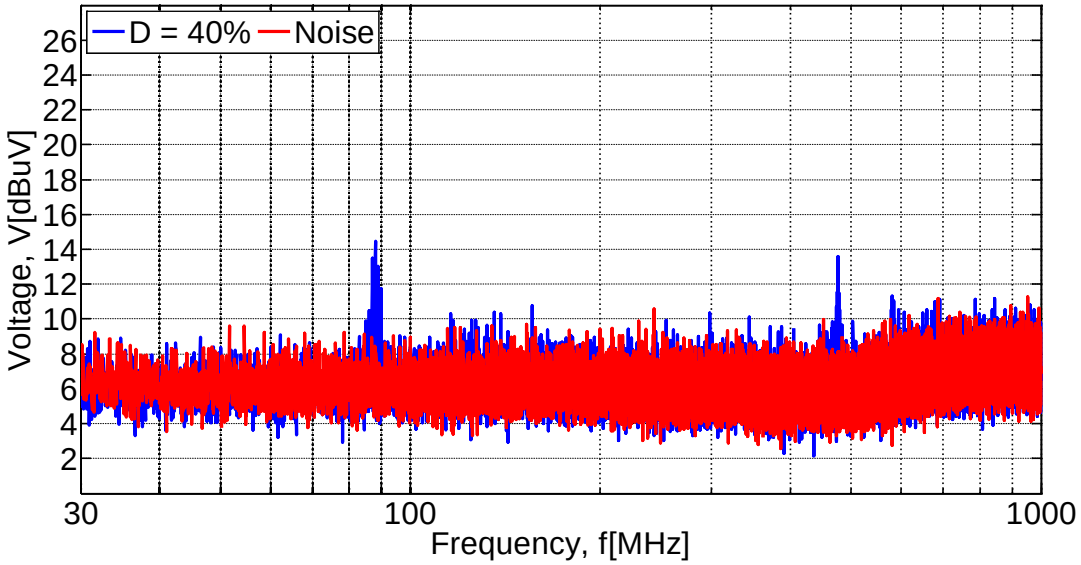


Figure 34 Radiated emissions with horizontal position, turned 90º and sum output.


D = 30%
Noise
Voltage, V[dBuV]
26
24
22
20
18
16
14
12
10
8
6
4
2
30
100
1000
Frequency, f[MHz]


D = 40%
Noise
Voltage, V[dBuV]
26
24
22
20
18
16
14
12
10
8
6
4
2
30
100
1000
Frequency, f[MHz]

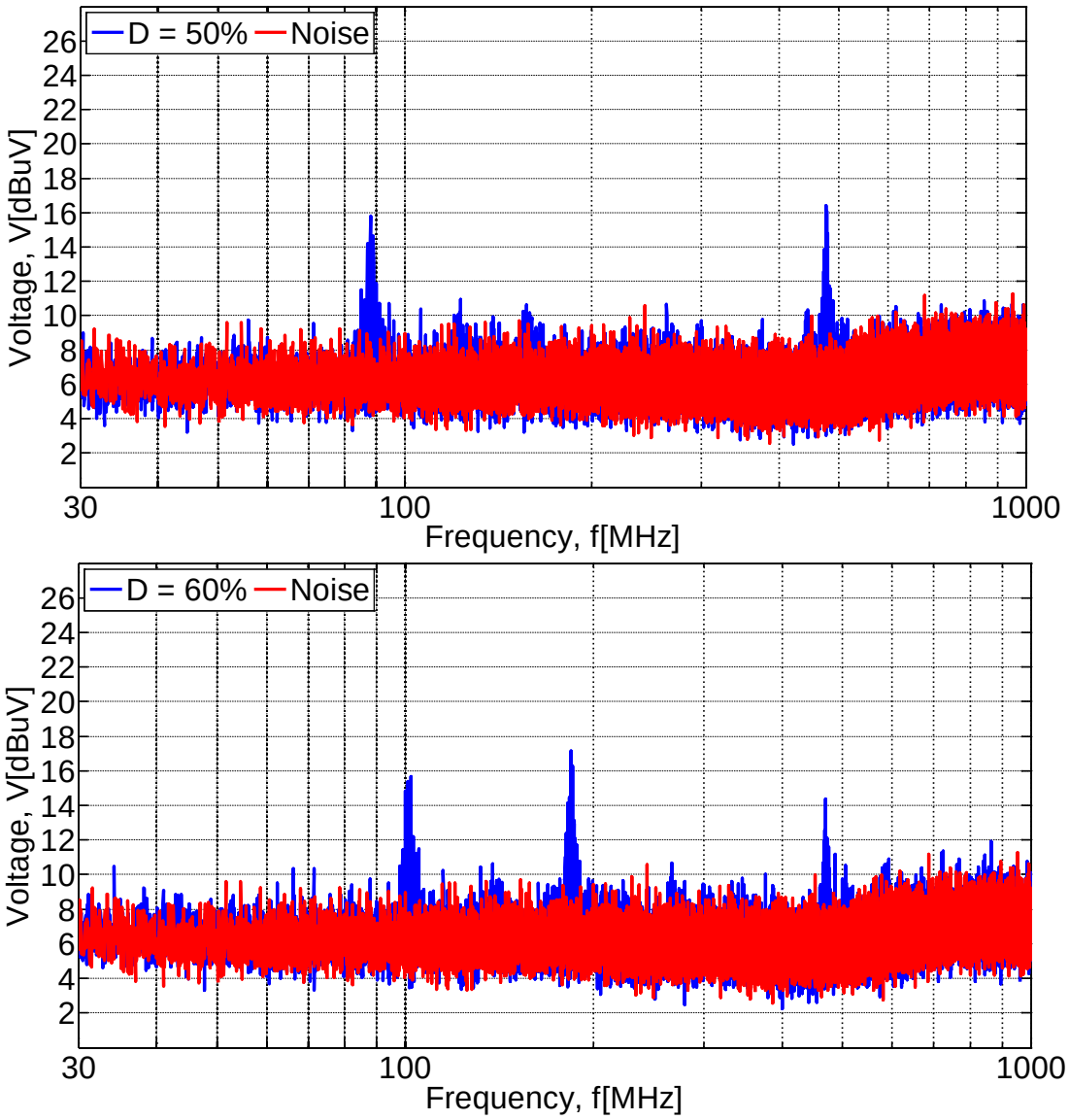
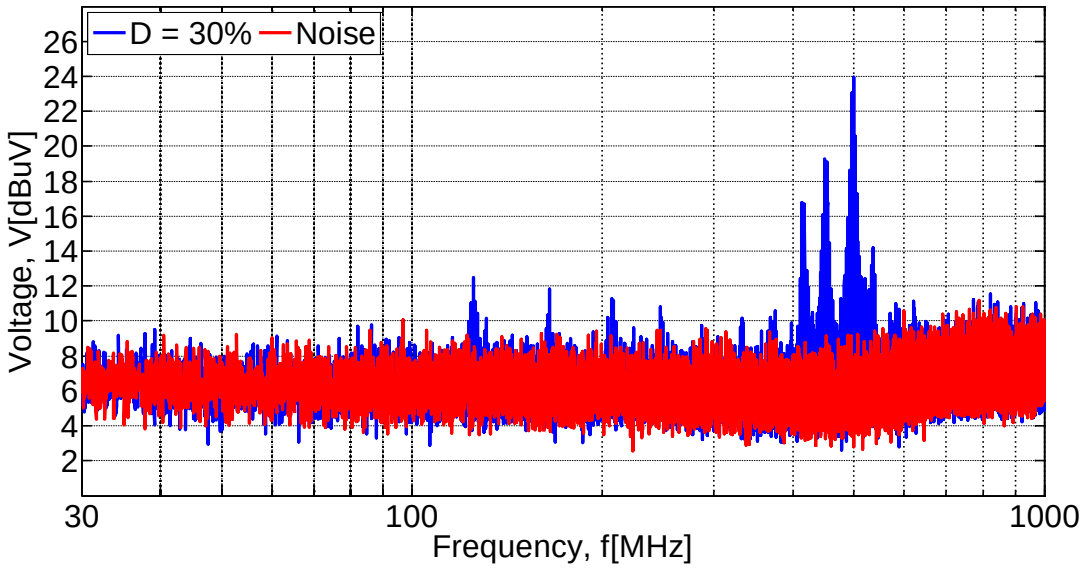
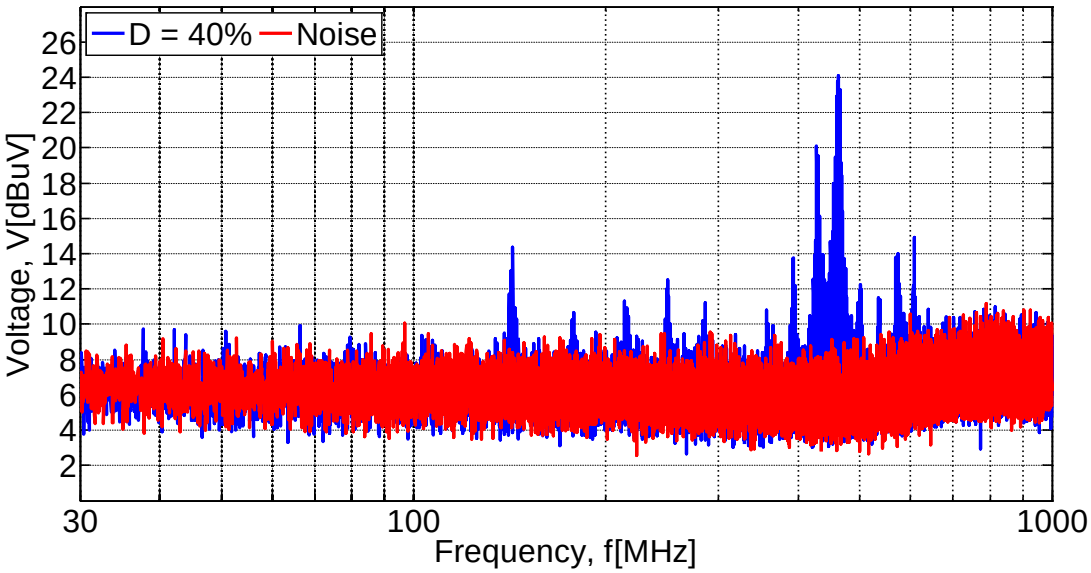


Figure 35 Radiated emissions with vertical position, turned 90º and sum output.


D = 30%
Noise
Voltage, V[dBuV]
26
24
22
20
18
16
14
12
10
8
6
4
2
30
100
1000
Frequency, f[MHz]


D = 40%
Noise
Voltage, V[dBuV]
26
24
22
20
18
16
14
12
10
8
6
4
2
30
100
1000
Frequency, f[MHz]

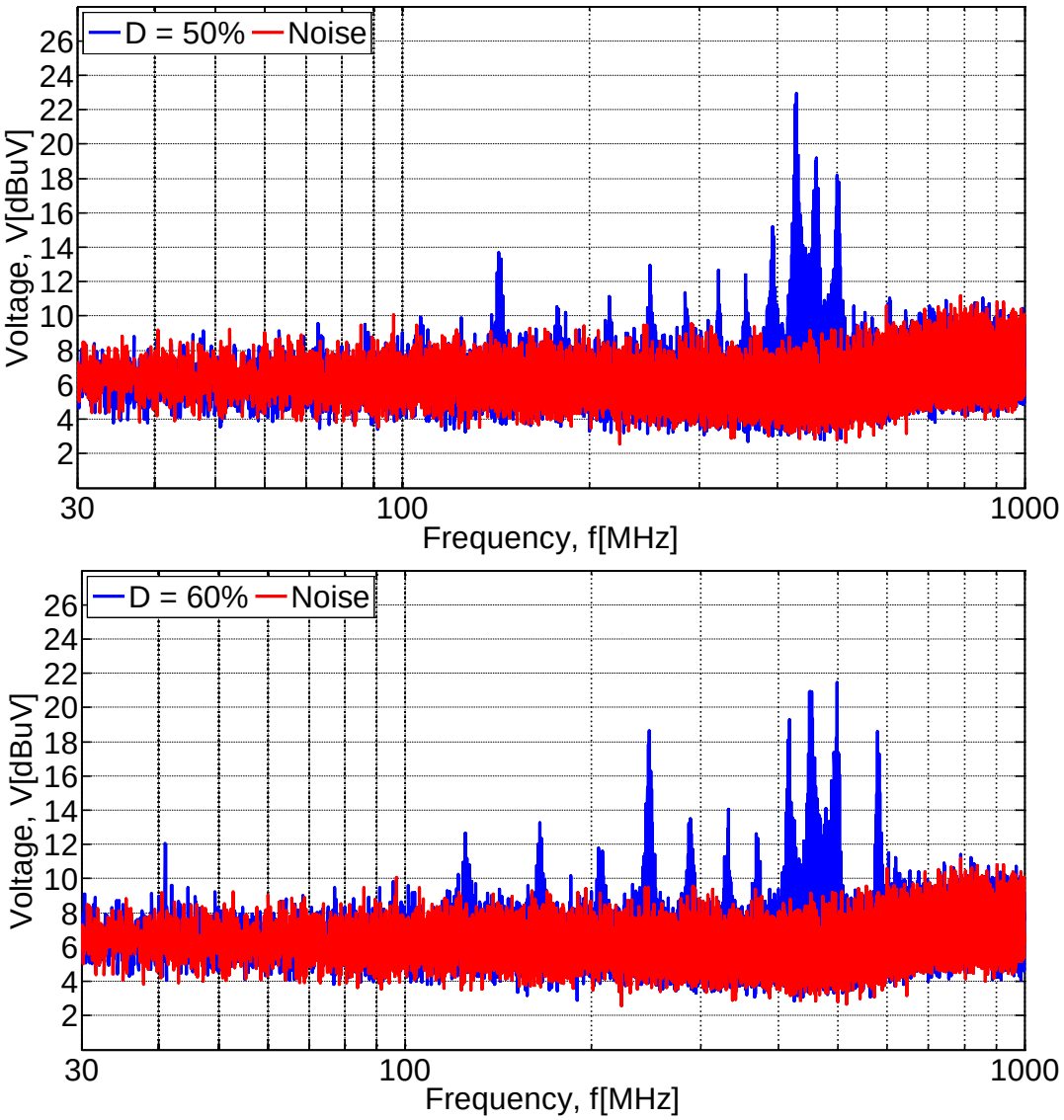


Figure 36 Radiated emissions with vertical position, turned 90º and differential output.

The peaks of different signals are given in Table 11.

RE Test	D = 30%	D = 40%	D = 50%	D = 60%
A1SUM	22.39 dB	19.25 dB	24.40 dB	18.50 dB
A2ISO	17.96 dB	18.43 dB	17.58 dB	15.31 dB
A2SUM	24.33 dB	21.80 dB	23.21 dB	24.46 dB
S2SUM	16.01 dB	14.45 dB	16.43 dB	17.14 dB
S2ISO	23.96 dB	24.11 dB	22.92 dB	21.44 dB

Table 11 Radiated emissions peaks

The results show the radiated emissions of the PCB. It can be observed that the largest peak does not exceed the established limit of 40 dB for the frequency

between 30 and 230 MHz at any time, so it should be noted that the level of radiated emissions is small. Despite the fact that all PCB´s have low emissions, it can be seen that the values decrease when the duty cycle increases, reaching the minimum average values when the duty cycle is 60% and the worst, with a duty cycle of 30%. However, the highest and the lowest peak are reached respectively in the A2SUM measurement for the duty cycle of 60% and in the S2SUM measurement for the duty cycle of 40%.

4.3. Conducted Emissions

This section shows the analysis of the conducted emissions of the designed boards.

Figure 37 shows the set up for the conducted emissions measurement.

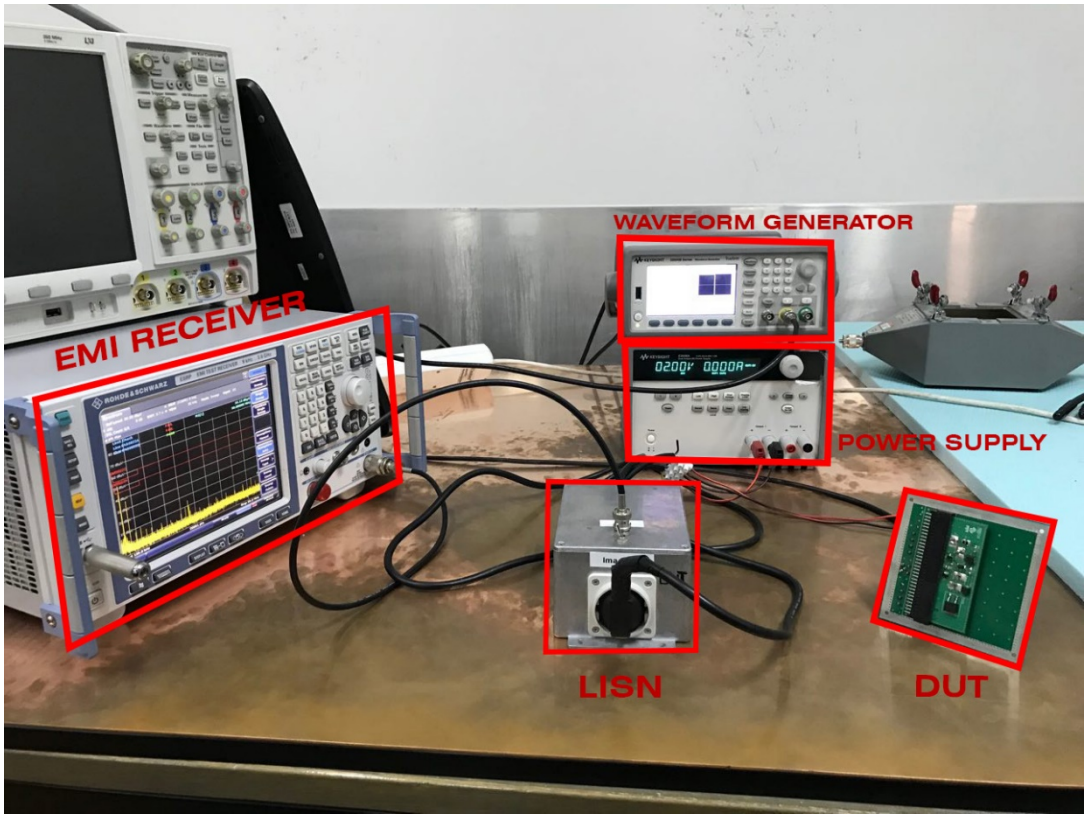


Figure 37 Conducted Emissions measurement set up.

The result for the different boards are plotted by a Matlab script.

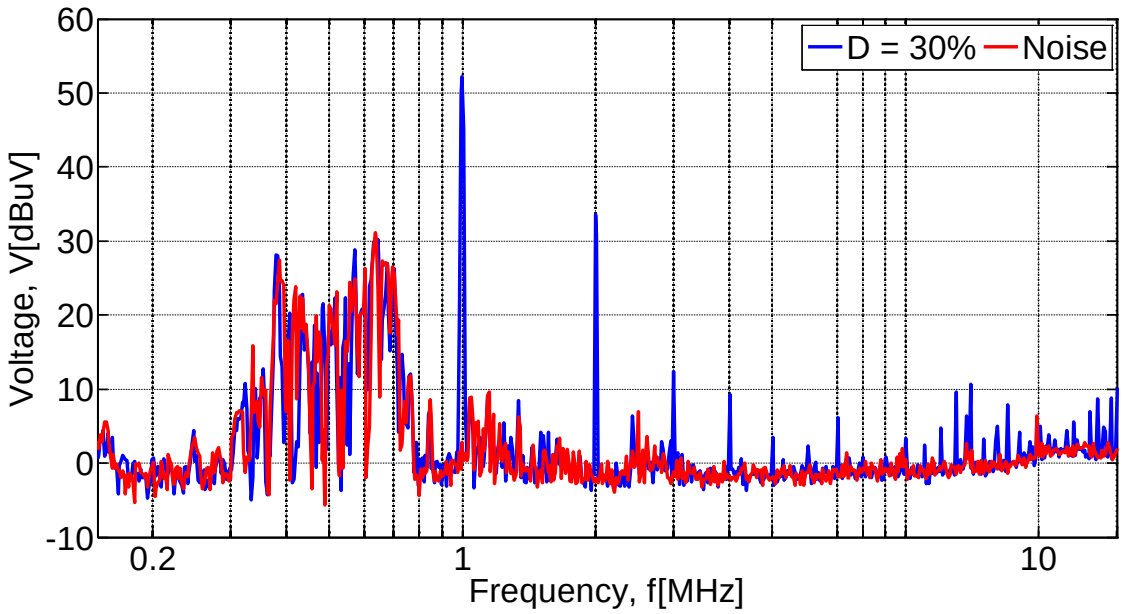


Figure 38 Conducted emissions for D = 30%.

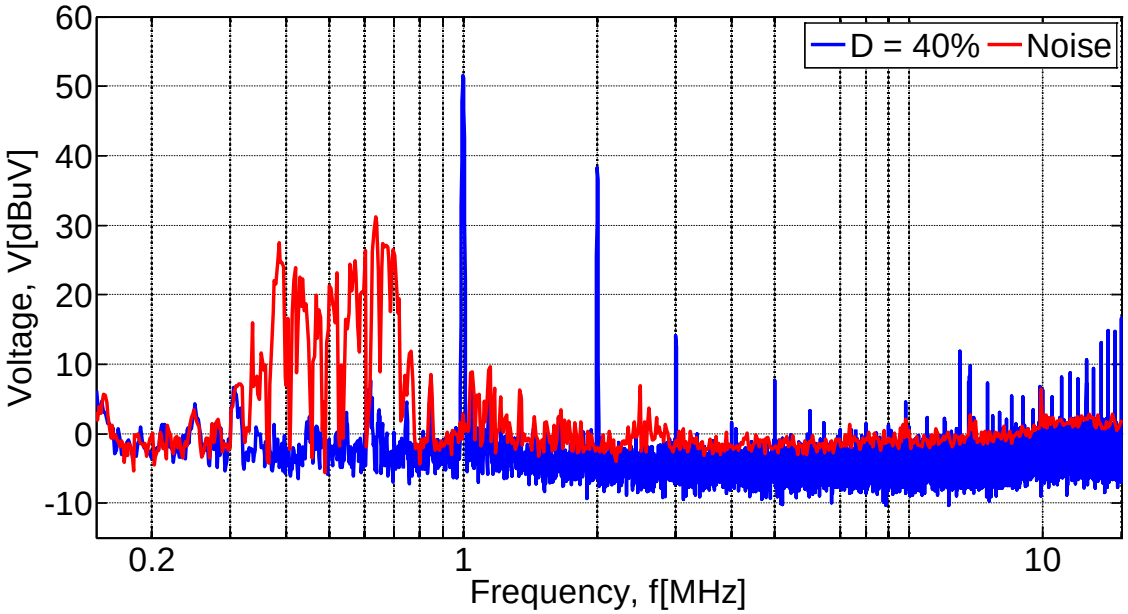


Figure 39 Conducted emissions for D = 40%.

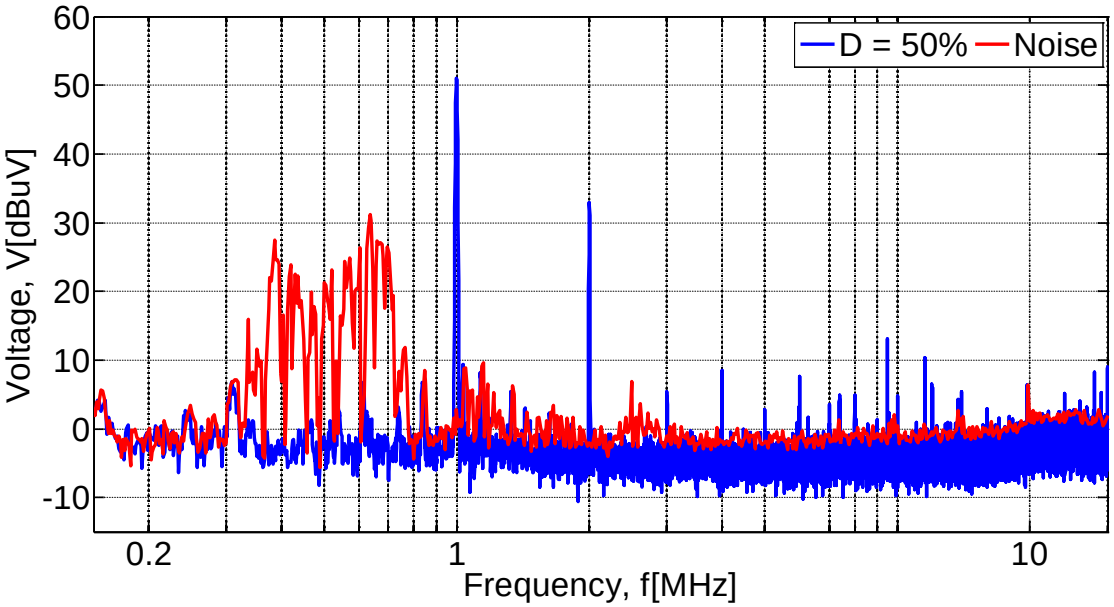


Figure 40 Conducted emissions for D = 50%.

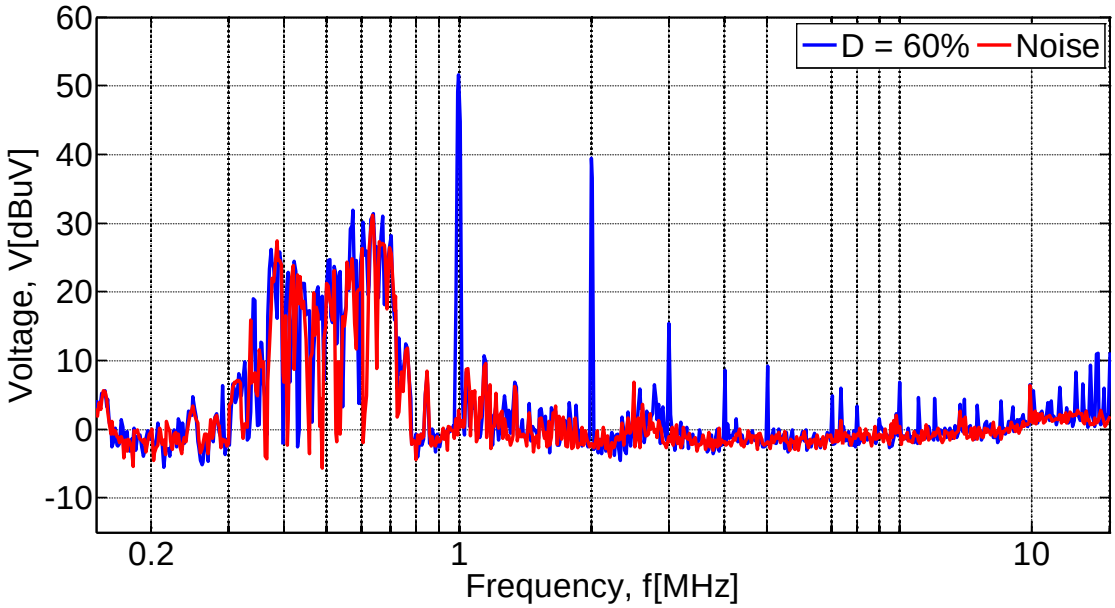


Figure 41 Conducted emissions for D = 60%.

The graph shows the two different duty cycles and the noise. This noise is plotted to notice its influence on the other signals. It should be pointed out that the first three harmonics of each duty cycle are very similar. These values of each duty cycle are given in Table 12.

Harmonic	D = 30%	D = 40%	D = 50%	D = 60%
1st	52.23 dB	51.48 dB	51.06 dB	51.60 dB
2nd	33.60 dB	38.20 dB	32.96 dB	39.50 dB
3rd	12.38 dB	14.11 dB	13.08 dB	15.43 dB

Table 12 Three first harmonics for the CE.

It can be seen how the noise is higher in the boards with duty cycle of 40% and 50%. It is because these measurements are done with another distribution of the cables, so the noise changes and the signal noise which was taken in the first measurement is used in plotting for the boards with duty cycle of 30% and 60%.

Another fact to emphasise, it is how the values of the first harmonics are smaller when the duty cycle increases, without taking into account the board with a duty cycle of 60%, which increases a bit more than the other two boards, but it is still smaller than the 30% of duty cycle. However, this fact does not happen with the other two harmonics, which increase when the duty cycles are higher.

Finally, according to the limit established for the class B products between 0.5-5 MHz is 56 dB, and all boards pass these constrains imposed by the regulations.

5. Conclusion

According to the design of the PCBs, all boards generate waveforms similar to those obtained in the simulations. Only in some cases, as in the current waveform of the convertors with the duty cycle of 60%, 50% and 40% it is higher than expected values. Despite this, it can be considered that the design of the converters is adequate because the waveforms are obtained as expected. However, analysing the results of the efficiency, it can be observed how none of the four PCBs obtains adequate values or the voltage and current output get the values predefined at the beginning of this thesis, for which the calculations of the parameters of the schematic have been made. After researching the possible consequences, it is concluded that the efficiency and the voltage and current output values can be significantly improved if the components are replaced by others components with a lower equivalent series resistance. Another aspect that is considered to improve the performance of the converters is to optimize the Matlab script, through which the parameters of the converter have been obtained.

Regarding the electromagnetic emissions test, the peaks of radiated and conducted emissions do not exceed the established limits. Consequently, in terms of EMC all converters would pass the standard tests. It is thanks to the architecture of the resonant convertors. The only drawback that the boards have presented is the low efficiency. The modification of the components by other components with less equivalent series resistance is left for future work.

References

[1] H. J. Zhang, ’’Basic Concepts of Linear Regulator and Switching Mode Power Supplies’’ Oct. 2013.

[2] Clayton R. Paul, “Introduction to Electromagnetic Compatibility”, New York, NY, USA, Wiley, 2006.

[3] Ippalapalli Sreenivasiah, David C. Chang and Mark T. MA, “Emission Characteristics of Electrically Small Radiating Sources from Tests Inside a TEM Cell” in *IEEE transactions on Electromagnetic Compatibility*, vol. EMC-23, no. 3, August 1981.

[4] N. Bertoni, G. Frattini, R. G. Massolini, F. Pareschi, R. Rovatti and G. Setti, "An Analytical Approach for the Design of Class-E Resonant DC–DC Converters," in *IEEE Transactions on Power Electronics*, vol. 31, no. 11, pp. 7701-7713, Nov. 2016.

[5] P. Wilson, “On Correlating TEM Cell and OATS Emission Measurements” in *IEEE Transactions on Electromagnetic Compatibility*, vol 37, no. 1, Feb. 1995.

Impact of the circuit parameters on the electromagnetic compatibility of a resonant switched-mode power converter

Abstract

This thesis describes the impact of the circuit parameters on the electromagnetic compatibility of resonant switched-mode power converters. Switched-mode power converters are more efficient than linear converters because of which they are used in many different applications. One of the most important disadvantages of switched-mode power converters, and switching circuits in general, are the levels of the generated electromagnetic emissions, which may violate the limits specified in the regulations. Resonant switched-mode power converters generate smaller emission than the hard-switched converters. Four converters are designed. All four converters convert the input voltage of 12 V into the output voltage of 5 V, at the output current of 1 A and at the switching frequency of 1 MHz. The converts differ in the duty cycle. The first one has the duty cycle of 30%, the second one 40%, the third one 50% and the fourth one 60%. The difference in the duty cycle leads to the difference in the circuit parameters and in the generated electromagnetic emissions. The characteristic waveforms in the time domain, the output voltages and the radiated and conducted emissions of the designed converters are shown.

Keywords: resonant switching converters, schematic design, PCB layout, time domain measurements, efficiency of the converters, conducted emissions, radiated emissions.

Impact of the circuit parameters on the electromagnetic compatibility of a resonant switched-mode power converter

Sažetak

U ovom diplomskom radu analiziran je utjecaj sklopovskih parametara na elektromagnetsku kompatibilnost rezonantnih prekidačkih pretvornika snage. Prekidački pretvornici snage su efikasniji od linearnih zbog čega se koriste u raznim aplikacijama. Među najveće nedostatke prekidačkih pretvornika snage, i prekidačkih sklopova općenito, spadaju razine generiranih elektromagnetskih smetnji koje mogu biti veće od zakonski dozvoljenih. Rezonantni pretvornici generiraju manje smetnje od klasičnih prekidačkih pretvornika. Četiri pretvornika su projektirana. Sva četiri pretvaraju ulazni napon od 12 V u izlazni napon od 5 V uz izlaznu struju od 1 A i frekvenciju preklapanja od 1 MHz. Pretvornici se razlikuju u radnom omjeru. Prvi ima radni omjer od 30%, drugi 40%, treći 50% i četvrti 60%. Razlika u radnom omjeru utječe na sklopovske parametre pretvornika, te time i na generirane elektromagnetske smetnje. Karakteristični valni oblici, izlazni napon, te vođene i zračene smetnje projektiranih pretvornika su prikazani.

Keywords: resonant switching converters, schematic design, PCB layout, time domain measurements, efficiency of the converters, conducted emissions, radiated emissions.