Integration of a Very High Quality Factor Filter in Empty Substrate Integrated Waveguide at Q-band

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***Abstract*—Recently, new methodologies for manufacturing empty waveguides completely integrated in a planar substrate have been proposed in order to improve the performance of substrate-integrated devices. One of these alternatives is the so-called Empty Substrate-Integrated Waveguide (ESIW). The height of high-frequency substrates, where ESIW devices are integrated, is very small. Then, the capacity of storing energy of ESIW resonators is drastically reduced, and, as a result, their quality factor is not as high as it could be with a higher ESIW. In order to overcome this restriction, a novel integrated structure is proposed to embed very high-quality factor filters based on ESIW with increased height. As a result we show in this work, for the first time, the successful integration of an increased-height ESIW filter in a printed circuit board (PCB) of 0.305 mm height at Q-band, achieving a quality factor above 1000, which is a remarkable result for a completely substrate-integrated device operating in this frequency band. When compared with the same filter manufactured with an ESIW with the same height as the substrate, the novel filter shows a measured Q-factor 85% higher.**

***Index Terms*—Quality factor, Empty Substrate Integrated Waveguide (ESIW), Substrate Integrated Waveguide (SIW), rectangular waveguide, microstrip transition.**

I. Introduction

In the last years, Substrate Integrated Circuits (SICs) have been developed due to their superior performance, and several solutions have been proposed for integrating non-planar waveguides in Printed Circuit Boards (PCBs). The most popular SIC is the Substrate Integrated Waveguide (SIW) [1].

However, SIW, and other related technologies, present high loss levels. The main cause of losses in SIW devices is the propagation of the electromagnetic fields through the dielectric substrate. Therefore, several strategies to reduce [2] or completely eliminate these losses [3] have been proposed. The Empty Substrate-Integrated Waveguide (ESIW) of [3] consists of a rectangular hole which is emptied in the substrate and then plated. Finally, the structure is closed with two metallic covers that are soldered to the main substrate, thus forming a completely empty and integrated rectangular waveguide. ESIW devices can provide enhanced performance, in comparison to SIW counterparts, in terms of losses and quality factors, at the expense of slightly increasing the size.

At high frequencies, conductor losses increase, which reduces more intensely the performance of resonant devices, as it is the case of bandpass filters. ESIW-based systems are very interesting because they can provide high-quality and completely integrated solutions. In order to preserve this high performance, even at high frequencies, the quality factor of resonant devices should be increased. This could be achieved, for example, if it were possible to increase the height of the integrated waveguides. In this paper, an increased-height ESIW filter has been, for the first time, successfully integrated in a commercial PCB for operation at Q band. The performance of this filter has been experimentally validated and compared to the performance of a standard, i.e. not increased in height [3], ESIW filter. This new kind of high-performance and low-cost filters can be used in many applications such as wireless and space communications.

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II. Integration of increased-height ESIW filters in a PCB

In order to integrate these increased-height filters, a suitable transition has been developed. The transition is composed by the cascade connection of the microstrip to ESIW transition of [4], and an ESIW transformer that changes the height of the integrated waveguide. Therefore, it works as a joint transition between the feeding microstrip lines and a high-profile ESIW waveguide.

The second part of the transition can be achieved using a quarter wavelength transformer. It is well known [5] that the characteristic impedance of a rectangular waveguide is proportional to its height. Then, assuming that the increased height waveguide is composed by N layers, the normalized impedance of the input and output ESIWs can be written as,

$$\overline{Z_{in}} = 1 \; ; \; \overline{Z_{out}} = N \tag{1}$$

where the impedance of the waveguides has been normalized to the feeding waveguide impedance.

Therefore, the impedance of the waveguide that implements the quarter wavelength transformer is $\overline{Z_t} = \sqrt{N}$. Since the ESIW transformer is also implemented with a stack of PCBs, $\overline{Z_t}$ must be an integer value. Therefore, N must necessarily be a perfect square. The first possible value, $N = 4$, has been selected in order to obtain the lowest possible height for the integrated device. Therefore, if the covers that close the guide

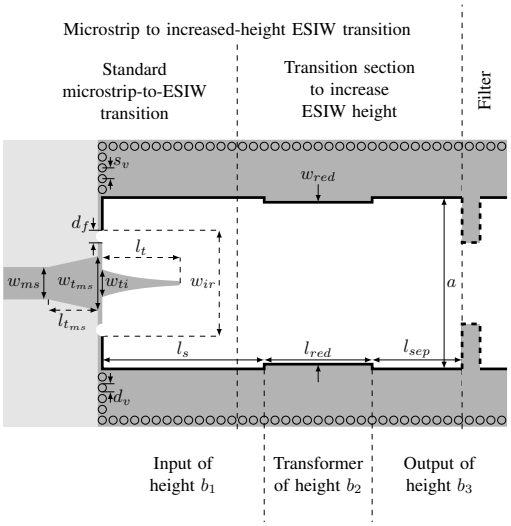


Fig. 1. Proposed microstrip to increased-height ESIW transition that allows the integration of high-performance ESIW filters. Light gray: dielectric substrate. Dark gray: copper metallization on top layer. Black: border metallization used to close the ESIW. White: air.

TABLE I
DIMENSIONS OF THE MICROSTRIP TO ESIW TRANSITION

Fixed parameters		**Tuning Parameters**	
Parameter	Value (mm)	Parameter	Optimized (mm)
a	7.1120	$1/c$	1.4404
h	0.3050	w_{ir}	3.2622
w_{ms}	0.6200	w_{ti}	1.3172
w_{tf}	0.2500	l_t	2.8171
d_f	0.5000	$w_{t_{ms}}$	0.9059
d_v	0.5000	$w_{t_{ms}}$	1.8523
s_v	0.8000		

are taken into account, 6 layers are needed to implement the whole device.

Although it is a good approximation, the previous analysis is not completely accurate. Since the different PCBs are soldered using a tin layer, the total height of the transformer and the output waveguide is not exactly an integer multiple of the input waveguide height, b_1, i.e. $b_1\sqrt{N}$ and $b_1 N$, respectively.

In order to compensate for this slight discrepancy, the width (w_{red}) and length (l_{red}) of the transformer must be modified (see second part of Fig. 1). These dimensions are optimized to provide a minimum reflection coefficient at the center frequency of operation.

A specific transition has been designed following this structure. This transition operates in the Q-band, and has been implemented using a Rogers 4003C substrate of height $h = 0.305$ mm, permittivity $\epsilon_r = 3.55$, metal thickness $t = 27\ \mu m$ (considering both original and galvanic metallizations), and tin soldering layers of 5 μm, which provides a device with a total height of 3.569 mm (including covers of 1 mm height and identical metallization). In order to implement the first part of the transition, the design procedure highlighted in [4] is applied. The optimized dimensions of this part of the transition (see first part of Fig. 1 or [4]) can be seen in Table I.

For the second part of the transition ($l_s = 5$ mm, $b_1 = 0.369$ mm, $b_2 = 0.733$ mm, and $b_3 = 1.461$ mm), the final dimensions for the optimized transformer are $l_{red} = 2.5085$ mm and $w_{red} = 7.0137$ mm.

TABLE II
DIMENSIONS OF THE ESIW FILTER

Parameter	**Value (mm)**	**Parameter**	**Value (mm)**
t	2.0000	w_3	2.7650
a	7.1120	l_1	5.6749
w_1	4.0028	l_2	6.4056
w_2	2.9792	l_3	6.4981

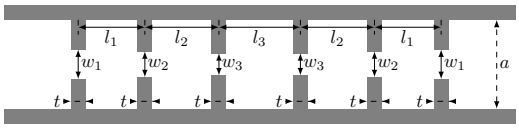


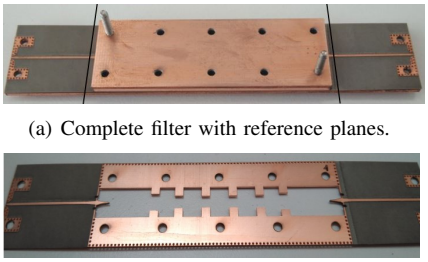
Fig. 2. Layout of the ESIW filter.

In the last step, the transition is used to integrate a specific filter. The final goal of this transition is the integration of an increased-height ESIW filter. In this case a five-pole standard cavity-coupled Chebyshev filter, with 0.01 dB ripple in the passband, centered at 35 GHz, and with 1 GHz bandwidth, has been designed [3], [6]. The layout of the ESIW filter is shown in Fig. 2, and its final dimensions can be seen in Table II.

When the joint transition and the filter are cascaded, they do couple each other. This coupling can be controlled with the distance between the transition and the filter, l_{sep} (see Fig. 1), and with the first inverter of the filter. Then, a last optimization process is performed in order to obtain the best possible interaction between both elements. The optimum values for the optimized parameters are: $l_{sep} = 5.0164$ mm, $w_1 = 3.9743$ mm, and $l_1 = 5.7044$ mm.

III. RESULTS

In order to test the design of the final ESIW filter presented in the previous section, a prototype has been fabricated. Fig. 3 shows two photographs of the manufactured prototype: the complete filter, and the main layer of the device holding the microstrip feedings. In order to de-embed the effect of connectors and microstrip feeding lines, the VNA is calibrated using a custom microstrip calibration kit. With this calibration, the measurement planes are shifted to the beginning of the joint microstrip-to-ESIW transition (see Fig. 3(a)). The scattering parameters of the complete filter, measured in a frequency range from 32 to 38 GHz are represented in Fig. 4, and compared with the CST simulated results. The simulated results have been calculated taking into account the conductivity reduction due to metal roughness. The root mean square (RMS) of the metallic surface roughness has been measured using a SJ-410 surface roughness tester of Mitutoyo, being 0.75 microns. Following the expressions of [7], it has been estimated that the copper conductivity is reduced, because of the characterized roughness, to $1.606 \cdot 10^7\ S/m$ at 35 GHz. Using this corrected conductivity in the filter simulation, one can find a good agreement between simulated and measured values, as it can be seen in Fig. 4.



(a) Complete filter with reference planes.

(b) Main layer with microstrip feeding.

Fig. 3. Manufactured ESIW device.

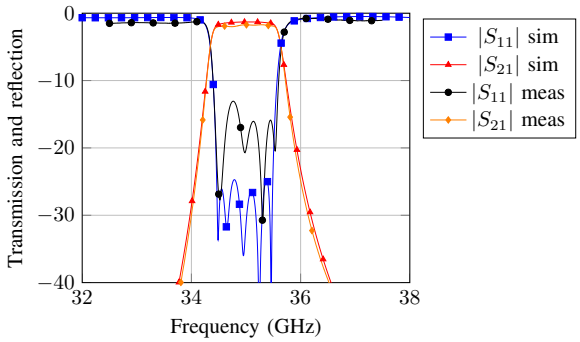


Fig. 4. Comparison between measured and simulated results.

In order to determine the gain in performance that a filter implemented in an increased height ESIW can provide, an ESIW filter with the same response features, but with the same height as the substrate holding the feeding microstrip lines (see [3]), has been fabricated. The measured results of this last filter are shown in Fig. 5, and compared, in the same figure, with the measured S-parameters of the multilayer filter with the novel integration scheme proposed in this paper.

According to the results, the measured values for the losses of the filters are 3.15 dB for the typical ESIW filter, and 1.7 dB for the enhanced device. The quality factor can be obtained from the measurements of the filter as indicated in [8].

For the classical ESIW filter an unloaded quality factor of $Q_u = 379$ is achieved, and $Q_u = 703$ is obtained for the device proposed in this work, which represents an increase of 85% in terms of quality factor. In both cases, the losses of the microstrip to ESIW transitions have been considered in the previous calculations, so that the provided Qs also include the lossy effects of microstrip accessing lines. Considering all these effects, when the integration scheme proposed in this work is used, the total losses at the central frequency are considerably reduced (in 1.45 dB).

Without the first part of the transition (the standard microstrip-to-ESIW transition), the proposed integration scheme can be used to embed a high-profile filter in a larger low-profile ESIW system (using only the second part of the transition of Fig. 1). The insertion loss of the removed part of the transition, i.e. the standard microstrip-to-ESIW transition, is 0.3 dB, according to the simulated results obtained with CST Studio Suite assuming rough copper with reduced conductivity. In this case, the insertion loss of the filter is

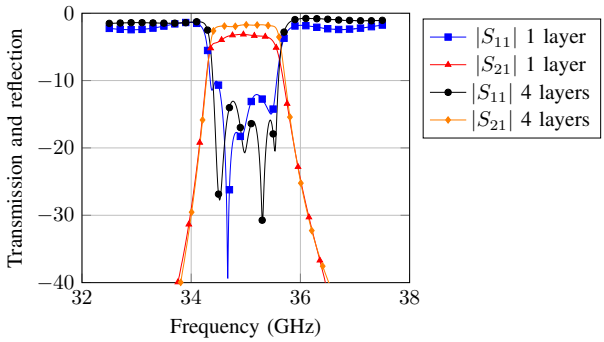


Fig. 5. Comparison between measured results of the typical ESIW single layer filter and the multilayer filter proposed in this paper.

reduced to 1.1 dB, and the integrated filter will be able to provide a quality factor of 1086 (considering the loss effects of low-profile ESIW feeding lines).

IV. Conclusions

In this work, a novel ESIW integration scheme has been proposed. With this novel approach, a high-profile filter with very high-quality factor can be embedded in a microstrip circuit ($Q_u = 703$ at 35 GHz) or, if the scheme is simplified, in a low-profile ESIW circuit ($Q_u = 1086$ at 35 GHz). The insertion losses of the increased-height filter are 1.45 dB smaller than those of the same filter implemented in a single layer ESIW of the same height as the feeding microstrip lines. The proposed transition between ESIWs of different heights may help developing a full range of useful devices, incorporating completely integrated filters with very low insertion loss, very high quality factors, and better power handling capabilities, thus becoming an interesting technique for designing high quality communication devices for operation at very high frequencies with possible applications in wireless and space communications.

References

[1] D. Deslandes and K. Wu, "Integrated microstrip and rectangular waveguide in planar form," *IEEE Microwave and Wireless Components Letters*, vol. 11, no. 2, pp. 68–70, February 2001.

[2] F. Parment, A. Ghiotto, T. P. Vuong, J. M. Duchamp, and K. Wu, "Air-filled substrate integrated waveguide for low-loss and high power-handling millimeter-wave substrate integrated circuits," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 4, pp. 1228–1238, April 2015.

[3] A. Belenguer, H. Esteban, and V. Boria, "Novel empty substrate integrated waveguide for high-performance microwave integrated circuits," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 4, pp. 832–839, April 2014.

[4] H. Esteban, A. Belenguer, J. R. Sánchez, C. Bachiller, and V. E. Boria, "Improved low reflection transition from microstrip line to empty substrate-integrated waveguide," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 8, pp. 685–687, Aug 2017.

[5] M. Sisodia and V. Gupta, *Microwaves : Introduction to Circuits,Devices and Antennas*. New Age, 2001.

[6] R. E. Collin, *Foundations for Microwave Engineering*, 2nd ed., ser. Electromagnetic Wave Theory. IEEE Press, 2001.

[7] T. Liang, S. Hall, H. Heck, and G. Brist, "A practical method for modeling PCB transmission lines with conductor surface roughness and wideband dielectric properties," in *2006 IEEE MTT-S International Microwave Symposium Digest*, June 2006, pp. 1780–1783.

[8] J.-S. Hong and M. J. Lancaster, *Microstrip Filters for RF/Microwave Applications*. John Wiley & Sons, Inc., 2001.