

Versatile Transition for Multilayer Compact Devices in Empty Substrate Integrated Waveguide

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Abstract—Empty substrate integrated waveguide (ESIW) devices can provide high quality and completely integrated devices, but they are usually larger than the same ones implemented with alternative technologies. One of the most extended strategies to compact electronic devices is the use of multilayer technology. Nevertheless, to perform multilayer devices in ESIW, a versatile and efficient transition between the guides in different layers is needed. Currently, only one multilayer device is known in this ESIW technology, which is a transition between a pair of guides built in contiguous layers that requires complex and nonstandard 3-D manufacturing processes. In this letter, a multilayer transition to connect a pair of guides separated by an arbitrary number of layers is successfully designed and experimentally validated without 3-D manufacturing processes. This novel and versatile transition opens the way to further develop multilayer compact devices in the ESIW technology such as compact filters.

Index Terms—Empty substrate integrated waveguide (ESIW), multilayer, transition.

I. INTRODUCTION

BELENGUER *et al.* [1] proposed the empty substrate integrated waveguide (ESIW), where an empty waveguide is integrated within a dielectric substrate. This technology retains the main features of the SIW [2], such as low cost, easy manufacturing, small size, and integration with other circuits, in the same substrate. Moreover, since the dielectric is removed in the ESIW circuits, better performance (mainly in terms of insertion losses) is obtained than with the SIW technology.

Next, a suite of different ESIW devices were designed and manufactured. Some examples are high-quality filters [1], couplers [3], [4], antennas [5], and a thru-reflect-line calibration kit [6]. All these important ESIW prototypes have one thing in common, i.e., they are all single layer devices.

However, multilayer devices would be able to achieve higher degrees of compactness. But, in order to develop such kind of devices, a versatile and efficient transition between ESIWs in

different layers is needed. In [7], a transition between ESIWs in contiguous layers was presented. But its application for connecting noncontiguous ESIWs with a separation of more than one layer would require the continuous concatenation of several versions of this transition, resulting in a bulky device losing compactness. Besides, this transition requires 3-D manufacturing processes, so that it cannot be developed using the standard printed circuit board (PCB) fabrication procedures.

In this letter, we propose a highly versatile and compact multilayer transition that can connect ESIWs separated more than one layer, whose fabrication is not based on 3-D manufacturing techniques. In fact, this versatile transition can be entirely manufactured using the standard PCB manufacturing processes, i.e., cutting, drilling, milling, plating, and soldering.

II. TRANSITION STRUCTURE

The layout of the transition is shown in Fig. 1(a). Layers 2 and 8 are the input and the output ESIW lines. The two transition layers (layers 3 and 7 in Fig. 1) must be present to ensure good matching between the input and output lines. But an arbitrary number of vertical layers [layers 4–6 in Fig. 1(a)] can be inserted between the two transition layers without degradation in the performance of the transition, since the vertical layers form a vertical ESIW. As a result, this structure can be used to connect an ESIW to another ESIW located in any other layer of a vertical stack, and the compactness does not depend on the vertical separation of the ESIW lines.

III. TRANSITION DESIGN

The transition versatility relies on the vertical ESIW line, which is formed with the vertical layers. Since this is, in fact, a vertical guide, reducing or increasing its length (the actual number of vertical layers) barely affects the behavior of the overall transition. The challenge is, then, to find an appropriate structure to transfer the electromagnetic fields from a typical horizontal ESIW line to a vertical one. In a first attempt, a simple E -plane 90° bend was tried, but with a poor performance. A pair of cascaded 45° bends could provide the desired performance, but it is not possible to perform oblique cuts with the traditional PCB fabrication procedures. However, it is possible to approximate oblique walls [depicted with dashed lines in Fig. 1(b)] with consecutive vertical cuts separated with a regular distance in the horizontal dimension, in the same manner as tapered walls are approximated in a corrugated horn. This is the purpose of the so-called transition layers, providing a low reflection connection between the horizontal and vertical

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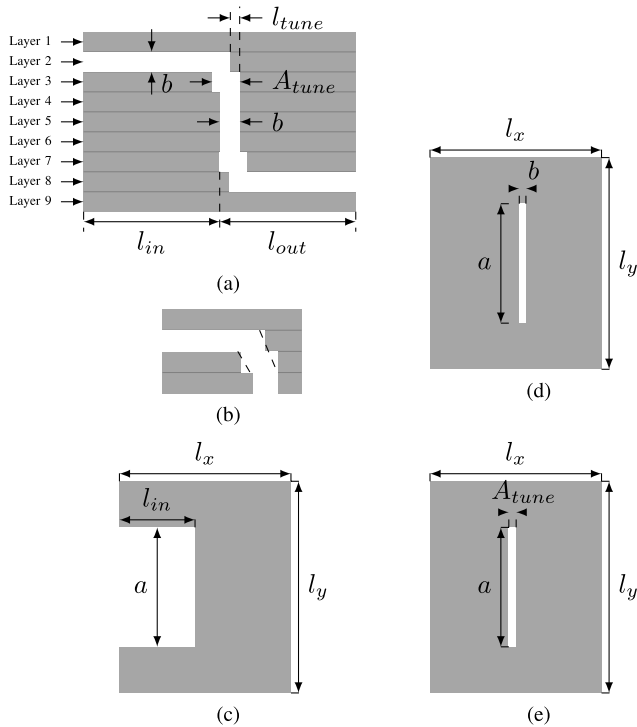


Fig. 1. Layout of the multilayer transition. (a) Longitudinal cut. (b) Bend detail. (c) Layer 2 and out 8. (d) Vertical layers (4–6). (e) Transition layers (3 and 7).

ESIWs with a response very close to that of a pair of cascaded 45° E -plane bends, whose equivalent circuit can be found, for example, in [8]. In order to control the position of the vertical cuts along the horizontal dimension and, in this way, maximize the return loss value in the frequency range of interest, parameters A_{tune} and l_{tune} are optimized (see Fig. 1). Since the optimization is quite simple (only two degrees of freedom), almost any optimization algorithm can be used. We have employed Computer Simulation Technology Design Studio 2014 to optimize the transition using the trust region framework algorithm. Based on the results of the optimization for different situations, we have derived good initial values for these parameters ($l_{\text{tune}} = 0.25 \cdot b$; $A_{\text{tune}} = 1.25 \cdot b$) that can be used in order to speed up the optimization process.

In order to validate the proposed transition, it has been designed for an ESIW line of $a = 15.7988$ mm width, which covers the entire Ku -band (12–18 GHz). This transition has been fabricated using a Rogers 4003C substrate of 0.813 mm height and copper metallization of $18 \mu\text{m}$. Since an ESIW is metallized, an additional copper layer is added. The height of the electrodeposited copper is $9 \mu\text{m}$. Finally, the different layers are soldered using tin solder paste. The height of the soldering is not negligible, around $5 \mu\text{m}$. All these contributions have been considered in the calculation of the total height of ESIWs [b in Fig. 1(a)]. The alignment of the different layers is guaranteed by a set of alignment holes that are also used to hold and press the whole structure in the soldering stage. After the solder paste is dried in a reflow oven, the screws can be removed.

After applying the design procedure detailed in the beginning of this section, the final dimensions for this particular

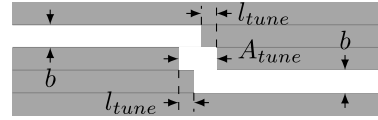


Fig. 2. Special case of a transition between a pair of ESIWs separated by a single layer.

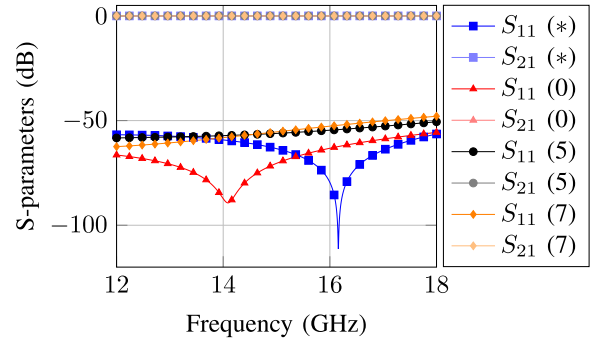


Fig. 3. Simulation results for different number of layers.

transition are $a = 15.7988$ mm, $b = 0.881$ mm, $l_{\text{in}} = l_{\text{out}} = 10$ mm, $l_x = 45.3778$ mm, $l_y = 39.05$ mm, $A_{\text{tune}} = 0.9708$ mm, and $l_{\text{tune}} = 0.4114$ mm.

The transition between a pair of ESIWs separated by a single layer can be considered as a special case, since it cannot be directly obtained from the general structure that has been presented in Section II, which requires at least two transition layers. In order to build this transition, only one transition layer is used (see Fig. 2), so the optimized values of A_{tune} and l_{tune} for the general transition are no longer valid, and have to be optimized specifically for this single layer separation case. The values of these parameters for the same substrate in the Ku -band described earlier, are $A_{\text{tune}} = 1.022$ mm and $l_{\text{tune}} = 0.424$ mm.

IV. SIMULATION

The transition has been simulated with two transition layers and a different number of vertical layers (0, 5, and 7). In all these cases, $A_{\text{tune}} = 0.9708$ mm and $l_{\text{tune}} = 0.4114$ mm. No microstrip-to-ESIW transition has been considered in the simulation. Fig. 3 shows the simulation results, where it is possible to observe the good performance of the transition, with return loss levels of below 50 dB and negligible insertion losses. The case with only a single transition layer ($A_{\text{tune}} = 1.022$ mm and $l_{\text{tune}} = 0.424$ mm) has also been simulated and included in Fig. 3 [results with (*) in the legend], obtaining also the excellent results for return and insertion losses.

V. MANUFACTURING

To test the goodness of the designed transition, three different versions have been manufactured with two transition layers and different number of vertical layers (0, 1, and 5) [Fig. 4(a)]. Fig. 4 shows the manufactured prototype before assembling. The layers are arranged according to their position within the stack. The bottom layer appears on the left of Fig. 4, and the

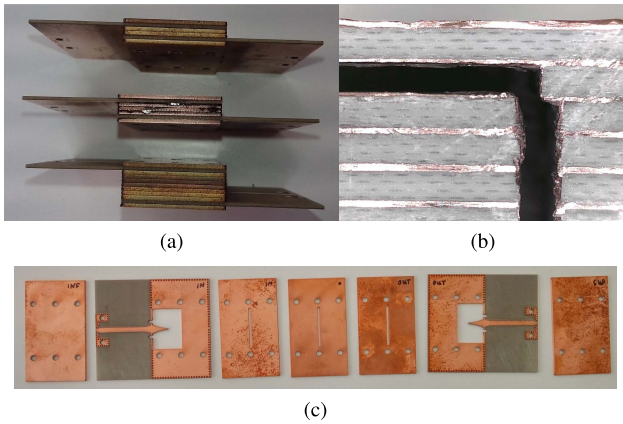


Fig. 4. Manufactured prototypes and assembling process. (a) Manufactured prototypes. (b) Bend detail. (c) Prototype with one vertical layer before assembling. Layers from left to right are stacked from bottom to top.

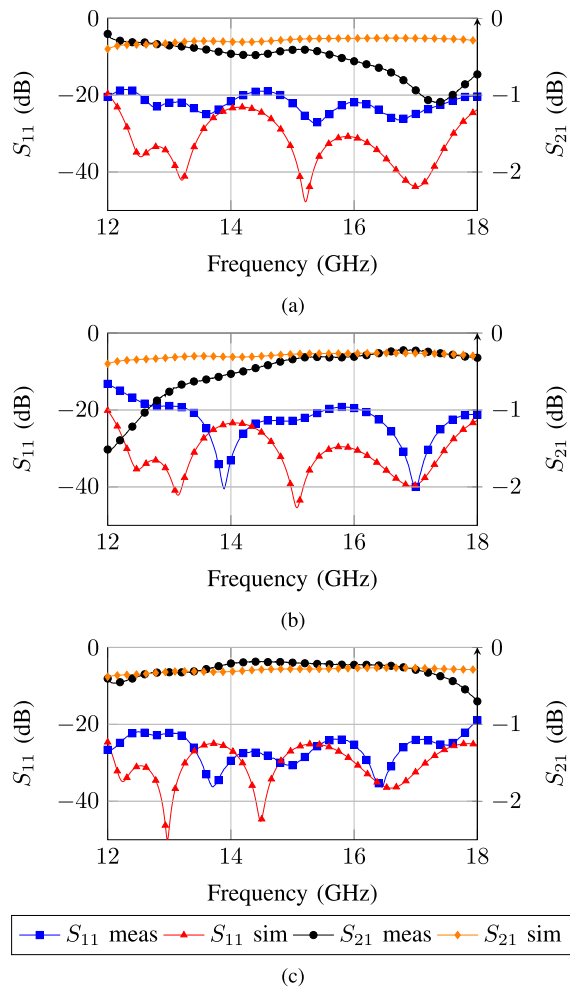


Fig. 5. Results obtained for the manufactured transitions. (a) Without vertical layers. (b) With one vertical layer. (c) With five vertical layers.

top layer on the right. The assembling process starts stacking the bottom cover and the bottom ESIW line, followed by the desired number of vertical layers [central layer in Fig. 4(c)], depending on the number of layers of the device, and finally, the top ESIW line and the top cover. All the layers have been drilled with holes for alignment screws that are removed when the soldering paste is dried.

VI. RESULTS

Once assembled, the prototypes of Fig. 4 have been measured with a network analyzer Anritsu MS4644A. The results obtained are shown in Fig. 5. Measured return losses are around 20 dB and insertion losses are below 1 dB in all the usable frequency band of the considered examples. These measurements include the effect of the microstrip-to-ESIW transitions that allow the connection of the prototype to the vector network analyzer (VNA).

Fig. 5 also shows the comparison with the simulated versions of the manufactured transitions (including microstrip-to-ESIW transition in all cases), where a good agreement between simulated and measured results can be observed.

VII. CONCLUSION

A transition for multilayer ESIW circuits has been presented. There are some advantages of this interlayer transition: it is highly versatile, does not require 3-D manufacturing, is easy to manufacture, and can connect ESIWs separated more than one layer, allowing the design of multilayer circuits with an arbitrary number of intermediate layers such as compact filters. In this letter, a modification of the transitions has also been presented that successfully connects ESIW lines separated only by one layer. Three prototypes have been manufactured, obtaining, in all cases, return losses around 20 dB and insertion loss values below 1 dB. These results include the effect of the microstrip-to-ESIW transitions that allow the connection of these devices to the VNA. These results are almost identical to those expected for a direct back-to-back connection of a pair of microstrip-to-ESIW transitions (see [9]). Therefore, it can be concluded that the distortion produced by the versatile multilayer transition is almost negligible, which is certainly the desired result.

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