UNIVERSITAT POLITÈCNICA DE VALÈNCIA

Escuela Técnica Superior de Ingeniería del Diseño

DESIGN AND IMPLEMENTATION OF AN SDR TRANSCEIVER

Final Undergraduate Project

Bachelor's Degree in Industrial Electronics and Automation Engineering

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TNO innovation for life

ABSTRACT

Software-defined-radio technology (SDR) is found interesting due to its adaptability characteristics. SDR devices offers the opportunity for having radio communication equipment which is software upgradeable and reconfigurable, increasing its lifetime when compared to conventional equipment. In the military domain, missions and technical requirements vary fast, so equipment able to adapt their communications to different protocols and waveforms are highly demanded.

The present Bachelor's Final Project has been conducted in collaboration with the Electronic Defense department of TNO (The Hague, the Netherlands) as an internship program.

The purpose of this project is to present the preliminary design and development of a hardware implementation for an SDR-based equipment, where miniaturization, performance optimization and use of cost-efficient components are pursued.

The dissertation goes through the procedure carried out, including the selection of the main components in the setup and the design process, manufacturing and implementation of a printed-circuit board in charge of the power supply management.

RESUMEN

La tecnología de radio definida por sofware (SDR, del inglés *software defined radio*) resulta interesante porque gracias a sus características, los dispositivos SDR ofrecen la oportunidad de tener equipos de radiocomunicación capaces de ser actualizados y reconfigurados via software, dotando a estos de una vida útil más larga que la de los equipos convencionales. En el ámbito militar, donde las misiones y los requerimientos técnicos varían rápidamente, los equipos que pueden adaptar las comunicaciones a distintos protocolos y formas de onda son altamente demandados.

El presente Trabajo Fin de Grado se ha realizado en colaboración con el departamento de *Electronic Defense* de la empresa TNO (La Haya, Países Bajos) en calidad de prácticas.

El propósito de este proyecto es presentar el diseño preliminar y desarrollo de una implementación en hardware para un equipo de SDR cuyo diseño persiga la miniaturización, la optimización del funcionamiento y el uso de componentes económicos.

La memoria recoge el procedimiento llevado a cabo, que incluye la elección de componentes que incluiría la configuración final, así como el proceso de diseño, fabricación e implementación de una placa de circuito impreso responsable de controlar y alimentar el sistema.

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LIST OF ABBREVIATIONS

ADC	Analog-to-digital converter
BOM	Bill of materials
DAC	Digital-to-analog converter
DC	Direct current
DDC	Digital down converter
DSP	Digital signal processing
DUC	Digital up converter
EOS	Electrical over-stress
ESD	Electrostatic discharge
ESR	Equivalent series resistance
GRC	GNU Radio Companion
IC	Integrated circuit
IF	Intermediate frequency
LDO	Low dropout
MIMO	Multiple-input and multiple-output
MLCC	Multi-layer ceramic capacitor
MMIC	Monolithic microwave integrated circuit
P1dB	1 dB compression point
PA	Power amplifier
PCB	Printed circuit board
PSRR	Power supply rejection ratio
RF	Radio frequency
SBC	Single board computer
SDR	Software defined radio
SMD	Surface-mount device
UVLO	Under-voltage lockout
VAT	Value added tax

I. DISSERTATION

1. INTRODUCTION

From an Electronic Defense perspective, it is relevant to know exactly what kind of signals are being transmitted within the electromagnetic spectrum. For this, it is required to gather information about who or what is transmitting, what information is being sent and what the location of the transmitter is. Signals can be transmitted for a wide range of reasons, including radar, communications, and navigation. As a basis for analyzing activities in the spectrum, use is made of software-defined radio (SDR). This technology makes radiofrequency (RF) hardware easier, it facilitates the addition of new features, since they are all in software, and it is more convenient to have one set of hardware handling multiple modulation techniques.

This project has been developed in the context of an internship at the Electronic Defence department of TNO (The Hague, the Netherlands). The motivation behind it is to illustrate the flexibility and versatility of SDR technology in a Safety and Security context with a demonstration setup that shows the potential of small, experimental and cost-effective components.

1.1. OBJECTIVES

On the basis of the software already available at TNO, a hardware implementation capable of transmitting RF signals relevant to the domain "Defense and Security" shall be designed and built. Given a squared field of 100 km², these signals have to be detected from any point in this area, wherever the device is located.

Setting a reasonable objective, the full implementation will not be pursued within the scope of the internship. However, the selection of the main components and the design of the power supply circuit board is aimed to be achieved, as a product or demonstration that can be shown to the client.

1.2. METHODS

To study and develop the hardware for this experimental SDR technology, the project proceeded through the following stages:

- Familiarization with SDR technology
- Definition and record of the functional requirements
- Proposal of the desired solution

- Research and selection of the required components
- Development and assembly of the power printed circuit board

Every stage will be duly documented and justified.

1.3. STRUCTURE OF THE PROJECT

The project is divided into four documents: dissertation, quotation, tender specifications and schematics.

The dissertation is organized into 7 chapters, bibliography and appendixes:

- *Introduction*. In Chapter 1 the objectives of this BSc Final Project are described. This chapter further gives an overview of the followed methodology.
- *Technological context.* Chapter 2 gives a review of the SDR technology.
- *Analysis.* In Chapter 3 global system requirements are identified.
- *Design of the proposed system.* Chapter 4 presents the elements that constitute the design.
- *Printed circuit board development.* Chapter 5 goes through the PCB design process.
- *Printed circuit board implementation.* Chapter 6 includes the PCB assembly and other laboratory work.
- *Conclusions.* Chapter 7 compares the initial objectives with the outcomes and gives recommendations for future work.
- *Bibliography.*
- *Appendix A: About TNO.*
- *Appendix B: Bill of materials.*

The quotation reflects the economic cost of the project.

The standards and regulations document includes the minimum technical conditions and regulations that are complied with during the development of the project.

The technical drawings contain the extra graphical information required to understand the project that has not been included in the dissertation.

2. TECHNOLOGICAL CONTEXT

2.1. SOFTWARE-DEFINED RADIO

Software-defined radio refers to wireless communication in which the transmitter modulation is generated or defined by a computer. The receiver then also uses a computer to recover the information signal. The primary goal of SDR is to replace as many analog components and hardwired digital devices of the transceiver as possible with programmable devices [1]. The two major advantages of SDR are flexibility to incorporate new functionalities and upgrades, and ease of adaptation to different standards [2].

2.1.1. Ideal concept

Joseph Mitola defined the term software-defined radio as a type of radios that could be reprogrammed and reconfigured through software. The ideal SDR (Fig. 1) was envisioned as a device composed of an antenna and an analog-to-digital converter (ADC) on the receiver side. Likewise, the transmitter would have a digital-to-analog converter (DAC) and a transmitting antenna. The rest of the functions would be handled by reprogrammable processors [3].

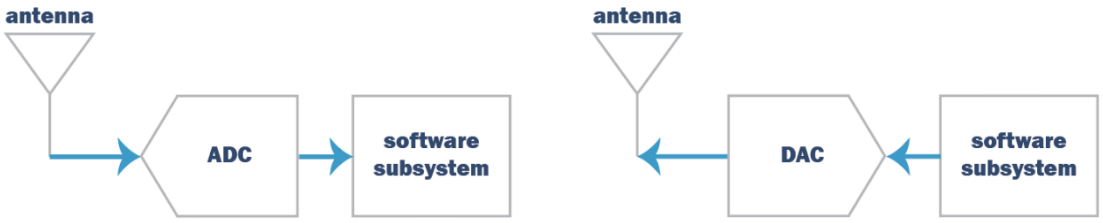


Figure 1. Ideal SDR hardware. Receive and transmit signal paths

The ideal scheme is not completely realizable due to the current limits of the technology. The main problem in both directions is the difficulty of conversion between the digital and the analog domains at a high enough rate and a high enough accuracy at the same time, and without relying upon physical processes like interference and electromagnetic resonance for assistance. To be specific, the digital signal processors are not fast enough to implement all radio functions.

For this reason, current SDR systems include an additional digital-conversion stage, down conversion in receivers and up conversion in transmitters. Its function is explained in the next section.

2.1.2. SDR hardware

2.1.2.1. SDR receiver

Figure 2 shows the block diagram of a SDR receiver.

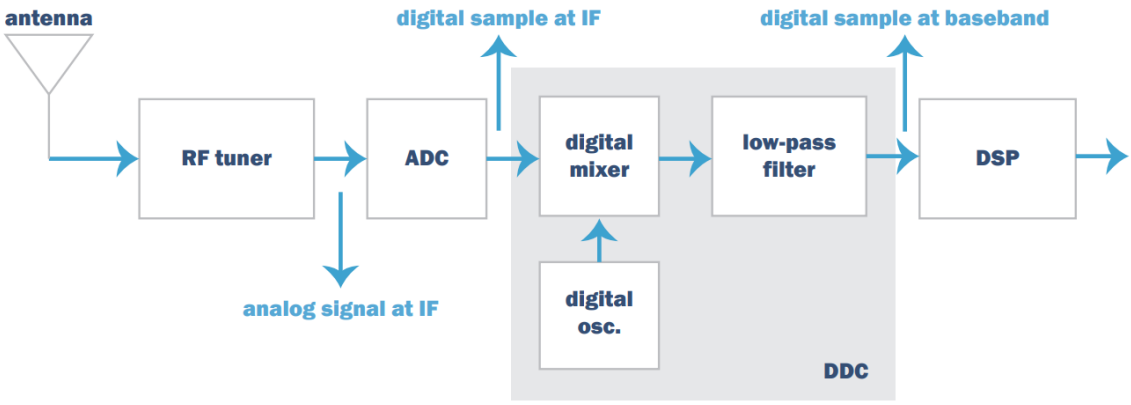


Figure 2. SDR receiver

At first, the RF tuner converts the analog signal to intermediate frequency (IF). Next, the IF signal is passed to the ADC converter in charge of changing the signal's domain, offering digital samples at its output. The samples are feed to the following stage's input which is a digital down converter (DDC). The DDC is commonly part of the SDR system. It consists of three main components: a digital mixer, a digital local oscillator, and a finite impulse response low-pass filter. The DDC shifts the IF digital samples to baseband, while limits the bandwidth of the final signal.

Another procedure, known as decimation, is commonly performed for reducing the sampling frequency or sample rate. Thus, the new sampling frequency in baseband results from the division of the original sampling frequency by an N factor, called decimation factor. The final sample rate can be as little as twice the highest frequency component of the useful signal, as proposed by the Nyquist theorem.

Finally, the baseband samples are passed to the digital signal processing (DSP) block, where tasks such as demodulating and decoding are performed.

DPS stages are commonly found within a general-purpose computer in the form of specialized software if versatility is to be added to the solution.

2.1.2.2. SDR transmitter

SDR transmitters receive a baseband signal as an input, typically generated by a DSP step as it is shown in figure 3.

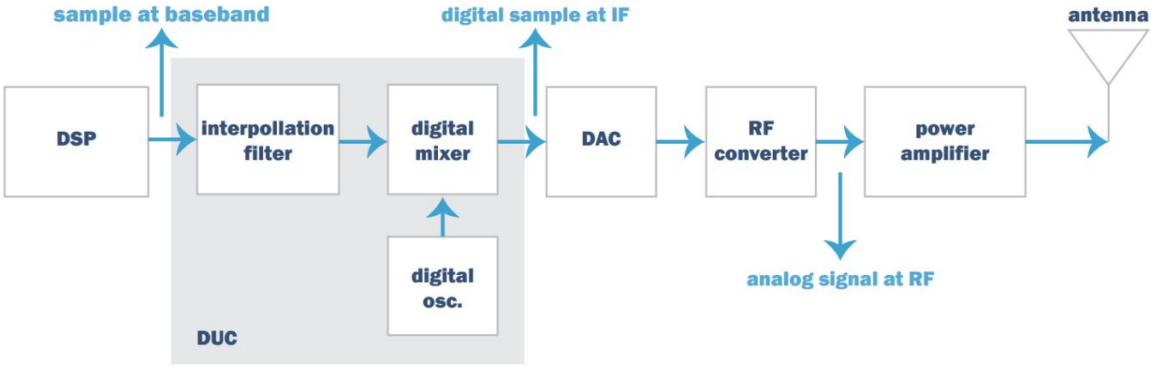


Figure 3. SDR transmitter

The first block is a digital up converter (DUC) which transfers the baseband signal to IF. The DAC that follows transform the samples to the analog domain. Next, the RF converter shifts the signal towards higher frequencies. Finally, the signal is amplified and directed to the antenna.

Within the DUC, the Interpolation Filter is responsible for raising the baseband signal's sample rate to match the operating frequency of the components that follow. Therefore, it performs the Decimator's opposite operation in the receiver's architecture.

Then, the digital mixer and the local oscillator shift the samples to IF, the sight being controlled by the local oscillator.

2.1.3. SDR software

While the hardware components are essentials in the SDR conception, the definition of the SDR points out the necessity of complementary dedicated software. A proper framework must be created providing low/level interface functions before developing software for enabling the interaction.

GNU Radio and MATLAB are the most used support frameworks in SDR investigation. Their success mainly resides in the fact that they provide easy to handle tools for the manipulation of signals.

2.1.4. *Enabling technologies*

Since the SDR itself is an emerging technology, its prospects are related to other important emerging technologies such as smart antennas, networking, software, semiconductors, signal processing and battery technology.

Advances in SDR development have provided impetus for ADC and DAC performance improvements, due to the importance of these components, whose technology has not reached, as stated before, high enough sample rates and accuracy yet.

Also, digital signal processors play a prominent role in SDR. Traditionally, DSP techniques were used for pre/modulation and post/detection functions in radio receivers. In recent times, DSP techniques have been used extensively for advanced digital communications transceiver designs, finding their way into detection, equalization, demodulation, frequency synthesis and channel filtering. Processors are evolving by being integrated with microcontrollers, getting net functions and specialized accelerators. Programmable processors are used for all functions possible within the current state of the art.

Although the ideal SDR has a set of features that are not yet attainable in commercial systems due to limitations in current technology and cost considerations, the increased performance and continually dropping costs of the enabling technologies of ADCs and DACs, high speed digital signal distribution, DSP chips and embedded computing are facilitating a shift toward software intensive approaches.

2.2. APPLICATIONS

SDR technology covers a wide spectrum of applications: RF test equipment and instrumentation, communications and telemetry equipment, communications infrastructure and general SDR radio platforms, inter alia.

In military communications, SDR is one of the main topics of interest. For defense electronics (radar, handheld and manpack battlefield radios), flexibility and mobility have always been valuable. SDR technology can support the development and evolution of new waveforms and allow a single platform to support a range of waveforms in MIMO configurations [4].

3. ANALYSIS

The key challenges that are faced while designing a small, portable setup able to transmit RF signals with SDR technology are related to the power and quality of transmission. Thus, achieving a level of output power so that the broadcast reaches the whole area that needs to be covered.

Other challenges that need to be addressed depend on the autonomy of the system. How it is going to be powered and in which way it is going to be controlled.

The main components of the system have to be studied and selected carefully attending to their specifications. Global performance and capacity to achieve the objectives depend on them.

Reducing the size and weight of the final configuration has to be considered every time a component is evaluated and chosen. With the purpose of reducing the costs of material, some components already available at TNO will be chosen, and with them, the proposed solution will try to fulfill the technical requirements. Given that these are the early stages of an experimental project, there is some freedom to determine what is intended to be achieved.

3.1. SPECIFICATIONS

Regarding the RF transmission, it is expected to broadcast frequencies from 200 MHz up to 2 GHz. This transmission will have an output power in the range of 1 – 10 watts (30 – 40 dBm). It is mandatory that the device's transmissions are sensed wherever the device is situated within the limits of the training field, which consist on a 10 km side square. To implement the software that has already been developed at TNO, the system must run on Linux. The device has to be GPS trackable and connected to 3G/4G, which most likely will be achieved through USB ports. It is intended to remotely control the device. By the means of this control, stored files are selected in order to be transmitted. The system is supposed to be working as long as possible thus batteries should last 24 hours. The whole set has to be budget-friendly. The design has to be compact, as small and light as possible, and be protected by a watertight casing.

Very high frequency (VHF) and ultra high frequency (UHF) bands are those of most interest to the scope of this project, that is why the bandwidth is defined as 200MHz – 2GHz. Common uses for VHF and UHF are two-way land mobile radio systems, television broadcasting, cell phones, radar, GPS, Wi-Fi, and Bluetooth, inter alia.

3.1.1. Link budget calculation

To estimate the optimal transmitter output power, the link budget calculation is used. A link budget is a way of quantifying a communication link's performance while accounting for the system's power, gains, and losses for both the transmitter and receiver. It is assumed that the receiver is capable to detect -120 dBm, that receiver and transmitter antennas gains are 0 dBi and that the transceiver will perform in an open field with no obstacles. Nevertheless, a margin of 30dB is granted for covering unpredicted losses during transmission. The link budget equation is the following:

$$P_{TX} = P_{RX} - G_{TX} + L_{TX} + L_{FS} + L_M - G_{RX} + L_{RX}$$

where:

$\boldsymbol{P_{TX}}$ = transmitter output power (dBm)
$\boldsymbol{P_{RX}}$ = received power (dBm)
$\boldsymbol{G_{TX}}$ = transmitter antenna gain (dBi)
$\boldsymbol{L_{TX}}$ = transmitter losses (coax, connectors…) (dB)
$\boldsymbol{L_{FS}}$ = free space loss (dB)
$\boldsymbol{L_M}$ = miscellaneous losses (fading margin, body loss, polarization mismatch…) (dB)
$\boldsymbol{G_{RX}}$ = receiver antenna gain (dBi)
$\boldsymbol{L_{RX}}$ = receiver losses (coax, connectors…) (dB)

The equation for the free space loss is:

$$L_{FS} = 32.45 + 20\,log(D) + 20\,log(f)$$

where:

$\boldsymbol{D}$ = distance (km)
$\boldsymbol{f}$ = frequency (MHz)

Assuming the worst case scenario, the transmitter and the receiver would be placed on opposite corners, this is the area's hypotenuse. The distance is rounded up to 15 km. Besides, the highest frequency would mean higher losses, thus calculations are made for a frequency of 2000 MHz:

$$D = 15\ km$$

$$f = 2000\ MHz$$

$$P_{RX} = -120\ dBm$$

$$L_{FS} = 32.45 + 20\log(15) + 20\log(2000) = 122\ dB$$

$$G_{TX} = G_{RX} = 0\ dBi$$

$$L_{TX} + L_M + L_{RX} = 30\ dB$$

$$P_{TX} = -120 - 0 + 30 + 122 - 0 = 32\ dBm$$

The transmitter output power aimed to achieve is set to 33 dBm (2 W).

3.2. PROPOSED SOLUTION

The proposed solution is a self-contained system capable of transmitting RF signals within the selected range. The system includes a computer that manages the correct operation and is controlled remotely.

The design of the whole system exceeds the scope of the internship in terms of time, so certain parts will not be discussed and will be left for future work.

The design stage is centered in selecting the appropriate components from a theoretical perspective, followed by a developing stage, in which those components that require so are built. During the implementation stage, the system is assembled and measurements are taken to validate its performance.

4. DESIGN OF THE PROPOSED SYSTEM

The design of the system is performed by studying each component needed to achieve and support the proposed solution. The use of off-the-shelf components will be prioritized in the prototype.

There are two main components that are the foundation of the design and influence the selection of any other part. These are the SDR platform and the computer. Given their relevant roles, a market research is carried out and incorporated as comparison charts, where the most important characteristics of each model are included.

Once the SDR platform and the SBC have been selected, it is possible to proceed with the design and development of the other modules that will make the system up.

4.1. PRELIMINARY DESIGN

The general design of the system may be divided in three functional subsystems that interact with each other as Figure 4 illustrates.

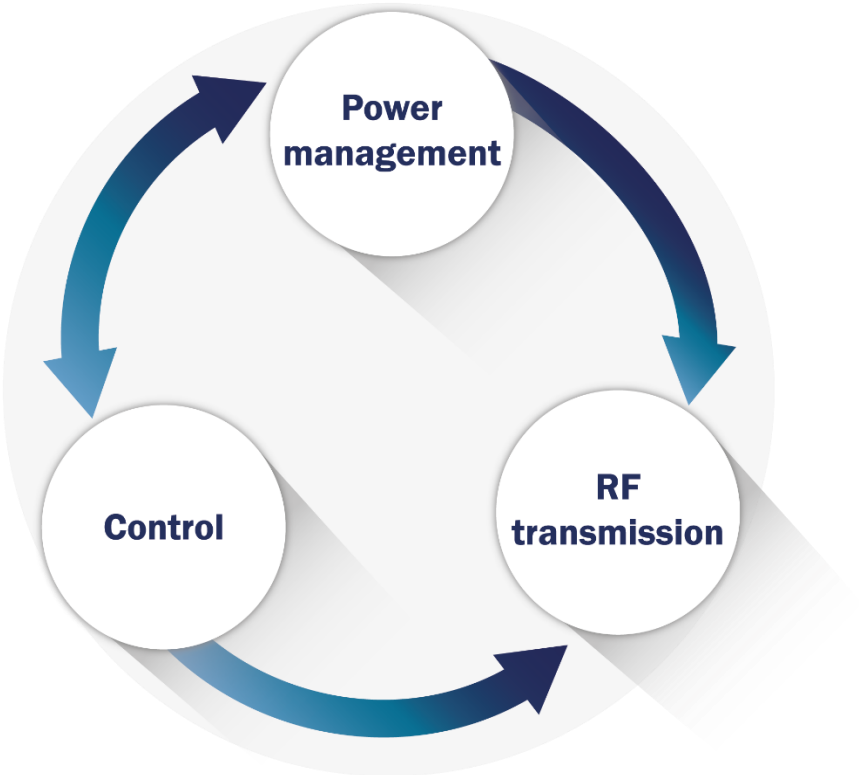


Figure 4. Functional subsystems

The RF subsystem encompasses all the components through which the RF signal travels. This is, those components that take part in the generation, amplification and transmission of the signal. SDR platform, power amplifiers and antennas are discussed down below.

The control subsystem is in charge of the proper operation of the system as well as of the external communication. It includes hardware and software components.

As the battery is the only source of power in the system, power management subsystem is required to regulate and supply power to every component.

4.2. RF TRANSMISSION

This subsystem is the most important. It is the one that performs the action that defines the whole system. The success of the setup relies on how well this subsystem operates.

4.2.1. Signal generation

The SDR platform is the core element in the signal transmission chain.

There is a great array of SDR peripherals in the market. Some significant models are covered in Table 1. Each of these devices is capable of transmitting RF signals, only receivers have not been taken into account. The characteristics of interest have been listed to compare the different devices, although not every manufacturer facilitates all of these data.

A great variability in prices among different models is appreciated. These values are not directly proportional to a single listed characteristic, even though it can be related to features as ADC/DAC resolution and frequency stability. In general, higher prices correspond to SDR platforms that include other components, such as processors, in Crimson TNG, and random-access memory (RAM), in Spectre. Different bands of radio frequency are covered by different models, from DC up to 6 GHz.

Based on the requirements, any of the SDR transmitters that are available at TNO operates at the selected frequency range. Aiming for the best performance, the priorities are high DAC resolution, high sampling rate and low weight. Besides the technical specifications, some other characteristics make USRP B205mini-i more interesting than the rest. The manufacturer, Ettus Research, provides an extensive database of its products, there are many open-access applications and the online community offers great support.

4.2.1.1. USRP B205mini-i

The USRP Bus Series provides a fully integrated, single board, Universal Software Radio Peripheral platform with continuous frequency coverage from 70 MHz – 6 GHz. It combines a fully integrated direct conversion transceiver providing up to 56 MHz of real-time bandwidth, an open and reprogrammable Spartan6 FPGA, and fast and convenient bus-powered SuperSpeed USB 3.0 connectivity.

Figure 5. USRP B205 mini-i

The RF frontend has individually tunable receive and transmit chains, in a SISO configuration. It has individual analog gain controls. The receive frontend has 76 dB of available gain; and the transmit frontend has 89.8 dB of available gain.

The analog frontend has a seamlessly adjustable bandwidth of 200 kHz to 56 MHz. Generally, when requesting any possible master clock rate, UHD will automatically configure the analog filters to avoid any aliasing (RX) or out-of-band emissions whilst letting through the cleanest possible signal.

Table 1. Software defined radio platforms comparison

Model	Tuning range	DAC resolution	Sampling rate	RF bandwidth	Channels	Freq. stability	Max. outpour power	Open source	Size and weight	Price
ADALM-PLUTO	300 MHz — 3.8 GHz	12 bit	61.44 MSPS	20 MHz	1 / 1	25 ppm	10 dBm	Yes	117 × 79 × 24 mm, 114g	$ 100
AD-FMCOMMS4-EBZ	70 MHz — 6 GHz	12 bit	320 MSPS	56 MHz	1 / 1					$ 399
ANAN-100	9 kHz - 55 MHz	16 bit	130 MSPS		1 / 1	0.1 ppm	100 W	Yes	376 x 79 x 264 mm, 5 kg	$ 2.489
bladeRF 2.0 micro	47 MHz - 6 GHz	12 bit	61.44 MSPS	56 MHz	2 / 2		8 dBm	Yes	36 x 102 x 18 mm, 90g	$ 480
Crimson TNG	DC - 6 GHz	16 bit	325 MSPS	1200 MHz	4 / 4		18 dBm	No	482.6 x 500 x 43.69mm, 5.4kg	$ 13.500
Flex 6700	30 kHz - 165 MHz	16 bit	491.52 MSPS	192 kHz	1 / 1	0.02 ppm	100 W	No	330 x 305 x 102 mm, 5.9 kg	$ 6.499
HackRF One	1 MHz - 6 GHz	8 bit	20 MSPS	20 MHz	1 / 1	20 ppm	15 dBm	Yes	120 x 75 mm	$ 299
Lime SDR	100 kHz - 3.8 GHz	12 bit	61.44 MSPS	61.44 MHz	2 / 2	4 ppm	10 dBm	Yes	100 x 60 mm	$ 299
Lime SDR mini	10 MHz - 3.5 GHz	12 bit	30.72 MSPS	30.72 MHz	1 / 1	4 ppm	10 dBm	Yes		$ 159
Lunaris SDR	10 kHz - 55 MHz	16 bit	122.88 MSPS		2 / 2	100 ppb	10 W	Yes	180 x 144 x 57.5 mm	$ 1.483
Spectre	400 MHz - 4GHz	16 bit	1230 MSPS	200 MHz	1 / 1		0 dBm		160 x 100 mm, 270 g	$ 10.000
SunSDR2 Pro	10 kHz - 160 MHz	14 bit	640 MSPS	312 kHz	3 / 4	0.5 ppm	10 dBm	No	165 x 165 x 35 mm, 1.5 kg	€ 1.890
ThinkRF R5500	9kHz - 27 GHz	14 bit	125 MSPS	100 MHz	1 / 1	1 ppm	10 dBm	Yes	269 x 173 x 55 mm, 2.7 kg	$ 3.000
UmTRX 2.3.1	300 MHz - 3.8 GHz	12 bit	13 MSPS	28 MHz	2 / 2	0.1 ppm	20 dBm	Yes	128 x 95 x 15 mm, 90 g	$ 1.300
USRP B210	70 MHz - 6 GHz	12 bit	61.44 MSPS	56 MHz	2 / 2	2 ppm	10 dBm	Yes	97 x 155 x 15 mm, 350 g	€ 1.220
USRP B205 mini-i	70 MHz - 6 GHz	12 bit	61.44 MSPS	56 MHz	1 / 1	2 ppm	10 dBm	Yes	83.3 x 50.8 x 8.4 mm, 24 g	€ 910
USRP N210	DC - 6 GHz	16 bit	400 MSPS		2 / 2	0.01 ppm	15 dBm	Yes	220 x 160 x 50 mm, 1.2 kg	€ 1.890
Zeus ZS1	300 kHz - 30 MHz	16 bit	100 MSPS	100 kHz	1 / 3		15 W	No	240 x 170 x 34 mm, 1.2 kg	$ 1.700

4.2.2. Signal amplification

The output power level of a system is typically the most important factor in the design and characterize the performance of almost all RF equipment. The output power delivered by the SDR is not enough to ensure a reliable communication, thus a power amplification stage will help to increase the output power to the range that was defined in the specifications.

4.2.2.1. Preliminary analysis

Each component in the signal chain must receive the proper signal level from the previous component and pass the correct signal level on to the subsequent component. If the output signal level is too low, the signal may be obscured in noise. Alternatively, if the signal level is too high, the performance will be nonlinear and distortion or damage will occur. To choose the adequate components, the level of output power that the SDR is capable of transmitting is checked.

There is some performance data available on the Ettus website (Fig. 6). However, the maximum gain tested is 86 dB and, as mentioned previously, the transmit frontend has 89.8 dB of available gain.

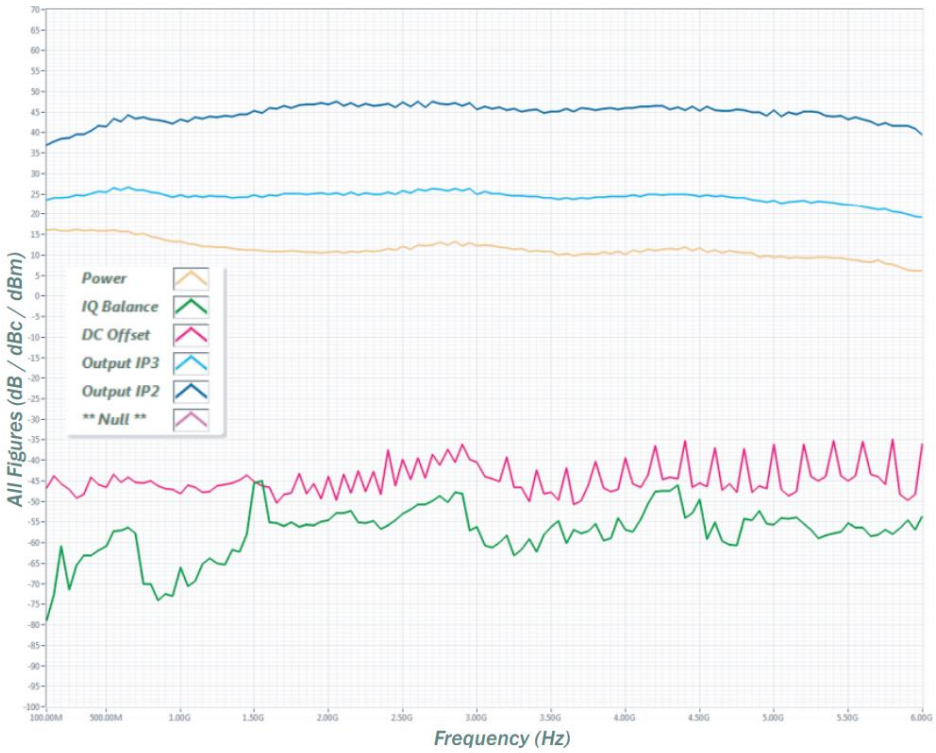


Figure 6. TX Figure vs Frequency w/ Gain=86.00dB.

The SDR's performance is tested with the aid of GRC and a spectrum analyzer (Rohde & Schwarz FSL6). Two different modulations are selected for this test: frequency modulation (FM) and binary phase-shift keying (BPSK). Since the output power is strongly dependent of the frequency, the goal is to find the maximum output powers delivered by the SDR at 200 MHz and 2 GHz, and to verify that the level of noise is correct (Fig 7, 8). These values will then be used to select the amplification components.

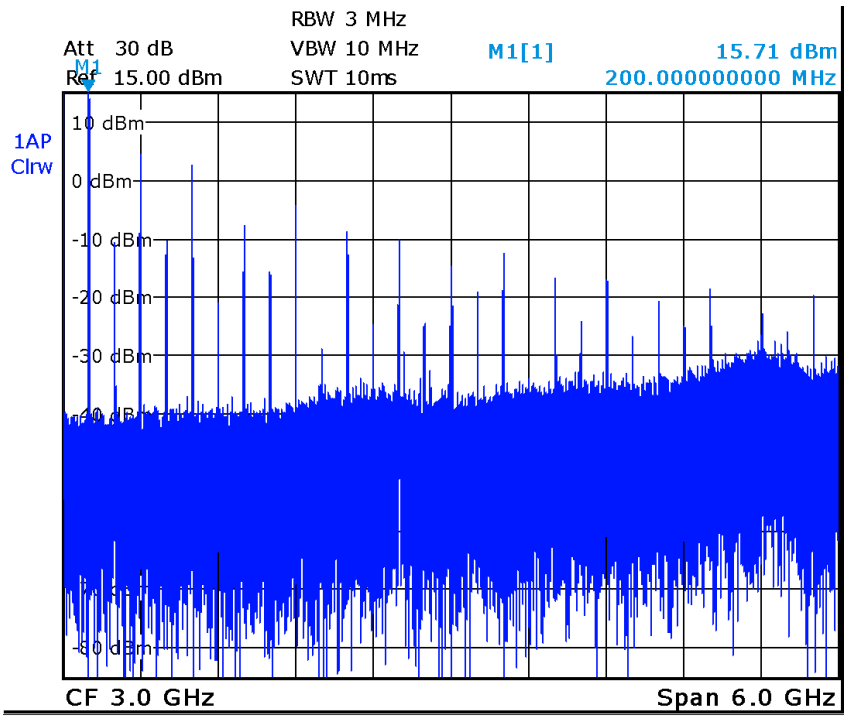


Figure 7. TX frequency spectrum with gain = 90 dB, at 200 MHz, BSPK modulation

The maximum value obtained is 15.71 dBm at 200 MHz and maximum gain with BPSK modulation, (Figure 7). The minimum value obtained is 6.94 dBm at 2 GHz and maximum gain with FM modulation, (Figure 8). Noise has a maximum level in the order of -30 dBm in both graphics, which it is considered an adequate result. Because a digital modulation is chosen in Fig. 7, the harmonic content in the spectrum corresponds, as expected, to a square wave: a sine wave at the fundamental frequency along with sine waves at the odd harmonics. In this case, the third and the fifth harmonics are over the 0 dBm. This undesirable high-frequency content has to be kept in mind when the actual bandwidth of the modulated signal is considered.

According to these data, a suitable amplifier will be one that admits a maximum RF input power over 16 dBm, and that is capable to amplify a 6.5 dBm signal (worst-case scenario) to the desired level.

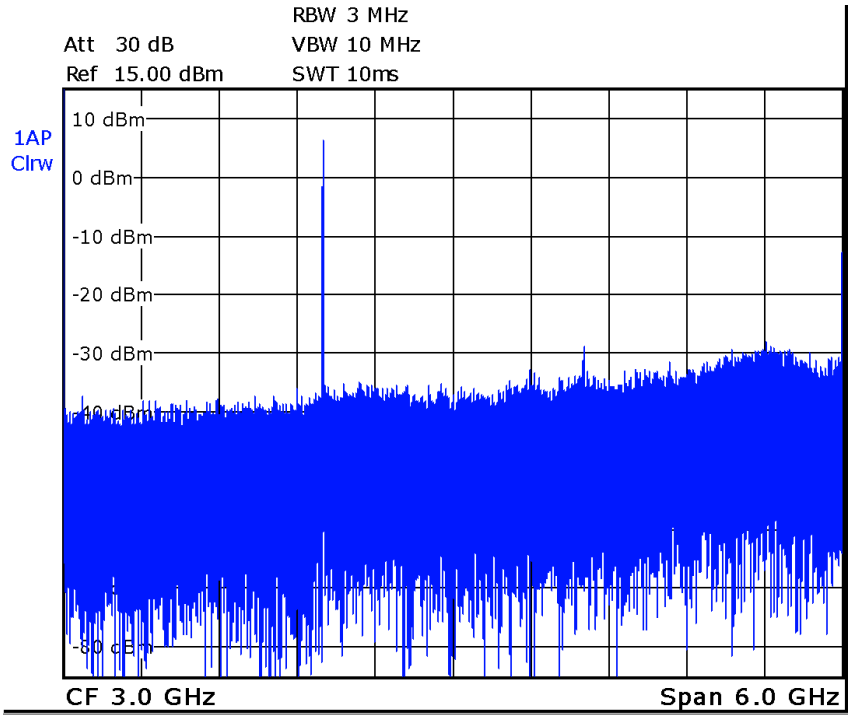


Figure 8. TX frequency spectrum with gain = 90 dB, at 2 GHz, FM modulation.

4.2.2.2. One-stage RF amplifier

With the data from the link budget calculation, a market research is conducted to find an amplifier that satisfies the requirements.

Some of the parameters that define an RF power amplifier are: output power, gain, bandwidth, linearity, DC supply voltage and efficiency. The maximization of any of these characteristics depends on the design goals. Some of these parameters cannot be sought at the same time as they are conflicting requirements (e.g., linearity and efficiency).

For the scope of this project, there are a few considerations to be taken into account. First, the minimum gain value has to be 18 dB, ideally 23 dB. Second, the maximum RF input power has to exceed 16 dBm. A third consideration is that the 1 dB compression point (P1dB) has to be, at least, of 33 dBm. Finally, the amplifiers are presented in different formats: modules and systems. A module is usually a smaller unit designed to be integrated into an assembly, whereas a full system is complete with chassis, cooling, etc. It seems more appropriate to find a module, for the purpose of miniaturization.

The RF amplifier's offer is extensive, due to all the performance possibilities related to different characteristics. In Table 2, amplifiers with interesting specifications are referred.

Once evaluated, none of these listed amplifiers entirely satisfies all the requirements. Either their prices are quite high or they don't reach the amplification level that is required in the worst case scenario (SDR power output = 6.5 dBm).

In the light of these results, it is considered more feasible to achieve the planned amplification in two stages.

4.2.2.3. Two-stage RF amplifier

As the final output power is known, the first step is to find the second amplifier. This amplifier has to deliver at least 33 dBm, as seen in section 3.1.1., and perform properly for a power input range of $6.5 - 16$ dBm.

Some models of amplifiers that would satisfy the requirements are referred in Table 3.

Aiming for the highest output power, the HMC8500PM5E and the TGA2216-SM are the best options. After going through their datasheets, the HMC8500PM5E is selected because it consumes, and loses, less power. It requires 28 V of power supply (compared to 40 V) and its quiescent current is 100 mA (compared to 360 mA).With the data of this HMC8500PMSE amplifier, the requirements for the first stage can be obtained. It is desirable for noise reduction purposes to avoid the use of an attenuator, meaning that the first stage has to be designed to not cause compression on the second stage. First, the required gain in the first stage is calculated:

$$max\ gain\ 1^{st}stage = max\ input\ power\ 2^{nd}stage - max\ SDR\ output = 33\ dBm - 16\ dBm = 17\ dB$$

Next, this gain is evaluated for the worst-case scenario:

$$min\ output\ power\ 1^{st}stage = min\ SDR\ output + gain\ 1^{st}stage = 6.5\ dBm + 17\ dB = 23.5\ dBm$$

$$min\ output\ power\ 2^{nd}stage = min\ output\ power\ 1^{st}stage + min\ gain\ 2^{nd}stage = 23.5\ dBm + 13\ dB = 36.5\ dBm$$

Some models of amplifiers with suited characteristics for the first stage are included in Table 4.

Table 2. Suitable commercially-available RF amplifiers

Model	Bandwidth	Gain	Linearity		Power supply	Output power	Power-added efficiency (PAE)	Maximum input power	Size and weight	Price
			P1dB	OIP3						
HPA-25W-272+	20 MHz – 2.7 GHz	50 dB	38 dBm	50 dBm	AC 110-240 V	44 dBm		5 dBm	480 x 513 x 87 mm, 13.6kg	$ 5395
HPA-50W-63+	700 MHz – 6 GHz	56 dB	43 dBm	50 dBm	AC 110-240 V				480 x 513 x 87 mm, 13.6kg	$ 17995
ZHL-25W-272+	20 MHz – 2.7 GHz	50 dB	40 dBm	49 dBm	28 V	44 dBm		5 dBm	250 x 185 x 165 mm, 4.6 kg	$ 3795
ZHL-4240W+	10 MHz – 4.2 GHz	42 dB	30 dBm	38 dBm	15 V				178 x 83 x 54 mm, 0.9 kg	$ 1495
RAMP00G18GA	0.01 GHz – 18 GHz	31 dB	26 dBm	35 dBm	AC 110-240 V				164 x 148 x 58 mm, 1kg	-
RAMP00G30GA	0.01 GHz – 30 GHz	40 dB	28 dBm	33 dBm	AC 110-240 V				164 x 148 x 58 mm, 1.1kg	-
PE15A5011	30 MHz – 2.5 GHz	43 dB	35 dBm		12 V	40 dBm	> 40 %		95 x 51 x 13 mm, 288 g	$ 7438
PE15A4017	20 MHz – 3 GHz	27 dB	30 dBm	39 dBm	12 V				53 x 27 x 13 mm, 43.32 g	$ 750
QPA2237	0.03 – 2.5 GHz	18.5 dB			32 V	40 dBm	52 %	33 dBm	4 x 4 x 0.85 mm	$ 130
TGA2216	0.1 – 3.0 GHz	22 dB	34 dBm		48 V	41 dBm	> 40%	33 dBm	1.8 x 1.8 x 0.10	$ 120
TGA2216-SM	0.1 – 3.0 GHz	21 dB	35 dBm		40 V	>40 dBm	> 50 %	33 dBm	5 x 5 x 1.45 mm	$ 140
TGA2976-SM	0.1 – 3.0 GHz	20 dB			40 V	>40 dBm	48 %	33 dBm	4 x 4 x 1.64	$ 130

Table 3. Second-stage suitable RF amplifiers

Model	Bandwidth	Min. gain	Linearity		Output power	Maximum input power	Price
			P1dB	OIP3			
HMC8500PM5E	0.01 – 2.8 GHz	13 dB		47 dBm	10 W	33 dBm	$ 100
CMPA0060002F	20 MHz – 6 GHz	16.8 dB			3 W		€ 140
TGA2216-SM	100 MHz – 3 GHz	13 dB	35 dBm		10 W	33 dBm	€ 150
HMC998A	DC – 22 GHz	14 dB	29.5 dBm	41 dBm	2 W	27 dBm	€ 215

Table 4. First-stage suitable RF amplifiers

Model	Bandwidth	Gain	Linearity		Maximum input power	Price
			P1dB	OIP3		
SXB2089Z	5 – 2500 MHz	23 dB	24 dBm	43 dBm	20 dBm	€ 7.55
MAAP-011232	0.1 – 3 GHz	24.5 dB	29 dBm	40 dBm	20 dBm	$ 15
MMA053AA	DC – 8 GHz	17 dB	29 dBm	43 dBm	TBD	€ 77
HMC637BPM5E	DC – 7.5 GHz	15.5 dB	28 dBm	39 dBm	25 dBm	$ 90
HMC459	DC – 18 GHz	14 dB	29.5 dBm	41 dBm	27 dBm	$ 117

Since the specifications of these devices are similar, it is necessary to conduct a detailed review of their datasheets in order to select the one that provides the best performance.

Model SXB2089Z shows the performance application data in very narrow bandwidths. It seems that the device will not be able to perform properly at a broad bandwidth.

A similar problem is encountered with MAAP-011232. The performance characteristics are split in two different application bandwidths, both smaller than the bandwidth that the design requires. Besides, the gain curve is very frequency-dependent, with a loss of 10 dB in a 1 GHz interval.

The model MMA053AA does not include any reference to efficiency or maximum RF input power.

Both HMC637BPM5E and HMC459 datasheets include application circuits for their whole range of operation, already matched to 50 Ω. Since they are designed to operate in wider frequency ranges, the parameters are conveniently linear in the 200 MHz – 2 GHz range. However, the performance characteristics charts are limited in the HMC459, being the HMC637BPM5E the one that provides more information. Furthermore, Analog Devices supplies an evaluation board for this device.

For these reasons, it is determined that the best choice is the HMC637BPM5E. Table 5 summarize the important component specifications of the selected components.

Table 5. Active components

Component	Part Number	Gain	OP1dB	IIP3	OIP3	Power output
SDR	Ettus B205 mini-i	89.8 dB		-20 dBm		> 10 dBm
1st PA	HMC637BPM5E	15.5 dB	28 dBm		39 dBm	30 dBm
2nd PA	HMC8500PM5E	15.0 dB	-		47 dBm	40 dBm

The theoretical outputs from the amplification stage are included in Table 6. The first row shows the values for the lowest frequency of the design bandwidth and the second one, the highest. The values are extracted from the typical performance characteristics graphs found in the datasheets.

Table 6. Expected signal outputs

B205mini		HMC637		HMC8500	
TX	**Out**	Gain	**Out**	Gain	**Out**
200 MHz	15 dBm	15.5 dB	30.5 dBm	22 dB	40 dBm
2 GHz	6.5 dBm	16 dB	22.5 dBm	13.5 dB	33 dBm

Reducing costs is not the only advantage of dividing the amplification stage by two. Other important benefit is that using two devices offers the heat flow two paths. This means that even though the power losses are virtually similar, the heat sink required is smaller [5].

HMC637BPM5E

The HMC637BPM5E from Analog Devices is a monolithic microwave integrated circuit (MMIC) power amplifier delivering 1 W (30 dBm). The device is self-biased in normal operation and features optional bias control. It operates from DC to 7.5 GHz with an excellent gain flatness, providing 15.5 dB of small signal gain, 28 dBm output power and requiring 345 mA from a 12 V supply voltage. Its inputs/outputs are internally matched to 50 Ω.

HMC8500PM5E

The HMC8500PM5E from Analog Devices is a broadband power amplifier delivering 10 W (40 dBm). The recommended DC bias conditions place the device in Class AB operation, resulting in high output power at improved levels of power efficiency. It provides 15.0 dB of small signal gain at an input power of 30 dBm, requiring a 28 V supply voltage. The device is internally pre-matched so that simple, external matching networks optimize the performance across the entire operating frequency range.

The PAs will be implemented using the evaluation boards provided by Analog Devices.

4.2.3. Signal transmission

The signal chain is represented in Figure 9. All the transmit ports have a 50 Ω characteristic impedance.

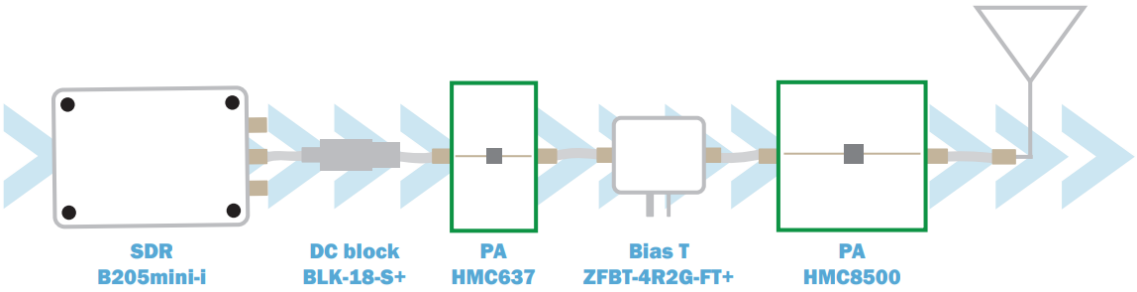


Figure 9. Signal transmission chain

An RF choke is required at the RF output to supply voltage at the V_{DD} bias pin and blocking capacitors are recommended at the RF ports for the HMC637BPM5E's evaluation board.

The operation frequencies of these components have to be adequate for use across the entire frequency range of the application. The RF output port functions as the V_{DD}, is provided at

the output through the DC port of the bias tee. The additional components in the signal chain are referred in Table 7.

Table 7. Additional component parameters for the HMC637BPM5E

Component	Part number	Frequency (MHz)		Insertion loss (dB)		Return loss (dB)		VSWR (:1)	
		f_L	f_U	Typ.	Max.	Typ.	Min.	Typ.	Max.
DC block	BLK-18-S+	10	18000	0.1	0.3	24	20		
Bias Tee	ZFBT-4R2G-FT+	10	4200	0.6	1.2			1.13	1.3

The last component within the signal chain is the antenna. The antenna selection is not covered in this project. However, some observations are included.

The bandwidth of design is too big to be covered by one single antenna. It is recommended, at least, to include one antenna for lower frequencies and another one for higher frequencies. However, to optimize the transmission, the selection of the most suitable antenna with the appropriate bandwidth would improve the performance, reducing non linearities.

4.3. CONTROL

Along with the computer, the control subsystem includes other components that are not mentioned in this project, such as the communication card and the software controlling the RF transmission.

4.3.1. Computer

A comparison among SBCs currently on the market is to be found in Table 8. Raspberry Pi SBC is not considered as a possible choice because its performance is not powerful enough. However, it is listed due to its high popularity, and as a reference point. The rest of the SBC proposed have at least 2GB RAM. Other technical specifications that are significant for the purpose are reflected on the following table.

It is observed that the price variability is not as significant as it is with the SDR peripherals. As the SBC is the component that carry out the digital signal processing, important characteristics in the selection of a correct SBC are frequency and number of cores of the central processing unit (CPU) and RAM.

Table 8. Single board computer comparison

Model	CPU			RAM	Storage		USB ports	Network		Operating system	Price
	Cores	Architecture	Frequency		On-board	Flash slots		Ethernet	Wi-Fi		
armStoneA9	4	ARM Cortex-A9	1.2 GHz	4 GB	1 GB	SD	4x USB 2.0	Yes	No	Linux (partial), Android, Windows	€ 299
Boardcon EM3399	6	ARM Cortex-A72 / A53	2.0 GHz	4 GB	8GB	micro SD	2x USB 2.0 3x USB 1.0	Yes	Yes	Linux (partial), Android	$ 150
Firefly-RK3288 Reload	4	ARM Cortex-A17	1.8 GHz	2 GB	16GB	micro SD	3x USB 2.0	Yes	Yes	Linux (partial), Android	$ 100
Gigabyte GB-BACE-3000	2	Intel Celeron N3000	1.04 GHz	8 GB		microSD	4x USB 3.0	Yes	Yes	Windows	€ 120
Huawei HiKey 960	8	Cortex-A73 / A53		3 GB	32 GB	microSD	1x USB 2.0 2x USB 3.0	No	Yes	Linux, Android	$ 240
Minix Neo Z83-4	4	Intel X5-Z8350	1.4 GHz	4 GB	32GB		3x USB 2.0 1x USB 3.0	Yes	Yes		€ 200
Nvidia Jetson TX1	8	ARM Cortex-A57	1.9 GHz	4 GB	16 GB	SD	1x USB 2.0 1x USB 3.0	Yes	Yes	Linux (partial)	$ 320
PC Engines APU .2C4	4	AMD GX-412TC	1 GHz	4 GB	No	SD	2x USB 2.0 3x USB 1.0	Yes	Opt.	Linux, Android	€ 193
Pine A64-LTS	4	ARM Cortex-A53	1.2 GHz	2 GB	16 GB	microSD	2x USB 2.0	Yes	Yes	Linux, Android	$ 32
Raspberry Pi 3 Model B+	4	ARM-Cortex-A53	1.4 GHz	1 GB		microSD	4x USB 2.0	Yes	Yes	Linux (partial), Windows	$ 35
Tronsmart Draco TW80	8	ARM Cortex-A15 / A7	1.3 GHz	4 GB	32 GB	SD	2x USB 2.0 1x USB 3.0	Yes	Yes	Android	$ 144
UDOO X86 Ultra	4	Intel N3710	2.56 GHz	8 GB	32GB	M.2 SSD microSD	3x USB 3.0	Yes	Opt.	Linux, Android, Windows	$ 267

Taking this into account, once the listed components have been reviewed, the UDOO X86 Ultra is selected, as it is the most powerful among them.

4.3.1.1. UDOO X86 Ultra

UDOO X86 embeds both a SoC of the Intel family and an Arduino 101-compatible platform. The SoC is Quad-Core, up to 2.56 GHz, with 64-bit instruction set and very low TDP. This single chip solution includes the memory controller, for up to 8GB DDR3L memory, directly soldered on-board. Even with this SoC, the UDOO is considered energy efficient.

Other features included are two SATA channels, microSD interface, four USB ports and four PCI Express lanes. This good wired connectivity along with the SoC make the UDOO X86 board stand out from the rest of competitors.

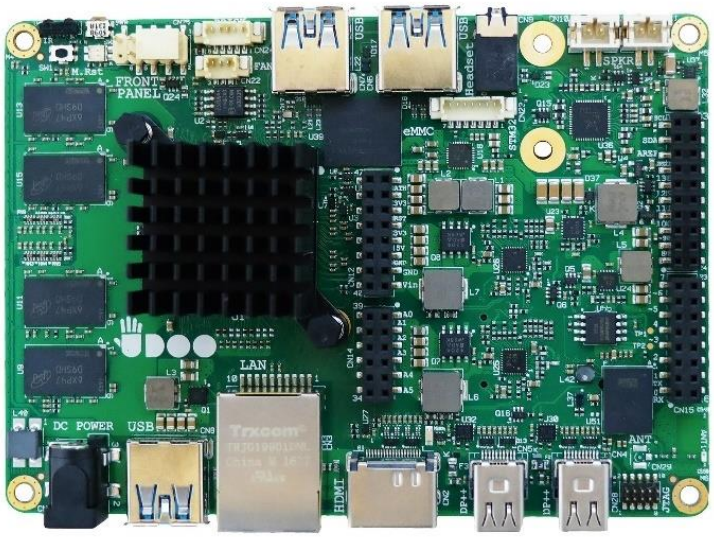


Figure 10. UDOO X86 Ultra

4.4. POWER SUPPLY

4.4.1. Power requirements

The total power consumption of the main components in the system is estimated in Table 9.

Table 9. Estimated power consumption

Power consumption mode	UDOO X86	B205 mini-i	HMC367	HMC8500	Total
Quiescent	83.33 mA 1W	-	345 mA 4.14 W	100 mA 2.80 W	455 mA 10.292 W
Average	833 mA 10 W	2.352 W [1]	375 mA 4.50 W	625 mA 17.5 W	2.303 A 34.352 W
Maximum	36 W [2]	-	475 mA 5.7 W	735 mA 20.6 W	4.68 A 64.652 W

[1] Measured with a 6 V power supply, 1 TX, 30.72 Msps. [6]
[2] The manufacturer recommends to use a power supply with a minimum power of 36 W.

4.4.2. Power source

The source of power of this system is a BB-2590/U battery. Due to the availability of this model within the military, selecting it as the power source is considered both suitable and feasible. This will facilitate the replacement and charge of batteries by the potential client.

The BB-2590/U has a capacity of 20.7 Ah, nominal 10.35 Ah. It supplies a nominal voltage of 28.8 V (maximum 33.6 V, minimum 20.0 V). Its size (126.8 x 111.6 x 62.6 mm) makes it easily integrable into small systems. If longer capacity is required, several batteries can be connected in parallel.

4.4.3. Power management

There are three main components that need to be powered: the SBC and the PAs. Knowing that each of these components needs a particular stable supply voltage and that the voltage supplied by the battery changes with time, it is mandatory to include an intermediate step between the battery and the components.

Figure 11 represents the power flow, where every block, named A to F, indicates a voltage conversion.

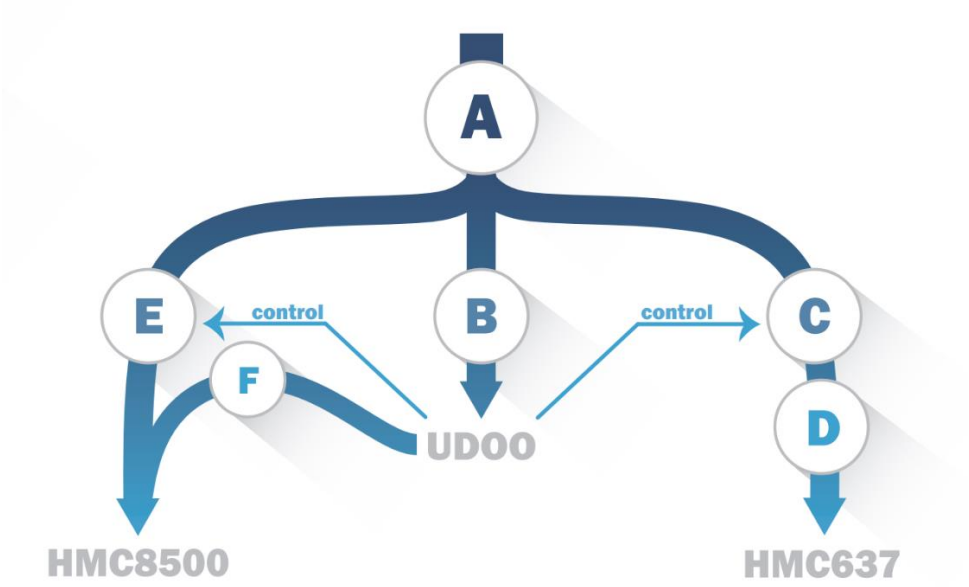


Figure 11. Power flow, stages.

Block A is in charge of regulating and stabilizing battery's output voltage. This will be achieved with a DCDC converter.

Block B converts A's output voltage into the required UDOO's supply voltage, by means of a step-down DCDC converter.

Blocks C and D regulate the V_{DD} of the first PA, while E does it for the second PA. The closest components to the PAs are low drop-out regulators (LDOs), while block C is a step-down converter.

Finally, block F supplies HMC8500's V_{GG}.

Even though the computer and the HMC637 require the same supply voltage, powering them separately is considered a better option for stability purposes. This will also allow to disconnect the PAs by controlling blocks C and E with the computer, for a further reduction in power consumption.

When selecting DCDC regulators, these devices should be designed for RF applications, be highly efficient and operate at high frequencies, meaning that they will require smaller external components.

The chosen components for every block will be explained down below.

4.4.3.1. Why LDOs regulators?

Switching converters are highly efficient, but their outputs are usually noisy over a wide bandwidth. Since the PAs are sensitive components, they require supply voltages free of noise and ripple. It is considered the best practice to supply the PAs with LDOs instead of switching converters. LDO regulators provide exceptionally clean supply rails by filtering out the output voltage ripple inherent to DCDC switching conversions; but they compromise, however, efficiency [7].

Efficiency in LDO regulators depends on headroom voltage (difference between input and output voltages) regardless of the load conditions.

$$Efficiency = \frac{I_o V_o}{(I_o + I_q)V_i} \times 100$$

It might seem that the headroom voltage should be minimized as much as possible, but there is another important factor to take into account: power supply rejection ratio (PSRR). PSRR measures the LDO ability to reject the output ripple caused by input voltage variations. Since a switching device powers the LDOs, high PSRR is sought. Values of -60 dB or less are considered adequate.

PSRR is strongly dependent on headroom voltage, and it decreases as headroom voltage decreases. As an example of this behavior, PSRR for different headroom voltages (V_{DO}) in TPS7A47-Q1 is shown in Figure 12.

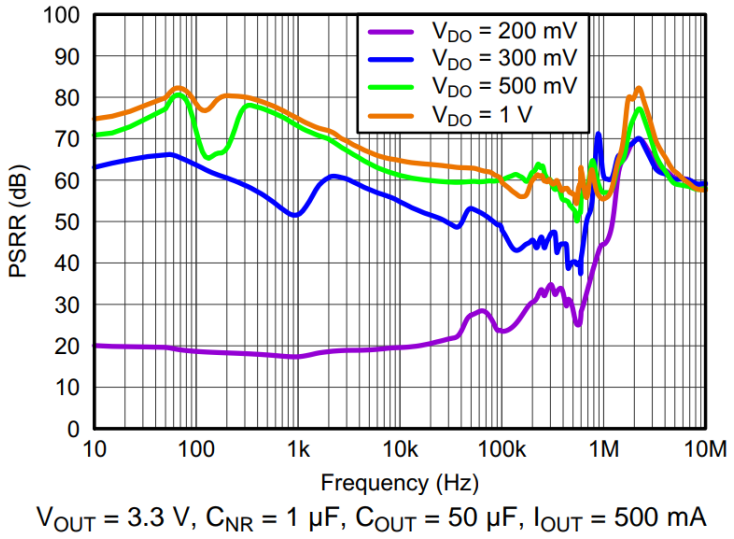


Figure 12. Power supply rejection ratio vs frequency and V_{DO}

Thus, it is important to find the balance between a small headroom (high efficiency) and a high PSRR for each LDO.

Knowing the supply requirements of each component, the output voltages of every stage can be designed. Putting these voltage conversions into numbers, the power flow is as represented in Figure 13.

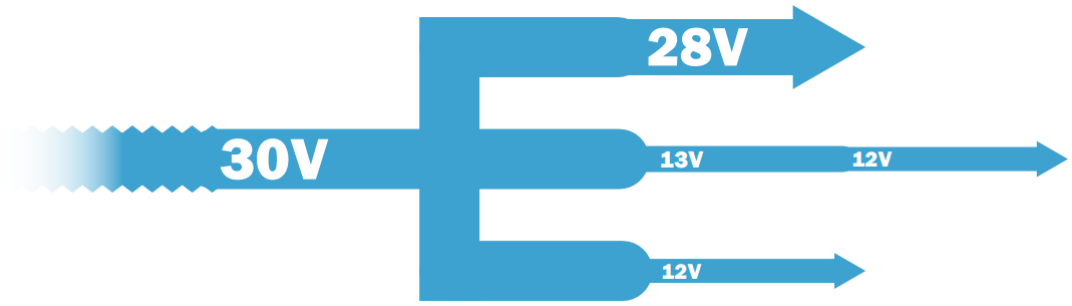


Figure 13. Power flow, voltages.

This diagram will be implemented by the means of a PCB that will be designed and fabricated.

4.4.4. Normalizing battery

The output voltage of the first converter is set at 30 V. The battery voltage can be above, below or equal to this value. That is why a buck-boost converter is selected for this task.

The LT8390A is a synchronous 4-switch buck-boost controller featuring low noise transitions and high efficiency.

Comparing advantages and disadvantages of selecting a high switching frequency, the highest frequency of operation is selected, 2MHz. This allows for smaller components, faster transient response, smaller voltage over and smaller undershoots. The same reasoning is applied with the buck converters.

4.4.5. HMC637's power supply

The amplifier requires 12 V supply voltage (V_{DD}). This conversion will be achieved in two steps since the voltage difference between LT8390A's output and HMC637's input voltage is too large to consider using just an LDO regulator. Therefore, a buck converter will reduce the

30 V up to 13 V, and then, an LDO will regulate this voltage down to 12 V. These devices must be able to deliver 345 mA.

The LT8607 is a high efficiency low EMI step-down switching regulator with a enable pin to shut down the device, and, consequently, the PA. It can deliver 750 mA of continuous current. For the design, it is adjusted to 2 MHz switching frequency.

The LT3045 is an ultralow noise, ultrahigh PSRR low drop-out linear regulator, which makes it excellent as a post-regulator for the buck-boost converter and as a RF power supply for the PA.

4.4.6. HMC8500's power supply

The power amplifier requires 28 V drain bias voltage (V_{DD}), and a value between -3V and -2.5 V gate bias voltage (V_{GG}) to achieve I_{DDQ} = 100 mA (-2.65 V typical).

For supplying 28 V, use is made of an LDO regulator. The TPS7A47 is an ultralow noise linear regulator designed for high-accuracy applications, ensuring maximum system performance in RF applications. In addition, it is ideal for post DCDC converter regulation. The enable pin will be controlled.

The negative gate voltage is achieved using a charge pump voltage inverter. The TPS6040 inverts input supply voltage coming from UDOO's CN22 connector, which makes it suitable to bias the PA. For the adjustment of V_{GG}, a trimming potentiometer is included.

4.4.7. UDOO's power supply

The computer requires 12 V supply voltage. The power consumption depends strongly on the utilization scenario. To cover high demanding scenarios, the manufacturer recommends a power supply capable of deliver 3 A.

The LT8614 is a high efficiency step-down switching regulator designed to minimize EMI emissions. It can deliver up to 4 A of continuous current. For the design, it is adjusted to 2 MHz switching frequency.

4.5. SYSTEM ARCHITECTURE

The following Figure 14 represent the interconnection of the components previously mentioned.

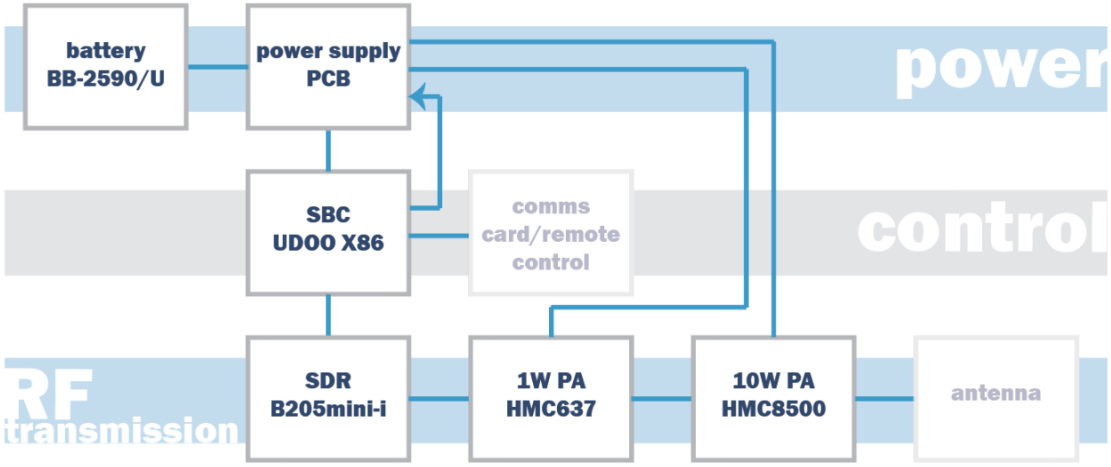


Figure 14. System architecture

5. PRINTED CIRCUIT BOARD DEVELOPMENT

As stated in the previous chapter, the power supply chain is implemented in a single PCB. The employed electronic design software is Altium Designer.

First, calculations are made for selecting the main external components according to the datasheets [8, 9, 10, 11, 12, 13]. Second, the circuit diagrams are drawn in Altium's schematic visualizer (Schematics document). Then, in the PCB visualizer, the actual location of each component is decided. Lastly, tracks and planes are placed.

The goal is to achieve a functional PCB with a simple, comprehensive and easily-tested layout.

5.1. EXTERNAL COMPONENTS SELECTION

The external components are selected following the manufacturer's recommendations. Use is also made of the LTpowerCAD (Fig. 15, 16) tool to check and estimate the performance of the designed applications.

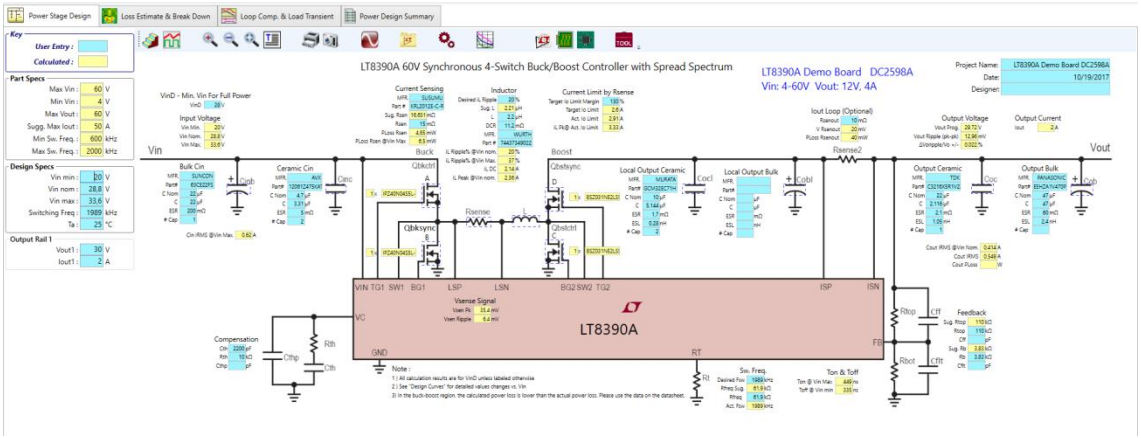


Figure 15. Power Stage Design tab in LTpowerCAD, LT8390A

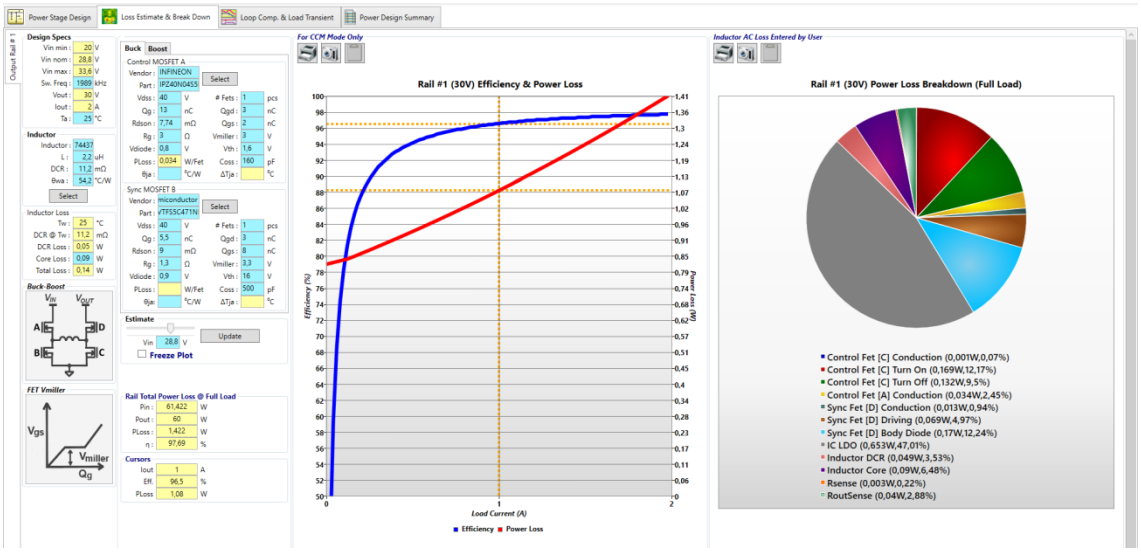


Figure 16. Loss Estimate and Break Down tab in LTpowerCAD, LT8390A

5.1.1. Buck-Boost Controller: LT8390A

5.1.1.1. Output voltage and thresholds

The LT8390A has a voltage feedback pin that can be used to program a constant-voltage output according to the equation:

$$V_{OUT} = 1\,V \cdot \frac{R_5 + R_6}{R_6} = 29.72\,V$$

In addition, it sets output overvoltage threshold and output short threshold, defined by:

$$V_{OUT(OVP)} = 1.1\,V \cdot \frac{R_5 + R_6}{R_6} = 32.70\,V$$

$$V_{OUT(SHORT)} = 0.25\,V \cdot \frac{R_5 + R_6}{R_6} = 7.43\,V$$

where R5 is a 110kohm resistor and R6 is a 3.83kohm resistor.

5.1.1.2. Enable

A resistor divider from V_{IN} to the EN/UVLO pin implements undervoltage lockout. The programmable UVLO thresholds are:

$$V_{IN(UVLO+)} = 1.233\,V \cdot \frac{R_7 + R_8}{R_8} + 2.5\,\mu A \cdot R_1 = 19.8774\,V$$

$$V_{IN(UVLO-)} = 1.220\,V \cdot \frac{R_7 + R_8}{R_8} = 18.7204\,V$$

where R7 is a 383kohm resistor and R8 is a 26.7kohm resistor.

5.1.1.3. Operating frequency

The switching frequency of the LT8390A is set by a resistor from the RT pin to ground. The selected value is 61.9 kΩ, corresponding to a 2 MHz switching frequency.

5.1.1.4. Inductor

The inductor value has a direct effect on ripple current. The highest current ripple happens in the buck region at $V_{IN(MAX)}$, and the lowest current ripple happens in the boost region at $V_{IN(MIN)}$. With a inductor current ripple ratio set at 30%, the minimum inductance is calculated:

$$L_{BUCK} > \frac{V_{OUT} \cdot (V_{IN(MAX)} - V_{OUT})}{f \cdot I_{OUT(MAX)} \cdot \Delta I_L\% \cdot V_{IN(MAX)}} = 1.70\ \mu H$$

$$L_{BOOST} > \frac{{V_{IN(MIN)}}^2 \cdot V_{OUT}}{f \cdot I_{OUT(MAX)} \cdot \Delta I_L\% \cdot {V_{OUT}}^2} = 2.54\ \mu H$$

For high efficiency and noise reduction, an inductor with low core loss, low DC resistance and shielded is selected. L1 is a shielded ferrite inductor of 3.3 µH with a R_{DC} of 6.5 mΩ.

5.1.1.5. Current sense resistor

The resistor is chosen based on the required output current. The duty cycle independent maximum current sense threshold (50mV) set the maximum inductor peak current. The maximum current sense resistor in boost and buck regions are:

$$R_{SENSE(BOOST)} = \frac{2 \cdot 50\ mV \cdot V_{IN(MIN)}}{2 \cdot I_{OUT(MAX)} \cdot V_{OUT} + \Delta I_{L(BOOST)} \cdot V_{IN(MIN)}} = 11.30\ m\Omega$$

$$R_{SENSE(BUCK)} = \frac{2 \cdot 50\ mV}{2 \cdot I_{OUT(MAX)} + \Delta I_{L(BUCK)}} = 17.50\ m\Omega$$

where $\Delta I_{L(BOOST)}$ and $\Delta I_{L(BUCK)}$ are peak-to-peak inductor ripple current in boost and buck regions and are calculated as:

$$\Delta I_{L(BOOST)} = \frac{V_{IN(MIN)} \cdot (V_{OUT} - V_{IN(MIN)})}{f \cdot L \cdot V_{OUT}} = 0.9183\ A$$

$$\Delta I_{L(BUCK)} = \frac{V_{OUT} \cdot (V_{IN(MAX)} - V_{OUT})}{f \cdot L \cdot V_{IN(MAX)}} = 0.4095\ A$$

The final resistor's value should be lower than calculated. An 10 mΩ current sense resistor with low ESL is selected.

5.1.1.6. Power MOSFET

Four N-channel power MOSFETs are required. MOSFETs with low Q_g low $R_{DS(ON)}$ and logic-level threshold must be used. Other important parameters are the breakdown voltage, reverse transfer capacitance and maximum current.

The most important parameters of the selected MOSFETs are included in Table 10.

Table 10. MOSFET parameters

	Input MOSFETs	Output MOSFETs
Q_g	13 nC	5.5 nC
$R_{DS(ON)}$	7.4 mΩ	9 mΩ
$V_{BR(DSS)}$	40 V	40 V
$V_{GS(TH)}$	1.6 V	1.6 V
C_{RSS}	10 pF	12 pF
$I_{DS(MAX)}$	40 A	41 A
T_J	-55 to 175 °C	-55 to 175 °C

The required $INTV_{CC}$ current must not exceed the current limit (145 mA).

$$I_{INTVCC} = f \cdot (Q_{gA} + Q_{gB} + Q_{gC} + Q_{gD}) = 0.074\ A$$

To ensure smooth transitions between modes of operation, the MOSFETs and the inductor must be selected to satisfy:

$$I_{OUT(MAX)} \leq \frac{0.025 \cdot V_{OUT}}{R_{A,B} + R_{C,D} + R_{SENSE} + R_L} = 17.56\ A$$

where $R_{A,B}$ is the maximum $R_{DS(ON)}$ of MOSFETs A/B at 25°C and $R_{C,D}$ is the maximum $R_{DS(ON)}$ of MOSFETs C/D at 25°C.

In order to select the power MOSFETs, the power dissipated by the device must be known. The input voltage takes the minimum and maximum values given by the battery, for boost and buck regions calculations, respectively.

For switch A, the maximum power dissipation happens in boost region, when it remains on all the time. Its maximum power dissipation at maximum output current is given by:

$$P_{A(BOOST)} = \left(\frac{I_{OUT(MAX)} \cdot V_{OUT}}{V_{IN(MIN)}}\right)^2 \cdot \rho_T \cdot R_{DS(ON)} = 0.1754\ W$$

where ρ_T is a normalization factor accounting for the significant variation in on-resistance with temperature. A value of 1.5 is selected.

Switch B operates in buck region as the synchronous rectifier. Its power dissipation at maximum output current is given by:

$$P_{B(BUCK)} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \cdot {I_{OUT(MAX)}}^2 \cdot \rho_T \cdot R_{DS(ON)} = 0.0071\ W$$

Switch C operates in boost region as the control switch. Its power dissipation at maximum current is given by:

$$P_{C(BOOST)} = \frac{(V_{OUT} - V_{IN}) \cdot V_{OUT}}{{V_{IN}}^2} \cdot {I_{OUT(MAX)}}^2 \cdot \rho_T \cdot R_{DS(ON)} + k \cdot {V_{OUT}}^3 \cdot \frac{I_{OUT(MAX)}}{V_{IN}} \cdot C_{RSS} \cdot f = 0.2171\ W$$

where the constant k has an empirical value of 1.7.

For switch D, the maximum power dissipation happens in boost region, when its duty cycle is higher than 50%. Its maximum power dissipation at maximum output current is given by:

$$P_{D(BOOST)} = \frac{V_{OUT}}{{V_{IN}}^2} \cdot {I_{OUT(MAX)}}^2 \cdot \rho_T \cdot R_{DS(ON)} = 0.0071\ W$$

From a known power dissipated in the power MOSFET, its junction temperature is given by:

$$T_J = T_A + P \cdot R_{TH(JA)}$$

Obtaining the following results:

$T\_A = 25\ °C$	$T_{J,A} = 35.52\ °C$	$T_{J,B} = 25.42\ °C$	$T_{J,C} = 35.85\ °C$	$T_{J,D} = 25.35\ °C$
$T_A = 80\ °C$	$T_{J,A} = 90.52\ °C$	$T_{J,B} = 80.42\ °C$	$T_{J,C} = 90.85\ °C$	$T_{J,D} = 80.35\ °C$

5.1.1.7. Top gate MOSFET driver supply

The top MOSFET drivers, TG1 and TG2, are driven between their respective SW and BST pin voltages. The boost voltages are biased from floating bootstrap capacitors C_{BST1} and C_{BST2}, which are normally recharged through both the external and internal bootstrap diodes when the respective top MOSFET is turned off. Both capacitors are charged to the same voltage as the $INTV_{CC}$ voltage. The bootstrap capacitors C_{BST1} and C_{BST2}, need to store about 100 times the gate charge required by the top switches A and D.

5.1.1.8. Input capacitors

The C_{IN} capacitor network (Fig. 17) must have low enough ESR and be sized to handle the maximum RMS current. The maximum RMS current happens in the buck region and is given by:

$$I_{RMS} \approx I_{OUT(MAX)} \cdot \frac{V_{OUT}}{V_{IN(MAX)}} \cdot \sqrt{\frac{V_{IN(MAX)}}{V_{OUT}} - 1} = 0.7618\ A$$

An aluminium bulk capacitor is placed at the input to control the voltage deviation when the converter reacts to a load transient at the output. The ripple current flows in the bulk capacitor, causing power dissipation in its ESR. Adding a parallel combination of ceramic capacitors reduces the ripple input voltage amplitude due to their extremely low ESR, reducing then the RMS current in the bulk capacitors and so the power loss.

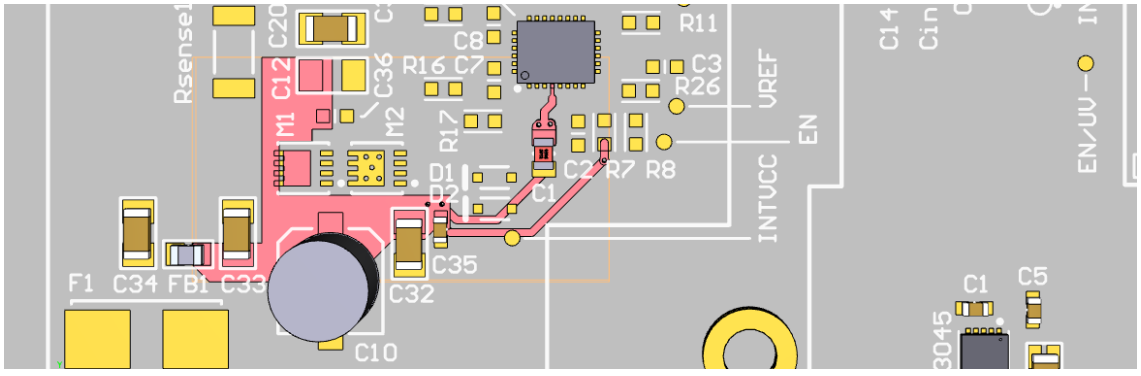


Figure 17. Input capacitors LT8390A

5.1.1.9. Output capacitors

The C_{OUT} capacitor network (Fig. 18) has to be able of reducing the output voltage ripple. A parallel combination of capacitors is used to achieve high capacitance and low equivalent series resistance (ESR). The maximum steady state ripple due to charging and discharging the bulk capacitance is given by:

$$\Delta V_{CAP(BOOST)} = \frac{I_{OUT(MAX)} \cdot (V_{OUT} - V_{IN(MIN)})}{C_{OUT} \cdot V_{OUT} \cdot f} = 3.8675\ mV$$

$$\Delta V_{CAP(BUCK)} = \frac{V_{OUT} \cdot \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)}{8 \cdot L \cdot f^2 \cdot C_{OUT}} = 0.2262\ mV$$

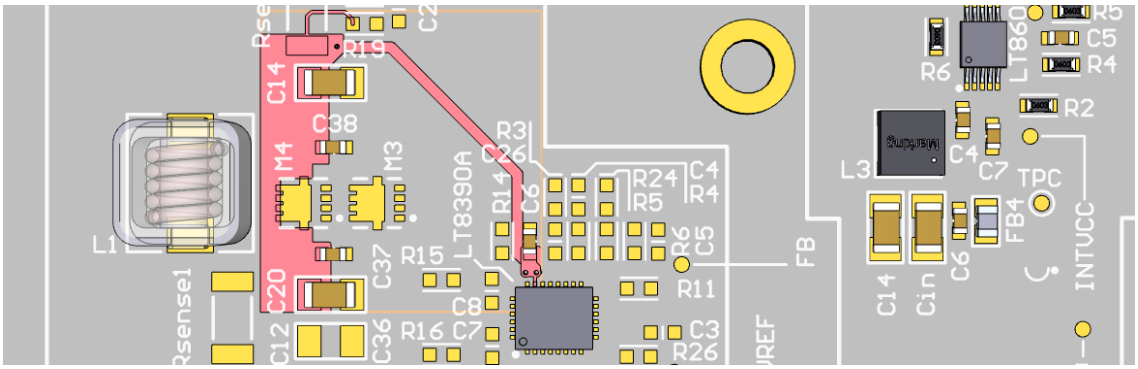


Figure 18. Output capacitors LT8390A

5.1.2. Step-Down Regulator: LT8610

5.1.2.1. Output voltage

The output voltage is programmed with the feedback resistor network tied to the FB pin, which is internally regulated at 0.970 V, according to:

$$V_{OUT} = 0.970\ V \cdot \frac{R_4 + R_5}{R_5} = 11.91\ V$$

where R4 is a 1 Mohm resistor and R5 is a 88.7 kohm resistor. These large resistor values are used to obtain a low input quiescent current and good light-load efficiency.

5.1.2.2. Operating frequency

The highest switching frequency for a given application can be calculated as follows:

$$f_{SW(MAX)} = \frac{V_{OUT} + V_{SW(BOT)}}{t_{ON(MIN)}(V_{IN} - V_{SW(TOP)} + V_{SW(BOT)})} = 9.04\ MHz$$

This equation shows that a slower switching frequency is necessary to accommodate a high V_{IN}/V_{OUT} ratio.

The switching frequency of the LT8610 is set by a resistor from the RT pin to ground. The selected value is 18.2 kΩ, corresponding to a 2 MHz switching frequency.

5.1.2.3. Inductor

A good first choice for the inductor value is:

$$L = \frac{V_{OUT} + V_{SW(BOT)}}{f_{SW}} = 6.075\ \mu H$$

Choosing a smaller value than the calculated implies that the LT8610 operates with higher ripple current, but allows the use of a physically smaller inductor or one with a lower DCR, resulting in higher efficiency. To avoid overheating and poor efficiency, an inductor must be chosen with an RMS current rating that is greater than the maximum expected output load of the application. In addition, the saturation current rating of the inductor must be higher than the load current plus ½ of in inductor ripple current:

$$I_{L(PEAK)} = I_{LOAD(MAX)} + \frac{1}{2}\Delta I_L = 2.819\ A$$

The peak-to-peak ripple current in the inductor can be calculated as:

$$\Delta I_L = \frac{V_{OUT}}{f \cdot L} \cdot (1 - \frac{V_{OUT}}{V_{IN(MAX)}}) = 1.637\ A$$

The selected inductor is a shielded inductor of 2.2 µH with a R_{DC} of 11.2 mΩ and a current rating of 7.5 A.

5.1.2.4. Input capacitors

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor (Fig. 19) is required to reduce the resulting voltage ripple at the LT8607 and to force this very high frequency switching current into a tight local loop, minimizing EMI.

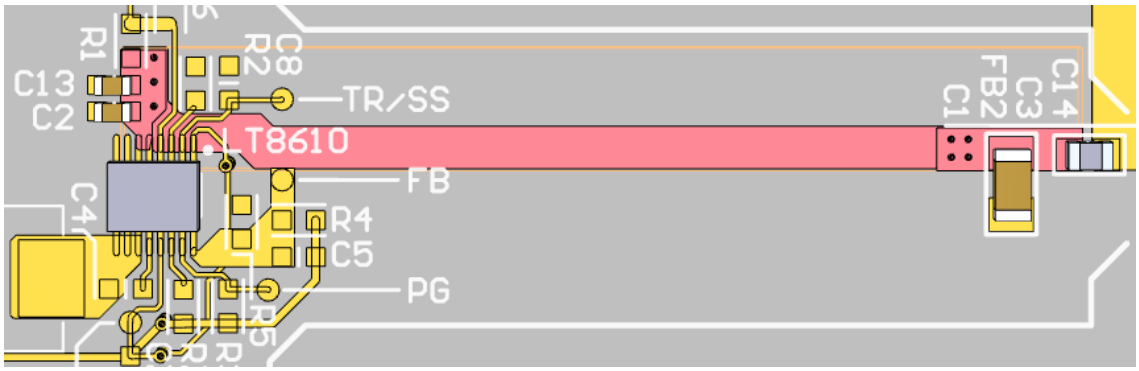


Figure 19. Input capacitors LT8610

5.1.2.5. Output capacitors

The output capacitor (Fig. 20) has two essential functions. Along with the inductor, it filters the square wave generated by the LT8610 to produce the DC output. It determines the output ripple. The second function is to store energy in order to satisfy transient loads and stabilize the LT8607's control loop. Ceramic capacitors have very low ESR and provide the best ripple performance. A good starting value is:

$$C_{OUT} = \frac{100}{V_{OUT} \cdot f} = 4.17\ \mu F$$

Transient performance is improved with a capacitor network, resulting in a total capacitance of 52.7 µF, and a phase-lead capacitor of 4.7 pF placed between V_{OUT} and FB.

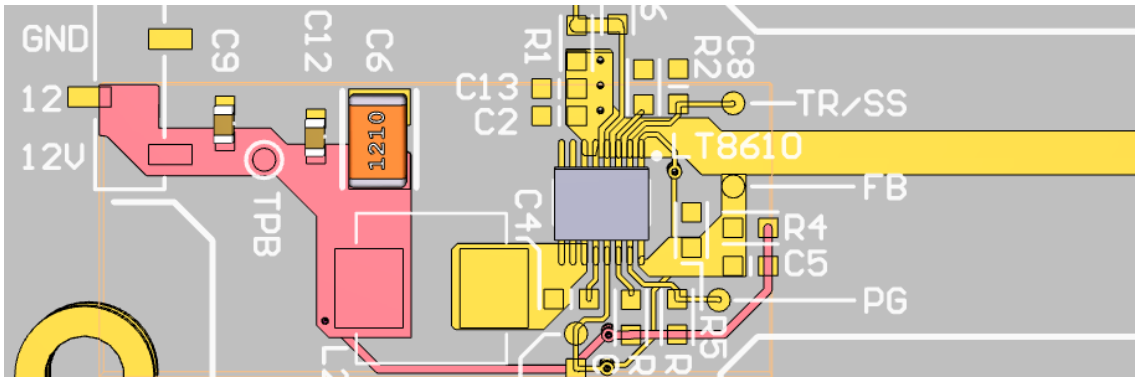


Figure 20. Output capacitors LT8610

5.1.3. Step-Down Regulator: LT8607

5.1.3.1. Output voltage

The output voltage is programmed with a resistor divider between the output and the FB pin, which is internally regulated at 0.778 V:

$$V_{OUT} = 0.778\ V \cdot \frac{R_4 + R_5}{R_5} = 13.05\ V$$

where R4 is a 1 MΩ resistor and R5 is a 63.4 kΩ resistor.

5.1.3.2. Enable

The rising threshold of the enable comparator is 1.05 V and supports up to 42 V. The EN pin is controlled externally with a 3.3 V voltage. A pull-down resistor is included to shut down the LT8607 when the external control is disabled.

5.1.3.3. Operating frequency

The highest switching frequency for a given application can be calculated as follows:

$$f_{SW(MAX)} = \frac{V_{OUT} + V_{SW(BOT)}}{t_{ON(MIN)}(V_{IN} - V_{SW(TOP)} + V_{SW(BOT)})} = 12.55\ MHz$$

The switching frequency of the LT8607 is set by a resistor from the RT pin to ground. The selected value is 18.2 kΩ, corresponding to a 2 MHz switching frequency.

5.1.3.4. Inductor

A good first choice for the inductor value is:

$$L = \frac{V_{OUT} + V_{SW(BOT)}}{f_{SW}} \cdot 2 = 13.12\ uH$$

To avoid overheating and poor efficiency, an inductor must be chosen with an RMS current rating that is greater than the maximum expected output load of the application. In addition, the saturation current rating of the inductor must be higher than the load current plus ½ of in inductor ripple current:

$$I_{L(PEAK)} = I_{LOAD(MAX)} + \frac{1}{2}\Delta I_L = 0.462\ A$$

The peak-to-peak ripple current in the inductor can be calculated as:

$$\Delta I_L = \frac{V_{OUT}}{f \cdot L} \cdot (1 - \frac{V_{OUT}}{V_{IN(MAX)}}) = 0.024\ A$$

The selected inductor is a shielded inductor of 10 µH with an R_{DC} of 100 mΩ and a current rating of 2.7 A.

5.1.3.5. Input capacitors

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor (Fig. 21) is required to reduce the resulting voltage ripple at the LT8607 and to force this very high frequency switching current into a tight local loop, minimizing EMI.

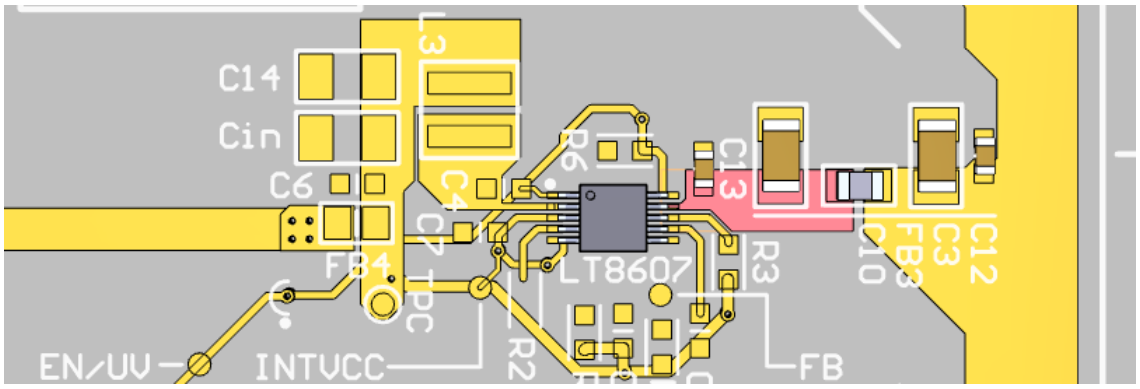


Figure 21. Input capacitors LT8607

5.1.3.6. Output capacitors

The output capacitor (Fig. 22) has two essential functions. Along with the inductor, it filters the square wave generated by the LT8607 to produce the DC output. It determines the output ripple. The second function is to store energy in order to satisfy transient loads and stabilize the LT8607's control loop. Ceramic capacitors have very low ESR and provide the best ripple performance. A good starting value is:

$$C_{OUT} = \frac{100}{V_{OUT} \cdot f} = 3.85\ \mu F$$

Transient performance is improved with a capacitor network, resulting in a total capacitance of 26.8 µF, and a feedforward capacitor of 10 pF placed between V_{OUT} and FB.

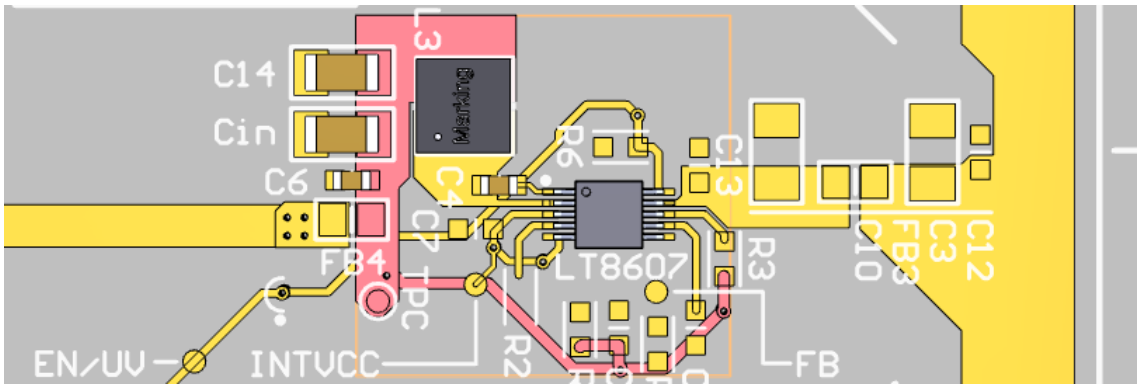


Figure 22. Output capacitors LT8607

5.1.4. LDO Voltage Regulator: LT3045

5.1.4.1. Output voltage

The LT3045 incorporates a precision 100 µA current source flowing out of the SET pin. Connecting a resistor from SET to ground generates a reference voltage. Internally, this voltage is tied to the inverting input of the error amplifier. This produces a low impedance version of this voltage on the noninverting input, the OUTS pin, which is externally connected to the OUT pin.

$$V_{OUT} = 100\ \mu A \cdot R_5 = 12.10\ V$$

where R3 is a 121 kΩ resistor.

A bypass capacitor is added to the SET pin to prevent unwanted signals to couple into the SET pin and cause unpredictable behavior.

5.1.4.2. Stability and input capacitance

The LT3045 is stable with a minimum 4.7 µF input capacitor. The input capacitance implemented (Fig. 23) consists on a 4.7 µF and a 0.1 µF ceramic capacitors.

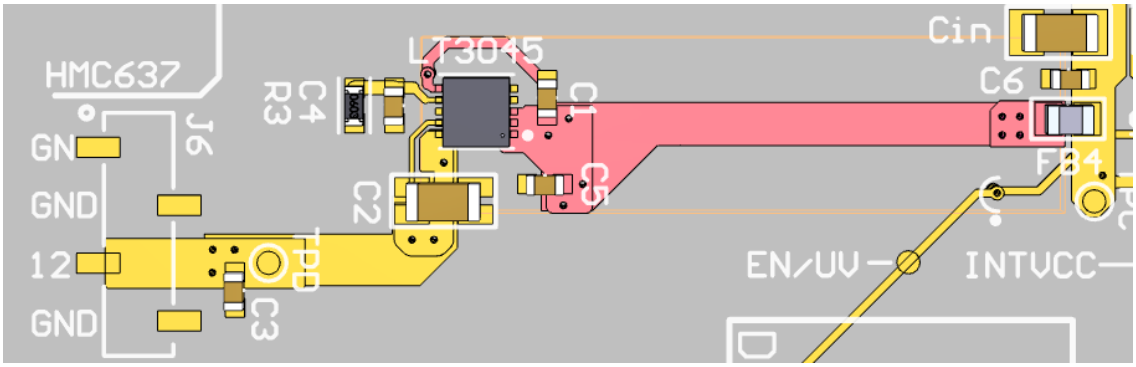


Figure 23. Input capacitors LT3045

5.1.4.3. Stability and output capacitance

The LT3045 requires an output capacitor for stability. A minimum 10 µF capacitance with an ESR below 20 mΩ and ESL below 2nH is required for stability. Given the high PSRR and low noise performance attained using a single 10 µF ceramic output capacitor, larger values of output capacitor only marginally improve the performance (low ESR and low ESL). Capacitor DC bias characteristics tend to improve as component case size increases. A 10 µF ceramic capacitor in a 1206 case is selected. A second 0.1 µF capacitor is added close to the output port (Figure 24).

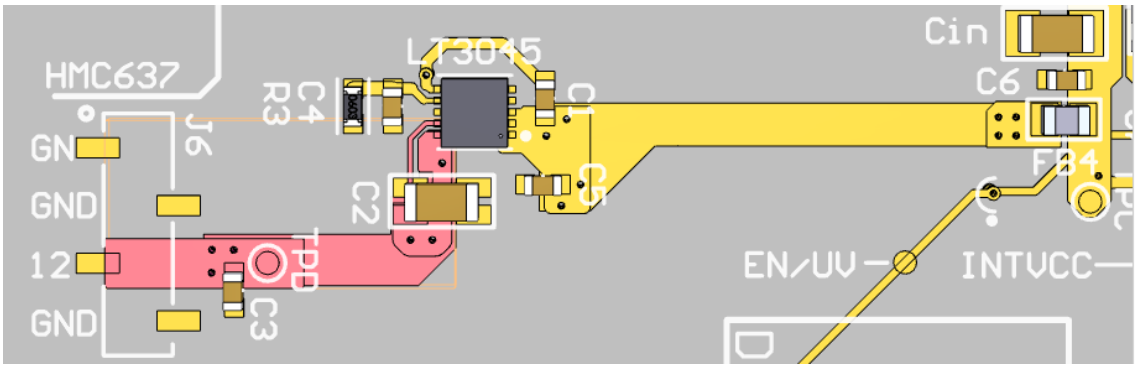


Figure 24. Output capacitors LT3045

5.1.5. LDO Voltage Regulator: TPS7A47

5.1.5.1. Output voltage, adjustable operation mode

The nominal output voltage is set using two external resistors. For high accuracy applications, the recommended value for R_2 is 10 kΩ. R_i is calculated using the following equation:

$$R_1 = \frac{V_{OUT} - V_{REF}}{I_{FB} + \frac{V_{REF}}{R_2}}$$

where V_{REF} is 1.4 V and I_{FB} is 350 nA. The calculated value is 189.5 kΩ. This value is achieved with the combination of two resistors in series, R_{11} and R_{12}, 84.5 kΩ and 105 kΩ respectively. 0.1% tolerance resistors are chosen to minimize the effects of resistor inaccuracy. The output voltage is then:

$$V_{OUT} = (I_{FB} + \frac{V_{REF}}{R_2}) \cdot R_1 + V_{REF} = 27.99\,V$$

5.1.5.2. Enable

The EN pin is controlled externally with a 3.3 V voltage. No pull-down resistor is needed since it is included internally. The TPS7A47 is shut down until the external control is enabled.

5.1.5.3. Input and output capacitor requirements

The TPS7A47 is designed and characterized for operation with ceramic capacitors of 10 μF or greater at the input and output. Optimal noise performance is achieved using a total of 50 μF at the output, by the means of five 10 μF capacitors in parallel.

5.1.5.4. Noise reduction capacitor

The noise reduction capacitor forms an RC filter for the noise that might be amplified by the control loop and appear at the output. An 1 μF capacitor is selected.

5.2. LAYOUT CONSIDERATIONS

5.2.1. Routing

- Route critical tracks first [14].
- In high current paths, use wider tracks, multiple vias connecting layers and ensure enough pins to carry the current.

- Keep length of tracks as short as possible to reduce inductance, expressly when connecting capacitive components. Special attention must be paid in feedback tracks and input/output decoupling filters.
- Connect input and output traces using planes to minimize trace resistance.
- Keep switching loop as small as possible (EMI).

5.2.2. Selection and placing of components

- Use ferrite beads on power lines.
- Place input and output capacitors as close as possible to the ICs to maximize their decoupling efficiency. Prioritizing the smaller capacitances.
- Choose low-ESR ceramic capacitors.
- Include bulk capacitors to control the voltage deviation at the input when the regulator reacts to a quick change in current demand.
- Place power MOSFETs as close as possible to the inductor to reduce the radiating switch node.
- Select through-hole style connectors. They are sturdier.
- Ensure that components are run below electrical over-stress.
- Select component parameters allowing a safe derating factor.
- Choose X7R and X5R capacitors. The letter code “R” stands for 10% change of capacitance over the temperature range.

5.2.3. Thermal considerations

- Include thermal reliefs in through-hole pads.
- Flood unused areas with copper. Components exceeding their design temperature benefit from additional conducting the heat away.
- Dedicate at least one layer to ground plane (increase heat dissipation and reduce loop inductance).
- Place heat generating devices such as linear regulators apart from each other.
- Place vias under ICs to remove heat.

5.3. EMIS REDUCTION

Since the PCB powers an RF system, EMI must be controlled.

5.3.1. Switching loops

Ground is not a current sink. Currents return to their sources, creating loops. In the loops, the AC current flows around an area and creates the magnetic field part of a normal dipole antenna. Currents follow the least impedance paths. This means lowest resistance paths at low frequencies and lowest inductance paths at high frequencies [15, 16].

The term hot loop is related to those loops where a fully switched AC current flows. These loops have the highest AC and EMI energy. In switching converters, the switching loops are the hot loops. In the buck typology, the hot loop covers the input capacitor and the input switches. In the buck-boost, there is also a hot loop between the output capacitor and the output switches.

By identifying the most conflicting loops and reducing their areas, EMI can be drastically reduced. Besides, a solid reference plane with minimum distance to the hot loop is one of the most effective ways to reduce EMI. Other considerations are: keeping expose lengths short, burying traces between planes whenever possible (no direct emissions from traces with no exposed length), and placing the smaller decoupling capacitor as close as possible to the hot loop with larger packages right behind it.

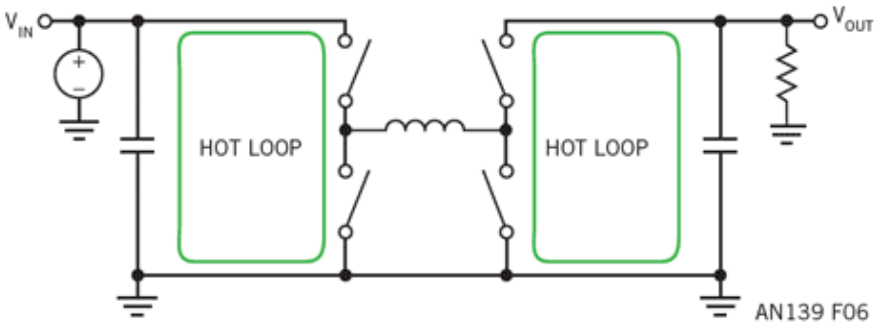


Figure 25. Four-switch buck-boost topology [16]

Figures 26 and 27 show the final layout. The input and output nets, represented in yellow, connect the input/ output capacitors to the drains of the top MOSFETs and to the VIN/VOUT pins. The pink nets are the switching nets, connecting the SW1/SW2 pins to top MOSFETs' sources and bottom MOSFETs' drains.

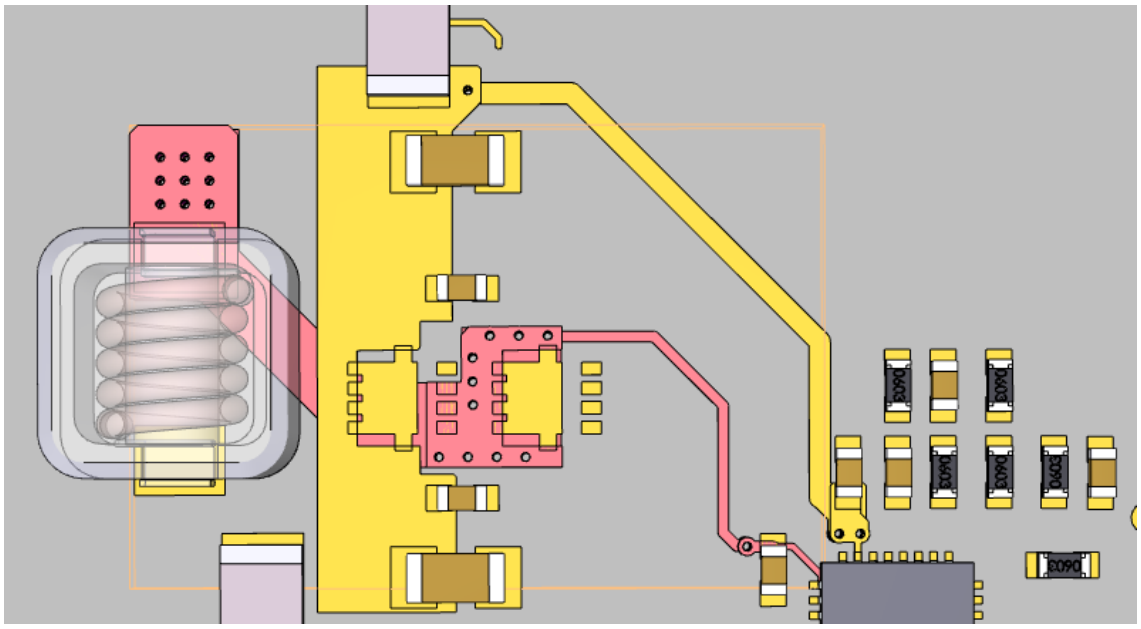


Figure 26. Output hot loop

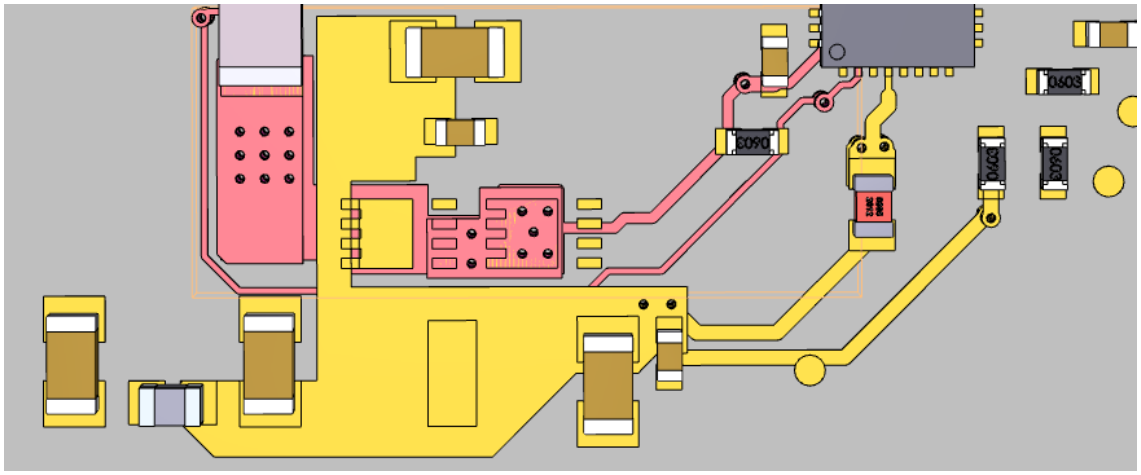


Figure 27. Input hot loop

5.3.2. Decoupling caps

Surface-mount devices (SMD) are better than leaded devices in dealing with RF energy because of the reduced inductances and closer component placements available. Connecting decoupling capacitors directly to the ground plane helps reduce EMI.

5.3.3. Filters

In buck topologies, the input side is much noisier than the output. The location of LC filters at the input of buck regulators, instead of between the output and the load, achieves greater EMI reduction

There are five Pi (Π) filters in the PCB, each one as an input filter for each functional block (A to E). These filters consist of MLCCs and ferrite beads. The insertion loss achieved is represented in Figure 28. To obtain this graph, use has been made of the noise filter design tool offered by Murata on its website.

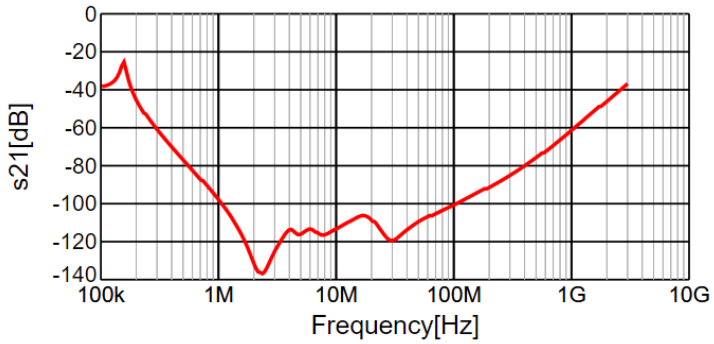


Figure 28. Insertion loss, Pi filter

Ferrite beads are useful for decoupling, since above a certain frequency they become resistive. They add isolation and decoupling for high frequency noise, being beneficial for low-pass LC filters. A ferrite bead will be located in series with the supply pin of each IC (LT8390A, LT8607, LT8614, LT3045 and TPS7A47), protecting them from external noise and the rest of the system from their internal noise. A more practical use of these ferrite beads is the possibility of disconnecting the ICs by removing the beads from the board. Figure 29 shows the behavior of the MPZ2012S300AT000 by TDK, the model selected for the PCB.

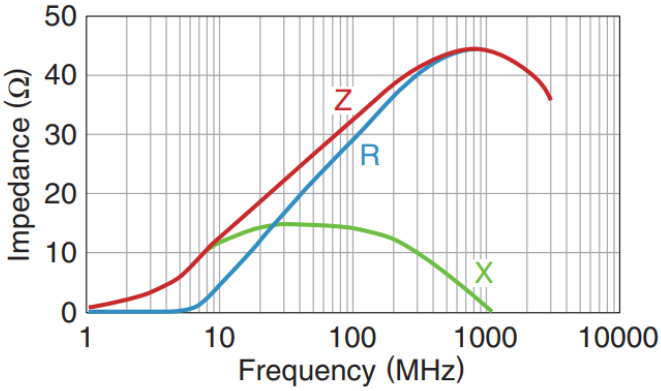


Figure 29. Ferrite bead behavior [17]

5.4. LAYOUT DESIGN

The first step is roughly defining the layout. The functional blocks and mayor components are deliberately placed considering the critical tracks and planes from the beginning and allowing sufficient spacing among components. For each block, the manufacturers' PCB layout recommendations have been taken into consideration [8, 9, 10, 11, 12, 13]. The input and output connectors are placed on one side of the board, while the control connector is placed closer to its linked components. The preliminary layout is represented in Figure 30.

The PCB dimensions match UDOO's board dimensions.

The PCB manufacturer, Eurocircuits, provides design classification parameters that define the lower limit measurements for the design. These include track width, track to track distance, annular ring size and hole dimensions. The technology 6C is selected for this design and its parameters are included in Altium's Rule Manager to prevent future problems while manufacturing.

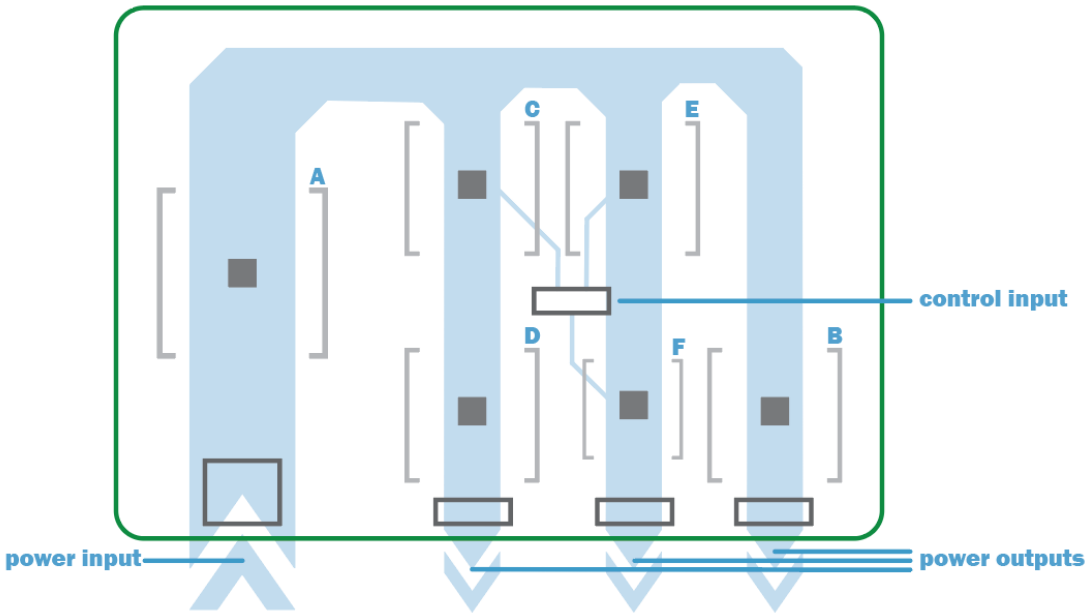


Figure 30. PCB's preliminary layout

Once all the components are properly placed (Fig. 31), connections are made: tracks, copper planes and vias are included.

Finally, completing a design rule check ensures that the board is ready to be manufactured.

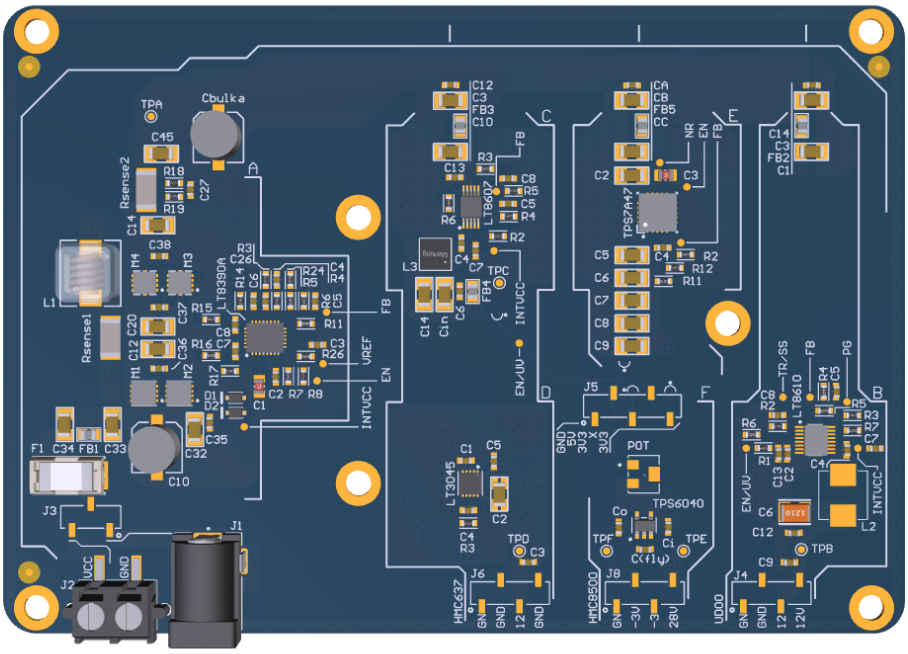


Figure 31. Top view from Altium's PCB visualizer

5.5. PCB LAYERS

The electrical information is contained in four copper layers. The first layer is dedicated to power and signals. The second and forth layers are dedicated to ground planes. Additional power and signal tracks are included in the third layer. Figure 32 describes the whole layer stack in detail.

The following figures (33, 34, 35, 36) correspond to these copper layers, that represent all the connections between components as they are on the electrical schematics. Copper planes and tracks are represented in ochre color, whereas white represents unfilled areas.

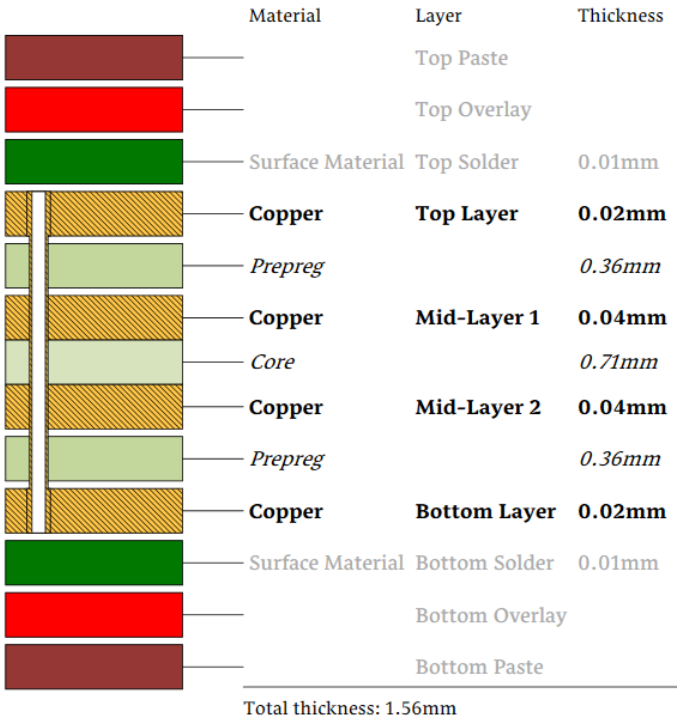


Figure 32. Layer stack

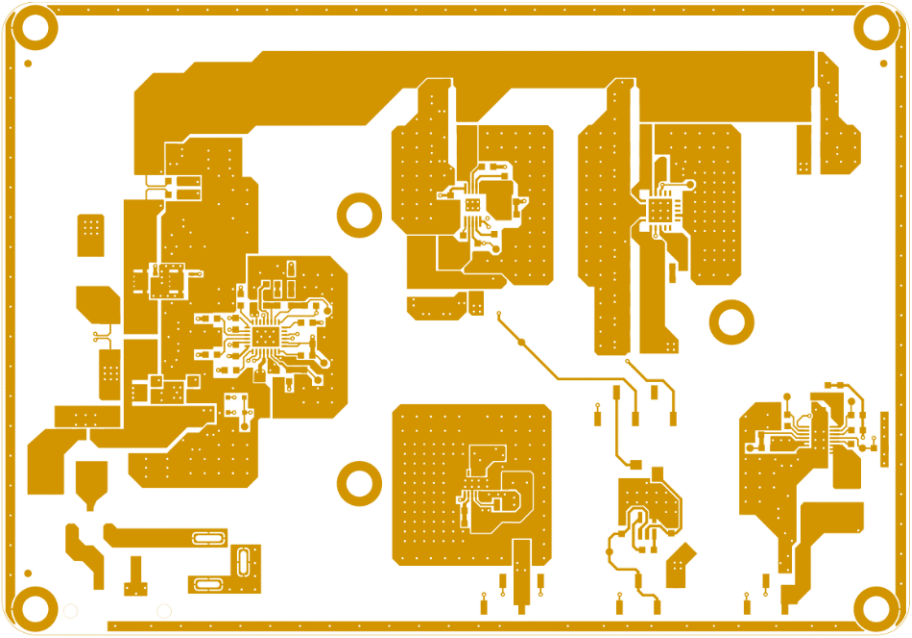


Figure 33. Top layer, power and signals

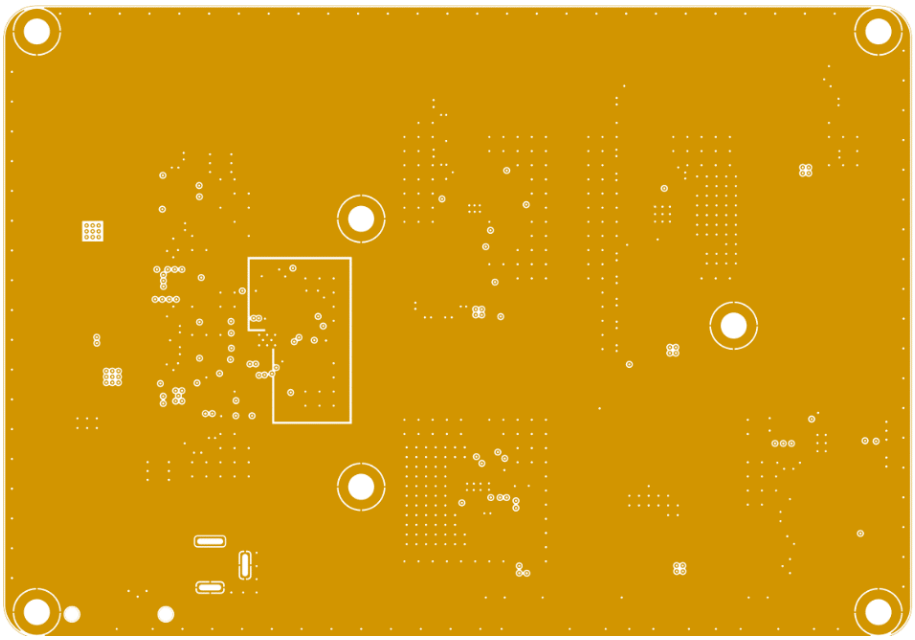


Figure 34. Mid-Layer 1, ground plane

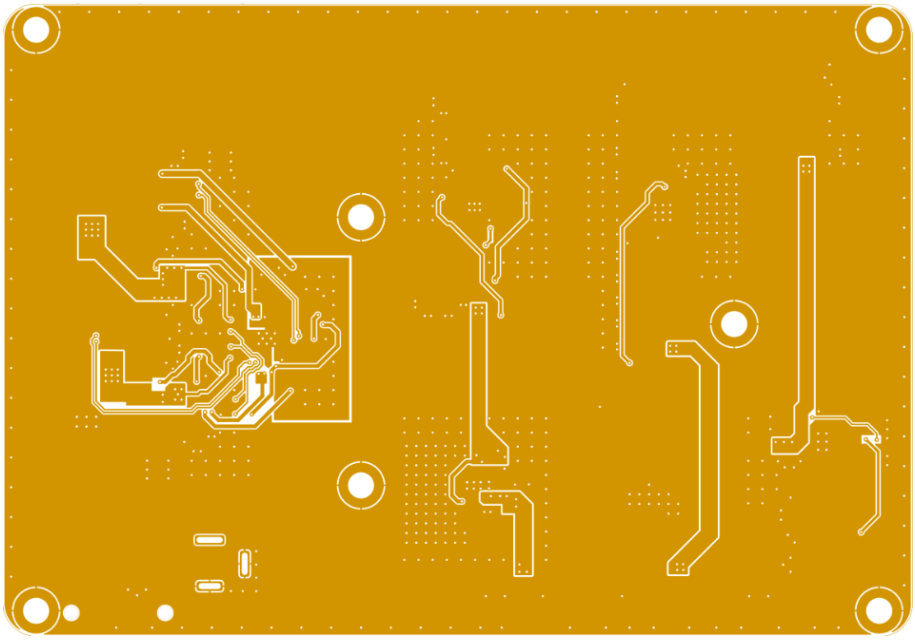


Figure 35. Mid-Layer 2, power and signals

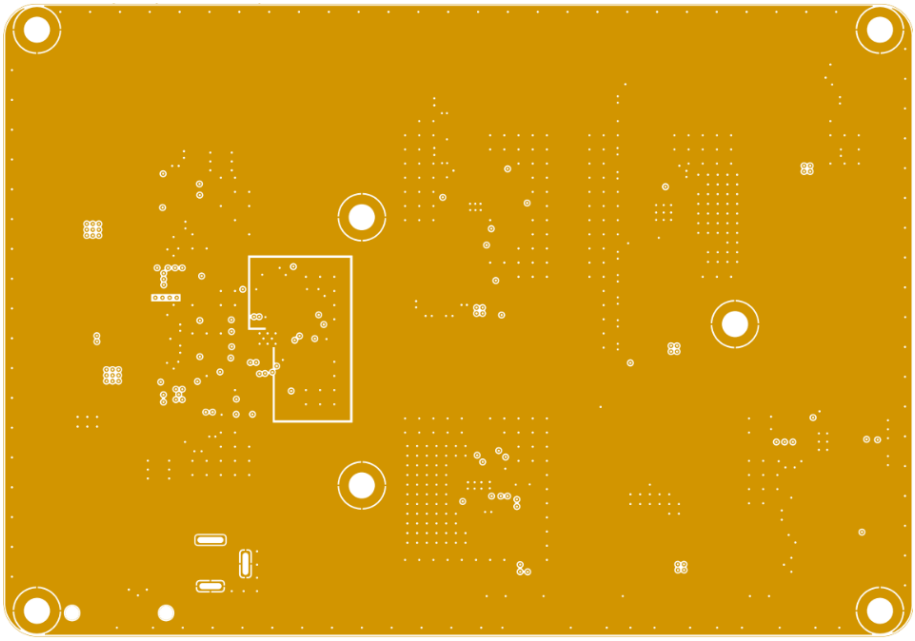


Figure 36. Bottom layer, ground plane

6. PCB IMPLEMENTATION

During the implementation stage, the PCB prototypes are assembled and tested. The bill of materials (BOM) is included in Appendix B.

6.1. PCB FIRST PROTOTYPE

For the assembly of the SMDs, use is made the reflow soldering technique. First, solder paste is applied to the PCB with the help of its stencil, and then the components are placed by hand (Fig. 36). Once all the components are placed, the PCB goes to the reflow oven. Finally, the through-hole components are soldered with the help of a soldering iron.

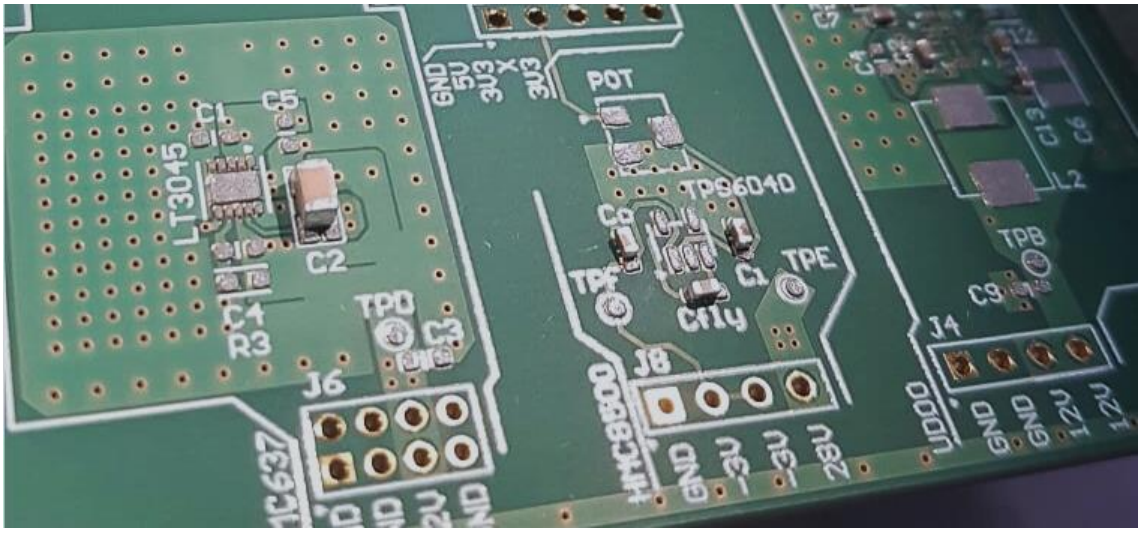


Figure 37. Detail of solder paste on PCB pads

The first test show up that the board is not operating properly: there is no significant voltage at the outputs. In an attempt to find where the fault is, a systematic inspection is conducted.

The output voltage in block A is 1.44 V, far from the 30 V that should deliver. The malfunction may be caused by different factors, the ones that are considered are: defects during manufacturing (faulty welded connections), defective components or components that might have been short-circuited or suffered an electrostatic discharge (ESD), and mistakes in the schematic layout.

The power MOSFETs' terminals are checked and no switching voltages are found. Giving these components a close look, there is no way to assure that the pins are properly soldered to the pads, so it is decided to de-solder and resolder these components (Fig. 38).

For the rework, use is made of a PCB pre-heater and a heat gun. This procedure is completed with some difficulty, since the components are connected to big planes (V_{IN} and GND) and several layers. Thus, they are exposed to prolonged high temperatures, far from ideal.

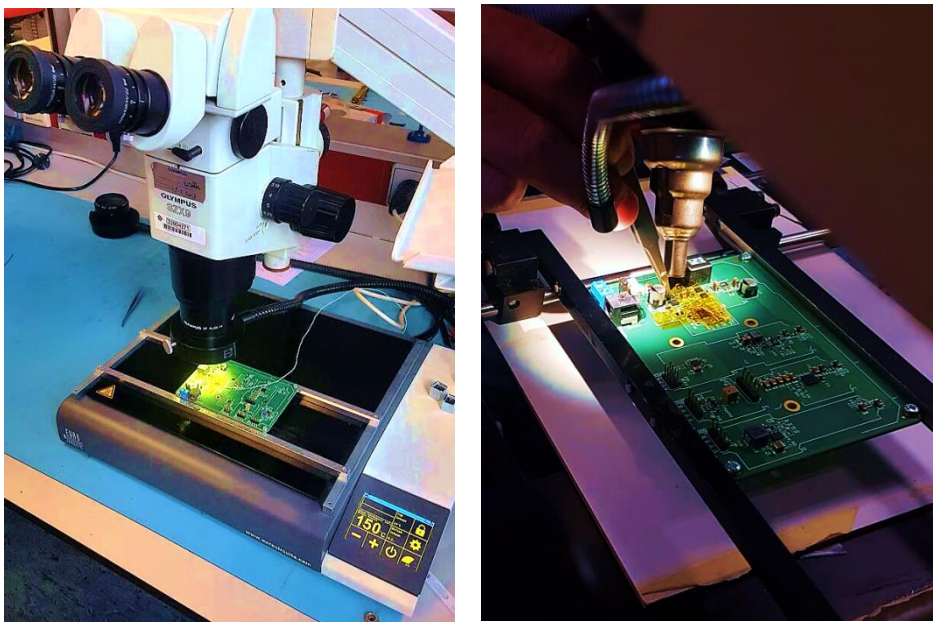


Figure 38. PCB pre-heater and heat gun during rework

The PCB is then tested again (Fig. 39), obtaining the same results. All the schematics are double-checked, no mistakes are found. The voltages at every pin, pad and connection within the A block are checked. While these values indicate that the components are connected in the right way, they are too low. The voltage reference output (V_{REF}) pin provides, according to the datasheet, an accurate 2 V reference. However, the measured voltage is 0.33 V. At this point, nothing can be done other than replacing the IC.

The PCB is then connected to a power supply at the test point A. This allows to test the other components as if the A block were delivering 30 V. C, D and F blocks work as expected.

B block presents a similar problem to A block. The output voltages are way too low. Since the enable pin is high, above 1 V, the switching regulator should be active.

The internal power drivers and control circuits in the LT8614 are powered from the internal regulator bypass pin ($INTV_{CC}$) voltage, which is powered by an internal 3.4 V regulator. During the test, 0.087 V are measured at this pin. This seems to indicate that the IC does not work. This could be as a result of an ESD or defective solder.

The E block presents a different malfunction. In this case, values around 9.6 V are measured at the output, with small variations depending on the input voltage. Because the IC in this

block is an LDO instead of a switch regulator, the functional diagram is simpler and the problem is easier to track.

The TPS7A47 is on because both the enable pin and the UVLO are above the respective voltage thresholds. To exclude the possibility of having designed, by mistake, the output voltage at 9.7 V, the feedback pin is checked. This pin should operate at 1.4 V, but it is measured at 0.488 V. This value also shows that the ratio between V_{OUT} and V_{FB} is the correct.

$$\frac{V_{OUT\_design}}{V_{FB\_design}} = \frac{28\ V}{1.4\ V} \cong \frac{V_{OUT\_test}}{V_{FB\_test}} = \frac{9.7\ V}{0.488\ V}$$

The noise reduction pin voltage is also measured at 0.513 V, being 1.4 V the typical value.

The most likely justification is that these ICs are malfunctioning as a result of an ESD.

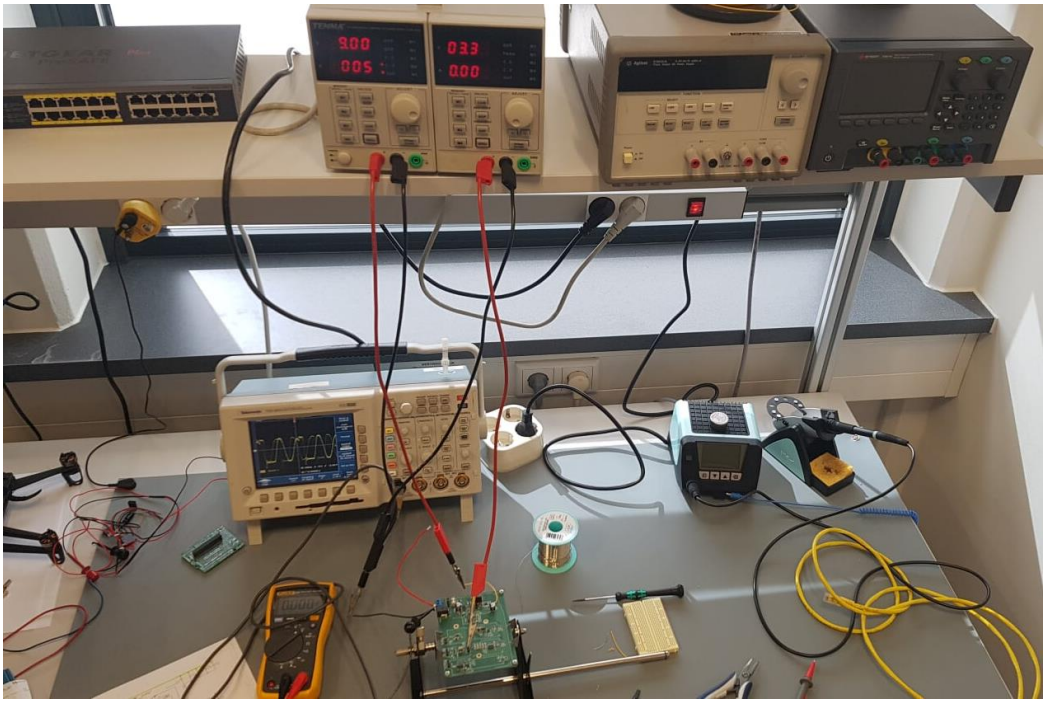


Figure 39. PCB testing

6.2. PCB SECOND PROTOTYPE

Some layout and component modifications are implemented to improve PCB's testing and assembly.

In the first prototype, soldering the through-hole components was challenging for those pins connected to ground planes, so except for the jack connector, all of the previous through-hole components are substituted by SMD.

The LT8614 IC is replaced by LT8610, which is presented in a package with leads.

Test points are added for all the reference and feedback voltages, to easy the testing process.

The whole process of assembly is repeated again on the second board (Fig. 40).

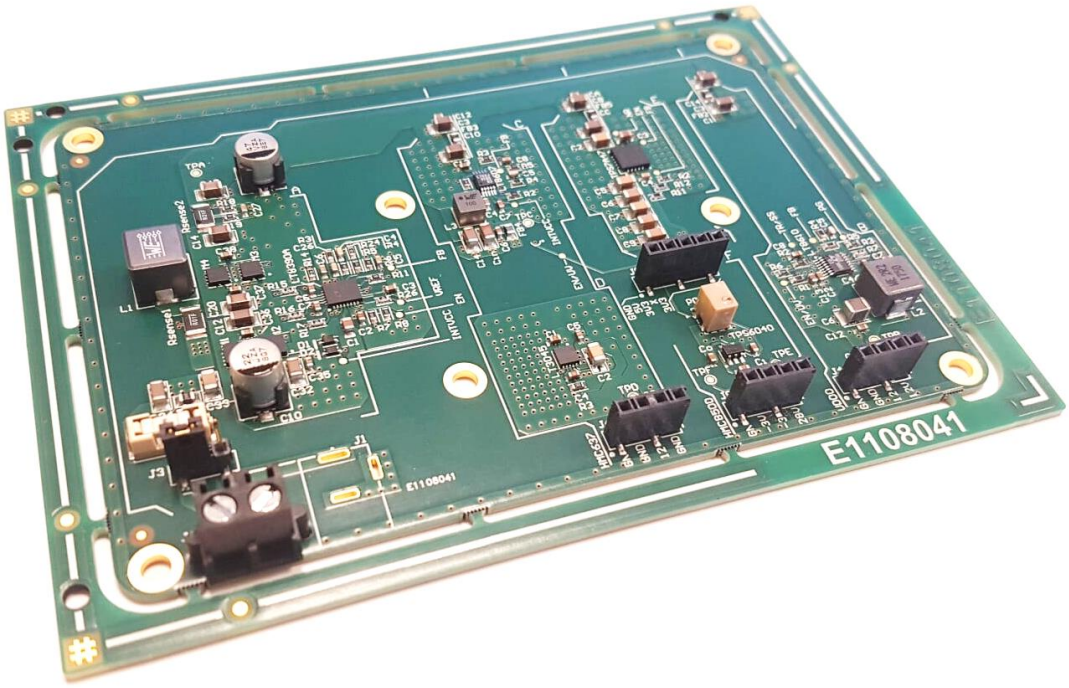


Figure 40. Second prototype

While verifying its operation, the reference voltage in the LT8390's VREF pin was far from the accurate 2V that the datasheet specifies. A connection from SS to VREF pins was causing a short-circuit, which was easily fixed on the software (Fig. 41). These pins may be connected through a resistor or not be connected at all.

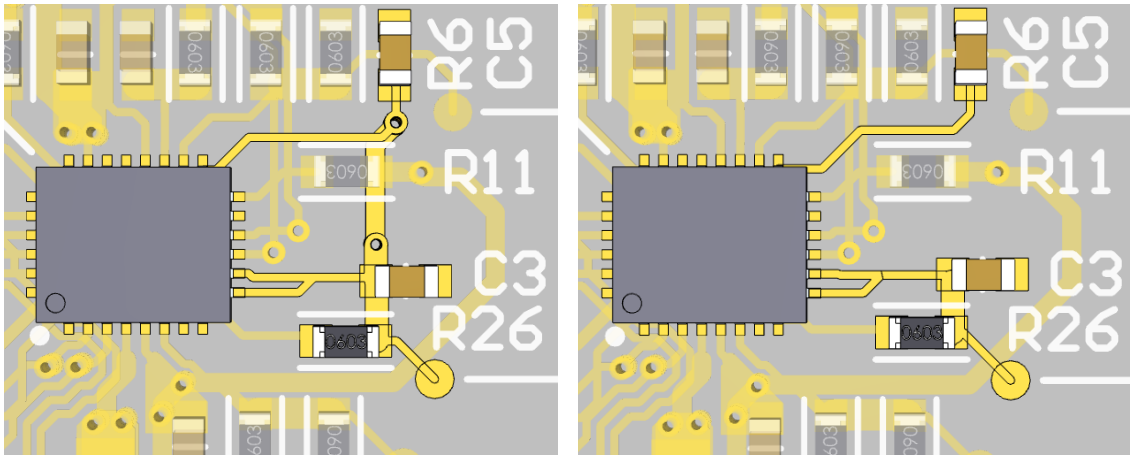


Figure 41. Short-circuit fix

The on-board modification involved scraping the track from SS to C5 (disconnecting SS from VREF), repositioning C5 and soldering a thin wire from the SS pin to C5 (Fig. 42).

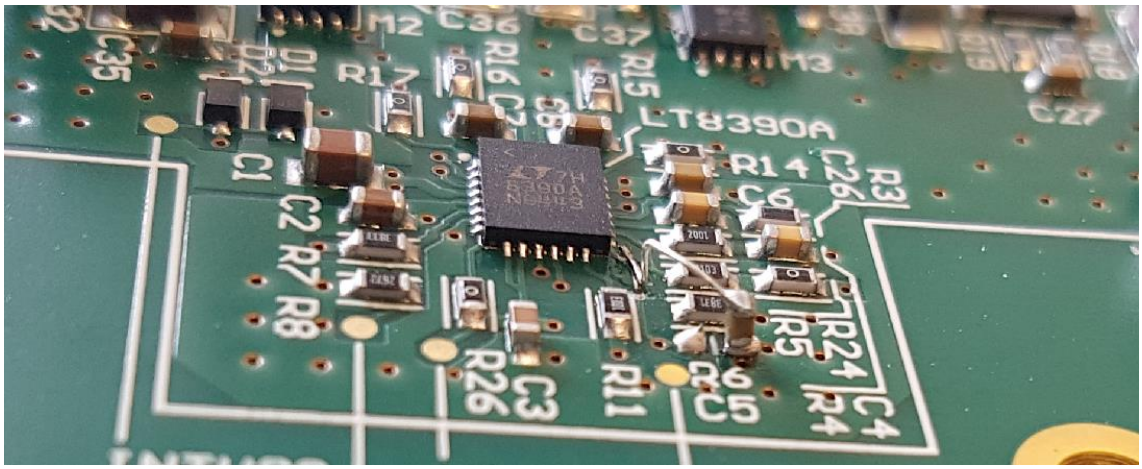


Figure 42. Reposition of C5

Once the fix was made, the VREF was tested again, showing 2 V. Then, all the test points included in the PCB were measured, providing very accurate values according to the designed voltages.

7. CONCLUSIONS

The final result is the successful design, development and assembly of a working power supply PCB.

Unfortunately, the time was limited due to the problems encountered with the first prototype, and the time required for the second fabrication and assembly, made it impossible to perform further tests. Nevertheless, some bases have been set for the continuation of the hardware setup, and are referred in the future directions section.

With regard to the economic side of the project, further reduction on global costs are achieved while working with a larger scale production, PCB fabrication prices reduce significantly with large orders. Another way of reducing cost might be the implementation of the PA stage as an independent PCB or even included with the power management in one single board, instead of purchasing off-the-shelf components.

7.1. FUTURE DIRECTIONS

The continuation of this work towards the final product includes testing of the power supply PCB (output voltage accuracy, efficiency and noise levels), interconnection of the subsystems explained in chapter 4 and testing of the RF signal transmission through the system.

Once proven that the RF transmission fulfils the requirements, other components should be selected and added to the assembly (e.g. antennas, communication card). Design for reliability needs to be done, as well, including the selection of a cooling system to ensure adequate thermal management.

Integrating all the components in a closed casing would be the last step.

8. BIBLIOGRAPHY

[1] Sadiku, M.N.O. & Akujuobi, C.M. (2004). "Software-defined radio: a brief overview". *IEEE Potentials*, 23(4), pp. 14-15. Retrieved from https://ieeexplore.ieee.org/document/1343223

[2] Sinha, D., Verma, A. & Kumar, S. (2016). "Software defined radio: Operation, challenges and possible solutions". *10th International Conference on Intelligent Systems and Control*, pp. 1-5. Retrieved from https://ieeexplore.ieee.org/document/7727079

[3] Mitola, J. (1992). "Software Radios. Survey, Critical Evaluation and Future Directions". *IEEE National Telesystems Conference*, pp. 13-15. Retrieved from https://ieeexplore.ieee.org/document/267870

[4] Barfoot, R. (2008). "Exploiting SDR to Help Improve Multinational Military Interoperability". *IET Seminar Cognitive Radio and Software Defined Radio*. London. Retrieved from https://ieeexplore.ieee.org/document/4656350

[5] Cárdaba, L. (2000). "Disipación térmica en semiconductors. Cálculo de radiadores". Retrieved from http://www.lcardaba.com/articles/heatsinks/heatsinks.htm

[6] Ettus Research. (2019). "B200/B210/B200mini/B205mini". Retrieved from https://kb.ettus.com/B200/B210/B200mini/B205mini

[7] Morita, G. (2014). "Ask the Applications Engineer - 41: LDO Operational Corners: Low Headroom and Minimum Load". *Analog Dialogue*, Volume 48. Retrieved from https://www.analog.com/en/analog-dialogue/articles/ldo-operational-corners.html

[8] Linear Technology. (2017). "LT8390A: 60V 2MHz Synchronous 4-Switch Buck-Boost Controller with Spread Spectrum". Retrieved from https://www.analog.com/media/en/technical-documentation/data-sheets/8390afa.pdf

[9] Linear Technology. (2012). "LT8610: 42V, 2.5A Synchronous Step-Down Regulator with 2.5μA Quiescent Current". Retrieved from https://www.analog.com/media/en/technical-documentation/data-sheets/8610fa.pdf

[10] Linear Technology. (2018). “LT8607: 42V, 750mA Synchronous Step-Down Regulator with 2.5µA Quiescent Current”. Retrieved from https://www.analog.com/media/en/technical-documentation/data-sheets/LT8607-8607B.pdf

[11] Linear Technology. (2016). “LT3045: 20V, 500mA, Ultralow Noise, Ultrahigh PSRR Linear Regulator”. Retrieved from https://www.analog.com/media/en/technical-documentation/data-sheets/3045fa.pdf

[12] Texas Instruments. (2014). “TPS7A470x: 36V, 1A, 4µVRMS, RF LDO Voltage Regulator”. Retrieved from http://www.ti.com/lit/ds/symlink/tps7a47.pdf

[13] Texas Instruments. (2015). “TPS6040x: Unregulated 60mA Charge Pump Voltage Inverter”. Retrieved from http://www.ti.com/lit/ds/symlink/tps60402.pdf

[14] Robert Feranec. (n.d.). “Home [YouTube channel]”. Retrieved from https://www.youtube.com/user/matarofe

[15] Archambeault, B. (2010). “EMC Control with PCB Design EMC Control with PCB Design for Working Engineers”. Retrieved from http://www.emcchicago.org/sectfiles/bruce.pdf

[16] Kueck, C. (2013). “Layout Power Supply Boards to Minimize EMI: Part 1”. Retrieved from https://www.powerelectronics.com/power-electronics-systems/layout-power-supply-boards-minimize-emi-part-1

[17] TDK. (2019). “Chip beads for power line MPZ series”. Retrieved from https://product.tdk.com/info/en/catalog/datasheets/beads_commercial_power_mpz2012_en.pdf

APPENDIX A: ABOUT TNO

TNO is the Dutch organization for applied scientific research. It is a not-for-profit knowledge organization that focuses its work on nine areas aligned with the challenges faced by society:

- Buildings, Infrastructure and Maritime,
- The Circular Economy and the Environment,
- Defence, Safety and Security,
- Energy,
- Healthy living,
- Industry,
- Information and Communication Technology,
- Strategic Analysis and Policy,
- Traffic and Transport.

Besides, TNO fulfils the role of innovator on behalf of the Ministry of Defence, the Ministry of Social Affairs and Employment, and the Geological Survey of the Netherlands.

During the internship, I worked for the Electronic Defence department, that is included in the Defence, Safety and Security domain.

The Electronic Defence department focuses on understanding how to use the electromagnetic spectrum (e.g. localizing transmitters, identifying unknown signals), and how to misuse the electromagnetic spectrum (e.g. jamming communications, falsifying positioning information). The department is the strategic research and technology partner of the Ministry of Defence, the Intelligence Services and the Ministry of Justice and Safety. The nature of this work implies that most of their projects are classified.

The department is divided in four expertise areas: electromagnetic signatures, radar electronic warfare, communications electronic warfare, and electro-optical systems and warfare.

APPENDIX B: BILL OF MATERIALS

The bill of materials contains the essential information to procure the components required for the designed PCB.

#	Item	Description	Footprint	Reference	Qnt	Manufacturer	Manufacturer Number	Supplier	Supplier Number	Supplier Price	Total Price
1	Jack connector	DC Power Connector, Jack, 5 A, 2 mm, Through Hole Mount		J1	1	Switchcraft	RAPC722X	Farnell	1608727	€ 1.8700	€ 1.87
2	2 pin connector	Wire-To-Board Terminal Block, 5 mm, 2 Ways, 30 AWG, 14 AWG, 2 mm^2, Screw, SMD		J2	1	Wurth Elektronik	691709710302	Farnell	2405977	€ 2.5400	€ 2.54
3	Strip connector	Board-To-Board Connector, Unshrouded, 2.54 mm, 3 Contacts, Header, TSM Series, SMD		J3	1	SAMTEC	TSM-103-01-L-SV	Farnell	2578716	€ 0.3620	€ 0.36
4	Strip connector	Board-To-Board Connector, 2.54 mm, 5 Contacts, Receptacle, SSM Series, SMD		J5	1	SAMTEC	SSM-105-L-SV	Mouser	200-SSM105LSV	€ 1.3800	€ 1.38
5	Strip connector	Board-To-Board Connector, Vertical, 2.54 mm, 4 Contacts, Receptacle, SSM Series, SMD		J4, J6, J8	3	SAMTEC	SSM-104-L-SV	Farnell	1668251	€ 0.7290	€ 2.19

6	Jumper	Jumper, TSW, MTSW, TLW, DW, EW, ZW, HW, & TSM Series Headers, 2 Ways, 2.54 mm, SMD		Shunt	1	SAMTEC	SNT-100-BK-G	Farnell	2505007	€ 0.1830	€ 0.18
7	Fuse	Fuse, Surface Mount, 6.3 A, OMNI-BLOK Series, 125 VAC, 125 VDC, Very Fast Acting, SMD		F1	1	Littlefuse	015406.3DR	Farnell	1817187	€ 2.6300	€ 2.63
8	Ferrite bead	Ferrite Bead, 0805 [2012 Metric], 30 ohm, 6 A, MPZ Series, 0.01 ohm, ± 10ohm, SMD	0805	FB1, FB2, FB3, FB4, FB5	5	TDK	MPZ2012S300AT000	Farnell	1301678	€ 0.0737	€ 0.37
9	Buck converter	Switching Voltage Regulators 42V, 0.75A Synchronous Step-Down Regulator, SMD	MSOP-10	LT8607	1	Analog Devices / Linear Technology	LT8607IMSE#TRPBF	Mouser	584-LT8607IMSE#TRPBF	€ 5.2700	€ 5.27
10	LDO	LDO Voltage Regulators 20V, 500mA, Ultralow Noise, Ultrahigh PSRR Linear Regulator, SMD	DFN-10	LT3045	1	Analog Devices / Linear Technology	LT3045EDD#PBF	Mouser	584-LT3045EDD#PBF	€ 5.9100	€ 5.91

11	Buck-boost converter	Switching Voltage Regulators 60V Synchronous 4-Switch Buck-Boost Controller, SMD	QFN-28	LT8390A	1	Analog Devices / Linear Technology	LT8390AIUFD#TRPBF	Mouser	584-8390AIUFDTRPBF	€ 1.2700	€ 11.27
12	Buck converter	Switching Voltage Regulators 42V, 2.5A Synchronous Step-Down Regulator, SMD	MSOP-16	LT8610	1	Analog Devices / Linear Technology	LT8610IMSE#PBF	Mouser	584-LT8610IMSE#PBF	€ 8.2500	€ 8.25
13	LDO	LDO Voltage Regulator, Adjustable, 3V to 36V in, 307mV drop, 1.4V to 34V/1A out, SMD	VQFN-20	TPS7A47	1	Texas Instruments	TPS7A4701RGWT	Farnell	2392488	€ 5.4400	€ 5.44
14	Voltage inverter	DC/DC Adjustable Charge Pump Voltage Converter, SMD	SOT-23-5	TPS6040	1	Texas Instruments	TPS60403DBVR	Farnell	2342564	€ 0.8360	€ 0.84
15	Power MOSFET	MOSFET Transistor, N Channel, 40 A, 40 V, 0.0061 ohm, SMD	TSDSON-8	M1, M2	2	INFINEON	IPZ40N04S5L7R4ATMA1	Farnell	2839475	€ 0.6500	€ 1.30
16	Power MOSFET	MOSFET Transistor, N Channel, 41 A, 40 V, 0.0074 ohm, SMD	WDFN-8	M3, M4	2	ON Semiconductor	NVTFS5C471NL	Farnell	2775457	€ 0.5930	€ 1.19

18	Current sense resistor	Current Sense Resistors - SMD 2watts .01ohms 1%, SMD	2010	Rsense1, Rsense2	2	Vishay	WSLP2010R0100FEA	Mouser	71-WSLP2010R0100FEA	€ 0.9960	€ 1.99
19	Inductor	Power Inductor, 3.3 µH, 14 A, Shielded, 8.5 A, WE-HCC Series, 8.4mm x 7.9mm x 7.2mm, SMD		L1	1	Wurth Elektronik	7443340330	Farnell	1848261	€ 2.3100	€ 2.31
20	Inductor	Power Inductor, 2.2 µH, 7.5 A, Shielded, 14 A, WE-LHMI Series, 7.3mm x 6.6mm x 4.8mm, SMD		L2	1	Wurth Elektronik	74437349022	Mouser	710-7443734902 2	€ 1.9800	€ 1.98
21	Inductor	Power Inductor, 10 µH, 2.7 A, Shielded, 4.6 A, WE-MAPI Series, 4.1mm x 4.1mm x 3.1mm, SMD		L3	1	Wurth Elektronik	74438357100	Farnell	2842190	€ 1.8100	€ 1.81
22	Schottky diode	Small Signal Schottky Diode, Single, 100 V, 250 mA, 850 mV, 2.5 A, SMD	SOD-323F	D1, D2	2	NEXPERIA	BAT46WJ,115	Farnell	1859908	€ 0.2530	€ 0.51
23	Trimmer resistor	Trimmer Potentiometer, 50 kohm, 11 Turns, Trimpot 3224 Series, 250 mW, ± 10%, SMD		POT	1	Bourns	3224W-1-503E	Farnell	1612575	€ 4.7700	€ 4.77

24	MLCC	SMD Multilayer Ceramic Capacitor, 1 µF, 50 V, 0603, 10%, X5R	0603	C6a, C27a, C2b	3	Murata	GRT188R61H105KE13D	Mouser	81-GRT188R61H105KE3D	€ 0.2600	€ 0.78
25	MLCC	SMD Multilayer Ceramic Capacitor, 1 µF, 35 V, 0603, 10%, X5R	0603	C7b, C12b, C7c, Cin, Cout, Cfly	6	AVX	0603DD105KAT2A	Mouser	581-0603DD105KAT2A	€ 0.5900	€ 3.54
26	MLCC	SMD Multilayer Ceramic Capacitor, 1 µF, 100 V, 0805, 10%, X7S	0805	C1a, C3e	2	TDK	C2012X7S2A105K125AE	Farnell	2803333	€ 0.5660	€ 1.13
27	MLCC	SMD Multilayer Ceramic Capacitor, 10 µF, 50 V, 1206, 10%, X5R	1206	C33a, C2d, C2e, C5e, C6e, C7e, C8e, C9e	8	Murata	GRT31CR61H106KE01L	Mouser	81-GRT31CR61H106KE1L	€ 0.4760	€ 3.81
29	MLCC	SMD Multilayer Ceramic Capacitor, 4.7 µF, 25 V, 0603, 10%, X5R, GRT Series	0603	C2a, C9b, C1d, C4d	4	Murata	GRT188R61E475KE13D	Farnell	2672159	€ 0.4620	€ 1.85
31	MLCC	SMD Multilayer Ceramic Capacitor, 10000 pF, 50 V, 0603, 5%, X7R	0603	C8c, C4e	2	AVX	06035C103JAT2A	Farnell	1833871	€ 0.1080	€ 0.22

28	MLCC	SMD Multilayer Ceramic Capacitor, 4.7 µF, 50 V, 1206, 20%, X7S, Soft Term	1206	C12a, C32a, C34a, C3b, C3c, C10c, C14c, Cbe, Cce, C1b	10	Murata	GCJ31CC71H475MA01L	Mouser	81-GCJ31CC71H475MA1L	€ 0.5910	€ 5.91
30	MLCC	SMD Multilayer Ceramic Capacitors, 0.1 µF, 50 V, 0603, ± 10%, X7R, GCJ Series, Soft Term	0603	C7a, C8a, C35a, C36a, C37a, C38a, C12c, C13c, C3d, C5d, C6d, C8b, C13b, C14b, Cae	15	Murata	GCJ188R71H104KA12D	Farnell	2688469RL	€ 0.2620	€ 3.93
33	MLCC	SMD Multilayer Ceramic Capacitor, 2200 pF, 50 V, 0603, 10%, X7R	0603	C4a, C26a	2	AVX	06035C222KAZ2A	Farnell	7569521	€ 0.2150	€ 0.43

32	MLCC	SMD Multilayer Ceramic Capacitor, 0.47 µF, 35 V, 0603, 10%, X7R, CGA Series	0603	C3a	1	TDK	CGA3E1X7R1V474K080AC	Farnell	2346964	€ 0.2200	€ 0.22
34	MLCC	SMD Multilayer Ceramic Capacitor, 22000 pF, 50 V, 0603, 10%, X7R	0603	C5a	1	AVX	06035C223KAT2A	Farnell	1658869	€ 0.1280	€ 0.13
35	MLCC	SMD Multilayer Ceramic Capacitor, 4.7 pF, 25 V, 0603, ± 0.25pF, C0G / NP0, AEC-Q200	0603	C5b	1	KEMET	C0603C479C3GACAUTO	Farnell	2478250	€ 0.3240	€ 0.32
36	MLCC	SMD Multilayer Ceramic Capacitor, 0.22 µF, 25 V, 0603, 10%, X7R, GCM Series	0603	C4b, C4c	2	Murata	GCM188R71E224KA55D	Farnell	2688625	€ 0.2510	€ 0.50
37	MLCC	SMD Multilayer Ceramic Capacitor, 10 pF, 25 V, 0603, 5%, C0G / NP0	0603	C5c	1	Wurth Elektronik	885012006032	Farnell	2533833	€ 0.0369	€ 0.04
38	MLCC	SMD Multilayer Ceramic Capacitor, 47 µF, 25V, 1210, 20%, X5R	1210	C6b	1	Taiyo Yuden	TMK325ABJ476MM-P	Mouser	963-TMK325ABJ476MM-P	€ 0.7950	€ 0.80

39	MLCC	SMD Multilayer Ceramic Capacitor, 22 µF, 35 V, 1206, 20%, X5R	1206	C14a, C20a, C45a, Cind	4	TDK	C3216X5R1V226M160AC	Mouser	810-C3216X5R1V226M	€ 1.0500	€ 4.20
40	Electrolytic capacitor	SMD Aluminium Organic Polymer Capacitor, 22 µF, 63 V, 105degC, VibeProof AEC-Q200		C10a	1	Panasonic	EEH-ZA1J220XV	Mouser	667-EEH-ZA1J220XV	€ 1.6600	€ 1.66
41	Electrolytic capacitor	SMD Aluminium Organic Polymer Capacitor, 47 µF, 35 V, 105degC, VibeProof AEC-Q200		Cbulka	1	Panasonic	EEH-ZA1V470V	Mouser	667-EEH-ZA1V470V	€ 1.5100	€ 1.51
42	Thick film resistor	SMD Chip Resistor, 0603 [1608 Metric], 61.9 kohm, ERJ3EK Series, 75 V, Thick Film, 100 mW	0603	R3a	1	Panasonic	ERJ3EKF6192V	Farnell	2059479	€ 0.0492	€ 0.05
43	Thick film resistor	SMD Chip Resistor, 0603 [1608 Metric], 10 kohm, CRCW e3 Series, 75 V, Thick Film, 100 mW	0603	R4a, R6c, R2e	3	Vishay	CRCW060310K0FKEA	Farnell	1469748	€ 0.0176	€ 0.05

44	Thick film resistor	SMD Chip Resistor, 0603 [1608 Metric], 110 kohm, CRCW e3 Series, 75 V, Thick Film, 100 mW	0603	R5a	1	Vishay	CRCW0603110K FKEA	Farnell	2138501	€ 0.0209	€ 0.02
45	Thick film resistor	SMD Chip Resistor, 0603 [1608 Metric], 383 kohm, CRCW e3 Series, 75 V, Thick Film, 100 mW	0603	R7a	1	Vishay	CRCW0603383K FKEA	Farnell	2138556	€ 0.0213	€ 0.02
46	Thick film resistor	SMD Chip Resistor, 0603 [1608 Metric], 26.7 kohm, CRCW e3 Series, 75 V, Thick Film, 100 mW	0603	R8a	1	Vishay	CRCW060326K7 FKEA	Farnell	2138449	€ 0.0209	€ 0.02
47	Thick film resistor	SMD Chip Resistor, 0603 [1608 Metric], 100 kohm, CRCW e3 Series, 75 V, Thick Film, 100 mW	0603	R11a, R3b	2	Vishay	CRCW0603100K FKEA	Farnell	1469649	€ 0.0166	€ 0.03
48	Thick film resistor	SMD Chip Resistor, 0603 [1608 Metric], 10 ohm, CRCW-HP e3 Series, 75 V, Thick Film, 250 mW	0603	R18a, R19a	2	Vishay	CRCW060310R0 FKEAHP	Farnell	1738878	€ 0.0765	€ 0.15

49	Thick film resistor	SMD Chip Resistor, 0603 [1608 Metric], 18.2 kohm, CRCW e3 Series, 75 V, Thick Film, 100 mW	0603	R2b, R2c	2	Vishay	CRCW060318K2 FKEA	Farnell	1652845	€ 0.0110	€ 0.02
50	Thick film resistor	SMD Chip Resistor, 0603 [1608 Metric], 1 Mohm, ERJ3EK Series, 75 V, Thick Film, 100 mW	0603	R4b, R4c, R1b	3	Panasonic	ERJ3EKF1004V	Farnell	2303325	€ 0.0492	€ 0.15
51	Thick film resistor	SMD Chip Resistor, 0603 [1608 Metric], 88.7 kohm, ERJ3EK Series, 75 V, Thick Film, 100 mW	0603	R5b	1	Panasonic	ERJ3EKF8872V	Farnell	2059491	€ 0.0492	€ 0.05
52	Thick film resistor	SMD Chip Resistor, 0603 [1608 Metric], 49.9 kohm, CRCW e3 Series, 75 V, Thick Film, 100 mW	0603	R3c, R6b	2	Vishay	CRCW060349K9 FKEA	Farnell	1652882	€ 0.0207	€ 0.04
53	Thick film resistor	SMD Chip Resistor, 0603 [1608 Metric], 63.4 kohm, CRCW e3 Series, 75 V, Thick Film, 100 mW	0603	R5c	1	Vishay	CRCW060363K4 FKEA	Farnell	2138479	€ 0.0211	€ 0.02

54	Thick film resistor	SMD Chip Resistor, 0603 [1608 Metric], 121 kohm, CRCW e3 Series, 75 V, Thick Film, 100 mW	0603	R3d	1	Vishay	CRCW0603121KFKEA	Farnell	2138507	€ 0.0209	€ 0.02
55	Thin film resistor	SMD Thin Film Resistor, 0603 [1608 Metric], 84.5 kohm, 0.1%	0603	R11e	1	Panasonic	ERA-3ARB8452V	Mouser	667-ERA-3ARB8452V	€ 1.1300	€ 1.13
56	Thin film resistor	SMD Thin Film Resistor, 0603 [1608 Metric], 105 kohm, 0.1% 25ppm	0603	R12e	1	Panasonic	ERA-3AEB1053V	Mouser	667-ERA-3AEB1053V	€ 0.5500	€ 0.55
57	Thick film resistor	SMD Chip Resistor, 0603 [1608 Metric], 3.83 kohm, CRCW e3 Series, 75 V, Thick Film, 100 mW	0603	R6A	1	Vishay	CRCW06033K83FKEA	Farnell	2138393	€ 0.0209	€ 0.02
58	Thick film resistor	SMD Thick Film Resistor, 0603 [1608 Metric], 0 ohm jumper, 100 mW, AEC-Q200	0603	R14a, R15a, R16a, R17a, R24a, R26a, R7b	7	Panasonic	ERJ-3GEY0R00V	Mouser	667-ERJ-3GEY0R00V	€ 0.0220	€ 0.15
										TOTAL	€ 97.83

II. QUOTATION

1. INTRODUCTION

The quotation corresponds to the work performed during the internship at the Electronic Defence department of TNO, The Hague.

For a closer estimation of the global costs involved during the internship, this document is divided into the specific budgets, including labour and equipment costs, and the global budget.

2. SPECIFIC BUDGETS

2.1. LABOUR COSTS

This section reflects the number of hours that the student and her tutor have spent working on the project. These hours account for weekly meetings meant to guide and choose objectives as well as to check on progress, and time that each person has worked individually.

Table 11. Labour costs of the project

Concept	Quantity [h]	Unit cost [€/h]	Amount [€]
Student	680	30.00	20400.00
Tutor	30	60.00	1800.00
		Total	**22200.00**

2.2. EQUIPMENT COSTS

For this project, the most relevant software that require license are Altium Designer and Microsoft Office suite. Other open-source, free-access software that is mentioned in the dissertation is not listed for having no effect over the budget.

All the equipment that was involved on the building of the PCB is nor reflected on this section. This is because part of it was performed by an external company and for the rest, use was made of the electronic workshop within TNO's facilities, where the student was granted free access and use of all the equipment.

Table 12. Equipment costs of the project

Concept	Amount [€]
Personal computer	800.00
Altium Designer license, from	6500.00
Microsoft Office Personal license	69.00
Ettus B205mini-i	910.00
UDOO X86	238.00
PCB, manufacturer	200.00
PCB, components	97.83
Total	**8814.83**

3. GLOBAL BUDGET

Finally, the total cost is calculated based on the previous specific budgets.

It should be noted that labour costs do not include VAT (21.00%), while equipment costs do.

Table 13. Global cost of the project

Concept	Amount [€]
Labout costs (before VAT)	22200.00
Labour costs (including VAT)	26862.00
Equipment costs	8814.83
Overhead costs (13%)	4637.99
Industrial profit (6%)	2140.61
Total	**42455.43**

The project's total budget is FORTY –TWO THOUSAND, FOUR HUNDRED AND FIFTY-FIVE EUROS AND FORTY-THREE CENTS.

III. STANDARDS AND REGULATIONS

1. DEFINITION AND SCOPE

This document defines the minimum technical conditions that have to be ensured regarding durability, use, performance, reliability and safety. The scope of the application of this document is extended to the electronic systems that are mentioned as selected for the setup as well as the PCB design and all of the tests that are conducted. Under certain conditions, inherent of their form or due to technological development, different regulations or standards shall be applied, as long as they are duly justified and do not lead to a decrease in the minimum quality requirements here referred.

2. GENERAL CONDITIONS

The general conditions are part of this project and therefore they conform the normative that applies in the project.

The designed PCB is an initial prototype, thus cannot be considered as a final product and therefore it does not have to comply with European market regulations. In case the final setup was to be released in the market, it would need to meet the requirements for the CE branding and fulfill the harmonized European standards.

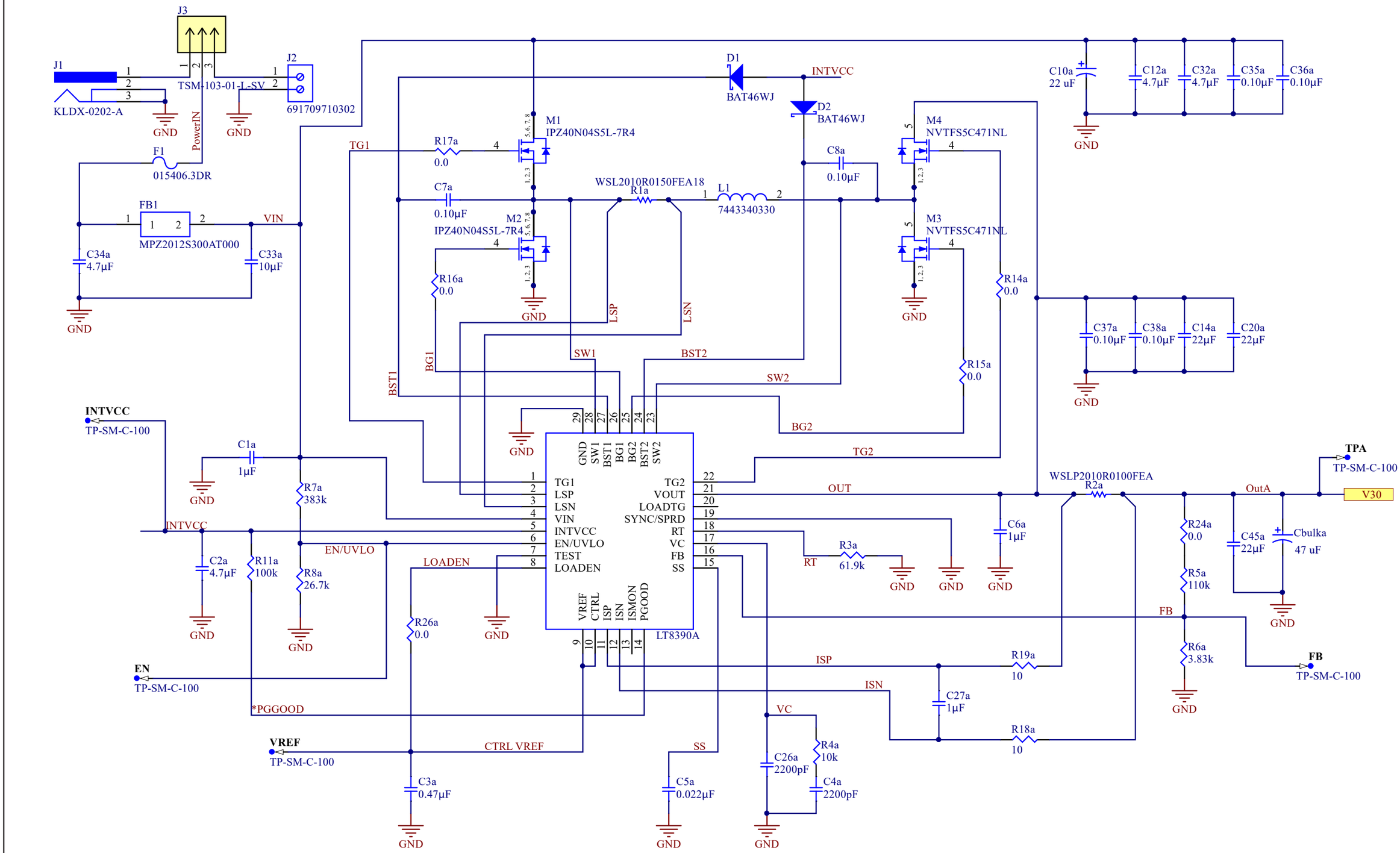
The current legal standards must be followed during design and manufacturing, and these are referred in the next section.

This project has been approved and supervised by the Electronic Defense department of TNO (The Hague, the Netherlands).

3. APPLICABLE REGULATION

- ANSI/IPC-A-600F, Class 2. Acceptability of Printed Boards.
- ICNIRP, Directive 2013/35/EU. Minimum health and safety requirements regarding the exposure of workers to the risks arising from physical agents (electromagnetic fields).
- ICNIRP, Recommendation 1999/519/EC. Limitation of exposure of the general public to electromagnetic fields.
- IEC TR 61000. Electromagnetic compatibility (EMC).
- EN 300 386 V1.6.1. Electromagnetic compatibility and Radio spectrum Matters (ERM); Telecommunication network equipment; ElectroMagnetic Compatibility (EMC) requirements.
- IEC 62586-1:2017. Power quality measurement in power supply systems – Part 1: Power quality instruments (PQI).
- EN 300 341 V2.1.1. Land Mobile Service; Radio equipment using an integral antenna transmitting signals to initiate a specific response in the receiver; Harmonized Standard covering the essential requirements of article 3.2 of the Directive 2014/53/EU.

IV. TECHNICAL DRAWINGS



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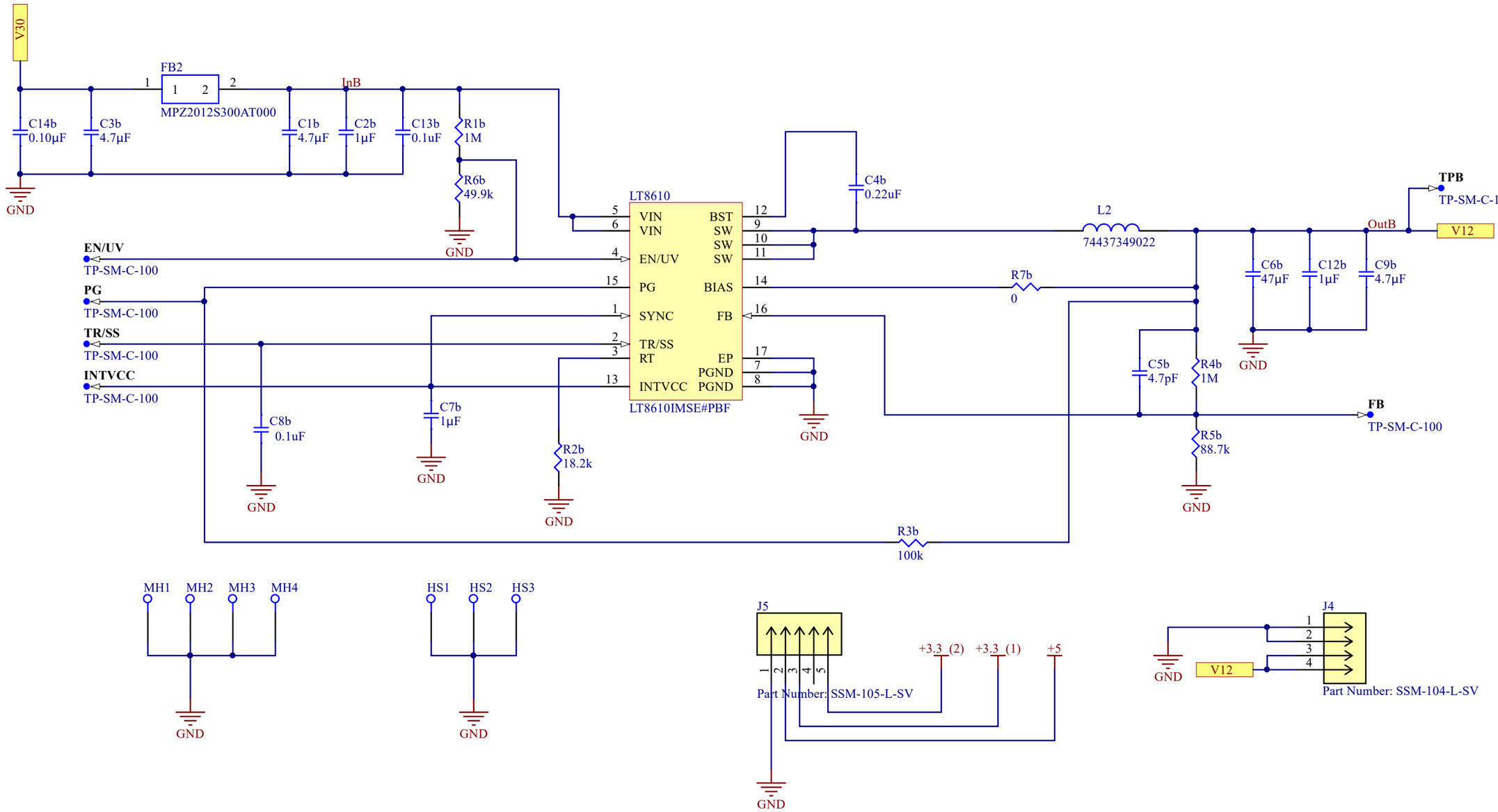
		Drawing by: Inés Bernal Leal	Scale: N/A	



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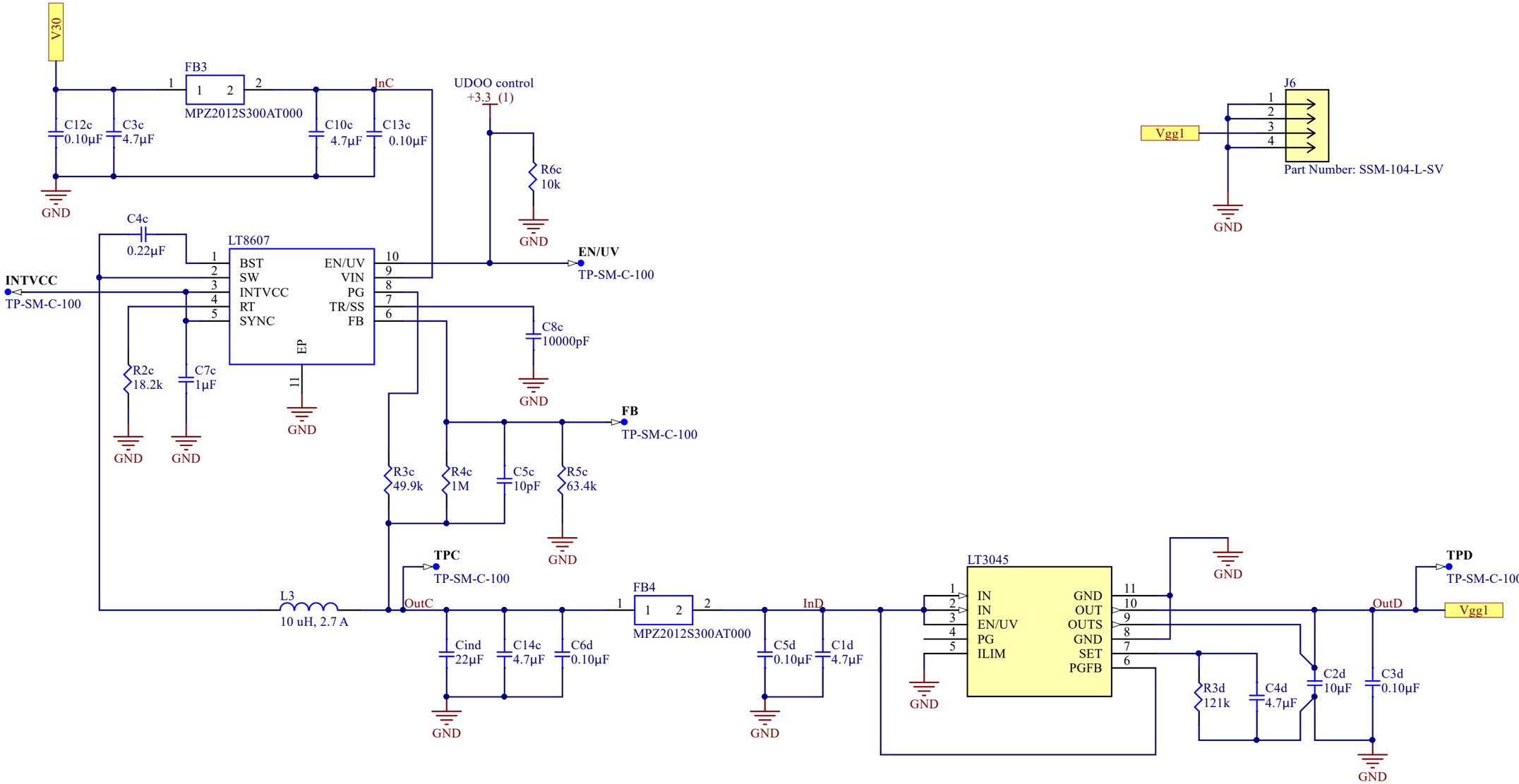
		Drawing by: Inés Bernal Leal	Scale: N/A	



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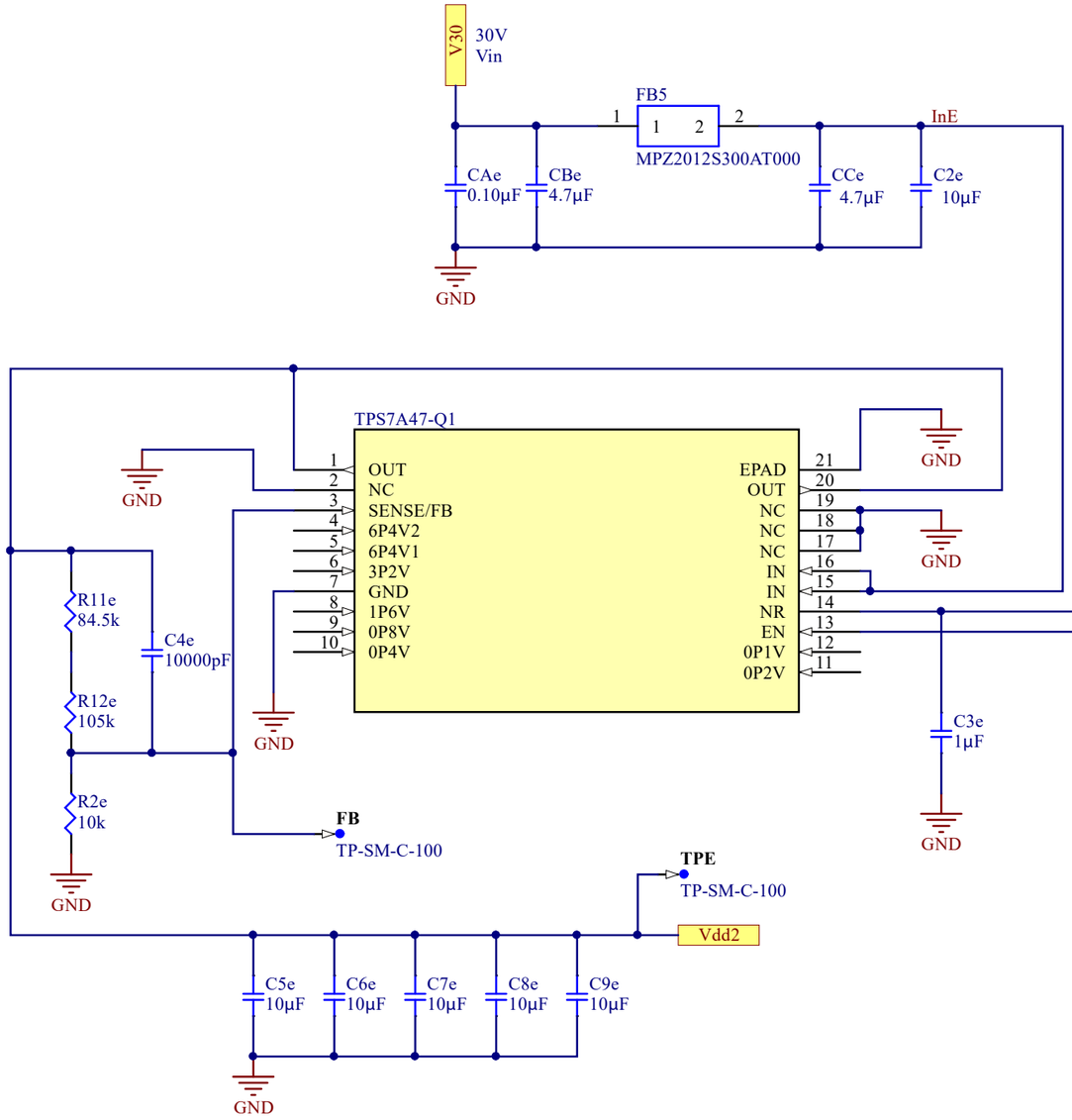
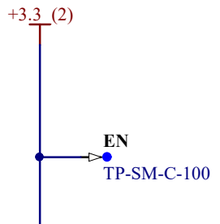
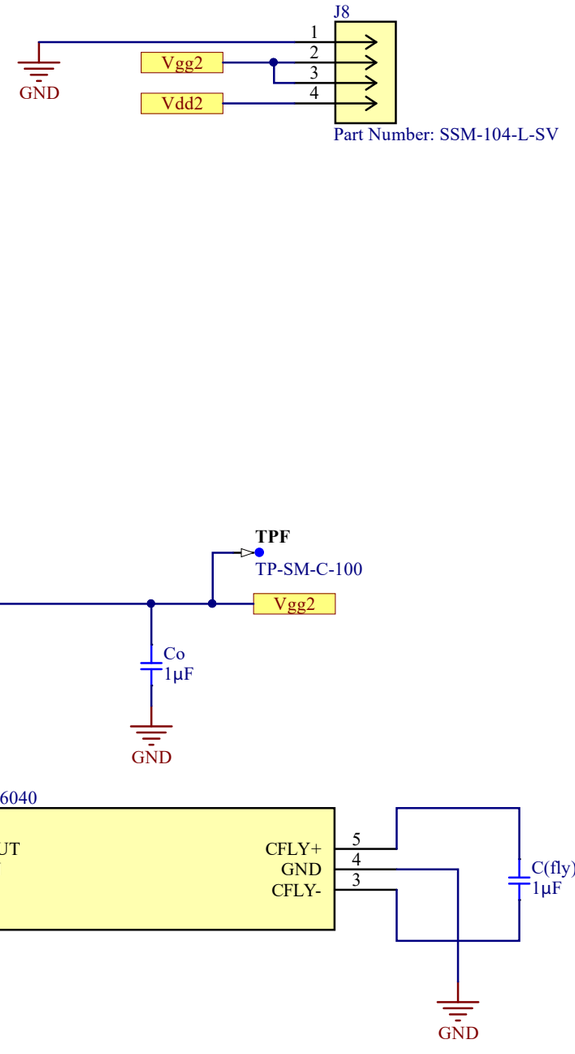
		Drawing by: Inés Bernal Leal	Scale: N/A	







BACHELOR'S FINAL PROJECT INDUSTRIAL ELECTRONICS AND AUTOMATION ENGINEERING UNIVERSITAT POLITÈCNICA DE VALÈNCIA Escuela Técnica Superior de Ingeniería del Diseño	Project: PRELIMINARY DESIGN OF AN INTEGRATED SOFTWARE DEFINED RADIO SYSTEM	Drawing: E block, TPS7A47, and F block, TPS6040 Drawing by: Inés Bernal Leal	Date: April 2019 Scale: N/A	Number: 4