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Empty Substrate Integrated Waveguide Technologies: A Major Step-Forward Towards Realizing Low-Cost and Low-Loss Microwave Circuits

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I. INTRODUCTION

Substrate integrated circuits (SICs) [1] have attracted much attention in the last several years because of their great potential. The first implementation of this concept can be found in [2], as a feeding mechanism for a slot array antenna. Deslandes and Wu [3], [4] used the term substrate integrated waveguide (SIW) to define this waveguide integrated in a substrate where the lateral walls are synthesized with metallized via holes, and the upper and lower walls are the top and bottom metallization of the substrate.

Many other SICs have been developed since the appearance of the SIW. In the substrate integrated slab waveguide (SISW) [5], the guide is synthesized on a substrate by cutting an air hole in the center of a SIW, and the frequency operating bandwidth is increased. The ridge substrate integrated waveguide (RSIW) [6] also increases the operation bandwidth by drilling cylindrical air holes in the middle of the SIW. The substrate integrated non-radiative dielectric waveguide (SINRD) [7] uses a specific pattern of air holes as lateral walls, and creates a dielectric waveguide channel reducing the radiation losses with respect to the SIW. The half mode substrate integrated waveguide (HMSIW) [8] reduces the size of the SIW by half, by exploiting the fact that there is a symmetry plane along the propagation direction that is equivalent to a magnetic wall.

The main advantage of this new concept of substrate integrated waveguide, when compared with classical planar circuits, is that it is low cost and easy to manufacture with standard printed circuit board (PCB) machinery. Moreover, it presents a higher quality factor for resonators and filters than other planar transmission lines. Many transitions have been developed from different planar lines (microstrip, coplanar, etc.) to each type of substrate integrated circuit, and so the SICs can be embedded in a substrate and easily connected to other planar circuits. When compared to the classical rectangular waveguide, SICs present smaller quality factor and greater insertion losses, but they are low cost, low profile, and can be easily embedded in a PCB.

A full suite of microwave devices has been developed with SICs, such as filters [9], [10], couplers [11], [12], phase shifters [13], antennas [14], [15], and tunable devices [16]. All of them prove the interesting features of SICs for being used in the microwave industry. However, the presence of a dielectric in these devices limits their performance, especially at high frequencies, due to the losses in the substrate that significantly increase the total insertion losses and reduce the related quality factor. In order to solve this problem, a new type of substrate integrated waveguide has appeared where the dielectric is removed, while maintaining the advantages of low cost, low profile, easy manufacturing and integration in a PCB.

The first attempts to combine planar circuits and empty waveguide devices are the so-called surface-mountable devices, or surface-mounted waveguides (SMW). In [17], a waveguide bandpass filter integrated within an MMIC is mounted on top of a planar substrate using a silicon pedestal. Then the filter is coupled with input and output microstrip lines through microstrip to waveguide transducers. In [18] another bandpass filter is mounted on top of a planar circuit. This time the filter is implemented in a reduced height metal waveguide fabricated with micromachining. The filter is connected to the planar substrate using slot coupling, and it is coupled to input and output microstrip lines via slots in the ground plane. These slots act as the first and last inverter of the filter. In [19], a pyramidal horn antenna micromachined in a metal body, and fed with a rectangular waveguide, is mounted on top of a substrate, which is coupled to a SIW line in this substrate by means of a quarter-wave stepped impedance transformer. A theoretical comparison between the same filter implemented in stand-alone SIW, and in a surface-mountable waveguide coupled to feeding SIW lines is presented in [20]. Finally, another surface-mounted waveguide filter is presented in [21]. In all these cases the surface mounted devices allow the propagation of waves through air, and this leads to lower insertion losses, and higher quality factors in filters. However, this is not a fully substrate integrated solution, requires non-planar manufacturing processes and transitions, thus not being a low-profile and low cost integrated solution.

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The first empty line truly integrated in a substrate was theoretically proposed in [22] in 2006. It was called modified SIW (MSIW), and its behavior was simulated, but not manufactured. It was a SIW line partially emptied, so that the electromagnetic waves propagated mainly through air. In 2014, the empty SIW (ESIW) was presented in [23]. It was a completely dielectric-free substrate integrated waveguide. Soon after the ESIW was proposed, also in 2014, two more empty substrate integrated waveguides were presented, the air-filled SIW (AFSIW) [24], and the Hollow SIW (HSIW) [25]. Both the AFSIW and the HSIW were very similar to the MSIW. The AFSIW was manufactured and integrated in conventional printed circuit boards, and the HSIW was manufactured with low-temperature cofired ceramic (LTCC) technology. In 2015, an empty substrate integrated coaxial line (ESICL) was proposed in [26]. Finally, a dielectricless SIW (DSIW) was recently presented in 2016 [27]. This time a thick substrate was milled and metallized, and then covered with a top metallic cover stuck with a prepreg (pre-impregnated composite fibers where a thermoset polymer matrix material, such as epoxy, is present) layer, so that an almost dielectric-free substrate integrated waveguide is obtained. The advantages of emptying the substrate are also outlined in [28], where the state-of-the art of substrate integrated solutions is reviewed.

All these empty substrate integrated waveguides (MSIW, ESIW, AFSIW, HSIW, ESICL and DSIW) are presented in the next sections. In the conclusions, a table is included where the main features of each one of these lines are compared.

II. MODIFIED SIW

The first empty substrate integrated waveguide was presented in [22]. In this work, the authors proposed for the first time the removal of part of the dielectric body in the substrate, in order to reduce the power dissipated in the dielectric. This structure can be seen in Fig. 1. In order to complete the guided structure, the emptied substrate has to be closed with a top and bottom conducting layers. These layers could be simple and low cost FR4 substrates, and the authors proposed to fix them to the central substrate using prepreg. The via holes forming the walls of the waveguide could be of any of the plated-through, buried or blind types (in Fig. 1 they are of buried type). The via holes are considered to be of square cross section in order to simplify the analysis. The authors proposed for this structure the name *Modified substrate integrated waveguide* (MSIW).

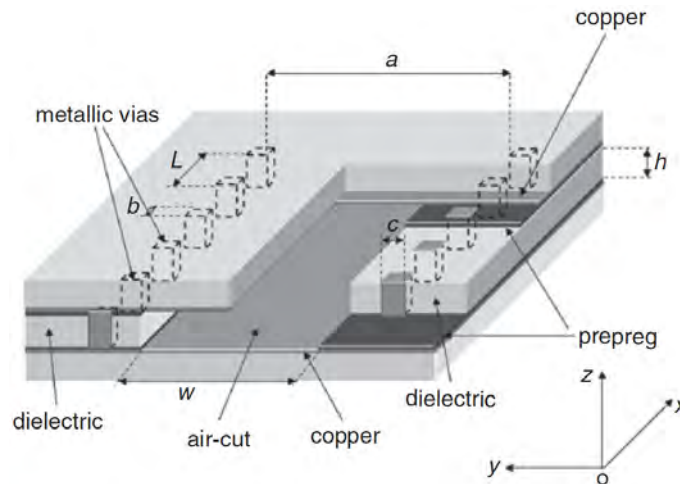


Fig. 1. Modified SIW with air-cut region (source [22]).

In [22] an analysis method for the MSIW is presented. The inhomogeneous region is divided into homogeneous parts. Inside each homogeneous region the field is expanded as a linear combination of spatial harmonics, and field continuity is enforced using mode-matching. The conductor losses are evaluated with the perturbational method. The results show that the higher the ratio w/a , the lower the losses.

In Fig. 2 the attenuation constants of MSIW and SIW are compared for the case of using RO4003C and RT5880 substrates. Only the losses in the dielectric are considered. It can be observed that the attenuation constant is reduced by approximately 1 Np/m and 0.3 Np/m respectively, for both substrates. It can also be observed that the cutoff frequency of the MSIW is increased when compared with that of the SIW. The attenuation constant in the MSIW is almost independent of the dielectric properties of the substrate, since losses are now mainly due to conductor and radiation, and not so much due to losses in the dielectric material.

All results in Fig. 2 are theoretical, since no prototype was manufactured and measured, and no transition to other planar or SIW lines are presented in [22].

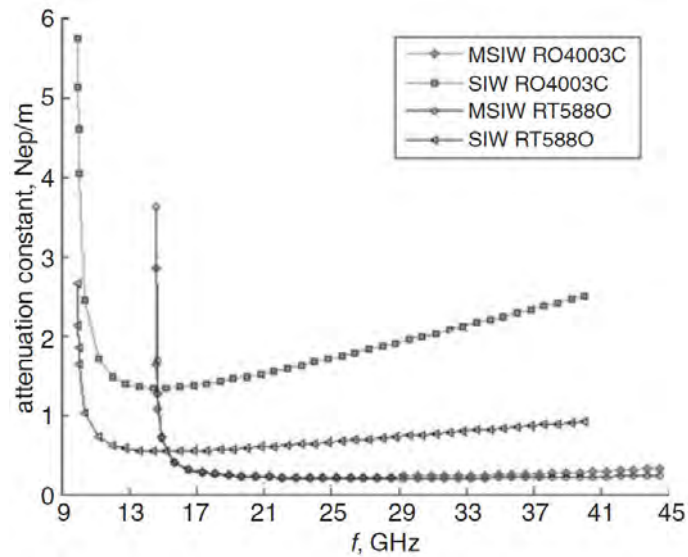


Fig. 2. Comparison between attenuation constants due to the dielectric of MSIW and SIW (source [22]).

III. EMPTY SIW

In [23], for the first time, the so-called Empty Substrate Integrated Waveguide (ESIW) was presented. This new type of empty substrate integrated circuit was manufactured by cutting a rectangular hole in the PCB. After that, this hole was plated following a standard procedure of PCB via metallization. As a result, the lateral walls of the waveguide are formed. Finally, the waveguide is closed by attaching two metallic covers to the main PCB substrate. One of the covers acts as the upper waveguide wall, while the other one becomes the lower face of the waveguide (see Fig. 3). The electrical connection among these different layers must be of very high quality. Otherwise, the device would not function adequately. This high quality interlayer connection is achieved by means of soldering. A tin-based soldering paste has been used to solder the different layers. This soldering paste is distributed on the top and bottom of the main layer. The structure is assembled and, finally, the solder paste is dried in a reflow oven. As a result, a solid tin layer is formed, which strongly links the main layer with the covers. The positioning of the top and bottom covers is not critical, since all the critical elements are placed in the central layer and manufactured in the same PCB. The top and bottom covers are usually plane metal laminates, but they can also be additional PCB sheets. This is a very interesting choice from the point of view of developing reconfigurable devices since these metallic lids can hold external circuitry that can interact with the integrated waveguide.

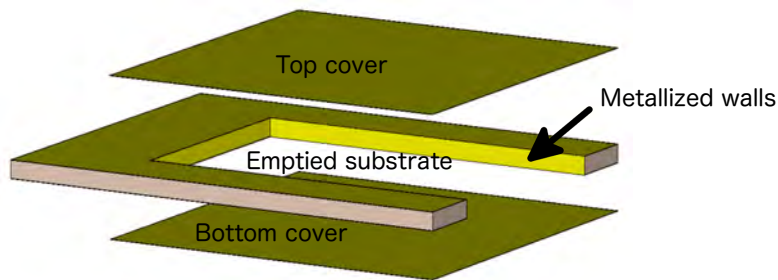


Fig. 3. ESIW fabrication (source [23]).

This new type of empty substrate integrated circuit, the ESIW, has the advantage that its geometry is very similar to that of the rectangular waveguide, but with low profile and low cost, so one would expect a behavior very similar to that of the rectangular waveguide. In [29] a procedure to characterize the propagation constant of ESIW lines is presented. In order to measure the phase constant of the line (β), a piece of ESIW line is measured using a calibration kit of [30], which will be explained later. Since the calibration kit removes the effect of the feeds from measurements, the actual response of a straight and empty piece of ESIW line is obtained. The propagation constant can be easily recovered from the phase of the measured S_{21} . Theoretically, the attenuation constant (α) could be also recovered from the modulus of this same parameter. However, α is very low, and it is completely masked by the measuring noise when it is measured directly from the transmission parameter of an empty ESIW line. An alternative is to use the procedure of [31], which has been reformulated to be applied to ESIW.

This procedure estimates the attenuation constant from the measured unloaded quality factor of a resonator slightly coupled to the input and output ports. In Fig. 4 one can see the measured ESIW (15.8988 mm width, and 1.524 mm height) phase and attenuation constants, which are compared to the phase and attenuation constant of an ideal rectangular waveguide of the same cross-section.

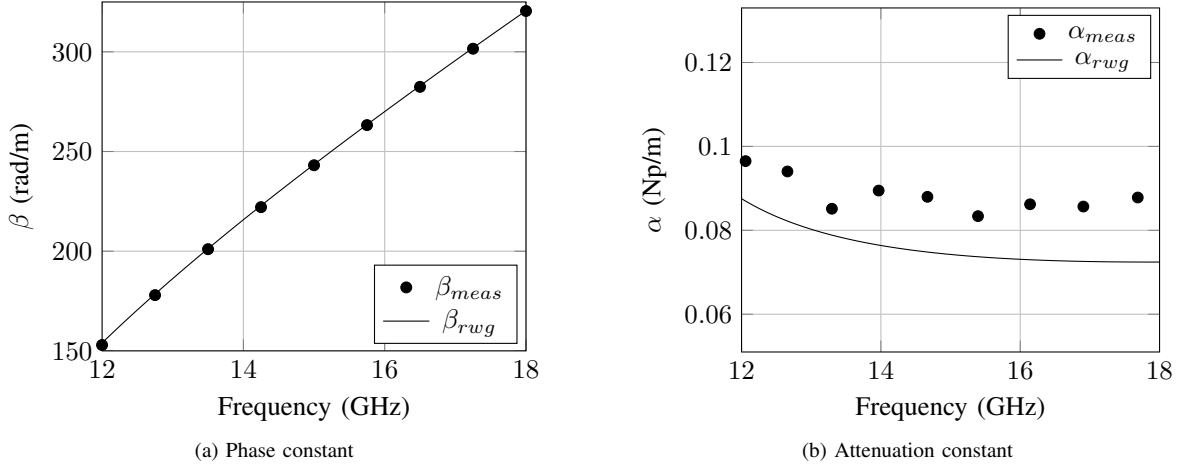


Fig. 4. Measured phase and attenuation constants of ESIW compared to the phase and attenuation constant of an equivalent rectangular waveguide (source [29]).

It can be observed that the ideal and measured phase constants are almost indistinguishable. This is of great importance, since it is the experimental confirmation that an ESIW can be modeled as an ideal rectangular waveguide, thus allowing the use of previously developed fast and accurate analysis methods used for analyzing rectangular waveguide devices (which take advantage of having a constant cross section along the propagation direction). All the design techniques and devices that can be implemented in traditional waveguides can be directly transferred to ESIW technology. On the other hand, the attenuation constant of an ESIW is slightly above the attenuation constant of the equivalent ideal rectangular waveguide. This happens because the metal that closes the ESIW is not perfectly plane, i.e it exhibits a certain degree of granularity, and because an ESIW is composed of three different metallic pieces while the ideal rectangular waveguide uses a single piece of metal (practical implementations of rectangular waveguides are usually based on two 3D metallic pieces screwed together). The small increase of losses does not affect the application of classic rectangular waveguide design procedures to ESIW, since most of these methods do not consider losses.

In order to integrate this structure into a printed circuit, a high-quality transition to a traditional planar line is mandatory. In [23] a transition from ESIW to a microstrip line is proposed (see Fig. 5a). The transition can be analyzed as a two stage mode converter. In a first stage, the microstrip mode is transformed into the fundamental mode of a waveguide partially filled with dielectric. In order to obtain a good match between both modes, a metallic iris has been opened in the back wall of the ESIW (see black lines in Fig. 5a). The second stage transforms the fundamental mode of the partially filled waveguide into the fundamental mode of the final empty integrated waveguide. In order to accomplish this goal, an exponential taper has been used, so that the dielectric filling of the initial waveguide is progressively reduced following an exponential law until it effectively vanishes. This transition is very short in electrical length, and provides very good results with very low insertion losses and high return losses.

However, this transition fails for thin substrates, since the feeding microstrip lines in these cases are very narrow. As a result, the exponential taper would be too narrow to be feasible. In order to overcome this problem, in [32], a modification to the taper has been proposed. This modification consists of adding a taper to the feeding microstrip line (see Fig. 5b). This taper increases the width of the feeding line and, thus, the exponential taper transforms the partially filled waveguide into the final empty integrated waveguide, with a practicable line width that can be fabricated. This transition achieves return losses greater than 13.5 dB, and insertion losses lower than 0.75 dB from 6.6 to 16.45 GHz.

This transition is further improved in [33] with the addition of two air holes of diameter d_f (see Fig. 5c). These holes ensure that the size of the opening in the back wall of the ESIW is exactly of the desired width (w_{ir}). Otherwise, the width that is obtained with the drill in the structure of Fig. 5b has large tolerances and introduces errors in the measurements from the simulation, as happens in [32]. Finally, via holes are added in order to prevent possible leaky waves traveling through the substrate outside the ESIW. d_v and s_v are chosen to avoid radiation leakage with the same design rules as the vias in a standard SIW [34]. Figure 6a shows a manufactured prototype of this last version of the back to back transition from microstrip to ESIW (a Rogers 4003 thin substrate with 0.813 mm width has been used), and a comparison between simulations and measurements can be seen in Fig. 6b. Measured insertion losses are lower than 0.6 dB and return losses are greater than 20 dB.

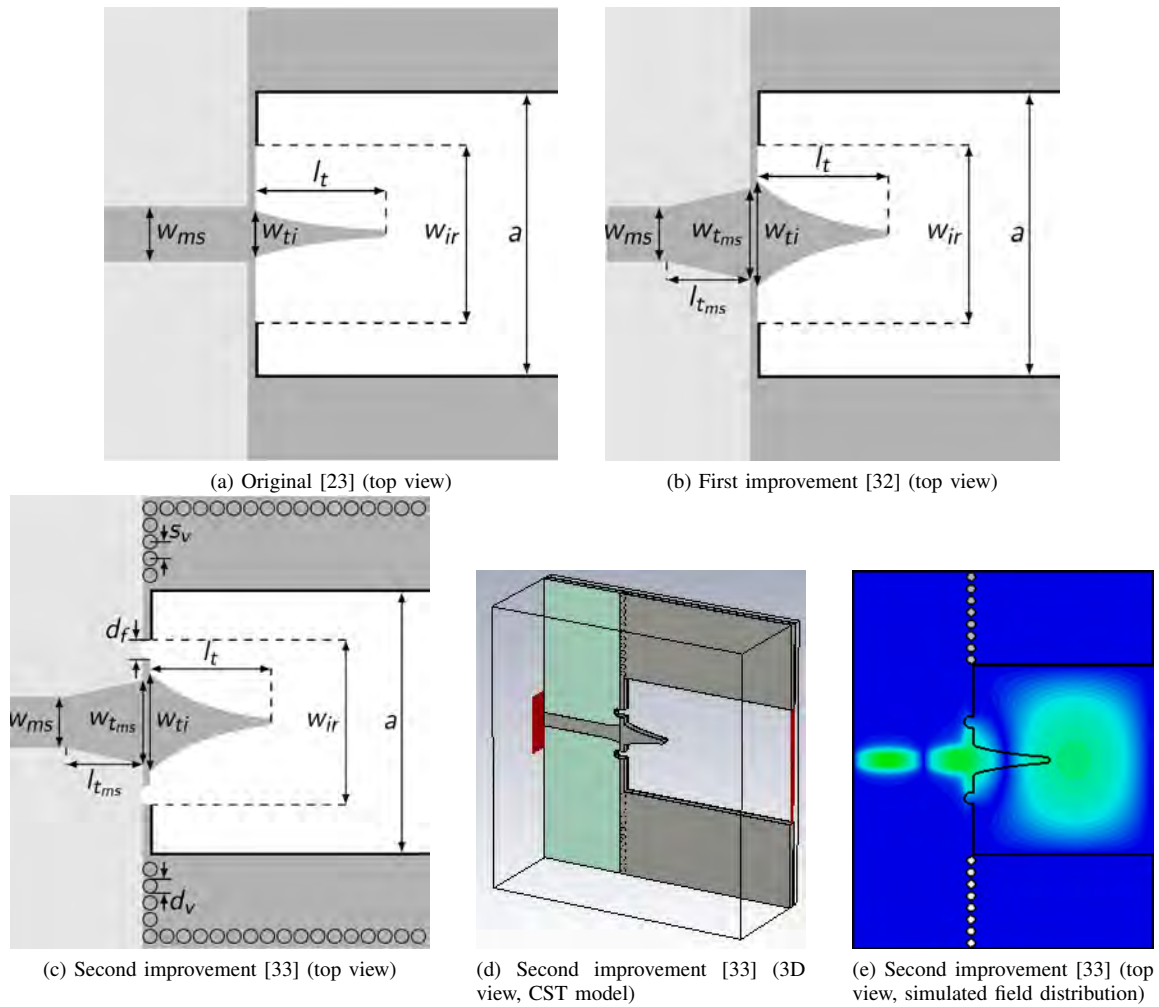


Fig. 5. Layout of the original version and the two successive improvements of the microstrip to ESIW transition (source [33]).

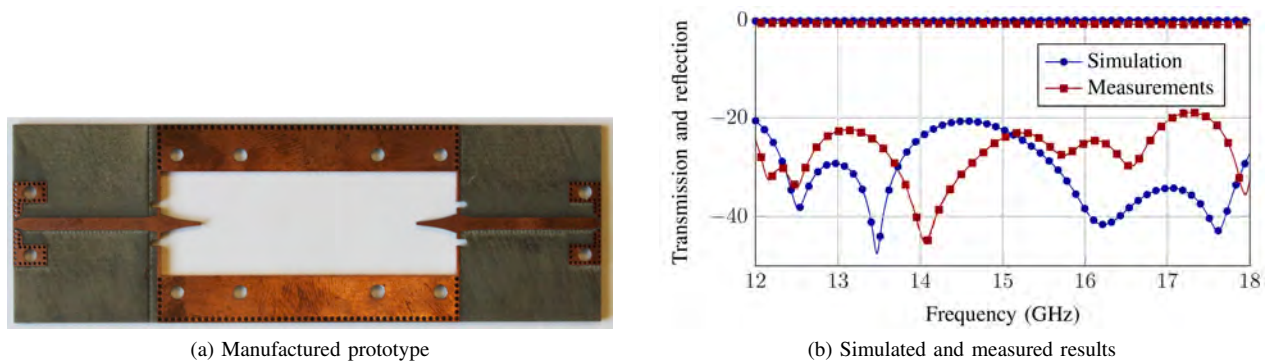


Fig. 6. Last version (see Fig. 5e) of the back to back transition from microstrip to ESIW (source [33]).

Transitions from ESIW to other lines, different from microstrip, can be also developed. For instance, a direct and wideband transition from coaxial (SMA connector) to ESIW is presented and experimentally validated in [35]. Good results (1 dB insertion losses, and 13 dB return losses) are obtained for thin substrates. As the height of the substrate increases, the radiation losses increase and the transition fails to work.

A transition between two ESIWs built in substrates at different levels has recently been presented in [36]. This transition will allow the development of multilayer ESIW circuits, which will provide higher compaction and versatility. The main disadvantage of this approach is that it requires 3D processing of the substrate and it will be necessary to add a partial recess in the main layers that support both ESIWs, in order to increase the return loss of the transition.

Once the transitions from ESIW to other planar lines, such as the microstrip line, are available, it is necessary to develop calibration kits that allow the de-embedding of the contribution of these transitions to the measurements, so that high-quality measurements of only the ESIW device can be obtained. To that purpose, a thru-reflect-line calibration kit is proposed in [30]. Using this measurement procedure, it is possible to recover the response of the ESIW device alone, since the response of the transitions and connectors are removed from measurements. Fig. 7 shows a set of calibration standards (TRL) for a Rogers 4003C substrate of 1.524 mm and a filter prototype. These calibration standards have been used to measure an empty ESIW line of 15.7988 mm width. The results for the empty piece of ESIW, displayed in Fig. 7b, show that the calibrated measurements are very accurate, since measurements clearly approach the expected behavior of an empty line (zero reflection and full transmission).

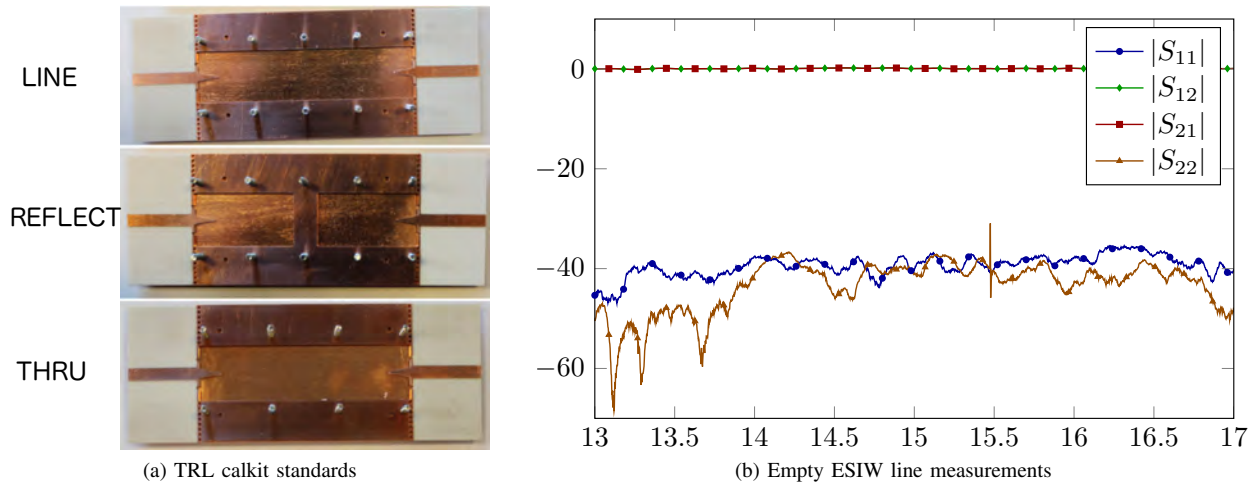


Fig. 7. Calibration standards and cavity coupled filter of [30], and results (source [30]).

The performance of the ESIW for implementing different communication devices has been tested in several publications. Table III summarizes all these contributions, which include coupled cavities filters [23] and [37], 90° hybrid directional coupler [38], a Moreno cross-guide directional coupler [39], and an H-plane horn antenna [40]. Low cost, low profile, high performance and low loss circuits can be implemented with this new ESIW technology.



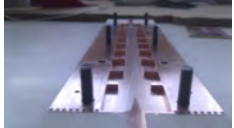

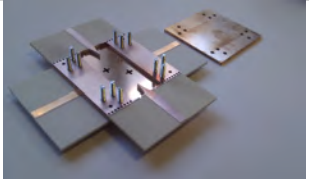

Device	Specifications	Prototype	Performance (all measured values)
X-band Filter (source [23])	4-pole Chebyshev filter 0.01dB ripple $f_0 = 11$ GHz $BW = 300$ MHz		IL=0.5 dB Q=1226
Ka-band Filter (source [23])	5-pole Chebyshev filter 0.01dB ripple $f_0 = 19.5$ GHz $BW = 500$ MHz		IL=0.8 dB Q=1196
Ku-band Filter (source [37])	8-pole Chebyshev filter 0.1dB ripple $f_0 = 15$ GHz $BW = 1$ GHz		IL=0.35 dB Q=2151
90° hybrid directional coupler (source [38])	$f_0 = 15$ GHz $BW \geq 4$ GHz 3 dB coupling 90° phase shift IS and RL ≥ 20 dB PSU ≤ 0.5 dB		Coupling $\in [3, 4]$ dB Phase shift $\in [86^\circ, 94^\circ]$ IL=0.083 dB RL ≥ 16 dB IS ≥ 18 dB PSU ≤ 0.5 dB
Moreno cross-guide directional coupler (source [39])	$f \in [12.4, 18]$ GHz Coupling 20.5 dB ± 1 RL ≥ 20 dB Directivity ≥ 15 dB		Coupling $\in [20, 21.5]$ dB RL ≥ 22 dB IS ≥ 37 dB Directivity ≥ 15 dB
H-plane horn antenna (source [40])	$f_0 = 15$ GHz $ S_{11} \leq -15$ dB $ S_{21} \geq -2$ dB		IBW = 210 MHz RL=50 dB at 15 GHz Directivity = 8.94 dBi Radiation efficiency = 95% Side lobe level = 8.55 dBi -3 dB beamwidth = 15°

TABLE I

PERFORMANCE OF THE UP-TO-NOW MANUFACTURED DEVICES IN ESIW. IL: INSERTION LOSS; RL: RETURN LOSS; IS: ISOLATION; PSU: POWER SPLIT UNBALANCE; IBW: -10 dB IMPEDANCE BANDWIDTH

IV. E-PLANE EMPTY SUBSTRATE INTEGRATED WAVEGUIDE

Substrate Integrated waveguides are usually H plane structures, that is, structures that mimic an H plane rectangular waveguide, where the geometry is invariant in height (shorter dimension of the waveguide cross section). However, there are some classical devices that can only be manufactured in E-plane topology, because its performance cannot be accomplished with an H-plane topology, such as the case of a wideband phase shifter, for example.

Recently [41], a completely different approach to integrate a rectangular waveguide in a planar substrate was proposed. Before this contribution, the waveguide was always integrated so that the H-plane coincided with the planar substrate. For SIWs and other empty substrate integrated approaches based on vias, there is no other possibility. Fortunately, ESIW, which presents continuous vertical and horizontal walls, has no such limitation. In [41], a novel transition to an empty substrate integrated waveguide with its E-plane coincident with the fabrication substrate is presented. This novel integrated waveguide is known as E-plane Empty Substrate Integrated Waveguide (ESIW-E). In the case of ESIW-E the vertical dimension is the longer side of the waveguide cross-section (a), while the horizontal dimension is the shorter side (usually b). In this novel integrated waveguide, it is possible to easily modify b , thus making feasible to integrate, in a printed circuit board waveguide, E-plane circuits, which had not been achieved before. The transition of [41] is inspired by the well-known coaxial-to-waveguide transition, which has been modified to become completely integrated. In Fig. 8 one can see the multilayer structure of the transition. As it can be seen in this figure, the transition respects the waveguide symmetry in order to maximize the return loss. In this realization of the ESIW-E, there are 8 layers. This is a complex structure, but that is the prize that one has to pay to integrate an E-plane waveguide in a substrate. The number of layers for creating the ESIW-E is not always 8, but depends on the operation frequency and the height of the layers. The higher the frequency, the lower the width a of the waveguide necessary to cover that frequency band. If a decreases, fewer substrate layers are needed to create the E-plane ESIW. Therefore higher frequency operation, fewer substrate layers of this height would be necessary.

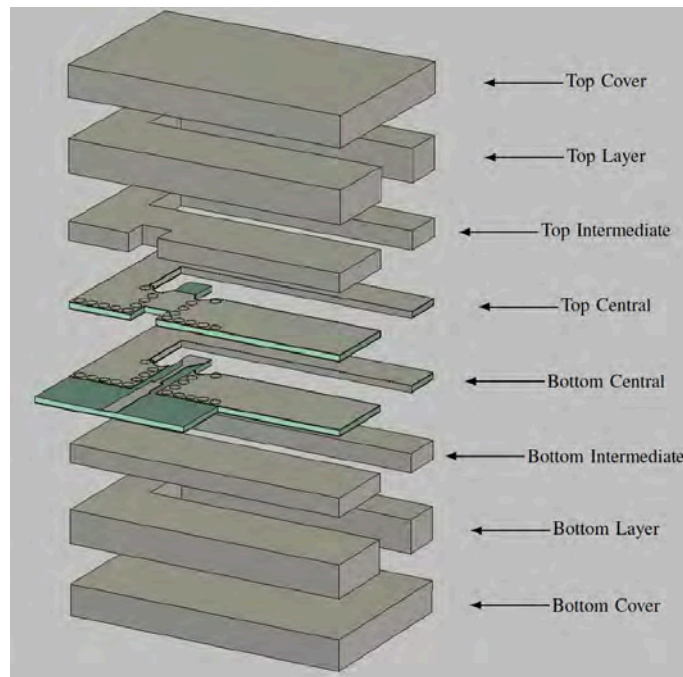


Fig. 8. Multilayer structure of the microstrip-to-ESIW-E transition of [41] (source [41]).

This transition is formed by three different parts. First, there is a transition from an open microstrip to a covered microstrip. This first stage has been included to facilitate the transition from the open microstrip to the closed stripline that feeds the waveguide probe. One can then find a transition from covered microstrip to stripline, and, finally the stripline feeds the probe that excites the fundamental mode of the integrated waveguide.

This transition has been fabricated for an integrated waveguide of 5.66 mm height (a) and 2.845 mm width (b) operating from 33 to 50 GHz. In order to fabricate this ESIW-E, an eight layer structure has been used. In Table II one can see the specific PCB layers involved in this ESIW-E realization (see also Fig. 8).

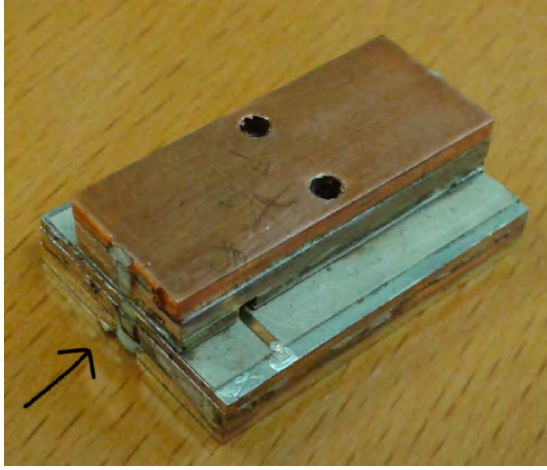
TABLE II

CHARACTERISTICS OF ALL THE PCB USED FOR THE MANUFACTURE OF THE ESIW-E OF [41]. h IS THE SUBSTRATE HEIGHT, t_1 IS THE THICKNESS OF THE SUBSTRATE METALLIC LAYER, t_2 IS THICKNESS OF THE ELECTRODEPOSITED METALLIC LAYER, AND $h_t = h + 2t_1 + 2t_2$ IS THE TOTAL HEIGHT OF THE LAYER. ALL DIMENSIONS ARE IN MM. (SOURCE [41]).

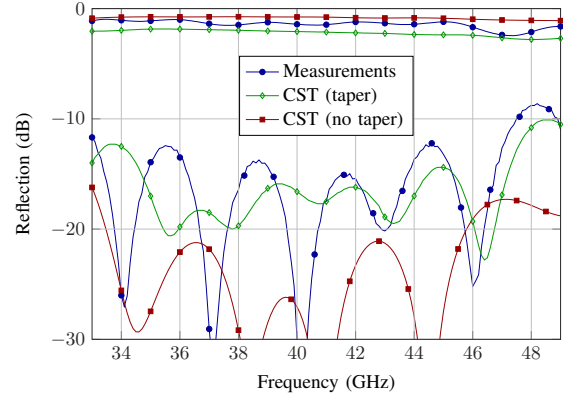
Layer	h	t_1	t_2	h_t	PCB name
Top cover	1.5	0.035	0	1.57	FR4
Top layer	1.5	0.035	0.020	1.614	FR4
Top intermediate	0.794	0.035	0.020	0.908	FR4
Top central	0.254	0.017	0.010	0.308	RO3003
Bottom central	0.254	0.017	0.010	0.308	RO3003
Bottom intermediate	0.794	0.035	0.020	0.908	FR4
Bottom layer	1.5	0.035	0.020	1.614	FR4
Bottom cover	1.5	0.035	0	1.57	FR4

In Fig. 9 one can see the results of this novel waveguide integration scheme. The measured results strongly agree with CST simulations when the commercial adapters from coplanar to microstrip lines that have been used to measure this device, are also considered in simulation (“CST (taper)” curves of Fig. 9).

A phase shifter has been implemented in ESIW-E and successfully integrated and measured [41]. This phase shifter could not have been achieved with an H-plane configuration because the desired bandwidth is too wide, so that it could not have been built using SIW, ESIW or other substrate integrated rectangular waveguide variants. In [41] the measured results of the phase shifter have been compared with a single piece of ESIW-E line, used for reference. The phase variation within the desired transmission band (from 35 to 47 GHz) is $\pm 5^\circ$, and the amplitude imbalance is ± 0.6 dB.



(a) Prototype



(b) Results (S-parameters in dB)

Fig. 9. Manufactured microstrip-to-ESIW-E back-to-back transition and results (source [41]).

V. AIR-FILLED SIW

The structure of the Modified SIW has been used and enhanced by other authors. These authors first implemented a SIW phase shifter with circular holes in [42], and in [24], [43], [44] and [45] they presented a practical implementation of the Modified SIW, called an *air-filled substrate integrated waveguide* (AFSIW).

A. Structure and performance of the air-filled SIW

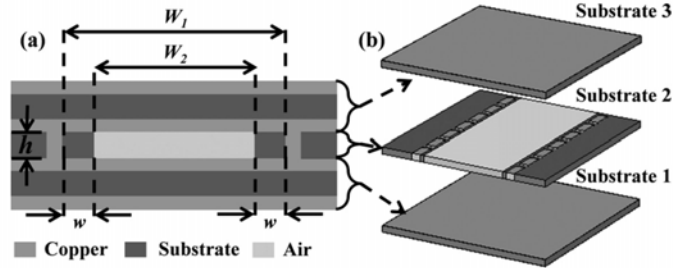


Fig. 10. Air filled SIW. Cross-sectional view and structure (source [43]).

Fig. 10 shows the layout of this air-filled SIW (AFSIW). It is a three layer structure, and the top and bottom substrates (substrates 1 and 3 in Fig. 10) can be low cost ones, such as FR-4, since they only act as metallic covers, and thus their dielectric does not interfere with the propagation of the fields. High performance millimeter-wave circuits and other electrical circuits can be also integrated in the top and bottom substrates.

The cut-off frequency of the fundamental mode in the AFSIW can be controlled with W_1 and W_2 (see [43]). The dielectric losses depend on the dielectric walls of width w . The lower w , the smaller the dielectric losses. Manufacturing reasons and mechanical integrity fix a lower limit for w , which in [43] is said to be 0.254 mm with wet etching and laser machining. Nevertheless, the dielectric walls are in a region with small electric field intensity, so dielectric losses will be small. The ohmic losses depend on the conductor material, and they are increased by a multiplying factor that depends on the surface roughness [46], [47]. The greater the roughness, the higher the losses. In the traditional SIW the inner surface roughness of the copper foil of the unique substrate has to be considered. But in the AFSIW it is the roughness of the outer face of copper foil of substrates 1 and 3 which has to be considered. In addition the roughness of the outer face ($0.3 \mu\text{m}$ for Rogers 5880) is lower than that of the inner face ($0.4 \mu\text{m}$), and so, surface roughness and conductor losses are slightly smaller than in SIW. In [48], the metallic surface of the top and bottom covers (FR-4 substrate in this case) are polished with a lapping and polishing machine, which reduces the insertion loss by 28%.

Fig. 11 shows the total loss of the dielectric filled SIW with 6002 and with 5880 substrates, as well as of the AFSIW based on 6002 substrate with the same height. Results are provided for Ka and U bands. In both cases total losses are less than one-third compared with the dielectric-filled SIW using the same substrate.

Another important characteristic of the line is the power-handling capability. In the case of the continuous-wave power limitation, or average power handling capability (APHC), the limit comes because the losses transformed into heat can alter

	6002-filled SIW	5880-filled SIW	Air-filled SIW		6002-filled SIW	5880-filled SIW	Air-filled SIW
Dielectric loss (dB/cm)	0.081	0.0523	0	Dielectric loss (dB/cm)	0.1226	0.079	0
Ohmic loss (dB/cm)	0.0533	0.0452	0.02973	Ohmic loss (dB/cm)	0.0686	0.0579	0.0375
Surface roughness loss (dB/cm)	0.0258	0.022	0.01437	Surface roughness loss (dB/cm)	0.0421	0.0355	0.024
Total loss (dB/cm)	0.1601	0.1195	0.0441	Total loss (dB/cm)	0.2333	0.1724	0.0615
Q -factor	187	251	680	Q -factor	195	264	740
APHC (dBm)	47.23	46.82	54.78	APHC (dBm)	44.12	43.8	49.84
PPHC (kW)	1046	2375	23.6	PPHC (kW)	695	1577	15.4
Width (mm)	4.11	4.77	7.04	Width (mm)	2.715	3.16	4.604

(a) Ka-band (values at 33 GHz)

(b) U-band (values at 50 GHz)

Fig. 11. Property comparison of SIWs of the same height (source [43]).

the structure of the device, which is a PCB formed by metal and dielectric parts. Since the temperature at which the dielectric transitions from a glass to a viscous state (transition glass temperature) is lower than in the case of the metal, the dielectric is the limiting material. As shown in Fig. 11, the APCH of an AFSIW is more than 5 dB higher than for the dielectric-filled SIW of the same height.

The peak power limit before breakdown (peak power handling capability or PPHC) is also an important characteristic. Breakdown can either occur as a multipaction (in vacuum) or as an ionization phenomenon. In [43] the PPHC for ionization in ground-based systems is calculated for the fundamental mode TE_{10} of the dielectric and air filled SIW. In this case the solid dielectric has a greater strength against ionization than gaseous dielectrics, thus simulated results in Fig. 11 give a PPHC of 23.6 kW and 15.4 kW at Ka and U bands, respectively, for the AFSIW, which is much smaller than the values of PPHC of the dielectric-filled SIW.

It can also be observed in Fig. 11 that the width of the AFSIW is greater than for the dielectric-filled SIW. This is because wavelength is smaller inside the dielectric.

It can be concluded, therefore, that the AFSIW has lower transmission losses, higher Q , and higher APHC, but has a larger foot-print and lower PPHC, when compared to dielectric-filled SIW.

B. Transition from dielectric-filled to air-filled SIW

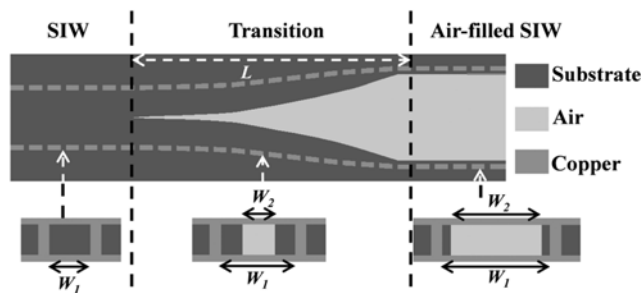
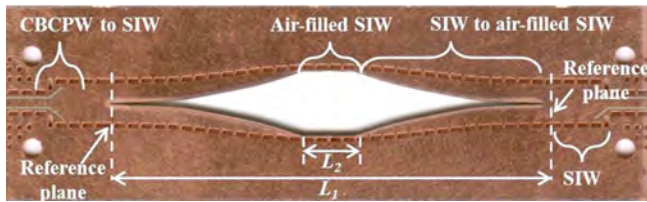


Fig. 12. Geometry of the dielectric-filled to air-filled transition with cross-sectional views (source [43]).

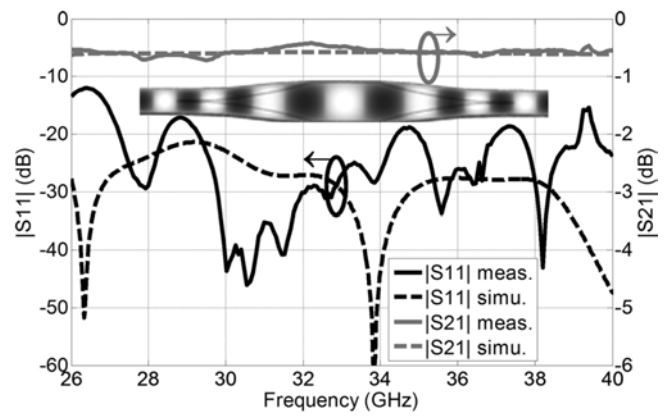
In [24] and [43] a transition from dielectric-filled to AFSIW was presented. The geometry of this transition is shown in Fig. 12. In order to minimize dispersion, the separation of the metallic vias (W_1) and the width of the air-filled region (W_2) in each section along the tapered transition are modified in order to keep the cutoff frequency of the fundamental TE_{10} mode nearly constant. This separation between sections is optimized to maximize return losses. There is a tradeoff between impedance matching and transmission losses when choosing the length of the transition. The longer the transition, the better the matching, but the greater the transmission losses.

As discussed in [43], inside the transition the fundamental and the second mode are both in propagation in the higher part of the usable frequency band, and because of the small manufacturing tolerances, there is an asymmetry, which causes both propagating modes to interfere with each other, thus slightly reducing the usable frequency band.

Fig. 13 shows a manufactured back-to-back transition, together with the measured and simulated results. A TRL calibration technique has been used to de-embed the effect of the transitions from grounded coplanar waveguide to SIW. The measured return loss is greater than 15 dB from 27 to 40 GHz, and the transmission loss is lower than 0.8 dB. Better results are obtained in [49] using a cosine geometry for the transition (return loss greater than 20 dB, and transmission loss lower than 0.35 dB).



(a) Manufactured prototype



(b) Measured and simulated results with E-field magnitude simulated at 33 GHz

Fig. 13. Back-to-back transition from SIW to AFSIW (source [43]).

C. Air-filled SIW devices

Many AFSIW devices have been developed since the proposal in [24] and [43] of the AFSIW. All these devices are summarized in Table III. It can be observed that low cost and low profile high quality communication devices can also be implemented with AFSIW. Most of these devices have been measured using an AFSIW TRL calibration kit described in [51], and shown in Fig. 14.

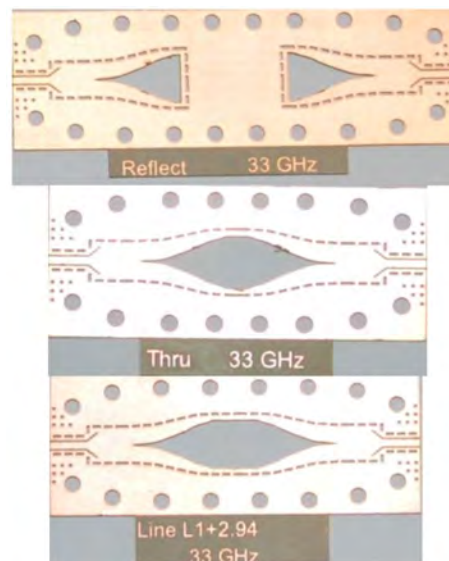


Fig. 14. AFSIW TRL calibraton kit (source [51]).

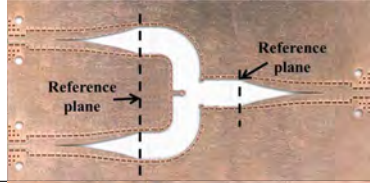
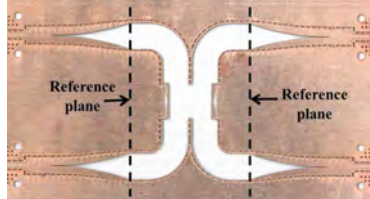



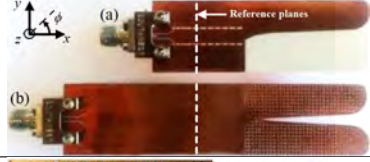
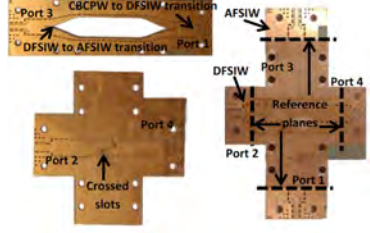
Device	Specifications	Prototype	Performance (all measured values)
T-junction (source [43])	$f \in [26.5, 40]$ GHz		$RL \geq 17$ dB $IL = 3.1 \pm 0.5$ dB Phase imbalance $\pm 2.5^\circ$ $AI = \pm 0.4$ dB Dimensions(mm) = 16.79×26.56
90° hybrid coupler (source [43])	$f \in [32, 36]$ GHz		$RL \geq 15$ dB $IL = 4.6 \pm 0.3$ dB Phase imbalance $90^\circ \pm 2.9^\circ$ $AI = \pm 0.3$ dB
Phase shifter (source [50])	U-band		$RL \geq 13.9$ dB $IL = 0.15 \pm 0.14$ dB Phase shift $30^\circ \pm 2.5^\circ$
Compensated phase shifter (source [48])	Same length as reference line Broadband Ka-band		Same length as reference line $RL \geq 12.5$ dB $IS = 0.35 \pm 0.17$ dB $AI = 0.23 \pm 0.2$ Phase shift = $43^\circ \pm 6^\circ$
Bandpass filter (source [51])	Third order filter $f_0 = 31.65$ GHz BW=15%		$RL \geq 20$ dB $IS = 0.18 \pm 0.17$ dB $Q = 706$ Dimensions(mm) = 7.04×16.64
Antipodal linearly tapered slot antenna (source [52])	Broadband matching $f \in [26, 40]$ GHz $f_0 = 35.5$ GHz		-10 dB IBW = 26-40 GHz xz -plane HPBW(f_0) = 56° xy -plane HPBW(f_0) = 39° Gain(f_0) = 11.7 dBi Cross-pol isolation(f_0) = 8.5 dB
Moreno directional coupler (source [53])	$f \in [26, 40]$ GHz		$RL \geq 15.5$ dB $IL = 0.6 \pm 0.2$ dB Coupling = -18.7 ± 1.3 dB $IS = 31$ dB Directivity = 11 dB

TABLE III

PERFORMANCE OF THE UP-TO-NOW MANUFACTURED DEVICES IN AFSIW. IL: INSERTION LOSS; RL: RETURN LOSS; AI: AMPLITUDE IMBALANCE; BW: -3 dB BANDWIDTH; Q: QUALITY FACTOR; IBW: -10 dB IMPEDANCE BANDWIDTH; HPBW: HALF POWER BEAMWIDTH; IS: ISOLATION

D. Half-mode Air-Filled SIW

Several modifications of the standard substrate integrated waveguide topology have been proposed with the aim of reducing its volume. Some examples are the folded SIW [54], the slow-wave SIW [55], or the half-mode SIW [56]. The same approach has been applied to the AFSIW in [57], where a half-mode AFSIW (or HM-AFSIW) is proposed. Similar to the half-mode SIW, only the quasi- $TE_{p-0.5,0}$ ($p = 1, 2, \dots$) modes can propagate in this structure, and consequently the single mode operation frequency range is approximately twice that in the case of the AFSIW. But since the structure is not closed, there is radiation, especially near the cutoff frequency. This radiation can be used to implement leaky wave antennas. In the case of the HM-AFSIW, the dielectric losses almost disappear when compared to the half-mode SIW. The total loss in the HM-AFSIW is reduced by a factor of 2.2 when compared with the half-mode SIW. A transition from SIW to HM-AFSIW was also presented in [57].

VI. HOLLOW SIW

Almost at the same time as the AFSIW was presented, another empty substrate integrated waveguide was proposed in [25]. It is called Hollow Substrate Integrated Waveguide (HSIW), and it is very similar to the AFSIW. This structure also consists of an emptied SIW with top and bottom metallic covers (see Fig. 15). The main difference is that the HSIW is implemented in low-temperature cofired ceramic (LTCC) technology. Employing LTCC allows the use of a high-permittivity substrate.

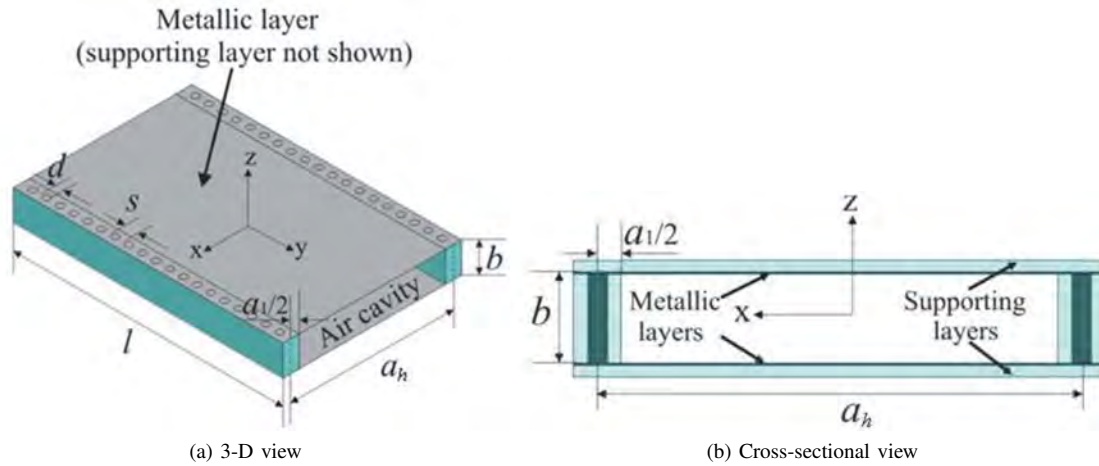


Fig. 15. Hollow substrate integrated waveguide (HSIW) (source [25]).

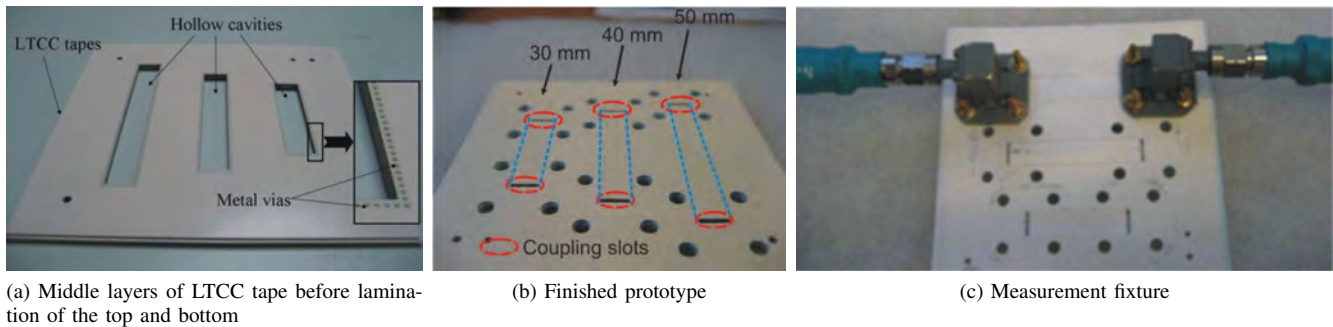


Fig. 16. Manufactured WR28-like HSIW lines with lengths of 30, 40 and 50 mm (source [25]).

In order to derive the propagation characteristics of the HSIW, an effective dielectric constant (EDC) of an equivalent rectangular waveguide completely filled with dielectric is defined in [25]. An expression is derived for the EDC, valid only for lightly loaded waveguides. This expression provides a means to calculate the geometrical parameters of the HSIW in order to achieve a specific cutoff frequency.

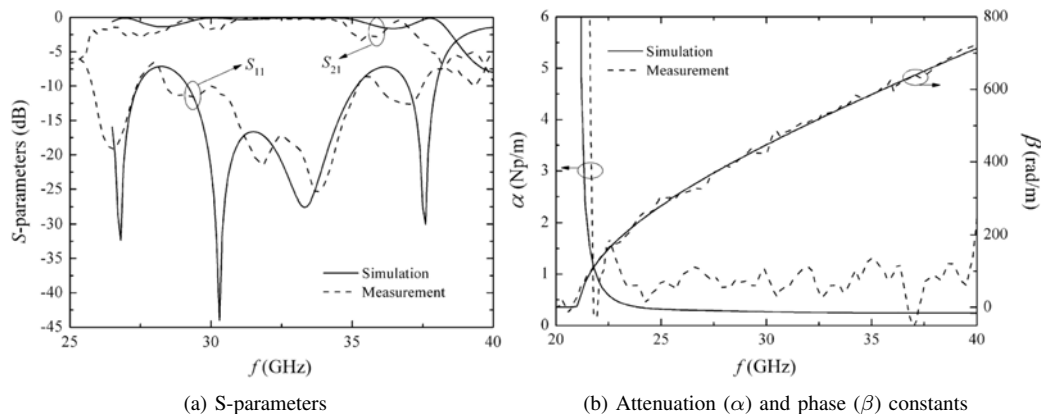


Fig. 17. Measured and simulated parameters of the 30 mm-long HSIW line (source [25]).

Fig. 16 shows three HSIW lines with similar characteristics as those of the WR28 rectangular waveguide, manufactured with LTCC in the same substrate. The three lines have lengths of 30, 40 and 50 mm. The HSIW lines are fed using rectangular

waveguides. A slot in the HSIW is used to couple the rectangular waveguide and the HSIW. The measured and simulated parameters of the 30 mm-long HSIW lines is shown in Fig. 17. There is good agreement between measurements and simulation for the phase constant, but not so for the attenuation constant, which is higher than expected, probably due to surface roughness and voids in the fired silver paste. Even so, an attenuation of 9 dB/m is achieved.

In [58], an HSIW is used to implement a slotted HSIW 6×6 antenna array. The impedance bandwidth is about 1.5 GHz, and the measured peak gain is 17.1 dBi, 1.3 dB lower than simulated.

In [59], a compact transition from coplanar waveguide to HSIW (in this work the HSIW is called empty LTCC integrated waveguide, or E-LIW) is presented. Their back-to-back prototype had insertion losses of 0.5 ± 0.2 dB and return losses over 20 dB from 57 to 66 GHz.

VII. EMPTY SUBSTRATE INTEGRATED COAXIAL LINE (ESICL)

Coaxial lines with air as dielectric medium, either air-filled or air-spaced coaxial lines, were first proposed in the early 1960s [60]-[62]. In these coaxial lines, the substrate was removed in order to obtain components with accurate and predictable electromagnetic properties that could be used as impedance standards due to the small differences between the measured line characteristics and their analytical properties. Since the publication of these first articles, others studies related to air-filled coaxial lines were proposed in [63]-[67]. For instance, air-filled coaxial cables have been employed to achieve immittance transformation, skin-effect corrections, as well as feed networks, just to cite a few examples among many other devices and/or applications. The fabrication of these air-filled cables was difficult, due to the cylindrical geometry of the arrangements employed and due to the low stability of the inner conductor. A new concept for air-filled rectangular coaxial lines using several planar layers arose beginning in 2000[68]-[69]. The proposed coaxial transmission lines (see Fig. 18) were monolithic air-filled rectangular coaxial lines, fabricated for high frequency operation by means of photolithography and copper electroplating processes. The top of the ground metal was partially opened to decrease the use of porous polymer layers. Due to the characteristics of air and the coaxial topology, these structures provided a low level of attenuation (less than 0.08 dB/mm at frequencies from 3 GHz to 38 GHz), low radiation and do not present electromagnetic interferences from other sources.

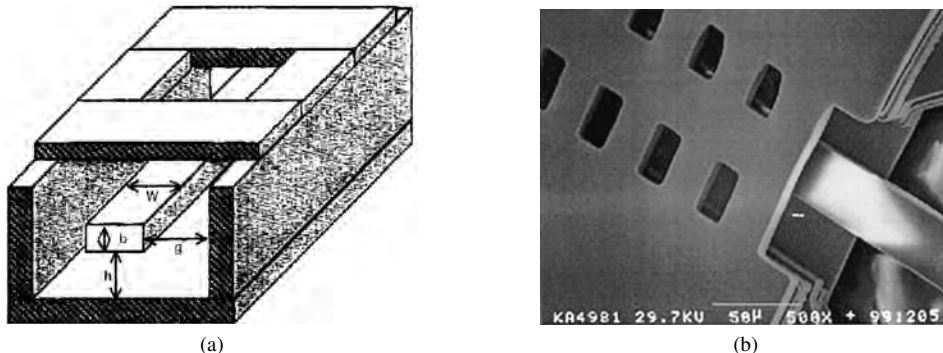


Fig. 18. (a) Air-filled coaxial line (source [68]), (b) fabricated device on thick oxide Si-substrate (source [69]).

These layered air-filled coaxial lines were inspired and based on previous approaches to structures based on conventional transmission lines, e.g. CPW or microstrip lines that operate without dielectric. Among them, the first approximation to a layered empty coaxial line was called the dielectric microshield transmission line presented in [70]. It was a metallic strip over a dielectric membrane with low permittivity to diminish losses, and shielded with a waveguide to avoid radiation. Other approximations were also designed using micromachining techniques but with different arrangements [71]-[81].

After the development of the former air-filled coaxial designs, subsequent research was intended to produce substrate-free coaxial lines with low-cost and high-performance, but employing simpler designs and technology at lower frequency. New structures based on micromachined 3D metallic blocks stacked together were presented in [82]-[87]. Fig. 19 shows the 3D air-filled square coaxial line, composed of five conducting layers. The structure made use of quarter-wavelength stubs connected to ground for fixing the central conductor suspended in air. Both the dielectric and radiation losses are negligible as the line is air filled. In [85], a fabricated prototype of this coaxial line, with a low-loss and wide bandwidth band-pass response at K-band frequencies, was successfully shown.

During the last few years, a new technology to fabricate empty coaxial lines from planar PCB substrate layers has been developed (see [88], [89] and [26]). These methodologies permit to avoid the use of 3D heavy metallic blocks, obtaining layered coaxial designs with low weight and low cost. In contrast to previous structures, transitions from and to other planar transmission lines have been developed for the empty substrate integrated coaxial line (ESICL) allowing it to be completely integrated in a substrate layer using conventional manufacturing processes. It is important to note that previous designs and structures were not completely integrated in substrate layers due to use of 3D structures or the absence of transitions. The main advantages of these empty substrate integrated coaxial lines are low loss due to the absence of dielectric, high Q-factor, fast simulation CPU times, no dispersion, simplicity in its design and fabrication, and low cost.

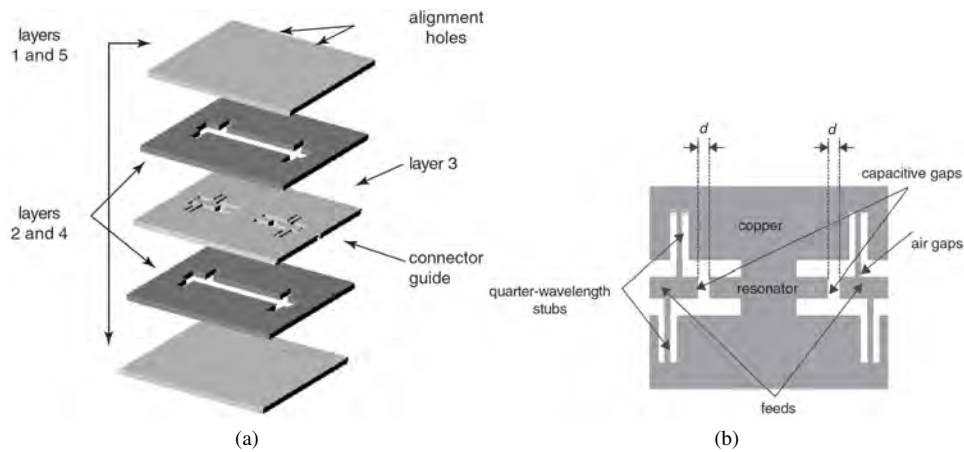


Fig. 19. 3D suspended air-filled coaxial line. a) five-layer coaxial assembly b) top view of layer 3, showing the centre conductor of the coaxial cable filter (source [83]).

A. ESICL Topology

The ESICL is implemented by means of conventional substrate layers. It is not fabricated from metallic 3D blocks, thus differing from the previous methodologies, and so cheaper and simpler designs can be obtained. In addition, the use of adequate transitions permits its easy integration with any planar structure. The general topology of the proposed coaxial transmission line can be observed in Fig. 20, which is composed of five separated PCB layers. The third substrate layer contains the central conductor of the coaxial line that is suspended in air. This layer is separated from the two metallic covers, placed at the first and last position, through two inner empty substrate layers. All dimensions are adjusted to obtain a reference input impedance of 50Ω . Note that the substrate properties do not affect to the structure as it is completely metallized and so very cheap dielectric substrate layers can be employed without any degradation of the ESICL performance.

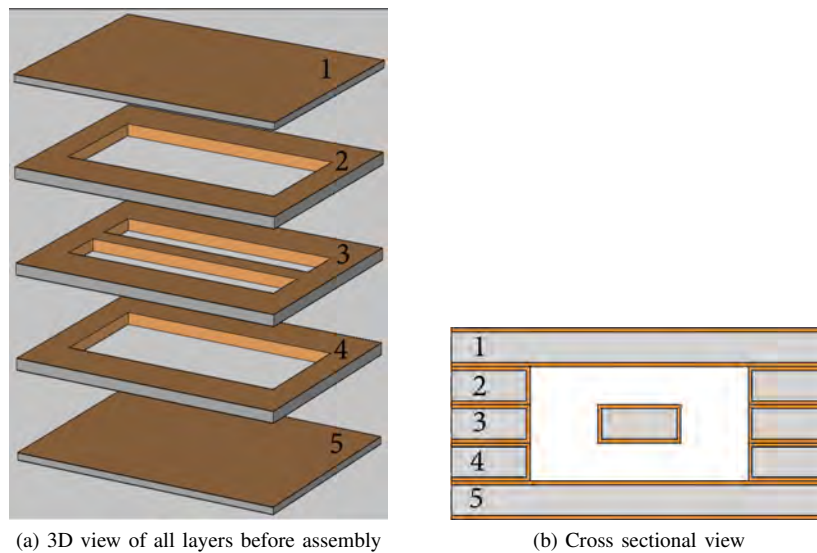


Fig. 20. 3D and cross sectional views of the ESICL. The ESICL is formed by 5 layers: Top cover (1), upper layer (2), central layer (3), lower layer (4), and bottom cover (5). Brown color indicates metallized areas and grey zones are dielectric substrate materials (source [26]).

The structure can be fabricated following standard manufacturing processes employed for mass-production. In summary, three general steps are followed. First, the five substrate layers are drilled, milled and cut. Next, they are metallized and drilled, milled and cut again. Finally, all layers are placed and stacked together using different alignment holes.

B. ESICL Transition

The proposed ESICL and the other air-filled coaxial lines are all very interesting, but they are useless in many real applications if they can not be finally integrated within a substrate. The transitions from and to other planar transmission lines are key for practical applications of this new coaxial line technology. The first topology for a transition of the ESICL from/to a planar line was presented in [26], [90]. A grounded CPW (GCPW) line access was proposed, but any other planar technology (e.g.

microstrip and striplines), or even the novel ESIW and related practical implementations, could have been chosen (introducing slight topological modifications with regard to the proposed transition solution). The final topology obtained for GCPW access ports is shown in Fig. 21.

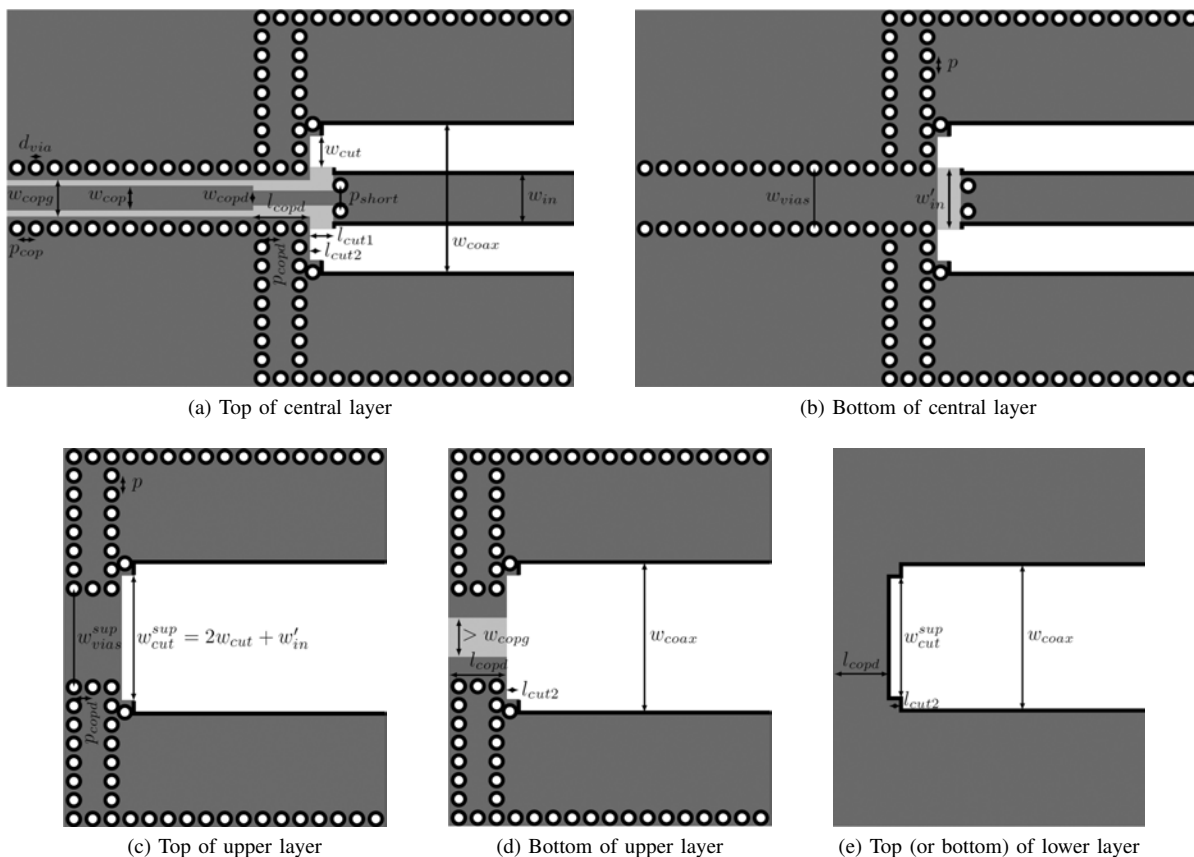


Fig. 21. GCPW to ESICL transition. Top and bottom views of all layers, except for top and bottom covers. White represents metallic via-holes. Light gray stands for substrate without metallic cover. Black represents the metallization along substrate edges (source [26]).

This transition has three different parts. The first one is a planar 50Ω GCPW line that is connected to a second GCPW line shielded by the inner top layer. As a consequence, the width of the central conductor of this second GCPW is reduced to keep 50Ω characteristic impedance to minimize undesired reflections. Finally, the shielded GCPW is connected to the ESICL, while keeping a constant reference impedance of 50Ω within the whole structure. The entire ESICL transition is surrounded by metallic via holes that inhibit signal leakage from the line, and from being potentially coupled inside the waveguides formed by the via holes and the ESICL metallic walls. The transition obtains a smooth change from the quasi-TEM mode of the GCPW to the fundamental TEM mode of the proposed ESICL. The simulated results, shown in Fig. 22, are very good, with good matching conditions over a very wide bandwidth, with reflection levels less than -30 dB and insertion losses less than 0.1 dB.

In addition, a back-to-back configuration of the proposed GCPW to ESICL transition was also manufactured in order to validate its good behavior experimentally. The simulated and measured responses are included in Fig. 23, where reasonable agreement can be observed. The manufactured device was fabricated in a Rogers 4003C substrate ($\epsilon_r = 3.55$, 0.813 mm thickness, and $35 \mu\text{m}$ of copper metallization). The implemented ESICL line (including the two transitions to GCPW) operates rather well over a wide bandwidth (i.e. from low frequency until 20 GHz).

C. ESICL Wide Pass-Band Filter

In order to show the advantages of using the ESICL configuration in filter applications, a wide pass-band filter was presented in [26]. More specifically, an eight cavity filter with a 100% fractional bandwidth, centred at 10 GHz and with an in-band ripple of 0.05 dB, was successfully designed and implemented. Any classical solution for bandpass filters based on coupled resonators can be easily implemented with the proposed ESICL technology. The filter resonators are realized with $\lambda/4$ shorted stubs that are coupled through $\lambda/4$ line sections acting as impedance inverters. The structure includes two transitions that permit the full integration of the filter within the substrate. The filter dimensions and topology are shown in Fig. 24. A prototype was fabricated in Rogers 4003C substrate following standard PCB fabrication procedures. The accurate simulation and optimization

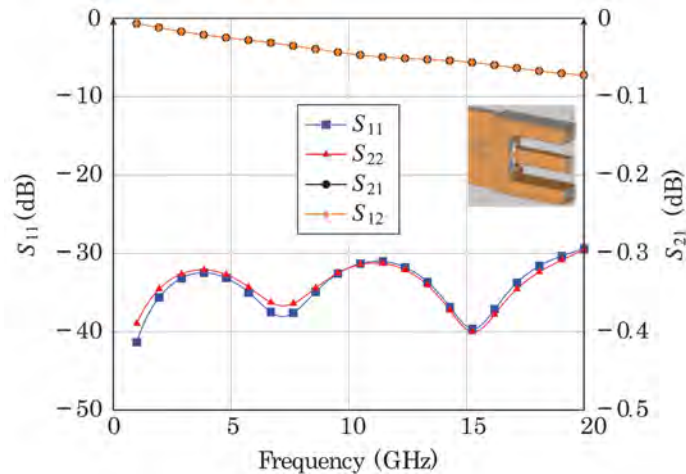
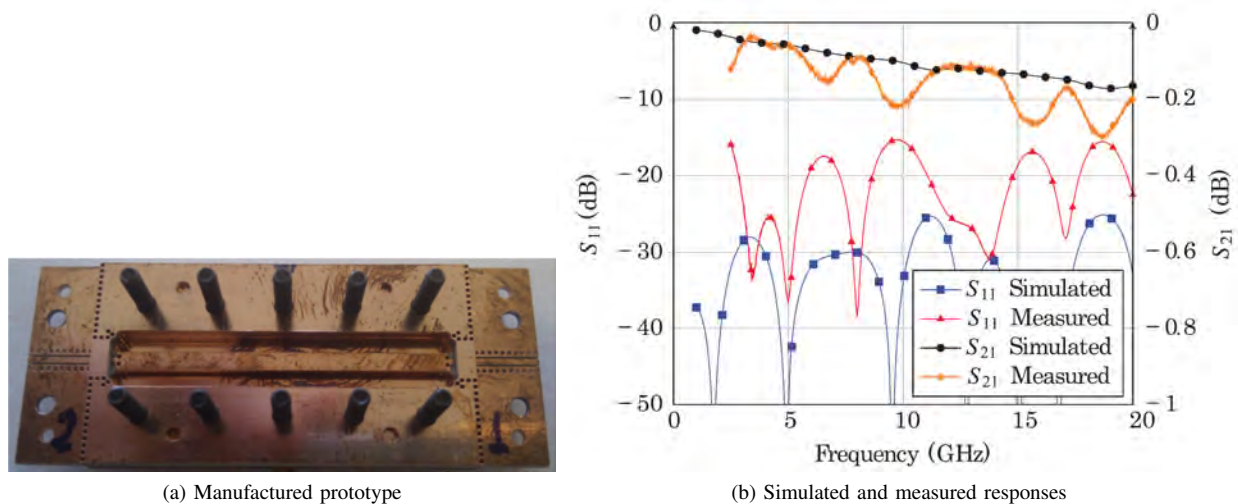


Fig. 22. Simulated GCPW-to-ESICL transition response (source [26]).



(a) Manufactured prototype

(b) Simulated and measured responses

Fig. 23. Back to back transition from GCPW to ESICL (source [26]).

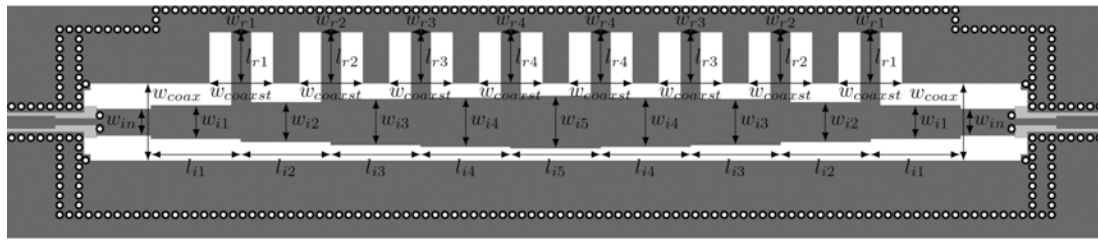
of the filter with commercial full-wave simulators is very fast, as this filter can be analyzed as a completely closed and air-filled structure.

The measured response of the wideband ESICL filter prototype is compared with simulated data in Fig. 25, where good agreement between both results is observed. The measured pass-band covers 5 GHz to 15 GHz, and the insertion loss is below 0.6 dB in the entire in-band frequency range, whereas experimental return losses are better than 13 dB. Such a wide 10 GHz bandwidth, cannot be easily obtained with standard waveguide technology due to dispersion effects and the potential excitation of higher order modes.

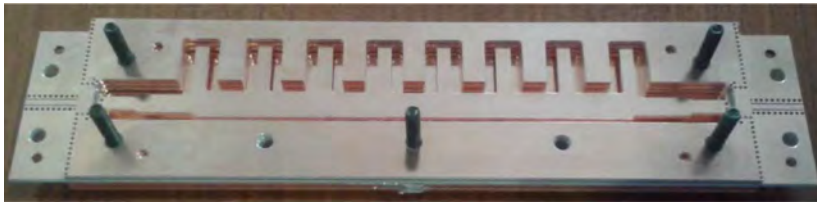
In summary, the potential use of ESICL as a transmission line is very promising for many future applications, particularly in terms of low insertion loss, negligible dispersion, low weight, simple design, cheap manufacturing costs, mass production, and full system integration following standard PCB manufacturing processes.

VIII. DIELECTRICLESS SIW

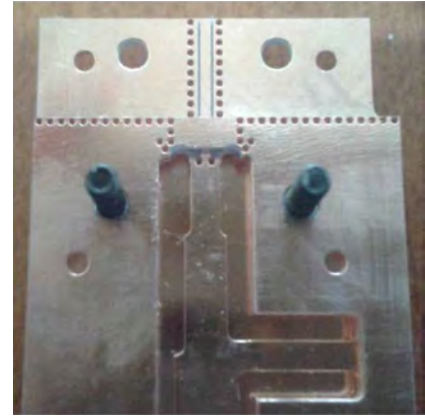
Another type of empty substrate integrated waveguide is the dielectricless substrate integrated waveguide [27], or DSIW. Fig. 26 shows a sketch of this waveguide where a low cost substrate, such as FR4, is milled with a z -controlled milling machine in such a way that a groove is created. This layer is then treated with a chemical bath in order to facilitate ion acceptances and then metallized with electroplating or chemical deposition. The groove forms a hybrid substrate rectangular waveguide, but it still has to be covered with a top metallic layer. The body and the top layers are glued together with a thin layer of prepreg, which has been previously machined in order to leave a hole coincident with the milled zones of the substrate body (see Fig. 26a). The holes in the prepreg layers are of larger diameter than the holes in the milled zones in order to take into



(a) Central layer



(b) Manufactured prototype



(c) Detail of the GCPW to ESICL transition

Fig. 24. Wideband ESICL filter composed of eight cavities (source [26]).

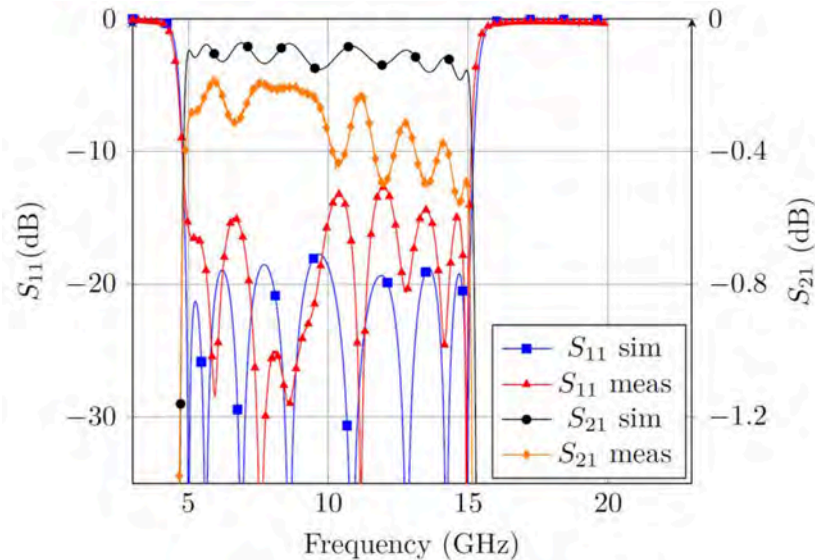


Fig. 25. Measured and simulated response of the wideband ESICL filter prototype (source [26]).

account the enlargement that it will suffer after assembling, and to avoid air gaps or leakage inside the waveguide. Electrical contact between the body and the top cover is accomplished by machining two rows of conductive vias at each side of the guide (see Fig. 26b). The distance and diameter of the vias is selected with the same criteria as for a standard SIW.

Since a small portion of electric field enters the prepreg layer between the lateral walls of the waveguide and the rows of metallized vias, the attenuation is slightly greater than in a rectangular waveguide of the same dimensions. The phase constant is almost identical.

Fig. 27 shows the body substrate with the milled groove before and after metallization of a manufactured dielectricless SIW prototype. The dielectricless SIW is fed with coaxial cables. The holes for the coaxial probe can be seen in Fig. 27.

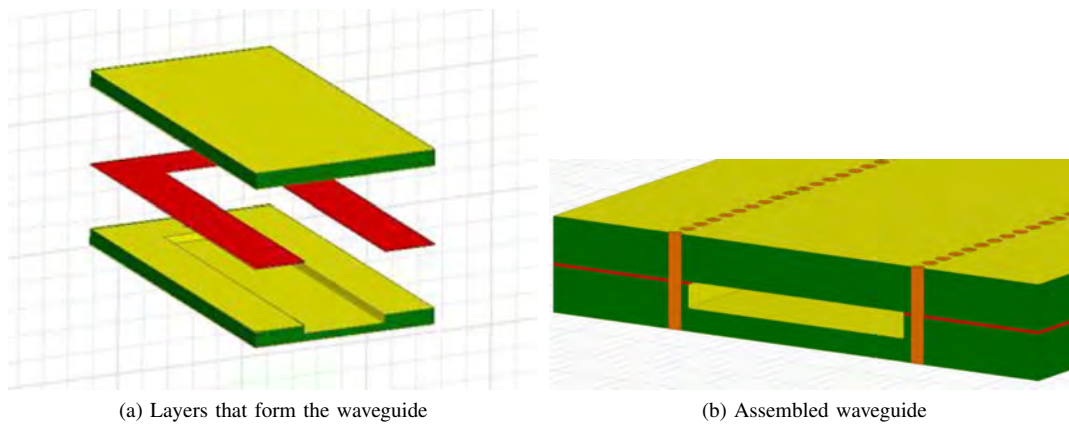


Fig. 26. Sketch of the dielectricless SIW (source [27]).

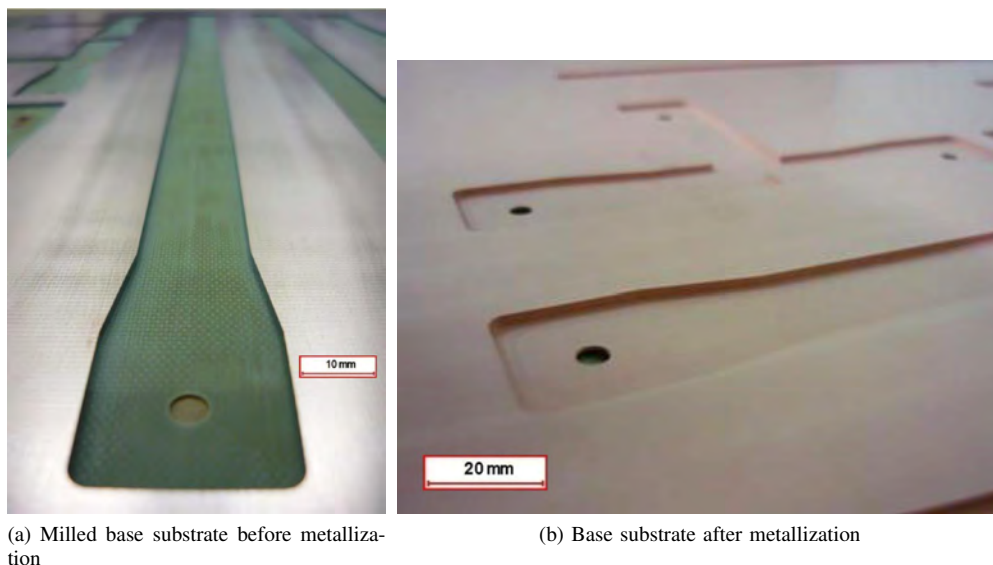


Fig. 27. Sketch of the dielectricless SIW (source [27]).

IX. CONCLUSION

This article has presented much of the published material regarding empty substrate integrated waveguide technologies, highlighting the main characteristics of each one. In order to better summarize all these designs, a comparative table (Table IV) shows the main features of all these empty integrated lines. One conclusion that can be drawn from the information in Table IV is that emptying the substrate either partially or completely drastically reduces or completely eliminates the dielectric losses, without greatly increasing the manufacturing complexity or cost. These lines clearly outperform traditional planar circuits, and they even perform better in terms of losses than the novel substrate integrated waveguide. It is the removal of the dielectric, at the expense of slightly increasing the size, that reduces losses while maintaining low cost and low profile. The performance of these empty substrate integrated waveguides in terms of losses and quality factor is so good that rivals that of high quality (but bulky and expensive) rectangular waveguide, and so they could be a very good alternative for communication applications where low cost, low weight, easy manufacturing and low loss devices are required. Several high performance communications devices (such as filters, antennas, and couplers) have already been successfully manufactured and measured.

ACKNOWLEDGMENT

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Name	Attenuation	Q factor	Height	Simulation method	Manufacturing	Transitions
SIW [91]	4.77 dB/m @ 15 GHz (total losses, simulated)	266 @ 19.5 GHz (measured, [23])	1 substrate + two covers	Several full-wave methods (FEM, MoM+MM, BI-RME, ...)	Laser micromachining or mechanical CNC micro-milling+electroplating	Almost from every planar or 3D line to SIW
MSIW [22]	2.17 dB/m @ 30 GHz (only dielectric)	-	1 substrate + two covers	Inhomogeneous region Perturbational method + mode matching	Not manufactured Partially filled with dielectric	None
ESIW [23]	0.7 dB/m @ 15 GHz (total loss, measured)	2150 @ 15 GHz (measured, maximum achieved)	1 substrate + two covers	Homogeneous region Mode-matching or other general methods (FEM, MoM, FDTD)	Laser micromachining or mechanical CNC micro-milling+electroplating Reflow soldering	microstrip to ESIW coaxial to ESIW
AFSIW [43]	4.41 dB/m @ 33 GHz (only metal)	680 @ 33 GHz	1 substrate + two covers	Dielectric losses neglected Simulated as if homogeneous Lateral walls are circular vias	Laser micromachining Lapping and polishing Sputtering + electro-deposition Partially filled with dielectric	SIW to AFSIW
HSIW [25]	9 dB/m @ 30 GHz (total loss, measured)	-	1 substrate + two covers	Equivalent homogeneous guide Effective dielectric constant Valid for $\epsilon_r \in [2, 12]$ Curve fitting, empirical expressions	Low temperature cofired ceramic (LTCC) Partially filled with dielectric	WR to HSIW
ESICL [26]	0.9 dB/m @ 15 GHz (total loss, measured)	1568 @ 15 GHz (measured, maximum achieved)	3 substrates + two covers	BI-RME, general method (FEM)	Laser micromachining or mechanical CNC micro-milling+electroplating Reflow soldering	GCPW to ESICL
DSIW [27]	0.87 dB/m @ 30 GHz (only dielectric)	-	1 thick substrate + prepeg + metallic cover	Full-wave simulator Lateral walls are vias Dielectric prepeg layer considered	z-controlled milling machine creates groove Chemical bath + electroplating Emptied prepeg + metallic cover Metallic vias	Coaxial to DSIWL

TABLE IV

COMPARISON OF THE DIFFERENT TYPES OF EMPTY SUBSTRATE INTEGRATED WAVEGUIDE TECHNOLOGIES DESCRIBED IN THIS REVIEW. FEM: FINITE ELEMENT METHOD; MOM; METHOD OF MOMENTS; MM: MODE.MATCHING; BI-RME: BOUNDARY INTEGRAL-RESONANT MODE EXPANSION; FDTD: FINITE-DIFFERENCE TIME-DOMAIN METHOD; WR: RECTANGULAR WAVEGUIDE; GCPW: GROUNDED COPLANAR WAVEGUIDE; CNC: COMPUTERIZED NUMERICAL CONTROL.

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