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Non-volatile epsilon-near-zero readout memory

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The lack of memory effect of silicon makes it unfeasible to store electronic data in photonics. Here, we propose a non-volatile readout photonic memory, which is electronically written/erased and optically read. The memory utilizes indium tin oxide (ITO) as a floating gate and exploits its epsilon-near-zero (ENZ) regime and electro-optic activity. Extinction ratios greater than 10 dB in a bandwidth of 100 nm for a 5-μm-long memory are obtained. Furthermore, power consumption in the order of μW with retention times of about years have been predicted. The proposed structure opens a pathway for developing highly integrated electro-optic devices such as memory banks.

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The silicon photonics platform has been highlighted as the most promising technology for developing photonic integrated circuits (PICs) [1]. However, the lack of memory effect of silicon makes it unfeasible for non-volatile applications such as electro-optic data storage.

In order to tackle this problem and combine both photonics and electronics, some solutions based on the same concept as the electronic flash memories have been proposed by either exploiting the silicon plasma dispersion effect [2–5] or utilizing 2D materials like graphene [6]. However, on the one hand, plasma dispersion effect is very weak, which imposes a trade-off between device footprint and broadband optical response. On the other hand, the integration of atomically thin materials, such as graphene, results in a poor overlap of the optical mode and thus, the resulting effect is also weak. Furthermore, keeping graphene quality over time is challenging which increases the difficulty for high-yield and large volume manufacturing.

Phase change materials have been proposed for non-volatile photonic applications [7]. For instance, the integration of GeSbTe (GST) in silicon can provide all-optical [8, 9] and thermo-optic [10, 11] memories. However, GST undergoes its phase change transition to crystalline for temperatures between 413 and 819 K and amorphizes when it is heated above 819 K [12]. As a result, non-volatile GST based switches may consume a significant amount of power and induce thermal cross-talk to adjacent silicon structures.

Transparent conducting oxides (TCOs), such as ITO or Al-doped zinc oxide (AZO), exhibit an epsilon-near-zero regime in the near-infrared spectrum, which can be electronically tuned by accumulating carriers. This extraordinary effect has been exploited for developing ultra-fast, low-power consumption and ultra-compact electro-absorption photonic modulators [13–20]. Also, ITO has been used in a memristor structure with a non-volatile effect [21]. However, it has to be noticed that, in that work, ITO only acts as an electrode and optical losses arise due to the formation of conductive paths between the ITO and the metal electrode. Consequently, ITO does not undergo an optical change and the benefits of the ENZ regime are not exploited.

In this work, we propose to integrate ITO as a floating gate in a flash-like electronic structure to achieve a non-volatile electro-optic readout memory. The memory acts as an electro-absorption switch at telecommunication wavelengths by electrically driving the ITO floating gate between a low and high loss optical state, being the latter in the ENZ regime. Hence, the memory is electronically written/erased and optically read.

The structure of the memory is depicted in Fig. 1, which is comprised of a stack of metal-oxide-metal-oxide-semiconductor (MOMOS). On top of the stack, a 10-nm-thick low-doped ITO layer acts as the control gate to electrically contact the memory. Conversely, the 500×220 nm^2 silicon waveguide is electrically grounded. The floating gate is another low-doped ITO layer to minimize optical losses and is sandwiched between the two oxide layers. The oxide between the semiconductor and the floating gate is known as the tunneling oxide since it enables an electron flow between the floating gate and the semiconductor when a voltage pulse is applied to the control gate ($\pm V_{CG}$). On the other hand, the oxide between the floating and the control gates acts as a blocking layer in order to keep the electrons within the floating gate and avoid any leakage current from the floating to the control gate. The MOMOS waveguide structure is surrounded by a SiO_2 cladding.

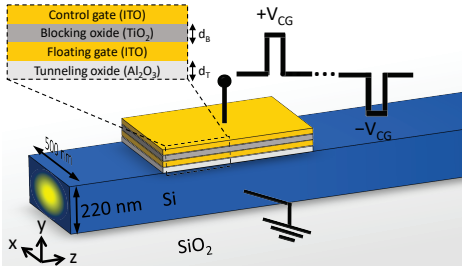

Fig. 1. Schematic illustration of the proposed memory based on a MOMOS structure.

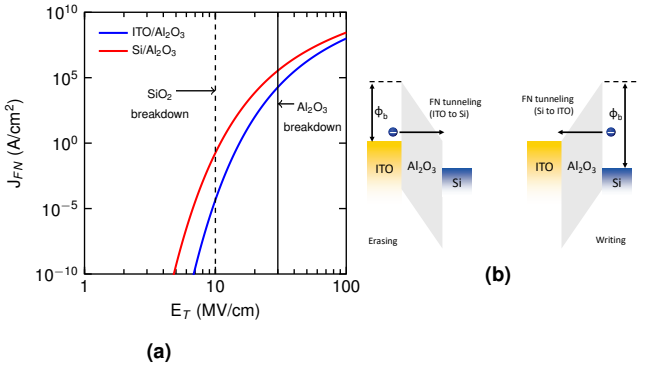

Fig. 2. (a) Fowler-Nordheim current density as a function of the E-field in the tunneling oxide for the ITO/Al_2O_3 and Si/Al_2O_3 interfaces. (b) Band diagram schematic during the memory erasing and writing processes.

The switching mechanism of the tunneling oxide between an insulating and a conducting state is based on the Fowler-Nordheim (FN) quantum mechanical tunneling [22]. The energy bands of the tunneling oxide bend in the presence of a sufficient high electric field that is induced in our case by the control gate voltage. This decrease of the potential barrier enables the flow of a current between the semiconductor and the floating gate. Conversely, when the control voltage is released, the tunneling oxides turns back to insulating and the accumulated carriers inside the floating gate get trapped. The FN current density (J_{FN}) through the tunneling oxide is given by:

$$J_{FN} = \frac{q^3}{8\pi^2 h\phi_b} E_T^2 \exp\left(-\frac{8\pi\sqrt{2m^*}\phi_b^{3/2}}{3hq}\frac{1}{E_T}\right) \quad (1)$$

where q is the fundamental charge, h is the Planck constant, ϕ_b is the energy difference between the tunneling oxide and the interfaced material, m^* is the electron effective mass and E_T is the electric field within the tunneling oxide. It has to be noted that ϕ_b should be calculated for the oxide/Si interface and the oxide/ITO interface depending on whether the floating gate is written (charged) or erased (discharged), respectively.

The ITO-ENZ regime is found for carrier densities around 6.5×10^{20} cm^{-3} at $\lambda = 1.55$ µm. This means that E-fields with values above the dielectric breakdown ($\sim$ 10 MV/cm) of typical oxides such as SiO_2 must be supported by the tunneling oxide. Therefore, we choose Al_2O_3 since it can handle up to 30 MV/cm [23]. The FN current density as a function of the E-field inside the tunneling oxide for the Si/Al_2O_3 and the ITO/Al_2O_3 interfaces is shown in Fig. 2a. It can be noticed that J_{FN} for the ITO/Al_2O_3 interface is shifted to higher E-field intensities due to the higher ϕ_b than the Si/Al_2O_3 interface as it is depicted in Fig. 2b. Furthermore, the utilization of Al_2O_3 instead of SiO_2 allows to increase the FN current density from 10^{-5} to 10^4 A/cm^2, which implies an increment of around 10 orders of magnitude. On the other hand, the utilization of a high-κ dielectric for the blocking oxide helps to reduce both the control voltage and the current leakage induced by the accumulated charge in the floating gate. Hence, we choose TiO_2 as the blocking oxide, which exhibits a static permittivity of 80 [24].

From the electrical point of view, the memory can be seen as a superposition of series and parallel capacitors. On the one hand, the series configuration (see Fig. 3a) occurs when a write/erase voltage pulse is applied to the control gate. On the other hand, the parallel configuration exists when no control voltage is applied, because of the accumulated carriers in the floating gate, which induce an electric potential ($-V_{FG}$) between the floating gate and the semiconductor/control gate (see Fig. 3b). By developing the electrostatics equations of the circuit model we arrive to:

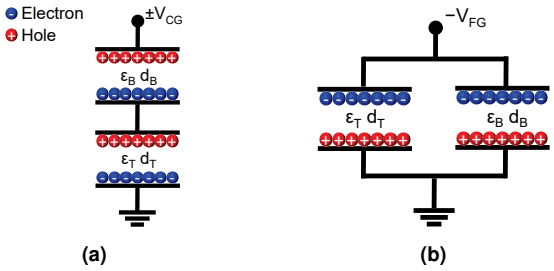

Fig. 3. Equivalent circuit model (a) during and (b) after a voltage pulse is applied to write/erase the memory.

$$E_T = \frac{V_{CG}}{d_T + d_B\frac{\varepsilon_T}{\varepsilon_B}} - \frac{\rho_{FG}}{\varepsilon_T + \varepsilon_B\frac{d_T}{d_B}} \quad (2)$$

where the under-scripts T and B stand for the tunneling and blocking oxide layer, d_i the thickness and ε_i the static permittivity. The surface charge density in the floating gate (ρ_{FG}) is calculated as:

$$\rho_{FG} = \int J_{FN} \cdot dt \quad (3)$$

Hence, the electrical response in the time domain of the MOMOS structure is obtained by combining Eqs. 1-3.

A 5-nm-thick ITO layer is used for the floating gate. Two accumulating layers are formed in both ITO interfaces and, thus, an overlap between them can be expected. Hence, the ITO carrier concentration (N) is estimated with uniform shape and by averaging ρ_{FG} to the floating gate thickness. Several works have utilized the Thomas-Fermi screening theory [25], Drift-Diffusion [26] or Quantum Hydrodynamic [27] models to explain the carrier distribution inside the ITO layer. However, experimental results utilizing ITO in a metal-oxide-semiconductor (MOS) structure do not fully agree with simulation results based on the aforementioned models [28].

The thicknesses of the tunneling and blocking oxides play an important role in terms of the retention time of the memory,

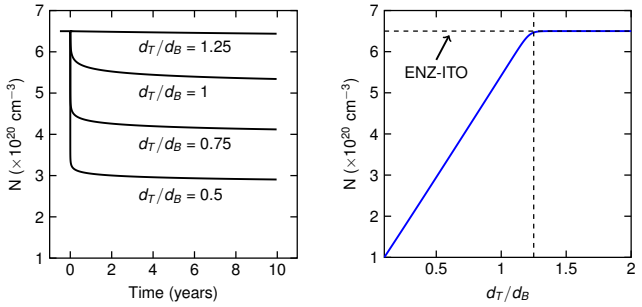

Fig. 4. Accumulated carriers in the floating gate as a function of (a) time for different oxide thicknesses relation and (b) after 5 years.

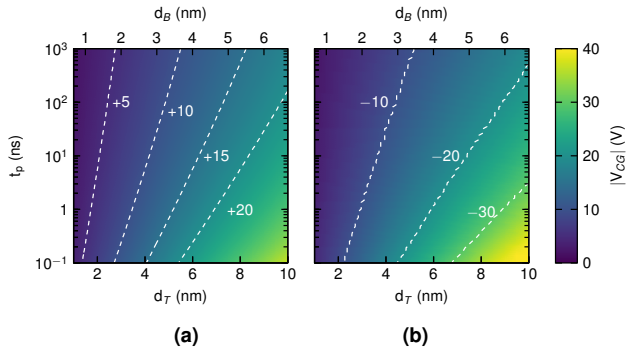

Fig. 5. Voltage needed to drive the ITO floating gate to/from the ENZ regime as a function of the electrical pulse duration and thicknesses of the oxides for the memory (a) writing and (b) erasing processes.

the voltage needed to drive the ITO to/from the ENZ state and the duration of the write and erase electrical pulses. In order to set the thicknesses of the oxides we first analyze the retention time after the writing pulse is applied and then, the ITO floating gate is driven to the ENZ regime. By inspecting Eq. 2, it can be noticed that the leakage current induced by the accumulated carriers depends on the relation between the tunneling and oxide thicknesses. The time evolution of the carrier density for different oxides thickness relations is shown in Fig. 4a. Initially, the floating gate experiences a rapid drop of its carrier concentration due to the self-induced FN current by the accumulated carriers. This rapid discharge reduces the E-field and, hence, the leakage current is diminished to almost negligible values. In order to achieve long retention times and avoid a degradation of the ITO-ENZ regime, the oxides thickness relation must be greater than 1.25 as it is shown in Fig. 4b, where the carrier concentration as a function of the oxides thickness relation after 5 years is depicted.

Considering the aforementioned results, the oxides thickness relation is set to 1.25 and the influence of the electric parameters such as the amplitude and duration (t_p) of the control voltage pulse is investigated. Figs. 5a and 5b show the contour maps of the control gate voltage that is necessary to drive the ITO in the ENZ regime (writing process) and to fully discharge the ITO from this state (erasing process), respectively. For both

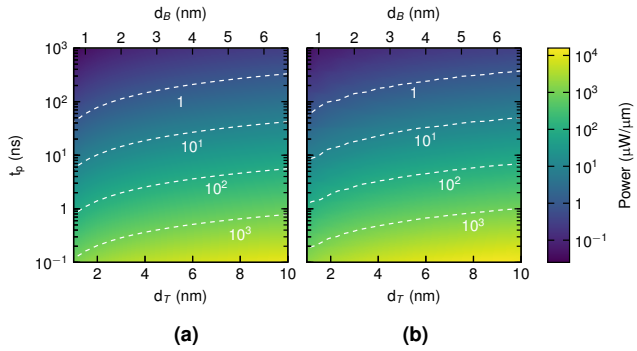

Fig. 6. Power consumption of the memory per length to switch ITO floating gate to/from the ENZ regime as a function of the electrical pulse duration and thicknesses of the oxides for the memory (a) writing and (b) erasing processes

processes, the lower the oxides thickness, the lower the control voltage needed, since $E_T \propto 1/d$. On the other hand, for a given thickness, the control voltage can be reduced at the expense of the need to apply longer control pulses and vice versa. Therefore, the accumulated charge can be obtained by either applying a high voltage in a short time or a lower voltage in a longer time, taking into account that $E_T \propto V_{CG}$. Finally, the erasing process shows slightly higher power consumption for the same pulse duration because of the different ϕ_b between both processes. This imposes the use of higher control voltage to erase than to write the memory because of the higher band energy of ITO/Al_2O_3, as stated before.

The power consumption to write/erase the memory can be calculated as:

$$P_{switch} = \frac{1}{4}\frac{CV_{CG}^2}{t_p} \tag{4}$$

where C is the equivalent capacitance of the two series capacitors formed by the tunneling and blocking oxide layers (see Fig. 3a). Figs. 6a and 6b show the power consumption per length for the written and erased processes, respectively, in order to charge and discharge the ITO floating gate to/from the ENZ regime as a function of the oxide thicknesses and the control voltage pulse. As it can be noticed, the power consumption does not show a sharp variation with the oxides thicknesses unlike the control voltage. This is because the lowering of the control voltage with the oxides thicknesses is counteracted by an increase of the total capacitance. Hence, the power consumption is mainly determined by the duration of the control voltage pulse. Power consumption lower than μW could be achieved for pulse durations below the μs range with memory lengths of few microns.

In order to analyze the optical response of the memory after the writing and erasing processes, the thicknesses of the tunneling and oxide layers are fixed to 6 and 4 nm, respectively. These are feasible values to achieve by atomic layer deposition (ALD) [23, 29]. Thus, the MOMOS structure could be fabricated by using ALD. On the other hand, the silicon waveguide could be electrically contacted by using silicon contact strips [18], whereas for the ITO control gate a sub-micron via would be used.

The ITO carrier density is mapped to refractive index by applying the Drude model:

$$\varepsilon = \varepsilon_\infty \left(1 - \frac{\omega_p^2}{\omega^2 + j\omega\Gamma}\right) \tag{5}$$

where $\varepsilon_\infty = 3.9$ is the high-frequency ITO permittivity; $\Gamma = 1.8 \times 10^{14}$ rad/s is the damping factor [30]; ω is the angular

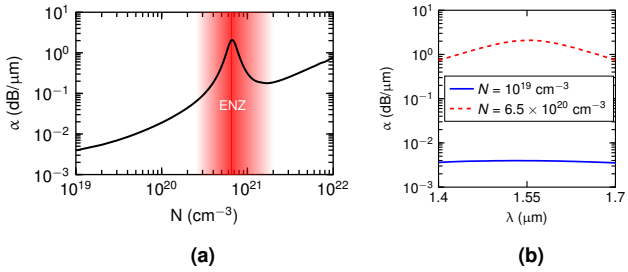

Fig. 7. Propagation losses for the TM-like mode as a function of the (a) ITO carrier concentration at $\lambda = 1.55$ μm and (b) the wavelength in the low-loss ($N = 10^{19}$ cm^{-3}) and ENZ ($N = 6.5 \times 10^{20}$ cm^{-3}) states.

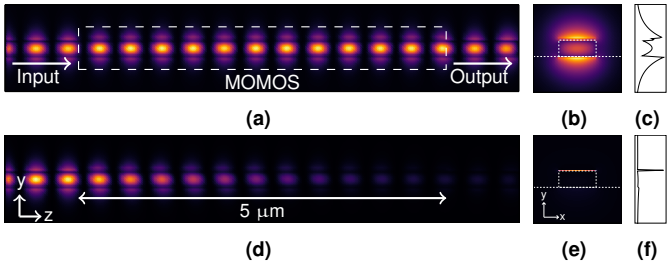

Fig. 8. 3D-FDTD simulations of the optical mode propagation for the memory state after the (a) erasing and (d) writing processes. Mode profiles (E_y) and y-cut of the mode profile after the (b, c) erasing and (e, f) writing processes. Simulations were carried out at $\lambda = 1.55$ μm.

frequency and ω_p is the plasma frequency which is given by:

$$\omega_p = \sqrt{\frac{Nq^2}{\varepsilon_\infty \varepsilon_0 m^*}} \tag{6}$$

being N the ITO carrier concentration; q the fundamental charge; ε_0 the vacuum permittivity and $m^* = 0.35m_e$ the effective electron mass, being m_e the rest mass of the electron.

Because the MOMOS structure is vertically stacked, the memory works with transverse-magnetic (TM) polarization. The mode profiles and effective indices are calculated by using a finite element method (FEM) solver. Fig. 7a depicts the propagation losses as a function of the carrier concentration of the ITO floating gate. The peak loss found in the ITO ENZ regime is enabled by the combination of the lossy ITO and the lowering of the ITO-$|\varepsilon|$. The latter drastically enhances the confinement of the optical mode within the floating gate ITO layer as shown in Figs. 8e and 8f. The effective index of the optical mode outside the MOMOS structure is 1.77, whereas inside is $1.82 + j1.12 \times 10^{-4}$ ($N = 10^{19}$ cm^{-3}) and $1.80 + j5.78 \times 10^{-2}$ ($N = 6.5 \times 10^{20}$ cm^{-3}). In the low-loss state ($N = 10^{19}$ cm^{-3}) the propagation losses are below 0.02 dB/μm and increase up to 2.1 dB/μm when the ITO is driven to the ENZ state ($N = 6.5 \times 10^{20}$ cm^{-3}), thus, propagation losses between both states show a difference of more than 2 orders of magnitude. Furthermore, the memory exhibits a broadband optical response as shown in Fig. 7b. An ultra-high optical bandwidth, far beyond 100 nm is achieved thanks to the use of a non-resonant structure and low wavelength dependence of ITO.

Figs. 8a and 8d show the 3D finite-difference time-domain (3D-FDTD) simulated mode propagation in both memory states for a 5-μm-long memory. The memory exhibits 0.2 dB and 10.6 dB of losses after the erasing and writing processes, respectively, which is in agreement with FEM propagation losses simulations. Furthermore, power consumption of around 1 μW could be achieved for voltage control pulses of 11 V (writing) and 12 V (erasing) with a pulse duration of ~ 1 μs.

In this work we have proposed a non-volatile electro-optic readout memory by exploiting the ENZ regime of a ITO floating gate. The memory could be electrically written and optically read by acting as a non-volatile electro-absorption switch. Retention times of about a decade have been predicted with power consumptions in the μW range. Furthermore, insertion losses as low as 0.2 dB with an optical extinction ratio above 10 dB have been obtained for a 5-μm-long memory with an optical bandwidth greater than 100 nm.

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REFERENCES

1. R. Soref, IEEE J. Sel. Top. Quantum Electron. **12**, 1678 (2006).
2. C. A. Barrios and M. Lipson, J. Light. Technol. **24**, 2898 (2006).
3. J.-F. Song, A. E. J. Lim, X. S. Luo, Q. Fang, C. Li, L. X. Jia, X. G. Tu, Y. Huang, H. F. Zhou, T. Y. Liow, and G. Q. Lo, Opt. Express **24**, 21744 (2016).
4. J. F. Song, X. S. Luo, A. E. J. Lim, C. Li, Q. Fang, T. Y. Liow, L. X. Jia, X. G. Tu, Y. Huang, H. F. Zhou, and G. Q. Lo, Sci. Reports **6**, 1 (2016).
5. M. Grajower, N. Mazurski, J. Shappir, and U. Levy, Laser Photonics Rev. **12**, 1 (2018).
6. Y. Li, H. Yu, T. Dai, J. Jiang, G. Wang, L. Yang, W. Wang, J. Yang, and X. Jiang, IEEE Photonics Technol. Lett. **28**, 284 (2016).
7. M. Wuttig, H. Bhaskaran, and T. Taubner, Nat. Photonics **11**, 465 (2017).
8. C. Rios, M. Stegmaier, P. Hosseini, D. Wang, T. Scherer, C. D. Wright, H. Bhaskaran, and W. H. Pernice, Nat. Photonics **9**, 725 (2015).
9. X. Li, N. Youngblood, C. Rios, Z. Cheng, W. H. P. Pernice, C. D. Wright, and H. Bhaskaran, Optica **6**, 1 (2019).
10. H. Zhang, L. Zhou, B. M. Rahman, X. Wu, L. Lu, Y. Xu, J. Xu, J. Song, Z. Hu, L. Xu, and J. Chen, IEEE Photonics J. **10**, 1 (2018).
11. P. Xu, J. Zheng, J. K. Doylend, and A. Majumdar, ACS Photonics **6**, 553 (2019).
12. Z. Yu, J. Zheng, P. Xu, W. Zhang, and Y. Wu, IEEE Photonics Technol. Lett. **30**, 250 (2018).
13. V. J. Sorger, N. D. Lanzillotti-Kimura, R. M. Ma, and X. Zhang, Nanophotonics. **1**, 17 (2012).
14. K. Shi, R. R. Haque, B. Zhao, R. Zhao, and Z. Lu, Opt. Lett. **39**, 4978 (2014).
15. Q. Gao, E. Li, and A. X. Wang, Photonics Res. **6**, 277 (2018).
16. M. G. Wood, S. Campione, S. Parameswaran, T. S. Luk, J. R. Wendt, D. K. Serkland, and G. A. Keeler, Optica. **5**, 233 (2018).
17. X. Liu, K. Zang, J. H. Kang, J. Park, J. S. Harris, P. G. Kik, and M. L. Brongersma, ACS Photonics **5**, 4484 (2018).
18. E. Li, Q. Gao, R. T. Chen, and A. X. Wang, Nano Lett. **18**, 1075 (2018).
19. E. Li, Q. Gao, S. Liverman, and A. X. Wang, Opt. letters **43**, 11 (2018).
20. E. Li, B. A. Nia, B. Zhou, and A. X. Wang, Photonics Res. **7**, 473 (2019).
21. C. Hoessbacher, Y. Fedoryshyn, A. Emboras, A. Melikyan, M. Kohl, D. Hillerkuss, C. Hafner, and J. Leuthold, Optica. **1**, 198 (2014).
22. R. H. Fowler and L. Nordheim, Proc. Royal Soc. A **119**, 173 (1928).
23. H. C. Lin, P. D. Ye, and G. D. Wilk, Appl. Phys. Lett. **87**, 1 (2005).
24. G. D. Wilk, R. M. Wallace, and J. M. Anthony, J. Appl. Phys. **89**, 5243 (2001).
25. A. P. Vasudev, J.-H. Kang, J. Park, X. Liu, and M. L. Brongersma, Opt. Express **21**, 26387 (2013).
26. G. Sinatkas, A. Pitilakis, D. C. Zografopoulos, R. Beccherelli, and E. E. Kriezis, J. Appl. Phys. **121** (2017).
27. U. Koch, C. Hoessbacher, J. Niegemann, C. Hafner, and J. Leuthold, IEEE Photonics J. **8** (2016).
28. Q. Gao, E. Li, and A. X. Wang, Opt. Mater. Express **8**, 2850 (2018).
29. J. P. Niemelä, G. Marin, and M. Karppinen, Semicond. Sci. Technol. **32** (2017).
30. F. Michelotti, L. Dominici, E. Descrovi, N. Danz, and F. Menchini, Opt. Lett. **34**, 839 (2009).

FULL REFERENCES

1. R. Soref, "The Past , Present , and Future of Silicon Photonics," IEEE J. Sel. Top. Quantum Electron. **12**, 1678–1687 (2006).
2. C. A. Barrios and M. Lipson, "Silicon Photonic Read-Only Memory," J. Light. Technol. **24**, 2898–2905 (2006).
3. J.-F. Song, A. E. J. Lim, X. S. Luo, Q. Fang, C. Li, L. X. Jia, X. G. Tu, Y. Huang, H. F. Zhou, T. Y. Liow, and G. Q. Lo, "Silicon photonic integrated circuits with electrically programmable non-volatile memory functions," Opt. Express **24**, 21744 (2016).
4. J. F. Song, X. S. Luo, A. E. J. Lim, C. Li, Q. Fang, T. Y. Liow, L. X. Jia, X. G. Tu, Y. Huang, H. F. Zhou, and G. Q. Lo, "Integrated photonics with programmable non-volatile memory," Sci. Reports **6**, 1–7 (2016).
5. M. Grajower, N. Mazurski, J. Shappir, and U. Levy, "Non-Volatile Silicon Photonics Using Nanoscale Flash Memory Technology," Laser Photonics Rev. **12**, 1–8 (2018).
6. Y. Li, H. Yu, T. Dai, J. Jiang, G. Wang, L. Yang, W. Wang, J. Yang, and X. Jiang, "Graphene-based floating-gate nonvolatile optical switch," IEEE Photonics Technol. Lett. **28**, 284–287 (2016).
7. M. Wuttig, H. Bhaskaran, and T. Taubner, "Phase-change materials for non-volatile photonic applications," Nat. Photonics **11**, 465–476 (2017).
8. C. Rios, M. Stegmaier, P. Hosseini, D. Wang, T. Scherer, C. D. Wright, H. Bhaskaran, and W. H. Pernice, "Integrated all-photonic non-volatile multi-level memory," Nat. Photonics **9**, 725–732 (2015).
9. X. Li, N. Youngblood, C. Rios, Z. Cheng, W. H. P. Pernice, C. D. Wright, and H. Bhaskaran, "Fast and reliable storage using a 5-bit, non-volatile photonic memory cell," Optica **6**, 1–6 (2019).
10. H. Zhang, L. Zhou, B. M. Rahman, X. Wu, L. Lu, Y. Xu, J. Xu, J. Song, Z. Hu, L. Xu, and J. Chen, "Ultracompact Si-GST hybrid waveguides for nonvolatile light wave manipulation," IEEE Photonics J. **10**, 1–10 (2018).
11. P. Xu, J. Zheng, J. K. Doylend, and A. Majumdar, "Low-Loss and Broadband Nonvolatile Phase-Change Directional Coupler Switches," ACS Photonics **6**, 553–557 (2019).
12. Z. Yu, J. Zheng, P. Xu, W. Zhang, and Y. Wu, "Ultracompact electro-optical modulator-based Ge2Sb2Te5 on Silicon," IEEE Photonics Technol. Lett. **30**, 250–253 (2018).
13. V. J. Sorger, N. D. Lanzillotti-Kimura, R. M. Ma, and X. Zhang, "Ultra-compact silicon nanophotonic modulator with broadband response," Nanophotonics. **1**, 17–22 (2012).
14. K. Shi, R. R. Haque, B. Zhao, R. Zhao, and Z. Lu, "Broadband electro-optical modulator based on transparent conducting oxide," Opt. Lett. **39**, 4978 (2014).
15. Q. Gao, E. Li, and A. X. Wang, "Ultra-compact and broadband electro-absorption modulator using an epsilon-near-zero conductive oxide," Photonics Res. **6**, 277 (2018).
16. M. G. Wood, S. Campione, S. Parameswaran, T. S. Luk, J. R. Wendt, D. K. Serkland, and G. A. Keeler, "Gigahertz speed operation of epsilon-near-zero silicon photonic modulators," Optica. **5**, 233 (2018).
17. X. Liu, K. Zang, J. H. Kang, J. Park, J. S. Harris, P. G. Kik, and M. L. Brongersma, "Epsilon-Near-Zero Si Slot-Waveguide Modulator," ACS Photonics **5**, 4484–4490 (2018).
18. E. Li, Q. Gao, R. T. Chen, and A. X. Wang, "Ultracompact Silicon-Conductive Oxide Nanocavity Modulator with 0.02 Lambda-Cubic Active Volume," Nano Lett. **18**, 1075–1081 (2018).
19. E. Li, Q. Gao, S. Liverman, and A. X. Wang, "One-volt silicon photonic crystal nanocavity modulator with indium oxide gate," Opt. letters **43**, 11–14 (2018).
20. E. Li, B. A. Nia, B. Zhou, and A. X. Wang, "Transparent conductive oxide-gated silicon microring with extreme resonance wavelength tunability," Photonics Res. **7**, 473 (2019).
21. C. Hoessbacher, Y. Fedoryshyn, A. Emboras, A. Melikyan, M. Kohl, D. Hillerkuss, C. Hafner, and J. Leuthold, "The plasmonic memristor: a latching optical switch," Optica. **1**, 198 (2014).
22. R. H. Fowler and L. Nordheim, "Electron Emission in Intense Electric Fields," Proc. Royal Soc. A **119**, 173–181 (1928).
23. H. C. Lin, P. D. Ye, and G. D. Wilk, "Leakage current and breakdown electric-field studies on ultrathin atomic-layer-deposited Al2O3 on GaAs," Appl. Phys. Lett. **87**, 1–3 (2005).
24. G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High-κ gate dielectrics: Current status and materials properties considerations," J. Appl. Phys. **89**, 5243–5275 (2001).
25. A. P. Vasudev, J.-H. Kang, J. Park, X. Liu, and M. L. Brongersma, "Electro-optical modulation of a silicon waveguide with an "epsilon-near-zero" material," Opt. Express **21**, 26387 (2013).
26. G. Sinatkas, A. Pitilakis, D. C. Zografopoulos, R. Beccherelli, and E. E. Kriezis, "Transparent conducting oxide electro-optic modulators on silicon platforms: A comprehensive study based on the drift-diffusion semiconductor model," J. Appl. Phys. **121** (2017).
27. U. Koch, C. Hoessbacher, J. Niegemann, C. Hafner, and J. Leuthold, "Digital plasmonic absorption modulator exploiting epsilon-near-zero in transparent conducting oxides," IEEE Photonics J. **8** (2016).
28. Q. Gao, E. Li, and A. X. Wang, "Comparative analysis of transparent conductive oxide electro-absorption modulators [Invited]," Opt. Mater. Express **8**, 2850 (2018).
29. J. P. Niemelä, G. Marin, and M. Karppinen, "Titanium dioxide thin films by atomic layer deposition: A review," Semicond. Sci. Technol. **32** (2017).
30. F. Michelotti, L. Dominici, E. Descrovi, N. Danz, and F. Menchini, "Thickness dependence of surface plasmon polariton dispersion in transparent conducting oxide films at 1.55 μm," Opt. Lett. **34**, 839 (2009).