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One-Cycle Zero-Integral-Error Current Control for Shunt Active Power Filters

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Abstract: Current control has, for decades, been one of the more challenging research fields in the development of power converters. Simple and robust nonlinear methods like hysteresis or sigma-delta controllers have been commonly used, while sophisticated linear controllers based on classical control theory have been developed for PWM-based converters. The one-cycle current control technique is a nonlinear technique based on cycle-by-cycle calculation of the ON time of the converter switches for the next switching period. This kind of controller requires accurate measurement of voltages and currents in order achieve a precise current tracking. These techniques have been frequently used in the control of power converters generating low-frequency currents, where the reference varies slowly compared with the switching frequency. Its application is not so common in active power filter current controllers due to the fast variation of the references that demands not only accurate measurements but also high-speed computing. This paper proposes a novel one-cycle digital current controller based on the minimization of the integral error of the current. Its application in a three-leg four-wire shunt active power filter is presented, including a stability analysis considering the switching pattern selection. Furthermore, simulated and experimental results are presented to validate the proposed controller.

Keywords: current control; power converters; one-cycle controller; active power filters; power quality

1. Introduction

Shunt active power filters (SAPFs) improve the power quality and energy efficiency in electrical systems by compensating the effects of unbalanced currents, reactive power, and harmonic distortion produced by inefficient loads [1,2]. The SAPF measures load currents and grid voltages at the point of common coupling (pcc) and then generates the inefficient currents required by the load, as shown in Figure 1. In this way, the grid provides only useful power, improving power quality and energy efficiency of the grid.

SAPF current control methods can be classified into two groups: (i) linear designs based on small-signal models of the SAPF, and (ii) nonlinear designs base on large-signal models of the SAPF. Linear controllers are based on the application of linear control theory to linearized SAPF models. In this way, [3–7] propose the use of proportional (P) controllers, proportional–integral (PI) controllers, and linear quadratic Gaussian (LQG) regulators, all working in a synchronous reference frame. In [3,8] the use of proportional resonant (PR) controllers is proposed. In [9], the use of an H_∞ robust control design technique together with a Kalman filter for state estimation is proposed. In [10,11], a minimum

time deadbeat control is proposed. Finally, [12] proposes the application of model predictive control (MPC) together with a modulation algorithm to improve the current ripple.

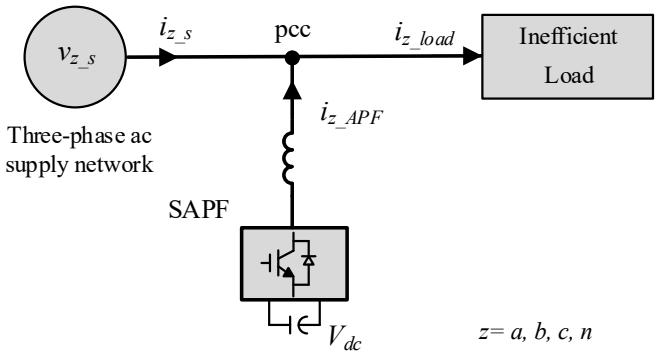


Figure 1. Shunt active power filter (SAPF) connection.

As a result of the linearization of SAPF models, the control may degrade when the SAPF is not working close to the linearization point. Although the design of robust controllers might guarantee the stability for the whole operating range of the SAPF, it comes at the cost of performance degradation.

Some nonlinear controllers applied to the SAPF are the following: hysteresis band current control (HCC) [13–17], sigma-delta control (SDC) [18,19], sliding mode control (SMC) [20–22], and one-cycle control (OCC) [23–28].

The great advantage of HCC is its implementation simplicity and its good dynamic response; however, the variable switching frequency is its main drawback. In order to alleviate this problem, in [15–17], changing the hysteresis band width dynamically (i.e., adjustable hysteresis band) is proposed, so as to obtain a quasi-fixed switching frequency.

SDC operation is asynchronous, hence, it suffers from the same drawbacks as HCC. In order to obtain synchronous sigma-delta control (SSDC), either an external clock signal is added to the sigma-delta modulator [19], or an adjustable hysteresis band (AHB) is used in the comparator of the sigma-delta modulator [18]. However, in [19], although the switching frequency is bounded by the external clock, it is not fixed because it may be the case that when switching happens, the integral error has not reached the hysteresis bound yet. In the case of using an AHB, as in [18], a fixed switching frequency can be obtained but at the cost of variable performance, because the current ripple depends on the hysteresis band, which is adjusted accordingly to keep the switching frequency fixed.

The HCC and SDC may be treated as special cases of SMC. SMC defines a sliding surface that characterizes the desired system performance, and a switched control that maintains the system on the surface. SMC is a well-developed theory with stable and robust results for general nonlinear control systems. However, as previously discussed, the design of SMC through HCC [20] and SDC results in controllers that can guarantee constant switching frequency or fixed system performance, but not both.

Finally, OCC guarantees that, for each switching cycle, the duty cycle is adjusted to accomplish some control objective. In [27], the duty cycle is computed to compensate the reactive power and harmonic distortion of load currents for single-phase and three-phase APFs. In [25], OCC is applied to a three-phase APF system operating with asymmetrical grid voltages and a load demanding unbalanced and nonlinear currents; and in [26], OCC is used in a three-phase four-leg APF to compensate the unbalanced, reactive and harmonic components of the load currents. Finally, OCC is used to compensate only for the load current harmonic components [23,24].

In this work, a new SAPF current control designed on the basis of the OCC paradigm is proposed. This control is based on the minimization of the integral error of the current on each switching period. Hence, the proposed control provides, with fixed switching frequency, a constant performance level of zero current integral error for each switching cycle. The influence of the switching pattern in the controller stability has also been studied. As a result, an alternating switching pattern strategy is selected

to achieve stable behavior of the controller independently of the grid voltage sign. Implementation of this controller requires accurate measurements and high-speed computing to calculate the next switching period control in time. A real setup has been developed using a powerful microcontroller performing high-speed computing, combined with sigma-delta modulators to obtain precise measures at high sampling frequencies.

The paper is structured as follows. In Section 2, the current control application is presented. In Section 3, the proposed controller is derived, and the stability analysis is presented. Section 4 presents stability analysis considering different switching patterns and the final control algorithm. In Section 5, the control algorithm is tested under simulation. Section 6 shows the experimental setup and the obtained results. Finally, Section 7 includes the conclusions of the work.

2. Problem Statement

Consider the three-leg four-wire grid-tied power converter presented in Figure 2. The converter operates as a three-phase voltage source inverter (VSI) connected to the ac power network through inductances $L_{a,b,c}$. Equivalent series resistance (ESR) of the dc bus capacitors and the resistive part of the inductances are neglected for clarity. The fourth wire connects the neutral wire of the power network to the dc bus midpoint. This power stage configuration is commonly used in SAPFs and can be treated as three independent single-phase converters sharing a unique dc bus. The VSI switches should be an IGBT–diode association allowing bi-directional current flow. The switches of a branch are controlled in a complementary fashion, meaning that at any time, only one switch per branch is in the ON state. Neglecting switching times, also for simplicity, only two states are possible and the per-phase equivalent circuit of Figure 3 is obtained. The control system should include dc bus voltage regulation; dc bus midpoint voltage unbalances compensation and ac-side current control.

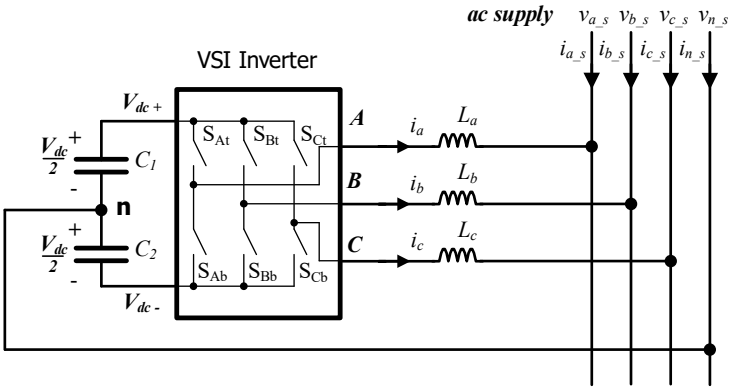


Figure 2. Three-leg four-wire grid-tied converter.

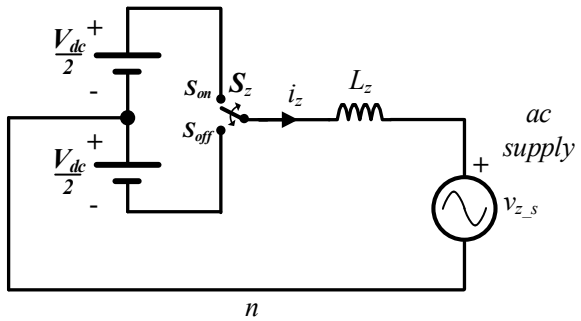


Figure 3. Per-phase equivalent circuit of the grid-tied converter.

Consider now the application of one-cycle current control, with fixed switching period T_{sw}, to the circuit of Figure 3. The one-cycle control paradigm [23,24] is based on computing the control in one switching cycle, as shown in Figure 4. As a result, given an initial current through the inductance i_k and a constant current reference value to be tracked i_{rk}, the problem is to find the ON time (t_{on} or t_1 in Figure 4) that allows the performance of optimal reference tracking. Subscript z, which refers to the converter phases, is hereafter omitted for clarity.

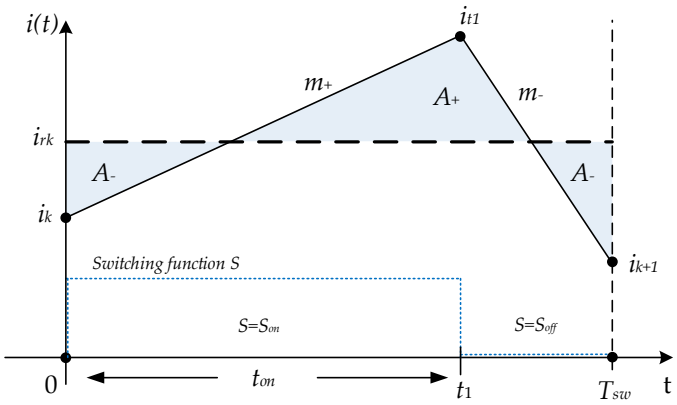


Figure 4. Time evolution of phase current $i(t)$ with respect to t_{on} in a switching period.

This work proposes a one-cycle control method that seeks to minimize the absolute value of the current error integral in a switching cycle, that is:

$$\min_{t_{on}\in[0,T_{sw}]}\left|\int_0^{T_{sw}} e(t)dt\right| \tag{1}$$

where $e(t) = i_{rk} - i(t)$. Graphically, the above optimization problem is equivalent to the minimization of the sum of the gray areas in Figure 4. The minimum value of the optimization problem is zero, which is achieved when positive areas A_+ are equal to negative areas A_-. If the optimal value is greater than zero, then it provides the optimal ON time (t_{on}*) that minimizes the integral error.

The rationale behind this figure of merit lies in the fact that when the minimum value is achieved, and V_{dc} and v_s are nearly constant for one switching cycle, the control provides, in one cycle, the same power as the one defined by the current reference. Note that, given the switching nature of the converter, it is impossible to track perfectly the reference in every instant within a switching cycle; however, the mean value of the signals over a switching cycle can be equal.

In the rest of the article, the following assumptions are considered:

1. The reference current i_{rk} is constant during the switching period.
2. For a switching cycle k, when $S = S_{on}$, the phase current $i(t)$ increases with slope m_+, defined as $m_{+,k} = \frac{\frac{V_{dc}}{2} - v_{s,k}}{L}$, which is always positive because $\frac{V_{dc}}{2}$ is always greater than v_s. On the other hand, when $S = S_{off}$, the phase current decreases with slope m_-, defined as $m_{-,k} = \frac{-\frac{V_{dc}}{2} - v_{s,k}}{L}$, which is always negative.
3. Slopes m_+ and m_- are assumed constant during the switching cycle. For high switching frequencies (in the range of kHz), v_s and V_{dc} are nearly constant for a switching period. Then, slopes m_+ and m_- can be considered constant for the entire switching cycle. The error produced by this assumption is considered and proved not significant, so it does not justify the increased complexity.

3. One-Cycle Zero-Integral-Error

The optimal ON time t_{on}* is obtained by solving the following constrained optimization problem:

$$\min_{t_1 \in [0, T_{\mathrm{sw}}]} \left| \int_0^{T_{\mathrm{sw}}} e(t)dt \right| \tag{2}$$

With the current error $e(t)$ defined as:

$$e(t) = \begin{cases} e_+(t) = i_{rk} - (i_k + m_+ t) & \text{if } 0 \le t < t_1 \\ e_-(t) = i_{rk} - (i_{t_1} + m_-(t - t_1)) & \text{if } t_1 \le t \le T_{sw} \end{cases} \tag{3}$$

i_{t_1} is the current at the switching point given by:

$$i_{t_1} = i_k + m_+ t_1 \tag{4}$$

The optimization problem (2) can be solved analytically by first computing the one-cycle integral error as:

$$\int_0^{T_{sw}} e(t)dt = \int_0^{t_1} e_+(t)dt + \int_{t_1}^{T_{sw}} e_-(t)dt \tag{5}$$

The integral of the error when the switch is ON is:

$$\int_0^{t_1} e_+(t)dt = \int_0^{t_1} \underbrace{(i_{rk} - i_k)}_{e_k} - m_+ t dt = \left(e_k - \frac{m_+}{2} t_1\right) t_1 \tag{6}$$

The integral of the error when the switch is OFF is:

$$\begin{array}{c} \int_{t_1}^{T_{sw}} e_-(t)dt = \int_{t_1}^{T_{sw}} i_{rk} - i_{t1} - m_-(t - t_1)dt \\ = \quad e_k(T_{sw} - t_1) - m_+ t_1 (T_{sw} - t_1) - \frac{m_-}{2}(T_{sw} - t_1)^2 \end{array} \tag{7}$$

Finally, adding both integrals yields the following expression:

$$\int_0^{T_{sw}} e(t)dt = \left(\frac{m_+ - m_-}{2}\right) {t_1}^2 + (m_- - m_+) t_1 T_{sw} + \left(e_k - \frac{m_-}{2} T_{sw}\right) T_{sw} \tag{8}$$

As a result, the integral of the error is a quadratic polynomial in t_1, equivalently in t_{on}, defined as, and given by:

$$p(t_{on}) = \underbrace{\left(\frac{m_+ - m_-}{2}\right)}_{a} {t_{on}}^2 + \underbrace{(m_- - m_+) T_{sw}}_{b} t_{on} + \underbrace{\left(e_k - \frac{m_-}{2} T_{sw}\right) T_{sw}}_{c} \tag{9}$$

The polynomial $p(t_{on})$ has the following properties:

1. The quadratic function is convex, because $\frac{d^2 p(t_{on})}{d {t_{on}}^2} = m_+ - m_- > 0$.
2. The minimum of the function is always at $t_{on} = T_{sw}$, because $\frac{dp(t_{on})}{dt_{on}} = 0 = (m_+ - m_-) t_{on} + (m_- - m_+) T_{sw}$ and $\frac{dp(t_{on})}{dt_{on}} = 0$ yields $t_{on} = T_{sw}$.

Note that the function to be minimized is not $p(t_{on})$, but its absolute value $\left|p(t_{on})\right|$. Its minimum (t_{on}*) can be obtained by the following procedure:

1. Compute $p(T_{sw})$. If $p(T_{sw}) \ge 0$, the optimizer is $t_{on}{}^* = T_{sw}$, and the optimal value is $p(T_{sw})$. This condition is equivalent to $e_k \ge \frac{m_+}{2} T_{sw}$.

2. Compute $p(0)$. If $p(0) \leq 0$, the optimizer is ${t_{on}}^* = 0$, and the optimal value is $\left|p(0)\right|$, because $p(t_{on})$ is convex and, with a minimum at $t_{on} = T_{sw}$, if $p(0)$ is negative, then $p(0)$ is the maximum value for $t_{on} \in [0, T_{sw}]$ and as we take the absolute value $\left|p(t_{on})\right|$, it follows that $p(0)$ is positive and the minimum value for $t_{on} \in [0, T_{sw}]$. This condition is equivalent to $e_k \leq \frac{m_-}{2} T_{sw}$.
3. Finally, if $\frac{m_-}{2} T_{sw} \leq e_k \leq \frac{m_+}{2} T_{sw}$, the optimal ${t_{on}}^*$ is obtained by the solution of $p(t_{on}) = 0$, that is given by:

$$ {t_{on}}^* = T_{sw} - \sqrt{{T_{sw}}^2 - \frac{(2e_k - m_- T_{sw}) T_{sw}}{m_+ - m_-}} \tag{10} $$

3.1. Control Algorithm

The control algorithm requires us to measure the phase current at the beginning of each switching cycle (i_k) in order to compute the current error $e_k = i_{rk} - i_k$. Depending on the value of the current error e_k, the optimal control action to be applied is:

1. If $e_k \geq \frac{m_+}{2} T_{sw}$, then ${t_{on}}^* = T_{sw}$.
2. If $e_k \leq \frac{m_-}{2} T_{sw}$, then ${t_{on}}^* = 0$.
3. If $\frac{m_-}{2} T_{sw} \leq e_k \leq \frac{m_+}{2} T_{sw}$, then

$$ {t_{on}}^* = T_{sw} - \sqrt{{T_{sw}}^2 - \frac{(2e_k - m_- T_{sw}) T_{sw}}{m_+ - m_-}} $$

The following remarks are in order:

1. The optimization problem achieves the minimum value of 0 when $\frac{m_-}{2} T_{sw} \leq e_k \leq \frac{m_+}{2} T_{sw}$. In this case, the control provides the one-cycle zero integral error.
2. In the case that $e_k \geq \frac{m_+}{2} T_{sw}$ or $e_k \leq \frac{m_-}{2} T_{sw}$, the minimum value achieved is greater than zero and the one-cycle zero integral error property is no longer achieved, although the algorithm still minimizes its value. These cases arise when the value of the error is so large that it saturates the control action (i.e., ${t_{on}}^* = T_{sw}$ or ${t_{on}}^* = 0$).
3. In general, slopes m_+ and m_- are not constant but time varying in each switching cycle. Hence, the slopes must be updated accordingly in each cycle.

3.2. Stability Analysis

Once ${t_{on}}^*$ is obtained, a stability analysis is performed. The phase current at the end of switching cycle i_{k+1} is related to the current at the beginning i_k by:

$$ i_{k+1} = i_k + m_+ t_{on} + m_-(T_{sw} - t_{on}) \tag{11} $$

Subtracting Equation (11) from the reference current in one-cycle i_{rk}, the evolution of the error is obtained as:

$$ e_{k+1} = i_{rk} - i_{k+1} = \underbrace{i_{rk} - i_k}_{e_k} - m_+ t_{on} - m_-(T_{sw} - t_{on}) = e_k - m_- T_{sw} + (m_- - m_+) t_{on} \tag{12} $$

The objective is to analyze the error evolution of Equation (12) when the optimal ON time (10) is applied. Substituting (10) into (12) and arranging terms, the following nonlinear iterated map is obtained:

$$ e_{k+1} = e_k - m_+ T_{sw} + \sqrt{(m_+ - m_-) T_{sw}} \sqrt{m_+ T_{sw} - 2e_k} \tag{13} $$

First, the fixed points of the map are computed, that is, e $= e_k = e_{k+1}$. The fixed points are given by solving:

$$-m_+T_{sw} + \sqrt{(m_+ - m_-)T_{sw}}\sqrt{m_+T_{sw} - 2e} = 0 \tag{14}$$

The unique solution is:

$$e = -\frac{T_{sw}}{2}\frac{m_+m_-}{(m_+ - m_-)} \tag{15}$$

The next step is to determine the stability of the fixed point. For unidimensional iterated maps $x_{k+1} = f(x_k)$, the fixed point x is stable if $\left|\frac{df(x_x)}{dx_k}|_{x_k=x}\right| < 1$. Particularizing the stability result to Equation (14):

$$\begin{aligned}\frac{de_{k+1}}{de_k} &= 1 + \sqrt{(m_+ - m_-)T_{sw}}\left(\tfrac{1}{2}\right)(m_+T_{sw} - 2e_k)^{-1/2}(-2) \\ &= 1 - \sqrt{(m_+ - m_-)T_{sw}}(m_+T_{sw} - 2e_k)^{-1/2} = 1 - \sqrt{\frac{(m_+ - m_-)T_{sw}}{(m_+T_{sw} - 2e_k)}}\end{aligned} \tag{16}$$

Particularizing the derivative Equation (16) with the fixed point e given in (15):

$$\frac{de_{k+1}}{de_k} = 1 - \frac{m_+ - m_-}{m_+} = 1 - \left(1 - \frac{m_-}{m_+}\right) = \frac{m_-}{m_+} \tag{17}$$

Finally, the system is stable if:

$$\left|\frac{m_-}{m_+}\right| < 1 \tag{18}$$

Considering the equivalent circuit in Figure 3, the stability condition (18) leads to an unstable behavior of the controller during the positive half-cycle of the supply voltages, where m_- is greater than m_+. Stability properties considering the switching pattern are analyzed and a stable controller for a complete voltage cycle is derived in Section 4.

4. Stability and Switching Pattern

Consider the evolution of the phase current with the switching pattern shown in Figure 5. In this case, the switching period starts in the OFF state and turns on at time t_1, remaining in the ON state until the end of the switching period.

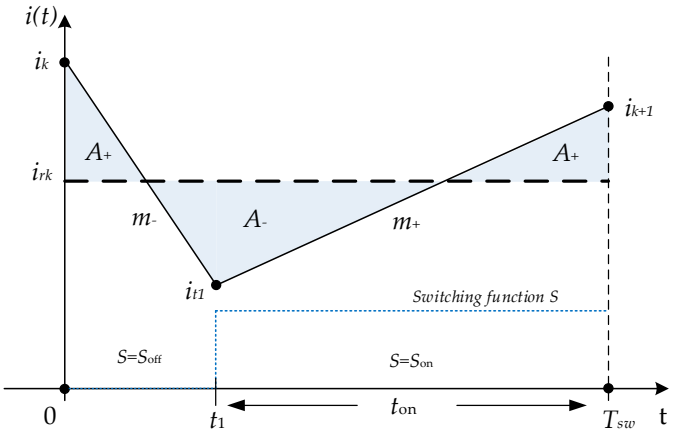


Figure 5. Time evolution of current $i(t)$ with respect to t_{on}.

Using this switching pattern, and following an analog procedure, i.e., the one in Section 3, the one-cycle integral defines again a quadratic polynomial in $t_{on} = T_{sw} - t_1$, given by

$$p(t_{on}) = -\underbrace{\left(\frac{m_+ - m_-}{2}\right)}_{a} {t_{on}}^2 + \underbrace{\left(e_k - \frac{m_-}{2}T_{sw}\right)}_{c} T_{sw} \tag{19}$$

The polynomial $p(t_{on})$ has the following properties:

1. The quadratic function is concave, because $\frac{d^2 p(t_{on})}{{dt_{on}}^2} = -(m_+ - m_-) < 0$.
2. The minimum of the function is always at $t_{on} = 0$, because $\frac{dp(t_{on})}{dt_{on}} = -(m_+ - m_{m-})t_{on}$ and $\frac{dp(t_{on})}{dt_{on}} = 0$ yields $t_{on} = 0$.

In an analogous manner to the previous section, the minimum of $\left|p(t_{on})\right|$ can be obtained by the following procedure:

1. Compute $p(0)$. If $p(0) \leq 0$, the optimizer is ${t_{on}}^* = 0$, and the optimal value is $\left|p(0)\right|$. This condition is equivalent to $e_k \leq \frac{m_-}{2}T_{sw}$.
2. Compute $p(T_{sw})$. If $p(T_{sw}) \geq 0$, the optimizer is ${t_{on}}^* = T_{sw}$, and the optimal value is $p(T_{sw})$. This condition is equivalent to $e_k \geq \frac{m_+}{2}T_{sw}$.
3. Finally, if $\frac{m_-}{2}T_{sw} \leq e_k \leq \frac{m_+}{2}T_{sw}$, the optimal ON time is obtained by solving $p(t_{on}) = 0$, that is given by:

$${t_{on}}^* = \sqrt{\frac{(2e_k - m_- T_{sw})T_{sw}}{m_+ - m_-}} \tag{20}$$

The stability analysis for the optimal ${t_{on}}^*$ obtained with the new switching pattern is repeated. The resulting nonlinear map of the current error is, in this case:

$$e_{k+1} = e_k - m_- T_{sw} + \sqrt{(m_+ - m_-)T_{sw}}\ \sqrt{m_+ T_{sw} - 2e_k} \tag{21}$$

The fixed point is given by:

$$e = \frac{T_{sw}}{2}\frac{m_+ m_-}{(m_+ - m_-)} \tag{22}$$

As can be seen, the fixed point is equal in magnitude, but with opposite sign to the one previously computed in (15). Finally, the stability condition is shown to be:

$$\left|\frac{m_+}{m_-}\right| < 1 \tag{23}$$

That is complementary to stability condition (18) computed in Section 3 with the switching pattern of Figure 4. Summing up, the use of two distinct switching patterns (one for each half-cycle of the voltages) renders the one-cycle zero-integral-error current control stable.

Control Algorithm

This subsection summarizes the one-cycle zero-integral-error control algorithm. The control algorithm requires us to measure the phase current at the beginning of each cycle (i_k) in order to compute the current error $e_k = i_{rk} - i_k$. Furthermore, the algorithm also requires computing the slopes m_+ and m_- that, in general, are time varying at each switching cycle. The slopes are necessary to choose the stable switching pattern and to compute the optimal ON time. Hence, the slopes must be updated each cycle. The control algorithm is resumed in the flowchart of Figure 6.

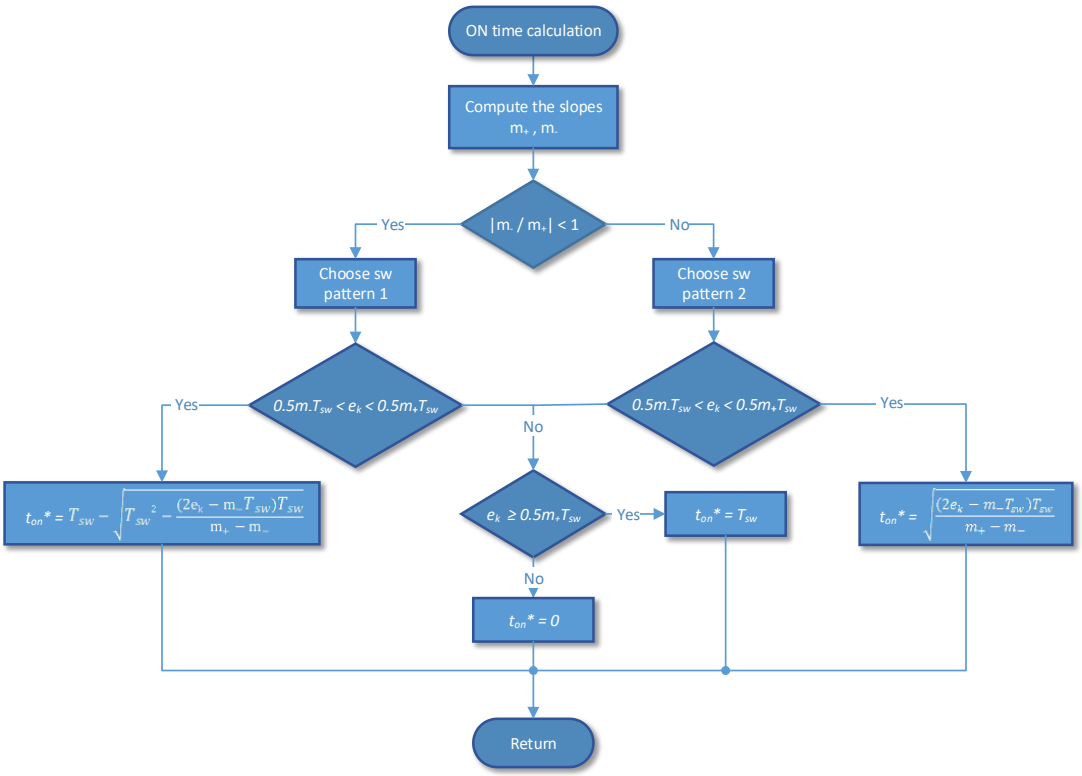


Figure 6. Flowchart of the digital control algorithm.

5. Simulation Results

Consider the power system presented in Figure 7. A three-phase four-wire SAPF is used to achieve balanced currents, low current total harmonic distortion (THD) and unity power factor (PF) upstream from the pcc, where a linear load and a nonlinear load are connected.

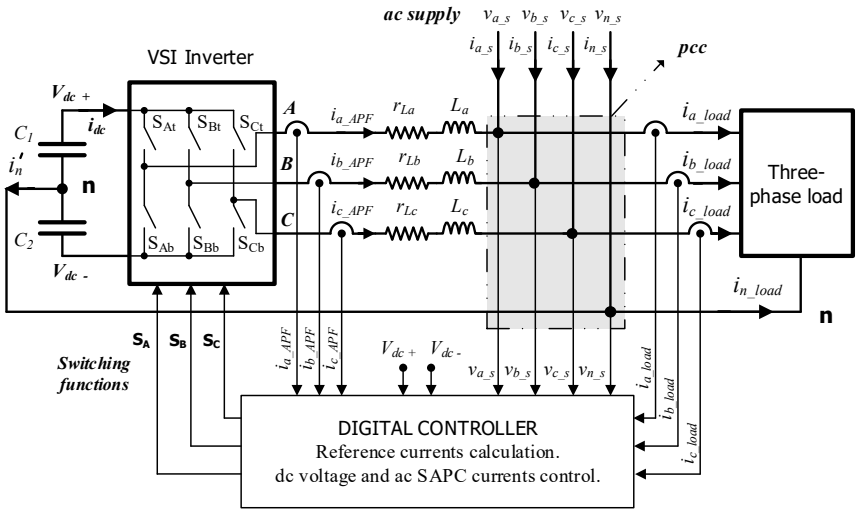


Figure 7. Block diagram of the power system under consideration.

The values used in the circuit Figure 7 are: $L_a = L_b = L_c = 3$ mH; $r_{La} = r_{Lb} = r_{Lc} = 0.1\ \Omega$; $C_1 = C_2 = 4.7$ mF. The dc bus voltage is $V_{dc} = 450$ V. Supply voltages (v_{a_s}, v_{b_s} and v_{c_s}) are symmetrical with rms values equal to $V_{a\_s} = V_{b\_s} = V_{c\_s} = 120$ V. Fundamental frequency is 50 Hz. SAPF switching frequency is 20 kHz. The nonlinear load uses a diode-based three-phase rectifier feeding a series R-L

load. An unbalanced three-phase linear load is also connected at the pcc. Load values are presented in Table 1.

Table 1. Load values.

Linear load		
Z_a	Z_b	Z_c
$R_a = 24\ \Omega$ $L_a = 18$ mH	$R_b = 50\ \Omega$ $L_b = 6$ mH	$R_c = 350\ \Omega$ $L_c = 12$ mH
Nonlinear load *Three-phase Rectifier + R-L Load*		
$L_r = 6$ mH	$R_r = 37\ \Omega$	

Current slopes for each phase are given by: $m_{+z} = \frac{\frac{V_{dc}}{2} - V_{z\_s}\sin(wt+\varphi_z)}{L}$; $m_{-z} = \frac{-\frac{V_{dc}}{2} - V_{z\_s}\sin(wt+\varphi_z)}{L}$. where z = a, b, c and φ_z are the corresponding phase-shifts $\varphi_a = 0$, $\varphi_b = \frac{-2\pi}{3}$, $\varphi_c = \frac{-4\pi}{3}$.

The power system has been simulated with Matlab/Simulink®. Figure 8 shows the load currents, while the active filter reference currents are presented in Figure 9. By generating these currents, the SAPF achieves global compensation, meaning that reactive, unbalanced and distortion powers are reduced to near-zero values.

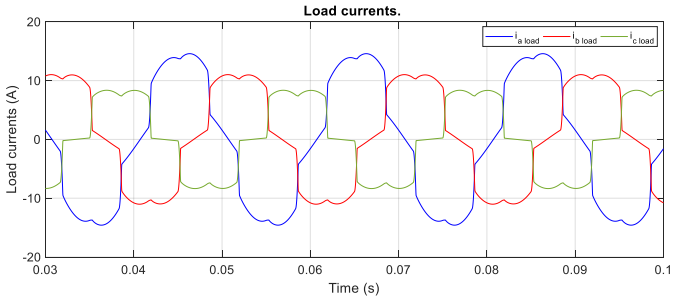


Figure 8. Load current waveforms.

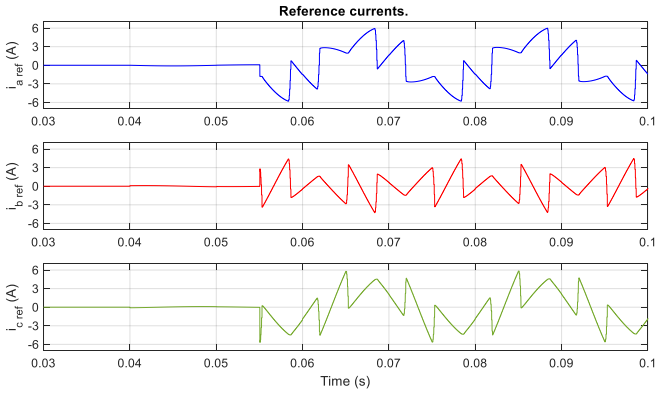


Figure 9. SAPF reference currents.

Figure 10 presents the current tracking performance of the controller proposed in Section 4, while two details of this figure are presented in Figures 11 and 12. The quality of the proposed control is demonstrated by the precise current tracking achieved. Note that a small current surge appears when a zero-crossing of the phase voltages occurs, exactly when the control changes the switching pattern. It appears because two consecutive high or low states are concatenated in the change of pattern. It also causes a small transient that stabilizes in several µs, as can be seen in Figure 12. In order

to reduce these surges, it is possible to modify the control algorithm to force the ON or OFF time to be small for the first switching period of the new pattern.

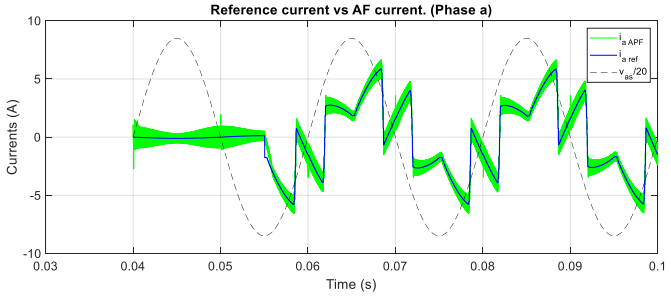


Figure 10. Current tracking performance for phase *a*.

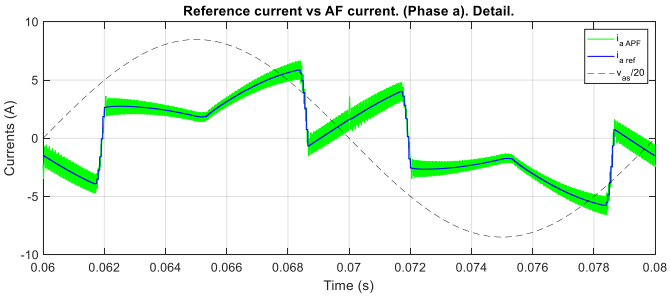


Figure 11. Current tracking performance for phase *a*. Detail 1 (0.06 s < t < 0.08 s).

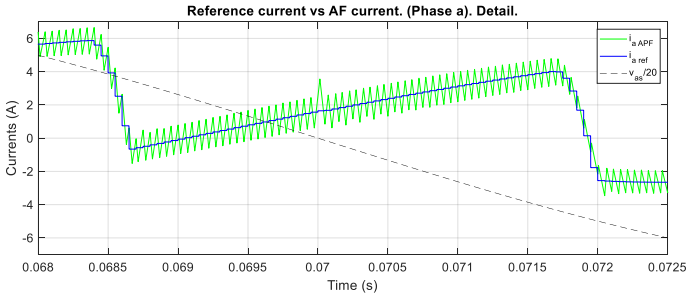


Figure 12. Current tracking performance for phase *a*. Detail 2 (0.068 s < t < 0.0725 s).

Figure 13 shows the current tracking error corresponding to the detail of Figure 12. Figure 14 shows the supply currents before and during the SAPF operation ($t > 0.055$ s). The current waveforms become a set of balanced, sinusoidal currents, showing a THD of 1.83% and a PF equal to 0.9987. The error observed in the tracking of high reference derivatives can be reduced by increasing the switching frequency. However, for the one-cycle control technique, it means increasing control frequency and reducing computing time, as well as increasing the switching losses.

Finally, Figure 15 presents the harmonic spectrum of supply currents obtained during compensation. Low-order harmonic components are small compared to the fundamental component, as indicated by the resulting THD value. Higher harmonics are concentrated around the switching frequency (order 400 for 20 kHz).

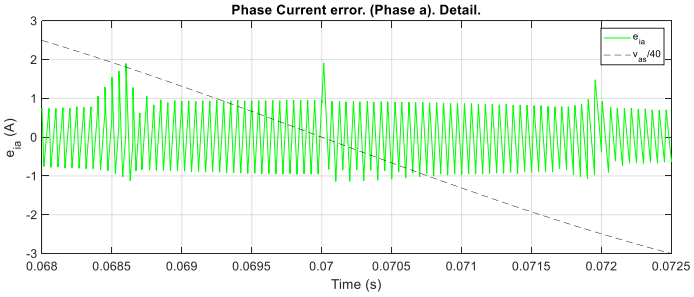


Figure 13. Current tracking error during detail 2 time interval.

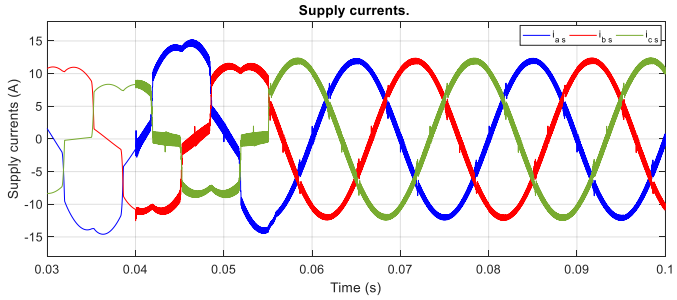


Figure 14. Supply currents before and during SAPF compensation.

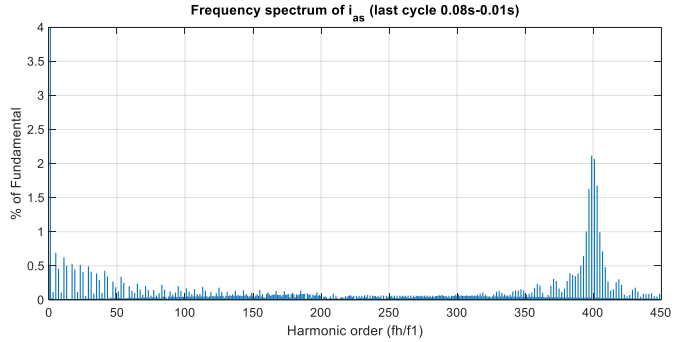


Figure 15. Supply current harmonic components during SAPF compensation.

6. Experimental Results

Figure 16 shows the prototype implemented in the lab to perform the experimental tests. SAPF has been implemented by means of a Toshiba PM75CG1B120 (75 A, 1200 V) three-phase power stage switching at 20 kHz. The scheme of the power system matches the one shown in Figure 7. SAPF component values (dc bus capacitors and phase inductances) as well as the load components are the same as those presented for the simulation example in Section 5. A Pacific Power A-360MX three-phase power supply generates the 120 V rms three-phase supply voltages. A dc bus voltage controller assures $V_{dc} = 450$ V and a capacitor voltage-balancing controller keeps the voltage equally distributed between the capacitors [2]. A LeCroy waveJet 324 oscilloscope (200 MHz-2 GS/s) is used to carry all measurements and to obtain the voltage and current figures presented in this section.

The proposed one-cycle control requires high-speed computing, because it has to calculate the reference currents and the ON times of the next switching period in a few microseconds. To obtain good current tracking, it also needs accurate measurements of load and SAPF phase currents at the beginning of the switching period, as shown in Figures 4 and 5. Dc bus and supply voltage measurements are not so time-critical because they change slowly compared with the switching period. However, to wait until the end of the cycle means overlapping part of the next switching period with the calculations

needed to compute its corresponding ON time. This is a problem because no action is possible until the computations are finished.

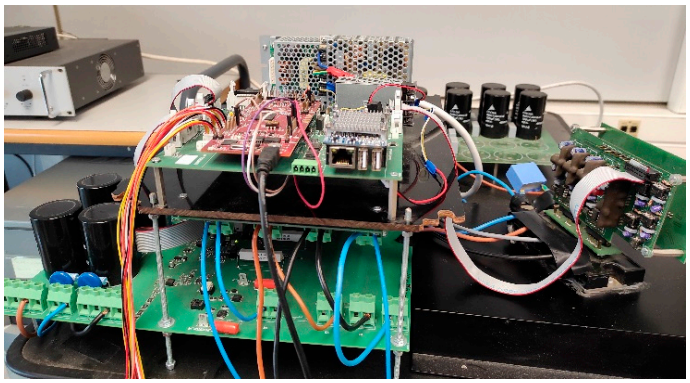
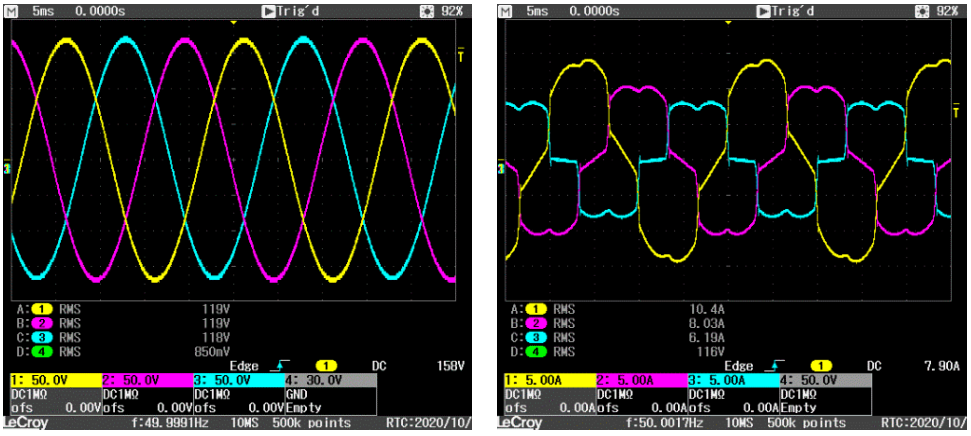


Figure 16. Experimental setup.

To avoid this problem, SAPF currents and load currents are measured using six AMC1303E2520 sigma-delta modulators that feature 20 mega samples per second (MSPS), an internal clock and Manchester modulation. Using these sigma-delta modulators, 40 high-precision samples per switching cycle (at 800 kSPS) are obtained, allowing us to precompute the slope of each one of the six currents and their values at the end of the switching period, whilst avoiding possible mismeasurements due to semiconductor switching. This forward calculation allows for computing the next ON time, avoiding the need to wait until the end of the switching period to sample the currents and compute the ON times. It is also important to remark that, due to the switching times of the semiconductors in the power stage, a dead-band is needed. Considering this restriction, minimum and maximum values for t_{on} could be limited to 5% and 95% of the switching period, respectively. This characteristic also conditions the dc voltage level needed to track reference currents, which must be slightly higher, consequently increasing the current ripple of phase currents.

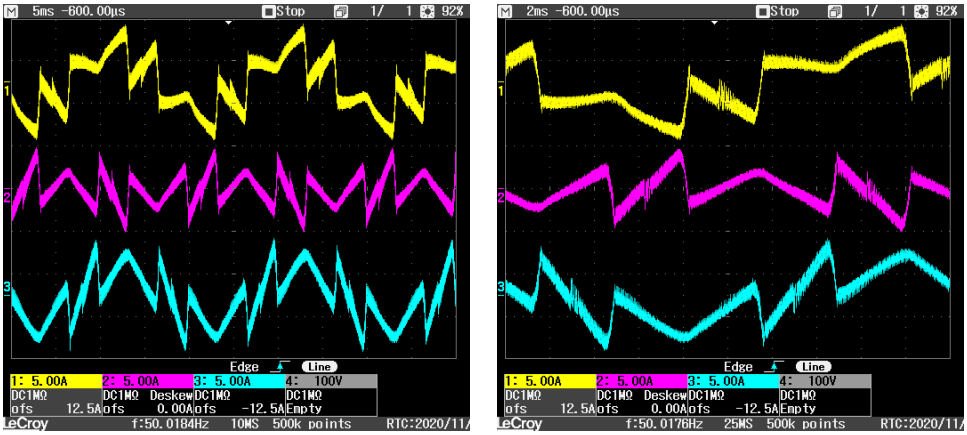
In order to carry out these high-speed tasks, a Texas Instruments dual core TMS320F28379D microcontroller has been selected. This digital controller features up to 800 MIPS (200 MHz), and includes two programmable control law accelerators (CLAs), an IEEE 754 floating-point unit (FPU), a trigonometric math unit (TMU), eight sigma-delta filter module (SDFM) input channels and many other peripherals. Combining the powerful microcontroller and the sigma-delta modulators, the proposed control has been implemented and the experimental results are shown in the next figures.

Figure 17a shows the supply voltages, a set of three-phase balanced voltages of 120 V rms. The load currents are shown in Figure 17b and correspond to the mixed load presented in Table 1. The currents delivered by the SAPF to achieve global compensation are presented in Figure 18a and details of SAPF phase currents are presented in Figures 18b and 19. These detailed waveforms show the good shape of the currents, in both positive and negative half-cycles. As expected, a small surge and a short instability appear at zero-crossings of the supply voltages, when the control changes the switching pattern. The excellent performance of the current tracking is validated by the good supply current waveforms obtained during the compensation. Figure 20 shows how supply currents become a set of balanced sinusoidal currents. The small surges in the waveforms have two causes. As mentioned before, there are surges caused by the change of switching pattern at zero-crossings of voltages, and second, there are surges due to the normal error produced in tracking the sudden slope changes in the reference currents. The supply current THD is 2.8% and PF reaches a value of 0.997. A slight increment in the current THD value compared with the one obtained in the simulation can be appreciated. This is caused by the real characteristics of the semiconductors and tolerances of the passive components used in the experimental setup.



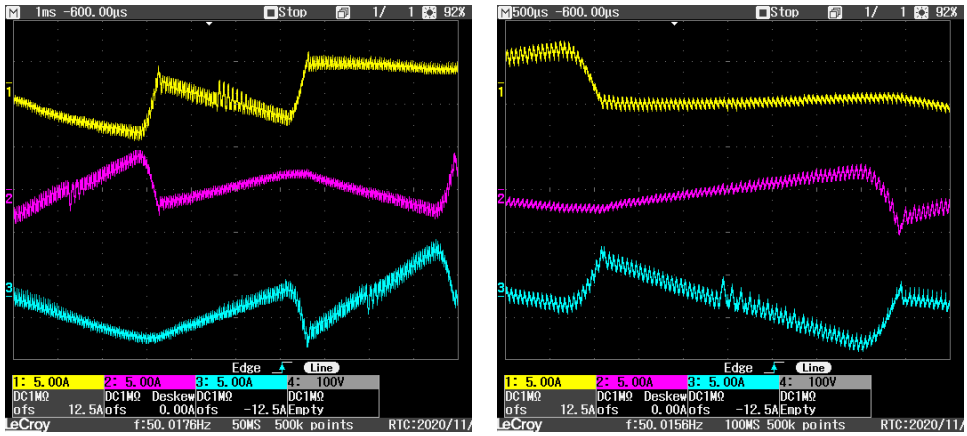
(**a**) (**b**)

Figure 17. Supply voltages (**a**) and load current waveforms (**b**).



(**a**) (**b**)

Figure 18. SAPF phase current waveforms (**a**) and a detail at 2 ms/div (**b**).



(**a**) (**b**)

Figure 19. Details of SAPF phase current waveforms at 1 ms/div (**a**) and 500 µs/div (**b**).

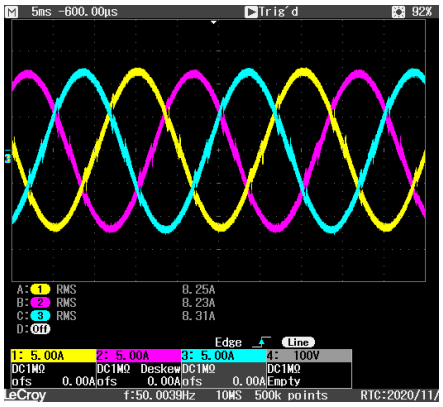


Figure 20. Supply currents during SAPF compensation.

7. Conclusions

In this work, a one-cycle digital current controller has been proposed. Based on the minimization of the current integral error, the optimal ON time is obtained for every switching period. Two switching patterns have been studied and stability analysis demonstrates that both patterns are complementary and stable for one half-cycle of the supply voltages. After this conclusion, a current controller combining the two switching patterns were proposed. Simulated and experimental methods were carried out over a shunt active power filter platform, demonstrating the quality of the proposed controller that performs current tracking well, achieving low THD and high PF. A powerful microcontroller combined with sigma-delta-based measurements was used to implement the demanding control system.

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