APPENDIX A
Tools used and relationship between the studied masters degree to this work

A.1 Tools used

As for the tools used, we used many standard hardware implementation and verification tools, as well as scripting languages and simulation frameworks.

A.1.1. Xilinx Vivado

For synthetising the Selene SoC design we used Vivado on its CLI (Command Line Interface) mode.

With this mode of Vivado there was no need to use the graphical user interface and thus, efficient scripts could be written. The whole syntetization process is based on "GNU make" and Vivado TCL scripts.

In order to use our target VCU118 board, the usage of Vivado to synthetize the bitstream to be uploaded is mandatory as there is no other tool that can syntetize bitstreams for Xilinx FPGA boards.

We also extensively used the Vivado library and IP-core suite to implement our memory controller and some core functionality of our SoC, such as the accelerators, created with Vivado HLS and ported into our design with Vivado.

A.1.2. Mentor Graphics Questasim

For simulating the Selene SoC and our proposed implementations we used the Questasim simulator. This simulator offers great tools for debugging by offering step by step debugging for Verilog processes and mixed SV (System verilog) and VHDL simulation.

We extensively used the memory snooping capabilities, the waveform tool and the breakpoints tool. The majority of complex mechanisms that we implemented on the SELENE SoC where designed using the Questasim to debug and verify.

We extensively used the Questasim IDE to edit and debug our code, and the Questasim waveform tool debug it and ensure the system has the expected behaviour. We also made use of the TCL scripting language inside the Questasim tool to ease the debugging process.

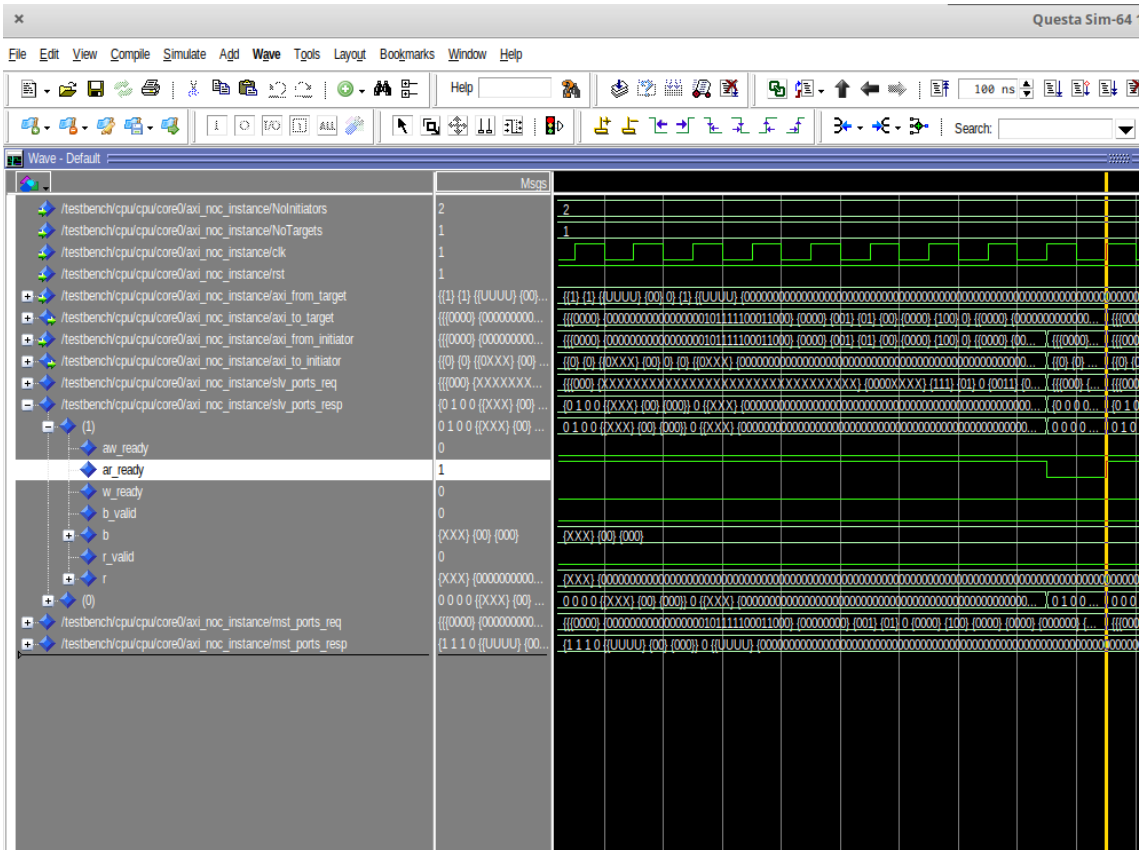

Figure A.1: Questasim waveform screenshot

A.1.3. GNU Make

> Make gets its knowledge of how to build your program from a file called the makefile, which lists each of the non-source files and how to compute it from other files. When you write a program, you should write a makefile for it, so that it is possible to use Make to build and install the program.[25]

The GNU Make tool is an indispensable tool to automate compilation workloads inside a big project such as the SELENE H2020 Project. We extensively used the Make tool to create a tree of make targets, integrating our VCU118 specific workflow with the existing generic Gaisler GRLIB make hierarchy.

A.1.4. Shell scripting, GRMON scripting and Python scripting

For the obtention and parsing of the majority of results of this work we used a combination of C software programs running on the SELENE SoC and shell scripts used to interface with GRMON and obtain the results of the programs running on the FPGA.

This project uses a wide variety of bash scripts, shell scripts, GRMON scripts and python scripts to obtain the results on a CSV (Comma separated value) manner. This csv files are necessary to easily import the results into Microsoft Excel and Google Sheets, the two graphing programs used on this work to obtain the presented graphs.

We used Python to further parse the results of reading the PMU memory addresses with GRMON, converting from hexadecimal to decimal the values and assigning the overflow bit correctly to each of the read results.

A.2 Relation between the studied maters degree and this work

There is a strong relation between the studied masters degree and this work. This masters degree is the computer architecture and networking masters degree. In this masters degree there is a strong focus on interconnection networks and computer architecture, specially at the microprocessor level.

The strong focus on interconnection networks of this master made it much easier to understand the concepts used on this work and the structure of the AMBA AHB standard. The REC (Redes en chip) *on chip networks* subject was specially relevant for this work, as we had a seminar directly orientated to the AMBA AHB standard.

This masters degree also focuses on designing small paper-like works with latex, giving us the tools and expertise to easily create this TFM on latex already knowing how to use this PDF creation language.

Finally, the studied masters degree also puts a strong emphasis on chip design and internal chip structure with its ATP subject. Where I understood the internal architecture of a complex processor and the importance of the memory subsystem, as well as the indeterminism that this memory subsystem can produce. This understanding of computer processors was also used on this work to better understand the traffic needs of the Selene NOEL-V cores.