UNIVERSITAT POLITÈCNICA DE VALÈNCIA

UNIVERSITAT POLITÈCNICA DE VALÈNCIA

Escuela Técnica Superior de Ingeniería Industrial

RESEARCH OF THREE PHASE INVERTERS

Trabajo Fin de Máster

Máster Universitario en Ingeniería Industria

AUTOR/A: Guillem Carrillo, Sergio

TUTOR/A: Trujillo Ruiz, Francisco de Borja

CURSO ACADÉMICO: 2022/2023

VILNIUS GEDIMINAS TECHNICAL UNIVERSITY

FACULTY OF ELECTRONICS

DEPARTMENT OF ELECTRONICS

DESIGN AND ESEARCH OF THREE-PHASE HIGH-POWER INVERTER

Master‘s degree Thesis

Sergio Guillem Carrillo

Dr Gediminas Staigvila

VILNIUS 2023

VILNIUS GEDIMINAS TECHNICAL UNIVERSITY

FACULTY OF ELECTRONICS

DEPARTMENT OF ELECTRONICS

SERGIO GUILLEM

Design and research of Three-phase high-power inverter

Master‘s degree Thesis

Electrical Energetics Systems Engineering 2023, 6211EX049

Generation of energy

Electrical Engineering

Supervisor dr Gediminas Staigvila

Vilnius, 2023

Annotations (in Lithuanian and in English) must be printed from mano.vgtu.lt . Also, one copy of the annotations (in Lithuanian and in English) must be presented to the department.

Vilnius Gediminas Technical University

Electronics Faculty

Electrical Engineering Department

ISBN ISSN

Copies No. 2

Date ….-….-….

Electrical engineering engineering / Automatics study program master's thesis

Title**: Design and research of Three-phase high-power inverter**

Author **Sergio Guillem** Academic supervisor **Prof. Dr Gediminas Staigvila**

Thesis language

[ ] Lithuanian

[X] Foreign (English)

Annotation

The final master's thesis deals with the study os the three-phase inverters and their importance in today‘s electrical market, being crucial into the development of renewable energies and the energy transition. Diferrent types of inverters and their modulation techiques are explained. Circuits of these inverters and their modulation techniques are provided and analyzed. Having analyzed theoretical and practical aspects, the conclusions and suggestions of the final thesis are presented

Structure: introduction, Descrptive part, Practical part, conclusions and references.

Thesis consist of: 95 p. text without appendixes, 89 pictures, 10 tables, 33 bibliographical entries.

Keywords: VSI, PWM, three-phase inverters, filter, waveform, sinusoida, load, voltage, current.

VILNIUS GEDIMINAS TECHNICAL UNIVERSITY
FACULTY OF ELECTRONICS
DEPARTMENT OF ELECTRONICS

Electrical engineering

Electrical Energetics Systems Engineering 2023, 6211EX049

Generation of energy

OBJECTIVES FOR MASTER THESIS

Vilnius

For student Sergio Guillem

Master Thesis title: Design and research of Three-phase high-power inverter

The Final work has to be completed by xxxx, 2023

THE OBJECTIVES:

Research about the different types of inverters and modulation techniques. Study the different components to improve the quality of the work of the inverters. Create, design and analyse different circuis and how they work through different changes.

Consultants of the Master Thesis: None
Academic Supervisor: Dr Gediminas Staigvila

Objectives accepted as a quidance for my Master Thesis

……..
(Student‘s Name, Surname)

……..…....
(Date)

TABLE OF CONTENTS

INDEX

LIST OF FIGURES

LIST OF TABLES

INTRODUCTION

Relevance of the topic. In the field of the power electronics the Voltage Source Inverters (VSI) play a key role in a variety of applications, specially three-phase inverters, from generation systems to electric motor control. The main objective of static power converters is to produce an ac output waveform from a dc power supply. The basic operation of a three-phase inverter is based on the principle of switching semiconductor devices, such as power transistors, to control the direction and amplitude of the current in each phase. This is achieved through different modulations, which will be explained and discussed in this paper, including circuits to show how they work. The most important one is PWM which consists of varying the duration of the current pulses as a function of a reference signal.

A fundamental aspect in the design of a three-phase inverter is the generation of the PWM modulation signal. There are different modulation techniques, such as Space Vector Pulse Width Modulation (SVPWM) and Triangle Carrier Modulation (PWM). These techniques allow to control the output amplitude and frequency of the alternating current generated by the inverter.

Three-phase inverters find applications in various sectors, such as the generation and distribution of electric power, renewable energy systems, electric motor drive, electric vehicle traction systems, among others. In power generation systems, three-phase inverters are used to convert power generated by renewable sources, such as solar panels or wind turbines, into alternating current synchronized with the electrical grid. Due to the green transition accelerated in the last years and specially with the war in Russia, three-phase inverters are becoming more important, and they will play an even more important role in the future as solar energy is becoming one of the most promising and installed renewable energy.

One of the most prominent benefits of three-phase inverters is their ability to supply higher power compared to single-phase inverters. In addition, the three-phase connection allows a better balance of the load and a greater efficiency in the transmission of energy. This makes them an ideal choice in applications that require high power levels, such as heavy industry.

The design and control of three-phase inverters have also benefited from advances in power electronics and high-power semiconductor devices. The use of technologies such as IGBTs (insulated gate transistors with high voltage and high current blocking capacity) has allowed improving the efficiency and reliability of inverters, as well as reducing their size and associated costs.

In summary, three-phase inverters are fundamental devices in the field of power electronics, allowing the conversion of direct current into three-phase alternating current. Their

ability to supply power to three-phase loads efficiently and reliably makes them indispensable in various applications.

Research object – High power three-phase inverters.

Aim – The aim of the works is to study and the importance of three-phase inverters in the grid system and to analyse how their beahaviour through practical work.

Tasks:

1. Study the different types of inverters and their different uses.
2. Study the most important modulation techniques and explain how they work.
3. Investigate the elements that can be added to the imnverters to improve their operation.
4. Create different circuits changing some elements and parameters to analyze its behaviour.

Research Methods. Electrical books, scientific papers and softwares to create electrical circuits.

1. DESCRIPTIVE PART

1.1. Voltage Source Inverters

Voltage source inverters (VSI's) basically convert DC voltage into AC voltage. The shape of the ideal VSI output voltage waveform should be independent of the load connected to the inverter, they are extensively necessitated for the commercial purpose as well as for the industrial applications these include adjustable speed drives (ASD), uninterruptable power supplies (UPS), active filters, Flexible AC transmission systems (FACTS), voltage compensators, and photovoltaic generators (S. Kharjule, 2015). Voltage source inverters can be used practically in both single-phase and three-phase applications.

To work as a switches VSI's are composed with semiconductor devices. These devices tend to approximate ideal switches, but they differ in some aspects:

- Limits on the amount and direction of on-state current.
- a nonzero on-state voltage drops (such as a diode forward voltage).
- some levels of leakage current when the device is supposed to be off.
- limitations on the voltage that can be applied when off.
- Operating speed. The transition between on-state and off-state, this is one of the key aspects of the different semiconductor devices.

Many different types of semiconductors have been applied in VSI's. In general, these fall into two groups:

- Diodes, widely used in rectifiers and in supporting roles.
- Transistors, suitable for control of single-polarity circuits, in this work we will focus in IGBT and MOSFET.

1.1.1. Diodes

Among all the static switching devices used in power electronics, the power diode is perhaps the simplest.

It is a two-terminal device, and terminal *A* is known as the anode whereas terminal *K* is known as the cathode. If terminal *A* experiences a higher potential compared to terminal *K*, the device is said to be forward biased, and a current called forward current (I_f) will flow through the device in the direction as shown. This causes a small voltage drop across the device (<1V), which in ideal condition is usually ignored. On the contrary, when a diode is reverse biased, it does not conduct and a practical diode do experience a small current flowing in the reverse

direction called the leakage current. Both the forward voltage drop and the leakage current are ignored in an ideal diode. Usually in power electronics applications a diode is an ideal static switch (Rashid, 2017).

Current ratings from under 1 A to more than 5000 A. Voltage ratings from 10V to 10 kV or more. The fastest power devices switch in less than 10 ns, whereas the slowest require 100μs or more.

Figure 1. Diode quadrant.

Current ratings from under 1 A to more than 5000 A. Voltage ratings from 10V to 10 kV or more. The fastest power devices switch in less than 10 ns, whereas the slowest require 100μs or more.

Among all the static switching devices used in power electronics, the power diode is perhaps the simplest.

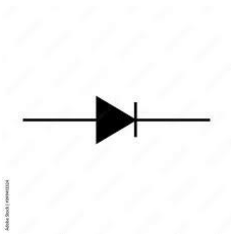

Figure 2. Device symbol. Carries in one direction, blocks in the other.

1.1.2. Transistors

Initially the DC to AC conversion is carried out by using the transistors. The basic circuit of the DC to AC conversion consist of two transistors. One is pnp transistor and the other is npn transistor.

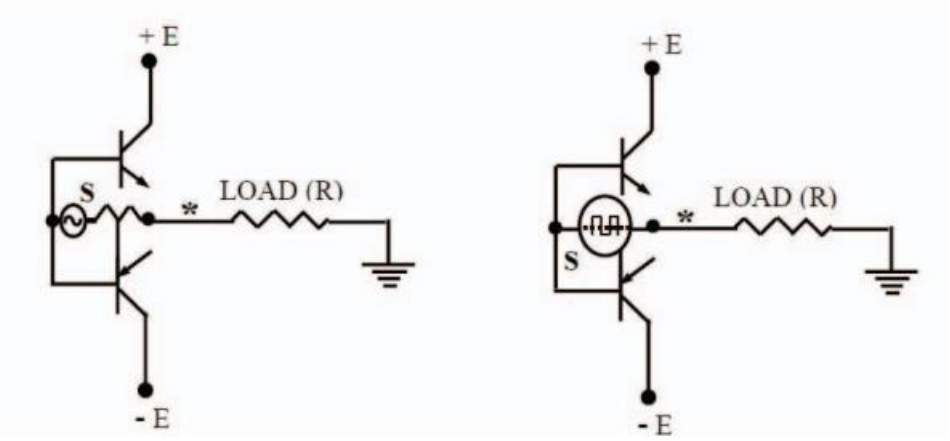

Figure 3. Transistorized VSI

As shown in the Fig. 3 the transistors are connected in push-pull manner and operates in common emitter configuration. The base and emitter of both the transistors are shorted. Collector of npn transistor is connected to positive DC supply (E+), and collector of the pnp transistor is connected to the negative DC supply (E-). The resistive load is connected between the emitter shortening point and the power supply ground. For the positive voltage the npn transistor conducts and we get the positive pulse at the output and for the negative supply voltage pnp transistor conducts and we get the negative pulse at the output voltage.

There exist different types of transistors and depending on the characteristics of the circuit and the application of the VSI they are used. The most important are IGBT and MOSFET.

1.1.3. IGBT

IGBT comprises a repetitive array of millions of cells arranged, in a topological layout, providing a large aspect ratio: with versus length (W/L). Fig. 4 shows a three-dimension image of the transistor.

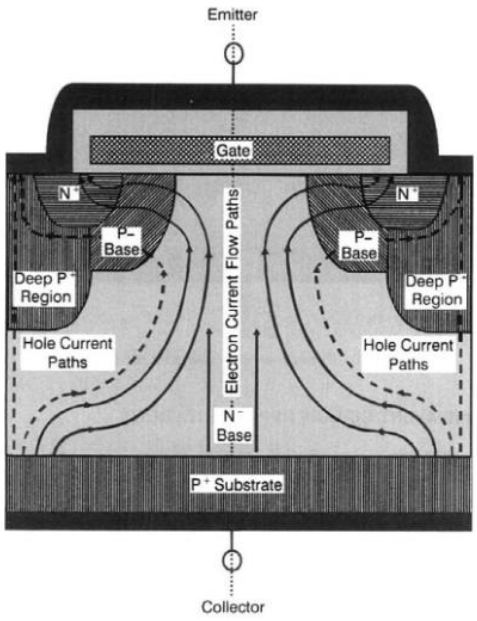

Figure 4. IGBT unit cell.

IGBT devices have the following characteristics (Khanna & kumar, 2004):

- Two-carrier device.
- Operates by minority carrier diffusion.
- Current driven.
- Collector current α emitter length and area.
- Higher breakdown voltage requires lightly doped collector region.
- Current density for given voltage drop is medium and severe trade-off exists with switching speed.
- Positive temperature coefficient of collector current.
- Charge stored in based and collector.
- Low input impedance.
- Devices cannot be easily paralleled.
- Lower switching speed tan MOSFETs.
- Ratings from 10 A to more than 600 A, with voltages of 600 to 2500V.
- The IGBT is popular in inverters from about 1 to 200kW or more. It is found almost exclusively in power electronics applications.

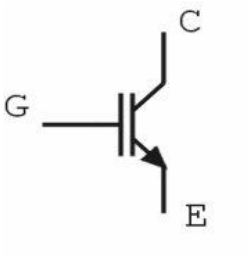

Figure 5. Device symbol

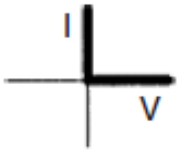

Figure 6. Quadrant operation. Carries or blocks current in one direction.

1.1.4. MOSFET

MOSFET is the fastest power switching device with a high switching frequency, up to 1MHz. Unlike other types of MOSFET power MOSFET use vertical channel structure in order to increase the device power rating (USA Department of Energy, 2009). In the vertical channel structure, the source and drain are in opposite side of the silicon waver. Figure 7 shows vertical cross-sectional view for a power MOSFET.

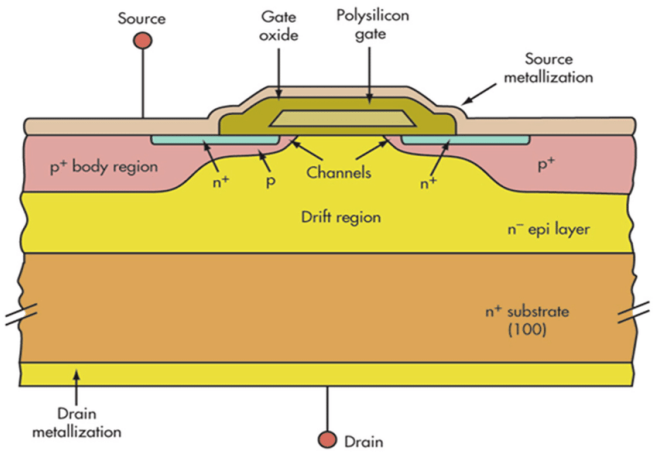

Figure 7. Vertical cross-sectional view for a power MOSFET

The P–N junction between p-base (also referred to as body or bulk region) and the n-drift region provide the forward voltage blocking capabilities. The source metal contact is connected directly to the p-base region through a break in the n+ source region in order to allow for a fixed potential to p-base region during the normal device operation. When the gate and source terminal are set the same potential ($V_{GS} = 0$), no channel is established in the p-base region. The lower doping in the n-drift region is needed in order to achieve higher drain voltage blocking capabilities. For the drain–source current, i_D , to flow, a conductive path must be established between the n+ and n−regions through the p-base diffusion region.

MOSFET devices have the following characteristics:

- Single-carrier devices.
- Voltage driven.
- Less drive power needed than IGBT.
- Higher breakdown is achieved using lightly doped drain region.
- Current density is high at low voltages and low at high voltages.
- Negative temperature coefficient of drain current.
- No charge store.
- High input impedance.
- More linear operation and less harmonics.
- Sharing current in parallel devices is possible.

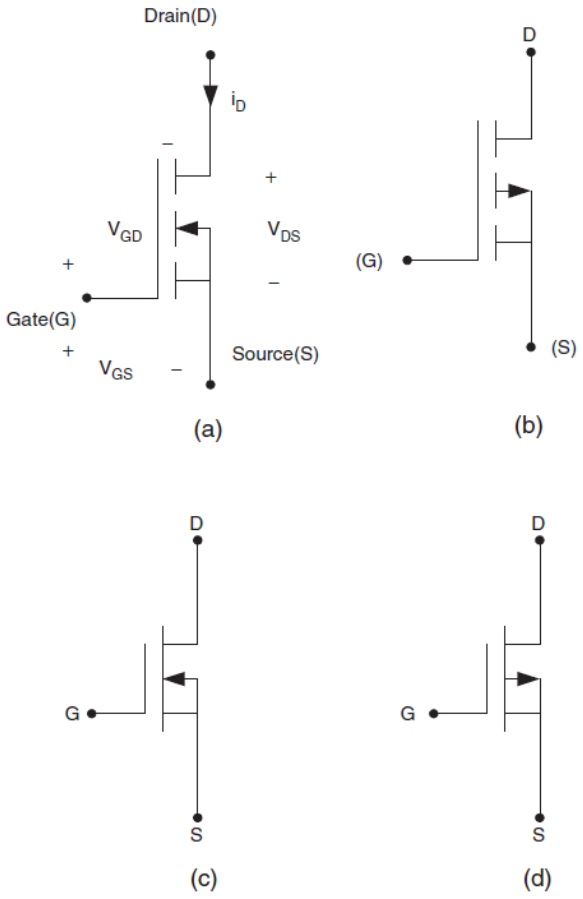

Figure 8. Device symbols: (a) n-channel enhancement-mode; (b) p-channel enhancement-mode; (c) n-channel depletion-mode; and (d) p-channel depletion-mode

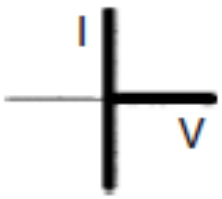

Figure 9. MOSFET quadrant operation. Carries in one direction or blocks in both directions.

1.2. Single-phase Voltage Source Inverters

Single-Phase VSI can be found as half-bridge and full-bridge topologies. The power range that the can cover is the low one, however they are widely use in different fields as power supplies or single-phase ups (Xue, Chang, Kjaer, Bordonau & Shimizu, 2004). In the following chapters the most important configurations will be discussed.

1.3 Half-Bridge VSI

Fig. 10 shows the standard topology of a half-bridge VSI, in this circuit, two capacitors are needed to give a neutral point N, these capacitors are needed to keep a constant voltage $v_i/2$. How the current harmonics injected by the operation of the inverter are low-order harmonics, a set of large capacitors ($C+$ and $C-$) is required. Looking at the circuit is obvious that both switches cannot be on at the same time, in that case a short circuit across the dc link voltage source v_i would appear.

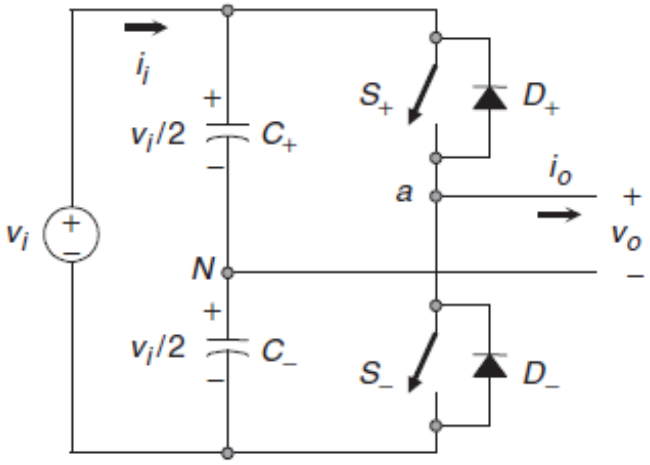

Figure 10. Single-phase half-bridge VSI.

There are two defined (states 1 and 2) and one undefined (state 3) switch state as shown in the table. With the aim to avoid short circuit across the dc bus and the undefined state mentioned before, the modulation technique used should always ensure that at any instant either the top or the bottom switch of the inverter leg is on.

Table 1. Switching states for a half-bridge single-phase VSI.

State	State#	v_0	Components conducting
S_+ is on and S_- is off	1	v_1	S_+ if $i_0 > 0$ D_1 if $i_0 < 0$
S_- is on and S_+ is off	2	$-v_2$	D_2 if $i_0 > 0$ S_- if $i_0 > 0$
S_+ and S_- are all off	3	v_1 $-v_2$	D_2 if $i_0 > 0$ D_1 if $i_0 < 0$

1.3.1. PWM technique

The carrier-based PWM technique fulfills such a requirement as it defines the on- and off-states of the switches of one leg of a VSI by comparing a modulating signal v_c (desired ac output voltage) and a triangular waveform v_Δ (carrier signal). When $v_c > v_\Delta$ the switch S_+ is on and the switch S_- is off, at the same time when $v_c < v_\Delta$ the switch S_+ is off and the switch S_- is on.

A different case is when the modulating signal v_c is a sinusoidal at frequency f_c and amplitude ∇_c, and the triangular signal v_Δ is at frequency f_Δ and amplitude ∇_Δ. This is the sinusoidal PWM (SPWM) scheme. In this case, the modulation index m_a (also known as the amplitude-modulation ratio) is defined as:

$$m_a = \frac{\nabla_c}{\nabla_\Delta} \tag{1}$$

and the normalized carrier frequency m_f (also known as the frequency-modulation ratio) is:

$$m_f = \frac{f_\Delta}{f_c} \tag{2}$$

he PWM technique permits an ac output voltage to be created that cracks a given modulating signal. When the modulating signal is sinusoidal, the SPWM provides, in the linear region, an ac output voltage that varies linearly as a function of the modulation index, and the harmonics are at well-defined frequencies and amplitudes. These characteristics help to simplify the design of filtering components.

In the following figures we have the half-bridge VSI Ideal waveforms for the SPWM (m_a= 0.8, m_f = 9):

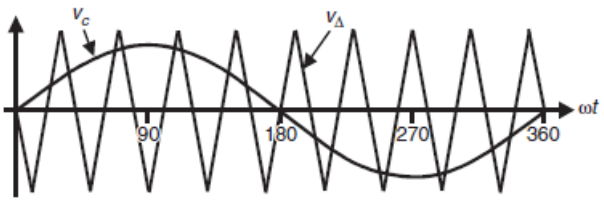

Figure 11. Carrier and modulating signals.

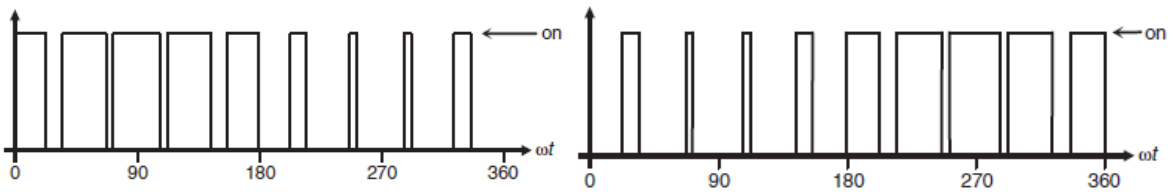

Figure 12. Q1 switch state (left) Q2 switch state (right).

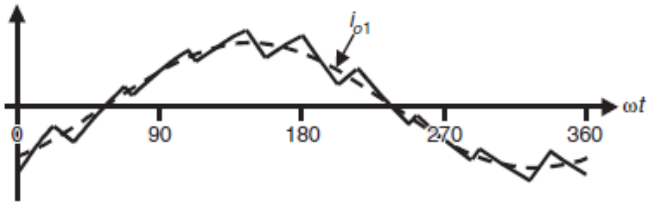

Figure 13. AC output current.

for large values of m_f (m_f > 21), the subharmonics are negligible if an asynchronous PWM technique is used, however, due to potential very low-order subharmonics, its use should be avoided; finally, in the overmodulation region (m_a > 1) some intersections between the carrier and the modulating signal are missed, which leads to the generation of low-order harmonics but a higher fundamental ac output voltage is obtained.

The PWM technique allows an ac output voltage to be generated that tracks a given modulating signal.

1.3.2. Square wave modulating technique.

In this case, both switches S_+ and S_- are on for one half-cycle of the ac output period. This technique is very similar to SPWM but with an infinite modulation index m_a.

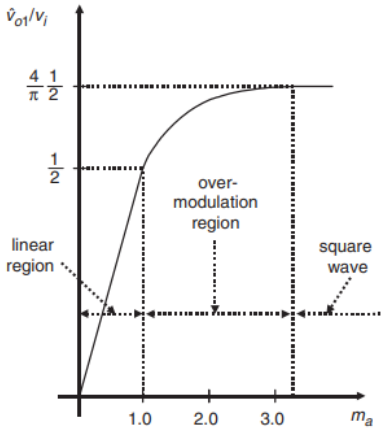

Figure 14. Normalized fundamental ac component of the output voltage in a half-bridge VSI SPWM modulated.

The normalized ac output voltage harmonics are at frequencies h = 3,5,7,9… and for a given dc link voltage we can obtain the ac output voltage features an amplitude given by:

$$\nabla_{o1} = \nabla_{aN1} = \frac{4}{\pi}\frac{v_i}{2} \tag{3}$$

And the harmonics feature an amplitude given by:

$$\nabla_{oh} = \frac{\nabla_{o1}}{h} \tag{4}$$

The ac output voltage cannot be changed by the inverter. However, by controlling the dc link voltage v_i it could be changed (Youssef, 2020).

1.3.3. Selective harmonic elimination (SHE).

In SHE technique, low-order unwanted harmonics are eliminated by determining the angle of the gating pulse of the switch. The inverter voltage equation is expressed in Fourier series as in (5)

$$V(\omega t) = \sum_{n=1}^{\infty} [a_n \sin(n\omega t) + b_n \cos(n\omega t)] \tag{5}$$

Owing to the PWM waveform characteristics of odd functions and quarter-wave symmetry, a_n=0, for all *n*, and the output voltage reduces to:

$$V(\omega t) = \sum_{n=1}^{\infty} b_n \sin(n\omega t) \tag{6}$$

Where ω is the radian frequency of the output voltage. Based in the equation above b_n is expanded regards to number of switching angles and fundamental output voltage, as we can see in (7). Fig.15 shows the sample of output voltage with few notches per quarter-wave cycle.

$$b_n = \frac{2V_{dc}}{n\pi}[2\sum_{k=1}^{N}(-1)^{k-1}\cos n\alpha_k - 1] \tag{7}$$

With the use of pre-determined lookup table, the trajectories of switching angles over a ½π period lie between 0º and 90º when 3^{rd}, 5^{th}, 7^{th}, 9^{th}, 11^{th}, 13^{th}, 15^{th}, 17^{th} harmonic orders are eliminated (Azmi, Shukor & Rahim, 2018)

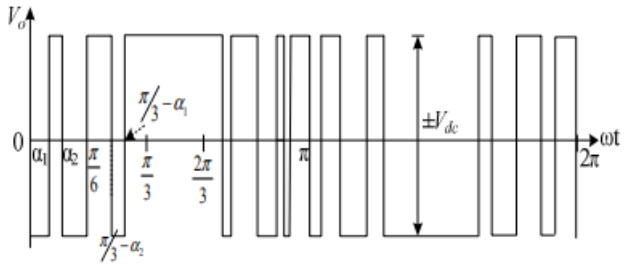

Figure 15. Unipolar output voltage with notches per quarter-wave cycle.

Fig.16 shows the trajectories of switching angles with varying modulation index. Table 2 lists the switching angles plotted in Fig.15 when m_a is 0.9.

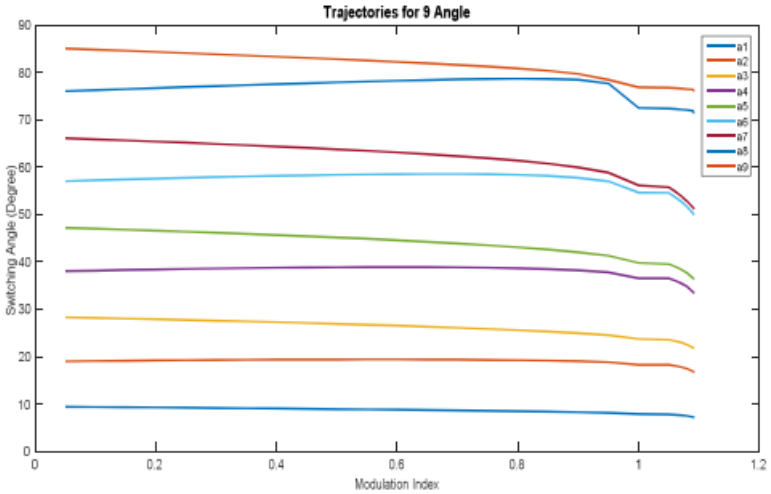

Figure 16. Switching angle trajectories when nine angles are eliminated.

Table 2. Switching angles when ma = 0.9.

α_1	α_2	α_3	α_4	α_5	α_6	α_7	α_8	α_9
8.29	19.06	24.98	38.22	42.05	57.75	59.95	78.42	79.66

1.4 Full-Bridge VSI

Fig. 17 shows the power topology of a full-bridge VSI. Is quite similar to the Half-bridge inverter but with two extra switches.

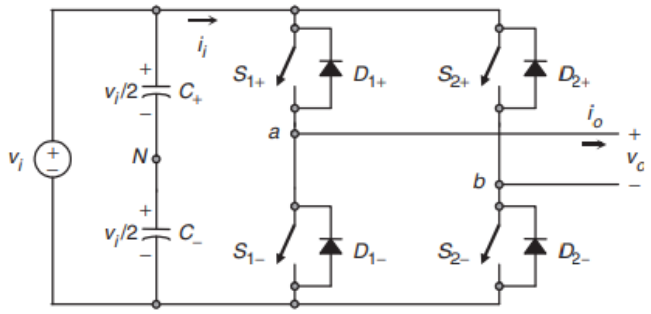

Figure 17. Single-phase full-bridge VSI

In all inverters, if the load is pure resistive, the current waveform is the same as the voltage waveform, with the corresponding scale. However, when the load has reactive components, the intensity will be positively or negatively outdated against the voltage. At intervals where the current and voltage do not coincide in sign, the switches shall be cut in need of the incorporation of diodes in antiparallel, to enable a bidirectional switch in current.

In the table below the switch states of a full-bridge inverter are shown.

Table 3. Switching states for a Full-Bridge single-phase VSI.

State	State#	v_0	Components conducting
S_{1+} and S_{2-} are on and S_{1-} and s_{2+} are off	1	v_1	S_{1+} and S_{2-} if $i_0 > 0$ D_1 and D_4 if $i_0 < 0$
S_{1-} and S_{2+} are on and S_{1+} and S_{2-} are off	2	$-v_1$	D_3 and D_2 if $i_0 > 0$ S_{1-} and S_{2+} if $i_0 < 0$
S_{1+} and S_{2+} are on and S_{1-} and S_{2-} are off	3	0	S_{1+} and D_2 if $i_0 > 0$ D_1 and S_{2+} if $i_0 < 0$
S_{1-} and S_{2-} are on and S_{1+} and S_{2+} are off	4	0	D_3 and S_{2-} if $i_0 > 0$ S_{1-} and D_4 if $i_0 < 0$
$S_{1+}, S_{2+}, S_{1-}$and S_{2-} are all off	5	v_1 $-v_1$	D_3 and D_2 if $i_0 > 0$ D_1 and D_4 if $i_0 < 0$

Keeping S_{1+} and S_{2-} excited (state 1), the a-end of the charge is connected to the positive pole of the battery and the b end to the negative pole, leaving the charge subjected to the VS voltage of the battery. By blocking S_{1+} and S_{2-} and exciting S_{2+} and S_{1-} (state 3), the tension in the load is reversed. Alternatively, the load is subjected to a square alternating voltage of the amplitude equal to the VS battery voltage, which is an advantage over the inverter with a medium battery. In contrast, double semiconductors are needed here (Soomro, Memon, Tayab & Shah, 2016).

Several modulating techniques have been developed that are applicable to full-bridge VSIs. Among all of them are the PWM (bipolar and unipolar) techniques.

1.4.1. Bipolar PWM technique.

A bipolar switching scheme implemented on full bridge inverter is called a two-level inverter, since output voltage switches between two states either positive or negative value of applied voltage as shown in fig. 18(d).

In bipolar switching scheme, carrier and modulating signal are compared. The inverter switches are turned on whenever the reference signal is greater than the carrier signal and vice versa.

This resulting gate pulse shown in fig. 18(b) is applied to switches S_{1+} and S_{2-} of the inverter while its inverted gate pulse is applied to switches S_{2+} and S_{1-} as shown in fig. 18(c).

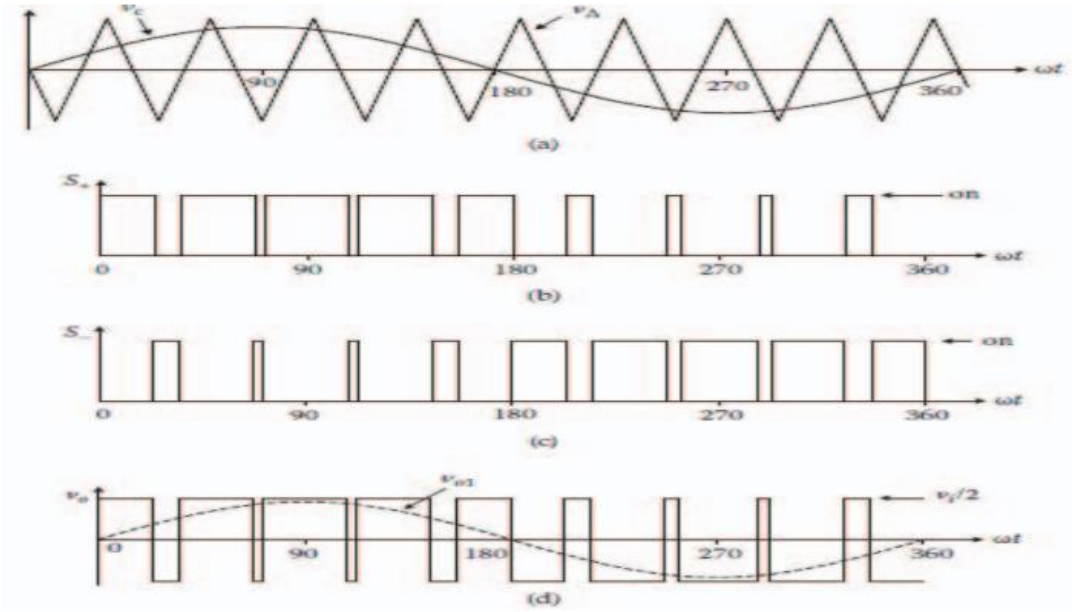

Figure 18. Bipolar Switching scheme.

The ac output voltage waveform in a full-bridge VSI consists basically in a sinusoidal waveform that faces a fundamental component of amplitude ∇_{o1} that accomplishes the expression:

$$\nabla_{o1} = \nabla_{ab1} = \nabla_i m_a \tag{8}$$

in the linear region of the modulating technique ($m_a \leq 1$), which is twice that obtained in the half-bridge VSI. Identical conclusions can be drawn for the frequencies and the amplitudes of the harmonics in the ac output voltage and dc link current, and for operations at smaller and larger values of odd mf (including the overmodulation region ($m_a > 1$), than in half-bridge VSIs, but considering that the maximum ac output voltage is the dc link voltage v_i.

Thus, in the overmodulation region the fundamental component of amplitude ∇_{o1} satisfies the expression:

$$v_i < \nabla_{o1} = \nabla_{ab1} < \frac{4}{\pi} v_i \tag{9}$$

1.4.2. Unipolar switching technique.

A unipolar switching scheme implemented on full bridge inverter is called a two-level inverter, since output voltage switches between two states either positive or negative value of applied voltage as shown in fig. 19(d).

In unipolar PWM, two sinusoidal signals having 180° phase shift are taken having same magnitude and frequency. The two sinusoidal signals are compared with same triangular pulse. The gate signal for switch S_{1+} is generated by comparing positive reference signal and triangular signal as shown in fig. 19(b) while comparing 180 phase shifted reference signal and triangular signal results in gate signal for switch S_{1-} as shown in fig. 19(c).

The switch S_{2+} has complementary switching as compared to S_{1+} and similarly switch S_{2-} has complementary switching as compared to S_{1-}.

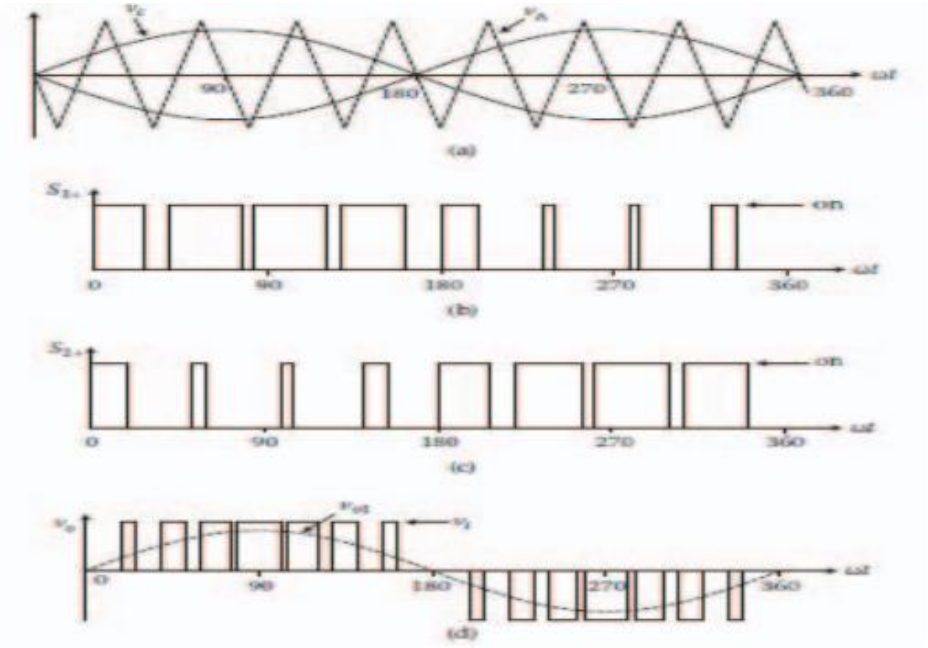

Figure 19. Unipolar Switching scheme.

This feature is considered to be an advantage because it allows the use of smaller filtering components to obtain high-quality voltage and current waveforms while using the same switching frequency as in VSIs modulated by the bipolar approach.

1.5 Three-Phase VSI

While single-phase VSIs cover low-range power applications and three-phase VSIs cover medium- to high-power applications. The main purpose of these topologies is to provide a three-phase voltage source, where the amplitude, phase, and frequency of the voltages should always be controllable. Although most of the applications require sinusoidal voltage waveforms (e.g. ASDs, UPSs, FACTS, var compensators), arbitrary voltages are also required in some emerging applications (e.g. active filters, voltage compensators). The standard three-phase VSI topology is shown in Fig. 20.

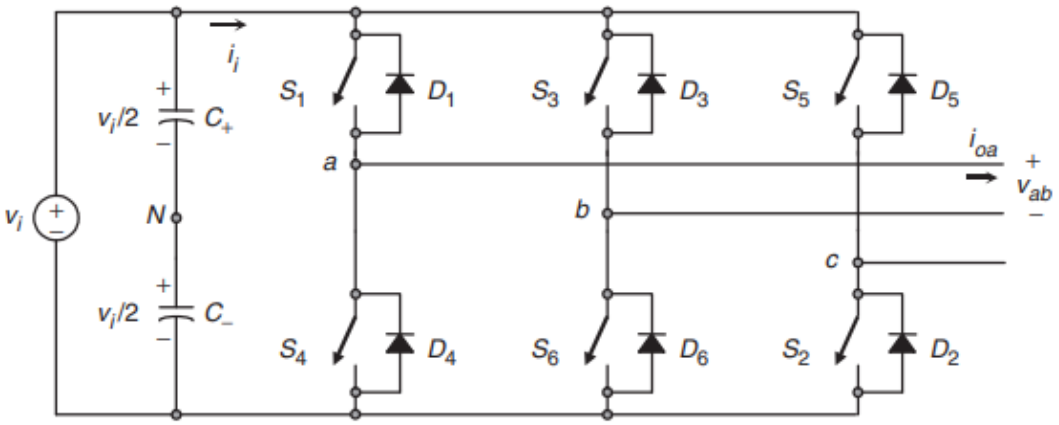

Figure 20. Conventional Three-phase VSI topology

The switching estates are given in Table 4. It is likely to single-phase VSI, the switches of any leg of the inverter (S_1 and S_4, S_3 and S_6 or S_5 and S_2) cannot be witched at the same time, since it would result in a short-circuit across the dc link voltage supply. Similarly, in order to avoid undefined states in the VSI, and thus undefined ac output line voltages, the switches of any leg of the inverter cannot be switched off simultaneously as this will result in voltages that will depend upon the respective line current polarity.

Two of the states from the table produce zero ac line voltages (7 and 8) the remaining states produce non-zero ac line voltages. In order to generate a given voltage waveform, the inverter moves from one state to another. Thus, the resulting ac output line voltages consist of discrete values of voltages that are v_i, 0, and -v_i for the topology shown in Fig. 20. The selection

of the states in order to generate the given waveform is done by the modulating technique that should ensure the use of only the valid states.

Table 4. Valid switch states for a three-phase VS

State	State #	v_{ab}	v_{bc}	v_{ca}	Space vector
S_1, S_2, S_6 on and the rest, off	1	v_i	0	$-v_i$	$\overrightarrow{v_1} = 1 + j0.577$
S_2, S_3, S_1 on and the rest, off	2	0	v_i	$-v_i$	$\overrightarrow{v_2} = j1.155$
S_3, S_4, S_2 on and the rest, off	3	$-v_i$	v_i	0	$\overrightarrow{v_3} = -1 + j0.577$
S_4, S_5, S_3 on and the rest, off	4	$-v_i$	0	v_i	$\overrightarrow{v_4} = -1 + j0.577$
S_5, S_6, S_4 on and the rest, off	5	0	$-v_i$	v_i	$\overrightarrow{v_5} = -j1.155$
S_1, S_5, S_6 on and the rest, off	6	v_i	$-v_i$	0	$\overrightarrow{v_6} = 1 - j0.577$
S_1, S_3, S_5 on and the rest, off	7	0	0	0	$\overrightarrow{v_7} = 0$
S_4, S_2, S_6 on and the rest, off	8	0	0	0	$\overrightarrow{v_8} = 0$

1.6 Multilevel inverters

Conventional two-level inverter produces only two levels in the output voltage and PWM is used to form the AC output waveform. Even though the AC output waveform is produced it includes harmonics and these causes the high rate of change of voltage as compared to the multilevel inverter (Krishna & Padma, 2016). Some devices requests for low rate of change in voltage.

Multilevel inverters generate more than two voltage levels with almost pure sinusoidal voltage waveform, all of this with a low dv/dt and low harmonic distortions (Nordwall, 2011). Multiple voltage levels in the output waveform turns this smoother but with increasing levels the circuit becomes more complex due to the addition of the extra valves. Because of the complexity of the circuit a complicated control is also required.

In the following table we have a brief comparison of conventional and multilevel inverter (Kosti, Amol and Rao, 2017).

Table 5. Comparison of traditional and multilevel inverter.

TRADITIONAL	**MULTILEVEL**
High rate of change of voltage	Low range of change of voltage
Switching losses are high	Switching losses are low
For low voltage application	For high voltage application
Voltage stress is more on switches	Voltage is less on switches
High switching frequency	Low switching frequency
Multiple voltage levels cannot be produced	Multiple voltage levels can be produced
More harmonics	Less harmonics

1.7 Multilevel inverters topologies

Three major multilevel inverter structures have been mostly applied in industrial applications classified according to the voltage source used in the inverter. Fig.21 shows them. Moreover, different hybrid multilevel inverters have been developed (Bendre, Krstic Meer, Venkataramanan, 2005).

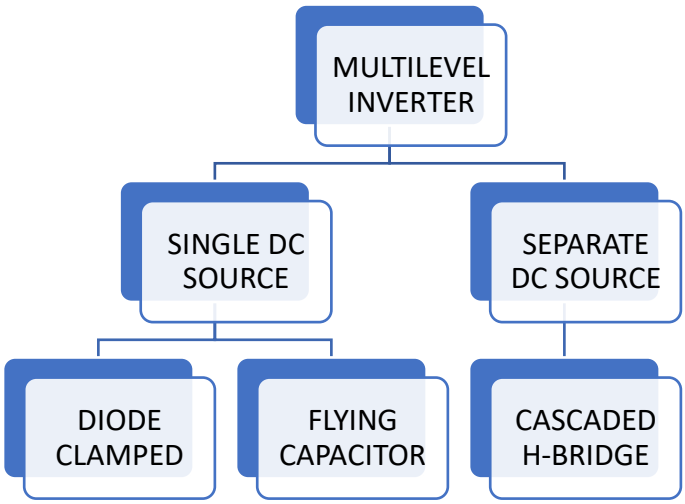

Figure 21. Classification of multilevel inverter topologies according to the voltage source

1.7.1 Diode clamped multilevel inverter.

There exist DC-MLIs with three, four five and six levels for different uses like static VAR compensators, high voltage grid interconnections, and variable speed motor drives.

In the Fig. 22 a three-phase five-level DC-MLI topology is shown. Each of the three-phase outputs of inverter shares a common DC bus voltage that has been divided into five levels over four DC bus capacitors. The capacitors have been subscripted from C_1 to C_4. The middle point of C_2 and C_3 capacitors constitute the neutral point of inverter and output voltages have five voltage states referring to neutral point. The voltage across each capacitor is V_{dc} /4 and the voltage stress on each switching device is limited to V_{dc} through the clamping diodes that have been named as $D_{1.3}$ and $D_{1.3^*}$.

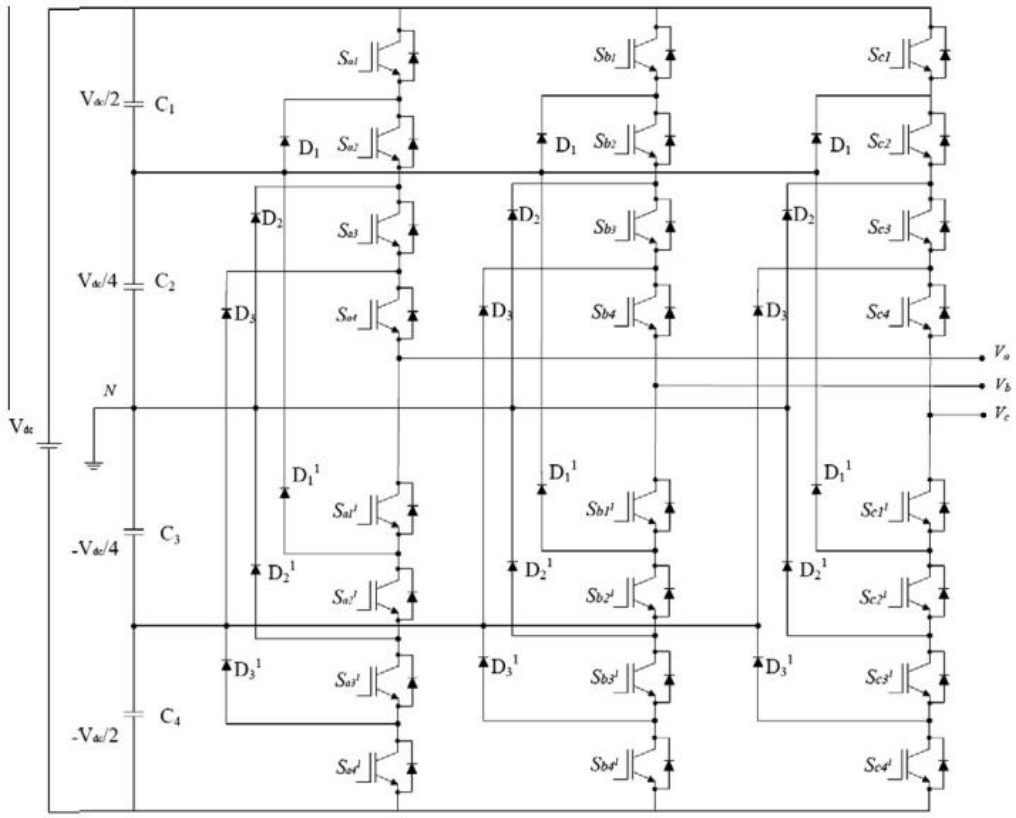

Figure 22. Three-phase five-level topology of a diode clamped multilevel inverter.

Clamping diodes are the key components that differ this topology from a conventional two-level inverter. The neural point n has been assumed as the output phase voltage reference and the switching combinations have been analyzed for phase A output voltage V_{an} as we can observe in Table 6.

For the five-level DC-MLI in Fig. 22, a set of four switches is ON at any given period and they are S_a1 to S_a4 for voltage level of V_{an} = V_{dc}/4. The second switching state shows the voltage level of V_{an} = V_{dc}/4 and S_{a2} to S_{a1} switches should be triggered. The remaining switching states that constitute 0 and negative outputs can be seen in Table 6. The clamping diodes require different voltage ratings for reverse voltage-blocking due to each triggered switch is only required to block a voltage level of V_{dc}*/(m-1)*. By assuming the switches from S_{a1} to S_{a4} are triggered as seen in first line of Table 6, D_1 blocking diode needs to block a voltage at the rate of $3V_{dc}$/4 that is generated by three DC bus capacitors.

Since each blocking diode voltage rating is the same as the active device voltage rating, the number of diodes required for each phase will be calculated as *(m-1)×(m-2)*, where m represents number of inverter levels. The following equations are used to determine the e required device numbers to form a given level of a diode clamped MLI. If m is assumed as the number of levels, the number of capacitors at the DC side (*c*) can be known by using Eq. (10).

The number of freewheeling diodes (*d*) per phase, and the number of clamping diodes (*j*) can be calculated by using Eqs. (11) and (12) respectively.

$$c = m - 1 \tag{10}$$

$$d = 2(m - 1) \tag{11}$$

$$j = (m - 1) \times (m - 2) \tag{12}$$

Table 6. Voltage levels of five-level DC-MLI and switching states.

Voltage V_{an}	Switching state							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a1^*}	S_{a2^*}	S_{a3^*}	S_{a4^*}
$V_4 = V_{dc}/2$	1	1	1	1	0	0	0	0
$V_3 = V_{dc}/4$	0	1	1	1	1	0	0	0
$V_2 = 0$	0	0	1	1	1	1	0	0
$V_1 = -V_{dc}/4$	0	0	0	1	1	1	1	0
$V_0 = -V_{dc}/2$	0	0	0	0	1	1	1	1

The DC-MLIs are quite efficient in fundamental switching applications, however the number of clamping diodes needed is quadratically related to the number of levels. Fundamental switching will cause an increment o voltage and current THD, while increased number of clamping diodes makes the topology bulky (Swarmy & Venkatesan, 2019) also in this case the cost and size of the system increases. To design more level inverter, DCI produces fewer harmonics. In this topology filters are not required (Çolak & Kabalci, 2008).

1.7.2 Flying capacitor multilevel inverter

This type of inverter was introduced as an alternative to DC-MLI. In Fig.23 a three-phase five-level topology of this inverter is shown. Main structure of this topology is similar to DC-MLI but the inverter uses DC side capacitors in a ladder form instead of clamping diodes. The voltage change between two adjoining capacitor legs gives the size of the voltage steps in the output waveform. In an m level structure, the FC-MLIs require *(m-1)* DC link capacitors and *(m-1) × (m-2)/2* auxiliary capacitors per phase comparing to DC-MLI topology (Song, Kim, Lai, Seong, Kim & Park, 2001). By using a huge quantity of storage capacitors be able to ride-through abilities throughout a power outage

In Fig. 23, each of the three-phase outputs of inverter shares a common DC bus voltage that has been divided into five levels over four DC bus capacitors like DC-MLI topology. The auxiliary capacitors (C_{a1}, C_{a2}, C_{a3}) are pre-charged to the voltage levels of $V_{dc}/4$, $V_{dc}/2$, $3V_{dc}/4$ V respectively. The pre-charge operation ensures the effectiveness of the inverter allowing it to generate multilevel voltage waveforms. Voltage synthesis in a five-level FC-MLI has more flexibility than a DC-MLI. The FC-MLI topology also consists of complementary switch pairs as (S_{a1} - S_{a1^*})), (S_{a2} - S_{a2^*})), (S_{a3} - S_{a3^*})), and (S_{a4} - S_{a4^*})) as seen in Fig. 23. The switching

pairs may differ as asymmetrically according to control strategies, but both pair selection strategy will cause the switching state redundancy that can be used to achieve voltage balancing in FC-MLIs (Kuhn, Ruger & Mertens, 2007).

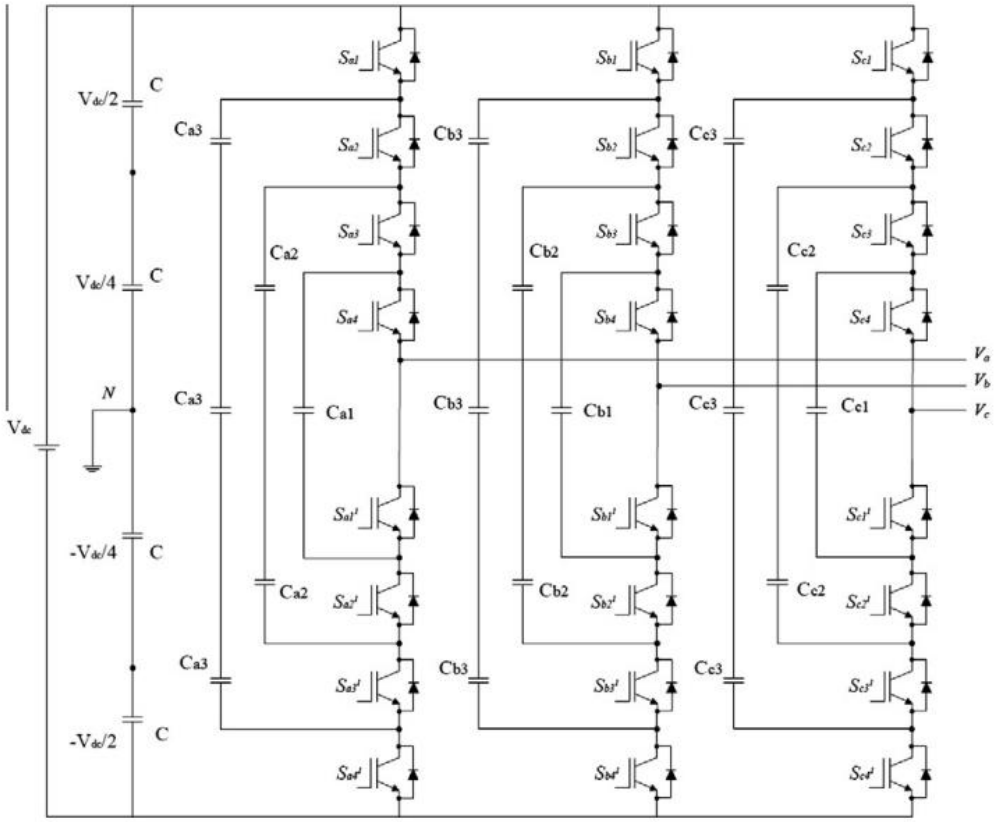

Figure 23. Three-phase five-level topology of a flying capacitor multilevel inverter.

In table 7 we can observe the switching combinations for phase voltage output (V_{an}) which is relative to neutral point of n. The optional switching states for voltage levels of $V_{dc}/4$, 0, $-V_{dc}/4$ shows the phase redundancies of FC-MLI as an advantage to line-to-line redundancies of DC-MLI. This advantage allows the user to select charging and discharging orders of capacitors by constituting proper switching algorithms.

FC-MLI topology has introduced quite significant advantages, the most important are preventing the filter demand, and controlling the active and reactive power flow besides phase redundancies. Despite these advantages, the increment of m level will restrain the accurate charging and discharging control of capacitors. The cost of inverter will increase and device will be more enlarged due to increased number of capacitors. For real power transmission controlling of this topology is very difficult making switching losses and switching frequency losses are bigger (Rodriguez, Lai & Peng, 2002)

Table 7. Voltage levels of five-level DC-MLI and switching states.

Voltage V_{an}	Switching state							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a1^*}	S_{a2^*}	S_{a3^*}	S_{a4^*}
$V_4 = V_{dc}/2$	1	1	1	1	0	0	0	0
$V_3 = V_{dc}/4$	1	1	1	0	1	0	0	0
	0	1	1	1	0	0	0	1
	1	0	1	1	0	0	1	0
$V_2 = 0$	1	1	0	0	1	1	0	0
	0	0	1	1	0	0	1	1
	1	0	1	0	1	0	1	0
	1	0	0	1	0	1	1	0
	0	1	0	1	0	1	0	1
	0	1	1	0	1	0	0	1
$V_1 = -V_{dc}/4$	1	0	0	0	1	1	1	0
	0	0	0	1	0	1	1	1
	0	0	1	0	1	0	1	1
$V_0 = V_{dc}/2$	0	0	0	0	1	1	1	1

1.7.3 Cascaded H-bridge multilevel inverters (CHB-MLI)

An alternative multilevel inverter topology with less power devices requirement compared to previously mentioned topologies is known as cascaded H-bridge multilevel inverter (CHB-MLI) and the topology is based on the series connection of H-bridges with separate DC sources. Since the output terminals of the H-bridges are connected in series, the DC sources must be isolated from each other. Owing to this property, CHB-MLIs have also been proposed to be used with fuel cells or photovoltaic arrays in order to achieve higher levels (Kuhn, Ruger & Mertens, 2007).

The resulting AC output voltage is synthesized by the addition of the voltages generated by different H-bridge cells. Each single-phase H-bridge generates three voltage levels as $+V_{dc}$, 0, $-V_{dc}$ by connecting the DC source to the AC output by different combinations of four switches, S_{A1}, S_{A1^*}, S_{A2}, S_{A2^*} as seen in first cell of Fig. 24. The CHB-MLI that is shown in Fig. 24 utilizes two separate DC sources per phase and generates an output voltage with five levels. To obtain $+V_{dc}$, S_{A1} and S_{A2^*} switches are turned on, whereas $-V_{dc}$ level can be obtained by turning on the S_{A2} and S_{A1^*}. The output voltage will be 0 by turning on S_{A1^*} and S_{A2} switches or S_{A1^*} and S_{A2} switches. If n is assumed as the number of modules connected in series, m is the number of output levels in each phase as seen in Eq. (13). The switching states of a CHB-MLI (*sw*) can be determined by using Eq. (14)

$$m = 2n + 1 \tag{13}$$

$$sw = 3^n \tag{14}$$

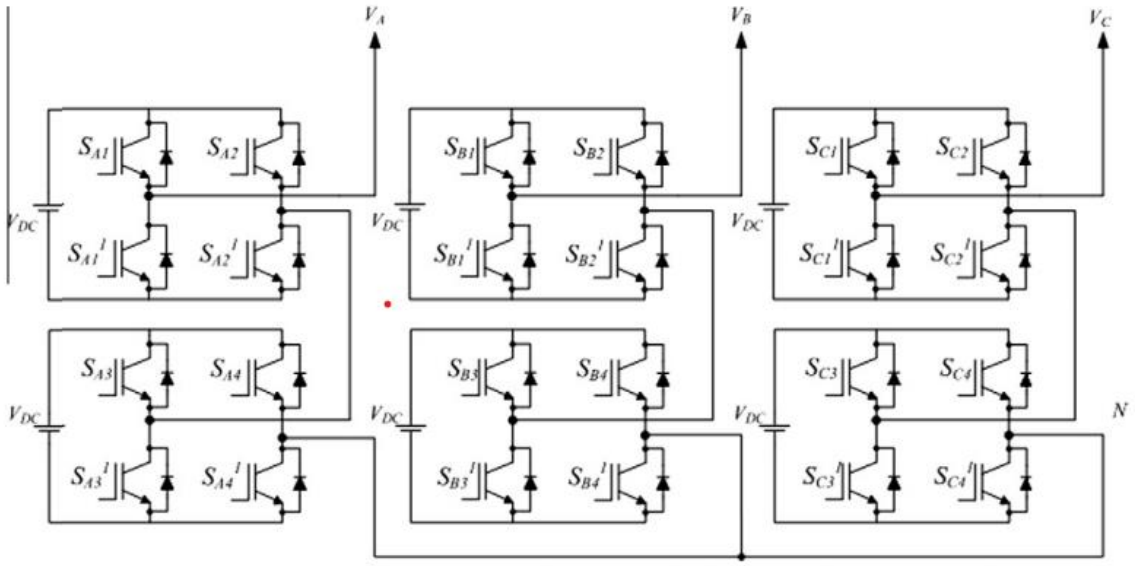

Figure 24. Three-phase five-level topology of cascaded H-bridge multilevel inverter

In Fig. 24 we can see that the first leg phase voltage (V_{an}) is continued by multiplying V_{a1} and V_{a2} values of series connected H-bridge cells and will generate a stepped waveform as seen in Fig. 25.

Negative output pulses are indicated as P_{1^*} and P_{2^*} while the positive output pulses are shown P_1 and P_2. The equation 15 shows the Fourier series expansion of the general multilevel stepped output voltage. In equation 16 n is the harmonic number of the output voltage of inverter.

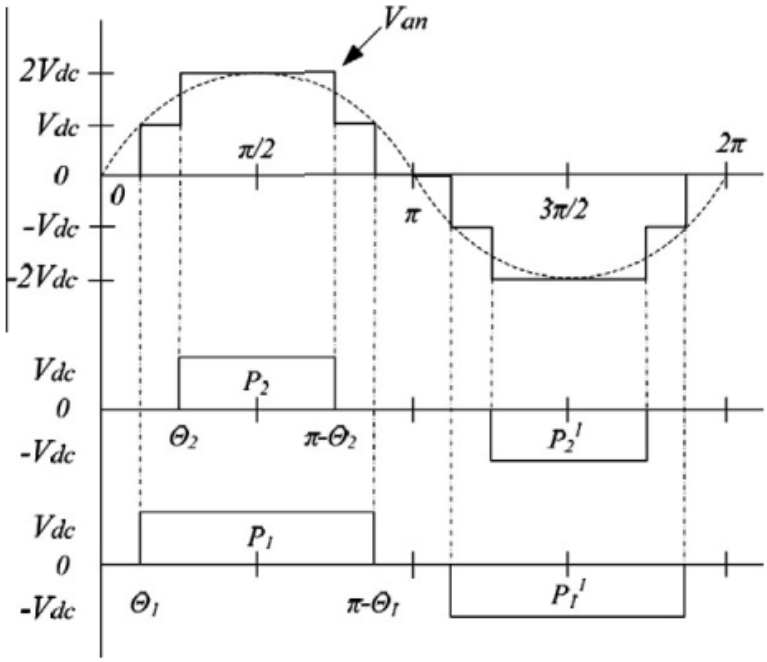

Figure 25. Phase output voltage waveforms of a five-level topology CHB-MLI with two separate DC sources.

$$V(\omega t) = \frac{4V_{dc}}{\pi} \sum_{n=1,3,5....}^{\infty} [\cos(n\theta_1) + \cos(n\theta_1) + ... + \cos(n\theta_5)] \frac{\sin(n\omega t)}{n} \quad (15)$$

$$V(\omega t) = \frac{4V_{dc}}{\pi} \sum_{n=1,3,5....}^{\infty} [\cos(n\theta_1) + \cos(n\theta_1)] \frac{\sin(n\omega t)}{n} \quad (16)$$

CHB-MLIs have been previously designed for static VAR compensators and motor drives, but the topology has been prepared an interface with renewable energy sources due to using separate DC sources. There are numerous studies have been performed on CHB-MLIs for connecting renewable energy sources with AC grid and power factor correction.

They require lower number of components associated with all other converters to reach a similar number of output levels. For real power conversions required isolated dc sources for cascaded H-Bridge MLI. Table 8 indicates the comparison between three basic multi-level topologies.

Table 8. Comparison between three basic Multi-level topologies.

Topologies	DC- MLIs	FC- MLIs	H-Bridge MLIs
DC bus capacitors	(m-1) m- Levels	(m-1)	(m-1)/2
Switching devices	2(m-1)	2(m-1)	2(m-1)
Clamping Diodes	(m-1)(m-2)	-	-
Flying capacitors	-	(m-1)(m-2)/2	-

1.8. Modulation techniques.

The efficiency parameters of a multilevel inverter such as switching losses and harmonic reduction are principally depended on the modulation strategies used to control the inverter. Multi-level inverter control techniques are based on fundamental and high switching frequency as we can see in Fig. 26

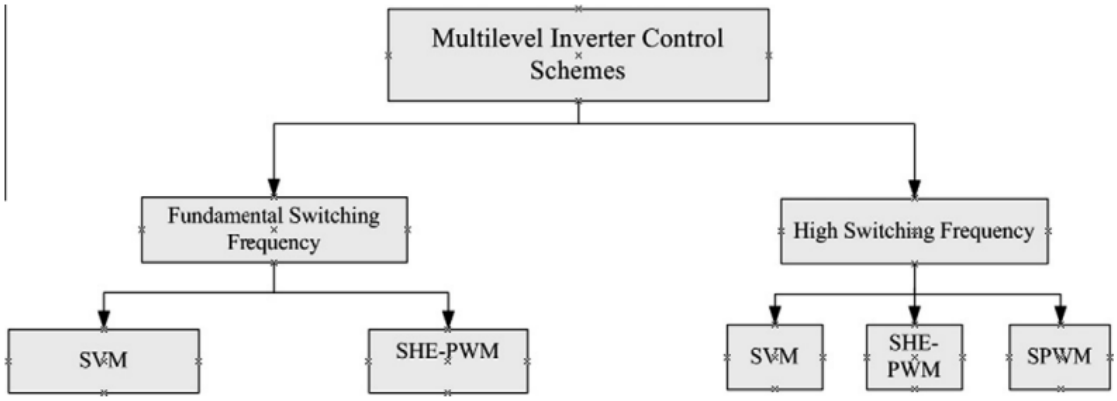

Figure 26. Classification of multilevel inverter control scheme based on switching frequency.

There exists also another popular classification for the multi-level inverters based on open loop and closed loop concepts as we can see in Fig. 27.

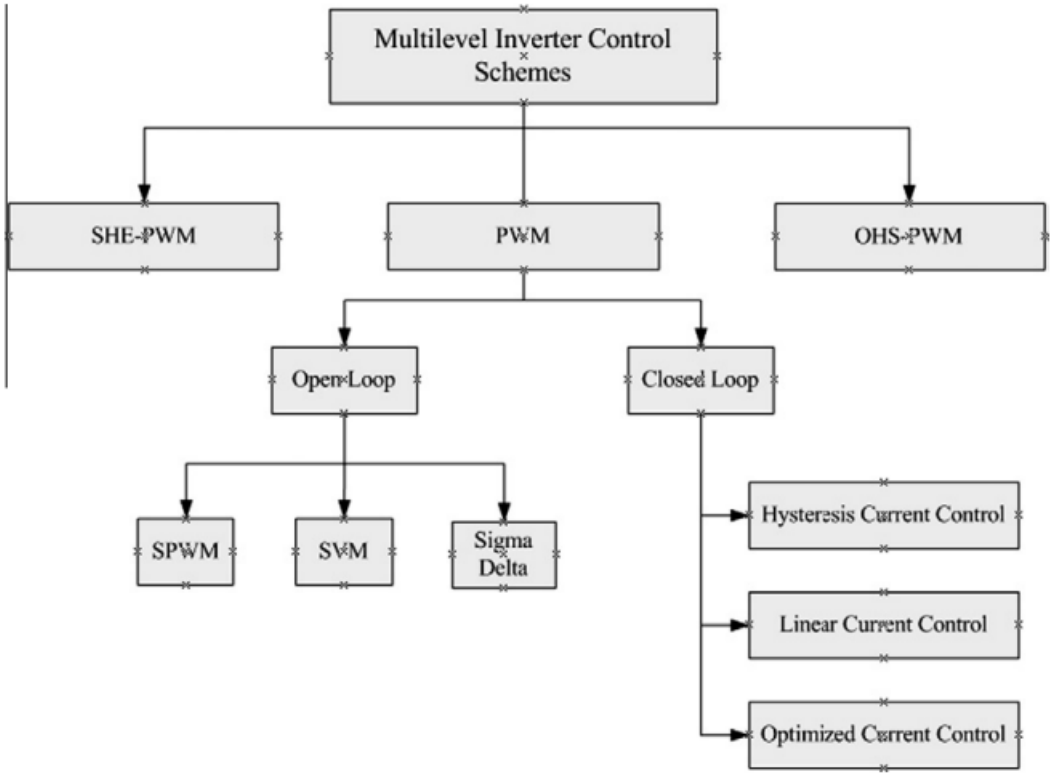

Figure 27. Control schemes of multilevel inverters.

Three main control techniques of multilevel inverters are SHE-PWM, PWM, and optimized harmonics stepped pulse width modulation (OHS–PWM). The open loop PWM techniques are SPMW, space vector PWM, sigma–delta modulation, while closed loop current control methods are defined as hysteresis, linear, and optimized current control techniques.

Among various control schemes, the sinusoidal PWM (SPWM) is the most used control scheme for the control of multilevel inverters. In SPWM, a sinusoidal reference waveform is compared with a triangular carrier waveform to generate switching sequences for power semiconductor in inverter module.

SVM results to be one of the most promising methods in three-phase systems, the only problem is that is quite complex due to the increased number of power semiconductors. One of the most important methods to optimize control of the inverter is to select and design appropriate PWM modulation according to inverter topology.

Fundamental switching frequency methods shall be selected to reduce switching losses for high voltage modules, while multi-carrier SPWM is selected to control low voltage modules.

1.8.1 Selective harmonic elimination PWM (SHE-PWM)

The main idea of this method is based on defining the switching angles of harmonic orders to eliminate and obtaining the Fourier series expansion of output voltage. An example output voltage Fourier expansion of an 11-level inverter can be written as in Eq. (15), which we have seen previously. The required switching angles to eliminate 5th, 7th, 11th, and 13th harmonic orders at fundamental switching frequency for an 11-level multilevel inverter can be calculated as given in Eq. (17).

$$\cos(\theta_1) + \cos(\theta_2) + \dots \cos(\theta_5) = 5 * m_a \tag{17}$$
$$\cos(5\theta_1) + \cos(5\theta_2) + \dots \cos(5\theta_5) = 0$$
$$\cos(7\theta_1) + \cos(7\theta_2) + \dots \cos(7\theta_5) = 0$$
$$\cos(11\theta_1) + \cos(11\theta_2) + \dots \cos(11\theta_5) = 0$$
$$\cos(13\theta_1) + \cos(13\theta_2) + \dots \cos(13\theta_5) = 0$$

The switching angles of θ_1, θ_2, θ_3, θ_4 and θ_5 can be determined to minimize voltage THD ratio, while m_a defines the modulation index of modulator. The values are obtained using Newton-Raphson iterations (explained earlier in this paper) due to the nonlinearity of the parameters. The switching angles can be obtained at the values of θ_1 = 6.57, θ_2 = 18.94, θ_3 = 27.18, θ_4 = 45.14 and θ_5 = 62.24 by assuming m_a as 0.8 and solving with Newton–Raphson Iteration. Possible switching angles are calculated previously and saved to look-up tables in an independent memory or microprocessor. The main drawback of SHE-PWM is the requirement of calculations to determine switching angles as in fundamental frequency switching method. Increased DC sources or switching angles will prevent to obtain the most accurate solution (Smail, Taib, Saad, Isa & Hadzer, 2002).

1.8.2 Sinusoidal PWM (SPWM)

SPWM technique is one of the most popular modulation techniques among the others applied in power switching inverters. In SPWM, a sinusoidal reference voltage waveform is compared with a triangular carrier waveform to generate gate signals for the switches of inverter. Power dissipation is one of the most important issues in high power applications.

The fundamental frequency SPWM control method was proposed to minimize the switching losses. The multi-carrier SPWM control methods also have been implemented to increase the performance of multilevel inverters and have been classified according to vertical or horizontal arrangements of carrier signal. The vertical carrier distribution techniques are defined as Phase Dissipation (PD), Phase Opposition Dissipation (POD), and Alternative Phase Opposition Dissipation (APOD), while horizontal arrangement is known as phase shifted (PS) control technique. In fact, PS-PWM is only useful for cascaded H-bridges and flying capacitors, while PD-PWM is more useful for NPC (Çolak, Bayindir & Kabalci, 2011).

Each of the mentioned multi-carrier SPWM control techniques have been illustrated in Fig. 28, respectively. SPWM presents a lot of advantages among other modulations including easy implementation, lower harmonic outputs according to other techniques, and low switching losses. In SPWM control, a high frequency triangular carrier signal is compared with a low frequency sinusoidal modulating signal in an analog or logic comparator devices. The frequency of modulating sinusoidal signal defines the desired line voltage frequency at the inverter output (Gupta & Khambadkone, 2006)

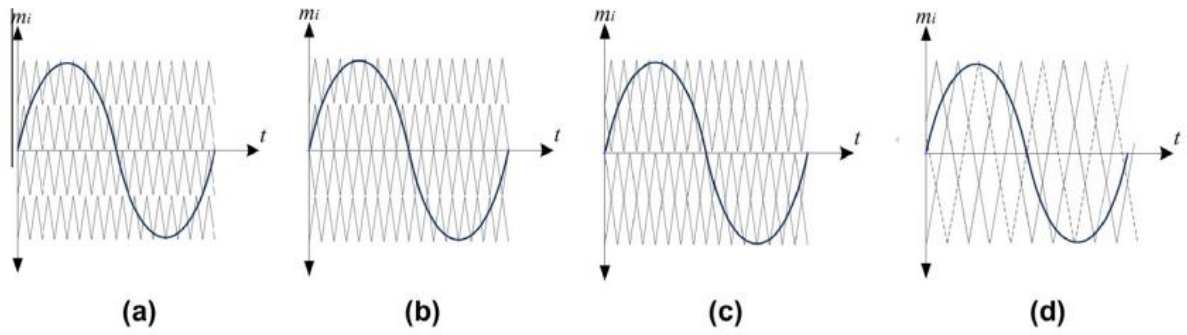

Figure 28. Multi-carrier SPWM control strategies: (a) PD, (b) POD, (c) APOD, (d) PS.

In SPWM control technique, the output voltage is obtained in linear modulation range,

$$V_{AB} = V_{BC} = V_{CA} = m_i \frac{\sqrt{3}V_d}{2} \quad 0 < m_i \leq 1 \tag{18}$$

and the output voltage value is defined for the over-modulation range as seen in Eq. (19).

$$\frac{\sqrt{3}V_d}{2} < V_{AB} = V_{BC} = V_{CA} < \frac{4}{\pi}\frac{\sqrt{3}V_d}{2} \quad m_i \geq 1 \tag{19}$$

1.8.3 Space vector PWM (SPV)

An alternative popular control method for multilevel inverters is defined as space vector PWM (SVM) that directly uses the control variable given by the control system and identifies each switching vector as a point in complex space of (α, β).

The harmonic elimination and fundamental voltage ratios in SVM schemes are obtained in better values compared to SPWM schemes. In addition to this, the maximum peak value of the output voltage is 15% greater than triangular carrier-based modulation techniques. Sector identification and look-up table requirement to determine the switching intervals for all vectors make SVM method quite complicated. Although the difficulty of determining sectors and switching sequences according to increased n-level of inverter, DSP and microprocessor implementations provide proper solution while preparing the algorithms.

The SVM method uses several level-shifted carrier waves to compare with the reference phase voltage signals when applied to multilevel inverters. Any three-phase n-level space vector diagram consists of six sectors that all contains $(n-1)^2$ vector combinations per sector and n^3 switching. Fig. 29 shows the space vector diagram of a three-phase three-level DC-MLI inverter. Each phase leg of inverter includes four switching devices and has three different switching states that are represented as 1, 0, or -1 to illustrate positive, zero, and negative switching sequences (Feng, Liang, Agelidis & Green, 2006).

The switching states have been shown on vector intersections and 27 different states have been located to illustrate required switching states. The switching states and definitions for output voltage levels are given in Table X as referring to DC-MLI.

The zero voltage vectors have three switching states as (0 0 0, 1 1 1, -1 -1 -1). The vectors given in Fig. X are classified into three groups that are named as small vectors ($V_1 - V_6$), middle vectors (V_8, V_{10},, V_{12}, V_{14}, V_{16}, V_{18}), and the large vectors (V_7, V_9,, V_{11}, V_{13}, V_{15}, V_{17}). By assuming the reference voltage vector V_ref located in the 2nd region (∇_2) of S_1 sector, it can be constituted by voltage vectors of V_1, V_2, and V_8 during the sampling period (T_s). The reference voltage also depends on the dwelling times of voltage vector. Hence, the equation for ON time of the voltage vectors that constitutes the reference voltage can be given as in Eq. (20).

$$V_{ref} * T_s = V_1 * t_a + V_2 * t_b + V_8 * t_c \tag{20}$$

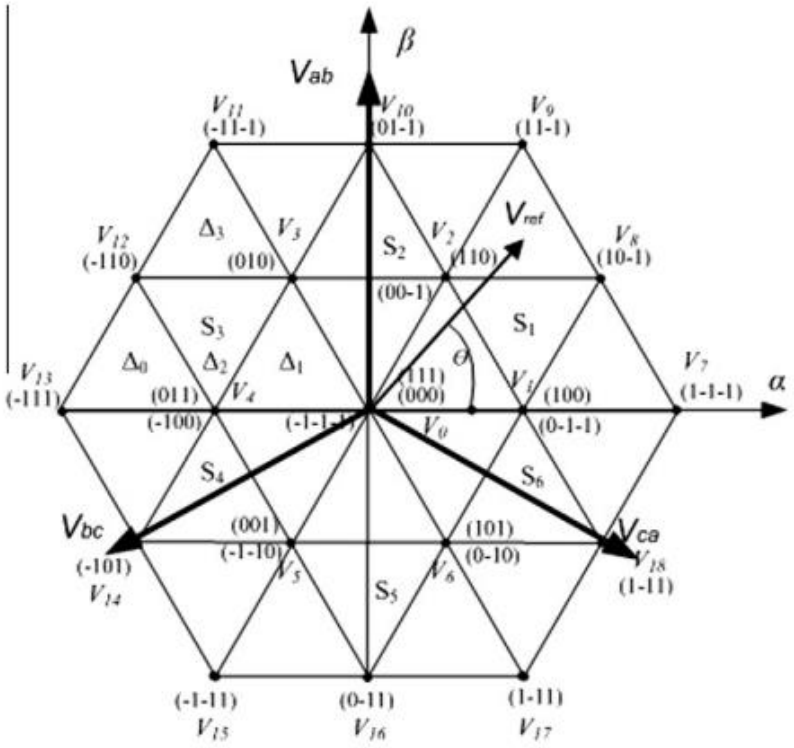

Figure 29. Space vector diagram of a three-level inverter with sector and subsectors.

ON times of voltage vectors can be determined using Eq. (21).

$$\left.\begin{aligned} t_a &= T_s - 2n\sin\theta \\ t_b &= 2n\sin\left(\frac{\pi}{3}+\theta\right) - T_s \\ t_c &= T_s - 2n\sin\left(\frac{\pi}{3}-\theta\right) \end{aligned}\right\} \tag{21}$$

Where:

$$n = \left(\frac{4\sqrt{3}}{3}\right)\left(\frac{V_{ref}}{V_{dc}}\right)T_s \tag{22}$$

The calculations given above has been performed to show one of the possible V_ref value in a region of sectors and required to reply to determine each switching sequence. There are various studies have been realized to reduce complicated calculations of vectors and simplify the required SVM algorithms in order to control multilevel inverters that generate five-level and above output voltage (Escobar, Martinez & Ramos, 2006).

Table 9. Switching states and definitions.

Switching symbol	Switching states						Phase voltage
	S_1	S_2	S_{1^*}	S_{2^*}	D_1	D_2	
1	ON	ON	OFF	OFF	OFF	OFF	$V_{dc}/2$
0	OFF	ON	ON	OFF	Depend on polarity load voltage		0
-1	OFF	OFF	ON	ON	OFF	OFF	$V_{dc}/2$

1.8.4 Sigma delta PWM (SDM)

Originally the DM was proposed as a 1-bit audio and video signal encoding method in digital modulating and control techniques issues. The sigma–delta modulation (SDM) has been described with in order to prevent the decreasing on power density of modulated signal according to increased sampling frequency (Loh, Bode & Tan, 2005). Fig. 30a shows a typical topology.

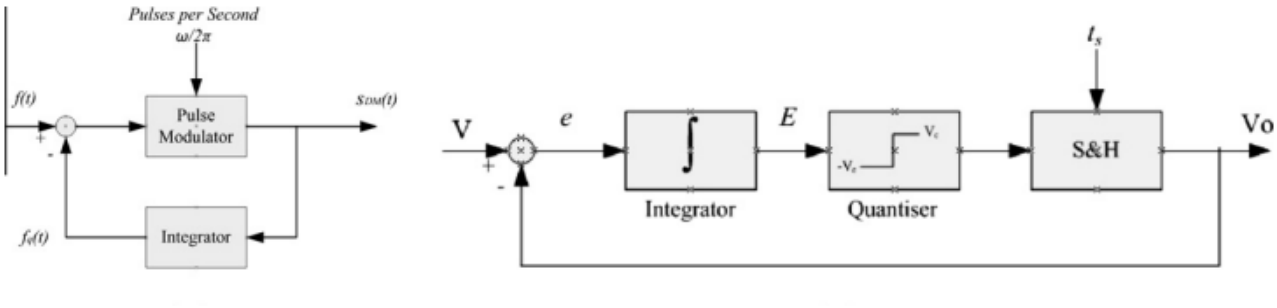

Figure 30. Block diagrams of delta modulation: (a) simple delta modulator, (b) sigma-delta modulator.

In the Fig. 30b, the output of modulator changes between $+V_0$, and $-V_0$ according to sampling period of fs and the output is compared with input amplitudes. The comparison result (e) is integrated (E) and the quantizer determines the output sign opposite to E. A multilevel SDM generates multi-bit data sequence and decoding the output yields several output states which can be used to control on/off states of the switches of multilevel inverter. Fig. 31 depicts the block diagram of an SDM controlled multilevel inverter. The interaction of SDM modulator and inverter is managed using a multilevel decode logic block that adopts the quantized SDM signals and decodes to switching signals for inverter. The last studies have shown that although it is great to control DC-link inverters, the sigma–delta modulators can be developed to control multilevel inverters using logic interfaces. For a SDM controlled multilevel inverter, the output errors such as irregular voltage distribution and system nonlinearity can be reduced in high frequency switching up to 200 kHz.

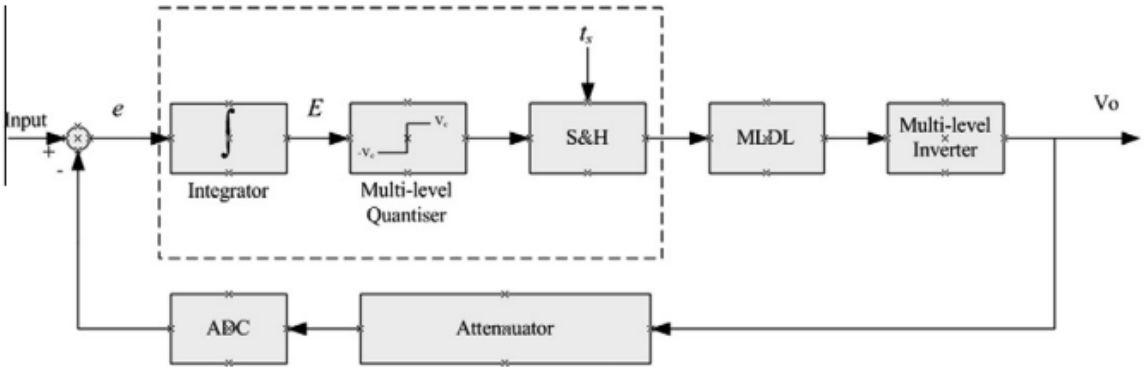

Figure 31. SDM control of a multilevel inverter.

1.8.5 Closed loop PWM control techniques

Most applications of three-phase voltage source PWM inverters such as motor drives, active filters, and static VAR compensators require a control structure comprising an internal current feedback loop. Multilevel inverter systems also utilize photovoltaic (PV) sources or wind generators to integrate renewable energy sources to grid. The performance of the inverter systems which are supplied with DC sources mentioned before largely depends on the quality of the applied current control strategy. Numerous studies have been performed to reduce harmonic contents using current control for active power filter or PV and wind generator interconnection to grid applications of MLIs. The applied current control techniques are mostly focused on hysteresis current control (HCC) and linear current control (LCC) (Chen, Xu & Ni, 2004).

The hysteresis modulation is a feedback current control method where the load current tracks the reference current within a hysteresis band in nonlinear load application of an MLI. Fig. 32a shows the block diagram of a hysteresis control of an H-bridge and Fig. 32b shows the operation principle of the hysteresis modulation. The controller generates the sinusoidal reference current of desired magnitude and frequency that is compared with the actual line current. If the current exceeds the upper limit of the hysteresis band, the next higher voltage level should be selected to attempt to force the current error towards zero. However, the new inverter voltage level may not be sufficient to return the current error to zero and inverter should switch to next higher voltage level until the correct voltage level is selected. As a result, the current gets back into the hysteresis band, and the actual current is forced to track the reference current within the hysteresis band. Three hysteresis controllers which are used to implement the correct voltage level selection are defined as double offset band three level, double band

three level, and time-based three level hysteresis controllers (Siwakot, Yam, Forouzesh, Mojtaba & Pham, 2018).

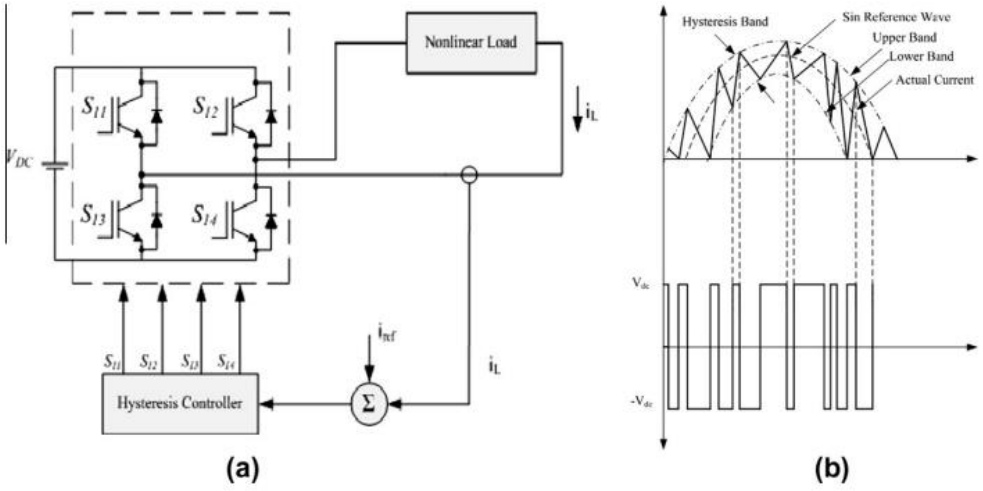

Figure 32. Hysteresis current control: (a) block diagram of a H-bridge cell with hysteresis controller, (b) hysteresis current band and voltage curves of load feedback.

As an alternative approach of MLI applications, the grid interconnection with inverter also requires current control schemes. Linear current controllers are classified as ramp comparison controller, stationary vector controller, and synchronous vector controller. The ramp comparison current controller utilizes the output-current ripple and feedback to control the switching instants. In the three-phase isolated neutral-load topology, the three-phase current should have a sum of zero. Therefore, two linear compensators are required and the three-phase inverter reference voltage signals can be established algebraically using two-tothree-phase conversion ab/abc blocks as seen in Fig. 33.

The basic linear current controller consists of a tracking regulator with a proportional-integrator compensator for PV inverters.

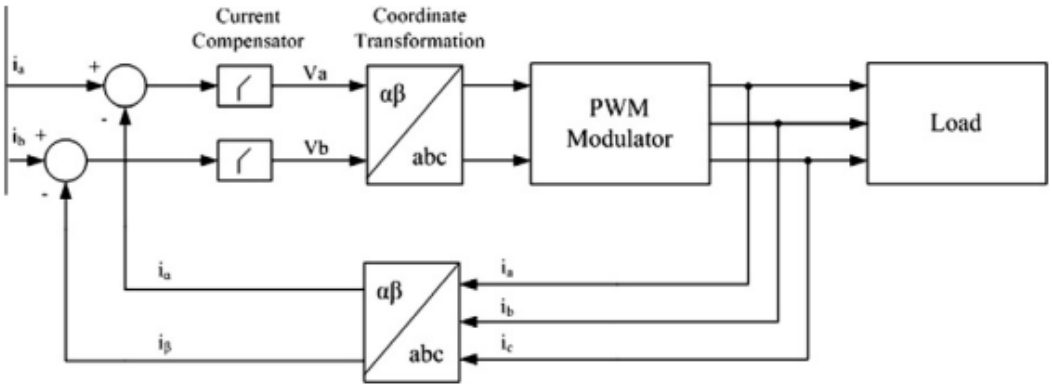

Figure 33. The block diagram of stationary linear current controller**.**

1.8.6 Comparison of the topologies and control scheme.

MLIs are increasingly being used in medium voltage and high-power applications owing to numerous advantages such as low power dissipation due to reducing the voltage stress on switching devices and minimizing the harmonic contents at the output of the inverter. The selected control scheme for an MLI determines the affectivity on harmonic elimination, while generating the ideal output voltage.

The applications of MLIs including induction machine and motor drives, active filters, renewable energy sources interconnection to grid, flexible AC transmission systems (FACTS), and static compensators (STATCOM) have been widely used in industrial applications. Although the variety of MLI applications, there are several limitations have been discussed for topologies and control schemes. DC-MLIs, especially three-level structure, have a wide popularity in motor drive applications besides other multilevel topologies due to reducing THD with robust control of SHE-PWM control scheme. However, it would be a restriction of complexity and pre-defined switching angles when the level exceeds the three. The SPWM and SVM modulation techniques succeed this limitation of DC-MLI for higher level topologies. Other applications of DC-MLI can be defined as active filters and STATCOM in high voltage grid interconnections. Table 10 illustrates the most appropriate control schemes with application matching according to selected multilevel inverter topology.

Table 10. The most appropriate control scheme and application matching diagram according to topologies.

Topology	Control scheme			Application			
	SHE-PWM	SPWM	SVM	Motor drive	Active filters	PV, fuel cells	STAT COM
DC-MLI	✓✓	✓	✓	✓✓	✓	✓	✓
FC-MLI	✓	✓	×	✓	✓	×	×
CHB-MLI	×	✓✓	✓	✓✓	✓✓	✓✓	✓✓
H-MLI	×	✓✓	×	✓	✓	✓	✓
AH-MLI	×	✓✓	✓	✓✓	✓	✓✓	✓

The sign of bolded check means the proper matching between topology and control scheme or topology and application. The plain checks have been used to emphasize that there are some studies given in the literature about these applications but does not provide proper solutions. The bolded double check shows the most appropriate selection, while the cross defines the undesirable matching about harmonic reducing or affectivity issues. The DCMLIs are efficient in fundamental frequency switching applications such SHE-PWM and SVM, but the SVM will cause to an increment on voltage and current THD in the increased number of clamping diode conditions.

The FC-MLI is the unique topology that requires the most switching and auxiliary devices to generate a staircase output voltage. The increment of level will cause to increase

auxiliary capacitor number and restrain the accurate charging and discharging control of capacitors, hence designer will be encountered with the requirement of a pre-charge controller system. Although these disadvantages, the most important advantages of FC-MLI topology are preventing the filter demand and controlling the active and reactive power flow besides phase redundancies. The FC-MLI topology is mostly used in motor drive and active filter applications with SHE-PWM or phase shifted PWM control methods.

The CHB-MLI has the least components for a given number of levels according to topologies discussed before. The CHB-MLI topology consists of a series of H-bridge cells to synthesize a desired voltage from SDCSs which may be obtained from batteries or fuel cells. All these properties of cascade inverters allow using various pulse width modulation (PWM) strategies to control the inverter accurately. CHB-MLIs have been previously designed for static VAR compensators and motor drives, but the topology has been prepared an interface with renewable energy sources due to using separate DC sources. There are numerous studies have been performed on CHB-MLIs for connecting renewable energy sources with grid and power factor correction. The SPWM control scheme is mostly being used in the control of CHB-MLI due to simplified design considerations according to SVM.

1.9 Passive filters.

PWM modulation techniques used in voltage source inverters produce many switching harmonics in the grid current and produce not perfect sinusoidal waveforms that can affect the long-term performance of motor cables or inductors. This unperfect sinusoidal waveform produce voltage spikes on motor terminals caused by the dv/dt during switching transition, it also causes reflections in the cable which can led to cause the motor terminal voltage to see double the voltage tap and they can also produce additional losses (Steinke & Juergen, 1999).

in the past years harmonic distortion and these problems mentioned before have been dealt with the use of passive filters, the problem with this type of filters is that for harmonic reduction they may result in parallel resonances with the network impedance, overcompensation of reactive power at fundamental frequency, and poor flexibility for dynamic compensation of different frequency harmonic components.

Passive filters are those built using passive components, those which are not able to produce energy of their own and they are only capable of dissipating energy like resistors or storing energy like inductors or capacitors.

The passive filter not only affects inverter harmonic injection but impacts on the harmonics produced by a coupled non- linear load (Ahmed, Khaled, Finney, Stephen, Williams & Barry, 2007). There are several techniques for controlling harmonic current flow, such as

magnetic flux compensation, harmonic current injection, DC ripple injection, series and parallel active filter systems, and static VAr harmonic compensation.

Passive harmonic filters are often used to reduce voltage harmonics and current distortion in distributed generation systems. The harmonic currents injected by a grid connected inverter can be classified as:

- Low frequency harmonics.
- Switching frequency harmonics; and
- High frequency harmonics.

Each category harmonic must be corrected and attenuated appropriately. The current harmonics generated, if injected into the grid, can cause the malfunction of sensitive apparatus connected to the same bus. Grid networks have harmonic standards that must be accomplished, these determine the level of current that can be injected to the grid, power filters job is to attenuate the harmonics to the specific levels.

The three main existing harmonic filter topologies for three-phase inverters are the following.

1.10 L-Filter

The attenuation of the basic inductor is quite low, by using this filter the switching frequency needs to be quite high in order to sufficiently attenuate the inverter harmonics.

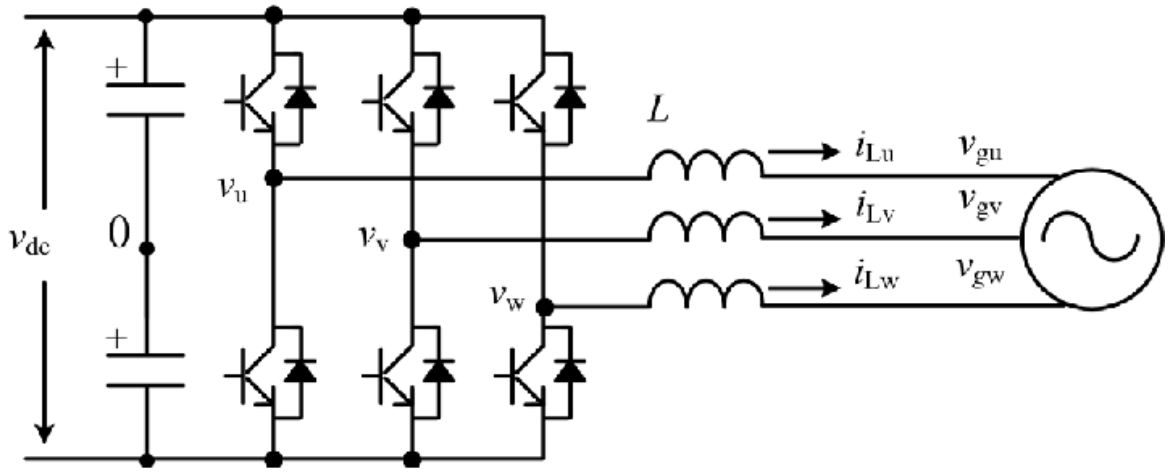

Figure 34. Traditional three phase grid connected inverter with L-Filter.

In order to see the performance of this filter configuration it will be analyzed with a distributed generation unit assumed to be operating in the grid connected mode, with the inverter connected to the grid network through a power filter.

Based on the equation (23) Fig. 35 shows the output power as function of DC link voltage and the coupling filter inductance (L-filter) between the inverter and the grid network.

$$P_0 = \frac{3V_g}{X_L}\sqrt{V_I^2 - V_G^2} \tag{23}$$

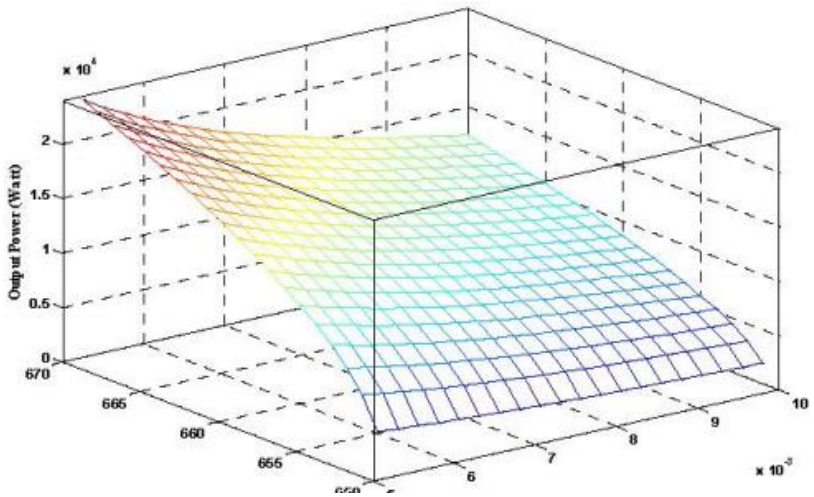

Figure 35. Output power as function of DC link voltage and inductor inductance.

The figure above shows that output power increases with increasing DC link voltage V_{DC} and decreasing filter inductance (L).

The aim of the filter inductance is to reduce the current harmonics injected into the grid. In Fig. 36a the first surface is the inductor harmonic current which is injected into the grid network while the second surface is the standard grid injected harmonic current limits. Both surfaces are calculated as a function of DC link voltage and the filter inductance, at a switching frequency of 10 kHz. Grid voltage V_g comprises only a fundamental frequency component and at other frequencies the network is a short circuit. Also, de grid network is assumed stiff, this means that the impedance is zero. The harmonic current expression is:

$$|I_{o\,har}| = \frac{|V_{I\,har}|}{X_{Lh}} \tag{24}$$

If harmonic order (h) is greater than 35, the harmonic currents injected to the grid network must be less than 0.3 %. L-filter cannot achieve the harmonic limit and this filter limitation can be seen in Fig. 36a. One solution could be to increase the switching frequency as shown in Fig. 36b.

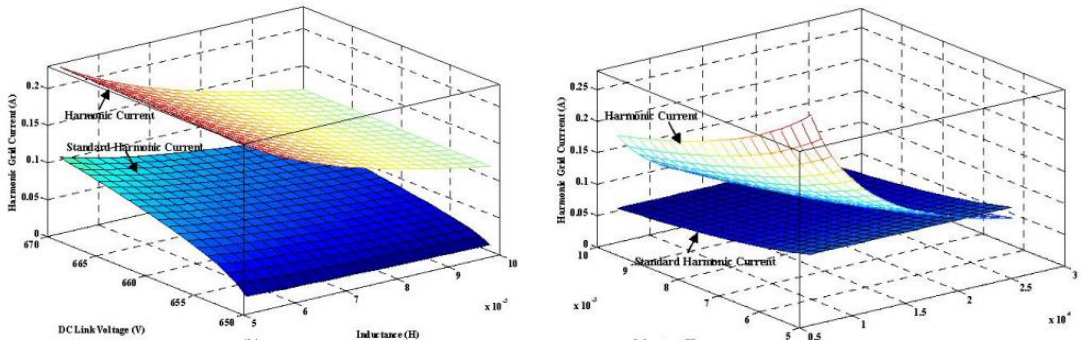

Figure 36. (a) harmonic current as function of DC link voltage and inductor inductance (b) harmonic current as function of switching fequency and inductor inductance**.**

1.11 LC-Filter.

LC-filter is a second order filter giving medium attenuation. Since the L-filter achieves low attenuation of the inverter switching components, a shunt element is needed to further attenuate them. This shunt component must be selected to produce low reactance at the switching frequency. The element must present a high magnitude impedance within the control frequency. A capacitor is used as the shunt element. Resonant frequency is calculated as in equation (25).

$$f_0 = \frac{1}{2\pi}\frac{1}{\sqrt{LC}} \tag{25}$$

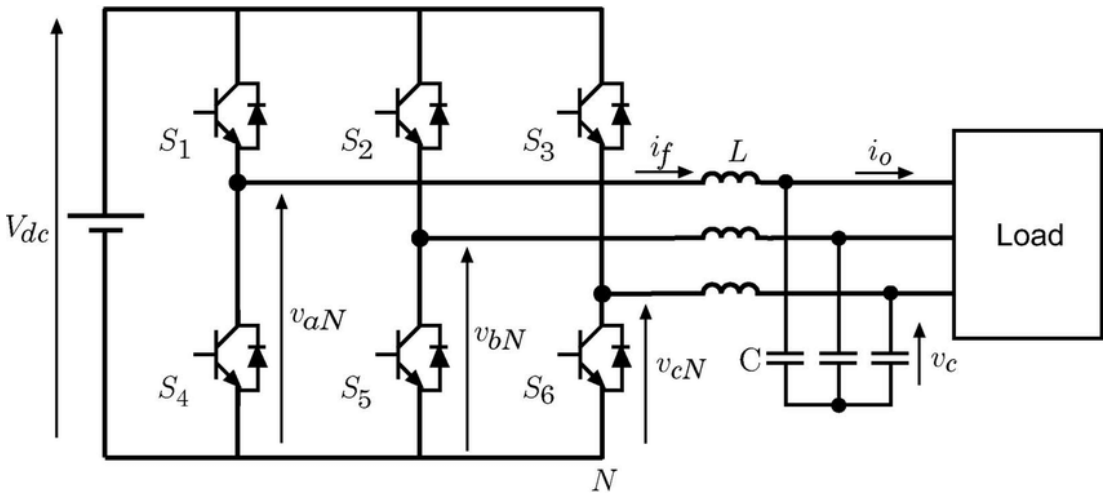

Figure 37. Three-phase inverter with output LC filter

All problems mentioned before can be solved with an introduction of a LC-filter between inverter output terminals and the motor cables, nevertheless LC-filters introduce some problems too. Resonance frequency must be eliminated and common mode voltages on motor

terminals against earth can exist, the introduction of the filter leads to increasing costs of the inverter and additional losses inside the inverter are generated.

In order to achieve an almost sinusoidal motor voltage, the resonance frequency of the filter must be well below the lowest harmonic frequency of the inverter voltage resulting from PWM. With the objective to avoid additional resonance suppressing control, he resonance frequency has also to be well above the fundamental frequency of the inverter voltage. Frequencies need to be at least a factor of 10 between them to decouple the effects. For medium voltage applications the filter resonance will be always excited, and the motor voltage will contain a visible residue of harmonics resulting from PWM. the theoretical maximum of resonance frequency is therefore equal to one half of the switching frequency and simulations of a filter resonance damping control showed that is possible to damp resonant frequencies up to 80% of the theoretical maximum. In the case of a three-phase inverter pulse frequency is twice the switching frequency, therefore with an average of 600 Hz switching frequency, resonance frequencies up to 480 Hz are controllable.

The filter capacitor compensates a part of the reactive power of the motor. The filter choke adds reactive power. If the filter choke's inductance is kept as low as possible, more reactive power is compensated by the capacitor than generated by the filter choke. The resulting rms current of the inverter is smaller with filter than without filter in this case.

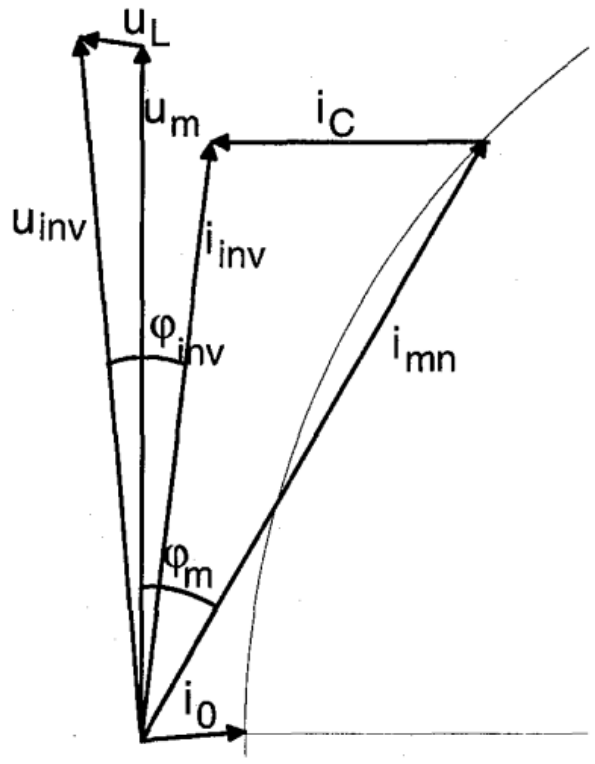

Figure 38. Vector diagram of motor and inverter current and voltage.

Fig. 38 shows the vector diagram of currents and voltages. The vectors of inverter, capacitor, rated motor and no-load motor current are i_{inv}, i_C, i_{mn} and i_0. The angle between motor voltage and motor current is φ_m, the angle between inverter voltage and inverter current is φ_{inv}. To calculate the perfect value of the LC-filter the motor data is needed.

1.12 LCL-Filter.

LCL-filters produces a better attenuation of inverter switching harmonics that the other filters commented above. The main advantages of this type of filter are:

- Low grid current distortion and reactive power production
- High attenuation
- Possibility of using a relatively low switching frequency for a given harmonic attenuation.

The resonant frequency of the LCL-filter is given by:

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{L_1 + L_2}{L_1 L_2 C}} \tag{26}$$

An LCL filter can achieve reduced levels of harmonic distortion with lower switching frequencies and with less overall stored energy. On the other hand, the LCL filter may cause both dynamic and steady state input current distortion due to resonance.

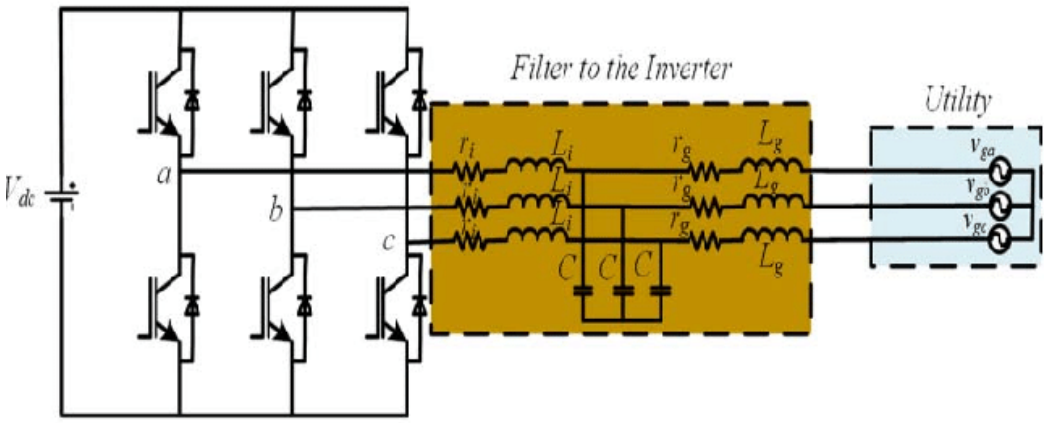

Figure 39. Three-Phase inverter with a LCL-filter.

One setback of LCL-Filters is that the require more complex current control strategies to maintain system stability and are more susceptible to interference caused by grid voltage harmonics because of resonance hazards and the lower harmonic impedance presented to the grid (Twining, Holmes & Grahame, 2003).

In most applications, an isolation transformer is used between the grid and the power filter. This provides leakage inductance, which is seen by the grid. To analyze this type of filter L_2 will have a constant leakage inductance on the output, it also will be equal to the leakage inductance of the isolated transformer.

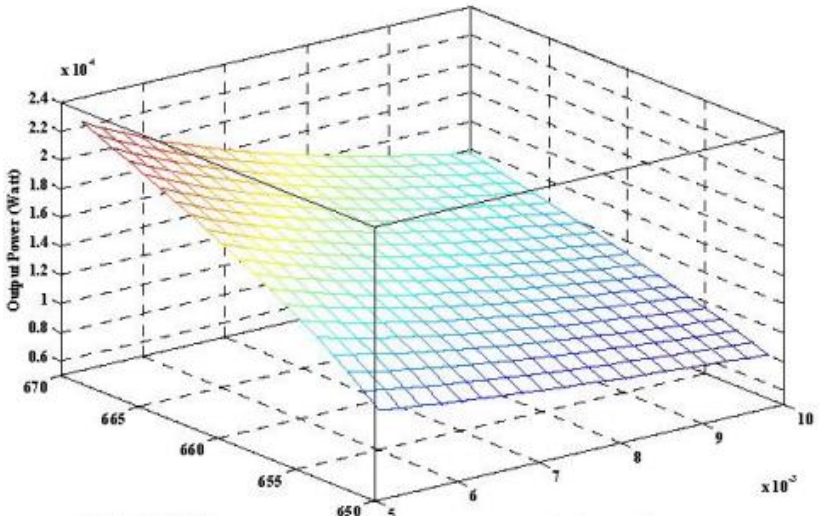

Figure 40. Output power as function of DC link voltage and inductor inductance.

Fig. 40 shows the output power as function of DC link voltage and inductor filter inductance, given by equation (27). The output power increases with DC link 670 voltage increase and decreasing filter inductance.

$$P_0 = \frac{3V_g}{X_{L1} + X_{L2} - \frac{X_{L1}X_{L2}}{X_C}} \sqrt{V_I^2 - V_g^2(1 - \frac{X_{L1}}{X_C})\text{^}2} \tag{27}$$

For a stiff grid, the output current harmonics injected are:

$$|I_{o\ har}| = \frac{|V_{I\ har}|}{X_{L1} - \frac{X_{L2}X_C}{X_{L2} - X_C}} \frac{X_C}{X_{L2} - X_C} \tag{28}$$

Fig. 41 shows the output grid harmonics and current harmonics limits as a function of DC link voltage and inductance (L_1). The switching frequency is 10kHz and comparing with LC-filter, it can be proved that LC-Filter with an isolated transformer can satisfy the harmonic limit requirements with a considerable margin.

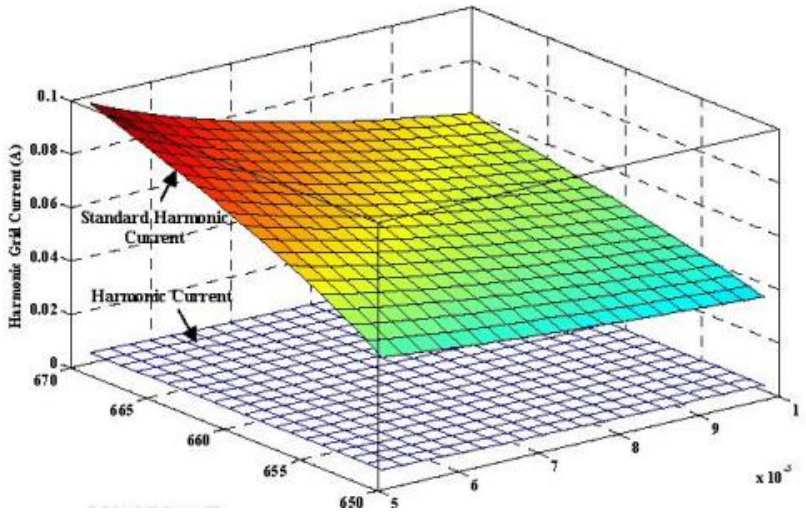

Figure 41. Harmonics current as fuction of DC link voltage and inductor inductance

In Fig. 42 we can see the harmonic grid currents and the harmonic injection limits into the grid network as a function of the switching frequency and inductance. The harmonic requirement can be achieved with a switching frequency greater than 3.5 kHz.

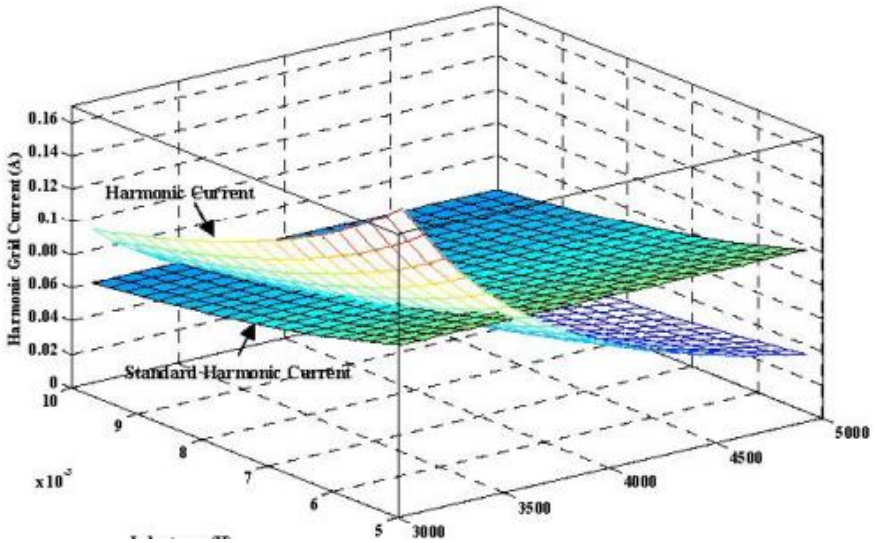

Figure 42. Harmonic current as function of switching frequency and inductor inductance.

A relationship between L_1 and C with constant output power, DC link voltage and isolated transformer inductance can be obtained from equations (29) and (30), where the desirable harmonic limits are considered. The required output harmonic limits can be achieved for a range of values of L_1 and C. Raising capacitance increases Var consumption and raises inverter harmonic currents while decreasing inductance raises the possible output power. Meanwhile, inductor harmonic content affects both the control system and the inverter rating.

$$X_{L1h} = \frac{1000V_g|V_{I\,har}|X_{Ch} + X_{L2}X_{Ch}P_0}{X_{L2h} - X_{Ch}} \qquad X_{Ch} = \frac{1}{2\pi(f_s - 2f_0)C} \qquad X_{L2h}$$

$$= 2\pi(f_s - 2f_0)L_2 \tag{29}$$

$$L_1 = \frac{1000V_g|V_{I\,har}|X_{Ch} + X_{L2}X_{Ch}P_0}{2\pi(f_s - 2f_0)X_{L2h} - X_{Ch}} \tag{30}$$

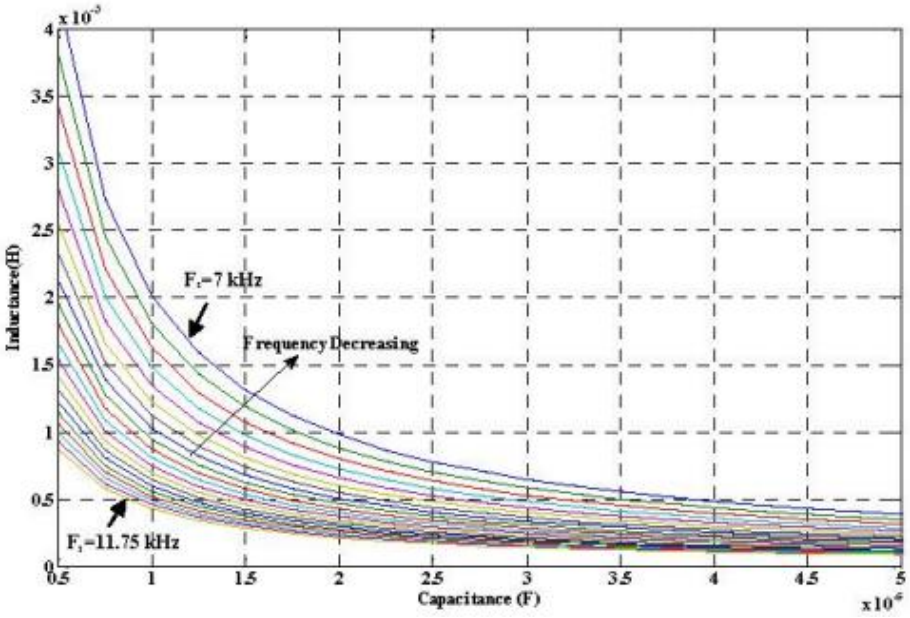

Figure 43. Inductance versus capacitance and frequency.

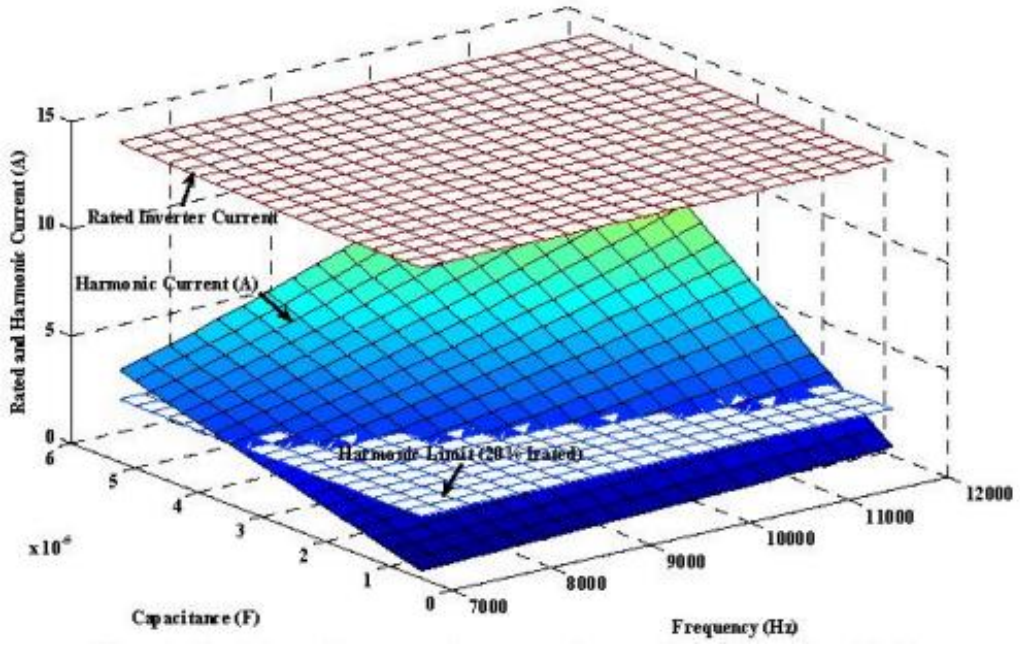

Figure 44. Rated and harmonic currents as a function of switching.

The inductor (inverter) current variation with capacitance and isolated transformer inductance is given by equation:

$$|I_{inv}| = \sqrt{\left(\frac{P_r}{3V_g}\left(1 - \frac{X_{L2}}{X_C}\right)\right)^2 + \left(\frac{V_g}{X_C}\right)^2} \tag{31}$$

The fundamental inverter current does not depend on the switching frequency. The inductor harmonic current caused by the inverter switching $(f_s - 2f_0)$ is given by:

$$|I_{inv\ har}| = \frac{V_{I\ har}}{X_{L1h} - \frac{X_{L2h}X_{Ch}}{X_{L2h} - X_{Ch}}} \tag{32}$$

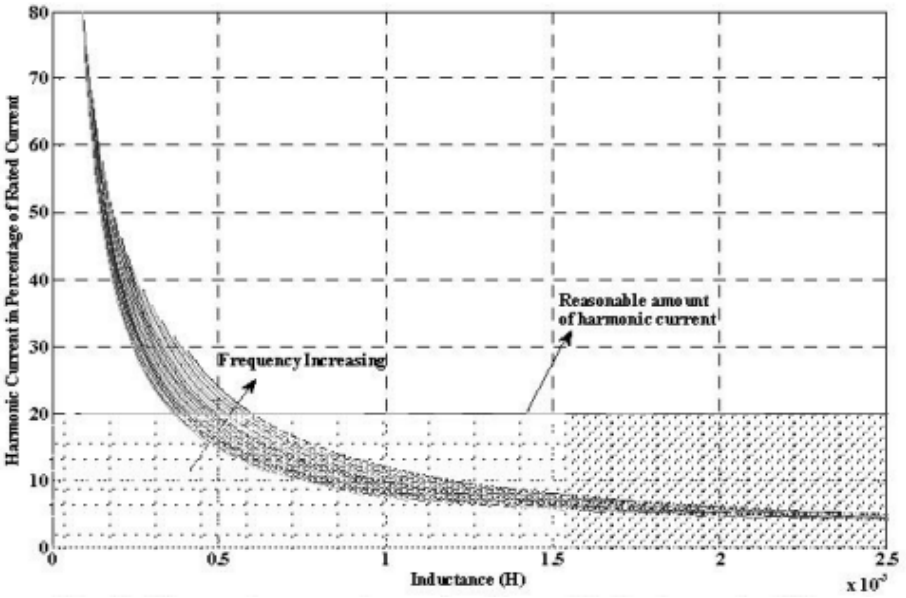

Figure 45. Harmonic current as a function of inductance at different.

1.13 Active power filters.

The electrification of the economy and the growing number of renewable energy plants has produced a great impact on the quality of electric supply and the grid network. Increasing domestic loads and more usual high power industrial loads cause disturbance in the distribution grid and harmonics in the network voltages. At the same time this equipment causing all the problems and disturbance is very sensitive to deviations from the ideal sinusoidal waveform. Eventually, power quality problems are created by the consumer itself. Moreover, in the last years the growing concern related to power quality comes from:

- proliferation of load equipment with microprocessor-based controllers and power electronic devices which are very sensitive to different types of power quality disturbances.

- Awareness of consumers that are getting more concerned about the power quality issues motivated to increase electrical efficiency.
- Emphasis of improving overall productivity and the durability of the equipment which has led to the installation o high-efficiency products, such as adjustable speed drives and power factor correction equipment. Eventually this turn has resulted in a increase in harmonics injected into the grid network causing concern in the system.

For an increasing number of applications, conventional methods like passive filters may result in parallel resonances with the network impedance, overcompensation of reactive power at fundamental frequency, and poor flexibility for dynamic compensation of different frequency harmonic components.

All these problems have led to develop dynamic and adjustable solutions to the power quality problems. This equipment is known as active filters. The advantage of this type of filters are that they are able to compensate reactive power, compensate current and voltage harmonics, suppress flickers regulate terminal voltage and improve voltage balance in three-phase systems. This type of filtering instantly adapts to changes in the network and load fluctuations and they can compensate several harmonic orders. Another important advantage is that they take much less time compared to traditional methods. Active filters maintain their performance with the load and can apply additional gain to the signal.

1.14 Types of active power filters.

Active power filters can be classified according to power rating and speed response, the type of converter, scheme, topology and compensation characteristics among others. Nevertheless, Fig. 46 shows the classification according to power rating and speed response, these two play a major role in deciding the control philosophy to implement the required filter. They also follow a reciprocal relationship. In general, the cost of any particular system is proportional to the required speed of response (El-Habrouk, Darwish & Metha, 2003).

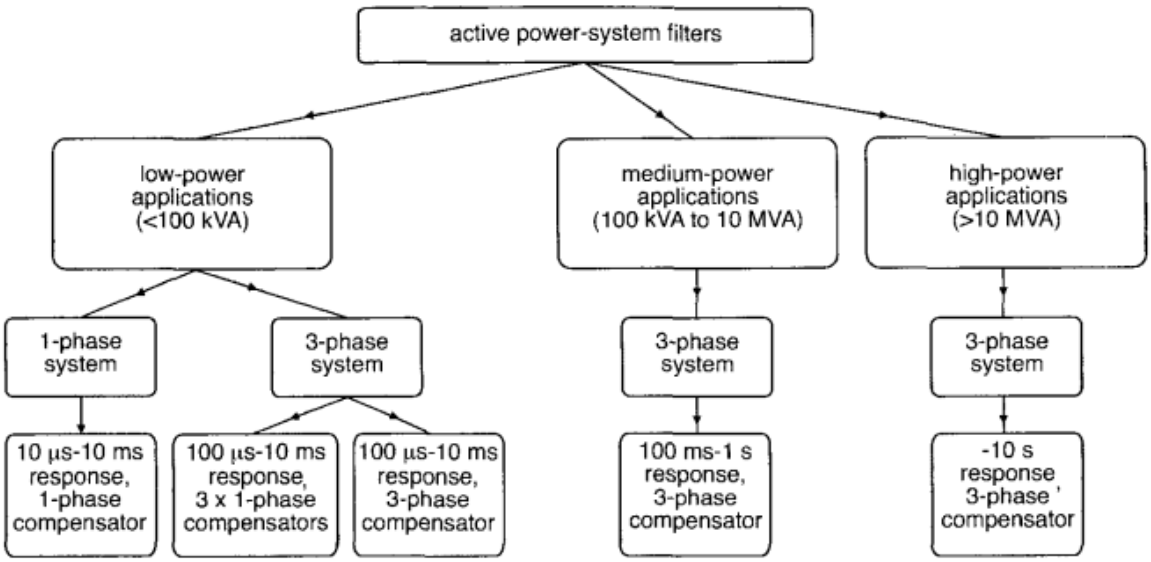

Figure 46. Suhdivison of power system filters according to power rating and speed of response.

The most popular classification is based on the topology such as shunt, series, or hybrid. Hybrid configuration is a combination of the other two. These different configurations are shown in Fig. 47.

Sunt active power filters (Fig 47.a) are widely used to compensate reactive power, current harmonics and load current unbalanced. It can also be used as a static var generator in power system networks for stabilizing and improving voltage profile. Meanwhile series active power filters (Fig 47b) are connected before the load in series with the ac mains using a coupling transformer with the aim to eliminate voltage harmonic and to regulate and balance the terminal voltage of the load of the line. Hybrid configurations is ideal for the compensation of high-power systems because the rated power of the active filter is significantly reduced since the major part of the hybrid filter consists of the passive shunt LC filter used to compensate lower order current harmonics and reactive power at fundamental frequency.

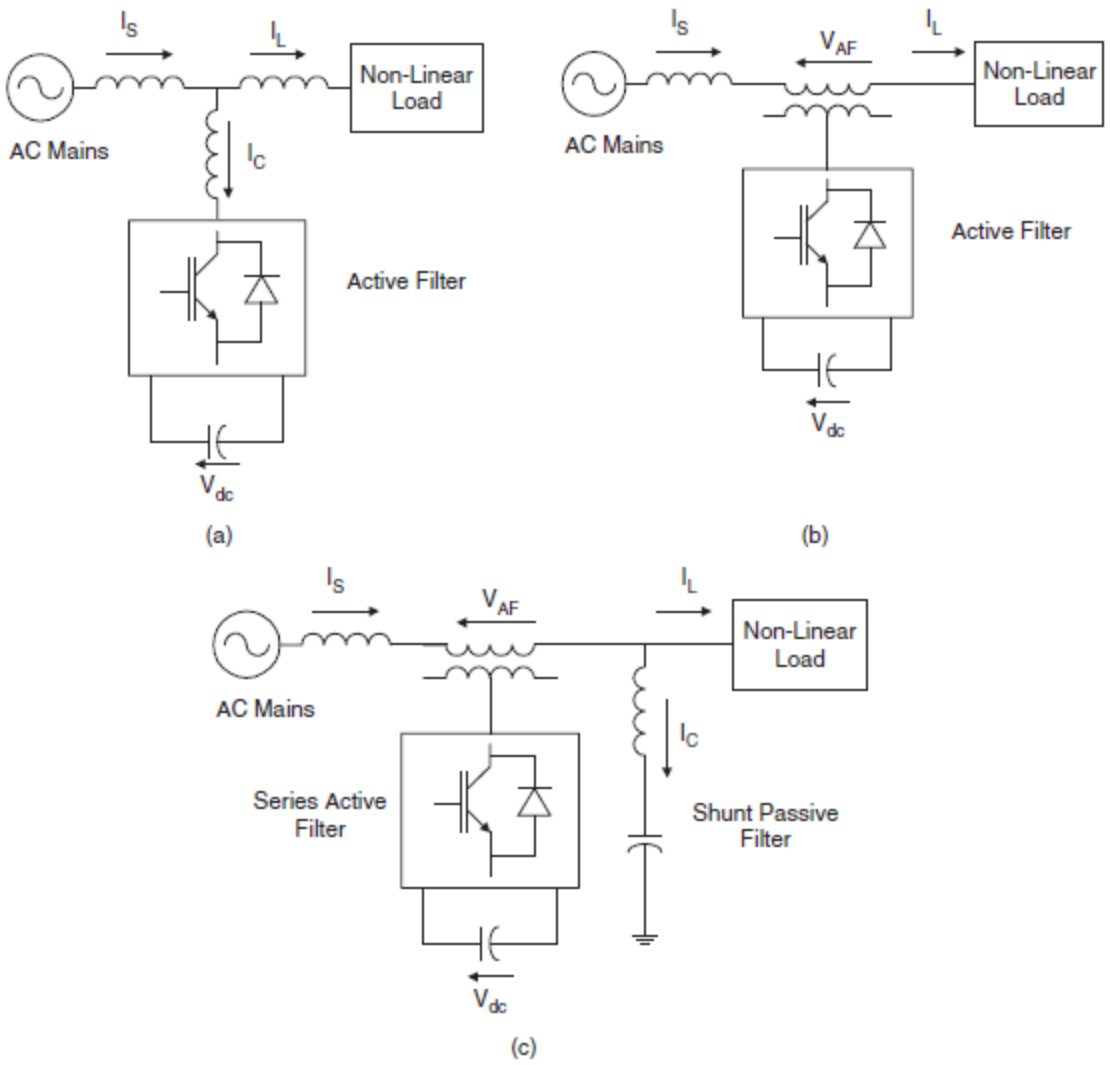

Figure 47. Active power filter topologies implemented with PWM-VSI: (a) shunt active power filter; (b) series active power filter; and (c) hybrid.

1.15 Shunt active power filters

Shunt active power filter is a most eminent filter among other types of power conditioning filters, which is used to cancel out current harmonics. In order to make, load current to be sinusoidal, SAPF generate the compensating current of 180 degree out of phase with same magnitude of the harmonic currents (Singh, 2018). This method is applicable to any type of load considered as a harmonic source.

Furthermore, the active power filter with an appropriate control scheme is able to compensate the load power factor. Basic configuration of SAPF is shown in Fig. 48.

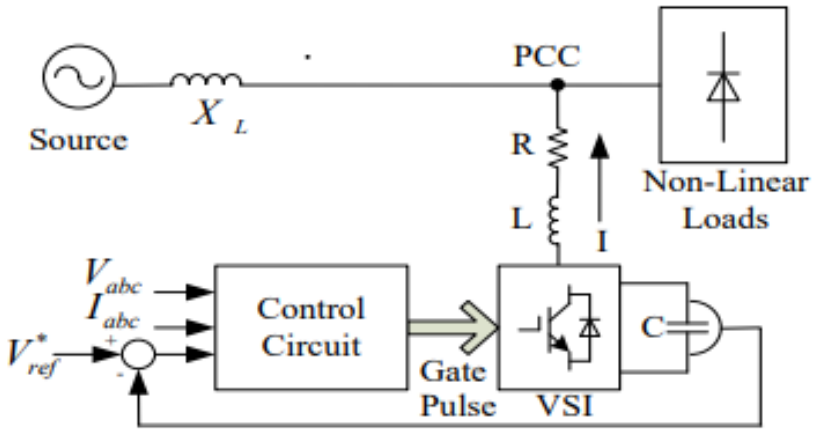

Figure 48. Compensation characteristics of a shunt active power.

1.15.1 Basic components of shunt active power filters.

- **Control circuitry**. Main functions of control circuitry are current control, voltage control and current reference generation. Current control is maintained thanks to artificial neural network, fuzzy logic and sliding mode controllers. Voltage control can be achieved with the help of PI and sliding mode control techniques. Current reference is generated with the mean of PQ theory Fourier transform, synchronous reference frame method and by applying various soft computing approaches.
- **Firing angle generator**. The goal of firing angle generator is to generate gate pulses for the operation of the VSI. The most likely used approaches for triggering of VSI switches are hysteresis controller, fuzzy logic controller and Pulse width modulation.
- **Voltage source Inverter**. Two levels PMW VSI is the most commonly type used ind SAPFs. In high power applications multilevel VSIs are used. THD in voltage and current waveforms of three levels VSI is quite lesser as contrast with two levels VSI. The performance of the mentioned VSI depends on various factor as the dimensions of energy storing elements, current control strategies, dc bus voltage and current reference generations techniques adopted.

1.15.2 Shunt active power filters control algorithms.

Control algorithms of SAPFFs are developed to operate SAPFs under the case of an ideal source voltage where this source is assumed to be sinusoidal and balanced. The main goal of SAPFs is to mitigate harmonic currents generated by nonlinear loads and a distortion-free source voltage is essential for SAPF operation. The angular position of the source voltage is usually taken as the reference to coordinate the phase of its output injection current, so it will

work in phase with the operating power system. Now we will discuss control algorithms applied to operate SAPFs (Hoon, 2017).

1.15.3 Harmonic extraction algorithm.

The extraction or detection of harmonic currents from the harmonic-polluted power line to generate the reference current signal ire f by using a harmonic extraction algorithm is deemed the first and the most important operation stage of a SAPF's control system. It is the first algorithm to operate in the controller, it extracts accurate and fast harmonic currents which result in proper and fast reference current generation which further controls the SAPF to efficiently reproduce the reference current signal i_ref as the desired injection current i_nj for harmonics mitigation.

Basically, the algorithm utilizes a signal-processing function known as distortion identifier which takes the distorted load current signal and generates a corresponding reference current signal ire f by isolating the distortion components from the fundamental component.

- **Time-Domain**. Time-domain harmonics extraction approaches are based on the instantaneous derivation of reference current signals from harmonic-polluted sources. They are considered as the simplest harmonic extraction approaches, offering increased speed and fewer calculations as compared to their counterparts in the frequency-domain and learning technique categories. In time-domain, the most widely applied algorithms are synchronous reference frame (SRF) (Hoon, Radzi, Hassan, Mailah & Wahab, 2016) and instantaneous power theory-based approaches (Hoon, Radzi, Hassan & Mailah, 2016).

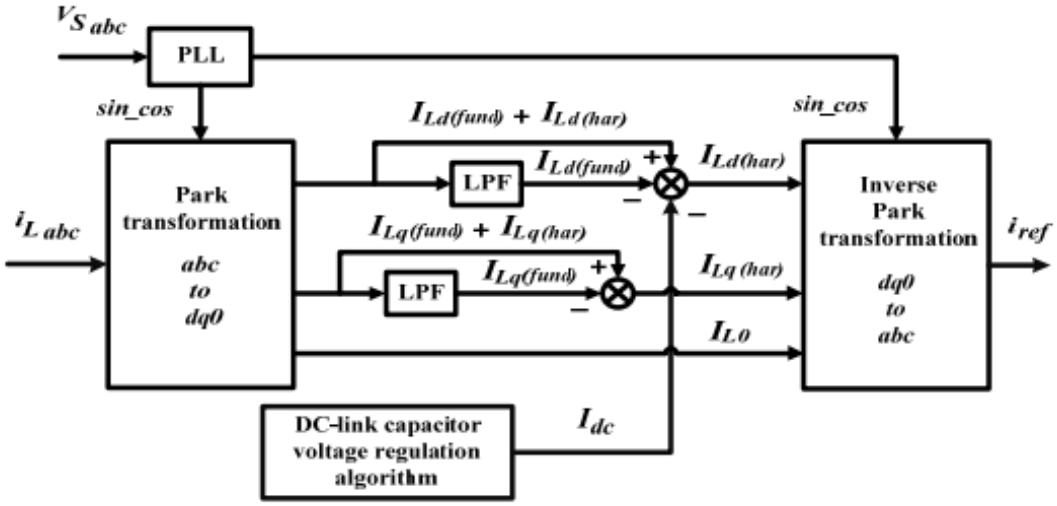

Figure 49. Control structure of a typical synchronous reference frame (SRF) algorithm

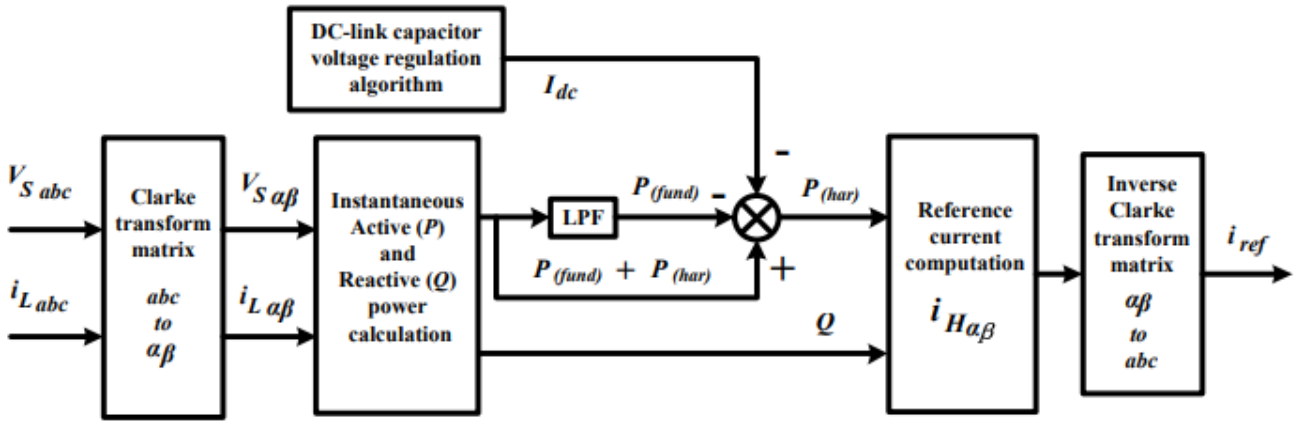

Figure 50. Control structure of a typical pq theory algorithm.

- **Frequency-Domain**. Frequency-domain harmonic extractions are based on Fourier analysis which involves either fast Fourier transform, or discrete Fourier transform of the distorted current signals. The desired harmonic components are splitted or isolated from the measured signals and then reconstructed back in the time-domain to generate reference current signals. Frequency-domain approaches are suitable for both single- and three-phase systems. The main disadvantage is that they require time to gather sufficient samples so that they can be processed in Fourier analysis. A good and fast control processor is needed.

- **Learning Techniques**. The available techniques included in this category are artificial intelligence such as Genetic Algorithm (GA), optimization and artificial neural network (ANN). Optimization algorithms have been applied in switched capacitor active filters to extract the harmonic components which are directly used to generate the switching pattern of the reference current. GA has been incorporated to improve the convergence time, but these techniques are difficult to implement. ANN is applied to learn the characteristics of the harmonic-polluted distribution system so that a suitable reference current signal can be set to achieve an allowable level of harmonic distortion in the distribution system.

1.15.4. DC-Link Capacitor Voltage Regulation Algorithm.

Another important control stage of a SAPF's control system is to ensure constant voltage at DC side of the power converter via a DC-link capacitor voltage regulation process. Generally, DC-link capacitor voltage regulation is related to a voltage source inverter-based SAPF configuration where a DC capacitor is usually installed for energy storage. The voltage should remain constant in an ideal case, with no real power exchange between the SAPF and the AC network. However, this condition is not possible in practical environments due to power losses in the power converter as a result of conduction and switching activities. Therefore, DC-link capacitor voltage regulation is crucial in maintaining a constant voltage across the DC-link capacitor, and it must be maintained at a level which is high enough so that the SAPF is able to precisely inject the desired injection current i_{inj} back into the harmonic-polluted power system.

Basically, DC-link capacitor voltage is regulated by controlling the real power drawn by the SAPF throughout its switching operation. The voltage regulation process is said to have accomplished when the real power drawn by the SAPF is made equal to its switching losses. Therefore, in order to constantly the maintain proper function of SAPFs, the magnitude of the generated reference current i_{ref} must be suitably adjusted by manipulating the magnitude I_{dc} of a control variable known as instantaneous DC-link charging current signal i_{dc}.

1.15.5. Current control algorithm.

Final control stage of SAPFs control system is the generation of switching pulses by means of the current control (switching) algorithm to stablish an adequate switching of power switching devices, so that the desired reference current signal i_{ref} can be reproduced as the injection i_{inj} for harmonics mitigation. The current control harmonic works tracking and comparing feedback controlled current to a specific reference current signal i_{ref}. At the same time i_{dc} is taken to adjust the magnitude of i_{ref} accordingly, so that appropriate real power can be drawn by the SAPF to regulate its potential losses. All existing current control algorithms can be grouped into two major operation schemes known as direct current control (DCC) and indirect current control (ICC) schemes.

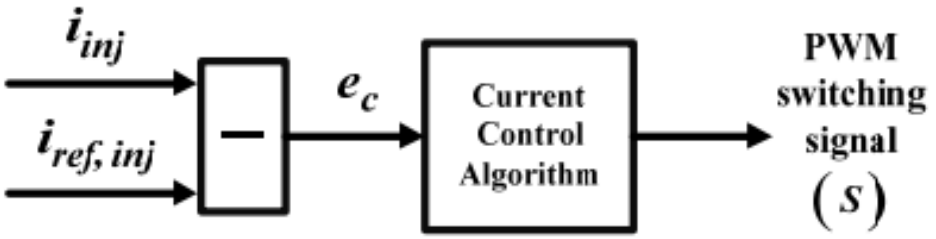

Figure 51. Conceptual model of direct current control (DCC) scheme.

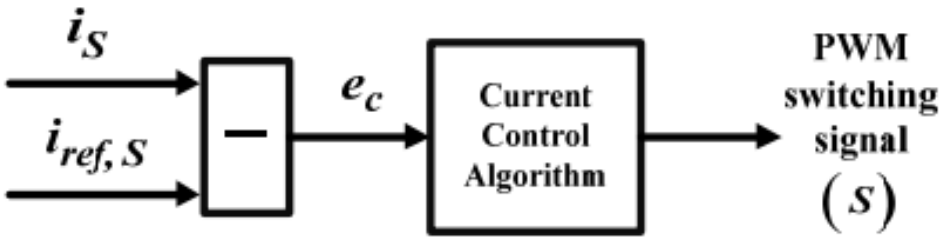

Figure 52. Conceptual model of an indirect current control (ICC) scheme.

1.16 Series active power filters.

Series active power filters operate principally as a voltage regulator and harmonic isolator between the non-linear load and the utility system. This type of filter is more adequate to protect the consumer against a malfunction of the supply voltage quality. It is recommended for voltage distortion, compensation of voltage unbalances and voltage sags from the ac supply. It is specially recommended for low power applications because it is more economically than UPS, since no energy storage is necessary. The series active power filter injects a voltage component in series with the supply voltage and therefore can be regarded as a controlled voltage source.

If passive LC filters are connected in parallel to the load, the series active power filters operate as an harmonic isolator forcing the load current harmonics to circulate mainly through the passive filter rather than the power distribution system. The main advantage of this scheme is that the rated power of the series active power filter is a small fraction of the load kVA rating, typically 5%. A drawback is that the rated apparent power of the filter may increase too, in case voltage compensation is required.

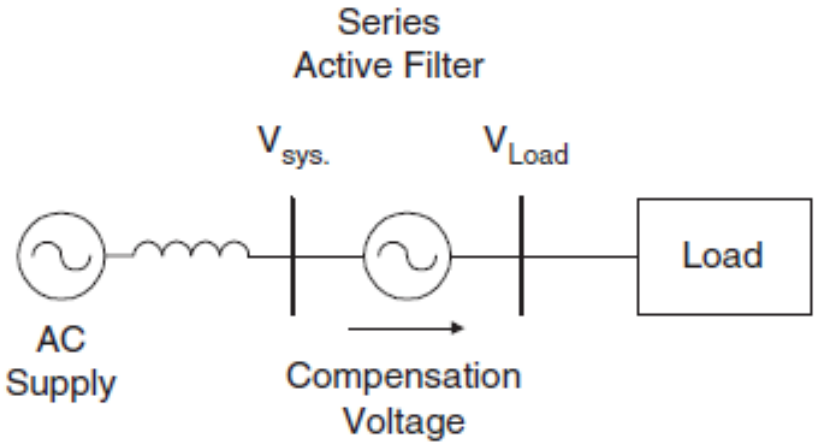

Figure 53. The series active power filter operating as a voltage compensator.

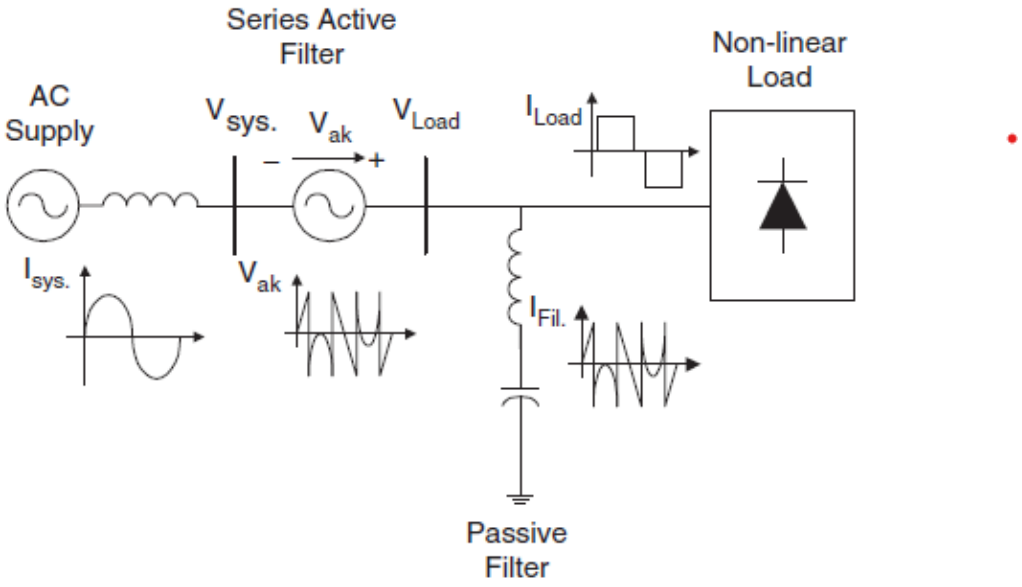

Figure 54. Combination of series active power filter and passive filter for current harmonic compensation.

The pulses for the series active filter are generated with help of power vectorial theory which connects and regulate the unbalance voltage in three-phase system. Fig. 55 shows the schematic diagram of series active filter which is made of a three-phase PWM VSI injecting compensation voltage through three separates transformers. Afterwards the output of inverters is connected to a second order filter which helps to eliminate the high frequency created by the high switching action of the inverter. The secondary winding of each transformer is connected in series with each phase of the power supply (Kumar, Kalyanapu & Ilango, 2014).

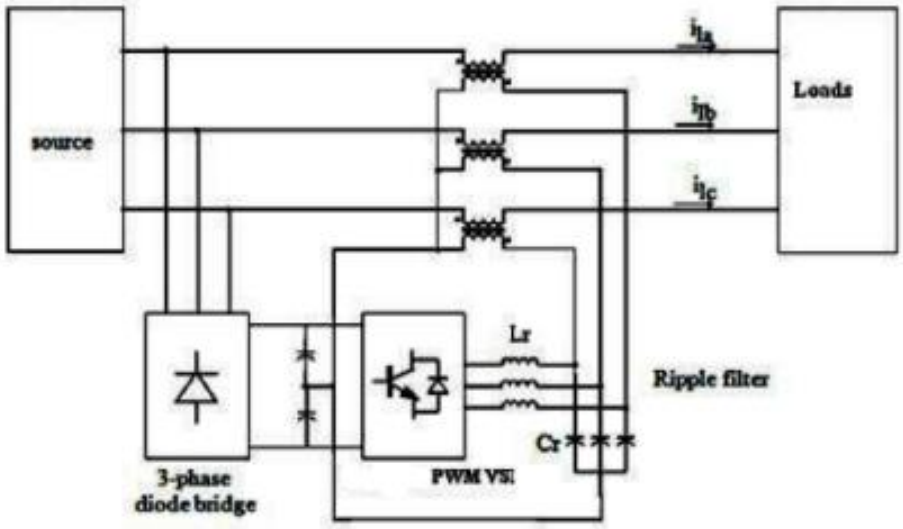

Figure 55. The series active power filter topology**.**

1.16.1 Control algorithm.

As mentioned before this type of filter is used to eliminate the voltage unbalance and harmonics. Different types of control methods are used to control the series filter. Using one or another determine the accuracy and the speed of the response of the filter. Fig. 54 shows one of the most typical algorithms known as power vectorial theory, which is mainly used for voltage unbalance compensation.

If the active filter presents an infinite impedance, then the compensation characteristic becomes ideal. In Fig. 55 the passive LC filter connected in parallel with the load is turned to eliminate the fifth and seven harmonics. For the fundamental harmonics, the passive filters also must supply the reactive power of the load. The active filter must generate a voltage proportional to the harmonic component of the source current, calculated applying the vectorial theory of the electric power. The reference current is calculated as follows (Peng, Akagi & Nabae, 1988).

$$i_{ref} = i_1 - \frac{p}{v^2}V \tag{33}$$

Where i_1 is the current vector of the load and passive filter, p is the average power, V is the voltage vector before active filter v^2 is Norm of the voltage.

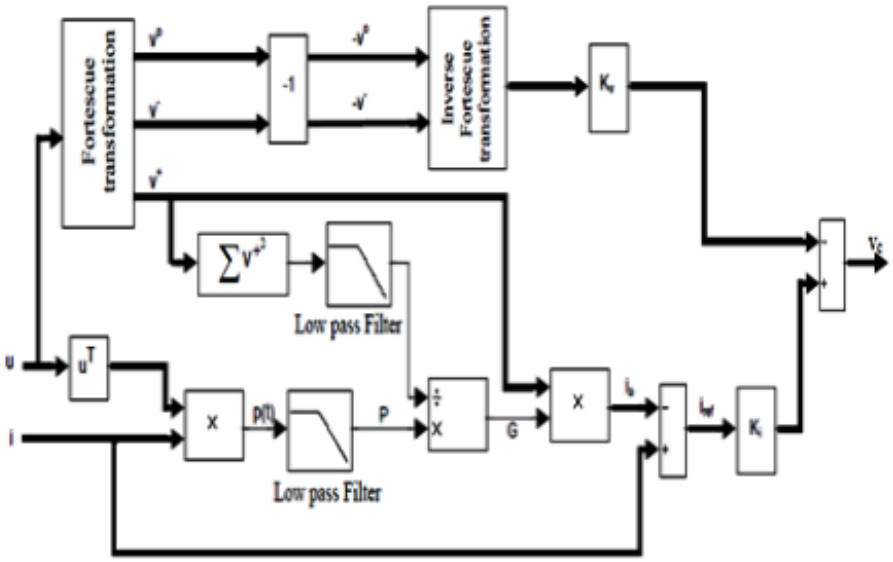

Figure 56. Control scheme for the series active filter.

The reference voltage to compensate the voltages unbalance is obtained by calculating the zero and inverse sequence components from eq. (34). The active filter must generate these components, but in reverse phase. Applying the inverse of the Fortescue transformation the following equations are obtained.

$$\begin{bmatrix} v_{ref\,a} \\ v_{ref\,b} \\ v_{ref\,c} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \begin{bmatrix} -v_{a0} \\ 0 \\ -v_{a0} \end{bmatrix} \tag{34}$$

Fig. 56 shows the control scheme for obtaining the reference signal. The voltage compensation signal is generated by the PWM inverter. The gain K_v is the turn ratio of the series transformers, which is applied to the reference signal for the voltage unbalance. The gain K_i is the proportional constant for the harmonics of the source current; it gets the magnitude od the impedance for high frequency. Thus, the inverter must generate compensation signal as follow as:

$$V_c = K_i I_{ref} + K_v V_{ref} \tag{35}$$

The gating signals of the inverter are generated by comparing the resultant reference signal with the output of the inverter through a bang-bang control.

1.17 Hybrid active power filters.

The combination of passive and active filtering through hybrid topology can significantly enhance the compensation properties of basic passive filters, making them a cost-effective solution for high-power applications. Furthermore, by connecting an active power filter in series with the passive filter, the compensation characteristics of the latter can be further

enhanced, adding more flexibility to the overall compensation process. The hybrid active filter configuration is illustrated in Fig. 57 where the active power filter is integrated with a three-phase PWM voltage-source inverter that operates at a fixed switching frequency and is connected in series with the passive filter through a coupling transformer. The active power filter enforces the utility line currents to become sinusoidal and in sync with their respective phase-to-neutral voltage, thus improving the compensation characteristics of the passive filter.

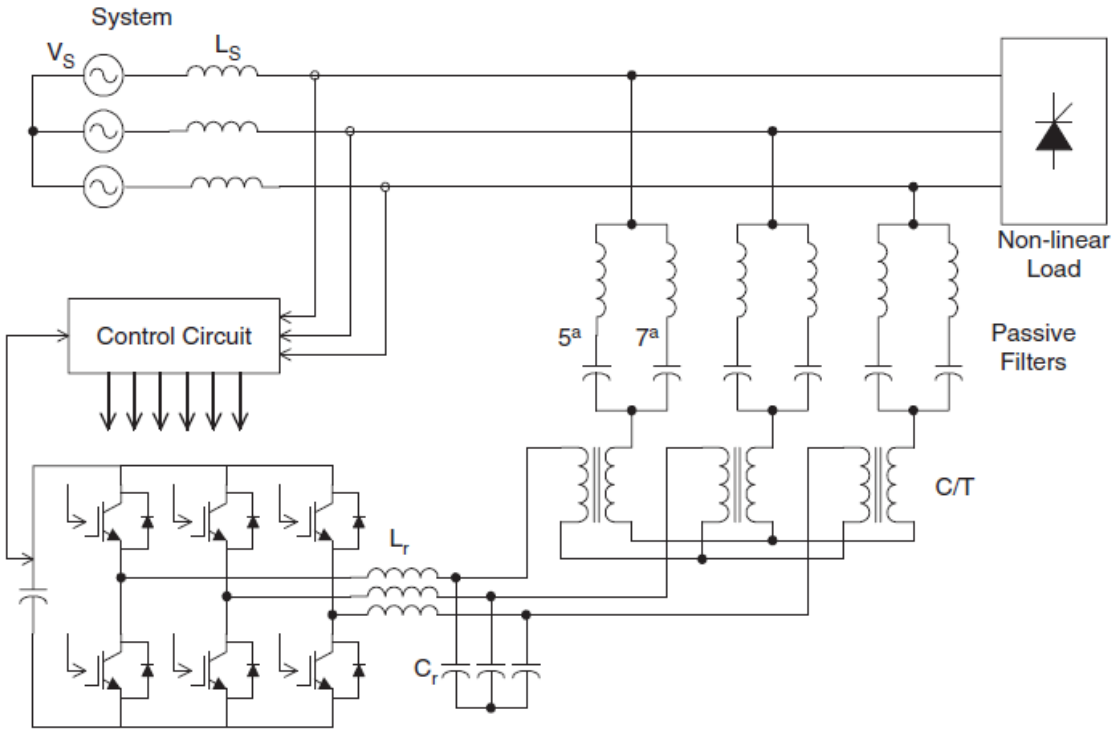

Figure 57. The hybrid active power filter configuration.

1.17.1 Control scheme.

As the active power filter is connected in series to the passive filter through a coupling transformer, it applies a voltage signal to the primary terminals, directing the current harmonics through the passive filter to enhance its compensation properties, irrespective of the alterations in the selected resonant frequency of the passive filter. The control structure proposed in Fig. 58 includes three modules: the dc voltage control, the voltage reference generator, and the inverter gating signal generator.

To generate the voltage reference waveform for the inverter control structure, a sinusoidal reference waveform in phase with the respective phase-to-neutral voltage is adjusted to the required amplitude and then subtracted from the corresponding ac Line current. This

sinusoidal reference signal can be obtained from the voltage system, and its amplitude controls both the inverter dc voltage and the ac mains displacement power factor. The inverter dc voltage varies with the amount of real power absorbed by the inverter, while the ac mains power factor depends on the amount of reactive power generated by the hybrid filter, which can be regulated by adjusting the amplitude of the fundamental component of the inverter output voltage.

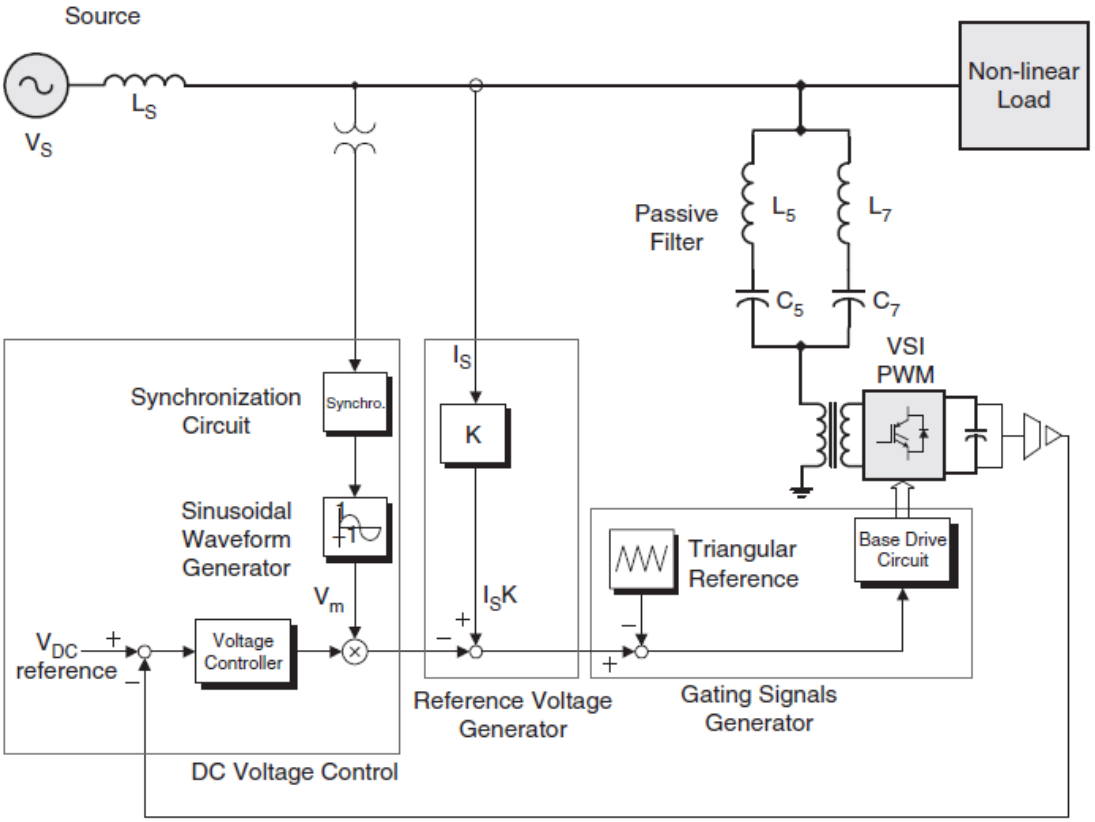

Figure 58. The hybrid active power filter topology and associated control scheme.

In the current harmonic compensation mode, the active filter improves the filtering characteristic of the passive filter by imposing a voltage harmonic waveform at its terminals with an amplitude value equals to:

$$V_{ch} = K * I_{Sh} \tag{36}$$

Where I_{Sh} is the harmonic content of the line current to be compensated, and K is the active power filter gain. If the ac mains voltage is purely sinusoidal, the ratio between the harmonic component of the non-linear load current and the harmonic component of the ac line current is obtained from eq (37)

$$\frac{I_{Sh}}{I_{Lh}} = \frac{Z_F}{K + Z_F + Z_S} \tag{37}$$

Equation above shows that the effectiveness of the hybrid topology (I_{Sh}/I_{Lh}) for filtering depends on the value of the passive filter's equivalent impedance, Z_F. Additionally, since the tuned factor, δ, and quality factor, Q, can alter the filter's bandwidth and harmonic equivalent impedance, their values must be chosen carefully to maintain the compensation effectiveness of the hybrid topology. Specifically, a high value of Q results in a larger bandwidth of the passive filter, thereby improving the compensation characteristics of the hybrid topology. Conversely, a low Q value and/or high tuned factor increase the required voltage generated by the active power filter, which is necessary to maintain the same compensation effectiveness.

This subsequently raises the active power filter rated power. Also, it needs to be noted that the factor K affects the THD of the line current, THD of the line current decreases if K increases.

In other words, the compensation of the hybrid filter improves as the active power filter generates larger voltage harmonic components. The compensation ability of the hybrid filter relies on the compensation characteristics of the passive filter. This means that the filter's impedance value and tuned frequency impact the active filter's rated power needed to meet the system's line current compensation needs. The correction of the displacement power factor can be accomplished by managing the voltage drop over the capacitor in the passive filter. To achieve this, a voltage at the fundamental frequency is produced at the inverter's AC terminals, with an amplitude equivalent to:

$$V_C = \beta * V_T \tag{38}$$

By utilizing the capacitive equivalent impedance of the passive filter at the fundamental frequency, control of the displacement power factor can be achieved. Altering the voltage imposed by the active power filter at the terminals of the passive filter capacitor can produce reactive power from the passive filter. The hybrid topology can generate or absorb reactive power at the fundamental frequency, depending on whether a positive or negative β is selected. This allows compensation for the leading or lagging displacement power factor of the non-linear load, which can be accomplished by manipulating the voltage across the passive filter capacitor.

2. PRACTICAL PART

In the following chapters some of the topologies and the control schemes explained before will be discussed, the circuits are done with the help of LTspice.

2.1 Half-Bridge VSI.

Fig. 59 shows the power topology of half-bridge VSI. It is obvious that both switches (Q_1 and Q_2) cannot be on simultaneously since it would produce a short circuit across the dc link voltage source. Switches are made with the bipolar transistor 2N3904 and a diode as a support.

The value of the components present in the circuit are:

$$R_1 = 10\Omega \quad L_1 = 100mF \quad V_1 = 25V \quad V_2 = 25V$$

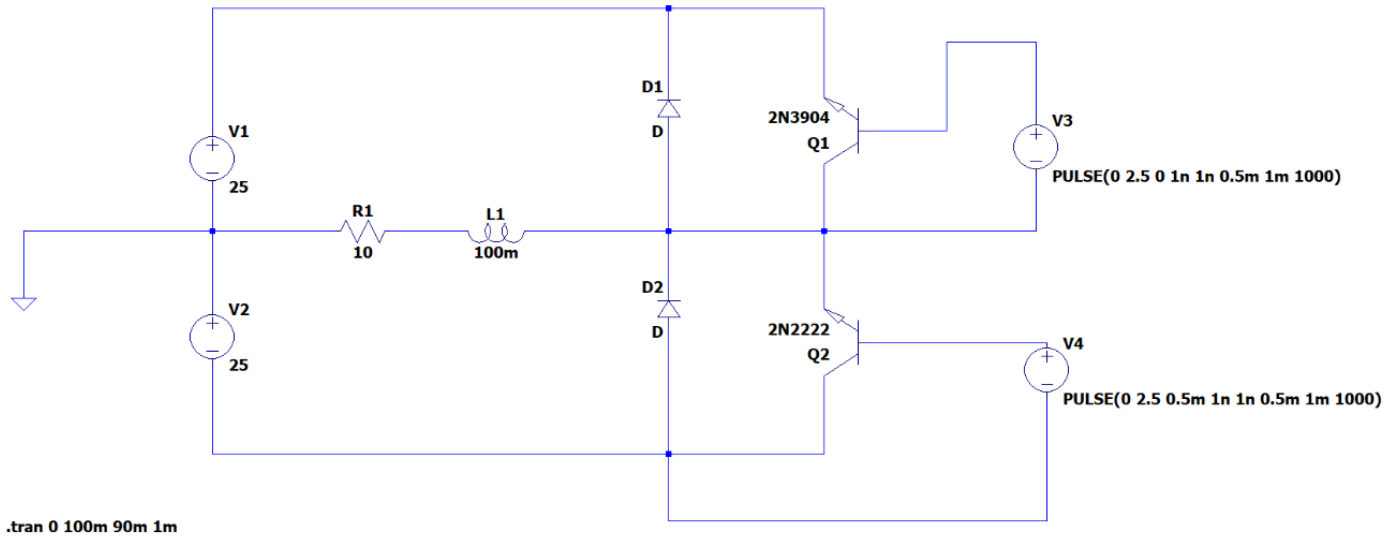

Figure 59. Single-Phase half bridge VSI.

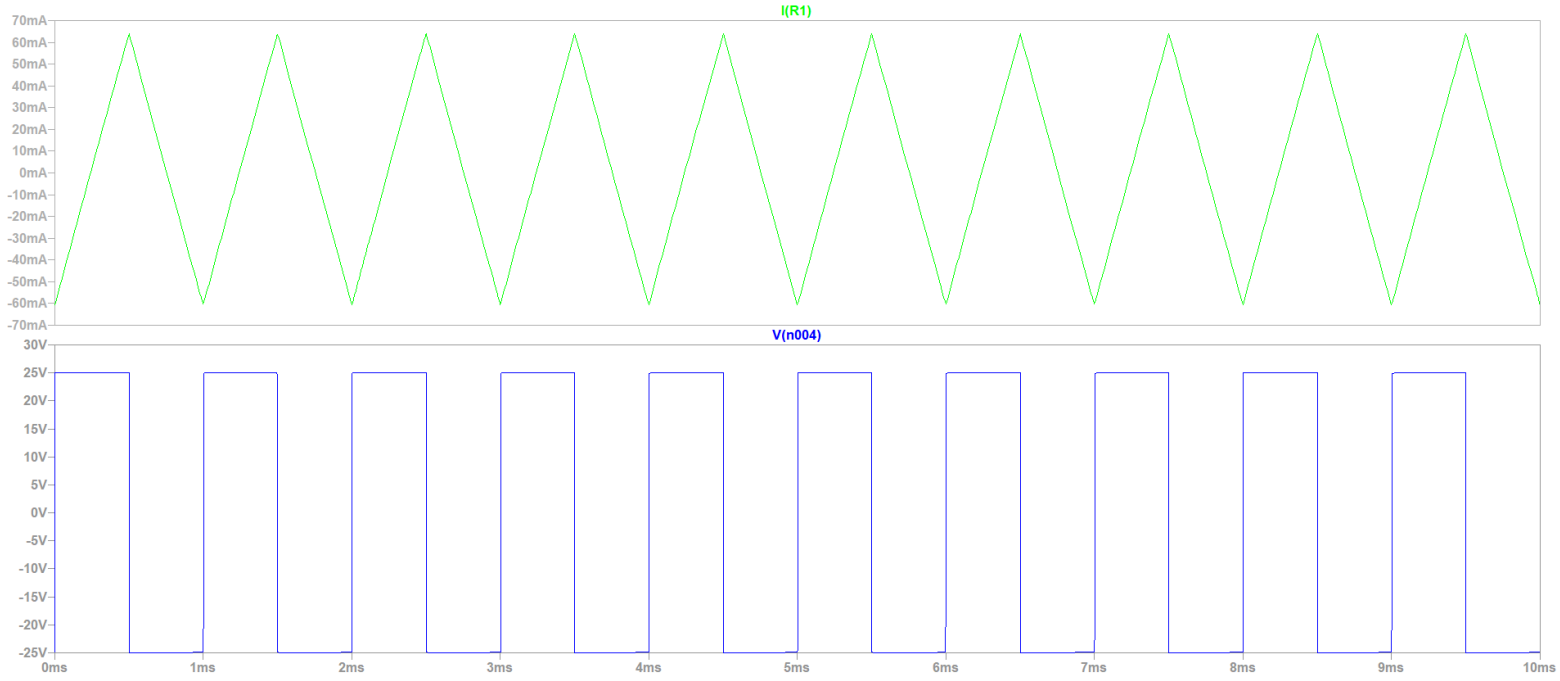

Figure 61. Current and voltage passing through the line.

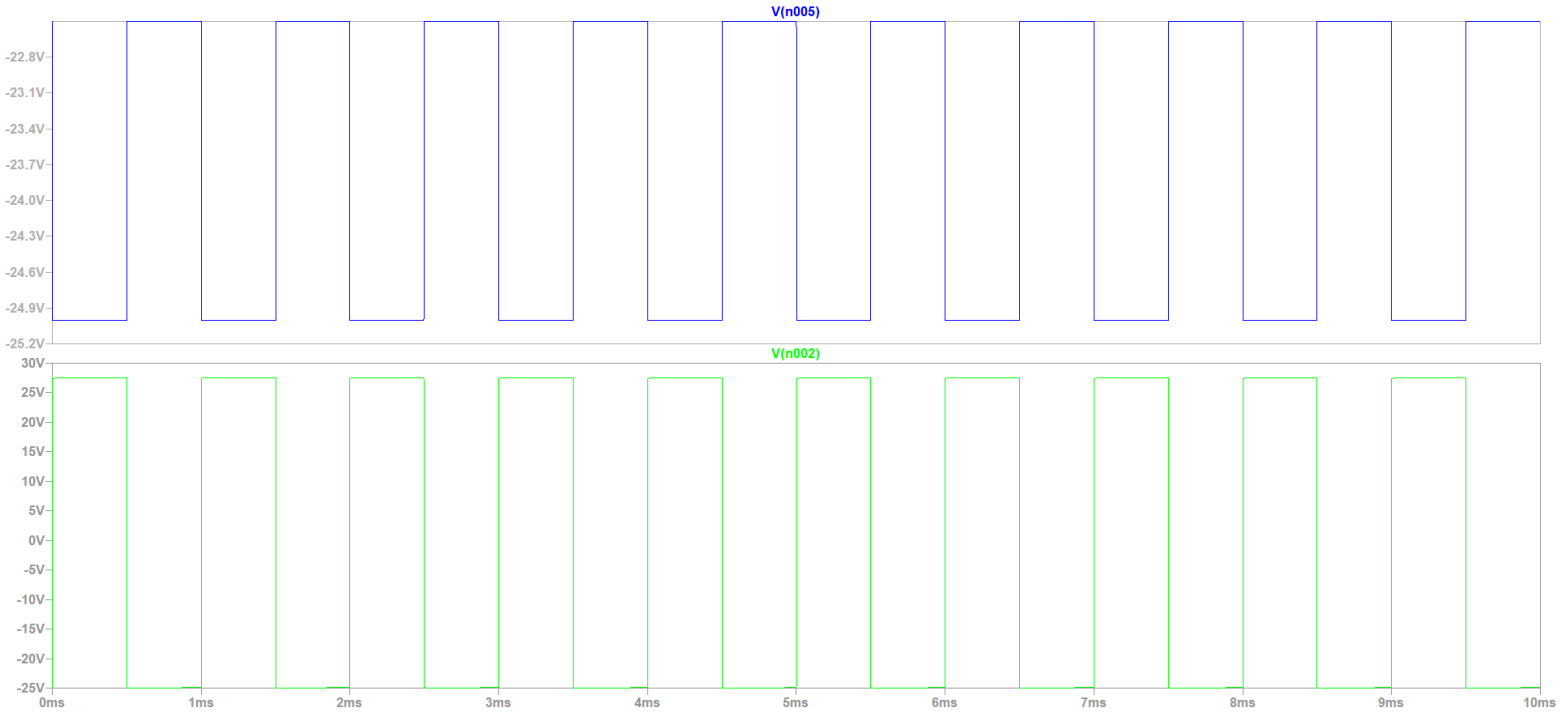

Figure 60. Voltage passing through the switches.

2.2. Full-Bridge VSI

Fig. 62 shows the power topology of a full-bridge VSI in LTspice. This inverter is quite similar to the half-bridge inverter, a second leg provides the neutral point to the load. As mentioned before all switches cannot be on because a short-circuit will be produced.

Switches are made with the bipolar transistor 2N3055 and a diode as a support. The value of the rest of the components are:

$$R_1 = 10\Omega \quad L_1 = 100mF \quad V_1 = 50V$$

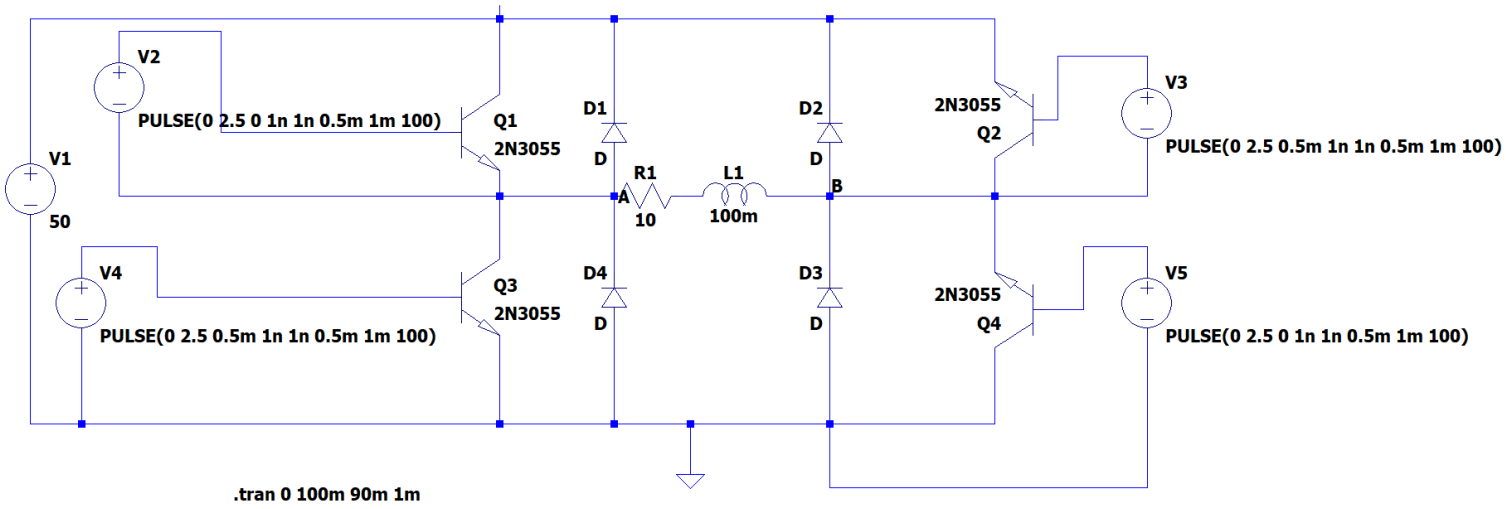

Figure 62. Single-Phase full bridge VSI.

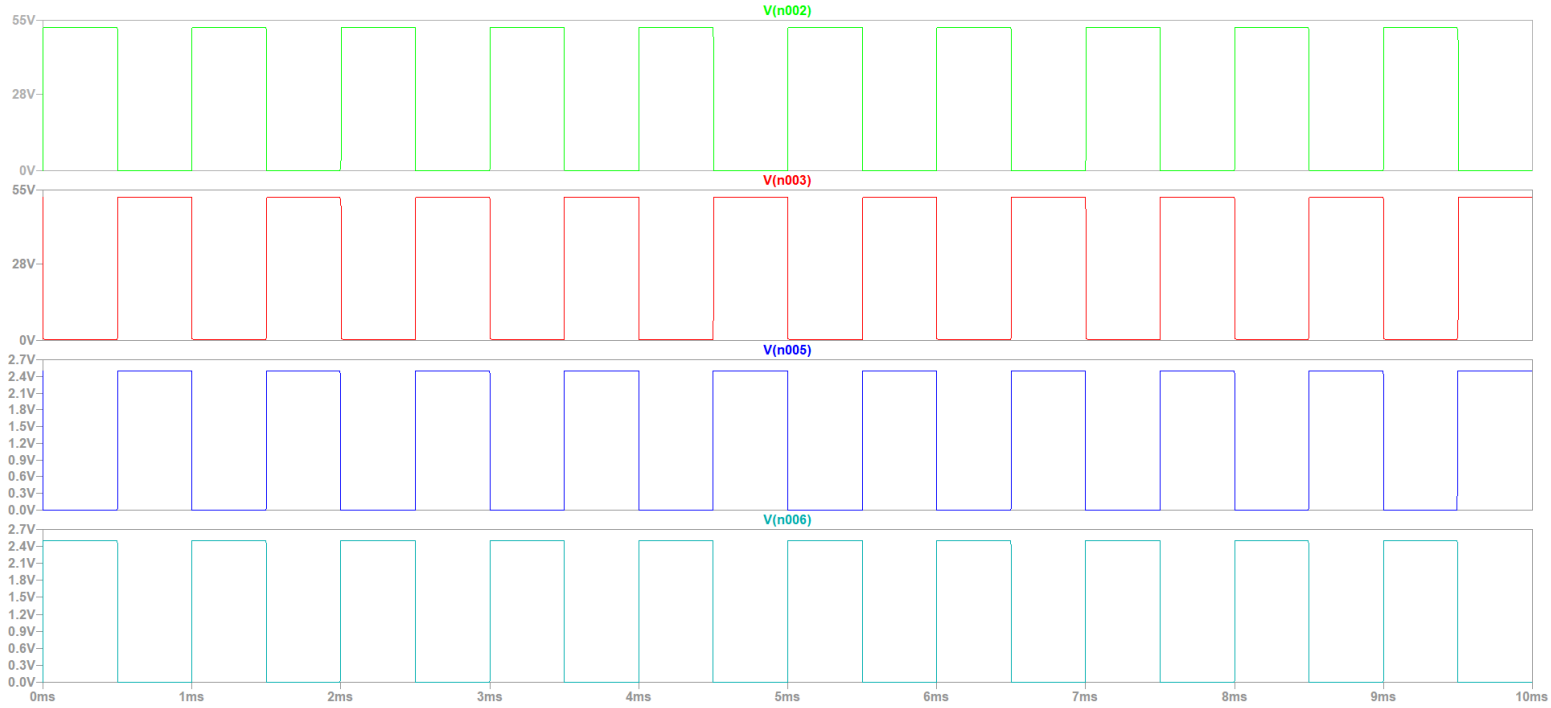

Figure 63. Voltage passing through the switches.

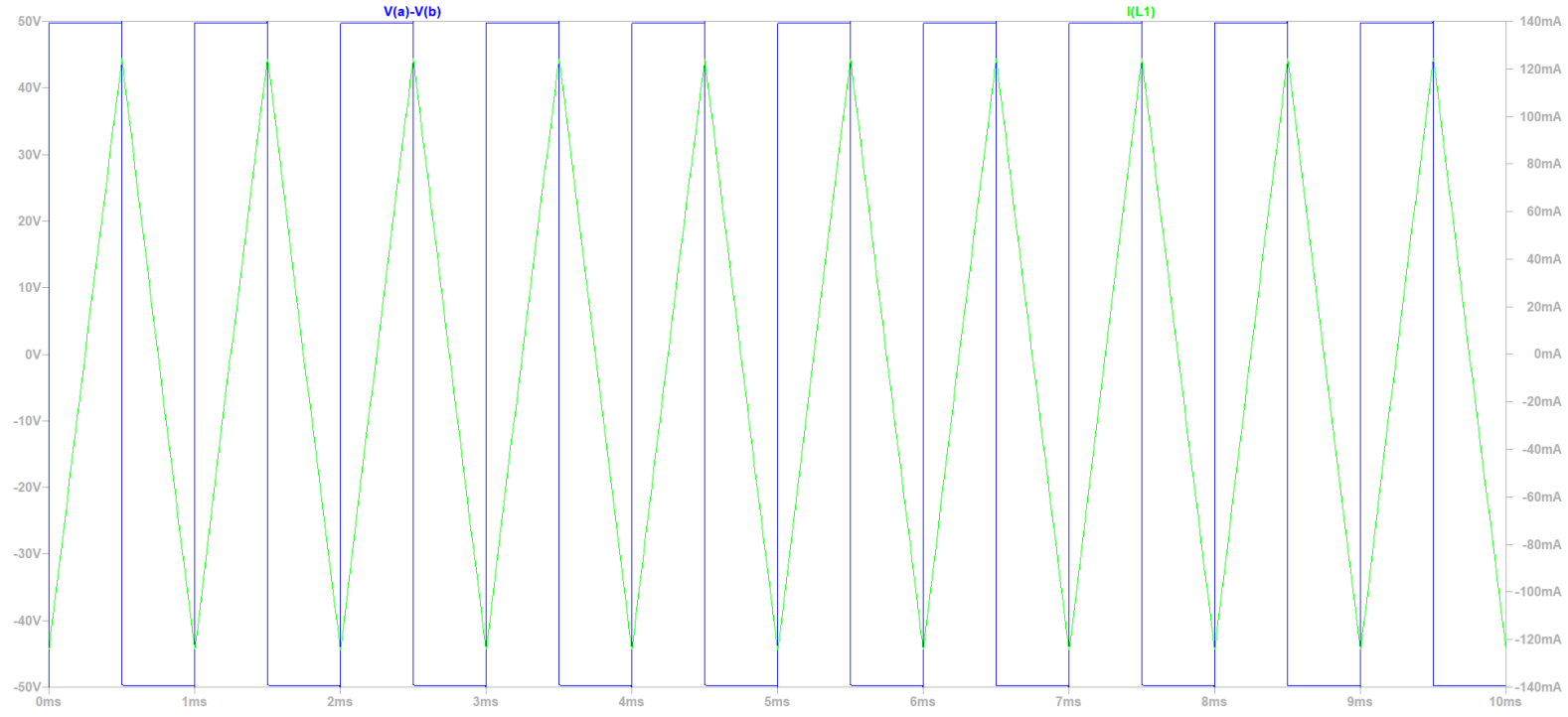

Figure 64. V(a)-V(b) and current passing through the line.

2.2.1. PWM Modulation technique.

In order to implement PWM modulation technique, another circuit has been made with LTspice. Switches are made with the Mosfet SPA11N60C3 and a diode as a support. The value of the rest of the components are:

$$V_{in} = 100\ V \quad R_1 = 100\ \Omega \quad L_1 = 100\ mF$$

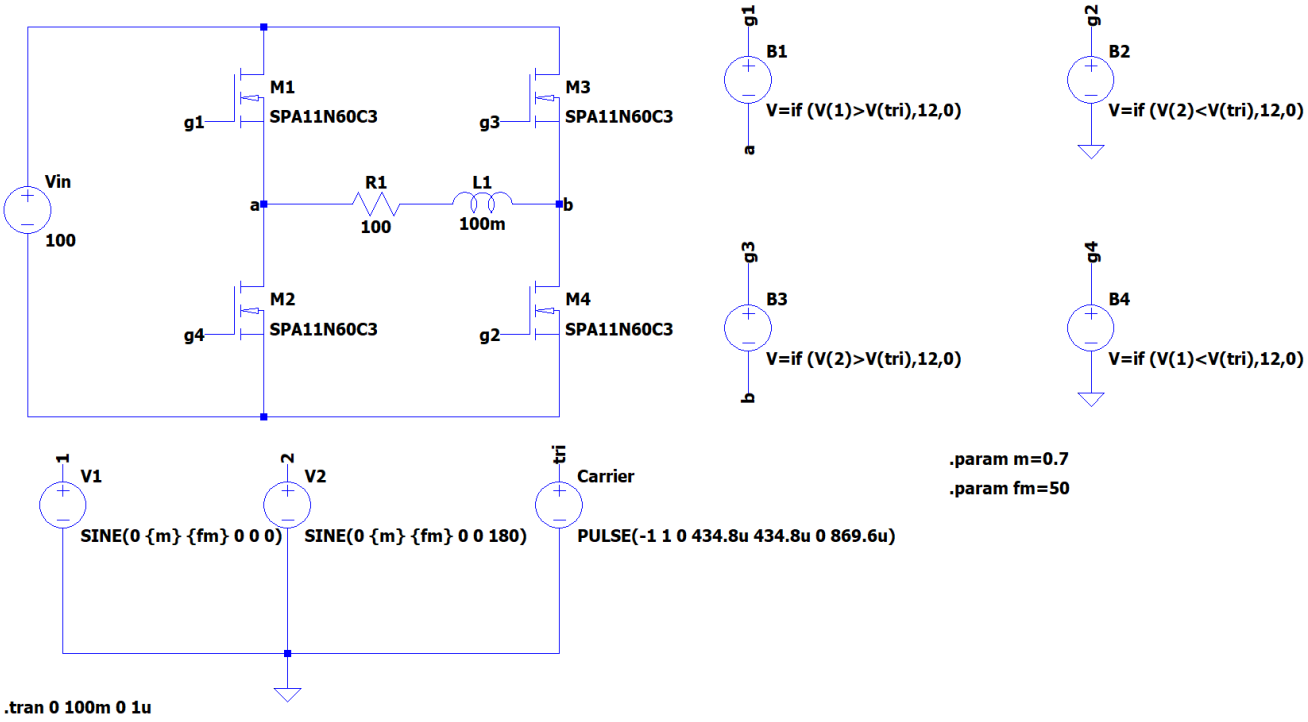

Figure 65. Full-Bridge VSI with PWM modulation.

As mentioned before in a unipolar switching scheme for pulse-width modulation, a high frequency triangular carrier is compared with two low frequency sinusoidal references. The output $v_o = v_{ab}$ is switched either from high to zero or from low to zero. That is why it is called unipolar. In unipolar switching scheme:

- S1 is on when $v_{sine} > v_{tri}$.
- S2 is on when $-v_{sine} < v_{tri}$.
- S3 is on when $-v_{sine} > v_{tri}$.
- S4 is on when $v_{sine} < v_{tri}$.

Variables "*m*" and "*fm*" determine the amplitude modulation ratio and frequency of output voltage, respectively. Amplitude modulation ratio is the ratio of amplitude of sinusoidal reference to the amplitude of triangular carrier:

$$m = \frac{V_{Sinusoidal\ Reference}}{V_{Triangular\ Carrier}} \tag{39}$$

Frequency modulation ratio is the ratio of carrier frequency to frequency of sinusoidal reference:

$$m_f = \frac{f_{Triangular\ carrier}}{f_{Sinusoidal\ Reference}} \tag{40}$$

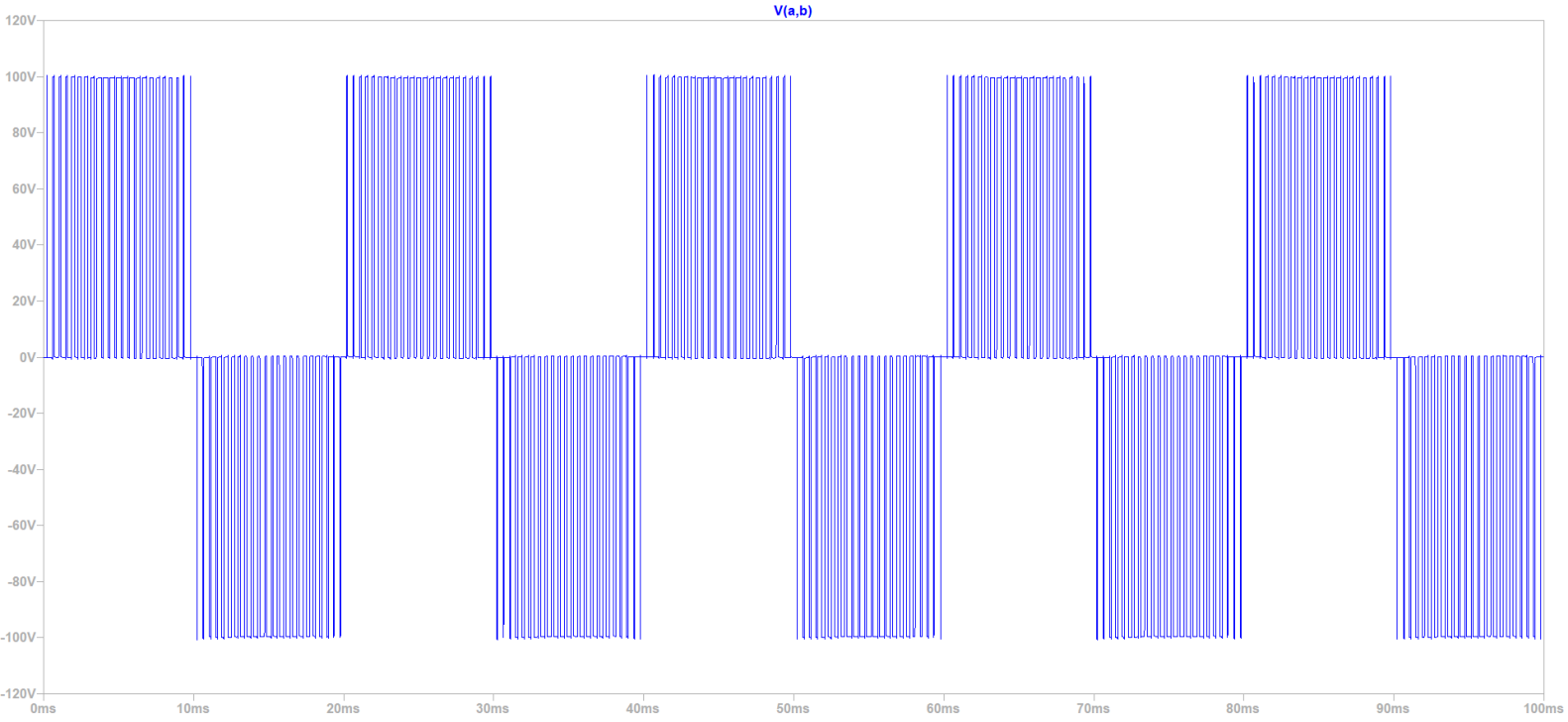

Figure 66. Graph of voltage across the RL load.

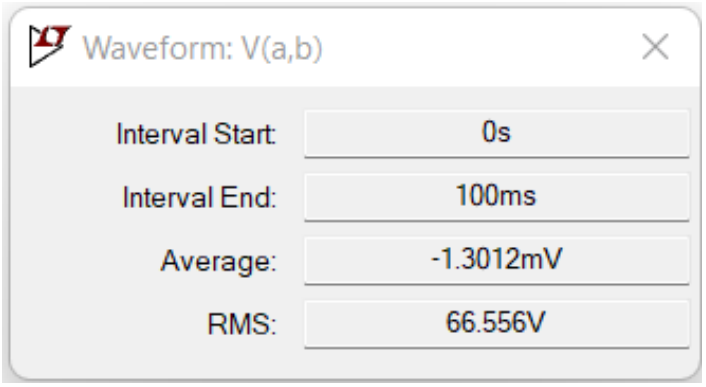

Figure 67. RMS of the load voltage is around 66.556 V**.**

The waveform of the load current is shown in Fig. 66. This waveform is similar to a sinusoidal waveform. The load contains an inductor, and the impedance of inductor increases

with frequency. So, the inductor acts as a filter and decreases the harmonic content of the load current. According to Fig. 69, the RMS of load current is 470.32 mA

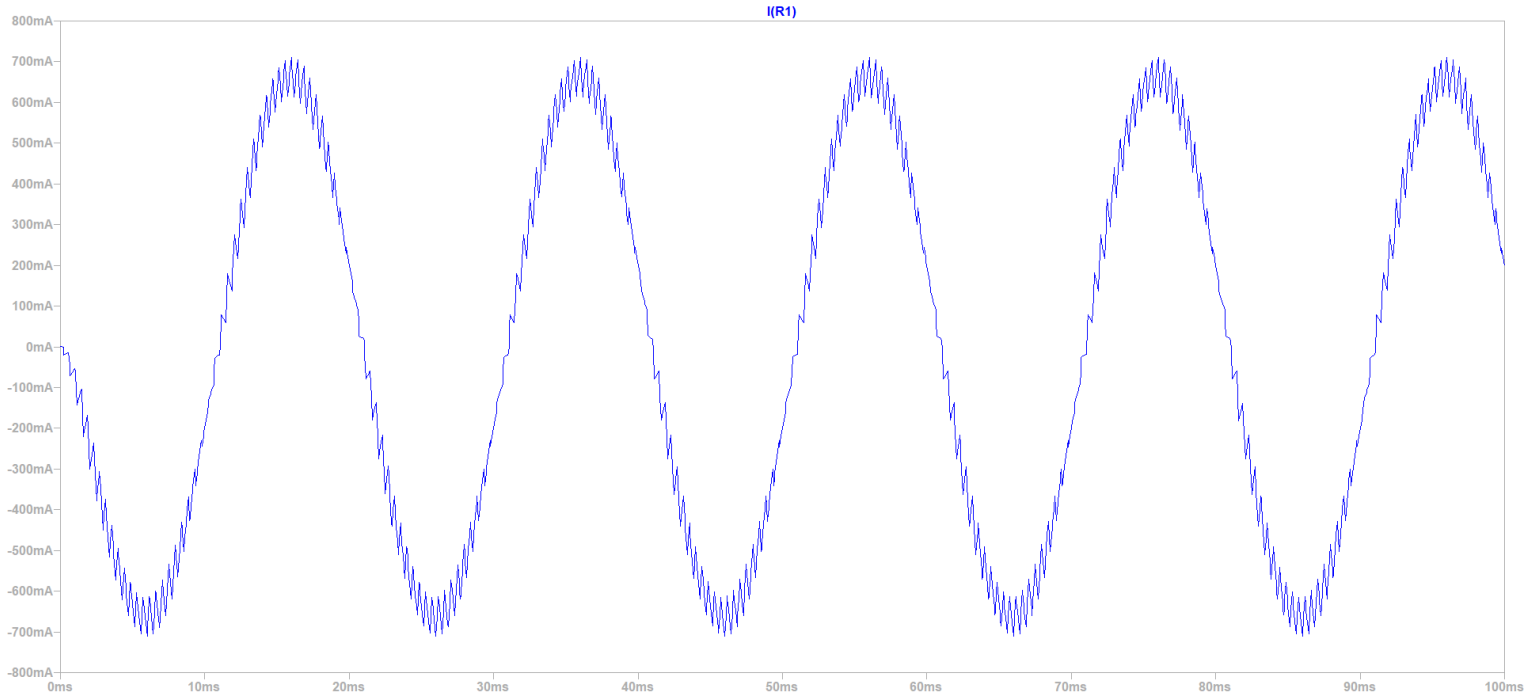

Figure 68. RL load current.

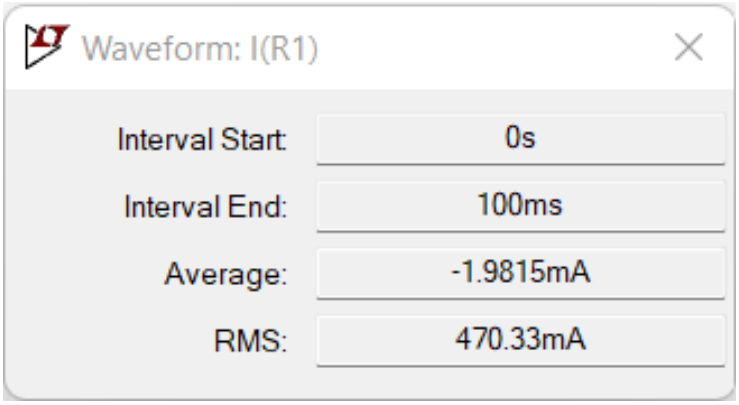

Figure 69. RMS of load current is 470.32 mA.

2.3. Three-phase VSI.

Figure 70 shows a standard Three-Phase VSI. Switches are made with the MOSFET IRF6607 and a diode as a support. The value of the rest of the components are:

$$R_1 = R_2 = R_3 = 5\Omega \;\; L_1 = \;\; L_2 = \;\; L_3 = 23mF \;\; V_1 = 220V$$

The switching estates are given in Table 4. It is likely to single-phase VSI, the switches of any leg of the inverter ($M_1$and M_4, M_3 and M_6 or M_5 and M_2) cannot be witched at the same time, since it would result in a short-circuit across the dc link voltage supply. Similarly, in order to avoid undefined states in the VSI, and thus undefined ac output line voltages, the switches of any leg of the inverter cannot be switched off simultaneously as this will result in voltages that will depend upon the respective line current polarity.

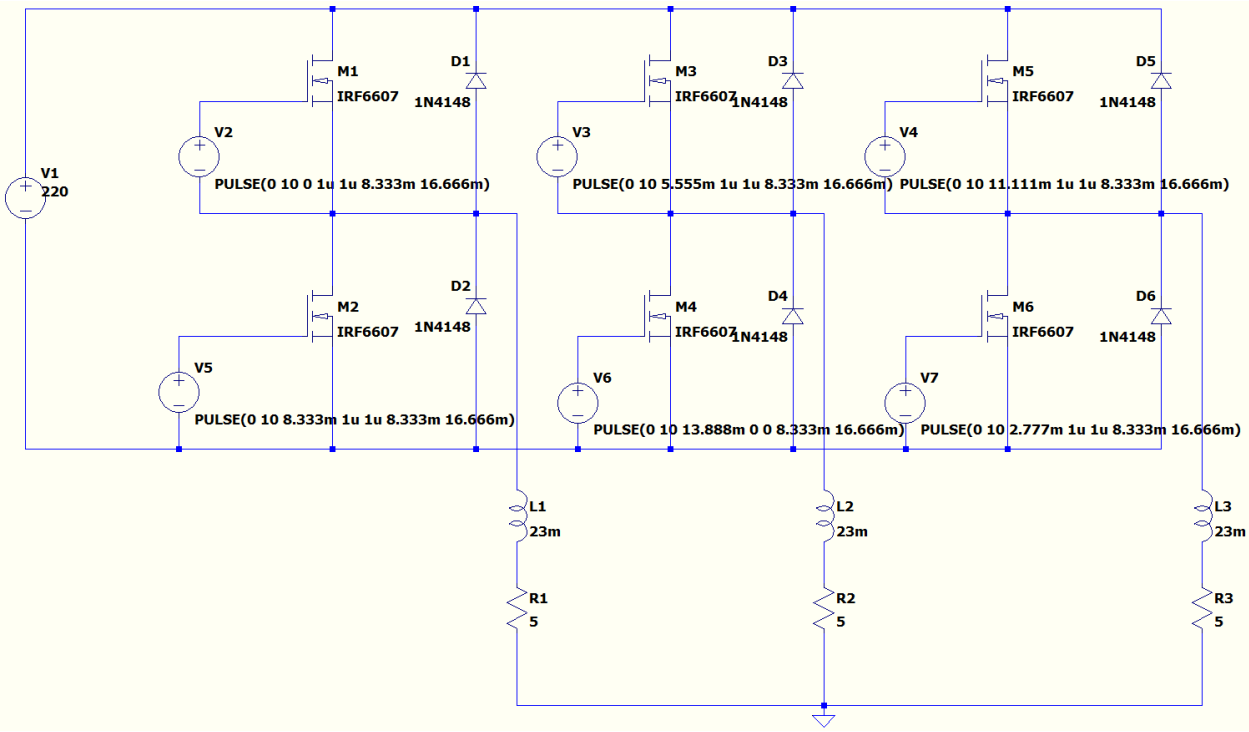

Figure 70. Three-phase VSI**.**

In the following images is shown how the three-phase VSI works.

In Fig.71 is clear that this configuration is not a perfect and the resultant waveform is not sinusoidal, this is the reason why a modulation technique is needed. The most important modulation technique and the one that will be shown in this paper is the Sinusoidal PWM technique.

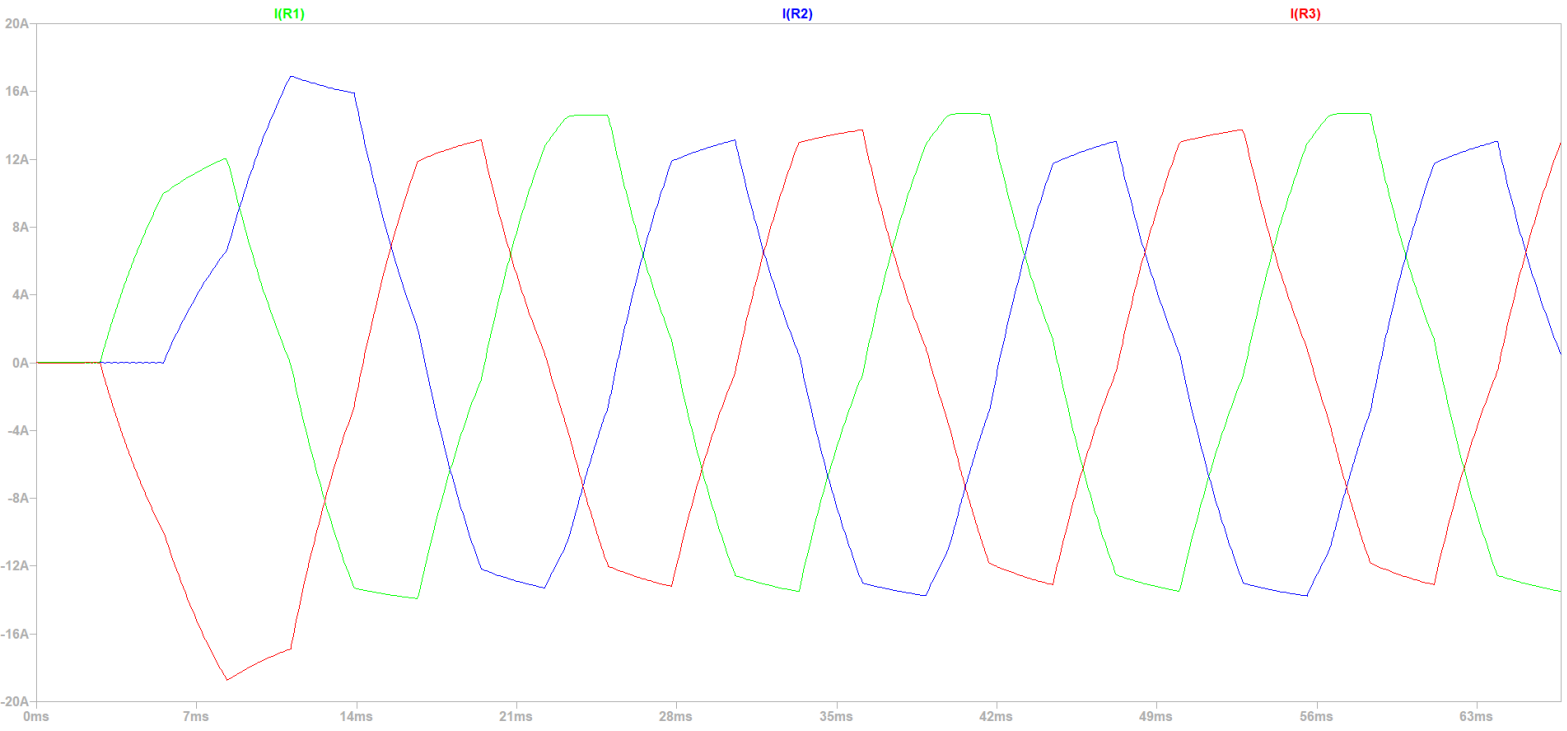

Figure 71. Current passing through the lines.

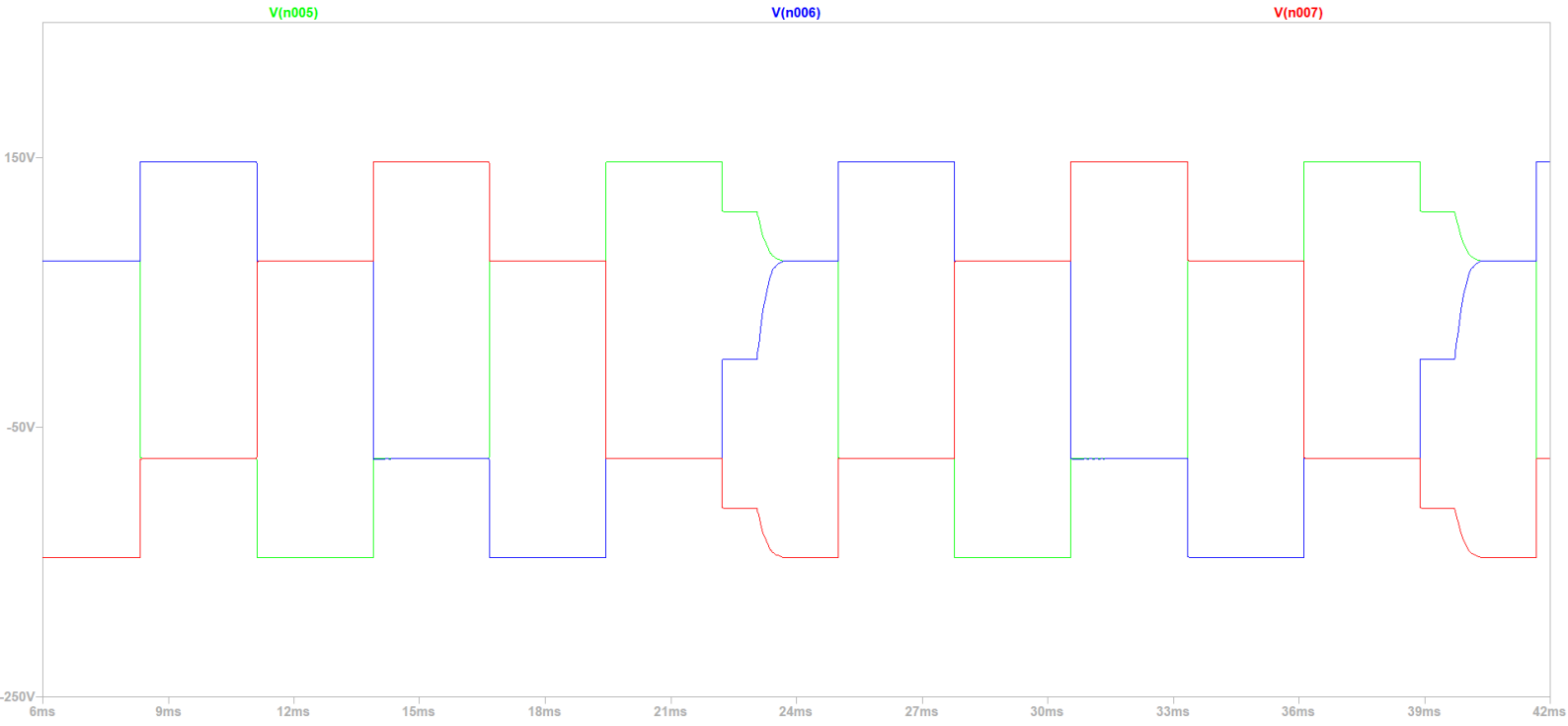

Figure 72. Voltage passing through the lines.

2.4. SPWM Case 1.

Below we will show an example of a full bridge Three-phase inverter and the SPWM modulator that has been designed to generate switching signals. Modulated SPWM signals have been used to control Mosfet switches of the inverter, a FFT and a THD analysis of output voltage and current have been performed.

In the following images is shown a circuit where the sinusoidal PWM technique has been applied.

In Fig.73 the switches used are MOSFET IRFH 5020. The value of the rest components are:

$$V_1 = 220V \; R_1 = R_2 = R_3 = R_4 = R_5 = R_6 = R_7 = R_8 = R_9 = 10\Omega \quad R_{10} = R_{11} = 1\text{k}\Omega$$

$$L_1 = \; L_2 = \; L_3 = 25\mu$$

$$C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = 0.3\mu$$

The modulation index is $m_a = 0.95$

The frequency modulation ratio is $m_f = 1000$

The frequency of the carrier wave is $f = 20\ kHz$

In order to calculate the FFT and THD the blocks on the right have been added.

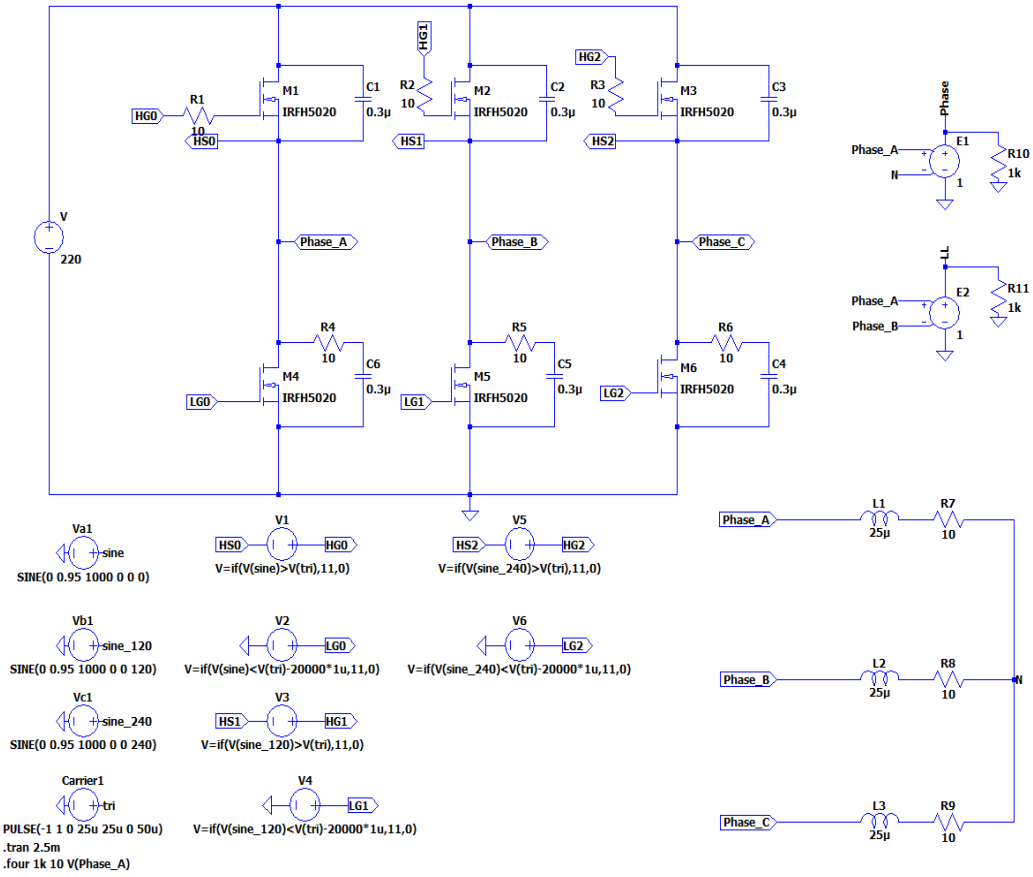

Figure 73. Three-Phase VSI with SPWM technique.

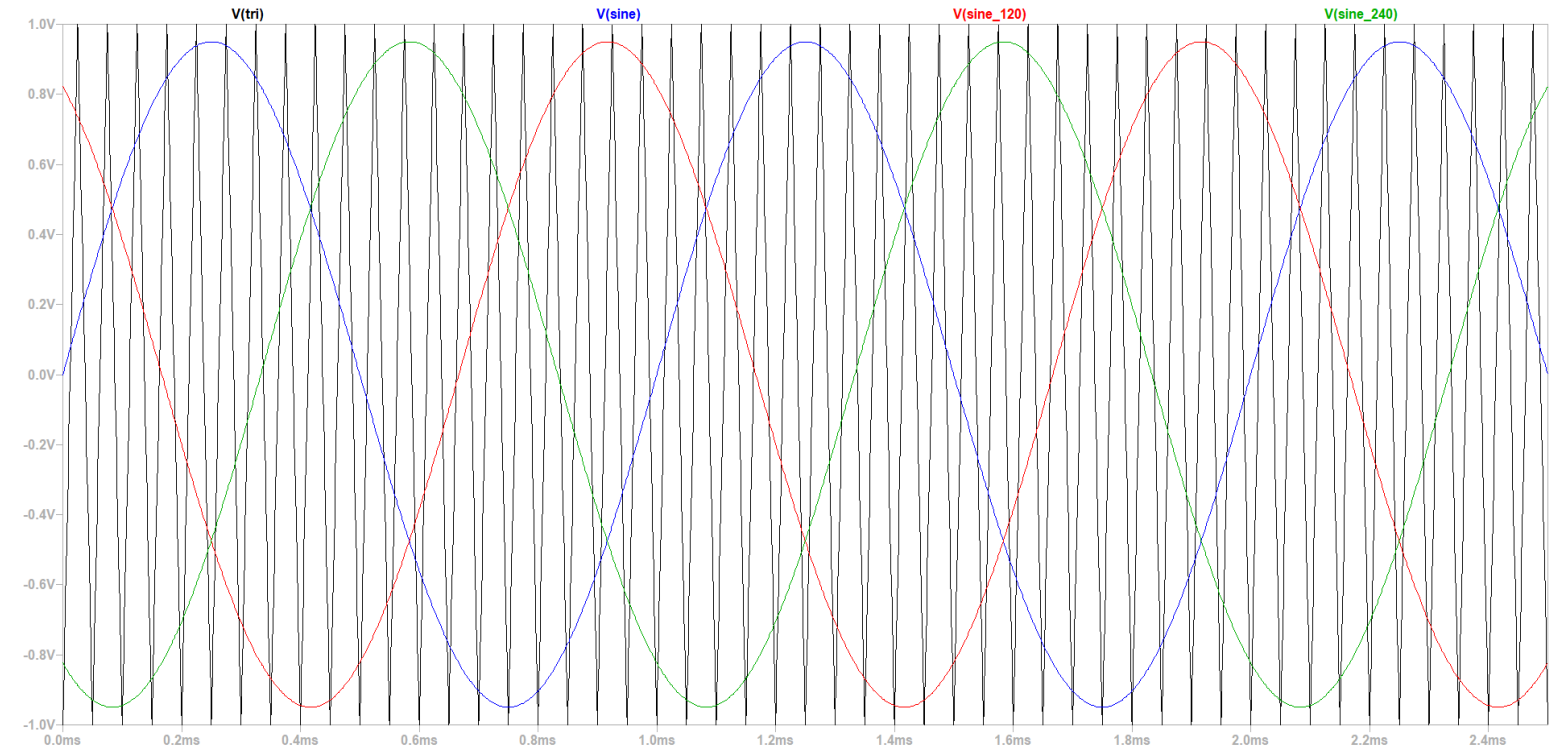

Figure 74. Carrier signal compared with the three sinusoidal waves.

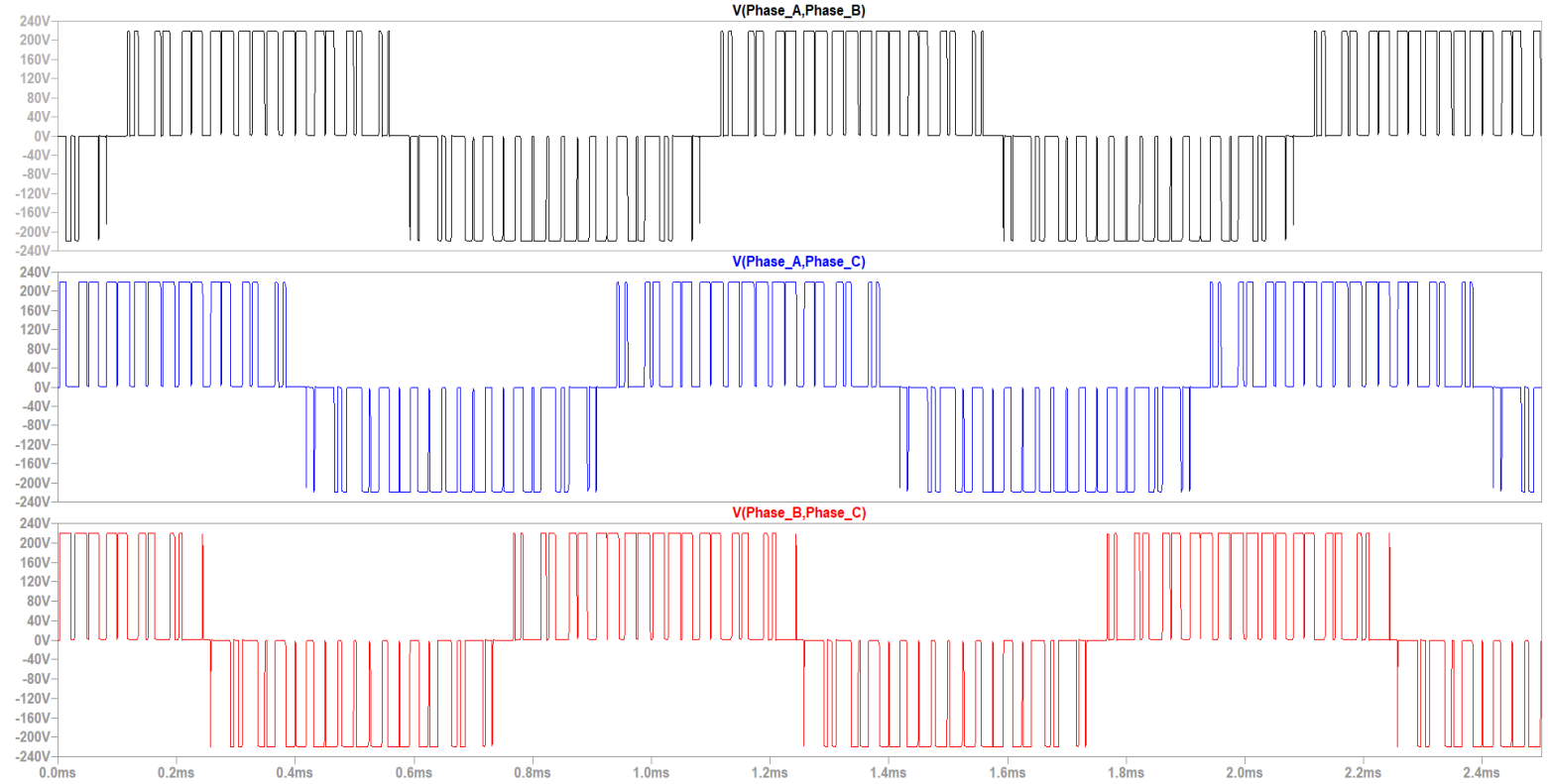

Figure 75. Voltage passing through the lines.

In Fig. 76 we can observe that the waves obtained are far away from being sinusoidal, these can be due to different factors as the value of the resistance and inductance in the lines or the switching frequency.

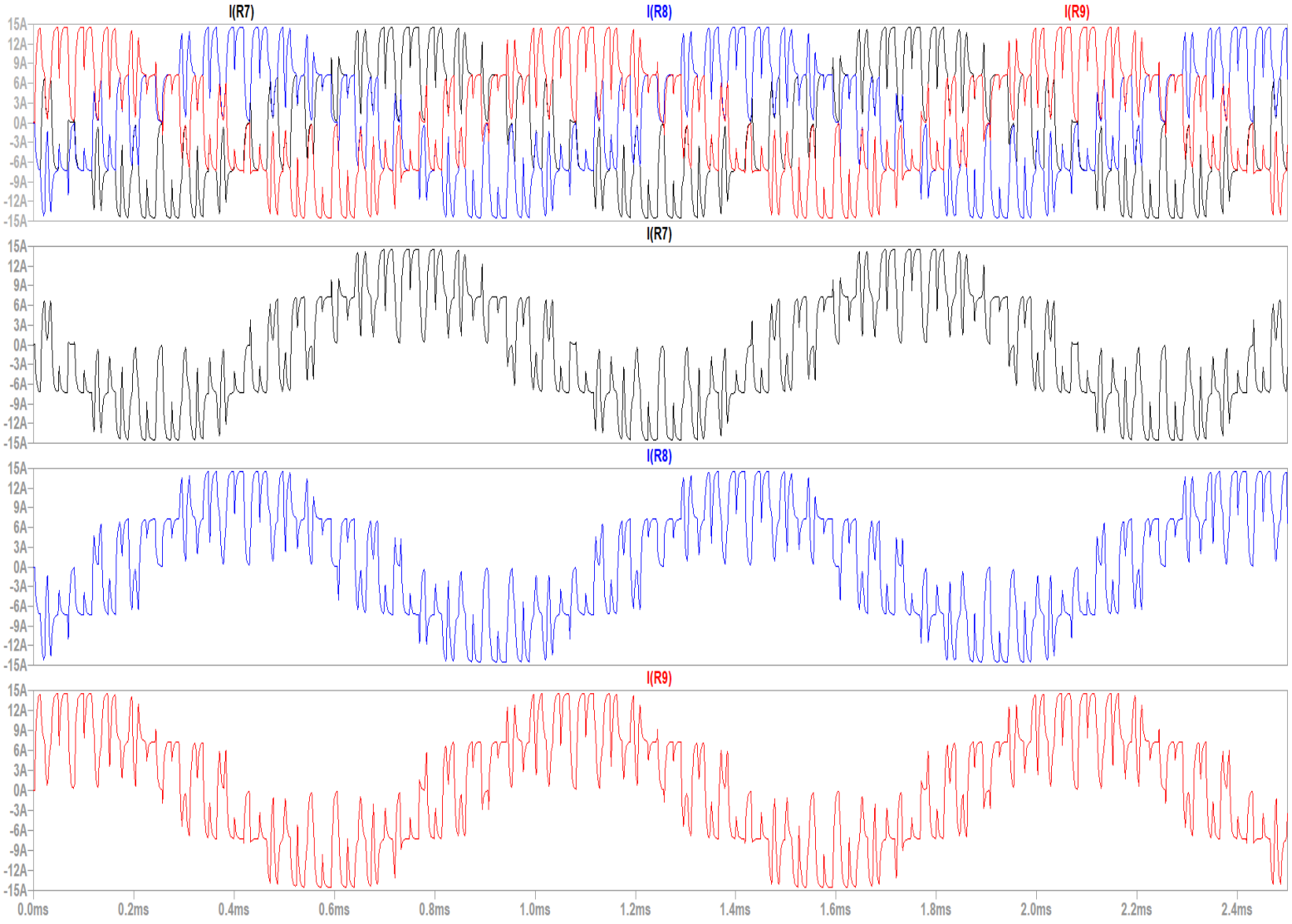

Figure 76. Current passing through the lines.

First, to try to solve this problem we are going to change the value of the resistance and inductance in the lines, the new value of the components are the following:

$$R_7 = R_8 = R_9 = 0{,}040667\Omega \quad L_1 = \ L_2 = \ L_3 = 27{,}33\mu$$

Changing these values, we can observe that the currents adopt a better sinusoidal waveform. Although these changes a LCL filter will be needed.

Anyway, this configuration for a Three-phase inverter needs to be improved because the values of the resistance and the inductance are very low and are far away to be suitable for a three-phase high power inverter.

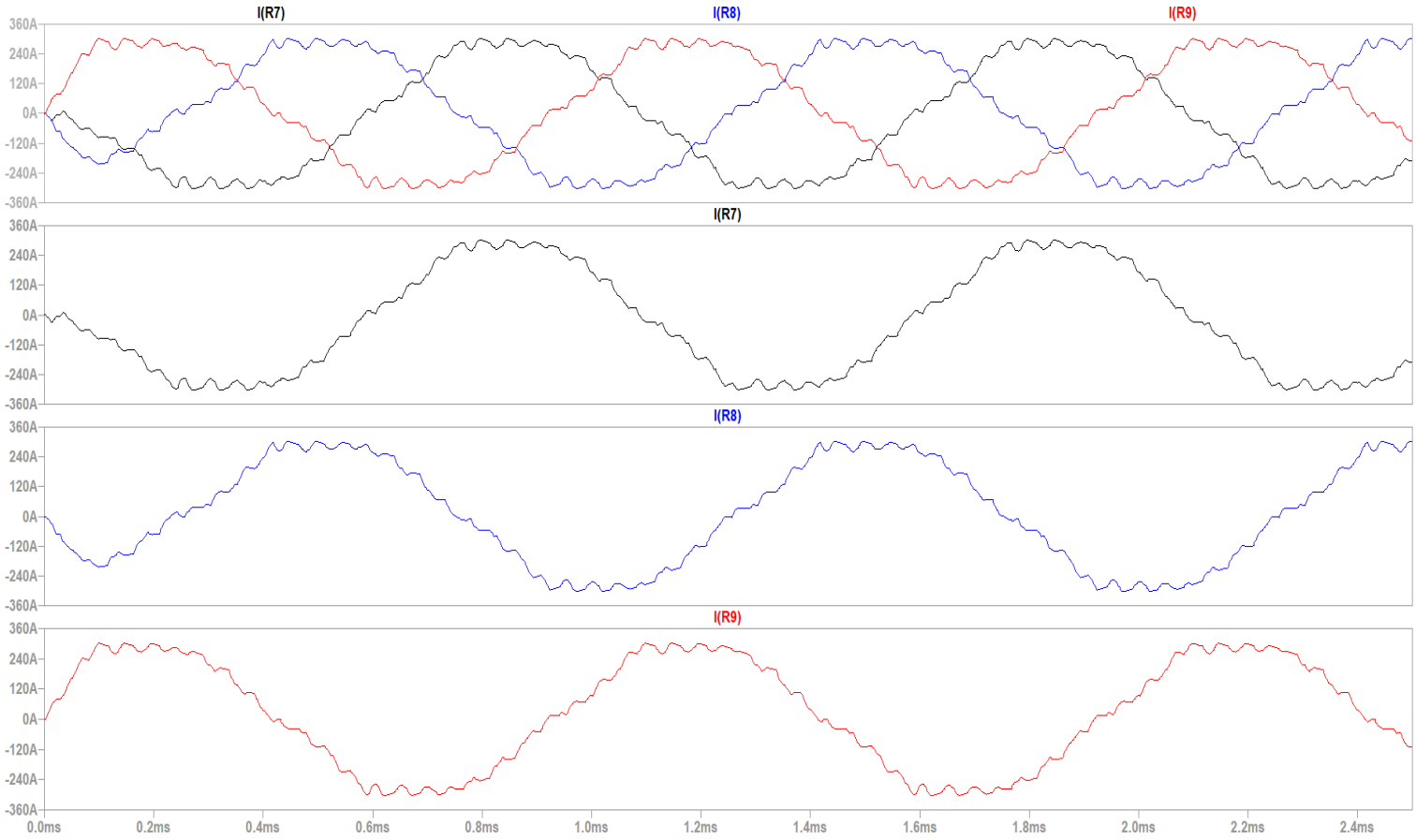

Figure 77. Current passing through the lines.

2.4.1. Fast Fourier Transformation (FFT).

The "Fast Fourier Transform" (FFT) is an important measurement method in the science of audio and acoustics measurement. It converts a signal into individual spectral components and thereby provides frequency information about the signal. FFTs are used for fault analysis, quality control, and condition monitoring of machines or systems.

In our case FFT will provide us important information about the noise in our signal.

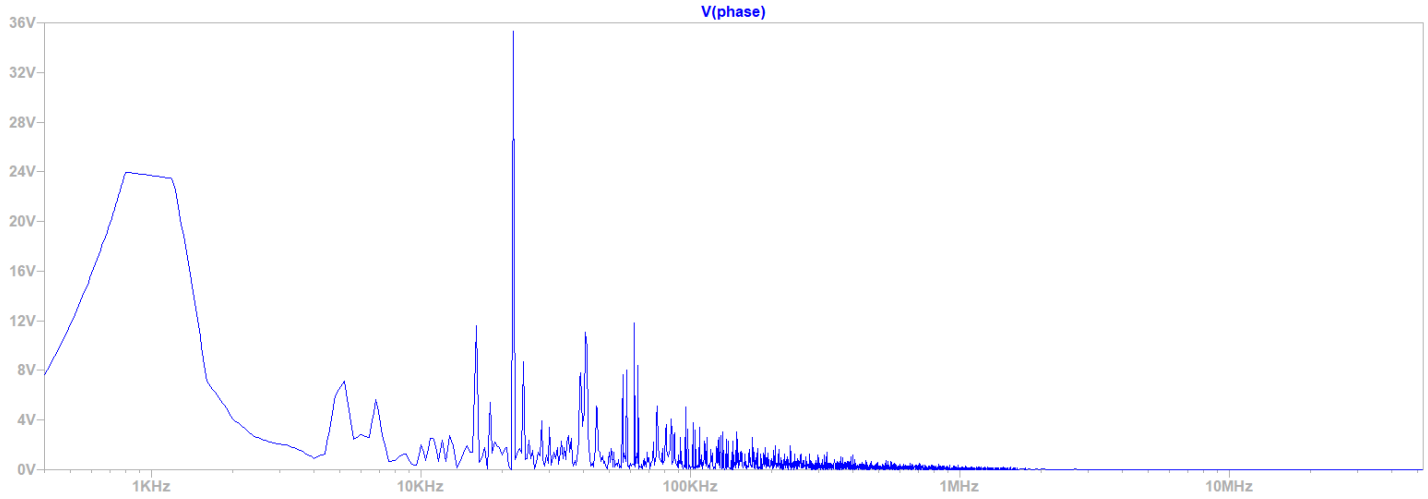

Figure 78. FFT on V(Phase) SPWM Case 1.

How our switching frequency is 20 kHz we can see that in Fig. 76 we get our first harmonic around that frequency. At higher frequencies we still get some harmonics, but they get lower when increasing frequency. At lower frequencies we can see the fundamental frequency values.

2.4.2. Total Harmonic Distortion (THD).

The power quality of distribution systems has a drastic effect on power regulation and consumption. Power sources act as non-linear loads, drawing a distorted waveform that contains harmonics. These harmonics can cause problems ranging from telephone transmission interference to degradation of conductors and insulating material in motors and transformers. Therefore, it is important to gauge the total effect of these harmonics. The summation of all harmonics in a system is known as total harmonic distortion (THD).

Waveform distortions can drastically alter the shape of the sinusoid. However, no matter the level of complexity of the fundamental wave, it is just a composite of multiple waveforms called harmonics. Harmonics have frequencies that are integer multiples of the waveform's fundamental frequency. Thus, harmonic distortion is the degree to which a waveform deviates from its pure sinusoidal values as a result of the summation of all these harmonic elements. The ideal sine wave has zero harmonic components. In that case, there is nothing to distort this perfect wave. Total harmonic distortion, or THD, is the summation of all harmonic components of the voltage or current waveform compared against the fundamental component of the voltage or current wave:

$$THD = \frac{\sqrt{V_{2^2} + V_{3^2} + V_{4^2} + \cdots V_{n^2}}}{V_1} * 100\% \qquad (41)$$

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]	Normalized Phase [deg]
1	5.000e+01	1.712e+00	1.000e+00	-13.92°	0.00°
2	1.000e+02	2.244e+00	1.311e+00	-87.26°	-73.34°
3	1.500e+02	4.815e+00	2.812e+00	-109.73°	-95.81°
4	2.000e+02	6.207e+00	3.625e+00	-146.33°	-132.41°
5	2.500e+02	9.486e+00	5.539e+00	-173.42°	-159.50°
6	3.000e+02	1.003e+01	5.858e+00	164.53°	178.45°
7	3.500e+02	1.090e+01	6.367e+00	136.07°	150.00°
8	4.000e+02	1.084e+01	6.333e+00	118.23°	132.15°
9	4.500e+02	8.747e+00	5.108e+00	95.74°	109.66°

Total Harmonic Distortion: 1394.625099%(10440.185772%)

Figure 79. SPWM Case 1 THD.

2.5. SPWM Case 2.

In order to proportionate a VSI with better specifications another example will be shown below. This inverter has been designed with SPWM too. Modulated SPWM signals have been used to control Mosfet switches of the inverter, a FFT and a THD analysis of output voltage and current have been performed.

In Fig.80 the switches used are MOSFET SPA11N60C3. The value of the rest components are:

$$V_{IN} = 220V \; R_1 = R_2 = R_3 = 100\Omega \;\; R_4 = R_5 = 1\text{k}\Omega$$

$$L_1 = \; L_2 = \; L_3 = 100m$$

The modulation index is $m_a = 0.7$

The frequency modulation ratio is $m_f = 50$

The frequency of the carrier wave is $f = 2.3\ kHz$

In order to calculate the FFT and THD the blocks on the right have been added.

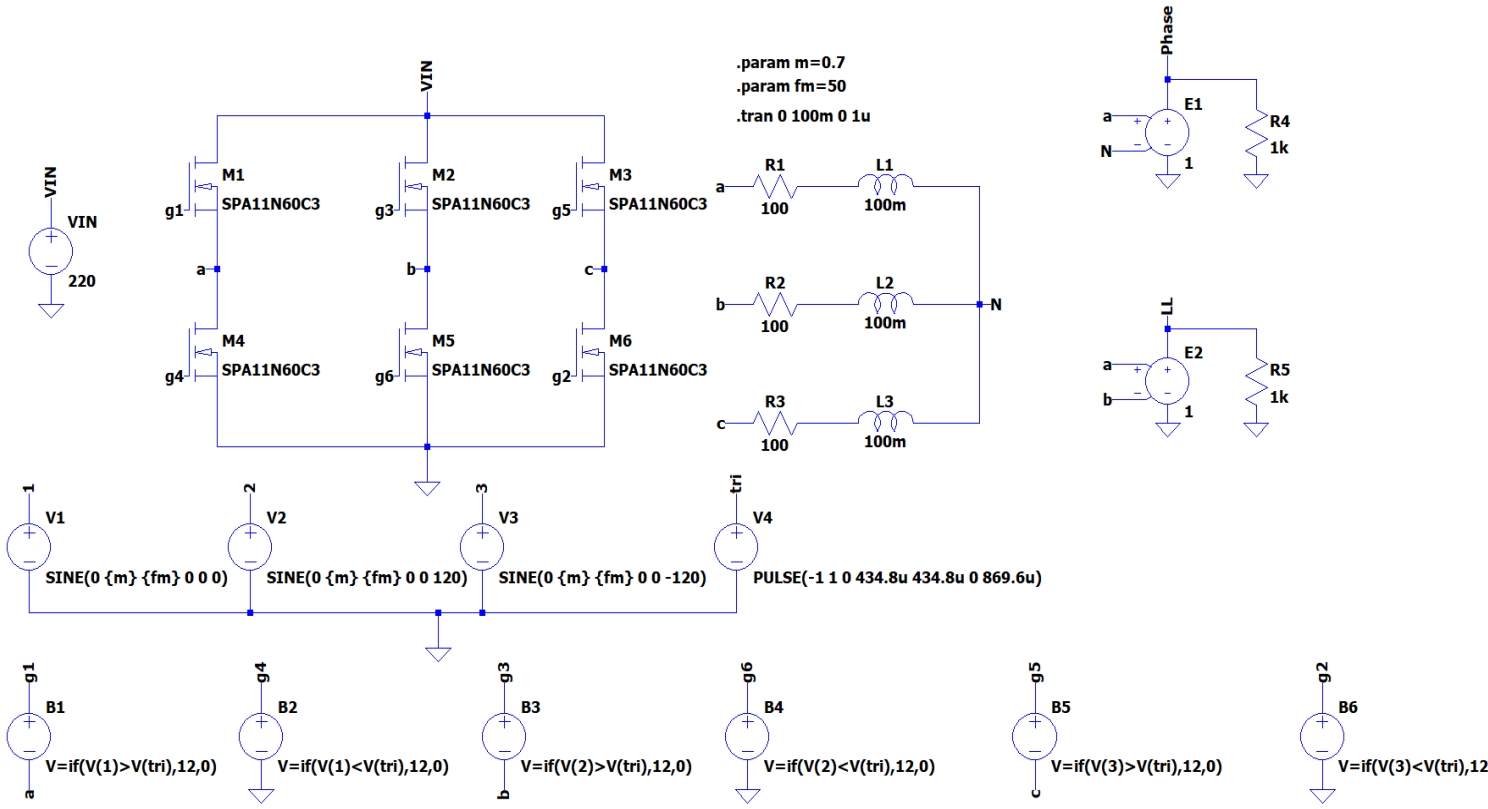

Figure 80. Three-Phase inverter with SPWM case 2.

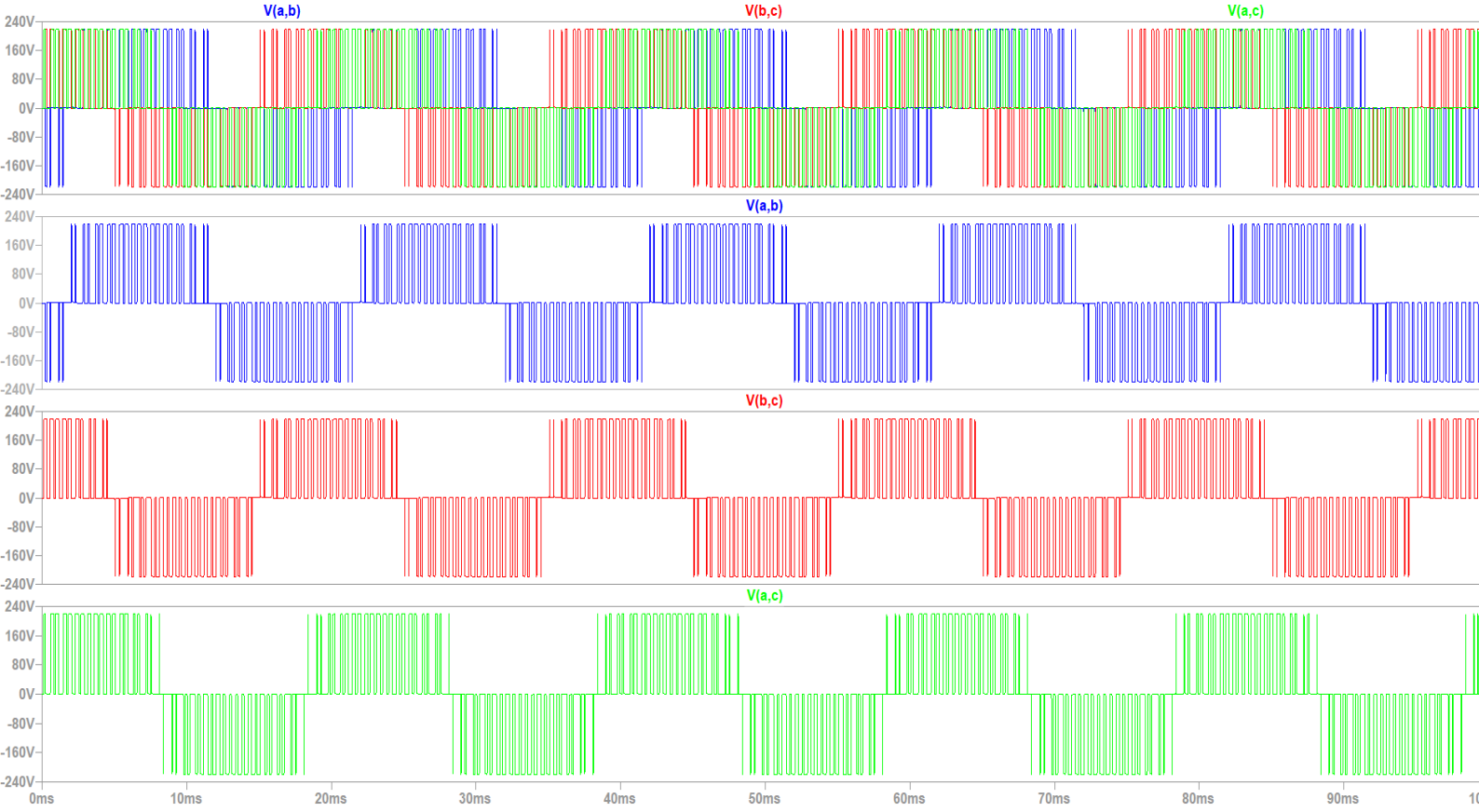

Figure 81. Voltage passing through the 3 phases.

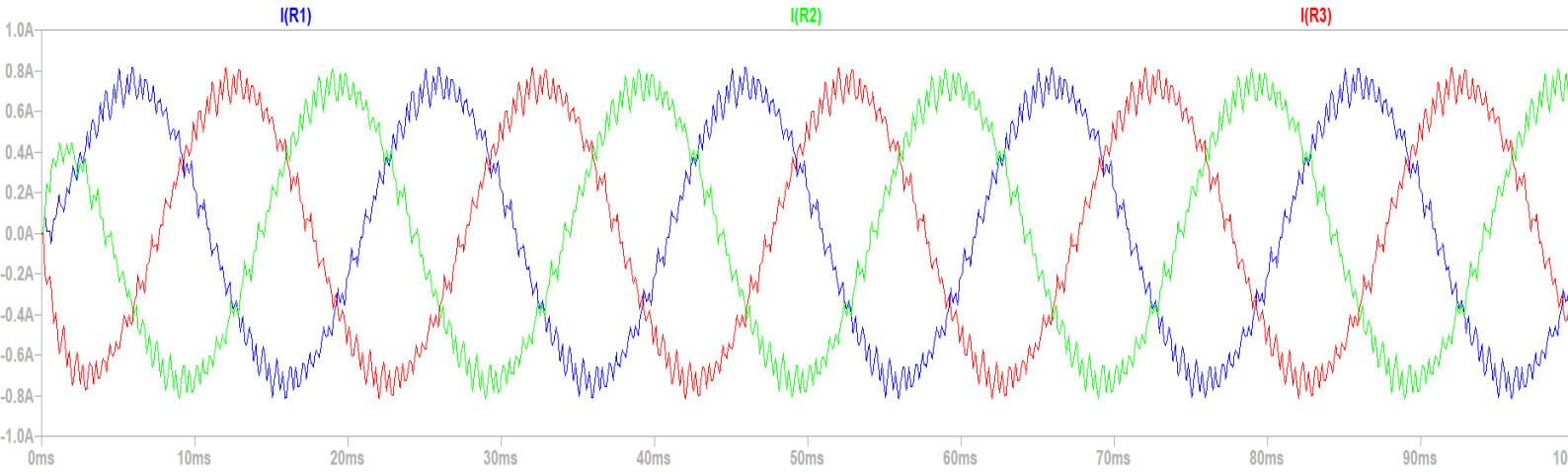

Figure 82. Current passing through the lines.

As we see in Fig. 82 the waveforms of the current passing through de lines adopt a better sinusoidal form than in case one. Anyway, some noise can be seen and a LCL filter will be needed.

2.5.1 Fast Fourier Transformation (FFT)

As we mentioned before the "Fast Fourier Transform" (FFT) is an important measurement method in the science of audio and acoustics measurement

In our case FFT will provide us important information about the noise in our signal.

How our switching frequency is 2,3 kHz we can see that in Fig. 81 we get our highest harmonic around that frequency. At higher frequencies we still get some harmonics, but they get lower when increasing frequency. At lower frequencies we can see the fundamental frequency values

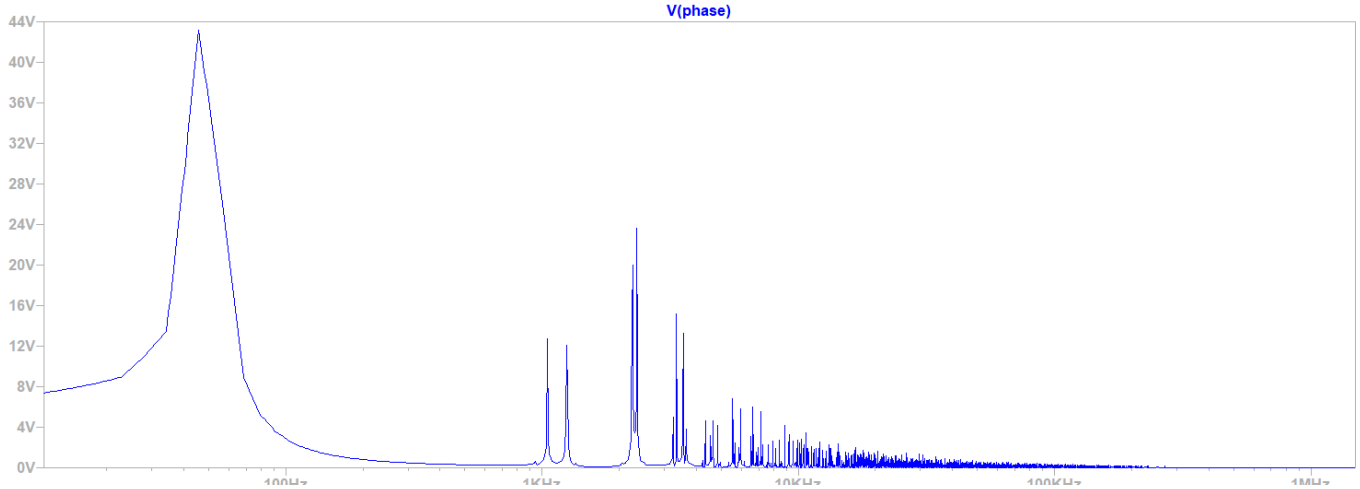

Figure 83. FFT SPWM Case 2.

2.5.2 Total Harmonic Distortion (THD)

In a previous chapter the importance of THD has been explained, In Fig. 82 we can see the THD obtained in our case. As we see this value is much lower than in case 1, what indicates that the waveforms have a better sinusoidal form and there are lower harmonics.

N-Period=1
Fourier components of V(phase)
DC component:0.000127636

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]	Normalized Phase [deg]
1	5.000e+01	7.676e+01	1.000e+00	0.06°	0.00°
2	1.000e+02	2.314e-04	3.014e-06	-17.63°	-17.69°
3	1.500e+02	1.649e-04	2.149e-06	124.61°	124.56°
4	2.000e+02	3.064e-04	3.992e-06	-118.35°	-118.40°
5	2.500e+02	2.241e-04	2.920e-06	-26.93°	-26.98°
6	3.000e+02	1.893e-04	2.466e-06	-169.86°	-169.92°
7	3.500e+02	5.376e-04	7.003e-06	-100.58°	-100.64°
8	4.000e+02	3.261e-04	4.249e-06	-68.72°	-68.77°
9	4.500e+02	5.187e-04	6.757e-06	-124.26°	-124.32°

Total Harmonic Distortion: 0.001253%(105.254110%)

Figure 84. THD of SPWM case 2.

2.6. Changing Load.

In this part of the work some experiments will be done, we will see how the inverter works and reacts with three different loads, comparing the results. THD will be used to compare which waveforms have a better sinusoidal form and the harmonics obtained. The different loads are the following:

- Load 1: $L_1 = \ L_2 = \ L_3 = 100m \ \ R_1 = R_2 = R_3 = 100\Omega$
- Load 2: $L_1 = \ L_2 = \ L_3 = 50m \ \ R_1 = R_2 = R_3 = 50\Omega$
- Load 3: $L_1 = \ L_2 = \ L_3 = 10m \ \ R_1 = R_2 = R_3 = 10\Omega$
- Load 4: $L_1 = \ L_2 = \ L_3 = 1m \ \ R_1 = R_2 = R_3 = 1\Omega$
- Load 5: $L_1 = \ L_2 = \ L_3 = 200m \ \ R_1 = R_2 = R_3 = 200\Omega$

As we can see in the Fig. 85 we can observe slightly differences between the images, the resultant sinusoidal is almost the same, in case d) where the load is 100 times smaller than in case 1 we can see more noise, which indicates that the THD will be higher. Anyway, the THD results will give more important information and will tell how the results differ from the perfect sinusoidal waveform.

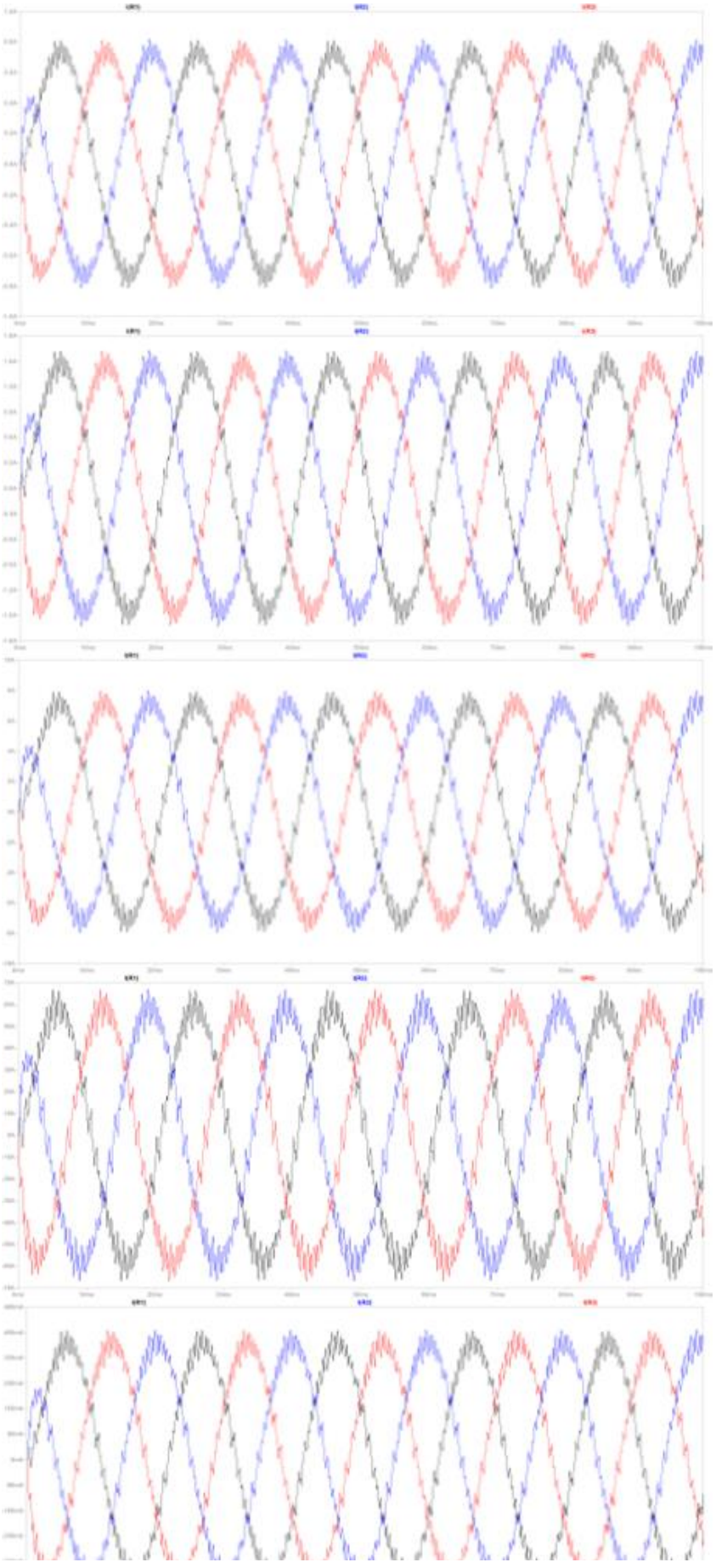

Figure 85. Comparison of the resultant waveform with different loads. a) load 1 b) load 2 c) load 3 d) load 4 e) load 5**.**

N-Period=1
Fourier components of V(phase)
DC component:0.000127636

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]	Normalized Phase [deg]
1	5.000e+01	7.676e+01	1.000e+00	0.06°	0.00°
2	1.000e+02	2.314e-04	3.014e-06	-17.63°	-17.69°
3	1.500e+02	1.649e-04	2.149e-06	124.61°	124.56°
4	2.000e+02	3.064e-04	3.992e-06	-118.35°	-118.40°
5	2.500e+02	2.241e-04	2.920e-06	-26.93°	-26.98°
6	3.000e+02	1.893e-04	2.466e-06	-169.86°	-169.92°
7	3.500e+02	5.376e-04	7.003e-06	-100.58°	-100.64°
8	4.000e+02	3.261e-04	4.249e-06	-68.72°	-68.77°
9	4.500e+02	5.187e-04	6.757e-06	-124.26°	-124.32°

Total Harmonic Distortion: 0.001253%(105.254110%)

N-Period=1
Fourier components of V(phase)
DC component:-5.57375e-005

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]	Normalized Phase [deg]
1	5.000e+01	7.653e+01	1.000e+00	0.11°	0.00°
2	1.000e+02	9.755e-05	1.275e-06	107.01°	106.90°
3	1.500e+02	1.361e-04	1.778e-06	-43.85°	-43.96°
4	2.000e+02	2.087e-04	2.727e-06	-101.86°	-101.97°
5	2.500e+02	2.449e-04	3.201e-06	-129.60°	-129.71°
6	3.000e+02	1.139e-04	1.489e-06	-89.52°	-89.63°
7	3.500e+02	3.141e-04	4.104e-06	-72.28°	-72.39°
8	4.000e+02	5.203e-04	6.799e-06	-99.34°	-99.45°
9	4.500e+02	5.402e-04	7.059e-06	-108.80°	-108.91°

Total Harmonic Distortion: 0.001173%(105.576034%)

N-Period=1
Fourier components of V(phase)
DC component:-1.97503e-005

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]	Normalized Phase [deg]
1	5.000e+01	7.496e+01	1.000e+00	0.44°	0.00°
2	1.000e+02	7.906e-05	1.055e-06	-87.49°	-87.93°
3	1.500e+02	9.847e-04	1.314e-05	-1.27°	-1.71°
4	2.000e+02	1.457e-04	1.943e-06	-83.91°	-84.35°
5	2.500e+02	3.387e-02	4.518e-04	89.79°	89.35°
6	3.000e+02	2.811e-04	3.750e-06	-94.35°	-94.79°
7	3.500e+02	1.859e-02	2.480e-04	66.62°	66.18°
8	4.000e+02	4.434e-04	5.915e-06	-94.52°	-94.96°
9	4.500e+02	1.981e-03	2.642e-05	172.04°	171.60°

Total Harmonic Distortion: 0.051629%(107.379536%)

N-Period=1
Fourier components of V(phase)
DC component:-8.87812e-005

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phas [degr
1	5.000e+01	6.125e+01	1.000e+00	3
2	1.000e+02	8.962e-04	1.463e-05	-109
3	1.500e+02	9.310e-03	1.520e-04	42
4	2.000e+02	9.077e-04	1.482e-05	-61
5	2.500e+02	8.333e-02	1.360e-03	-11
6	3.000e+02	4.270e-04	6.972e-06	-103
7	3.500e+02	4.410e-02	7.200e-04	4
8	4.000e+02	1.334e-03	2.177e-05	-92
9	4.500e+02	2.126e-02	3.471e-04	-54

Total Harmonic Distortion: 0.158541%(125.609794%)

N-Period=1
Fourier components of V(phase)
DC component:0.000118296

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phas [degr
1	5.000e+01	7.688e+01	1.000e+00	0
2	1.000e+02	2.404e-04	3.127e-06	-55
3	1.500e+02	1.423e-04	1.850e-06	57
4	2.000e+02	2.349e-04	3.056e-06	-162
5	2.500e+02	3.571e-04	4.645e-06	-86
6	3.000e+02	1.428e-04	1.857e-06	-33
7	3.500e+02	2.752e-04	3.580e-06	-138
8	4.000e+02	6.014e-04	7.822e-06	-98
9	4.500e+02	5.260e-04	6.841e-06	-77

Total Harmonic Distortion: 0.001298%(105.093124%)

Figure 86. Comparison of the THD results with different loads. a) load 1 b) load 2 c) load 3 d) load 4 e) load 5.

Observing the results of the THD confirms what we predicted before, the variation of all cases is very low, only with load 4 we can see a slightly big difference in the obtention of harmonics.

These two comparisons provide useful information, small-medium differences in the load (50-100%) do not affect the resultant waveform,

2.7. Use of filters.

How it has been explained before in the theory part, the use of filters is vital to the correct work of the three-phase inverter, in our case we will use a passive filter, a LCL filter which has resulted to be the ideal filter wo work with these types of inverters. The configuration of the inverter is the same as the one presented in case 2. The value of the components used in the inverter are the following:

$$R_1 = R_2 = R_3 = 1\Omega \quad R_6 = R_7 = R_8 = 100\Omega$$

$$L_1 = \ L_2 = \ L_3 = 90m \quad L_4 = \ L_5 = \ L_6 = 30m \quad L_7 = \ L_8 = \ L_9 = 100m$$

$$C_1 = \ C_2 = \ C_3 = 8\mu$$

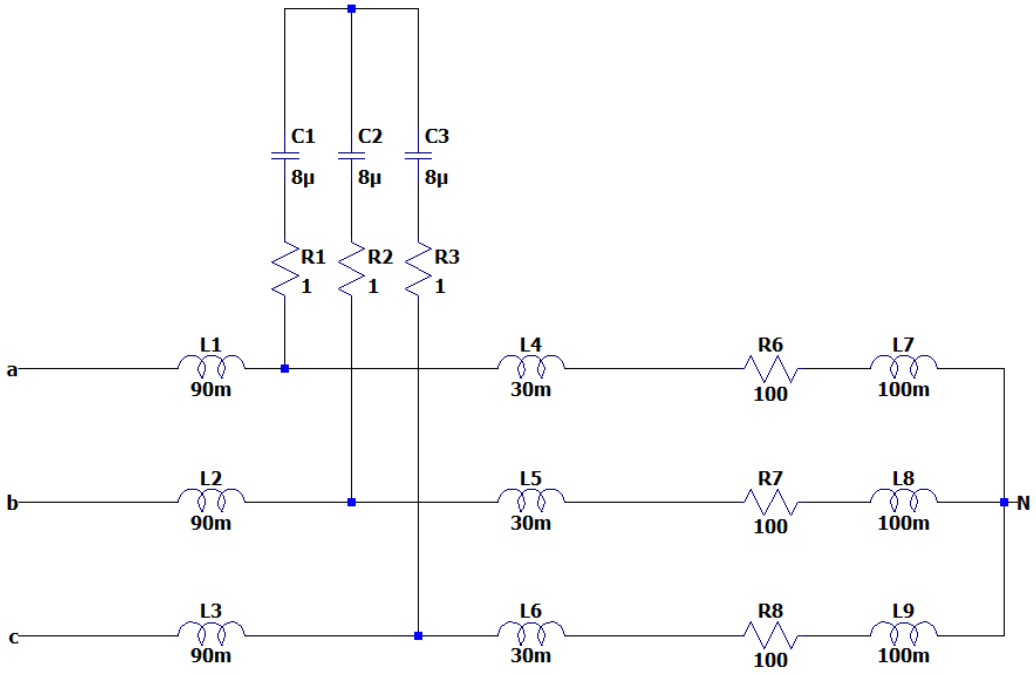

Figure 87. LCL filter.

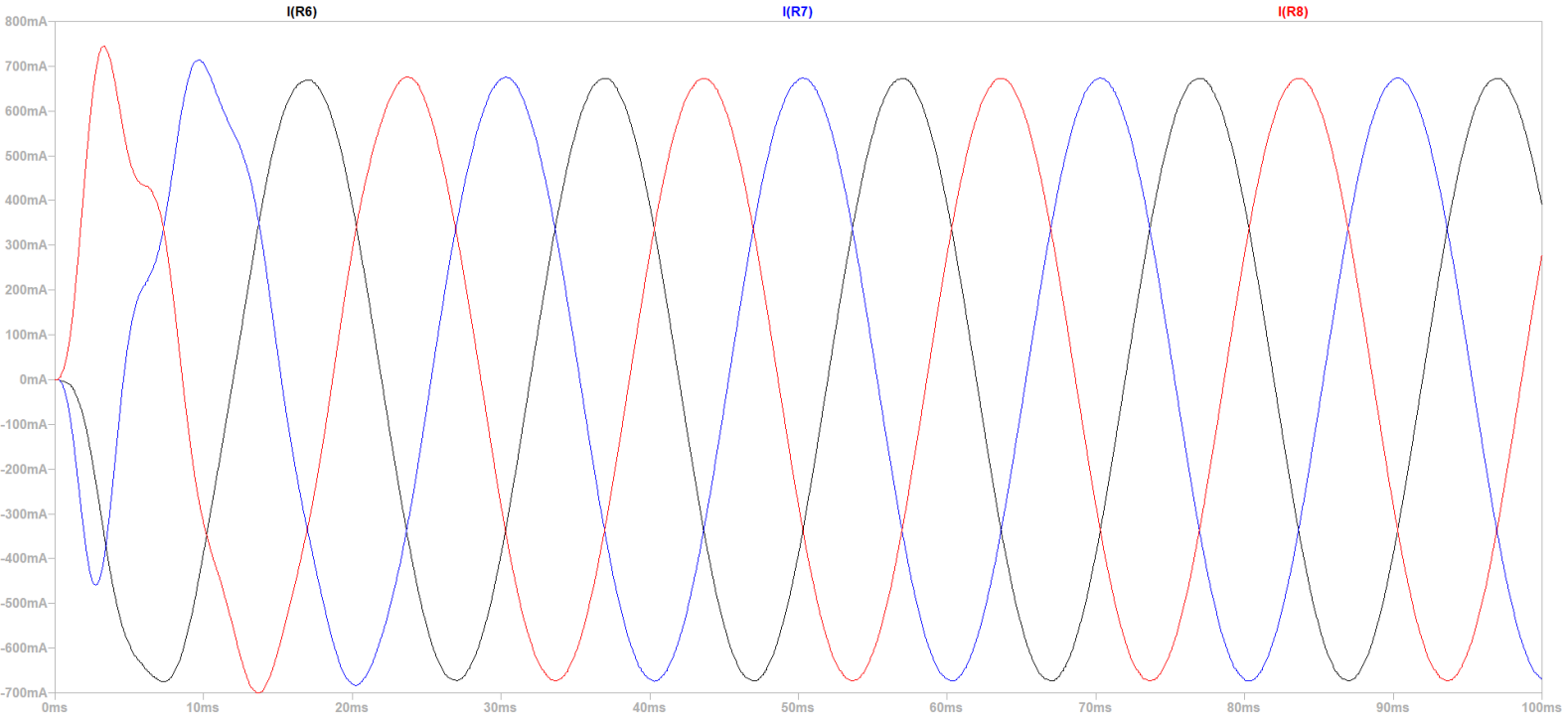

Figure 88. Resultant waveform with a LCL filter.

Fig. 88 shows how the waveform adopts an almost perfect sinusoidal waveform thanks to the filter. At the beginning of the testing some anomalies can be observed in the waveform, this is probably due to the effect of the capacitance, but after some time the sinusoidal waveform is obtained. In the image, no noise is visible. This waveform will be perfectly suitable for a high-power three-phase inverter.

2.7.1 Total Harmonic Distortion (THD)

```
N-Period=1
Fourier components of V(phase)
DC component:-102.35

Harmonic     Frequency     Fourier     Normalized    Phase      Normalized
 Number        [Hz]       Component     Component   [degree]    Phase [deg]
    1       5.000e+01    2.125e+02    1.000e+00       8.31°       0.00°
    2       1.000e+02    8.064e+01    3.794e-01     127.37°     119.06°
    3       1.500e+02    5.271e+01    2.480e-01     156.60°     148.29°
    4       2.000e+02    4.955e+01    2.331e-01    -154.13°    -162.44°
    5       2.500e+02    5.665e+01    2.665e-01       5.84°      -2.47°
    6       3.000e+02    8.688e+01    4.088e-01      88.01°      79.70°
    7       3.500e+02    9.801e+01    4.612e-01    -148.57°    -156.89°
    8       4.000e+02    1.598e+02    7.519e-01     -42.38°     -50.69°
    9       4.500e+02    1.161e+02    5.465e-01      52.17°      43.86°
Total Harmonic Distortion: 125.489002%(11260.698195%)
```

Figure 89. THD of the inverter with a LCL filter.

Fig. 89 shows the total harmonic distortion with the filter. This value gives more questions than answers such as this value is higher than without the filter even that is clearly seen in Fig 86 that there is less noise, and the waveform adopts a sinusoidal form. The higher value of the THD is probably due to the beginning of the results, as we commented before, at the start of the graph the results are far from being sinusoidal but after some time these changes. Although the THD value is higher it is obvious that the introduction of the filter is positive to the work of the inverter.

CONCLUSION

The incorporation of renewable energies in the electricity sector has experienced significant growth in recent years, and three-phase inverters play a fundamental role in this transformation. In this final master's project, the operation of inverters and their modulation techniques have been studied in depth, creating circuits in LTspice and analyzing their behavior by changing different variables and adding elements to improve their operation.

In the first place, the basic operation of triphasic inverters and their relationship with renewable energies have been investigated. These electronic devices are essential for converting direct current generated by sources such as solar or wind power into alternating current, which is the form of energy used in most electrical systems. Three-phase inverters allow the interconnection of renewable energy installations to the electricity grid, facilitating the integration of these sources into the global energy supply.

Secondly, all the types of three-phase inverters that are currently available have been investigated, analyzing their suitability depending on the application and comparing them with each other. In addition, the different modulation techniques used in these inverters have been studied and analyzed.

Finally, using LTspice all the types of circuits and the most important modulation techniques have been tested, changing some parameters to analyze it behavior and adding elements to improve the results obtained.

In conclusion, three-phase inverters play a crucial role in the transition towards a more sustainable energy system and the effective integration of renewable energies. These devices allow the efficient conversion of direct current generated by renewable sources into alternating current, maximizing the efficiency of the facilities and ensuring the stability of the electrical network.

REFERENCES

Kharjule, S. (2015, October). Voltage source inverter. In 2015 International Conference on Energy Systems and Applications (pp. 537-542). IEEE.

Rashid, M. H. (Ed.). (2017). Power electronics handbook. Butterworth-heinemann.

Khanna, V. K. (2004). Insulated gate bipolar transistor IGBT theory and design. John Wiley & Sons.

World Electrical Power Generation, US Dept. of Energy, May 2009, EIA (Energy Information Agency).

Xue, Y., Chang, L., Kjaer, S. B., Bordonau, J., & Shimizu, T. (2004). Topologies of single-phase inverters for small distributed power generators: an overview. IEEE transactions on Power Electronics, 19(5), 1305-1314.

Youssef, M., Boubahri, C., Aloui, F., & Fetni, S. (2020). Simulation and design of a single phase inverter with digital PWM issued by an Arduino board. International Journal of Engineering Research & Technology, 9(08), 560-566.

Azmi, S. A., Shukor, A. A., & Rahim, S. R. A. (2018, December). Performance evaluation of single-phase H-bridge inverter using selective harmonic elimination and sinusoidal PWM techniques. In 2018 IEEE 7th International Conference on Power and Energy (PECon) (pp. 67-72). IEEE.

Soomro, J., Memon, T. D., & Shah, M. A. (2016, November). Design and analysis of single phase voltage source inverter using Unipolar and Bipolar pulse width modulation techniques. In 2016 International Conference on Advances in Electrical, Electronic and Systems Engineering (ICAEES) (pp. 277-282). IEEE.

Suresh, L. P. (2016, March). A brief review on multi level inverter topologies. In 2016 international conference on circuit, power and computing technologies (ICCPCT) (pp. 1-6). IEEE.

Nordvall, A. (2011). Multilevel inverter topology survey.

Koshti, A. K., & Rao, M. N. (2017, February). A brief review on multilevel inverter topologies. In 2017 International Conference on Data Management, Analytics and Innovation (ICDMAI) (pp. 187-193). IEEE.

Bendre, A., Krstic, S., Meer, J. V., & Venkataramanan, G. (2004, October). Comparative evaluation of modulation algorithms for neutral point clamped converters. In Conference Record of the 2004 IEEE Industry Applications Conference, 2004. 39th IAS Annual Meeting. (Vol. 2, pp. 798-805). IEEE.

Zafari, A., Mehrasa, M., Sharifzadeh, M., Bacha, S., Al-Haddad, K., & Hosseinzadeh, N. (2021, October). A nine-level PEC based active power filter with double-frequency oscillation cancellation (DFOC) ability in reference current detection. In IECON 2021–47th Annual Conference of the IEEE Industrial Electronics Society (pp. 1-6). IEEE.

Çolak, I., & Kabalci, E. (2008). A review on inverter topologies and developments. Proceedings of Eleco. Song, B. M., Kim, J., Lai, J. S., Seong, K. C., Kim, H. J., & Park, S. S. (2001). A multilevel soft-switching inverter with inductor coupling. IEEE Transactions on Industry Applications, 37(2), 628-636.

Song, B. M., Kim, J., Lai, J. S., Seong, K. C., Kim, H. J., & Park, S. S. (2001). A multilevel soft-switching inverter with inductor coupling. IEEE Transactions on Industry Applications, 37(2), 628-636.

Kuhn, H., Ruger, N. E., & Mertens, A. (2007, June). Control strategy for multilevel inverter with non-ideal dc sources. In 2007 IEEE Power Electronics Specialists Conference (pp. 632-638). IEEE.

Rodriguez, J., Lai, J. S., & Peng, F. Z. (2002). Multilevel inverters: a survey of topologies, controls, and applications. IEEE Transactions on industrial electronics, 49(4), 724-738.

Ismail, B., Taib, S., Saad, A. M., Isa, M., & Hadzer, C. M. (2006, November). Development of a single phase SPWM microcontroller-based inverter. In 2006 IEEE International Power and Energy Conference (pp. 437-440). IEEE.

Colak, I., Kabalci, E., & Bayindir, R. (2011). Review of multilevel voltage source inverter topologies and control schemes. Energy conversion and management, 52(2), 1114-1128.

Gupta, A. K., & Khambadkone, A. M. (2006). A space vector PWM scheme for multilevel inverters based on two-level space vector PWM. IEEE Transactions on industrial electronics, 53(5), 1631-1639.

Feng, C., Liang, J., Agelidis, V. G., & Green, T. C. (2006, November). A multi-modular system based on parallel-connected multilevel flying capacitor converters controlled with fundamental frequency SPWM. In IECON 2006-32nd Annual Conference on IEEE Industrial Electronics (pp. 2360-2365). IEEE.

Escobar, G., Martinez, P. R., & Leyva-Ramos, J. (2007). Analog circuits to implement

repetitive controllers with feedforward for harmonic compensation. IEEE Transactions on Industrial Electronics, 54(1), 567-573.

Loh, P. C., Bode, G. H., & Tan, P. C. (2005). Modular hysteresis current control of hybrid multilevel inverters. IEE Proceedings-Electric Power Applications, 152(1), 1-8.

CHEN, R., XU, Z., & NI, Y. (2004). A new current control method based on SVM in αβ0 coordinate system. In 2004 IEEE Power Engineering Society general meeting (Denver CO, 6-10 June 2004).

Siwakoti, Y. P., Forouzesh, M., & Pham, N. H. (2018). Power electronics converters—An overview. Control of Power Electronic Converters and Systems, 3-29.

Steinke, J. K. (1999). Use of an LC filter to achieve a motor-friendly performance of the PWM voltage source inverter. IEEE transactions on Energy Conversion, 14(3), 649-654.

Ahmed, K. H., Finney, S. J., & Williams, B. W. (2007, May). Passive filter design for three-phase inverter interfacing in distributed generation. In 2007 Compatibility in Power Electronics (pp. 1-9). IEEE.

Twining, E., & Holmes, D. G. (2003). Grid current regulation of a three-phase voltage source inverter with an LCL input filter. IEEE transactions on power electronics, 18(3), 888-895.

El-Habrouk, M., Darwish, M. K., & Mehta, P. (2000). Active power filters: A review. IEE Proceedings-Electric Power Applications, 147(5), 403-413.

Singh, H., Kour, M., Thanki, D. V., & Kumar, P. (2018). A review on Shunt active power filter control strategies. International Journal of Engineering & Technology, 7(4.5), 121-125.

Hoon, Y., Mohd Radzi, M. A., Hassan, M. K., & Mailah, N. F. (2017). Control algorithms of shunt active power filter for harmonics mitigation: A review. Energies, 10(12), 2038.

Hoon, Y., Radzi, M. A. M., Hassan, M. K., Mailah, N. F., & Wahab, N. I. A. (2016). A simplified synchronous reference frame for indirect current controlled three-level inverter-based shunt active power filters. Journal of Power Electronics, 16(5), 1964-1980.

Hoon, Y., Mohd Radzi, M. A., Hassan, M. K., & Mailah, N. F. (2016). Enhanced instantaneous power theory with average algorithm for indirect current controlled three-level inverter-based shunt active power filter under dynamic state conditions. Mathematical Problems in Engineering, 2016.