Sizing and short-circuit capability of a transformerless HVDC DC-DC converter

R. Vidal-Albalate, D. Soto-Sanchez, *Member, IEEE*, E. Belenguer, *Member, IEEE*, R. Peña, *Senior Member, IEEE*, R. Blasco-Gimenez, *Senior Member, IEEE*

***Abstract*—This work aims at optimizing the converter design of the double-T MMC DC-DC converter in terms of transmitted power per submodule and also in terms of transmitted power per silicon area, while, at the same time, providing the capability to block dc faults. Firstly, the converter operation is described and the optimal values of the inner ac and dc voltages that minimize device power rating are derived. Next, the submodule topology is analyzed and a thorough study on the converter capability for blocking fault currents is carried out, showing that the converter is able to isolate dc faults both at the input and at the output of the converter. Finally, the previous analytical study is verified by means of detailed PSCAD simulations.**

***Index Terms*—dc-dc power conversion, fault blocking capability, HVdc grids, modular multilevel converter.**

I. Nomenclature

Subscripts:

$k(k = 1 \cdots k_T)$	number of T-section
p, n	positive and negative pole
$x = ise, ose, de$	branch names (input branch, output branch, derivation branch)

Variables:

V_{dci}	input dc voltage
V_{dco}	output dc voltage
V_{dcm}	inner dc voltage
I_{dci}	input dc current
I_{dco}	output dc current
I_x	dc current through the branch "x"
v_u	branch ac voltage
V_u	amplitude of v_u
i_{iu}	input ac circulating current
i_{ou}	output ac circulating current
I_{iu}	amplitude of the input ac circulating current
I_{ou}	amplitude of the output ac circulating current
i_x	current through the branch "x"
f_u	frequency of the circulating currents
i_q	ac current for balancing capacitor voltages
I_q	amplitude of i_q
k_T	number of parallel T-sections
N_x	number of SMs in branch "x"
N_{HB}	number of half-bridge SMs
N_{FB}	number of full-bridge SMs
k_r	transformation ratio (V_{dci}/V_{dco})
k_s	voltage safety margin
V_c	capacitor voltage
V_{cx}^{Σ}	sum of the capacitor voltages of the branch "x"
P_x	average exchanged power by branch "x"
W_x	average energy in branch "x"
P_{r_x}	installed power in branch "x"
P_T	nominal dc power transmitted by each T-section
P_{dco}	output dc power
P_{dci}	input dc power

Uppercase variables (voltages/currents) represent dc components or peak values of the ac variables and lowercase variables represent ac variables.

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R. Vidal-Albalate and E. Belenguer are with the Universitat Jaume I, 12071 Castelló de la Plana, Spain (e-mail: rvidal@uji.es, efbeleng@uji.es).

D. Soto is with the University of Magallanes, Punta Arenas, 6210427, Chile (diego.soto@umag.cl)

Rubén Peña is with Universidad de Concepción, Concepción, Chile (e-mail: rupena@udec.cl)

R. Blasco-Gimenez is with the Universitat Politècnica de València, 46022 València, Spain (email: r.blasco@ieee.org).

II. Introduction

HIGH voltage direct current (HVdc) links based on voltage source converters (VSCs) are the prevailing solution for the connection of distant offshore wind power plants. These links, which currently are point-to-point, are paving the way for future multiterminal HVdc (MT-HVdc) grids. However, interconnection of HVdc grids with different voltage levels will require dc-dc converters [1], [2].

Several topologies of dc-dc converters, including isolated and non-isolated dc-dc converters, have been proposed for HVdc grids. Isolated dc-dc converters make use of a transformer and two front-to-front connected dc-ac converters to build a dc-ac-dc converter. Topologies such as the modular multilevel converter (MMC) [3], the alternate arm converter (AAC) [4], or diode rectifiers if bidirectional power flow is not required [5] can be used for the ac-dc converters. Alternatively, the voltage transformation can be achieved by means of a series or parallel connection of several dual-active bridges (DABs) [6]. However, for low and medium voltage transformation ratios, these topologies result in a low utilization of the installed power semiconductor devices and relatively high losses [7], [8].

In the autotransformer (HVdc-AT) topology [8] [9], both dc-ac and ac-dc converters are merged and the power transfer is shared by the converters and the transformer. Hence, the converter and transformer rated powers are diminished and overall efficiency is increased [8]. However, the isolation between both dc grids is lost despite using a transformer.

In non-isolated converters the voltage transformation is carried out by the MMC itself [10], hence, the transformer is eliminated and both losses and converter footprint are reduced. However, inner ac voltages and circulating currents are needed

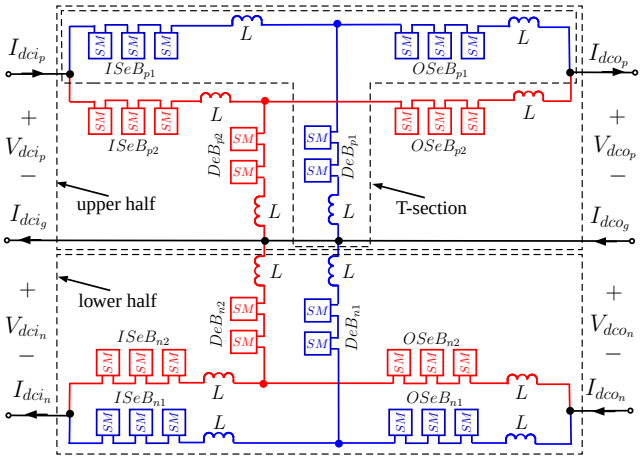


Fig. 1: Structure of the T-converter topology.

to compensate for the energy drift on the MMC branches [7]. The double-Π topology creates a constant pole-to-pole voltage, however, the pole-to-ground voltages present a noticeable ripple [11]. This ripple is eliminated by means of coupled inductors and capacitors in [12], [13]. However, coupled inductors of such power and voltage rating are not currently available, introduce a single point of failure in the converter and, if not accurately matched, could lead to ac residual currents circulating through the dc poles.

The inner ac circulating currents can also be prevented from flowing through the dc poles by using several capacitors rated for hundreds of kilovolts and connected between the midpoints of the converter branches [14]. However, as in the previous case, avoiding such large passive components is advisable in terms of reliability and risk of ac currents flowing to the dc poles.

In [15] a T-converter, which consists of two series-connected double-Π converters, uses two shunt branches to keep the ac voltages and currents inside the converter. Conversely, by paralleling two or more legs in the T-converter, the inner circulating currents can be made to flow from one leg to the other one. Thus, this configuration eliminates the need for shunt branches or dc link capacitors and increases the power device utilization and dc current handing [16]–[18]. On the other hand, the hybrid-cascaded converter uses the submodule (SM) capacitors as energy buffers to cyclically transmit power from the input to the output [19]. However, the current flow through each branch is discontinuous and high switching frequencies are required.

DC faults in HVdc grids are of major concern [20]–[25]. Isolated dc-dc transformers have dc fault blocking capability [24]. Conversely, the HVdc-AT and the non-isolated topologies cannot block dc faults unless a large number of additional full-bridge SMs, which are not required during the normal operation of the converter, are added at the expense of higher converter losses and lower power device utilization [9], [12], [25]. In this context, a dc-dc converter with fault blocking capability can reduce the overall cost of dc-dc converter and dc breaker and hence contribute to develop future multiterminal HVdc grids [26].

The power rating of non-isolated converters rapidly increases with the voltage transformation ratio. The higher the transformation ratio, the higher the auxiliary ac voltage

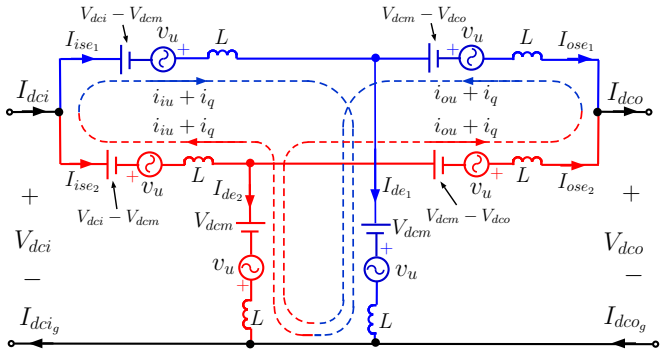


Fig. 2: Equivalent circuit of the converter.

and ac current needed to exchange energy amongst branches and to maintain the energy balance. These auxiliary ac components reduce the available voltage and current for the dc components, thus decreasing the power transfer capability. Moreover, inadequate selection of the amplitude of the auxiliary ac voltage and the inner dc voltage, which are two degrees of freedom in non-isolated dc-dc MMC design, may result in such a poor utilization of the power semiconductor devices that the converter becomes impractical. The influence of the value of the inner ac voltage and the capacitor voltages is analyzed in [27] with the aim of minimizing the ac circulating current. However, minimizing the circulating current does not ensure that the transmitted power per SM is optimized since it requires adding additional SMs. Moreover, no recommendations regarding the optimal values are provided in [27]. The design criterion in [28] is to use only HB-SMs in all branches. However, this criterion does not ensure that the transmitted power per SM is maximized either. In [18] the ISeb and DeB are constrained to the use of only HB-SMs regardless of the voltage ratio, which severely limits the transmitted power when operating at a high and close to unit step ratios.

In this paper, the double T-converter, whose topology and controls were presented in [16], [28], is analysed with the following objectives: i) optimal sizing in terms of installed capacity, that is, maximize the power transfer capability per SM, and ii) study of the converter fault blocking capability to isolate dc faults. Hence, the main goal is to carry out a thorough study of the double T-converter to obtain the optimal converter sizing and, at the same time, maximize converter functionality. Both these two issues are of particular relevance for the evaluation of this converter for actual projects.

III. Converter Description

The structure of the dc-dc T-converter is shown in Fig. 1, where the variables of the upper and lower halves are denoted with subscripts “p” and “n”, respectively. Each half consists of k_T T-sections connected in parallel (the T-sections are identified with subscripts “1”, “2”, etc.) and each T-section has three branches named input series (ISeB), derivation (DeB), and output series (OSeB), respectively (hereinafter the variables related to each branch are denoted with subscripts “ise”, “de” and “ose”, respectively). The branches consist of an arrangement of N cascaded SMs, where N can be different for each branch. Although only two T-sections ($k_T = 2$) are shown in Fig. 1, a higher number can be connected to increase the converter power handling.

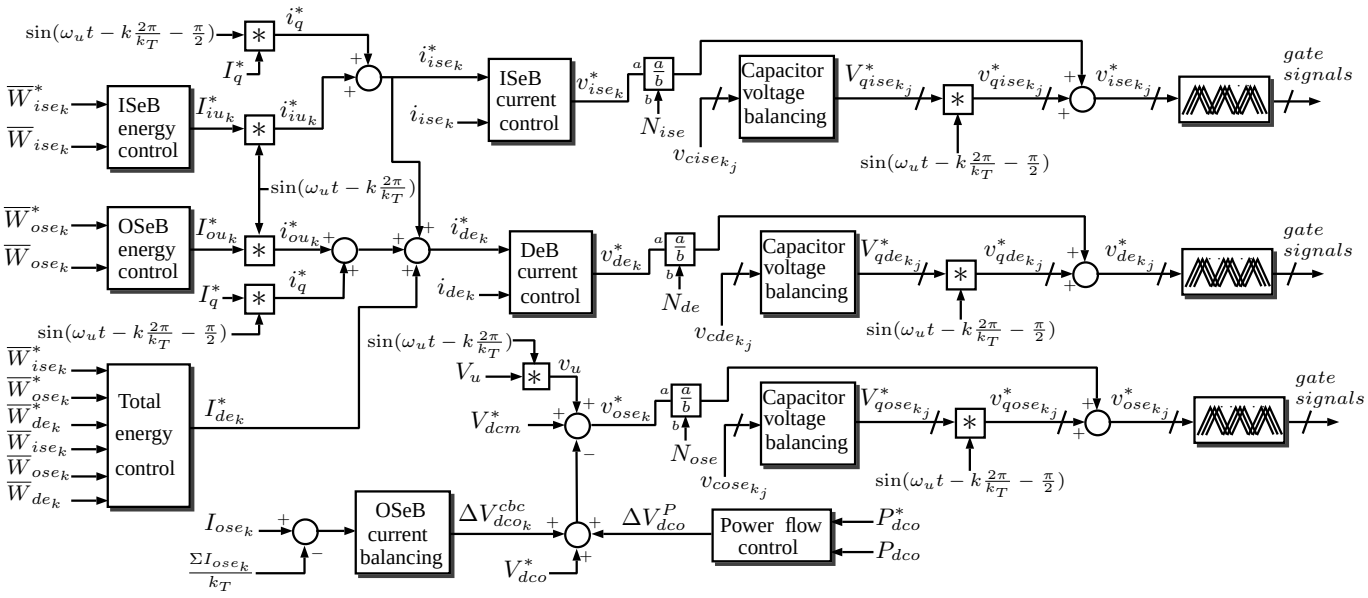


Fig. 3: Control of the converter (arrays of signals are represented with a crossed line).

IV. Converter control

Fig. 2 shows an equivalent circuit of the top half of the converter. Given that both halves operate in a similar manner, only the upper part will be analyzed. Moreover, the control of all T-sections is the same, thus, for the sake of generalization, subscripts "1", "2", "p" and "n" will be omitted hereinafter.

At the beginning, each branch should only generate a dc voltage and force the dc current to flow through it to transfer power between the input and the output. However, this would cause branch energy drifts, that is, sustained charge/discharge of the SM capacitors. Given that when the ISeB/OSeB dc current is positive the dc current through the DeB is negative, the energy drifts in the ISeB/OSeB and DeB are opposite. Hence, the SM capacitors of the ISeB/OSeB are charged whereas the SM capacitors of the DeB are discharged or vice versa, depending on the power transfer direction. To avoid this situation, ac voltages and currents are used in each branch so that the power exchanged by the dc components is balanced with the power exchanged by the ac components. In this way the net exchanged energy is zero and the averaged SM capacitor voltages remains constant. Moreover, to avoid circulating ac currents flowing through the dc poles, the T-sections operate in an interleaved manner, i.e., the auxiliary ac voltages and currents are shifted $2\pi/k_T$ rad. A diagram of the control of the T-sections is shown in Fig. 3 [16].

A. Branch energy control

To keep the branch energies constant, auxiliary internal ac branch voltages (v_u) and circulating ac currents (i_{iu} and i_{ou}) are required to exchange energy amongst the branches, Fig. 2. This enables to transfer energy from the branches having an excess of energy to those having a deficit of energy. Provided that the amplitude of the ac voltage v_u is kept constant, the amplitude of the currents i_{iu} and i_{ou}, which depending on the direction of the power exchange are set to be in-phase or anti-phase to v_u, determine the energy transfer between branches. The ac voltage of each T-section is defined as:

$$v_{u_k} = V_u \sin\left(2\pi f_u t - k\frac{2\pi}{k_T}\right) \qquad k = 1 \cdots k_T \tag{1}$$

where V_u and f_u are the amplitude and frequency, respectively.

From Fig. 2, the average power exchanged by each branch is as given in (2a)-(2c). Note that i_q is a circulating ac current intended to balance the SM capacitor voltages within each branch. For this reason, i_q is controlled to be in quadrature to v_u and does not exchange active power amongst branches. Hence, this current component helps in redistributing the energy amongst SMs without affecting the branch energy [16].

$$P_{ise_k} = \frac{d\overline{W}_{ise_k}}{dt} = (V_{dci} - V_{dcm})\, I_{ise_k} - \frac{V_u I_{iu_k}}{2} \tag{2a}$$

$$P_{de_k} = \frac{d\overline{W}_{de_k}}{dt} = V_{dcm} I_{de_k} + \frac{V_u\,(I_{iu_k} + I_{ou_k})}{2} \tag{2b}$$

$$P_{ose_k} = \frac{d\overline{W}_{ose_k}}{dt} = (V_{dcm} - V_{dco})\, I_{ose_k} - \frac{V_u I_{ou_k}}{2} \tag{2c}$$

According to (2a) and (2c), the energy of the ISeB and OSeB can be controlled by setting the amplitude of the ac circulating currents i_{iu_k} and i_{ou_k}, that is, I_{iu_k} and I_{ou_k}, respectively. The dc components I_{ise_k} and I_{ose_k} are considered as disturbances since they directly depend on the output current. Adding (2a), (2b) and (2c) yields to:

$$\frac{d\overline{W}_{ise_k}}{dt} + \frac{d\overline{W}_{de_k}}{dt} + \frac{d\overline{W}_{ose_k}}{dt} = V_{dcm}\left(\left(1 - \frac{V_{dco}}{V_{dci}}\right) I_{ose_k} + I_{de_k}\right) \tag{3}$$

The total converter energy is controlled by means of I_{de_k}. In all cases PI controllers that set the values of I_{iu_k}, I_{ou_k} and I_{de_k} are used to regulate the branch energies.

B. Capacitor balancing control

The circulating current i_q redistributes the energy amongst the capacitors within a branch. The value of this current is:

$$i_{q_k} = I_q \sin\left(2\pi f_u t - k\frac{2\pi}{k_T} - \frac{\pi}{2}\right) \qquad k = 1 \cdots k_T \tag{4}$$

Each SM also creates an ac voltage v_{q_j} ($j = 1 \cdots N$), which is in phase or shifted $180°$ from the circulating current i_{q_k}, to extract/inject power from/to each particular SM capacitor. For this purpose, each capacitor voltage deviation with respect to the branch average capacitor voltage is fed into a PI that sets

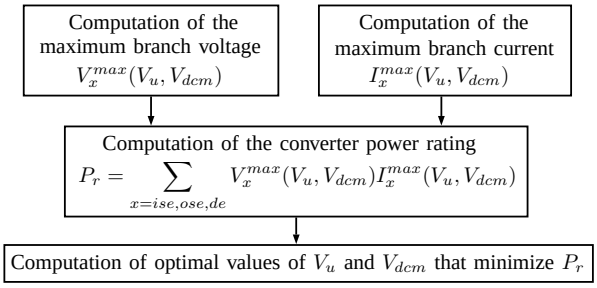


Fig. 4: Optimal SM power rating.

the amplitude of v_{q_j} [16]. As shown in Fig. 3, synthesis of the branch voltage is based on the PWM technique. However, other modulation techniques, like the Nearest Voltage Level, together with the Sort and Select method to maintain balance of the capacitor voltages can be used [29].

C. Branch current control

According to Fig. 2, the branch currents are:

$$i_{ise_k} = I_{ise_k} + I_{iu_k}\sin\left(2\pi f_u t - k\frac{2\pi}{k_T}\right) + I_q \sin\left(2\pi f_u t - k\frac{2\pi}{k_T} - \frac{\pi}{2}\right) \tag{5a}$$

$$i_{de_k} = I_{de_k} + \left(I_{iu_k} + I_{ou_k}\right)\sin\left(2\pi f_u t - k\frac{2\pi}{k_T}\right) + 2I_q \sin\left(2\pi f_u t - k\frac{2\pi}{k_T} - \frac{\pi}{2}\right) \tag{5b}$$

$$i_{ose_k} = I_{ose_k} - I_{ou_k}\sin\left(2\pi f_u t - k\frac{2\pi}{k_T}\right) - I_q \sin\left(2\pi f_u t - k\frac{2\pi}{k_T} - \frac{\pi}{2}\right) \tag{5c}$$

PI and PR controllers that set the branch voltages ($v^*_{ise_k}$, $v^*_{de_k}$, $v^*_{ose_k}$) are used to control the dc and ac components of the branch currents, respectively, as shown in Fig. 3.

D. Output current and power sharing control

To prevent ac current from flowing through the dc poles, the dc current flowing through each T-section has to be the same. In this way the amplitude of the ac current through each T-section is also the same ($I_{iu_1} = I_{iu_2} = \cdots = I_{iu_{k_T}}$ and $I_{ou_1} = I_{ou_2} = \cdots = I_{ou_{k_T}}$) and the ac components of the branch currents cancel out.

$$I_{ose_k} = I_{ose} = \frac{I_{dco}}{k_T} \tag{6a}$$

$$I_{ise_k} = I_{ise} = \frac{I_{dci}}{k_T} = \frac{V_{dco}}{V_{dci}}\frac{I_{dco}}{k_T} \tag{6b}$$

For this purpose, a current balancing control balances the dc current through each OSeB. This control adjusts the dc component of the DeB voltage of each T-section ($\Delta V^{cbc}_{dco_k}$) so the overall current is equally shared amongst the k_T sections. Moreover, the overall output current is controlled by the power flow control that adjust the output dc voltage (ΔV^{P}_{dco}).

V. Converter Analysis

According to Fig. 2, the inner ac voltage (V_u) and the dc voltage (V_{dcm}) do not affect the voltage conversion. Therefore the values of these two variables can be freely chosen to optimize the SM utilization. In this section, a study is carried out with the aim of maximizing the power that can be transmitted per SM. Although it is done for the T-topology, the study could be extended to any dc-dc topology that has some degree of freedom with regard to the inner converter variables (voltages and/or currents) used for the branch energy control.

A. Optimal SM power rating

The total SM power rating required to handle the rated output dc power (i.e. the installed power in terms of SMs), expressed as a ratio of the rated output dc power, is a useful measure of the utilization SMs. Optimization of this ratio results in a converter having the least requirements in SM and capacitor counting, that is, maximizes the transmitted power per SM. Considering steady-state operation, the installed power (*maximum branch voltage x maximum branch current*) is computed according to the flow chart shown in Fig 4:

$$P_{r_{ise}} = V^{\max}_{ise} I^{\max}_{ise} = \left(|V_{dci} - V_{dcm}| + V_u\right)\left(|I_{ise}| + |I_{iu}|\right) \tag{7a}$$

$$P_{r_{de}} = V^{\max}_{de} I^{\max}_{de} = \left(V_{dcm} + V_u\right)\left(|I_{de}| + |I_{iu}| + |I_{ou}|\right) \tag{7b}$$

$$P_{r_{ose}} = V^{\max}_{ose} I^{\max}_{ose} = \left(|V_{dcm} - V_{dco}| + V_u\right)\left(|I_{ose}| + |I_{ou}|\right) \tag{7c}$$

Using (6), the dc component of the DeB current is:

$$I_{de} = \left(\frac{V_{dco}}{V_{dci}} - 1\right)\frac{I_{dco}}{k_T} \tag{8}$$

Similarly, considering power balance between dc and ac branch power exchange, the ac current amplitude of the ISeB and OSeB currents is:

$$I_{iu} = 2\frac{V_{dci} - V_{dcm}}{V_u}\frac{V_{dco}}{V_{dci}}\frac{I_{dco}}{k_T} \tag{9a}$$

$$I_{ou} = 2\frac{V_{dcm} - V_{dco}}{V_u}\frac{I_{dco}}{k_T} \tag{9b}$$

Unlike the dc current, the amplitude of circulating current depends on the auxiliary ac voltage amplitude and the dc voltage at the T-section midpoint. Substituting the ac and dc branch currents given in (6), (8) and (9) into the power ratings in (7), the total power rating (P_r) of the converter, in per-unit of the output power ($P_{dco} = V_{dco}I_{dco}$), is as given in (10).

$\circ\ V_{dco} \geq V_{dcm}$: (10a)

$$P_r = \frac{2}{V_{dci}V_{dco}V_u}(V^2_{dci}V_{dco} + V_{dci}V^2_{dco} + 5V_{dci}V_{dco}V_u - 2V_{dci}V_{dco}V_{dcm} + V_{dci}V^2_u - 2V_{dci}V_{dcm}V_u - 3V_{dco}V_{dcm}V_u)$$

$\circ\ V_{dci} \geq V_{dcm} \geq V_{dco}$: (10b)

$$P_r = \frac{2}{V_{dci}V_{dco}V_u}(V^2_{dci}V_{dco} + 2V_{dci}V^2_{dcm} - 4V_{dci}V_{dco}V_{dcm} + 3V_{dci}V_{dcm}V_u + V_{dci}V^2_{dco} + V_{dci}V^2_u - 3V_{dco}V_{dcm}V_u)$$

$\circ\ V_{dcm} \geq V_{dci}$: (10c)

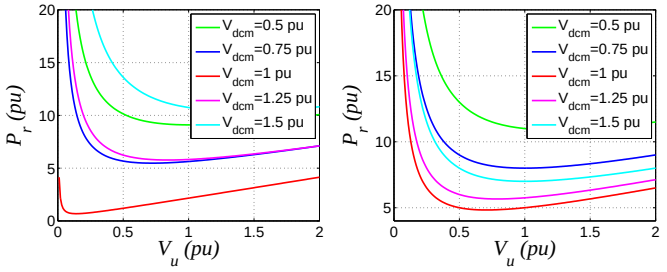
$$P_r = \frac{2}{V_{dci}V_{dco}V_u}(V^2_{dci}V_{dco} + 2V_{dci}V^2_{dcm} - 6V_{dci}V_{dco}V_{dcm} + 3V_{dci}V_{dcm}V_u + V_{dci}V^2_{dco} - 5V_{dci}V_{dco}V_u + V_{dci}V^2_u + 2V_{dco}V^2_{dcm} + 2V_{dco}V_{dcm}V_u)$$

The values of V_u and V_{dcm} that minimize the power rating are:

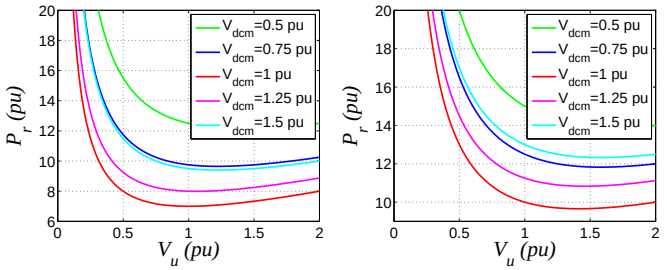
$$V_{dcm} = V_{dco} \tag{11a}$$

$$V_u = V_{dco}\sqrt{\frac{V_{dci}}{V_{dco}} - 1} = V_{dco}\sqrt{k_r - 1} \tag{11b}$$

Note that minimization of the power rating requires $V_{dcm} = V_{dco}$. This is explained by the fact that for the same dc voltage drop in the series branches ($V_{dci} - V_{dcm} = V_{dcm} - V_{dco}$), the ISeB requires an ac circulating current that is k_r ($k_r =$

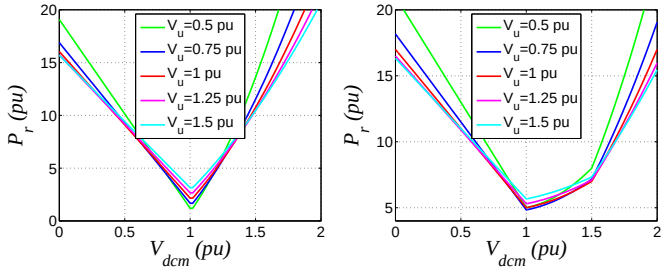


(a) $k_r = 1.02$ (b) $k_r = 1.5$

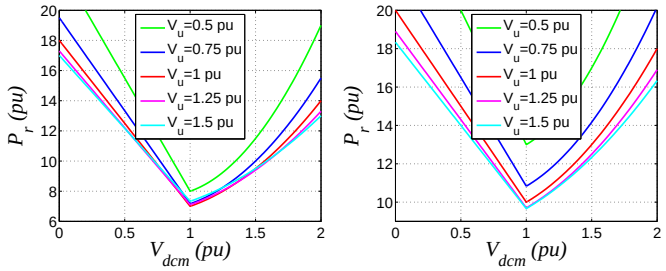


(c) $k_r = 2$ (d) $k_r = 3$

Fig. 5: Converter power rating as a function of V_u.



(a) $k_r = 1.02$ (b) $k_r = 1.5$



(c) $k_r = 2$ (d) $k_r = 3$

Fig. 6: Converter power rating as a function of V_{dcm}.

V_{dci}/V_{dco} with $V_{dci} > V_{dco}$) times smaller than that needed in the OSeB as given in (9). Thus, the dc voltage drop between the input and output sides must be inserted in the ISeB.

Fig. 5 shows the converter power rating (P_r) as a function of V_u for four voltage ratios (k_r) and five values of the inner dc voltage (with $V_{dco} = 1$ pu). The power rating for low values of V_u increases sharply due to the high circulating currents needed to transfer energy amongst the branches. Thus, most of the IGBTs current capability is used to handle the ac currents, which limits the dc power transfer. However, the power rating curves are relatively constant around the optimal value of V_u that minimizes the power rating. Hence, it is feasible to slightly modify V_u around this optimal point to take into account other design requirements that will be discussed later, for instance, the fault current blocking capability or the type of SMs.

Fig. 6 shows the power rating of the converter as a function of V_{dcm} for four voltages ratios and five values of the amplitude of the ac voltage. The slope of the power rating curves is quite pronounced around the optimal point. Hence, it is not advisable to select values of the inner dc voltage that do not correspond to the optimal voltage.

The previous results highlight the importance of a proper selection of the auxiliary ac voltage and midpoint dc voltage to avoid extremely high power ratings that lead to a low utilization of the installed power. Substituting (11) in (10b), the optimal power rating is:

$$P_{r,opt}\left(k_r\right) = \frac{6\sqrt{\left(k_r-1\right)^3} - 4k_r + 4k_r^2}{k_r\sqrt{k_r-1}} \tag{12}$$

Fig. 7 shows the minimum power rating in terms of SMs as a function of k_r (with $V_{dco}I_{dco} = 1\ pu$) when the optimal values of V_u and V_{dcm} given by (11) are used. High voltages ratios require large circulating currents, thus, most of the current capability of the IGBTs is used to handle the ac currents, which limits the dc power transfer.

A similar study has been carried out for the conventional

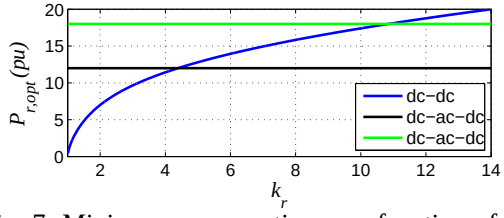


Fig. 7: Minimum power rating as a function of k_r.

dc-ac-dc [3] that uses to front-to-front ac-dc converters and a transformer. The balance between the dc and ac sides of one converter is:

$$3\frac{V_{ac}I_{ac}}{2} = 2V_{dco}I_{dco} \tag{13}$$

where V_{ac} and I_{ac} are the peak values of the ac voltages and currents, respectively. Taking into account that the peak ac voltage equals the dc voltage when HB-SMs are used, the previous equation can be simplified to:

$$I_{ac} = \frac{4}{3}I_{dco} \tag{14}$$

The peak value of the current through each branch of the converter is:

$$I_{br} = \frac{I_{dco}}{3} + \frac{I_{ac}}{2} = I_{dco} \tag{15}$$

The maximum branch voltage equals the dc pole-to-pole voltage. Hence, the installed power (*maximum branch voltage x maximum branch current*) in per-unit in the six branches of both converters is:

$$P_r = 2\frac{6I_{dco}2V_{dco}}{2V_{dco}I_{dco}} = 12 \tag{16}$$

Regardless of the voltage ratio, the dc-ac-dc converter needs an installed power in the power converters that is twelve times the power that can transfer. Thus, the dc-dc converter is able to transfer more energy with the same amount of SMs for voltages ratios lower than 4.4, see Fig. 7. However, in contrast to the dc-dc converter, the dc-ac-dc converter also needs a transformer. If the power rating of the transformer,

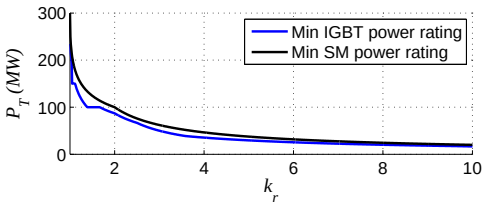


Fig. 8: Nominal dc power of each T-section.

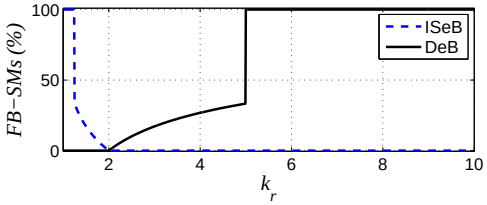


Fig. 9: Proportion of FB-SMs in the ISeB and DeB.

taken as the sum of the VA rating of the transformer windings, is considered in the analysis, for the same total installed power, the dc-dc converter will be able to transfer more power between the dc grids for voltages ratios lower than 10.85, see Fig. 7. Hence, the converter is specially suitable for applications that require low or medium voltage transformation ratios, for instance, for the interconnection of HVdc lines of comparable voltage rating to form HVdc grids, and the control of power in such dc networks.

B. Rated power

Neglecting i_q, the peak value of the currents through the ISeB and DeB is:

$$i_{ise}^{\max} = |I_{ise}^{\max}| + |I_{iu}^{\max}| = \frac{1}{k_r} I_{dco} + \frac{2}{k_r} \frac{V_{dci} - V_{dco}}{V_u} I_{dco} \quad (17a)$$

$$i_{de}^{\max} = |I_{de}^{\max}| + |I_{iu}^{\max}| = \frac{k_r - 1}{k_r} I_{dco} + \frac{2}{k_r} \frac{V_{dci} - V_{dco}}{V_u} I_{dco} \quad (17b)$$

From the previous expressions it can be seen that the branch that carries a higher current is:

$$i_{ise}^{\max} > i_{de}^{\max} \qquad k_r < 2 \quad (18a)$$

$$i_{ise}^{\max} < i_{de}^{\max} \qquad k_r > 2 \quad (18b)$$

Considering that the maximum IGBT current is I^{max}, the maximum dc currents can be obtained from (6) and (17):

$$\begin{aligned} I_{ise}^{max} &= \frac{1}{1 + 2\sqrt{k_r - 1}} I^{max} \\ I_{de}^{max} &= \frac{\sqrt{k_r - 1}}{\sqrt{k_r - 1} + 2} I^{max} \end{aligned} \quad (19)$$

The nominal dc power of each T-section is:

$$\begin{aligned} P_T &= V_{dci} I_{ise}^{max} \qquad k_r \leq 2 \\ P_T &= V_{dci} \frac{1}{k_r - 1} I_{de}^{max} \qquad k_r \geq 2 \end{aligned} \quad (20)$$

Fig. 8 (black trace) shows the nominal dc power of each T-section (i.e. the transmitted dc power) for $V_{dci} = 300$ kV and $I^{max} = 1$ kA when the optimal values of V_u and V_{dcm} given by (11) are used. As the voltage ratio k_r increases, the ac circulating currents also increase and the nominal dc power decreases. Hence, the T-topology is more convenient for relatively small voltage ratios in terms of power transmitted per SM. For large voltage ratios, the size of the considered converter will be too large and other topologies offer better power transmitted per SM (see Fig. 7).

C. SM type

Depending on the maximum and minimum values of each branch voltage, the corresponding branch requires half-bridge SMs (HB-SMs) or full-bridge SMs (FB-SMs). Considering the optimal values for V_{dcm} and V_u, the branch voltages are:

$$v_{ise} = V_{dci} - \left(V_{dco} + V_{dco} \sqrt{k_r - 1} \sin(2\pi f_u t) \right) \quad (21a)$$

$$v_{de} = V_{dco} + V_{dco} \sqrt{k_r - 1} \sin(2\pi f_u t) \quad (21b)$$

$$v_{ose} = V_{dco} \sqrt{k_r - 1} \sin(2\pi f_u t) \quad (21c)$$

If the voltages v_{ise}, v_{de}, and v_{ose} are either always positive or negative (i.e. a unipolar voltage), the corresponding branch can simply use HB-SMs. Otherwise, FB-SMs are needed. From (21), the ISeB requires FB-SMs when $k_r < 2$, the DeB needs FB-SMs when $k_r > 2$ and the OSeB always needs FB-SMs.

Note that the IseB and the DeB create a voltage that contains ac and dc components. Therefore, the branch voltages are shifted into the region of positive voltage values. Thus, these branches can use a combination of HB-SMs and FB-SMs, limiting the use of FB-SMs to the minimum required to create the negative voltage, if needed. Fig. 9 shows the proportion of FB-SMs in these two branches, which are given in (22).

$$N_{FB_{ise}}(\%) = \frac{\sqrt{k_r - 1} - k_r + 1}{k_r - 1 + \sqrt{k_r - 1}} \quad (22a)$$

$$N_{FB_{de}}(\%) = \frac{\sqrt{k_r - 1} - 1}{1 + \sqrt{k_r - 1}} \quad (22b)$$

Additionally, when the branch uses HB SMs alone, or in combination with FB SMs, the branch current should always alternate between positive and negative values within one cycle of the branch voltage. Otherwise, it is not possible to balance the HB-SMs and the FB-SMs since, depending on the direction of the current, the HB-SMs would only charge or discharge. Thus, the conditions $I_{ise} < I_{iu}$ and $I_{de} < I_{iu}$ should be met to use a combination of FH-SMs and FB-SMs in the ISeB and DeB, respectively. Otherwise, only FB-SMs can be employed.

$$\frac{V_{dco}}{V_{dci}} \frac{I_{dco}}{k_T} < 2 \frac{V_{dci} - V_{dcm}}{V_u} \frac{V_{dco}}{V_{dci}} \frac{I_{dco}}{k_T} \rightarrow 2(V_{dci} - V_{dcm}) > V_u \quad (23a)$$

$$\left(1 - \frac{V_{dcm}}{V_{dci}}\right) \frac{I_{dco}}{k_T} < 2 \frac{V_{dci} - V_{dco}}{V_u} \frac{V_{dco}}{V_{dci}} \frac{I_{dco}}{k_T} \rightarrow 2V_{dcm} > V_u \quad (23b)$$

Considering the optimal values of V_{dcm} and V_u given in (11), the conditions in (23) are met when $k_r > 1.25$ and $k_r < 5$, respectively. Taking into account the previous considerations, Fig. 9 shows the proportion of FB-SMs in these two branches.

As seen in Fig. 5, the converter power rating is relatively constant around the optimal value of V_u. This suggests that it may be possible to replace FB-SMs with HB-SMs by reducing V_u without worsen significantly the power rating.

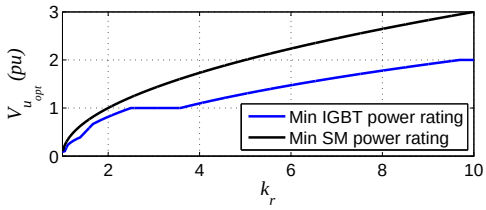


Fig. 10: Otimal value of V_u as a function of k_r.

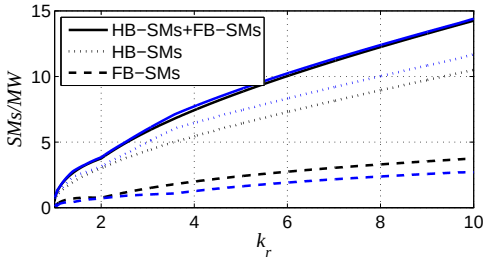


Fig. 11: Number of SMs required per MW of dc power. Black/blue: Optimal value of V_u obtained for the minimum SM/IGBT power rating is used.

D. Minimum power rating of the semiconductor power devices

The parameter P_r (P_r= *maximum branch voltage x maximum branch current*) only considers the maximum branch voltage regardless of the type of SMs that the branch actually needs to create that voltage. Therefore, it is a measure of overall voltage and current capacity of SMs that maximizes the power transmitted per SMs.

To find out the minimum (optimal) installed power in terms of IGBTs, a similar analysis to that described in section V-A for P_r, but taking into account the type of SM, is carried out. The optimal values for V_{dcm} and V_u are given in (24) and (25), respectively. The objective function (installed power in terms of IGBTs) and design constraints are in Appendix A.

$$V_{dcm} = V_{dco} \tag{24}$$

The optimal value of V_u and the type of SMs used in the ISeB/DeB/OSeB is as follows:

$$V_u = V_{dco}\sqrt{\frac{2-6k_r+4k_r^2}{1+3k_r}} \quad \text{for} \quad k_r \leq 1.046 \tag{25a}$$
FB-SMs / HB-SMs / FB-SMs

$$V_u = 2(k_r-1)V_{dco} \quad \text{for} \quad 1.046 \leq k_r \leq 1.115 \tag{25b}$$
HB-SMs and FB-SMs / HB-SMs / FB-SMs

$$V_u = V_{dco}\sqrt{\frac{2k_r-2}{1+3k_r}} \quad \text{for} \quad 1.115 \leq k_r \leq 1.387 \tag{25c}$$
HB-SMs and FB-SMs / HB-SMs / FB-SMs

$$V_u = (k_r-1)V_{dco} \quad \text{for} \quad 1.387 \leq k_r \leq 1.667 \tag{25d}$$
HB-SMs / HB-SMs / FB-SMs

$$V_u = V_{dco}\sqrt{\frac{2k_r-2}{3}} \quad \text{for} \quad 1.667 \leq k_r \leq 2.5 \tag{25e}$$
HB-SMs / HB-SMs / FB-SMs

$$V_u = V_{dco} \quad \text{for} \quad 2.5 \leq k_r \leq 3.581 \tag{25f}$$
HB-SMs / HB-SMs / FB-SMs

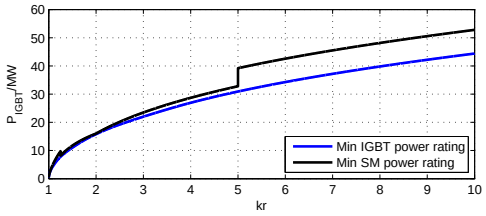


Fig. 12: IGBT power rating as a function of k_r.

$$V_u = V_{dco}\sqrt{\frac{4k_r-2k_r^2-2}{1-4k_r}} \quad \text{for} \quad 3.581 \leq k_r \leq 9.690 \tag{25g}$$
HB-SMs / HB-SMs and FB-SMs / FB-SMs

$$V_u = 2V_{dco} \quad \text{for} \quad 9.690 \leq k_r \leq 22.620 \tag{25h}$$
HB-SMs / HB-SMs and FB-SMs / FB-SMs

$$V_u = V_{dco}\sqrt{\frac{2-2k_r^2}{1-4k_r}} \quad \text{for} \quad k_r \geq 22.620 \tag{25i}$$
HB-SMs / FB-SMs / FB-SMs

Fig. 10 shows the optimal values of V_u obtained for the minimum SM power rating and for the minimum IGBT power rating. The IGBT power rating optimization takes into account the type of SM, thus, the number of IGBTs. As can be seen, the optimal V_u for minimum IGBT power rating is smaller than that for minimum SM power rating. In this way, fewer FB-SMs are required. For instance, for $k_r = 3$, the optimal values obtained for the minimum SM power rating are $V_{dcm} = V_{dco}$ and $V_u = 1.41V_{dco}$. Hence, given that $V_u > V_{dcm}$, the derivation branch requires FB-SMs. On the other hand, the optimal values obtained for the minimum IGBT power rating are $V_{dcm} = V_{dco}$ and $V_u = V_{dco}$. In this case, only HB-SMs are required in the derivation branch, so a fewer number of semiconductor power devices are required. However, as shown in Fig. 8, which plots the feasible nominal power of a 300 kV converter using 1.0 kA SMs, minimization of installed IGBT power leads to a smaller converter nominal power than minimization of installed SM power rating.

Fig. 11 shows the number of SMs required per MW of transmitted dc power for a 300 kV converter based on 2.5 kV, 1.0 kA SMs. As discussed on the previous paragraph, a converter designed on the basis of minimal SM power rating tends to use more FB-SMs than the one designed on the basis of minimal IGBT power rating. Nevertheless, the total number of SMs of both design approaches is very similar.

Fig. 12 shows the IGBT power rating in per unit of the output dc power ($V_{dco}I_{dco} = 1\ pu$) as a function of k_r using the values of V_u obtained from both optimizations. The installed IGBT power is similar regardless of the optimal value of V_u, specially for low and medium voltages ratios. As shown in Fig. 9, for $k_r > 2$, the DeB requires increasing the number of FB-SMs and becomes a hybrid branch. In contrast, if the optimal V_u for the minimum IGBT power rating were used, for example, between $2.5 < k_r < 3.581$, V_u is limited to $V_u = V_{dco}$. This avoids the use of FB-SMs since they increase the installed power in terms of IGBTs. The sharp increase in IGBT per MW in $kr = 5$ for the case of minimum SM power rating is due to the constraint of balance of capacitor voltages in hybrid branches (23). For $kr > 5$, only FB-SMs are used in the DeB.

TABLE I: Inner ac voltage for different dc-dc topologies.

Topology	$k_r = 1.25$		$k_r = 2$		$k_r = 5$	
	V_u	I_{ise}	V_u	I_{ise}	V_u	I_{ise}
[12]	0.2	0.333	0.5	0.333	0.2	0.083
[3]	0.5	0.667	0.5	0.667	0.5	0.667
T-converter	0.4	0.5	0.5	0.333	0.4	0.125

TABLE II: Device losses

Topology	$k_r = 1.25$	$k_r = 2$	$k_r = 5$
[12]	1.04%	0.99%	3.30%
[3]	1.82%	1.82%	1.82%
T-converter	0.92%	1.50%	3.72%

In general, results in Fig. 8, Fig. 11 and Fig. 12 show that, for low to medium voltage ratios, the total number of SMs, the maximum transmitted power and the IGBT power rating do not change significantly with the design approach (minimum SM power rating or minimum IGBT power rating). To some extent this is justified by the fact both optimization approaches yields the same inner dc voltage ($V_{dcm} = V_{dco}$) and that, as shown in Fig. 5, around optimal V_u, power rating does not vary significantly with V_u.

E. Losses

The studied T-converter is compared with the topologies proposed in [3] and [12] in terms of losses of the semiconductor power devices. The SMs are rated at 2.5 kV and 1 kA, hence, an IGBT of 4.5 kV and 1.2 kA is used (Infineon IGBT device FZ1200R45KL3_B5). The frequency of the circulating current is 100 Hz and a voltage margin factor (k_s) of 1.2 considered to account for SMs voltage reduction due to ripple in the capacitor voltages required to adequately force the branch current. The average switching frequency of the IGBTs is 500 Hz and 250 Hz for the HB-SMs and FB-SMs, respectively.

For a nominal branch current of 1 kA, the input dc current and the value of the voltage V_u in per unit of the input voltage are shown in Table I for three voltage ratios. In all cases, an input voltage of 41.6 kV has been considered, which corresponds to the nominal voltage of the front-to-front topology with 20 SMs per branch with $k_s = 1.2$. Table II shows the losses of the three topologies. Note that only the losses of the semiconductor power devices are considered. However, the topology in [3] uses a transformer and the topology in [12] uses a coupled inductor, which introduce additional losses.

VI. Fault Blocking Capability Analysis

The converter capability to block dc faults, either at its input side or output side, depends on the counter voltage it can insert into the fault current path once the converter is blocked [19]. Fig. 13 shows the equivalent circuit of the converter, assuming all power devices are blocked, for a dc fault at the input and output sides of the converter, respectively. In Fig. 13, the capacitors in green apply to case of FB-SMs. For HB-SMs no such capacitor exists and therefore the corresponding voltage is zero. Besides, for HB-SMs, depending on the direction of the fault current, the SM capacitor is bypassed by the antiparallel diode and, hence, the SM voltage is zero.

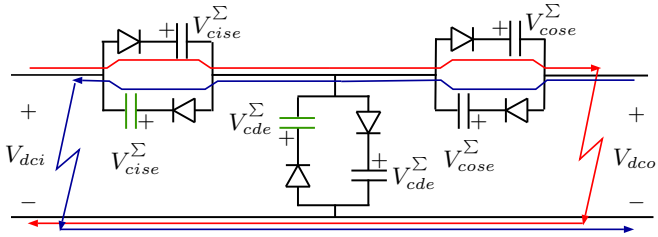


Fig. 13: Converter equivalent circuit in the event of a dc fault at the input and output sides.

After blocking the converter, the voltage inserted by each branch is the sum of all SM capacitor voltages in that branch and this is proportional to the maximum branch voltage during normal operation, i.e. the voltage rating of the branch, as given in (26).

$$V_{cise}^{\Sigma} = N_{ise}V_{cise} = k_s\left(V_{dci} - \left(V_{dco} - V_{dco}\sqrt{k_r - 1}\right)\right) \quad (26a)$$

$$V_{cde}^{\Sigma} = N_{de}V_{cde} = k_s\left(V_{dco} + V_{dco}\sqrt{k_r - 1}\right) \quad (26b)$$

$$V_{cose}^{\Sigma} = N_{ose}V_{cose} = k_s V_{dco}\sqrt{k_r - 1} \quad (26c)$$

For dc faults at the output side, the converter response does not depend on the SM type used in the ISeB and DeB (see the current path depicted in red in Fig. 13). Considering that the output voltage drops to zero, the converter will be able to block the fault current if:

$$V_{cise}^{\Sigma} + V_{cose}^{\Sigma} > V_{dci} \quad (27)$$

Substituting (26) in (27):

$$2k_s\sqrt{k_r - 1} > k_r - k_s(k_r - 1) \quad (28)$$

For a value of $k_s = 1.2$, the converter is able to block the fault current if $k_r > 1.16$.

Unlike the case of short-circuit at the output side, the converter response to a short-circuit at the input side depends on the SM type used in the ISeB. As shown in Section V-C, for $k_r > 2$ the ISeB does not use FB-SMs, therefore, only the OSeB can insert a voltage which opposes to the fault. Considering that the input voltage drops to zero, the converter will be able to block the fault current if:

$$V_{ose}^{\Sigma} > V_{dco} \quad (29)$$

Substituting (26) into (29):

$$k_s\sqrt{k_r - 1} > 1 \quad (30)$$

Given that the previous condition is always met, the converter can always block the fault currents when $k_r > 2$.

For lower voltage ratios ($k_r < 2$) the ISeB requires FB-SMs, therefore, it can also contribute to block the fault. Considering that the input voltage drops to zero, the converter will be able to block the fault current if:

$$N_{FB_{ise}}(\%) \cdot V_{cise}^{\Sigma} + V_{cose}^{\Sigma} > V_{dco} \quad (31)$$

Substituting (22a) and (26) in (31):

$$\frac{\sqrt{k_r - 1} - k_r + 1}{k_r - 1 + \sqrt{k_r - 1}} k_s\left(k_r - 1 + \sqrt{k_r - 1}\right) + k_s\sqrt{k_r - 1} > 1 \quad (32)$$

For a value of $k_s = 1.2$, considering the ISeB uses the percentage of FB-SMs given in (22a) (minimum number of FB-SMs as percentage of the total number of SMs), the

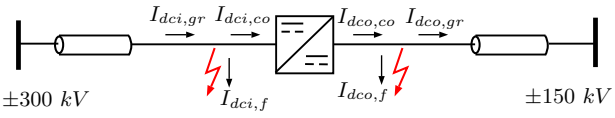
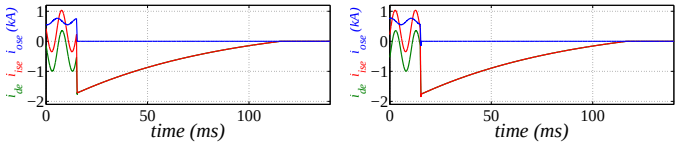


Fig. 14: Schematic of the bipolar HVdc grid.

TABLE III: System parameters.

V_{dci}	± 300 kV	V_{dco}	± 150 kV	P	400 MW
N_{ise}	150 (HB)	N_{de}	150 (HB)	N_{ose}	75 (FB)
V_c	2.5 kV	C_{SM}	3000 μF	L	35.8 mH
V_u	150 kV	V_{dcm}	150 kV	f_u	100 Hz
k_T	2	I_{max}	1 kA		



(a) Upper half of T-section 1. (b) Upper half of T-section 2.

Fig. 15: Converter branch currents during a dc fault at the input positive pole.

converter can block fault currents when $k_r > 1.35$. This value can be extended to $k_r > 1.125$ if all the SMs of the ISeB, instead of the fraction in (22a), are FB-SMs. Note that this exchange of HB-SMs to FB-SMs is only needed for $1.25 < k_r < 1.35$.

From the previous analysis it is concluded that if both the ISeB and the OSeB only use FB-SMs, the converter will be able to block faults at the output side when $k_r > 1.16$ and at the input side when $k_r > 1.125$. However, the converter can isolate dc faults for any voltage ratio by slightly increasing the number of FB-SMs in these two branches.

Other non-isolated topologies need to replace HB-SMs by FB-SMs and/or add additional FB-SMs to block dc faults, regardless of the voltage ratio [12], [25]. Thus, those topologies require additional SMs that are not needed during the normal operation of the converter. On the contrary, the T-topology does not require any modification for voltages ratios $k_r > 1.35$. Moreover, it only requires some additional SMs for voltages ratios $k_r < 1.16$.

VII. Results

The system shown in Fig. 14 is used to study the behavior of the T-converter in the event of dc faults. The grid has a bipolar topology and the parameters of the converter are listed in Table III. The converter is simulated using a simplified model that accurately reproduces its behavior during dc faults [30].

A. DC fault at the input side

Initially the converter transmits rated power (400 MW) from the high voltage to the low voltage side. At $t = 15\ ms$ the positive pole voltage of the $\pm 300\ kV$ grid drops to zero due to a pole-to-ground fault. The SMs of the top half of the converter are blocked after detecting the fault, that is, when the branch currents exceed 1.5 pu plus 100 μs that takes into account communication and converter blocking delays. Altogether, as shown by results here, the converter is blocked around 625 μs after the fault onset. Hence, following the

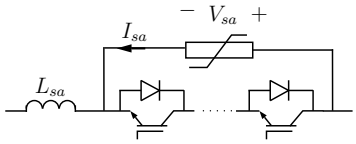
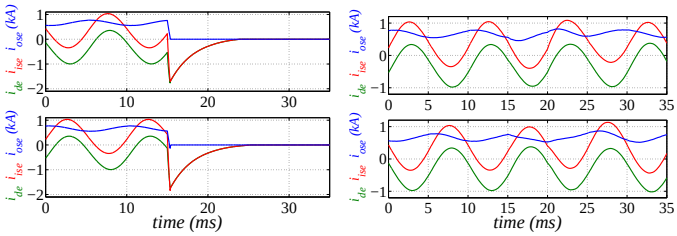


Fig. 16: Surge arrester.



(a) Upper half of the converter. Top: T-section 1, bottom: T-section 2.
(b) Lower half of the converter. Top: T-section 1, bottom: T-section 2.

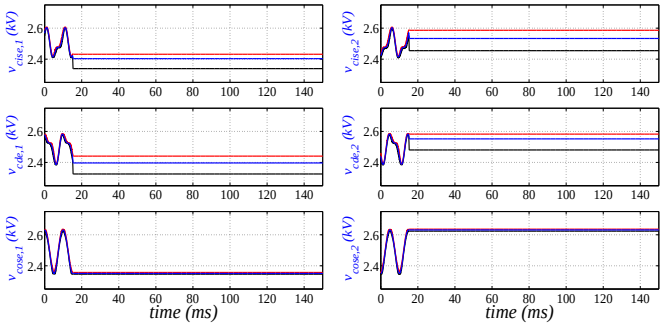
Fig. 17: Converter branch currents during a dc fault at the input positive pole. The surge arrester is used.

fault, the faulty converter pole takes 525 μs to hit the limit current, set to 1.5 pu. Fig. 15 shows the branch currents in both T-sections. After blocking the converter the current fed from the $\pm 150\ kV$ grid (i.e., the current that flows through the OSeB) immediately drops to zero due to the counter voltage inserted by the FB-SMs of the OSeB. On the other hand, the current through the ISeB and DeB flows through the antiparallel diodes but not through the capacitors. As a result the current decays much more slowly because the energy stored in the inductive components (branch inductors) is only dissipated in the resistive components of the system, i.e., the parasitic resistance of the branch inductors. The slightly differences between the current through both T-sections are because the ac currents are shifted 180º.

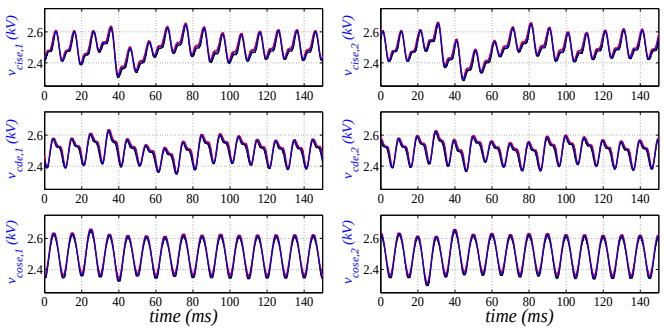
A surge arrester can be installed at the input side of the converter to dissipate energy, Fig. 16. In the event of a dc fault, the IGBTs are switched off and the current flows through the surge arrester where the energy is dissipated. Provided that the counter voltage between the input and output sides of the converter is inserted by the SM capacitors, the IGBTs of the surge arrester only have to withstand the voltage drop in the varistor while it is dissipating energy. Thus, a low number of semiconductor devices (around 5-10 devices depending on the value of the arrester) are needed in contrast to solid-state dc circuit breakers [31].

Fig.17a shows the branch currents through the top half of the converter when the arrester is connected after detecting the fault (with $L_{sa} = 0$ mH). Now the currents decay below 1 pu in about 2 ms and to zero in less than 8 ms. The bottom half keeps normal operation because the negative pole is not affected by the short-circuit as shown in Fig. 17b. However, now the current flows through the metallic return cable and the negative pole.

The SM capacitor voltages of each branch are shown in Fig. 18, where the SMs with the maximum and minimum voltage besides the average SM capacitor voltage are plotted in the graphs. Once the SMs of the top branches are blocked the capacitor voltages remain constant within safe values. On the other hand, the SM capacitor voltages of the bottom half remain well-controlled despite the transient that occurs when



(a) T-section 1 of the top half. (b) T-section 2 of the top half.



(c) T-section 1 of the bottom half. (d) T-section 2 of the bottom half.

Fig. 18: SM capacitor voltages during a dc fault at the positive input pole.

TABLE IV: Influence of the inductor L_{sa} on the fault current.

L_{sa} (mH)	t_{bl} (ms)	I_{pk} (pu)	E_{sa} (MJ)	V_{sa} (kV)	t_n (ms)	t_{cl} (ms)
0	0.350	1.80	0.108	21.06	1.93	7.8
50	0.980	1.69	0.199	16.39	3.62	34.35
100	1.44	1.60	0.238	13.79	10.51	53.72
150	1.93	1.56	0.296	12.98	14.54	72.26

the current starts flowing through the return cable. Fig. 19 shows the voltage drop, the current and the dissipated energy in the surge arrester.

The previous results have been obtained without considering the surge arrester inductor ($L_{sa} = 0$ mH, see Fig. 16). Table IV presents the results for different values of L_{sa}, where t_{bl} is the time when the converter is blocked and the surge arrester is connected, I_{pk} is the peak fault current, E_{sa} is the energy dissipated, V_{sa} is the surge arrester voltage, t_n and t_{cl} are the time when the current drops below 1 pu and to zero, respectively. A high value of L_{sa} limits the increase rate of the fault current, thus, it reduces the peak fault current without needing to detect the fault and to block the converter so fast. Moreover, the voltage in the surge arrester also decreases, hence, a lower number of IGBTs are required. However, the stored energy and the fault clearing time increase. A higher value of the resistance of the surge arrester reduces the clearing time at expense of higher V_{sa}. Provided that the branch inductors already limit the fault currents, high values of the inductance L_{sa} do not improve the fault clearing response.

B. DC fault at the output side

The converter response to dc faults at the output side is shown in Fig. 20. As previously, the converter transmits rated power from the high voltage to the low voltage side and at

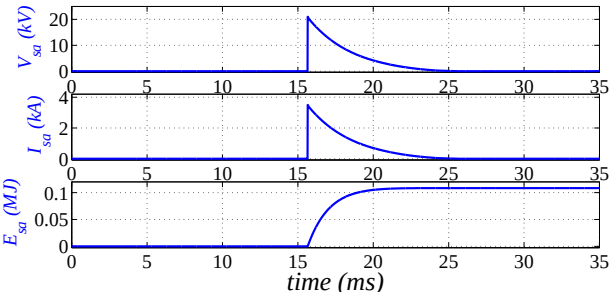
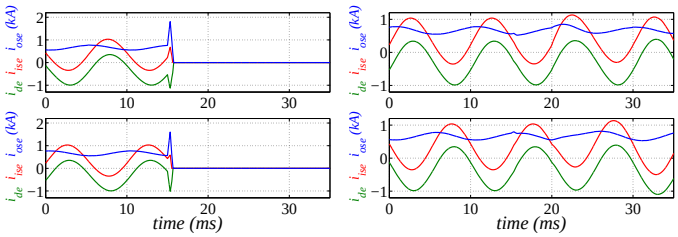
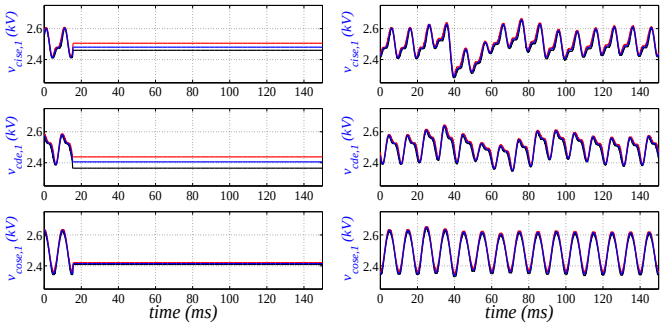


Fig. 19: Voltage, current and dissipated energy in the arrester.



(a) Upper half of the converter. Top: T-section 1, bottom: T-section 2. (b) Lower half of the converter. Top: T-section 1, bottom: T-section 2.

Fig. 20: Converter branch currents during a dc fault at the output positive pole. The surge arrester is not used.



(a) T-section 1 of the top half. (b) T-section 1 of the bottom half.

Fig. 21: SM capacitor voltages during a dc fault at the positive output pole. The surge arrester is not used.

$t = 15\ ms$ the positive pole voltage of the $\pm 150\ kV$ grid drops to zero due to a pole-to-ground fault. Immediately, the SMs of the top half of the converter are blocked. In this case both the ISeB and the OSeB insert a counter voltage so the current quickly drops to zero in both branches even without using the surge arrester, Fig. 20a. The SM capacitor voltages remain under safe values, Fig 21a. Now, instead of dissipating the energy in the surge arrester, it is stored in the SM capacitors:

$$\Delta E_{ise} \approx 0.044MJ, \quad \Delta E_{de} \approx 0MJ, \quad \Delta E_{ose} \approx 0.069MJ \quad (33)$$

where $\Delta E \approx 0.5C(\bar{V}_{c1}^2 - \bar{V}_{c0}^2)$, being $\bar{V}_{c0}$ the average SM capacitor voltage at the instant the converter is blocked and $\bar{V}_{c1}$ the final average capacitor voltage. These values are in line with the energy dissipated in the surge arrester in the previous case. Again, the lower part keeps transmitting power between both dc grids, Figs. 20b and 21b.

VIII. Discussion

A. DC-DC MMC Sizing

Transformerless dc-dc converters require inner ac branch voltages and ac circulating currents to transfer energy among

branches. This helps in maintaining the balance between the energy delivered and that recovered by each branch over a given time interval. In the T-topology, the value of the branch ac voltage (V_u) and the inner dc voltage (V_{dcm}) can be freely chosen to optimize converter design and operation. The analysis in section V shows that the amplitude of V_u and V_{dcm} has a significant impact on the number of SMs and power semiconductor devices required to transfer a given dc power.

The power transferred between branches is given by $P = V_u I_{iu}/2$. The higher the ac branch voltage, the lower the circulating current needed to maintain branch energy balance. Thus, for SMs of a given current rating, there is more room for the dc current and more dc power can be transmitted. However, higher ac voltages require a larger number of SMs.

Additionally, the voltage difference between the input and the output sides can be shared between the IseB and OseB. However, the OSeB requires an ac circulating current that is k_r times bigger than that of the ISeB. Thus, selection of suitable values of V_u and V_{dcm} is not obvious. Optimization analysis shows that $V_u = V_{dco}\sqrt{k_r - 1}$ and $V_{dcm} = V_{dco}$ minimizes the installed power in terms of SMs and power semiconductor devices, that is, these values maximizes the transmitted dc power per SM.

The optimal value of V_u that minimizes the power rating of the semiconductor power devices has also been obtained. In this case, for a given k_r, the optimal values of V_u are smaller than those which minimizes the SMs power rating. This is a way of minimizing the number of required FB SMs.

In general, the use of non-optimal values of V_{dcm} and V_u will lead to a converter with higher SM/IGBT power rating to transmit the same amount dc power.

The proposed sizing procedure can also be used to consider additional headroom for corner cases (i.e. transients and fault conditions) which can be translated to slightly increased voltage and current requirements.

B. DC-DC MMC Fault Blocking Capability

The T dc-dc converter can block dc faults over a wide range of voltage ratio without resorting to additional SMs. A converter design which minimizes the installed capacity in terms of SMs, for example, is able to block fault at the input side when $k_r > 1.25$ and at the output side if $k_r > 1.16$.

In general, the use of some additional FB-SMs contributes to block faults and allows the increase of the value of V_u, which, in turn, reduces the circulating current. Increasing the value of V_u has only a small effect on the power capability of the converter. In contrast, the use of a suboptimal value of V_{dcm} is not advisable because it significantly reduces the power capability of the converter. Therefore, the use of some additional FB-SMs is a good choice to extend the fault blocking capability of the converter, if they are also used to increase the value of V_u. In the optimized converter, extending the fault blocking capability to voltages ratios close to 1 requires only a few additional FB-SMs in the ISeB and/or OSeB (respect to those for normal operation).

Upon fault detection, the IGBTs of the SMs are blocked and arm currents rapidly decay to zero. Exception is made to faults at the input side for $k_r > 2$. The ISeB of the optimized converter, in this case, uses only HB-SMs. Therefore, the ISeB is unable to insert a counter voltage when the current flows from the converter midpoint towards the input side (the ISeB current flows through the antiparallel diodes). As a consequence, because of the energy trapped in the inductive components, the ISeB current decays slowly to zero. To accelerate the current decay, a surge arrester in the ISeB can be used to help in dissipating the trapped energy.

IX. Conclusions

This paper has studied two important aspects for the utilization of transformerless dc-dc converters in high voltage high power applications, namely optimal sizing and fault blocking capability. These aspects have an important impact on both the capital and operational cost of the converter.

In optimizing the converter design, the values of the inner dc voltage (V_{dcm}) and the branch ac voltages (V_u) that minimize either the installed converter capacity or the semiconductor area have been derived. It is found that minimization of the semiconductor area requires a slightly smaller ac voltage than that which minimizes the installed converter capacity. Nevertheless, both optimization criteria result in a high efficiency dc-dc converter, particularly for small voltage conversion ratios (k_r).

The fault blocking capability of the T-topology dc-dc converter using the optimal design has also been analyzed. In contrast to alternative topologies, like the HVdc-AT that requires additional HB-SMs and FB-SMs when compared to those required for the normal operation, the T dc-dc converter can block dc faults over a wide range of voltage ratio without resorting to additional SMs.

Therefore, the T-topology, designed according to a criterion which minimizes the installed capacity in power converters, or alternatively the silicon area, may be a good alternative for high voltage high power dc-dc converters that require a small voltage conversion ratio, while providing dc fault blocking capability at no or little additional cost.

Appendix

The required power in terms of IGBTs is:

$$P_{r2} = I \cdot 2 \cdot N_{eq} \cdot V_c \tag{34}$$

where $N_{eq} = (N_{HB} + 2N_{FB})$, being N_{HB} and N_{FB} the number of HB-SMs and FB-SMs, respectively, used in the converter. I is the peak value of the branch current.

The number of SMs in each branch is:

$$N_{ise} = \frac{|V_{dci} - V_{dcm}| + V_u}{V_c} \tag{35a}$$

$$N_{de} = \frac{V_{dcm} + V_u}{V_c} \tag{35b}$$

$$N_{ise} = \frac{|V_{dcm} - V_{dco}| + V_u}{V_c} \tag{35c}$$

As discussed in Section V-C, FB-SMs are needed to create a negative branch voltage. Otherwise branch voltage can be created by HB-SMs alone. Branch voltages depends not only on the input and output DC voltages but also on the internal ac and dc voltages (V_u and V_{dcm}).

For the ISeB:

$$\text{if} \quad V_{dci} \geq V_{dcm} \quad \& \quad V_{dcm} + V_u \leq V_{dci} \rightarrow \text{HB-SMs} \tag{36a}$$

$$\text{if} \quad V_{dci} \geq V_{dcm} \quad \& \quad V_{dcm} + V_u \geq V_{dci} \rightarrow \text{FB-SMs} \tag{36b}$$

$$\text{if} \quad V_{dci} \leq V_{dcm} \quad \& \quad V_{dci} + V_u \leq V_{dcm} \rightarrow \text{HB-SMs} \tag{36c}$$

$$\text{if} \quad V_{dci} \leq V_{dcm} \quad \& \quad V_{dci} + V_u \geq V_{dcm} \rightarrow \text{FB-SMs} \tag{36d}$$

For the DeB:

$$\text{if} \quad V_{dcm} \geq V_u \rightarrow \text{HB-SMs} \tag{37a}$$

$$\text{if} \quad V_{dcm} \leq V_u \rightarrow \text{FB-SMs} \tag{37b}$$

For the OSeB:

$$\text{if} \quad V_{dcm} \geq V_{dco} \quad \& \quad V_{dco} + V_u \leq V_{dcm} \rightarrow \text{HB-SMs} \tag{38a}$$

$$\text{if} \quad V_{dcm} \geq V_{dco} \quad \& \quad V_{dco} + V_u \geq V_{dcm} \rightarrow \text{FB-SMs} \tag{38b}$$

$$\text{if} \quad V_{dcm} \leq V_{dco} \quad \& \quad V_{dcm} + V_u \leq V_{dco} \rightarrow \text{HB-SMs} \tag{38c}$$

$$\text{if} \quad V_{dcm} \leq V_{dco} \quad \& \quad V_{dcm} + V_u \geq V_{dco} \rightarrow \text{FB-SMs} \tag{38d}$$

In case of needing FB-SMs, a combination of HB-SMs and FB-SMs can be used. The proportion of each type of SM is:

For the ISeB:

If $(V_{dcm} > V_{dci}$ & $V_{dci} + V_u > V_{dcm}) || (2\,|(V_{dci} - V_{dcm})| < V_u)$

$$p_{ise_{FB}} = 1 \tag{39a}$$

If $V_{dci} > V_{dcm}$ & $V_{dcm} + V_u > V_{dci}$

$$p_{ise_{FB}} = \frac{V_{dcm} - V_{dci} + V_u}{V_{dci} - V_{dcm} + V_u} \tag{39b}$$

$$p_{ise_{HB}} = 1 - p_{ise_{FB}} \tag{40}$$

where $p_{ise_{HB}}$ and $p_{ise_{FB}}$ are, respectively, the ratio of the number of HB-SMs and FB-SMs to the total number of SMs in the branch. The proportion of FB-SMs can be obtained as the ratio of the peak negative branch voltage to the maximum branch voltage, either the positive or negative voltage. Moreover, the limitation given in (23) is also considered.

The equivalent number of SMs is:

$$N_{ise_{eq}} = N_{ise}(p_{ise_{HB}} + 2p_{ise_{FB}}) \tag{41}$$

For the OSeB:

If $(V_{dcm} < V_{dco}$ & $V_{dcm} + V_u > V_{dco}) || (2\,|(V_{dci} - V_{dcm})| < V_u)$

$$p_{ose_{FB}} = 1 \tag{42a}$$

If $V_{dcm} > V_{dco}$ & $V_{dco} + V_u > V_{dcm}$

$$p_{ose_{FB}} = \frac{V_{dco} - V_{dcm} + V_u}{V_{dcm} - V_{dco} + V_u} \tag{42b}$$

$$p_{ose_{HB}} = 1 - p_{ose_{FB}} \tag{43}$$

The equivalent number of SMs is:

$$N_{ose_{eq}} = N_{ose}(p_{ose_{HB}} + 2p_{ose_{FB}}) \tag{44}$$

For the DeB:

$$\text{If } 2V_{dcm} < V_u: \qquad p_{de_{FB}} = 1 \tag{45a}$$

$$\text{If } V_u > V_{dcm}: \qquad p_{de_{FB}} = \frac{V_u - V_{dcm}}{V_{dcm} + V_u} \tag{45b}$$

$$p_{de_{HB}} = 1 - p_{FB} \tag{46}$$

The equivalent number of SMs is:

$$N_{de_{eq}} = N_{de}(p_{de_{HB}} + 2p_{de_{FB}}) \tag{47}$$

The maximum values of the arm currents are:

$$i_{ise}^{max} = I_{ise} + I_{iu} = \frac{I_{dci}}{k_T} + 2\frac{V_{dci} - V_{dcm}}{V_u}\frac{V_{dco}}{V_{dci}}\frac{I_{dco}}{k_T} \tag{48a}$$

$$i_{ose}^{max} = I_{ose} + I_{ou} = \frac{I_{dco}}{k_T} + 2\frac{V_{dcm} - V_{dco}}{V_u}\frac{I_{dco}}{k_T} \tag{48b}$$

$$i_{de}^{max} = I_{de} + I_{iu} + I_{ou} = \left(\frac{V_{dco}}{V_{dci}} - 1\right)\frac{I_{dco}}{k_T} + \tag{48c}$$

$$+2\frac{V_{dci} - V_{dcm}}{V_u}\frac{V_{dco}}{V_{dci}}\frac{I_{dco}}{k_T} + 2\frac{V_{dcm} - V_{dco}}{V_u}\frac{I_{dco}}{k_T} \tag{48d}$$

Replacing the values of (41), (44), (47) and (48) in (34), the installed power in terms of IGBTs, in per unit of the output power ($V_{dco}I_{dco}$), is:

$$P_{r2} = 2V_c\frac{i_{ise}^{max} \cdot N_{ise_{eq}} + i_{de}^{max} \cdot N_{de_{eq}} + i_{ose}^{max} \cdot N_{ose_{eq}}}{V_{dco}I_{dco}} \tag{49}$$

The previous expression depends on V_u and V_{dcm}. The optimal values of V_{dcm} and V_u that minimize the installed IGBT power are those given in (24) and (25), respectively.

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Ricardo Vidal-Albalate received the M.Sc. degree in industrial engineering and the Ph.D in electrical engineering from the Universitat Jaume I (UJI), Castelló de la Plana, Spain, in 2010 and 2017, respectively. He was a visiting scholar for 6 months at the Dept. of Electrical and Electronic Engineering of the University of Nottingham, U.K., in 2014. He has been a Lecturer with UJI since 2013. His research interests include MMCs for HVDC grids and grid integration of wind power.

Diego Soto-Sanchez (M'95) received the B.Sc. degree in electrical engineering from the University of Magallanes, Punta Arenas, Chile, in 1989, and the Ph.D. degree in electrical engineering from Imperial College of London, London, U.K., in 1999. Since 1991, he has been a Lecturer with the University of Magallanes, where he is involved in teaching and research in Power Electronics and Drives. From 2010 to 2012, he was also a Research Associate with the Control and Power Group, Imperial College London. His research interests include large power converters for power system applications such as FACTS and HVDC.

Enrique Belenguer (M'05) received the M.Sc. and Ph.D. degrees in electrical engineering from the Technical University of Valencia (UPV), Valencia, Spain, in 1992 and 1997, respectively. He is currently a Professor of electrical engineering with the Universitat Jaume I, Castelló de la Plana, Spain. His research areas are power system analysis, electrical machines, power quality, and grid integration of renewable energy systems.

Ruben Pena (S'95–M'97-SM'16) was born in Coronel, Chile. He received the B.Sc degree in electrical engineering from the University of Concepción, Concepción, Chile, in 1984, and the M.Sc. and Ph.D. degrees from the University of Nottingham, Nottingham, U.K., in 1992 and 1996, respectively. From 1985 to 2008, he was a Lecturer in the Universidad de Magallanes, Chile. He has been with the Electrical Engineering Department, Universidad de Concepcion, since 2008, where he is currently a Full Professor. His main interests include control of power electronics converters, ac drives, and renewable energy systems. Dr. Pena received the Best Paper Award from the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS in 2004, and the Ramon Salas Edward Award for research excellence from the Chilean Institute of Engineers in 2009.

Ramon Blasco-Gimenez (S'94–M'96–SM'10) obtained his BEng degree in Electrical Engineering from Universitat Politècnica de València (Spain) in 1992 and his PhD degree in Electrical and Electronic Engineering from the University of Nottingham (UK) in 1996. From 1992 to 1995 he was a Research Assistant at the Dept. of Electrical and Electronic Engineering of the University of Nottingham. In 1996 he joined the Dept. of Systems Engineering and Control of Universitat Politècnica de València, where he is currently a Professor. His research interests include HVdc diode rectifiers, Control of HVdc systems, Wind Power Generation and Grid Integration of Renewable Energy Systems. Dr Blasco-Gimenez has been a co-recipient of the 2004 IEEE Transactions on Industrial Electronics Best Paper Award.