UNIVERSITAT POLITÈCNICA DE VALÈNCIA

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## Escuela Técnica Superior de Ingeniería Industrial

Current source inverter. Design and simulation

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# CURRENT SOURCE INVERTER DESIGN AND SIMULATION

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# Current Source Inverters

## INTRODUCTION

In the forthcoming document, we embark on an in-depth exploration of the design process for a Current Source Inverter (CSI) specifically tailored for a 100 kW low inductance Permanent Magnet Synchronous Motor (PMSM). The primary objective of this project is to devise a system that adeptly manages both the current and the speed of the motor, while minimizing the Total Harmonic Distortion (THD) present in the current signals supplied to the motor.

To achieve enhanced control and efficiency, the design will integrate cutting-edge switching technologies, such as Gallium Nitride (GaN) and Silicon Carbide (SiC), which facilitate higher switching frequencies. This advanced approach necessitates the inclusion of diodes within the circuit to inhibit the reverse flow of current, thus maintaining the directional integrity of the current flow.

Furthermore, a significant aspect of this study involves determining the optimal component values to ensure the desired operation of the CSI. The project will culminate in a comprehensive simulation of the CSI's functionality, which will provide insights into its performance and operational viability in real-world applications. This aims to contribute to the enhancement of PMSM motor systems by incorporating innovative technologies and refined design techniques.

### USE CASES:

Current Source Inverters (CSIs) play a pivotal role in the effective operation of low inductance motors, such as those addressed in this project. The challenge with operating low inductance motors using Voltage Source Inverters (VSIs) lies in the necessity for exceedingly high switching frequencies, along with advanced control methodologies or the implementation of three-phase inductances to attain satisfactory performance. In contrast, CSIs excel in providing the motor directly with three-phase currents in a sinusoidal form, even under conditions of very low inductance loads.

This capability is particularly advantageous for motors that utilize an air core or have eliminated the traditional metal core, thereby reducing weight and enhancing utility in various demanding applications. Such lightweight motors are not only pivotal in aerospace and space exploration due to their reduced mass and improved efficiency but also play crucial roles in high-speed racing, portable electronic devices, and robotic systems where compactness and weight reduction are critical.

Moreover, CSIs significantly mitigate current ripple, a feature that holds substantial interest in applications such as submarine operations or any setting where reducing noise levels is imperative. This reduction in noise pollution is essential in maintaining the stealth characteristics of submarines and improving the operational efficiency and reliability of sensitive acoustic equipment. This diverse range of applications underscores the versatility and critical importance of CSIs in modern technological advancements.

# CSI PARTS AND OVERALL WORKING PRINCIPLE

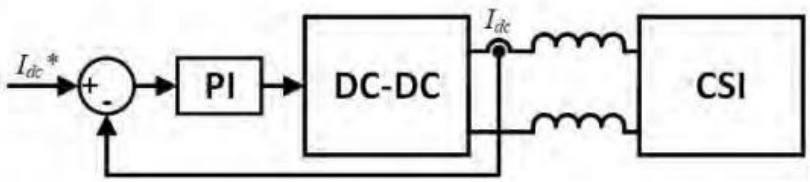



*Figure 1 Current Source Inverter basic topology*

The comprehensive power topology of the Current Source Inverter (CSI) is meticulously structured to facilitate efficient operation and control. The architecture begins with a pre-stage that functions as a virtual current source, providing the foundational current necessary for the subsequent stages. Central to the topology is the DC link inductance, which plays a crucial role in stabilizing the current throughout the switching process, thereby ensuring a consistent flow and reducing fluctuations that may degrade performance.

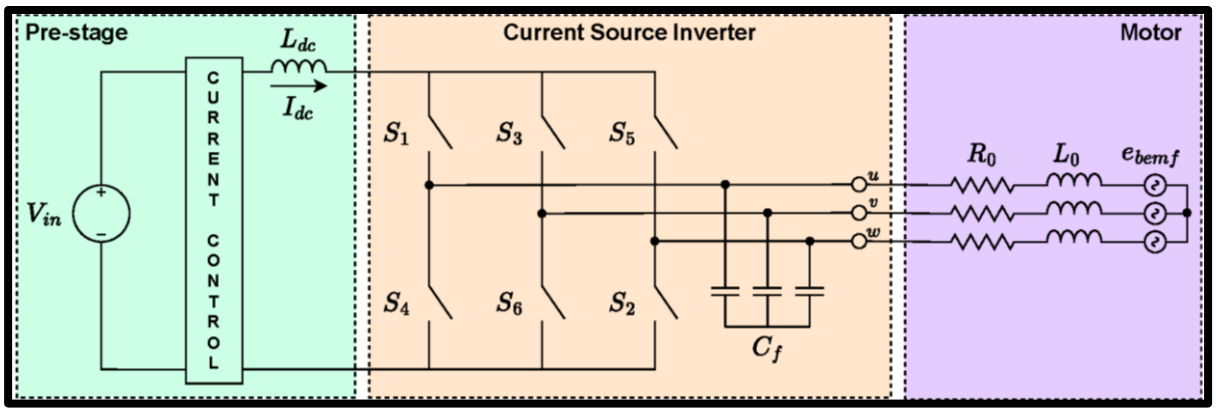



*Figure 2 Current source inverter topology with pre-stage (Fidone)*

Following this stabilization phase, the system incorporates a three-phase bridge. This bridge is instrumental in generating the Pulse Width Modulated (PWM) waves, which are essential for the accurate control of power delivery to the load. However, the currents produced at this stage are not yet suitable for direct application to the load, as they are not sinusoidal and contain high-frequency noise components.

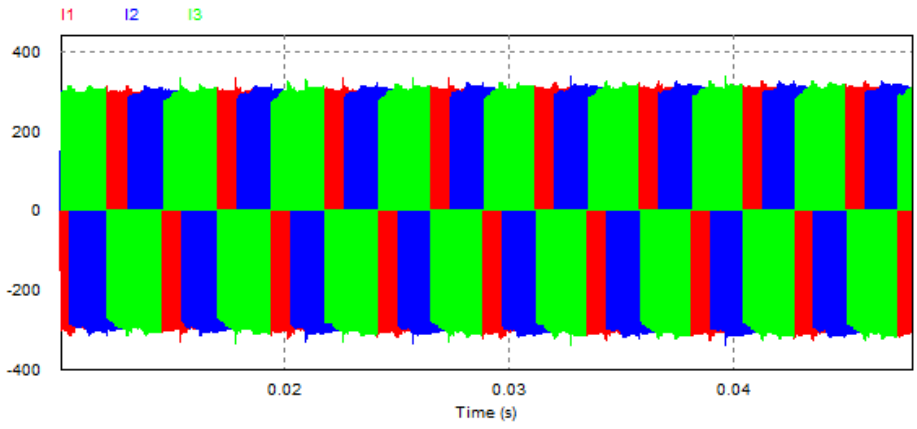



*Figure 3 Unfiltered current output*

To address this, the currents are passed through a three-phase capacitor filter. This filter effectively eliminates higher-order harmonic disturbances emanating from the switching process, thus refining the output to retain only the desired sinusoidal signal.

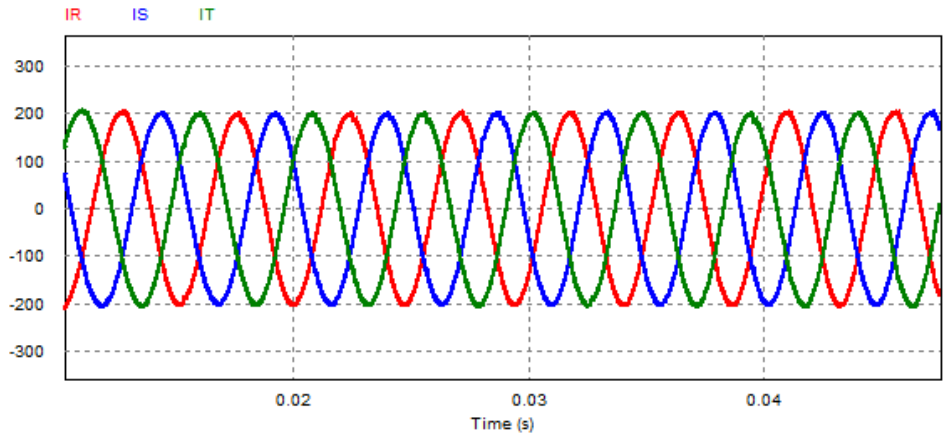



*Figure 4 Filtered current output to load*

In addition to the power stage, the CSI encompasses a sophisticated control stage, which is integral to managing the amplitude and frequency of the current supplied to the load. This control mechanism employs feedback from the rotor position and current to establish a dynamic feedback loop. Through this loop, the system continuously adjusts the current and speed settings to align with the operational demands and environmental conditions, thereby optimizing the motor's performance. This dual-stage configuration of power modulation and precise control underscores the advanced engineering and thoughtful design underlying the CSI's functionality.

# PWM Generation

To create the PWM signal needed we will make use of Space Vector PWM. Let's begin by explaining what Space Vector Pulse Width Modulation (SVPWM) is. This is a sophisticated technique employed in the control of AC motors, predominantly in the field of variable frequency drives. This technique, known for its proficiency in enhancing the performance of motors, operates by varying the current and frequency supplied to the motor.

At its core, SVPWM capitalizes on a mathematical model that represents the three-phase inverter as a single unit, rather than as three separate entities. This model visualizes the inverter's output current as a vector in a two-dimensional space. The primary objective of SVPWM is to control this vector's magnitude and direction, which, in turn, controls the motor.

The process of SVPWM involves the generation of three-phase current waveforms by modulating the duty cycles of inverter switches. These waveforms are not generated independently for each phase. Instead, the technique focuses on synthesizing a desired vector, which is achieved by appropriately activating the inverter switches.

The inverter's output current vector can be positioned at any point within a hexagonal space, formed by six active current vectors and two three vectors. These vectors correspond to the possible switching states of the inverter. The key to SVPWM's operation lies in its ability to calculate the duration for which each vector should be applied, ensuring that the average current over a switching period equals the desired current vector.

The process typically unfolds in two primary steps:

1. **Vector Decomposition:** The desired vector is mathematically decomposed into its nearest three neighboring vectors. Two of these vectors are active vectors, and the third is a zero vector.
2. **Time Calculation and Switching:** An algorithm calculates the time duration during which each of the three vectors should be applied. This ensures that the tip of the synthesized space vector effectively traces the trajectory of the desired voltage vector over time. The inverter's switches are then operated according to these calculated time durations.

In the cases of the Current Source Inverter we will not be focusing on extracting the highest voltage potential difference between the load. Instead, we will make use of the pre-stage to drive the needed phase current and will use the inverter to generate a rotating vector. By doing this we can minimize the switching patterns to avoid the unnecessary excess switching.

## VECTOR GENERATION ALGORITHM

In the synthesis of the desired voltage vector via Space Vector Pulse Width Modulation (SVPWM), the methodology pivots on formulating this vector as a linear combination of the three proximal vectors (Reney). This approach necessitates a strategic partitioning of the complex plane into distinct sectors. These sectors are demarcated by the array of nine potential vectors, which are derived from various configurations of the switching states in the inverter's bridge. Among these nine vectors, three are identified as zero states. In these states, the inverter effectively creates a short-circuit condition. This is achieved by concurrently activating both two of the upper and lower switches of the inverter's three phases, thereby closing the current path of the current supply.

The remaining six vectors delineate the periphery of a hexagon in the complex plane. This hexagonal formation is instrumental in the segmentation of the plane into six sectors. Each sector is defined by the angular span between two adjacent non-zero vectors and the origin. It is within this geometric construct that the desired voltage vector is synthesized.

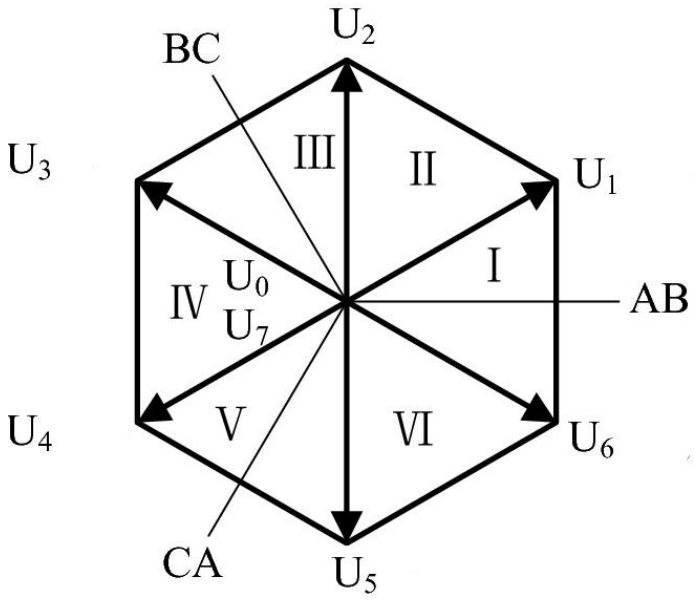



*Figure 5 iSVPWM hexagon with sectors (Li Delu)*

The operational essence of SVPWM lies in navigating this hexagonal space. By judiciously activating a combination of the inverter's switches, the system can effectively traverse this space, thereby generating a vector that closely approximates the desired trajectory. This process entails the calculation of the duration for which each adjacent vector, along with an appropriate zero vector, should be applied. Consequently, the synthesized vector, averaged over a switching cycle, aligns with the intended vector in both magnitude and phase.

To demonstrate further the working principle of this method we can begin with an example on the first sector of the hexagon.

## EXAMPLE OF CURRENT SPACE VECTORS

Let's say we want to create a vector, represented as the red vector in the lower image, where we represent the vector in a 2d space representing real and imaginary currents, that is positioned in between two of the hexagon vectors.

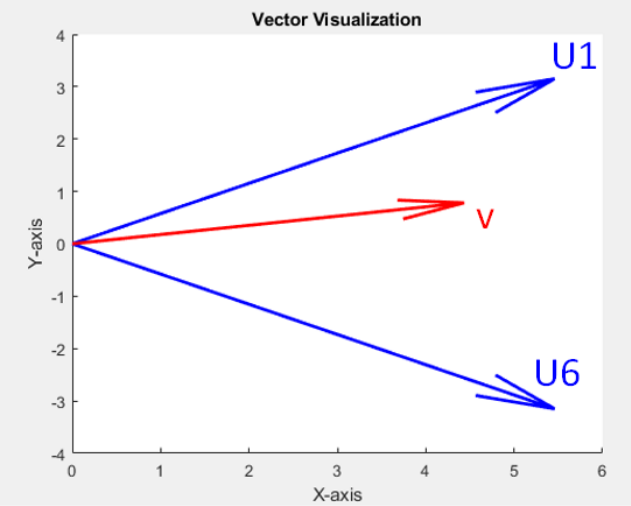



*Figure 6 Vector generation simulation*

To do so, we can find a linear combination of the adjacent vectors that will produce the desired vector. We know that mathematically we can represent that as:

$$I_{desired} = \alpha \cdot I_6 + \beta \cdot I_1 \quad (1)$$

Because we are working on a two-dimensional space, this single equation actually provides us with two different equations:

$$x_{I_{desired}} = \alpha \cdot x_{I_6} + \beta \cdot x_{I_1} \quad (2)$$

$$y_{I_{desired}} = \alpha \cdot y_{I_6} + \beta \cdot y_{I_1} \quad (3)$$

With these two equations we can calculate $\alpha$ and $\beta$ using the following equations:

$$\beta = \frac{x_{I_6} \cdot y_{I_{desired}} - x_{I_{desired}} \cdot y_{I_6}}{y_{I_1} \cdot x_{I_6} - x_{I_1} \cdot y_{I_6}} \quad (4)$$

$$\alpha = \frac{x_{I_{desired}} - \beta \cdot x_{I_1}}{x_{I_6}} \quad (5)$$

These alpha and beta represent the duty cycle of each of the base vectors that are closest to the one we want to generate. Because our vector is smaller in modulus than the combination of the two adjacent ones, and that is most generally the case during the rotating cycle, we need a

“zero” state. In our case to minimize switching in the converter the zero state that we will choose will require the least number of switches permutating state.

The corresponding duty cycle for this zero or null vector will be:

$$\gamma = 1 - \alpha - \beta \tag{6}$$

It is also worth mentioning that we are showing $x_{I_{desired}}$ and $y_{I_{desired}}$ in cartesian coordinates, but in reality the easiest way to visualize it is in its polar form. This way we can define it by it’s module and the absolute angle of the vector. Doing it this way allows us to filter in an easier way in which sector the vector is present.

Now we know how to create a vector that we want as a combination of the mentioned base vectors of each sector. But we don’t know yet what those vectors are. To understand what those vectors are we need to find what are our options for the switching of the inverter’s bridge.

## SWITCHING SCHEMES AND BASE VECTORS

Let’s begin by showing the different possible states that create a current flowing through the load. We will show the current controlled inverter with the following figure:

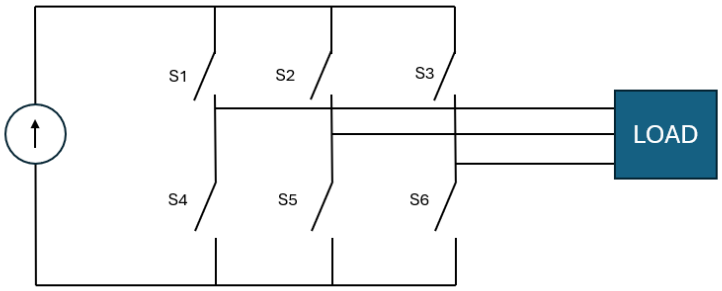



*Figure 7 Simplified CSI bridge scheme*

And we can represent the possible switching states like this:

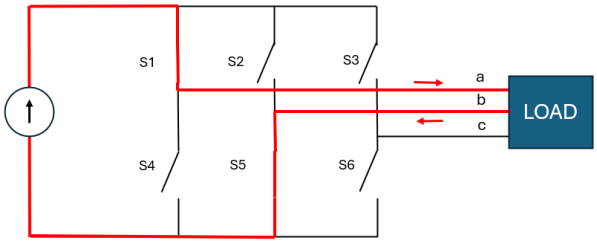



*Figure 8 State 1*

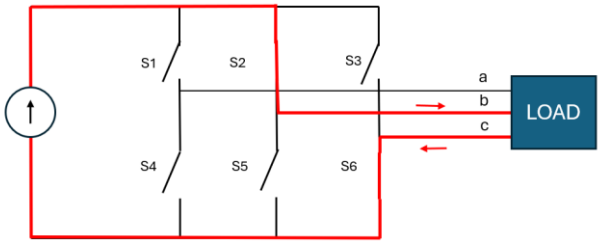



*Figure 9 State 2*

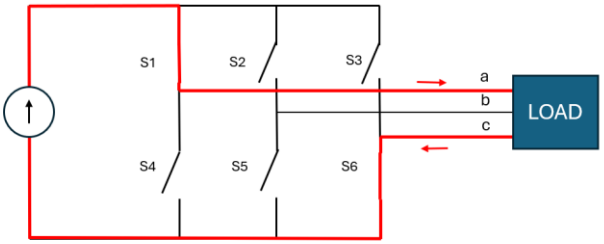



*Figure 10 State 3*

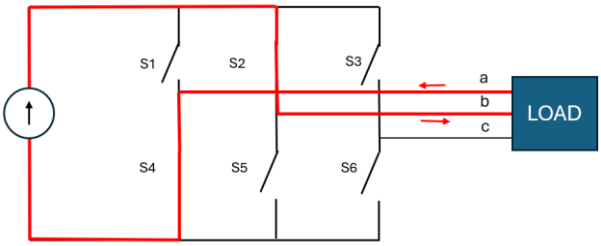



*Figure 11 State 4*

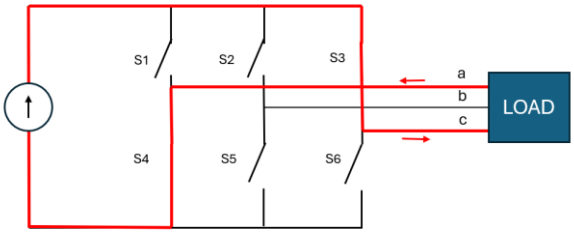



*Figure 12 State 5*

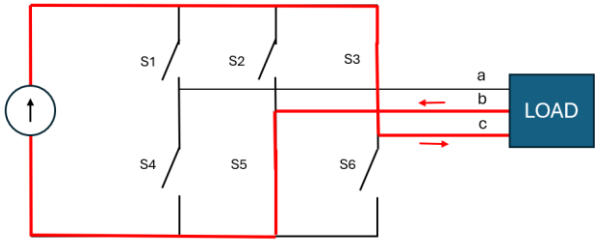



*Figure 13 State 6*

Those first were the active vectors that actually drive current through the load. Now let's show the 3 zero vectors that do not drive any current through the load:

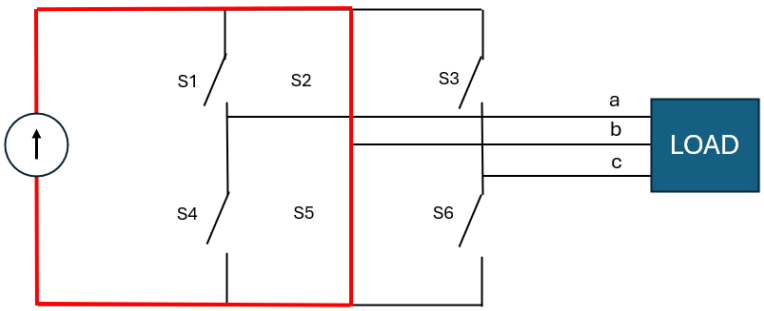



*Figure 14 Null state 1*

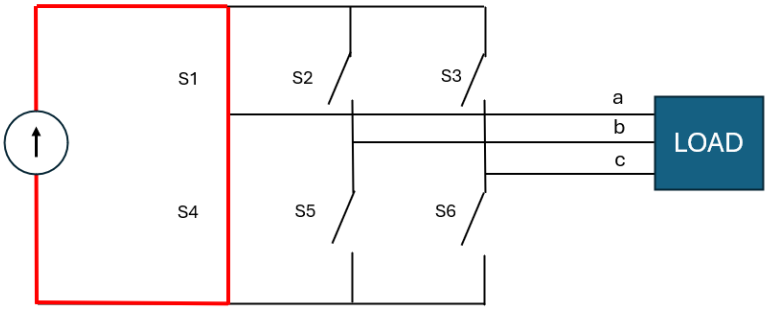



*Figure 15 Null state 2*

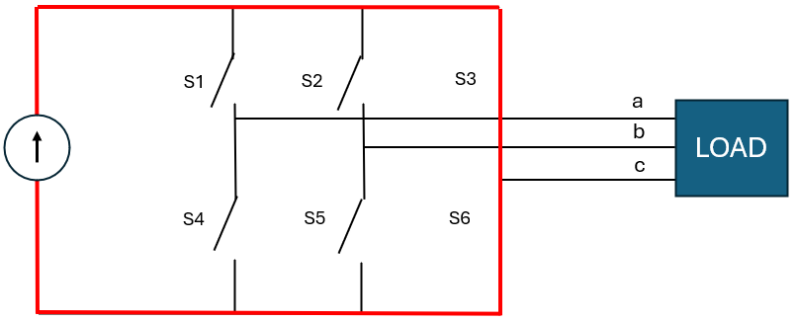



*Figure 16 Null state 3*

These combinations of vectors create the hexagon that we previously mentioned. Let's describe one of the vectors in the hexagon as a combination of the states as an example, as this is a simple task. Let's try to showcase this state:

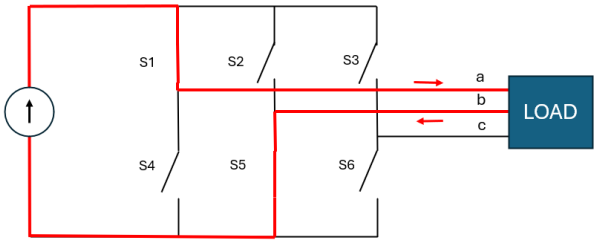



*Figure 17 State 4 situation*

In this switching state we have S1 and S5 closed, which creates a +Idc current in phase a of the load and a current -Idc in the phase b of the load. If we recall how the three phase currents are showcased, we can actually draw the vector that results from this combination:

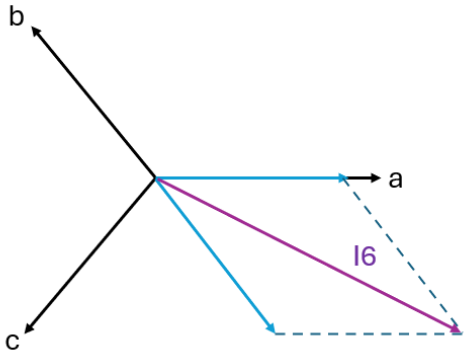



*Figure 18 U6 current vector*

If we continue doing the same for all the active vectors, we will end up with the hexagon that was previously described.

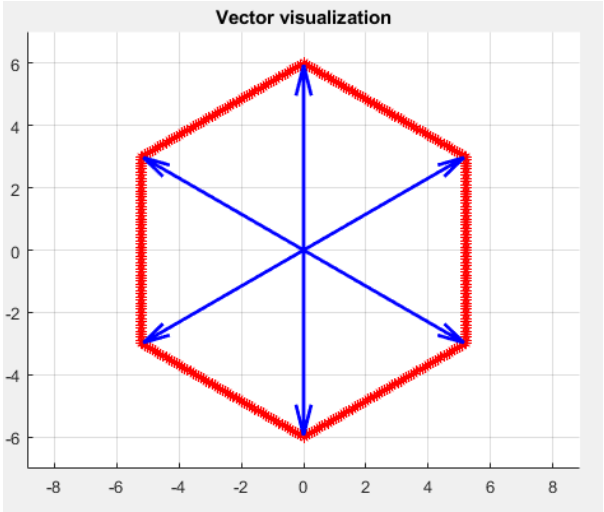



*Figure 19 Hexagon of maximum current*

We can now represent a vector in each sector as a linear combination of the base vectors of that sector. This allows us to more easily use what we know to recreate a wanted vector as a combination of the different switching states that create the currents through the load. We eventually want to create a rotating vector that will itself create a rotating magnetic field to drive a motor. We can visualize this in a picture if we imagine the vector rotating on the plane:

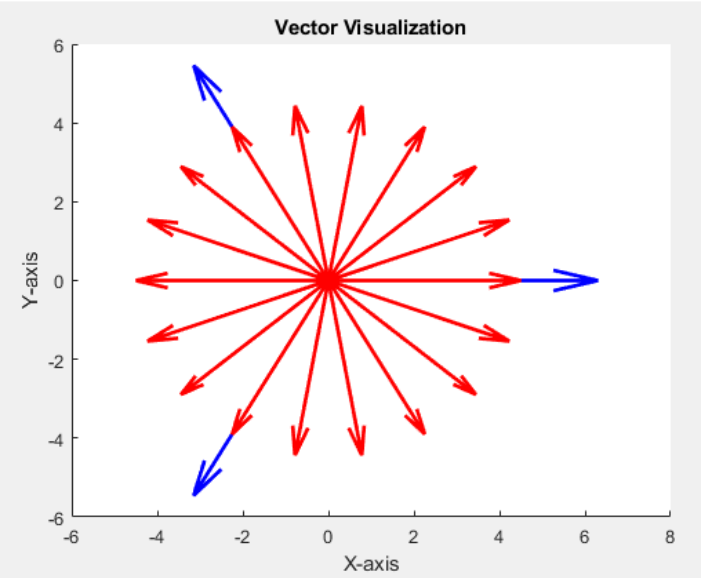



*Figure 20 Circular current generation*

With this rotating vector and the fact that we now know the sector we can use the combination of the switching patterns to define our desired vector. To do so we just have to remember to use the zero vector for each sector in which only one switch changes state. We can show the different switching states in the following table:

| SWITCHING TIMING TABLE | | |
|---|---|---|
| **SECTOR** | **SWITCH** | **DUTY CYCLE** |
| SECTOR 1 | S1 | 1 |
| | S2 | 0 |
| | S3 | 0 |
| | S4 | $1-\alpha-\beta$ |
| | S5 | $\alpha$ |
| | S6 | $\beta$ |
| SECTOR 2 | S1 | $\alpha$ |
| | S2 | $\beta$ |
| | S3 | $1-\alpha-\beta$ |
| | S4 | 0 |
| | S5 | 0 |
| | S6 | 1 |
| SECTOR 3 | S1 | 0 |
| | S2 | 1 |
| | S3 | 0 |
| | S4 | $\beta$ |
| | S5 | $1-\alpha-\beta$ |
| | S6 | $\alpha$ |
| SECTOR 4 | S1 | $1-\alpha-\beta$ |
| | S2 | $\alpha$ |
| | S3 | $\beta$ |
| | S4 | 1 |
| | S5 | 0 |
| | S6 | 0 |

| | | |
|---|---|---|
| SECTOR 5 | S1 | 0 |
| | S2 | 0 |
| | S3 | 1 |
| | S4 | $\alpha$ |
| | S5 | $\beta$ |
| | S6 | $1-\alpha-\beta$ |
| SECTOR 6 | S1 | $\beta$ |
| | S2 | $1-\alpha-\beta$ |
| | S3 | $\alpha$ |
| | S4 | 0 |
| | S5 | 1 |
| | S6 | 0 |

*Table 1 Switching timing.*

If we simulate the currents that would arraise from this sequence, which we can do because we know what currents flow for every combination of Sector positions, and we use the duty cycle to modulate the current Idc we obtain the following current for a rotating vector with the angle changing as it follows the complete circumference.

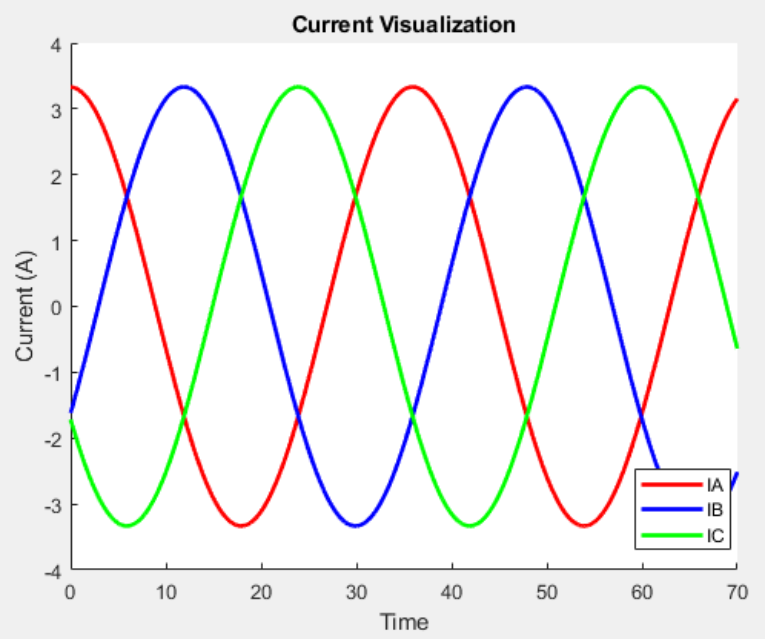



*Figure 21 3-Phase current simulation*

To this we can also incorporate the fact that $\alpha$ and $\beta$ cannot be higher than 1, and so the current is limited to a maximum value given by the current source. This can also be visualized if we try to increase the current demand above the highest possible value:

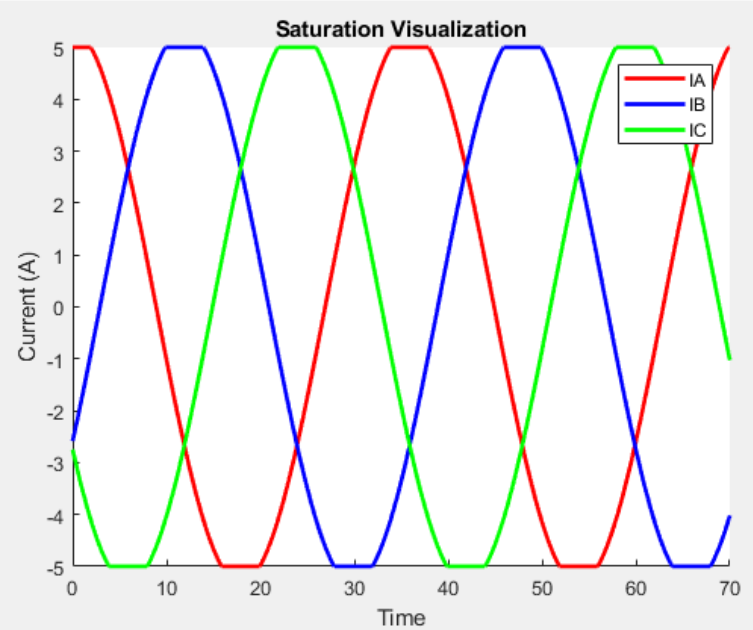



*Figure 22 3-Phase saturated current*

We can also visualize the switching patterns to, when it comes time to simulate the circuit verify proper operation.

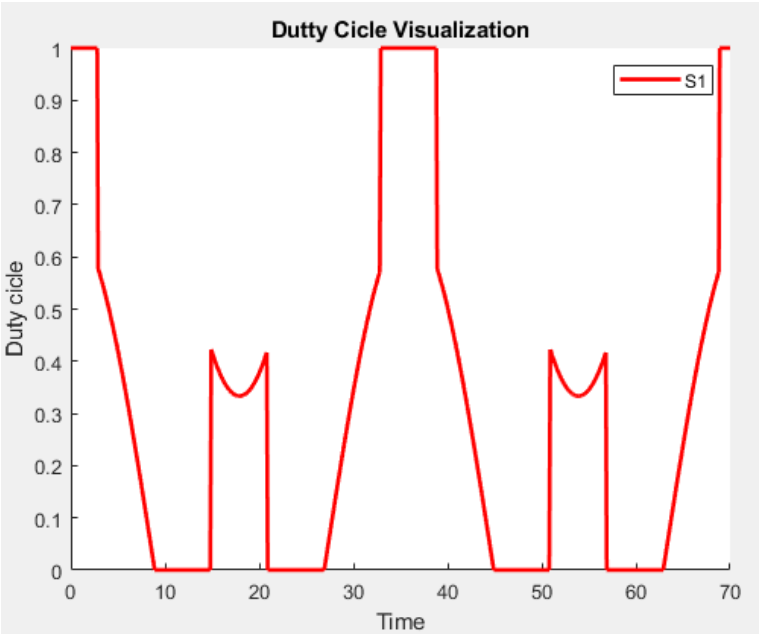



*Figure 23 Duty Cycle pattern for each switch*

From the previous image we can verify that there is symmetry in the switching patters, which is a good think that indicates that we are on the right path. We can now use some kind of simulation platform to test our code with a real CSI. Therefore, the next logical step is to design in the simulation software a simple version consisting of the major electrical elements, excluding the motor, that we will simulate as an inductive load by now.

# CIRCUIT DESIGN AND SIMULATION

## POWER STAGE

This section initiates with the circuit design process. Initially, the construction of a 3-phase bridge is required, which is essential for achieving the predefined switching states. This will involve the incorporation of both switches and reverse current protection diodes in each bridge to ensure robust and efficient operation.

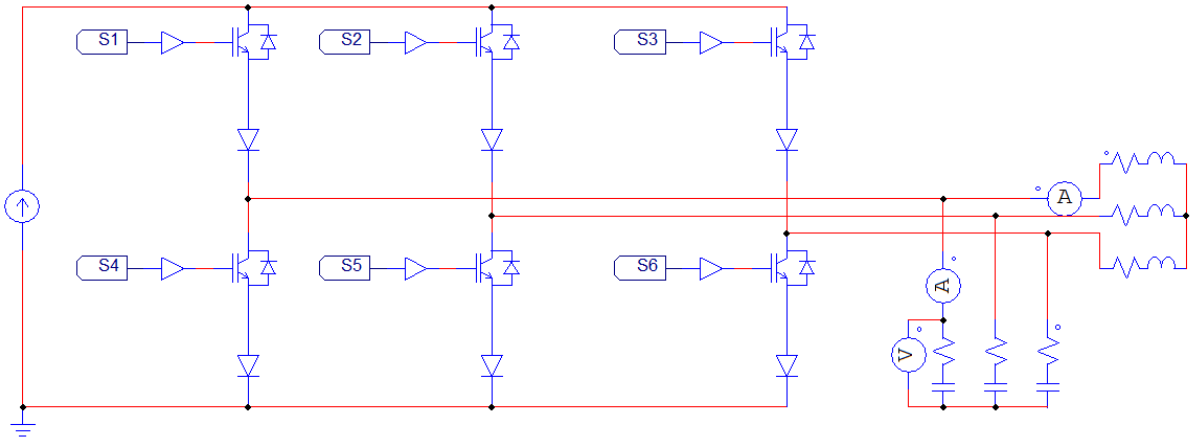



*Figure 24 Power stage*

In this image, we present the primary circuit configuration, wherein a current source is employed directly as the principal power supply, diverging from the actual pre-staging approach. This methodology is adopted to attenuate potential errors during the iterative phases of the design process. The load depicted here comprises a tri-phase arrangement of inductors and resistors, configured to emulate an inductive load scenario. Additionally, a tri-phase capacitor bank is integrated between each phase and the ground. This serves a dual purpose: it acts as a filter for the current traversing through the inductors, thereby refining the overall power quality and stability of the system, and also prevents the dc inductor from being tied on series.

## CONTROL STAGE

To regulate the previous circuit, we will employ the algorithm delineated in preceding sections, specifically Space Vector Pulse Width Modulation (SVPWM). The control block designated for this task will accept three principal inputs. The first input is the current setpoint, functioning analogously to a throttle for the Current Source Inverter (CSI), dictating the intensity of the current flow. The second input is the angle of the desired vector, representing a continuously rotating vector with a range from 0 to 360 degrees with a test frequency randomly selected as 60 Hz. This input is critical for determining the directional orientation of the current vector in the circuit. Lastly, the third input is the clock cycle, which governs the execution frequency of the control algorithm. This parameter is important to emulate the operational frequency of the actual controller, thereby contributing significantly to the stability and accuracy of the simulation.

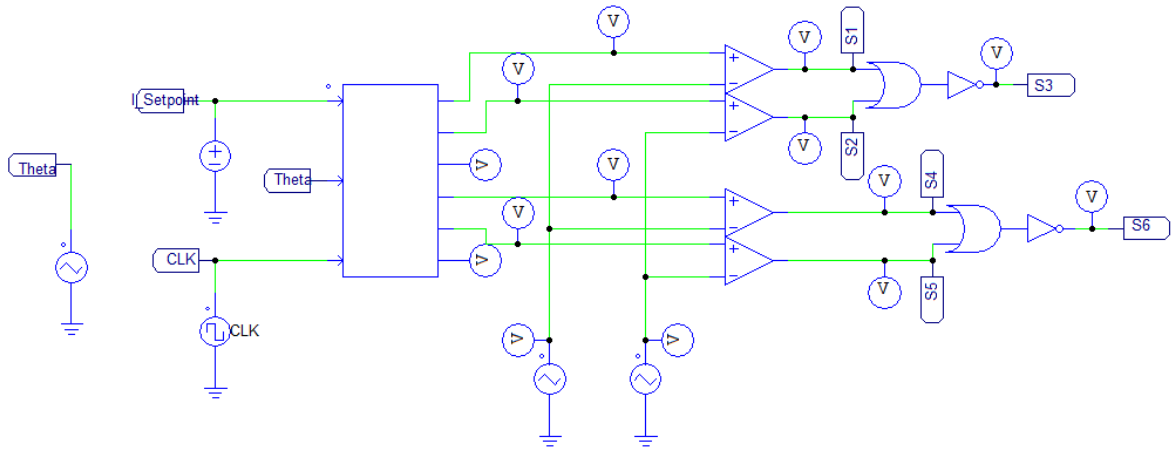



*Figure 25 Control stage*

The control block, as configured, will generate six duty cycle values essential for the modulation of the switches within the circuit. To effectively utilize these values for switch control, it is imperative to translate them into a Pulse Width Modulation (PWM) pattern.

To translate them into PWM we must be very careful on how it's done. The most important thing to keep in mind is the fact that because of the way a CSI works, there can never be an open circuit. This is so that the current source always has a path to inject current. To ensure that we need to assess one big problem. Common PWM generation techniques use one of this three modes to generate a PMW signal. First is "Left-Aligned" PWM, in this mode the PWM wave is generated starting from the left and growing as the duty cycle increases. "Right-Aligned" PWM therefore is the same but starting from the right. And finally, there's "Centre-Aligned" PWM, in which the PWM signal is aligned from the middle of the wave.

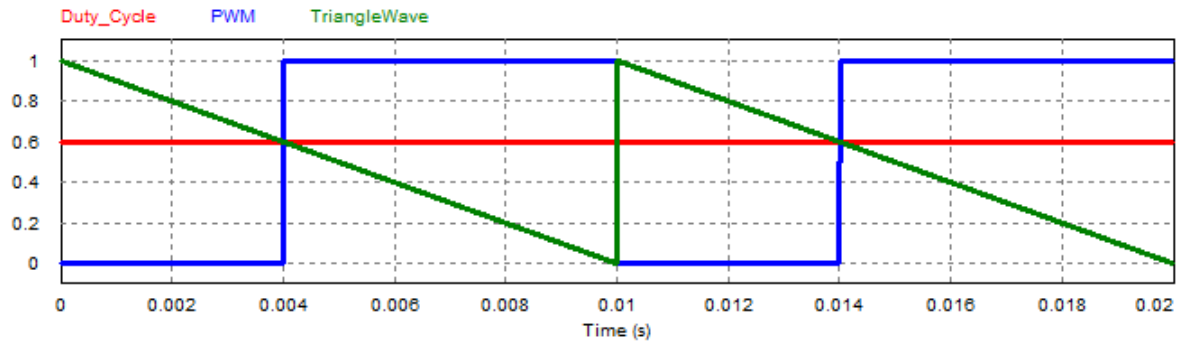



*Figure 26 Right aligned PWM*

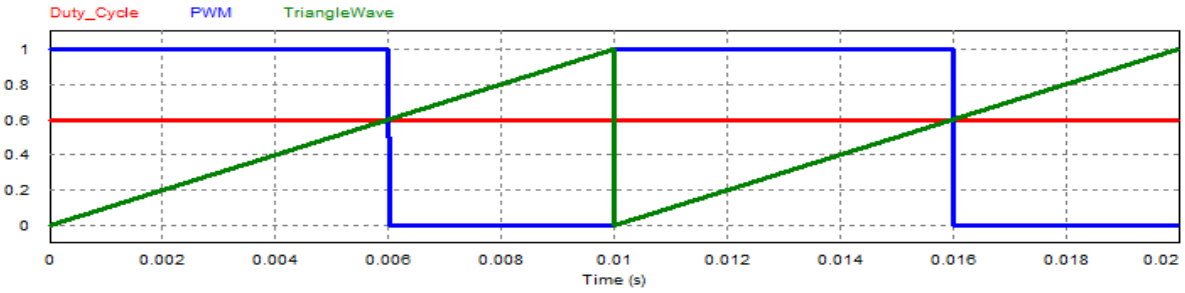



*Figure 27 Left aligned PWM*

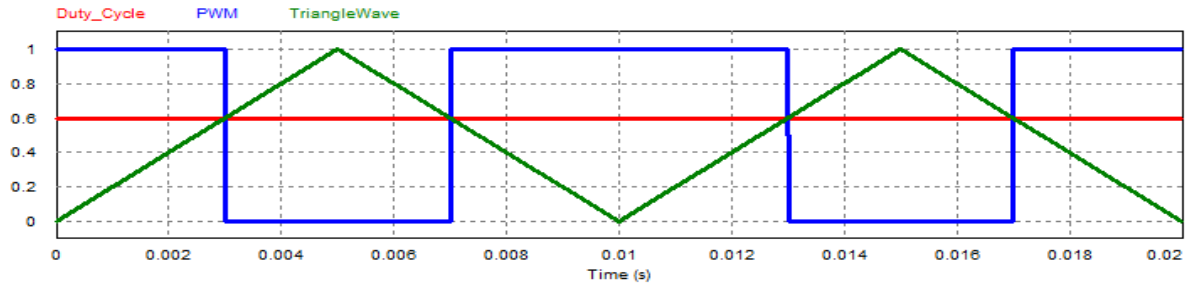



*Figure 28 Center aligned PWM*

To obtain this waveform we use a comparator that compares the duty cycle against a carrier wave, which will mark the frequency of the PWM.

The problem arises from the fact that there are some spaces of time within the period that none of the switches of one of the branches are closed, and therefore an open circuit situation happens:

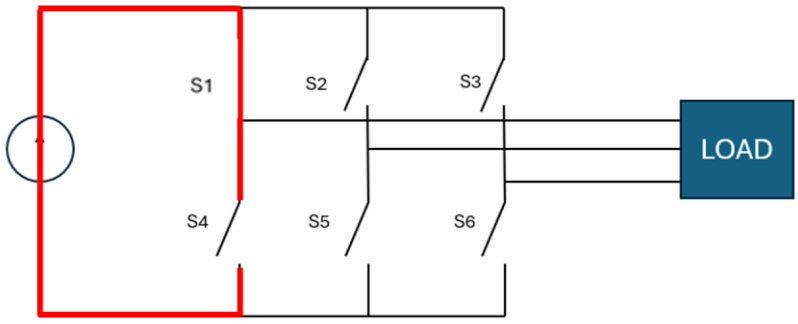



*Figure 29 Open circuit fault*

And that occurs because the PWM combined signals look like the following.

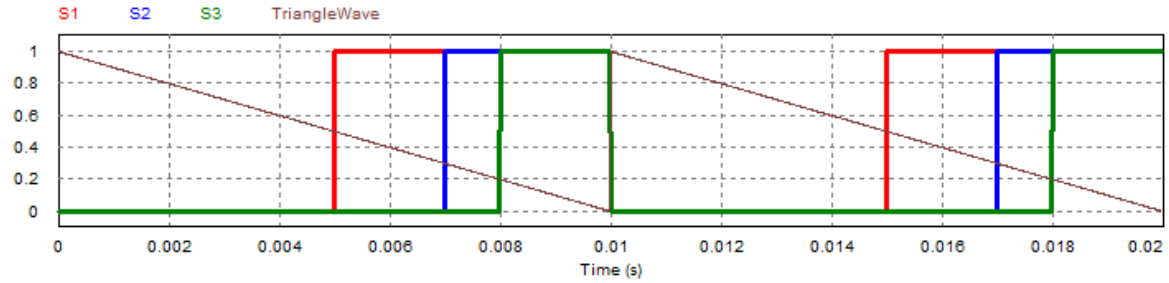



*Figure 30 Normal PWM generation*

In this example the duty cycles for S1, S2 and S3 are 0.5, 0.3, and 0.2 respectively. As we can tell, if we add them together, they sum 1. This is the condition that we previously stablished in theory, however, it is mandatory as we said before that there are no spaces in which no switches are turned on. We can visualize how this does happen on the example shown, and it will happen if all of the 3 switch signals use the same kind of PWM pattern generation.

To overcome this problem the solution that we provide is to generate S1 and S2 with Left-Aligned and Right-Aligned respectively. S3 will be obtained as the remainder of the sum of S1 and S2. The logic circuitry for this is the following:

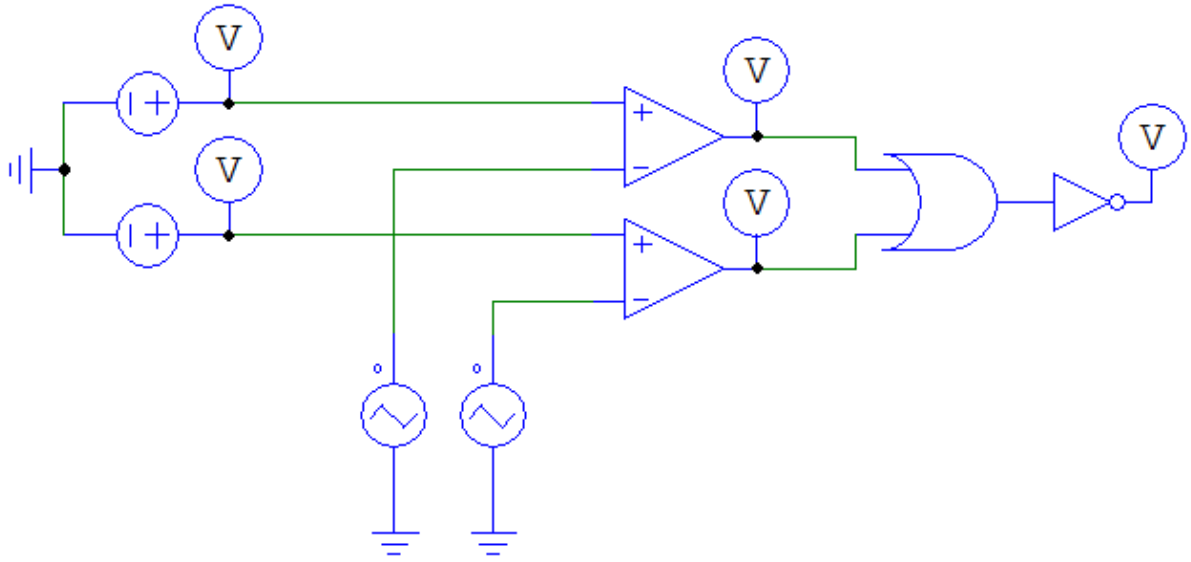



*Figure 31 Logic solution for PWM generation problem*

This are the results that this produces:

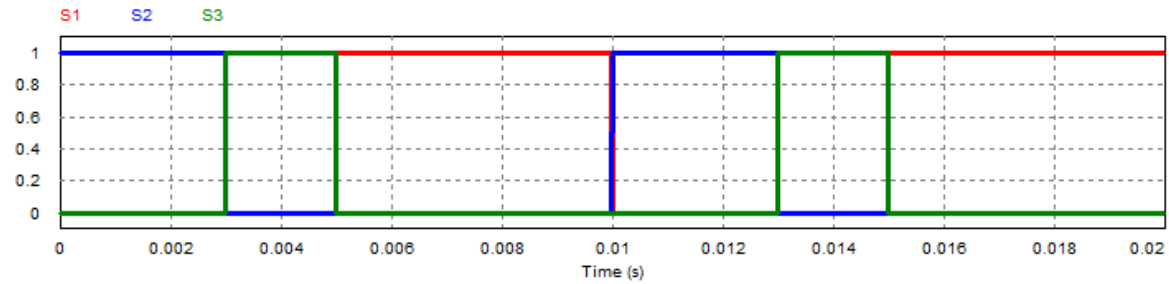



*Figure 32 PWM generation after solution*

As we can see, now there are no null spaces in between the PWM signals and we can assure, by the use of the or gate, that at no time will there be a branch with open circuit.

Having established the theoretical framework for the control block and the PWM generation methodology, we can now advance towards the simulation phase. This step involves executing the control algorithm and PWM pattern generation within a simulated environment to verify the correctness of the implemented code. The simulation will encompass the application of the six duty cycle values generated by the control block to the switches, employing the PWM pattern derived from the comparison with the triangular signal.

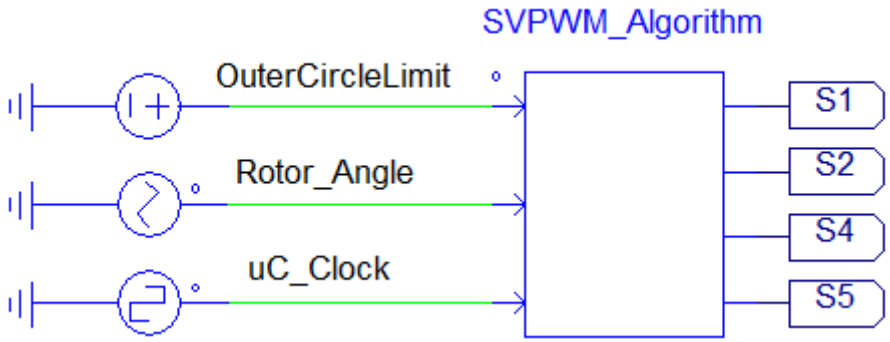



*Figure 33 Implementation of the code block to PSIM*

Through this process, we aim to scrutinize the operational dynamics of the circuit under controlled conditions, assessing the accuracy of the control signals and the stability of the PWM frequency. We will look now at the duty cycle commanded by the control block and see if it's coherent with the predicted one:

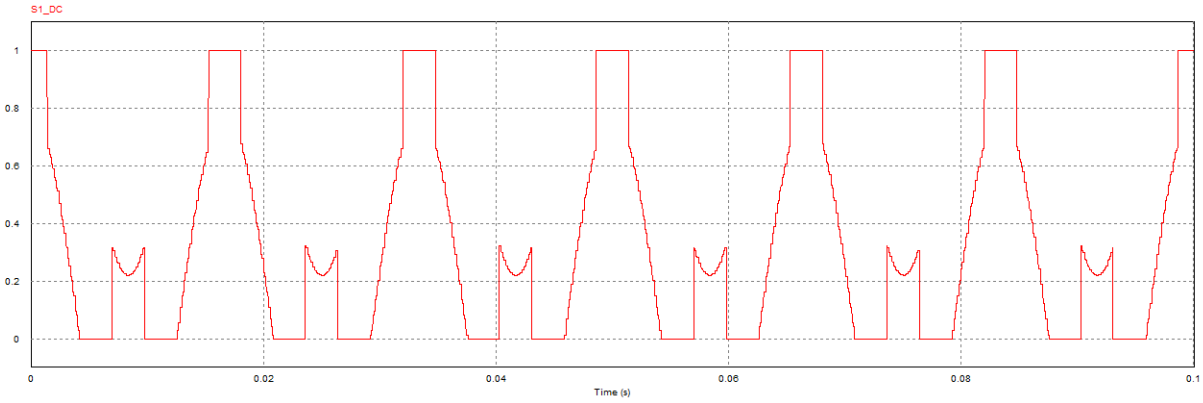



*Figure 34 Duty cycle output of the uC block*

As we can see the duty cycle matches perfectly with the one the Matlab code predicted. Now we can check if the actual PWM signal that the switches will get driven by matches this duty cycle commanded.

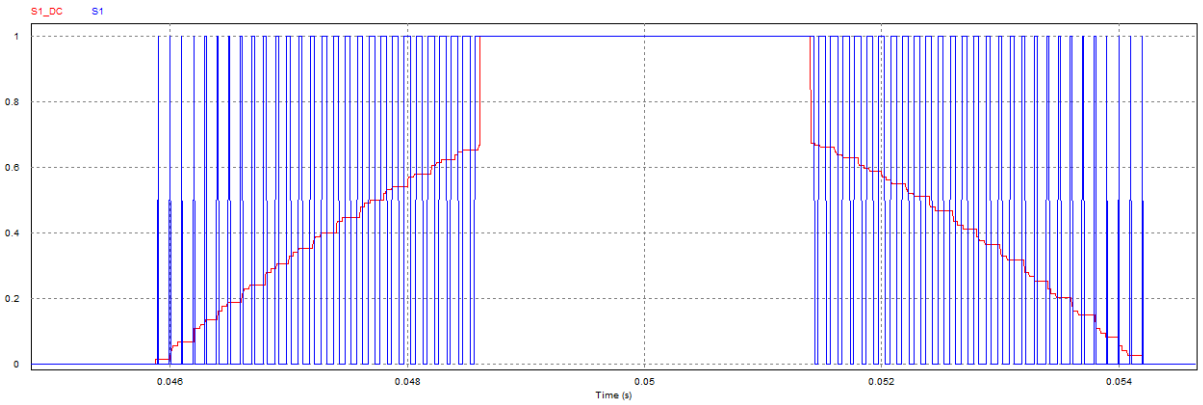



*Figure 35 PWM output signal to the switches*

As we can see, the PWM signal matches perfectly to the duty cycle, so we can now proceed to feed these signals to each one of the switches and see how the system behaves. To do so we will feed a 3-phase inductance load with the generated currents and check for the behavior of it. We should see 3 sinusoidal signals when measuring the current through each branch of the inductance load.

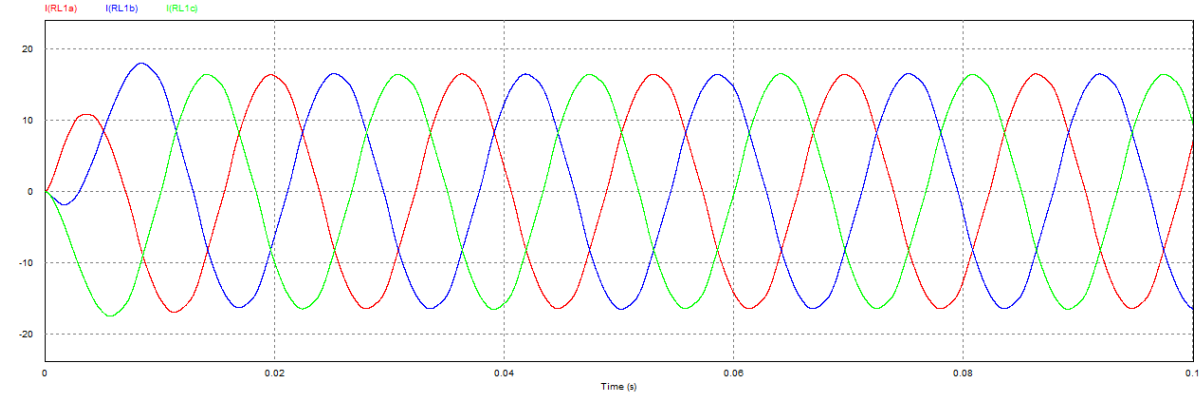



*Figure 36 Final current generated at load*

As we can see we are able to produce a 3-phase current on the inductive load. However, it is important to note that the actual value of the inductive load and the capacitive bank affect greatly the waveform that we can create. For this example, we are working with a load of 50mH and 10 ohm and a capacitor bank with a capacitance of 500uF and 0.5mohm of ESR. This load has been chosen as it matches well with typical 0.9 power factor PMSMs.

The power factor comes from the following calculations:

$$\cos(\phi) = \frac{R}{R + X_L} = \frac{10}{10 + 2\pi \cdot 60 \cdot 5 \cdot 10^{-3}} = 0.841 \quad (7)$$

This is the typical power factor that a common motor will hold during it's working.

## PRE-STAGE

Having successfully designed and operationalized the power and control stages, it is imperative to confront the reality that direct current (DC) sources do not manifest in the physical world. Consequently, the necessity arises to conceptualize and construct a preliminary stage capable of providing a consistent current. To achieve this objective, the employment of a DC-DC converter is proposed. Specifically, the selection has been made in favor of a buck converter, attributed to its superior capability in maintaining a more stable current output.

To transform the buck converter into an effective direct current (DC) source, it is essential to implement a current control mechanism. This entails the development of a current controller, a system designed to monitor the current flowing through the inductor. By accurately measuring this current, the system can adjust the duty cycle of the switching element within the buck converter accordingly. The adjustment of the duty cycle directly influences the converter's output current, ensuring it aligns with the predetermined reference value.

The current controller operates on a feedback loop principle, where the actual current is continuously compared against the desired reference current. Should discrepancies arise, the controller algorithm—often a Proportional-Integral (PI) controller or a similar advanced control strategy—modifies the duty cycle to correct the output current. This real-time adjustment facilitates the maintenance of a constant current output, despite variations in load or input voltage conditions.

For instance, in applications requiring highly stable power supplies, such as precision laboratory instruments or sensitive electronic devices, the ability to provide a consistent DC current is paramount. The buck converter, enhanced with a current control mechanism, becomes an invaluable component by ensuring the reliability and stability of the power supply to these critical applications.

The power design of the buck converter is the following:

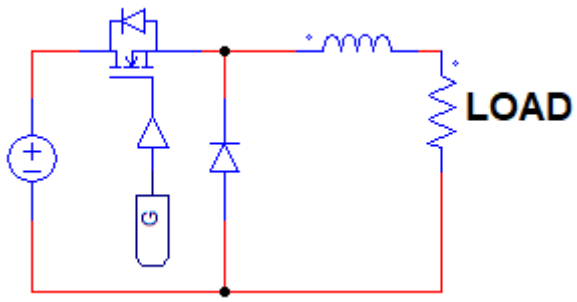



*Figure 37 Pre-stage chematic*

As we can see there is a feedback reading, that goes through the low pass filter, of the current that traverses the inductor. This is then used to feedback to a controller that has a reference on what the output current should be:

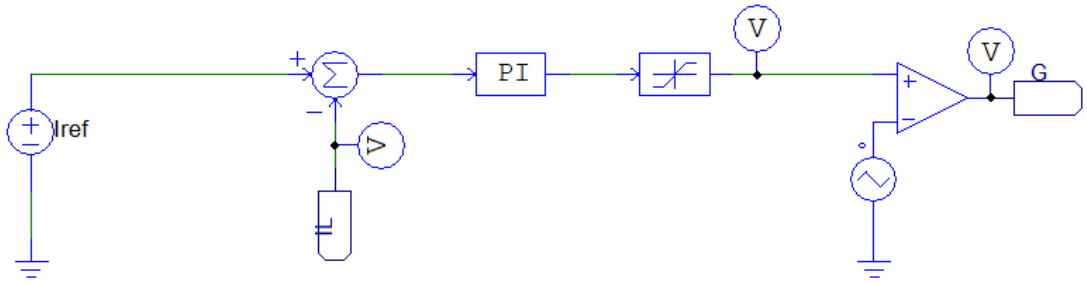



*Figure 38 Pre-stage control*

This control loop is based on a PI controller with a limiter so it can only send values between 1 and 0, as they represent the duty cycle to be fed to the switches. Those duty cycle values are then compared with a triangle wave to generate the appropriate PWM signal and are finally sent to the pre-stage switch. The PI controller is tuned around the stationary point where it would output a duty cycle that closely matches the steady state current demanded by the load. When implemented through code it should also be implemented along with an anti-windup system.

We now need to adjust the PI controller to behave properly and to be able to control the system without many oscillations and with a fast response. Once the PI is adjusted we obtain this response for a 0-100 A jump on the reference:

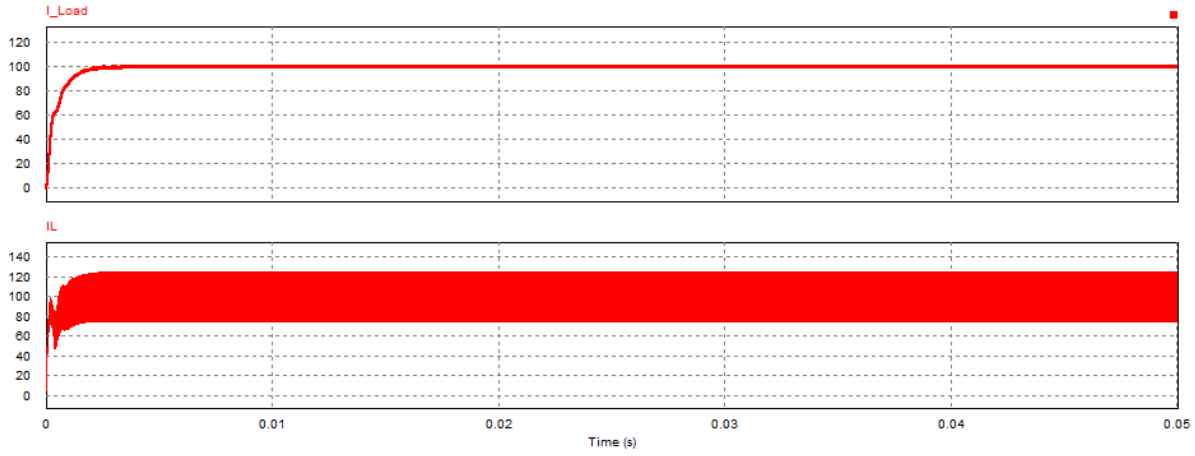



*Figure 39 Pre-stage controled current output*

We are now ready to implement this new “Current Source” into our CSI design and see how it behaves.

## COMBINATION OF ALL 3 STAGES

This is the combination of both the power, the control and the pre-stage put together in a single circuit:

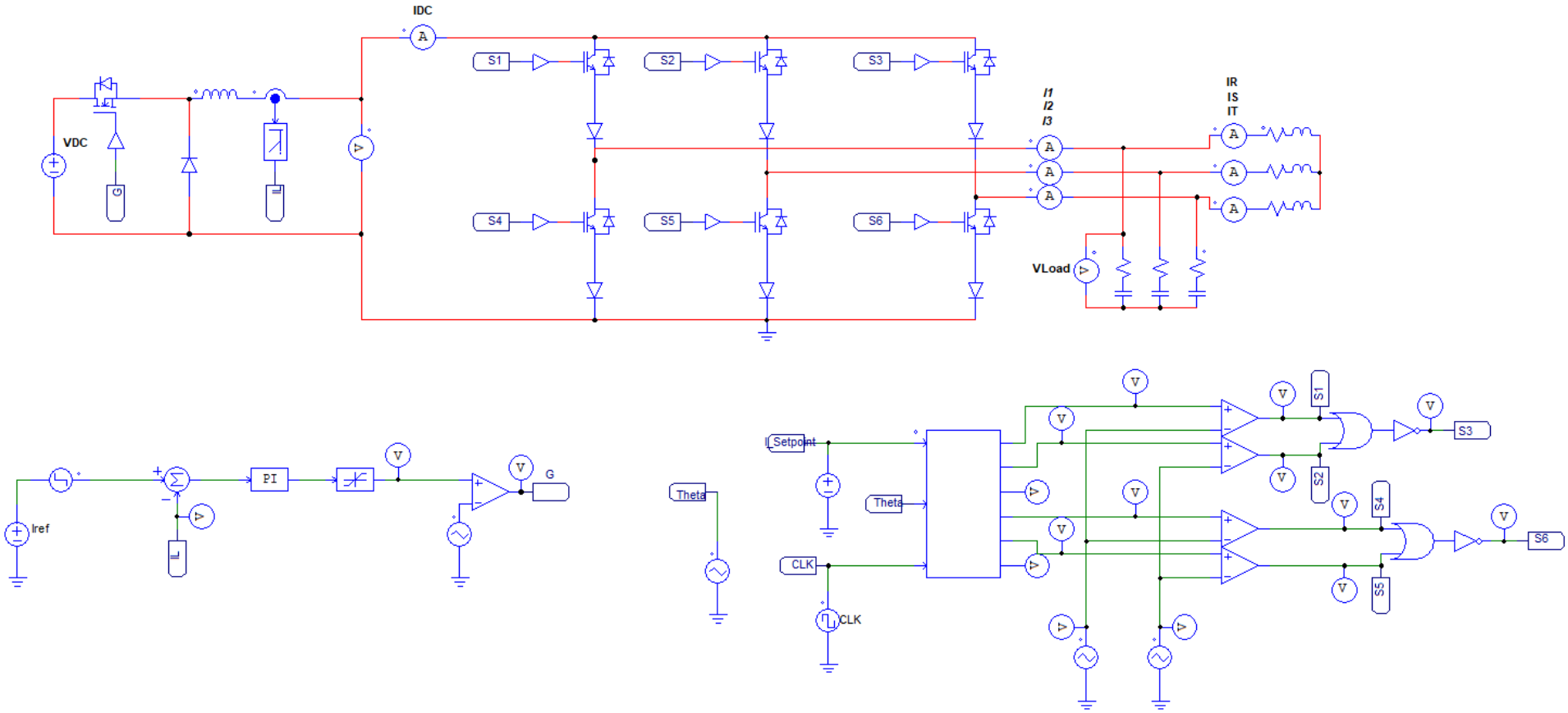



*Figure 40 Full system combination*

We now know perfectly how the system should behave, so the best thing would be to showcase the most important measurements that we need to take. The first important measurement is the dc current that the pre-stage should provide. This is proportional to how big the inductor between the pre-stage and the CSI is. The larger the inductor the less ripple it will have and the better signal we can get on the output currents of the CSI.

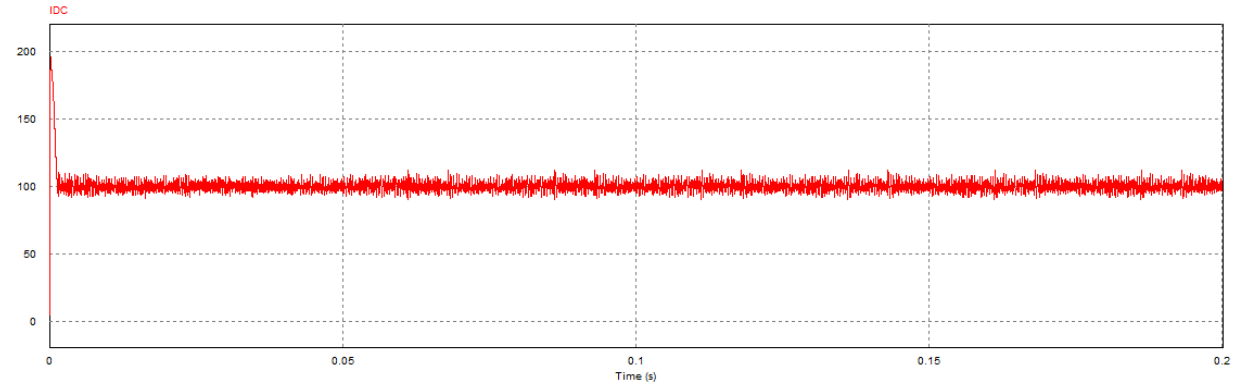



*Figure 41DC current output*

As we can see, after the initial connection of the system, the current through the inductor behaves very good. It is worth noting that we've not opted to include the capacitor of the output voltage of the buck converter, this is because we've noticed that this only increases the ripple current on the dc side.

With this DC current working we can continue to visualize what the output current of the CSI is. We expect it to be a 3-phase sinusoidal current, being filtered by the capacitor bank and the inductive nature of the load.

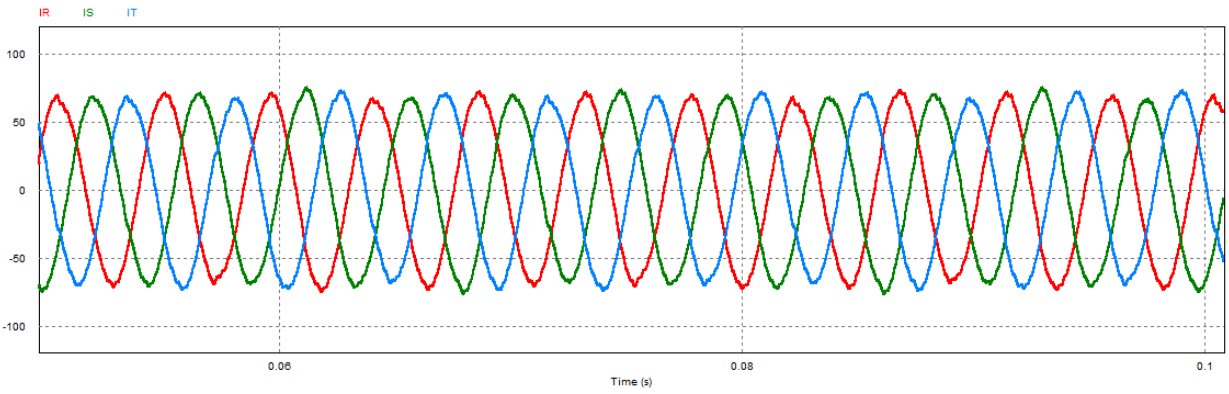



*Figure 42 Modulated currents after filter*

The small ripple we see superposed with the currents is a consequence of the DC current ripple delivered by the buck converter.

We can also visualize the currents going through the the CSI, those are the currents being generated by the inverter.

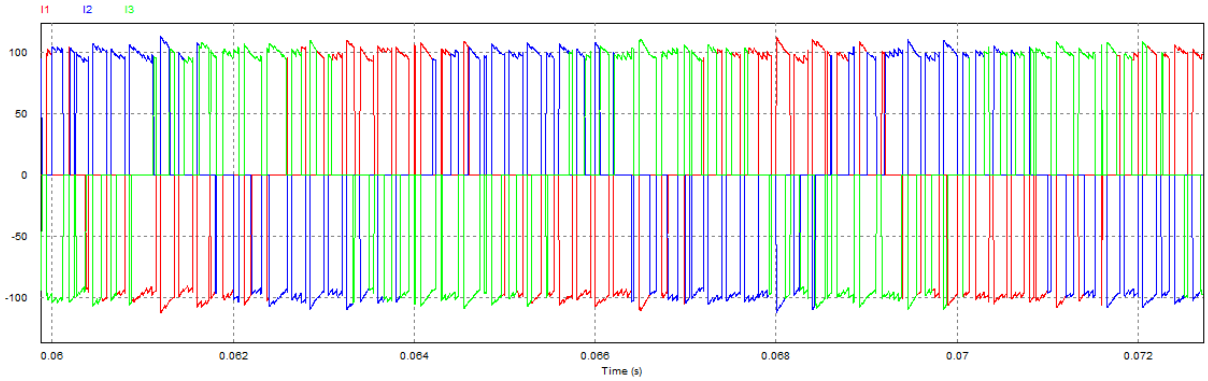



*Figure 43 Current output before filtering*

We can see clearly the PWM sequence of each phase and how the maximum current is the DC current that the pre-stage is providing. To be more precise we can showcase only one phase to be more accurate. We will also show the switching patterns of both S1 and S4 which directly affect the current of the first phase.

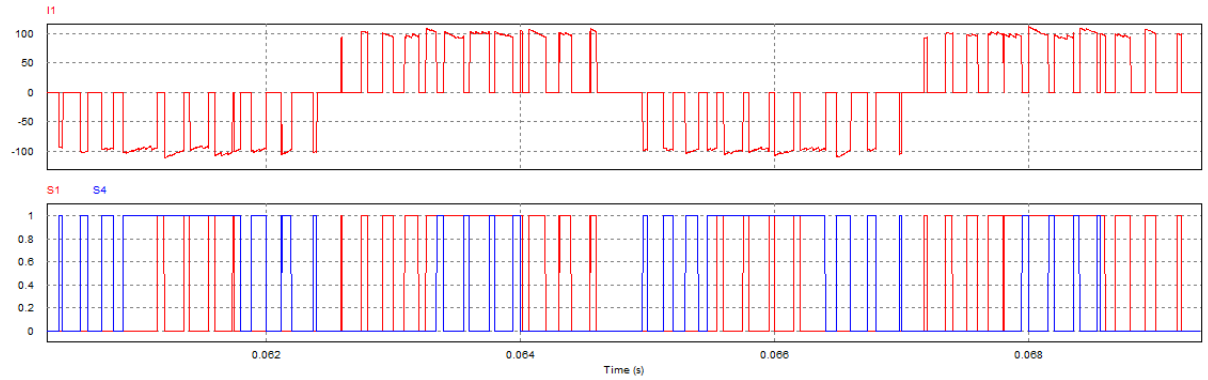



*Figure 44 Current through switches and equivalent pwm signal*

Another thing that we can make sure of now is how the system behaves against a change in the reference current. We will be testing a 50A increase in current demand and we should see the same proportional increase in the output 3-phase currents:

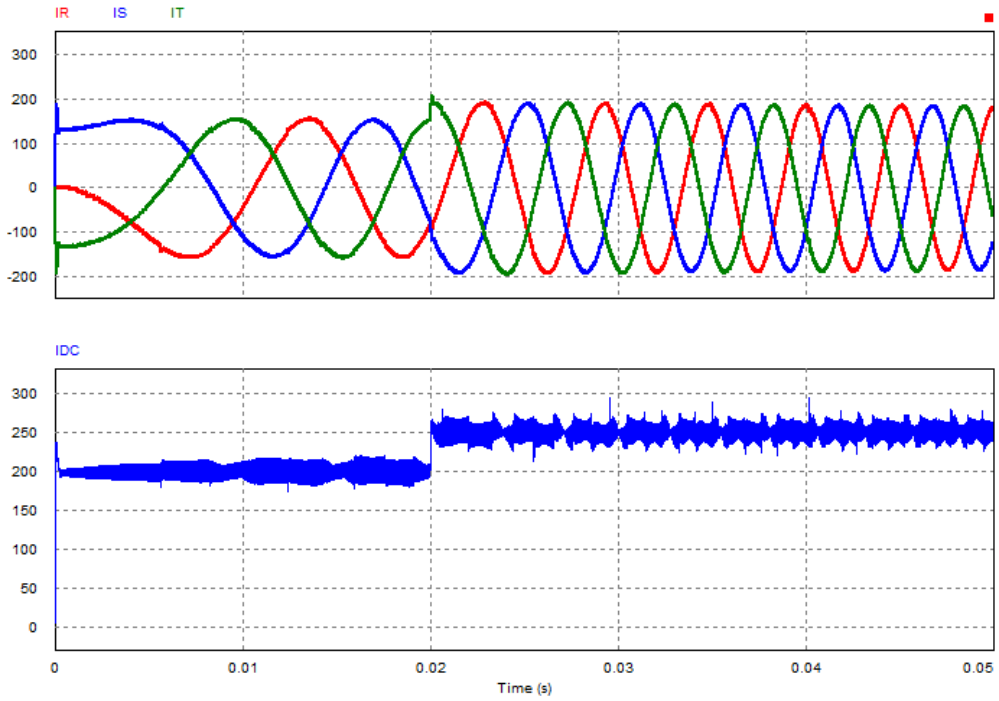



*Figure 45 Current step response*

As we can see, the system now behaves well. Now the next step is to implement the current and speed control for the system. This will be done by means of measuring the rotor position with an absolute encoder. To control the torque, we will use the current to estimate it.

# SPEED CONTROL

In addressing the challenge of speed control for the Permanent Magnet Synchronous Motor (PMSM) using a Current Source Inverter (CSI), it is crucial to integrate a current feedback mechanism. This feedback must be appropriately filtered to ensure accurate current control, which is pivotal for the effective operation of the motor.

## CURRENT FEEDBACK

To actualize this control and facilitate the motor's rotation, it is essential to manage both the q-axis and d-axis currents. The d-axis and q-axis currents are components derived from the transformation of the motor's three-phase current system into a two-dimensional coordinate system, a process which simplifies the analysis and control of the motor. This transformation is achieved using the Park transformation, which converts the three-phase currents into two direct currents aligned with the d-axis (direct axis) and the q-axis (quadrature axis). The d-axis current primarily influences the motor's magnetic flux, thereby affecting its torque production indirectly, while the q-axis current has a direct impact on torque generation.

To optimize torque generation within a Permanent Magnet Synchronous Motor (PMSM) controlled via a Current Source Inverter (CSI), emphasis is placed on the meticulous control of the q-axis current to a predefined reference value, while maintaining the d-axis current at zero. This strategy stems from the inherent characteristics of the q-axis current's role in torque production. The q-axis current generates a magnetic flux that is orthogonal, or 90 degrees, to the motor's main magnetic axis, facilitated by the rotor's permanent magnets. This perpendicular orientation of the q-axis flux relative to the d-axis (or motor axis) is key to maximizing torque output. By aligning the magnetic field generated by the q-axis current in this manner, it interacts most effectively with the rotor's magnetic field, thereby producing the highest torque per ampere of current supplied. This approach leverages the motor's electromagnetic properties to enhance efficiency and performance. Maintaining the d-axis current at zero is a strategic choice that aims to minimize energy losses associated with magnetic field generation that does not contribute to torque production. This ensures that the motor operates with maximum efficiency, as the electrical energy supplied is directly converted into mechanical energy with minimal waste. To achieve the current feedback, we will measure the 3 phase currents and transform them into the d and q axis. This will be done in this way:

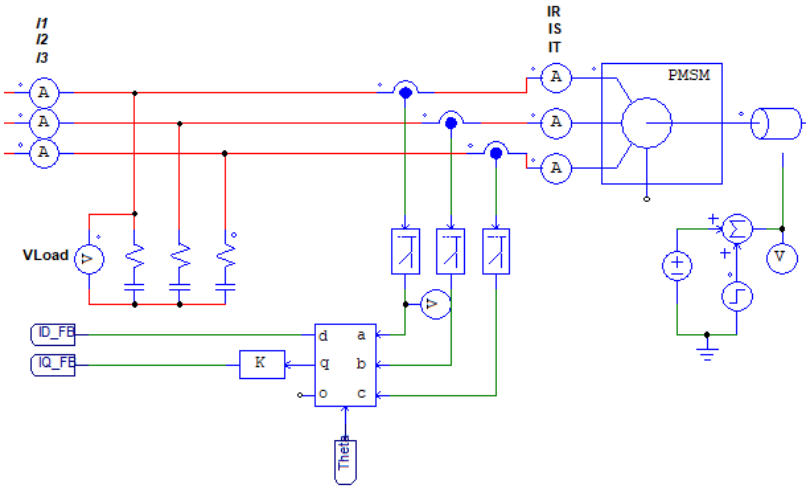



*Figure 46 Current feedback setup*

## ROTOR POSITION FEEDBACK

In addition to current measurement, the Park transform necessitates the rotor's position as an essential input. This requirement is due to the Park transform's function of converting the ab0 vectors coming from the Clark transform currents into two orthogonal components (d and q axis currents) in a rotating reference frame aligned with the rotor's position. To ascertain the rotor's precise position, an absolute encoder is employed. This device is capable of generating a series of pulses that correspond to incremental movements of the rotor, thereby providing a direct measurement of its angular position. The use of an absolute encoder ensures high-resolution position feedback.

Given that the application involves a 4 pole machine, the concept of a "virtual gearbox" is introduced to convert the mechanical angle, as measured by the encoder, into the electrical angle. The electrical angle is a pivotal parameter in motor control, especially for multi-pole machines, because it accounts for the multiple magnetic field cycles that occur within one mechanical rotation of the rotor. This conversion is necessary because the electrical angle turns at a rate that is proportional to the number of pole pairs in the machine, effectively "gearing up" the mechanical rotation to the faster electrical rotation. By implementing this virtual gearbox, the control system can accurately track the electrical position of the rotor relative to the stator's magnetic field, enabling precise modulation of the motor's electromagnetic interactions.

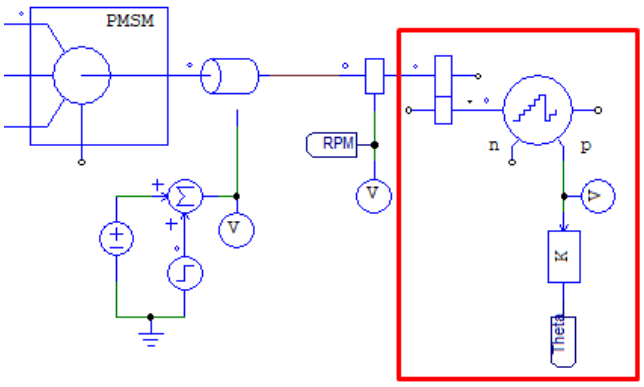



*Figure 47 Speed feedback setup*

## CURRENT CONTOLERS

In the context of implementing speed control for a Permanent Magnet Synchronous Motor (PMSM) the feedback mechanism is intricately designed around the d and q axis currents. These currents are pivotal in providing the necessary information for the control systems to effectively modulate the motor's operation. The control outputs are conceptualized as d and q axis action controls, forming a vector that dynamically aligns with the rotor's position. This vector is characterized by two key parameters: a phase angle and a modulus. The phase angle of the control action is crucial for determining the angle input to the CSI. This is strategically aligned to ensure that the vector follows the rotor's position with optimal synchronicity.

The modulus of the control action, on the other hand, plays a significant role in adjusting the pre-stage of the inverter. The pre-stage is responsible for modulating the current supplied to the motor, with the aim of minimizing zero positions in the CSI operation. Minimizing these zero positions is essential for achieving a smoother response from the system, reducing torque ripple.

By setting the CSI modulus to its maximum value, the control system ensures that the rotating vector remains circumscribed within the hexagon previously described. This geometric constraint aids on maximizing the efficiency of the inverter by maintaining the operational vector within the optimal bounds of the inverter's switching capabilities.

The control scheme that we will use is the following (Steven Pekarek, 2013) as it has been studied to produce a faster and more effective response than a PI controller:

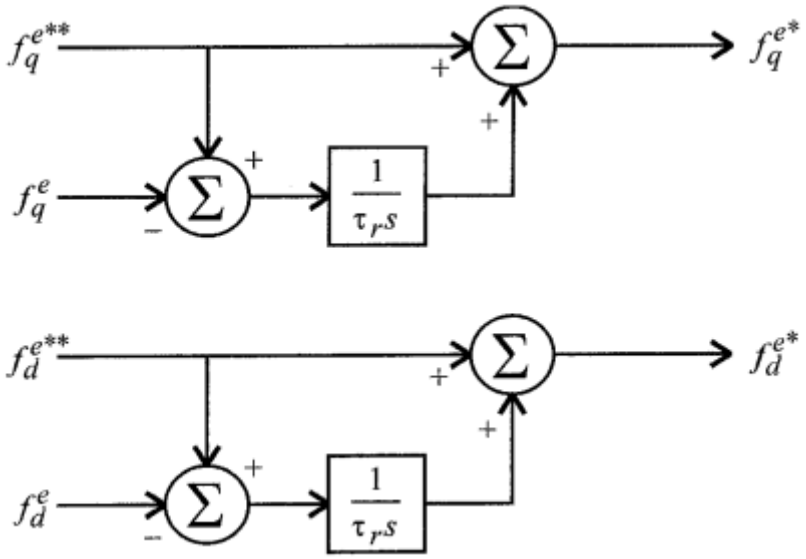



*Figure 48 Control technique diagram used for d and q currents*

# CURRENT CONTROL DIAGRAM

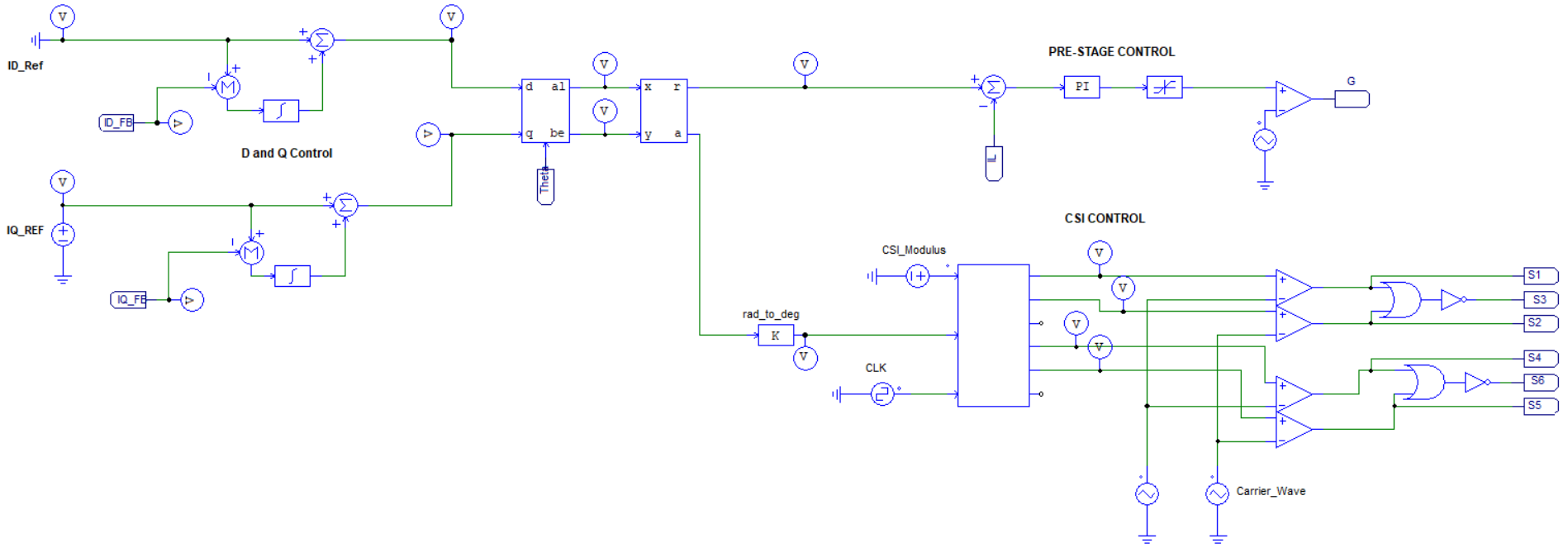



*Figure 49 Overall control diagram*

With the control block now established, our attention shifts to the evaluation of the system's performance through simulation results. This assessment will encompass a comprehensive analysis of several key parameters, essential for verifying the effectiveness of the implemented control strategy on the Permanent Magnet Synchronous Motor (PMSM) operation. The parameters to be analyzed include the d and q axis currents, the current supplied by the pre-stage and the three-phase currents delivered to the motor.

1. **D and Q Axis Currents Analysis:**

The primary focus will be on comparing the actual d and q axis currents to their respective reference values. This comparison is crucial for determining the accuracy and responsiveness of the current control loop. A well-tuned control system should minimize the error between the actual and reference currents, thereby ensuring that the motor operates efficiently and achieves the desired torque and speed characteristics.

2. **Pre-Stage Current Supply Examination:**

The current provided by the pre-stage to the motor will be analyzed to assess its adequacy and stability. The pre-stage plays a crucial role in modulating the current to the motor, and its performance directly impacts the system's overall noise level. This noise level can be modified by increasing or decreasing the size of the inductor between the pre-stage and the CSI.

3. **Three-Phase Currents Evaluation:**

An examination of the three-phase currents being supplied to the motor is essential for understanding the motor's operational dynamics. These currents are the direct drivers of the motor's electromagnetic force and, consequently, its torque production. Analyzing these currents can reveal insights into the phase synchronization, balance, and potential harmonics that may affect the motor's performance. We must note now that the harmonics of the currents can be changed by modifying the filtering capacitors implemented.

# SIMULATION RESULTS

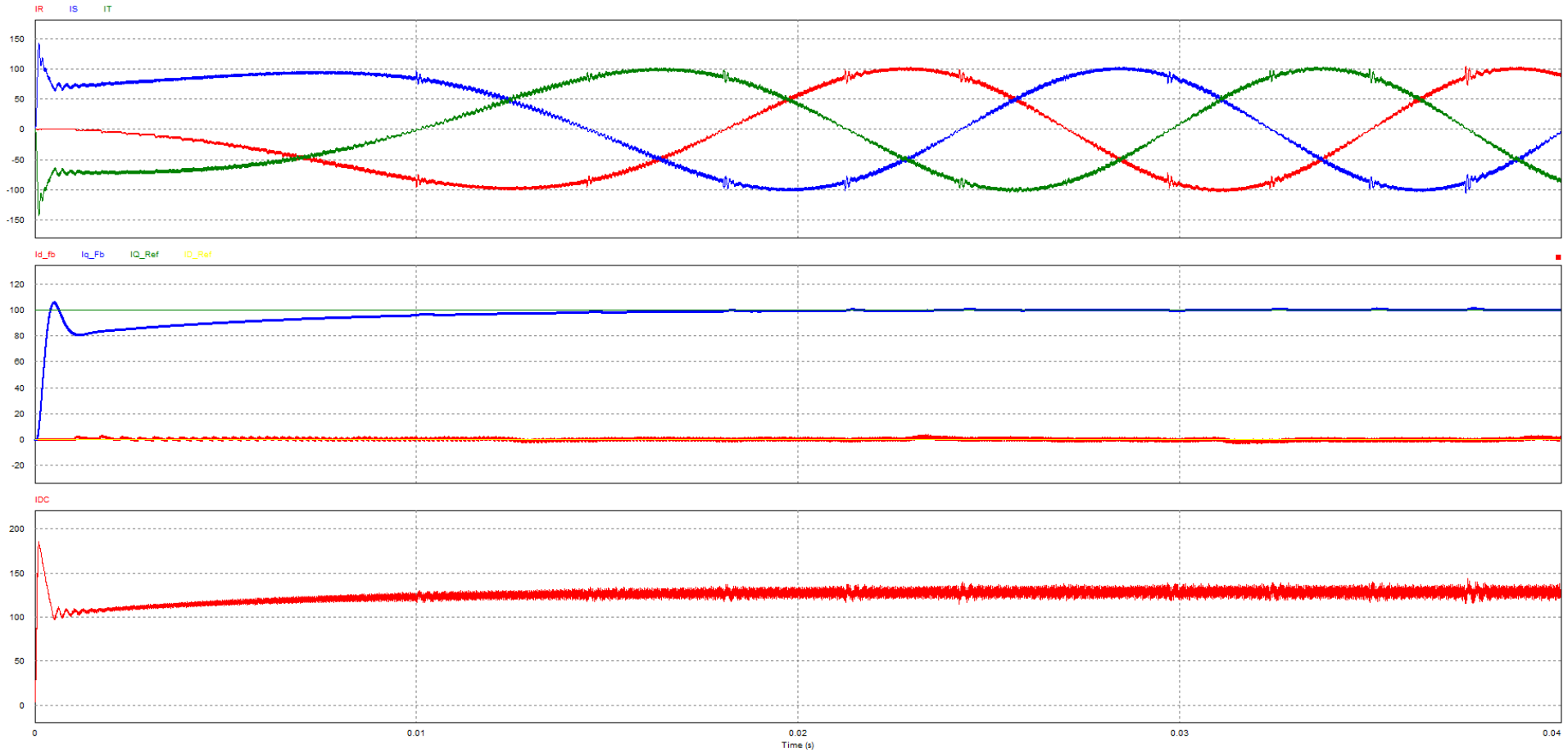



*Figure 50 Simulation resoults*

As we can see the control parameters of the system seem to be well adjusted. We previously mentioned how both the DC current noise component and the harmonic distortion for the 3 phase currents can be adjusted by changing the values of the inductance and the filtering capacitors. With this system working we can now implement a simple speed control that takes the shaft speed as a feedback and controls the q current to maintain a desired speed. There must be noted too that the initial spike of current is due to the initial current flowing through the inductor being 0 and it being an ideal inductor.

## SPEED FEEDBACK

We will use an RPM counter to get the speed feedback from the shaft. In this case we will take the reading from before the gearbox because the speed we are interested in is the shaft or mechanical speed and not the electrical speed.

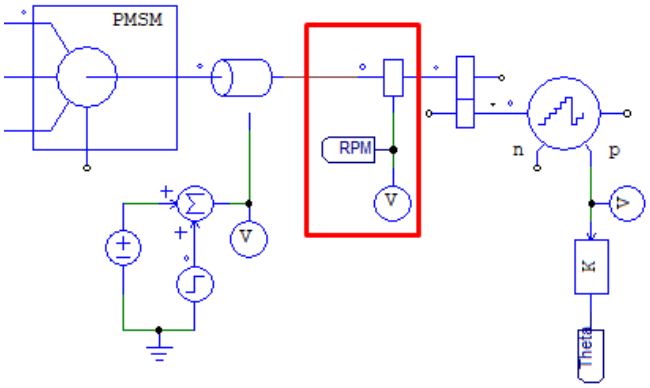



*Figure 51 Speed feedback*

## SPEED CONTROL DIAGRAM

As mentioned before, we will use a simple PI controller that will take the speed sensor as feedback and we will set a reference point for it to follow. The output or action control with be the input of the Q axis current control, as this is the one that produces torque.

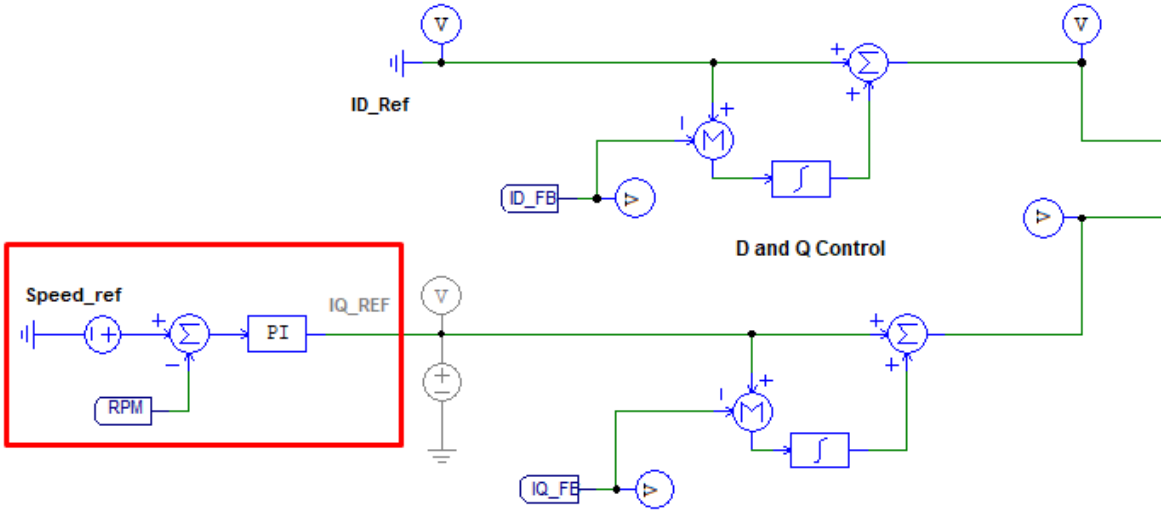



*Figure 52 Speed control diagram using PI*

## SPEED SIMULATION RESOULTS

Here is the response of the reference point for the speed controller. The reference point has been set to the nominal 6600 rpm of the motor we are working with, with a nominal load of 100kW.

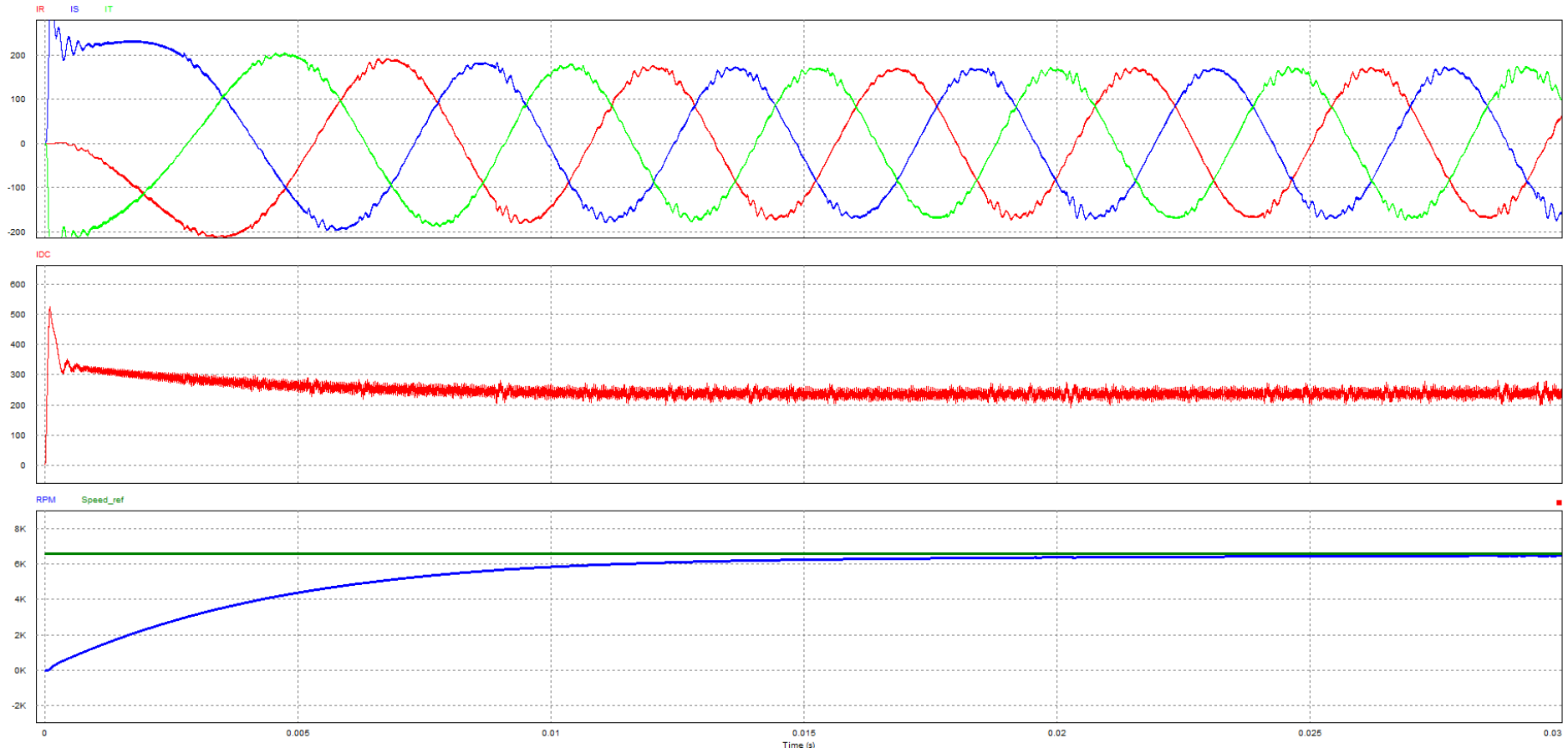



*Figure 53 Speed simulation resoults*

# ADJUSTING PARAMETERS

Transitioning to the optimization phase following the successful implementation of speed control in the PMSM system, the focus shifts towards minimizing the Total Harmonic Distortion (THD) in the three-phase output currents. Achieving low THD is crucial for enhancing motor efficiency and behavior by ensuring smoother operation and minimizing electrical component stress. This optimization must be balanced with the practicality and cost-effectiveness of passive component values within the system.

The inverter's switching frequency significantly influences THD, where higher frequencies can reduce THD through more precise current waveform control, albeit at the expense of increased switching losses. Filter design is also crucial, as optimal selection of inductors and capacitors can effectively reduce harmonics without substantially inflating the system's size or cost.

The quality and specifications of passive components, including inductors and capacitors, are directly linked to the system's harmonic filtering efficiency. Selecting high-quality components that align with operational requirements can enhance performance while maintaining economic viability and physical practicality.

The strategy we will follow involves a comprehensive study on the impact of modifiable parameters on the output currents, focusing on the switching frequency, pre-stage inductor value, and filtering capacitors. By examining how these variables influence the output waveforms, we aim to optimize the system for reduced Total Harmonic Distortion (THD) and improved efficiency. This analysis will allow us to identify the optimal settings that balance performance with practical component values, ensuring the PMSM operates effectively under varying conditions.

We will start by studying how the switching frequency both from the pre-stage buck converter and from the CSI affect the output.

## PRE-STAGE SWTICHING FREQUENCY

We will start from a low switching frequency of 20kHz and will increase it to see how big the change is and decide on the changes. The base values for the inductor and the capacitor will be of 100uH and 50uF for all frequency tests. For the pre-stage frequency testing we will leave the CSI switching frequency at 50kHz.

**20kHz**

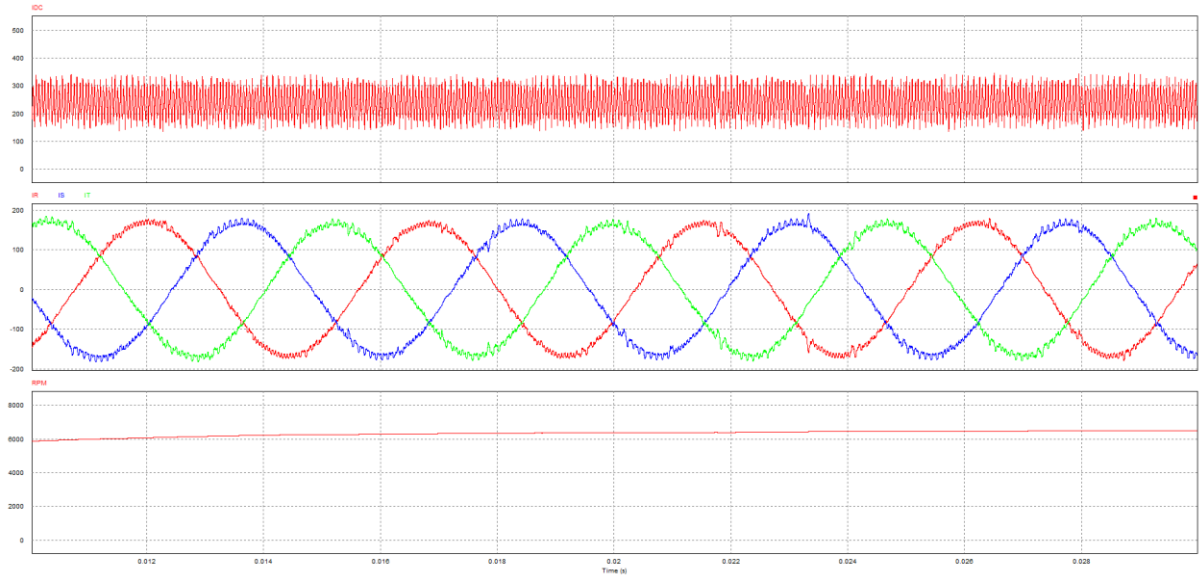


*Figure 54 20kHz pre-stage simulation*

At 20kHz we can see how the DC current has a very noticeable ripple that directly translates to the 3 phase currents. In this case if we perform the THD test when the motor has reached it's nominal speed we calculate it at around 4%. The objective will be to see how increasing or decreasing the pre-stage switching frequency affects it. Let's increase the frequency now to 40Khz.

**40kHz**

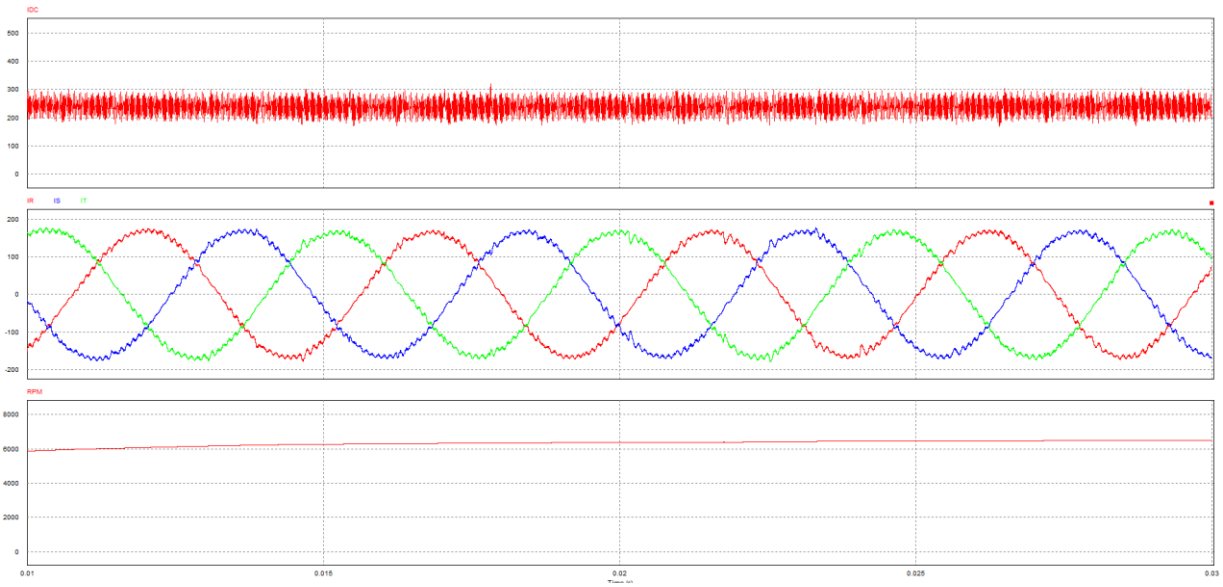


*Figure 55 40kHz pre-stage simulation*

At 40kHz we see a clear reduction in dc current ripple. In this case the calculated THD happens to be 3.5%. The trend here tells us that the higher we go into the switching frequency the better the response will be. We will now test at 60kHz and 80kHz.

**60kHz**

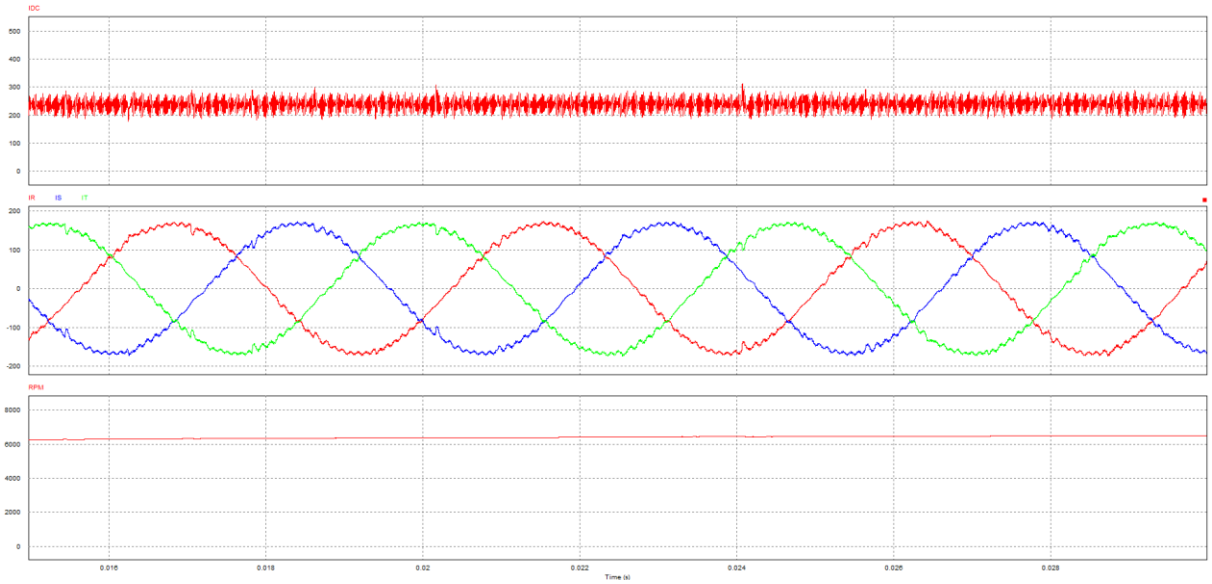


*Figure 56 60kHz pre-stage simulation*

THD = 3.4%

**80kHz**

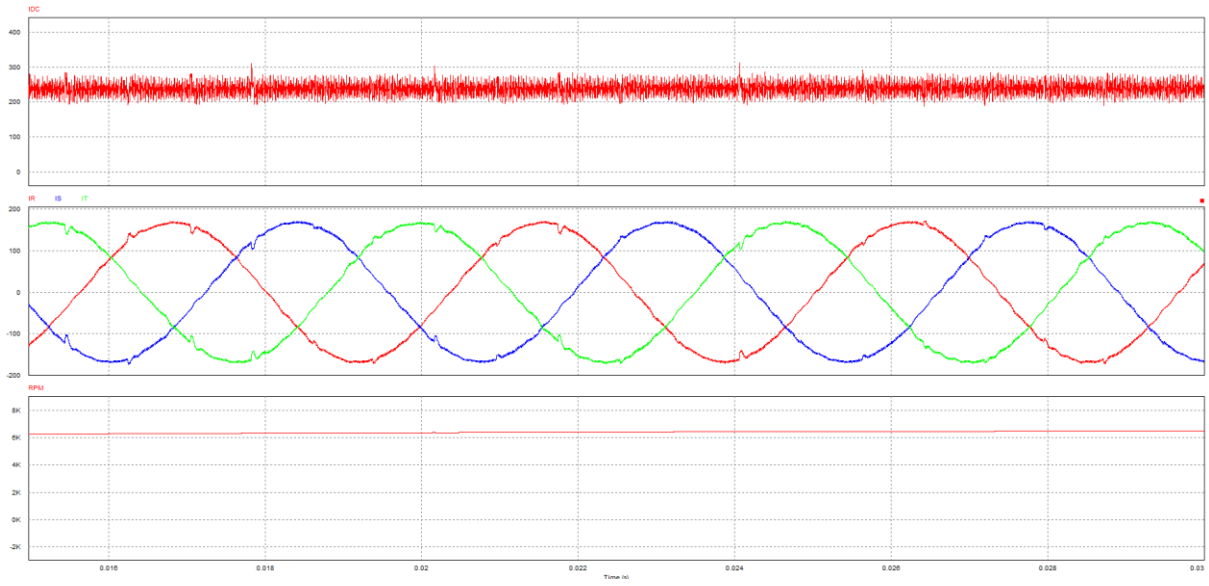


*Figure 57 80kHz pre-stage simulation*

THD = 2.2%

As we can see, the frequency with the best overall performance was the highest at 80kHz. This should come as no surprise as the faster the switching fundamental frequency of the pre-stage the more efficient the filtering capacitors act against it.

We can plot the THD against the commutation frequency of the pre-stage to visualize the effect that this has on the output. We would expect that the more we increase the switching frequency the lower the THD is.

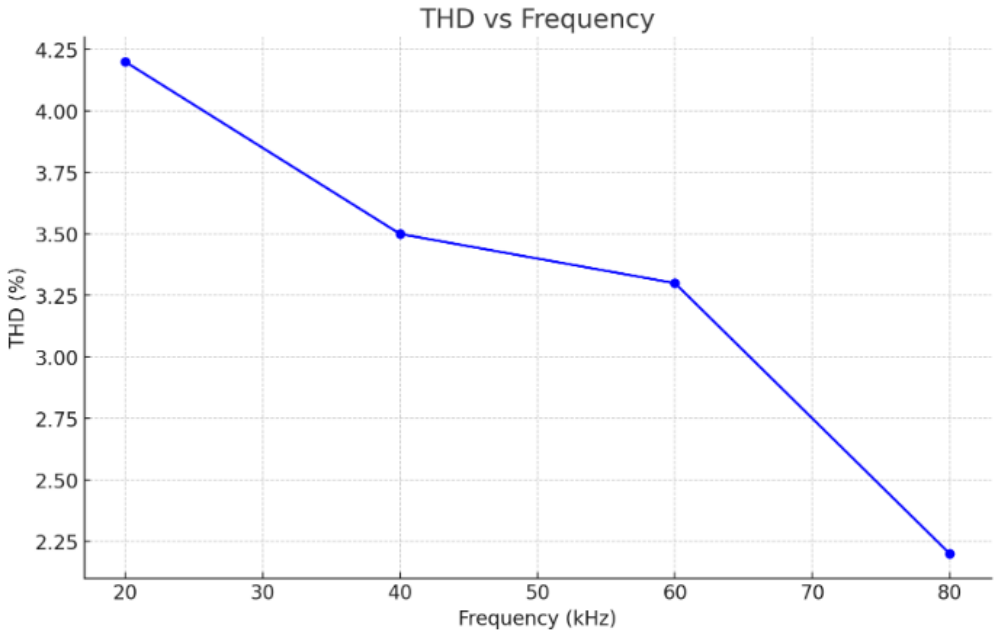



*Figure 58 THD vs Frequency for pre-stage*

So we can conclude that a faster switching frequency on the pre-stage yields us a better response.

# SWITCHING FREQUENCY

Continuing with our examination, we now shift focus from the pre-stage parameters to exploring the effects of varying the switching frequency for the Current Source Inverter (CSI). Similar to our previous methodology, we'll conduct simulations at four distinct frequencies: 20, 40, 60, and 80 kHz, aiming to uncover their impact on the Total Harmonic Distortion (THD) of the output currents. The selection of these specific frequencies is guided by the limitations imposed by the switching technology utilized in our system, with 80 kHz serving as the upper bound based on our prior investigations. Anticipating the outcomes of these simulations, it is logical to expect that an increase in the switching frequency would lead to an improvement in the THD performance. This hypothesis is founded on the premise that higher frequencies should enhance the efficacy of the filtering capacitors' ability to act as low-pass filters, thereby more effectively smoothing the output waveforms and reducing harmonic content.

**20kHz**

*Figure 59 20kHz bridge simulation*

The initial simulation, set at a 20kHz switching frequency, illustrates that this rate is insufficient for effectively filtering out the higher frequencies present in the DC current emanating from the pre-stage. This early observation hints at the interdependent relationship between the switching frequency and the necessary size of filtering capacitors. Lower switching frequencies tend to require larger capacitors to achieve the same level of harmonic reduction, as these capacitors must compensate for the wider range of frequency components not addressed by the switching action. This setup begins to sketch a picture of how crucial the balance between switching frequency and capacitor sizing is, setting the stage for a more in-depth analysis of how these elements interact to shape the system's performance in terms of both efficiency and the mitigation of harmonic distortion. In particular, for this switching frequency we can calculate a THD on the output currents of 75%.

**40kHz**

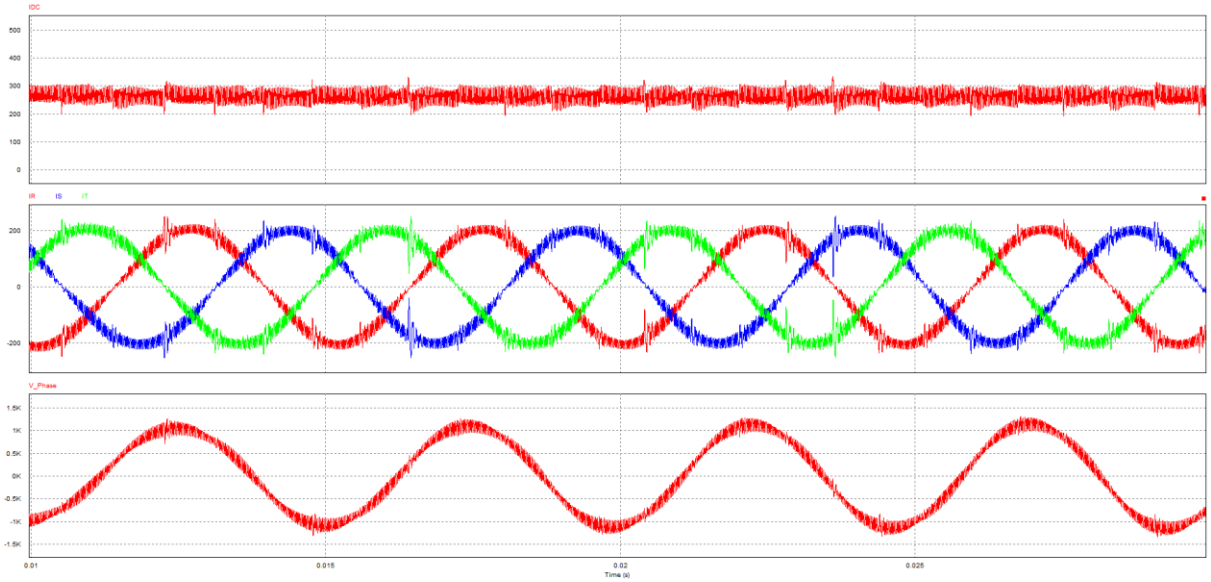


*Figure 60 40kHz bridge simulation*

At a 40kHz switching frequency, there's a notable improvement in system performance, evidenced by a Total Harmonic Distortion (THD) of 11%. This outcome reinforces the hypothesis that increasing the switching frequency enhances the system's ability to filter out undesirable harmonics, thereby improving the quality of the current output. The reduction in THD at this frequency level suggests a positive correlation between switching frequency and system efficiency, aligning with the premise that higher frequencies facilitate better harmonic filtering.

**60kHz**

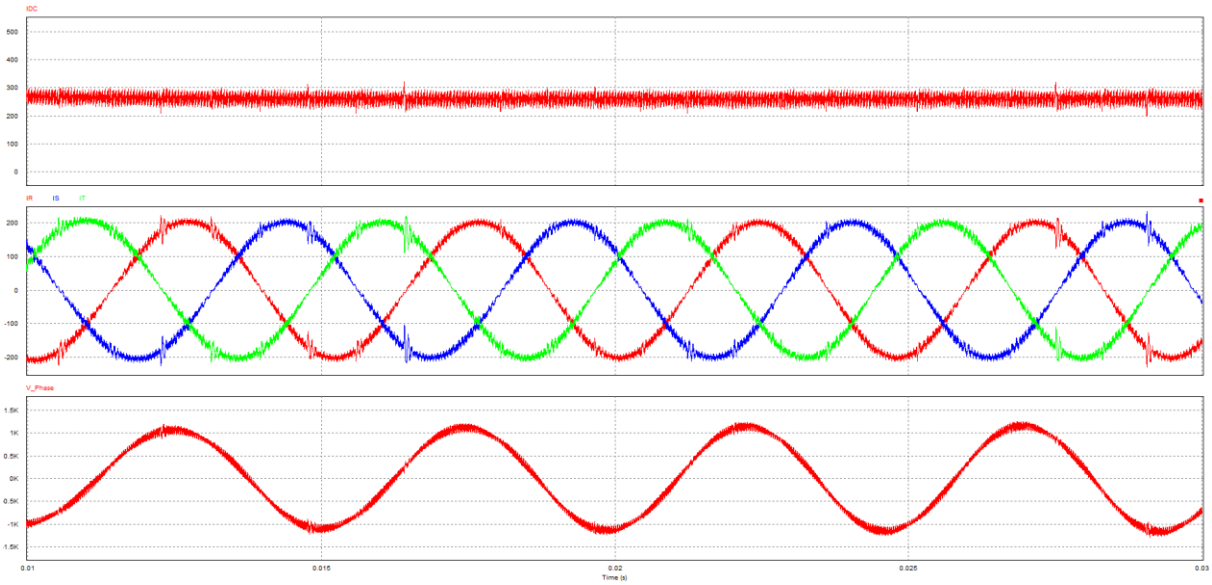


*Figure 61 60kHz bridge simulation*

THD = 6

**80kHz**

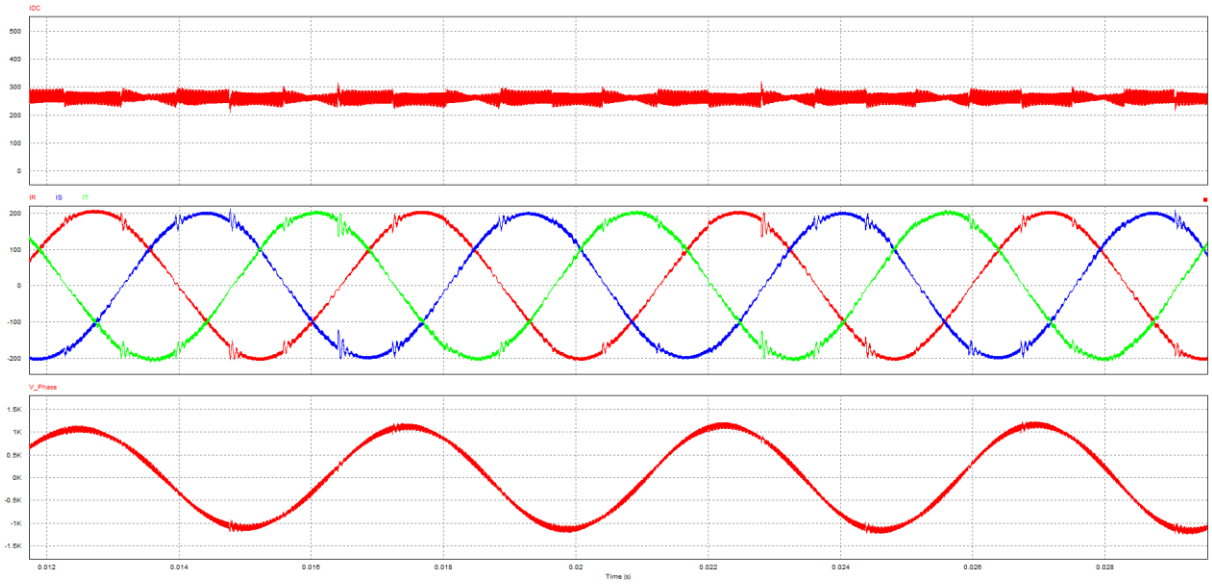


*Figure 62 80kHz bridge simulation*

THD = 3.5%

As we can see our predictions match the results of the simulations. Now let's proceed and graph again the distribution of the values measured.

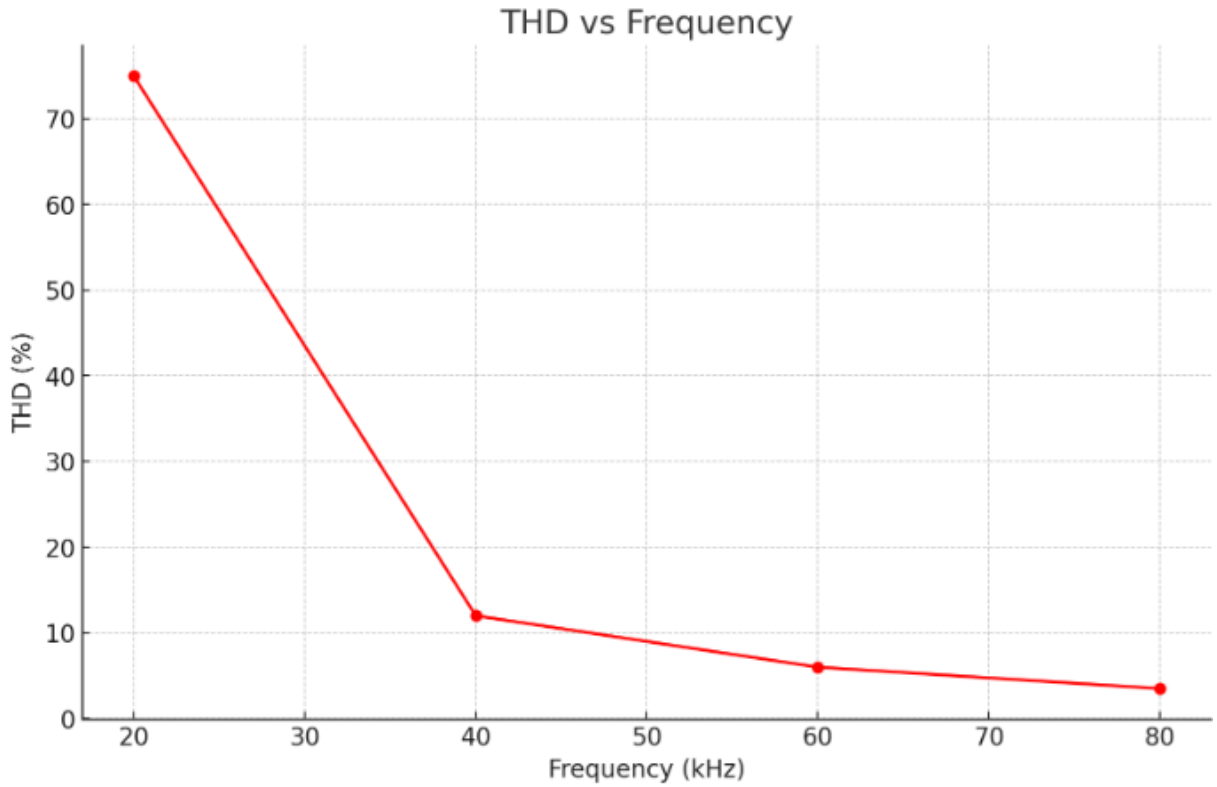



*Figure 63 THD vs Frequency for bridge*

We can conclude again that the higher the frequency the better the response we will obtain when it comes to the CSI.

## CAPACITOR SIZING

Shifting focus to the impact of capacitor size on Total Harmonic Distortion (THD) performance introduces a complex dimension to the optimization of the system. Unlike the relatively straightforward relationship between switching frequency and THD, the effects of capacitor size are multifaceted, influencing not only the THD but also the cost, physical dimensions, and filtering effectiveness of the system. Consequently, an analytical approach is warranted to understand how changes in capacitance affect the filter's ability to mitigate harmonic distortion.

This analytical study will involve examining the electrical characteristics of the filter capacitors, such as their impedance, which decreases with increasing frequency and capacitance, thereby affecting the filter's efficiency in blocking or passing certain frequency components. The approach that we will follow is to describe the per-phase equivalent of the motor to both study the system and to analyze if the equation we come up with is valid.

The aim is to derive insights into optimal capacitor sizing that can achieve the desired harmonic filtering performance without imposing undue burdens on the system's design and overall feasibility.

### PHASE ANALYSIS

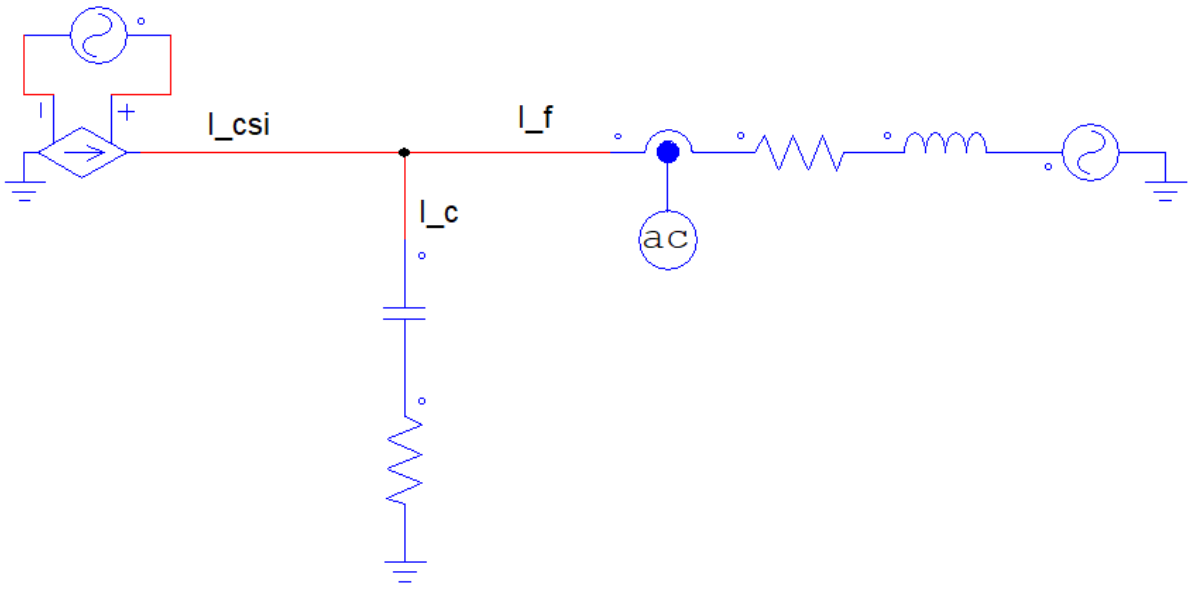



*Figure 64 Per-phase filtering equivalent*

This will be our phase equivalent circuit extracted from the parameters of the motor and the filtering capacitors. We are interested in how the current to the load ($I_f$) behaves with respect to the current sent by the CSI ($I_{csi}$). Let's start by applying the node theorem to compute the currents entering and exiting the node.

$$I_c \cdot X_c = I_f \cdot (R + X_l) + V_{EMF} \tag{8}$$

$$I_c = I_{csi} - I_f \tag{9}$$

Combining these two equations we get the following:

$$I_{csi} \cdot X_c - I_f \cdot X_c = I_f \cdot (R + X_l) + V_{EMF}$$

*( 10 )*

We can group terms and isolate the current from the CSI and the current to the load:

$$I_{csi} \cdot X_c = I_f \cdot (R + X_l + X_c) + V_{EMF}$$

*( 11 )*

As we are only interested in the behavior of the load current with respect to the CSI current, we can ditch the voltage term and express a transfer function with both currents.

$$\frac{I_f}{I_{csi}} = \frac{X_c}{R + X_l + X_c}$$

*( 12 )*

Now we proceed to express all impedances in the Laplace form to study them using Matlab. To do so we won't be taking into consideration the ESR of the capacitors, and that is because that will increase the complexity of the system and it being so small it will barely affect the output result.

$$\frac{I_f}{I_{csi}} = \frac{\frac{1}{s \cdot C}}{R + s \cdot L + \frac{1}{s \cdot C}} = \frac{1}{s^2 \cdot LC + s \cdot CR + 1}$$

*( 13 )*

We can now proceed to study this transfer function. We can do so by studying the bode plot of the system and in that way, we can compute the exact cut-off frequency of the filter. For a second-order system the cutoff frequency $\omega_n$ can be calculated like:

$$\omega_n = \frac{1}{\sqrt{LC}}$$

*( 14 )*

To now study the bode plot we must previously know what frequencies we are trying to filter out, to do so we will study the FFT of the currents in $I_{csi}$:

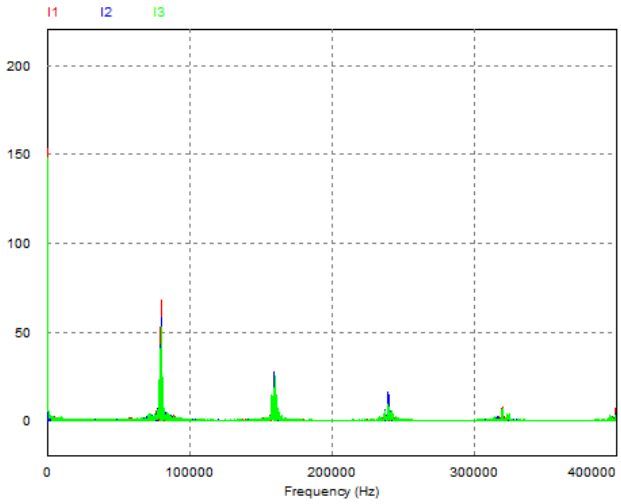



*Figure 65 THD study for the output currents*

We can see that the first frequency that we need to filter is precisely the 80kHz at which we are switching, if we want to decrease 10 times the value of the filtered components, we need a 20db attenuation. Given that a second order filter will give us -40db/dec we need our filtering point at:

$$20\ dB \cdot \frac{1}{40\ \frac{dB}{dec}} = 0.5\ dec \rightarrow 50kHz$$

*( 15 )*

So we need the filtering point to be, at least 50kHz prior to our 80kHz switching frequency. That is, our cut off frequency must be at 20kHz. If we apply the formula for $\omega_n$ that we calculated previously, knowing that the equivalent per phase inductance of the motor we are working with is 6.31 uH, we obtain:

$$f_{cut-off} = \frac{\frac{1}{\sqrt{C \cdot L}}}{2 \cdot \pi} \rightarrow C = 10.036\ uF$$

*( 16 )*

This means that we need at the very least 10uF per phase to decrease 10 times the higher frequency components that occur due to the switching frequency. It is obvious that the more we increase the capacitance the lower the cut-off frequency will be and therefore the more we will decrease the higher order components, but that comes as a cost.

We can also compute the ripple voltage that we will observe at the load using the following formula:

$$\Delta V_{cf} = \frac{I_{dc}}{4 \cdot f_{switching} \cdot C}$$

*( 17 )*

For our values, given that at full load the system will consume around 273 Arms the ripple voltage that we expect to see is around 85V peak to peak.

We can verify the filtering values by simulating the bode plot with matlab:

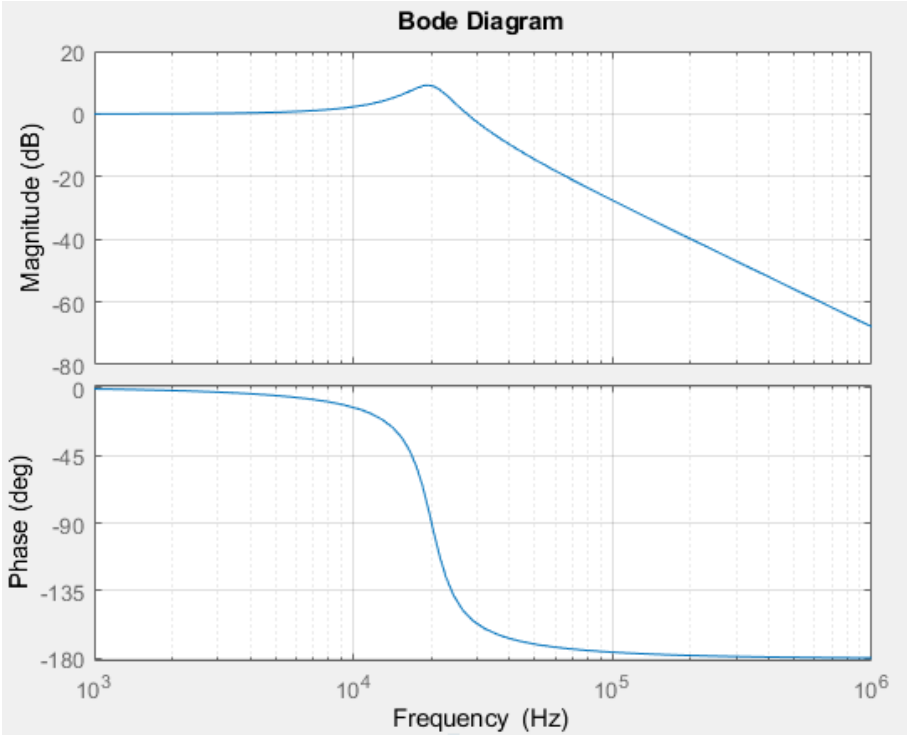



*Figure 66 Filter bode diagram from model*

As we can see the filtering cut-off frequency is at 20kHz as we expected it to be. And the same we find if we do an AC sweep with our equivalent frequency and the filtering values that we calculated:

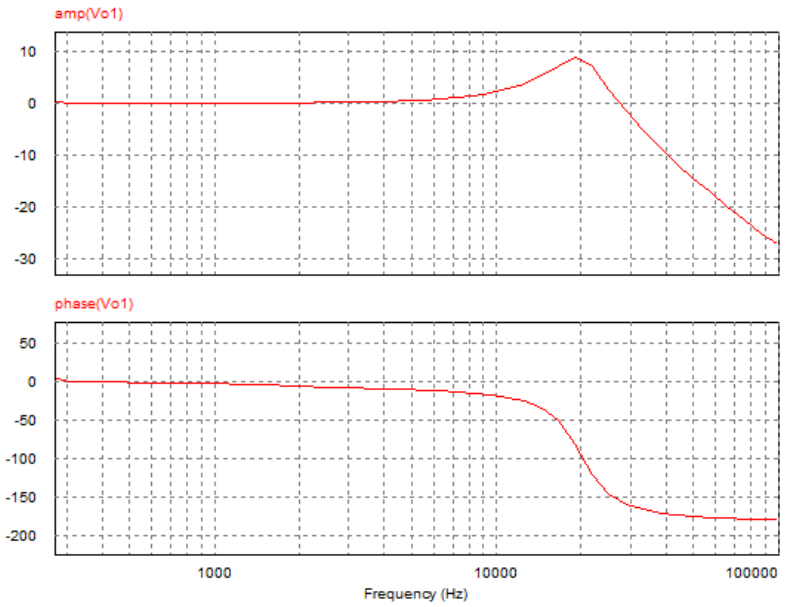



*Figure 67 Filter bode diagram from simulation*

Considering the 10uF capacitance requirement for optimizing THD performance, it's indeed feasible to source such a value from commercial distributors. The availability of 10uF capacitors is relatively common, and even if single capacitors with the required specifications are not available, achieving the desired capacitance by connecting multiple capacitors in parallel is a

practical and effective strategy. This approach not only allows for flexibility in meeting the capacitance needs but also addresses the challenge of handling high ripple RMS currents, which can be problematic for a single capacitor. By distributing the current across several capacitors, each component bears a portion of the total ripple, thereby reducing the stress on individual capacitors and enhancing the system's overall reliability and durability.

One possible option would be to use Panasonics line of polypropylene film capacitors, more specifically the model ECWFG1B505J. The three most important parameters from this capacitor is the capacitance, RMS permissible current and voltage rating.

■ Rated voltage [DC] : 1100 V Capacitance tolerance : ±5 %(J)

| Part No | Cap. (μF) | Dimensions (mm) | | | | | | | Permissible current *1 (Arms) | ESR [Typ.]*2 (mΩ) | ESL [Typ.]*3 (nH) | Min. order Q'ty (PCS) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | L | T | H | F | ød | P | Q | | | | Straight | Cut lead |
| ECWFG1B105J( ) | 1.0 | 31.5 | 10.5 | 21.0 | 27.5 | 0.8 | 0±1.0 | 2.0 | 3.3 | 36.5 | 17 | 300 | 300 |
| ECWFG1B155J( ) | 1.5 | 31.5 | 12.0 | 24.5 | 27.5 | 0.8 | 0±1.0 | 2.0 | 4.1 | 24.1 | 18 | 200 | 250 |
| ECWFG1B205J( ) | 2.0 | 31.5 | 12.0 | 24.5 | 27.5 | 0.8 | 0±1.0 | 2.0 | 4.8 | 18.7 | 13 | | |
| ECWFG1B225J( ) | 2.2 | 31.5 | 13.5 | 28.5 | 27.5 | 0.8 | 0±1.0 | 2.0 | 5.1 | 17.1 | 19 | 150 | 150 |
| ECWFG1B305J( ) | 3.0 | 31.5 | 16.0 | 29.5 | 27.5 | 0.8 | 0±1.0 | 2.0 | 6.3 | 12.7 | 19 | | |
| ECWFG1B335J( ) | 3.3 | 31.5 | 16.0 | 29.5 | 27.5 | 0.8 | 0±1.0 | 2.0 | 6.7 | 11.5 | 17 | | |
| ECWFG1B405J( ) | 4.0 | 31.5 | 17.5 | 32.5 | 27.5 | 0.8 | 0±1.0 | 2.0 | 7.5 | 9.6 | 19 | 100 | 100 |
| ECWFG1B475J( ) | 4.7 | 31.5 | 18.5 | 35.0 | 27.5 | 0.8 | 0±1.0 | 2.0 | 8.3 | 8.2 | 18 | | |
| ECWFG1B505J( ) | 5.0 | 31.5 | 18.5 | 35.0 | 27.5 | 0.8 | 0±1.0 | 2.0 | 8.6 | 7.7 | 15 | | |

＊( ) : Suffix for lead crimped *1 : 70 ℃, 10 kHz *2 : 20 ℃, 10 kHz *3 : 20 ℃

*Table 2 Capacitor sizing table*

In this case we see that the model chosen doesn't comply with all our needs by itself, however, It does comply with the Voltage rating. This means that we can set enough of them in parallel to make it withstand the current parameters and check if the capacitance rating matches our needs.

We know that by setting capacitors in parallel the current through them is reduced by the same rate as capacitors we set up. In the same way, the capacitance increases with the same rate. For our purpose, we will install at least 16 capacitors in parallel, so they only have to withstand 7.75 Arms each. The overall capacitance will be 80uF, which will greatly increase the filtering capabilities of the capacitor bank.

## INDUCTANCE ANALYSIS

Analyzing the appropriate size for the DC link inductor, situated between the pre-stage and the Current Source Inverter (CSI), is a crucial step in optimizing the system's performance. This inductance plays a vital role in stabilizing the current through the load during the intervals between switching events. The choice of inductance is critical because it directly influences the ripple present in the DC current, which, in turn, affects the magnitude of ripple observed in the three-phase output currents.

The relationship between the inductor size and the current ripple is inversely proportional, a larger inductance results in a smaller ripple. The goal is to select an inductance value that ensures the ripple current does not exceed 20%-25% of the RMS value of the DC current under normal load conditions. This threshold is set to maintain system stability and efficiency, preventing excessive ripple that could lead to performance degradation or component stress.

Selecting the right inductance involves a careful balance. An inductor that is too large could unnecessarily increase the system's size, cost, and potentially introduce higher resistance, reducing efficiency. Conversely, an inductor that is too small might not sufficiently mitigate the ripple, impacting the system's performance and longevity. Therefore, the chosen inductance must provide adequate ripple control without imposing significant drawbacks.

Given a DC current of around 290 Arms we will compute what value of Inductance gives us a low enough peak to peak current ripple. To do so we will use the following equation:

$$L_{DC} = \frac{\sqrt{3} \cdot V_{phase_{pk}}}{4 \cdot f_{sw} \cdot \Delta I_{dc}} = 106\ uH \tag{18}$$

Four our given case of 80kHz, and around 1.1kV of phase voltage peak.

We have to keep in mind that the ripple current that we see on the DC link inductor is not the one that we will eventually observe on the load, as the currents are being filtered and the high frequency components of the signal that correspond to that ripple will be filtered to approximately 10 times less than their actual value, so a higher ripple current is admissible here.

Also we must note that there are no commercially available inductors of those characteristics, specifically due to the high DC current that the Inductor will be subject to. This is why the inductor will have to be custom made for the application. Also note that we can further reduce the inductor value if we mount 2 serial inductors both on the forward and return branches of the pre-stage, effectively halving the inductance required.

## INDUCTOR DESIGN

In this section we will study how the inductor design could be approached. As mentioned above there are no commercially available inductors that fit our design in terms of current and inductance. This means that the best option will be to fabricate one ourselves. To do so we will make use of a commercially available magnetic core and we will check if the one we decided fits our purpose or not and how many turns and cable we should use.

To start the design the tool of use will be the Micrometals design tool. We can make use of this tool because our inductor matches one of the cases they offer, in this case the DC inductor. We need to provide the DC current, The switching frequency and both the on and off voltages on the inductor. The DC current needed is a known parameter that is easily calculated with the RMS value of the steady state inductor current on the simulation. The same goes for the switching frequency, it is a known parameter. What we haven't shown yet is the on and off voltages at the inductor. To do so we can add a voltmeter and read them on the simulator, as well as the switching pattern for the pre-stage switch.

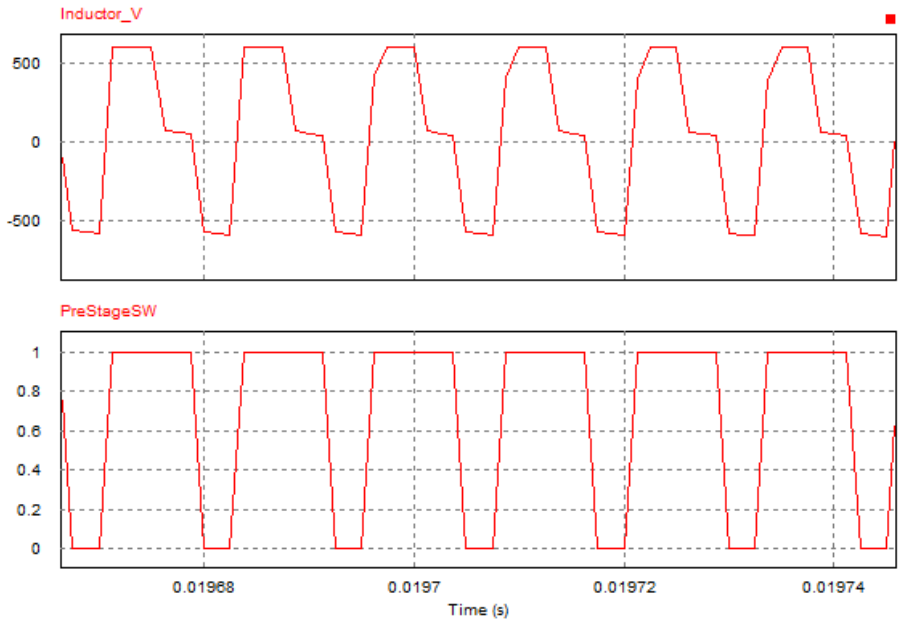



*Figure 68 Inductor voltage and switching state*

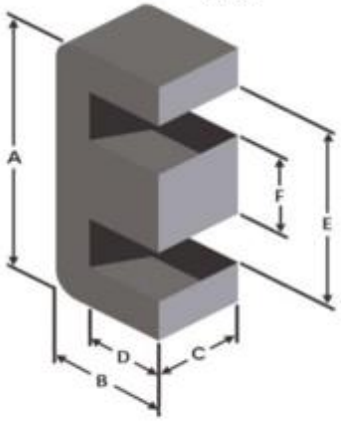
From here we can measure both the duty cycle of the pre-stage switching and the mean voltage when the switch is on and off. The values that we obtain can be plugged into the Micrometals tool and we obtain a matching duty cycle with what we obtain from the simulation and a peak-to-peak current that is around the 20% that we would expect.

This yields us a result of what Micrometals believes the best matching inductor core is for our purpose. In this case it suggests using the EBMS-300125030-060 inductor core. We can analyze ourselves the core and check if it will be suitable for our purposes and at the same time see if our results match the Micrometals suggestions.

The core itself is an E core block assembly. It is meant to be used with the respective I core to close the magnetic loop, or if necessary, another E block if the number of turns we needed were to high.

| Description | E core Block Assembly |
|---|---|
| Part Number: | EBMS-300125030-060 |

Revision: 6/20/2023




| | | |
|---|---|---|
| Magnetic Dimensions | $A_e$ - Eff. Mag. Cross Section | 30 cm² |
| | $L_e$ - Eff. Mag. Path Length | 60 cm |
| | $V_e$ - Eff. Core Volume | 1,800 cm³ |
| | WA - Nom. Window Area | 75.0 cm² |
| | sa - Surface Area | 2,180 cm² |
| | mlt - mean length per turn | 46.0 cm |
| Inductance | $\mu_i$(reference) | 60 |
| | $A_L$ value (reference) | 440 nH/N² |
| | Test Winding | N/A |
| | Frequency | N/A |
| | Voltage on Agilent 4284A | N/A |
| | $A_L$ tolerance | N/A |
| Core Loss | Core Loss(mW/cm³)= $\frac{f}{\frac{a}{Bpk^{3}}+\frac{b}{Bpk^{2.5}}+\frac{c}{Bpk^{1.65}}}+d\cdot Bpk^{2}\cdot f^{2}$ | |
| | where $B_{pk}$ expressed in gauss, $f$ expressed in hertz, and: | |
| | *a=7.89E+09, b=7.11E+08, c=8.98E+06, d=2.85E-14* | |
| | $B_{pk}$ | 1000 G |
| | frequency | 50 kHz |
| | Core Loss (nominal) | 323 mW/cm³ |
| | Core Loss (maximum) | 372 mW/cm³ |
| DC Saturation | $\%\mu_i = \frac{1}{a+b\cdot H^{c}}+d$ | |
| | where H expressed in oersteds, and: | |
| | *a=0.01, b=4.47E-06, c=1.74, d=0.00* | |
| | $H_{DC}$ | 100 Oe |
| | Percent Initial Perm(nom.) | 42.2% |
| | Percent Initial Perm(min.) | 34.7% |

*Figure 69 Inductance core datasheet*

The datasheet provides us with useful data and graphs to compute the values needed for checking if the core is valid or not. One of the most important parameters for a magnetic core is the saturation magnetic field density. Micrometals provides this value in the form of the DC saturation magnetic field intensity and the equivalent reduced permittivity.

To compute the saturation magnetic field density, we can use the following equation:

$$B_{max} = H_{max} \cdot \%_{init} \cdot \mu_{Fe} \cdot \mu_0$$

*( 19 )*

We must keep into account that the value provided for the saturation magnetic field intensity is given in Oesterds and we need it in the SI (A/m). In our case, the $B_{max}$ value is 0.2532 T.

With this value we can now compute the aproximate maximum inductance we could get out of it

$$L_{max} < \frac{n \cdot S \cdot l_{Fe}}{\mu_0 \mu_e} \cdot \left(\frac{B_{max}}{I_{max}}\right)^2$$

*( 20 )*

Where n is the number of cores that we want to use in parallel (1), S is the effective magnetic cross surface and $l_{Fe}$ is the effective magnetic path length. This gives us a maximum inductance of around 46uH for 280A of current with only one core. Note that this only approximate because the $\mu_e$ value is not linear close to the saturation point.

We can actually see this non linearity appear if we take the data from the datasheet in form of graphs and plot the magnetic flux density (B) and the magnetic field strength (H). In the image below we can tell how up to 0.2T of flux density the behavior is quite linear, but if we keep increasing the magnetic intensity we can no longer continue to increase B in the same rate as we did. For this core material micrometals allows us to work close to the saturation point. However, this is not typically the case and doing so could end up causing very high losses on the core.

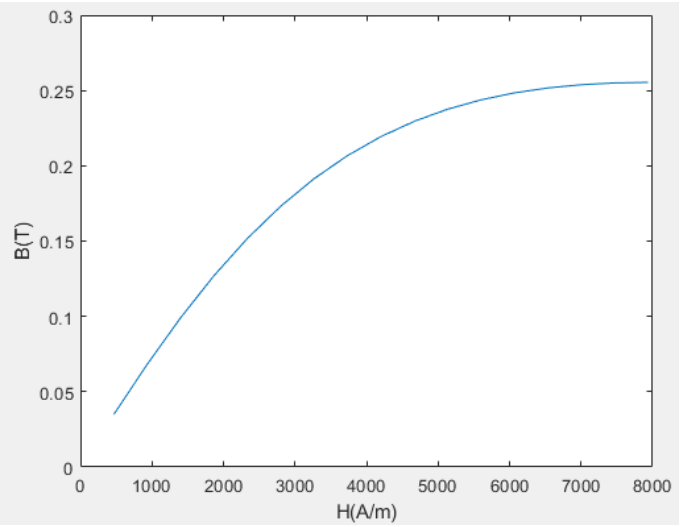



*Figure 70 B-H curve for inductor core selected*

Now we need to check how many turns we can iterate through this calculation with the help of the table provided in the datasheet or we can take the data from it and do so with Matlab. In this case we will plot the inductance and the maximum flux density with respect to the number of turns. This will allow us to rapidly see if, for the inductance that we want to obtain the core material gets saturated and for what amount of tuns we obtain this inductance.

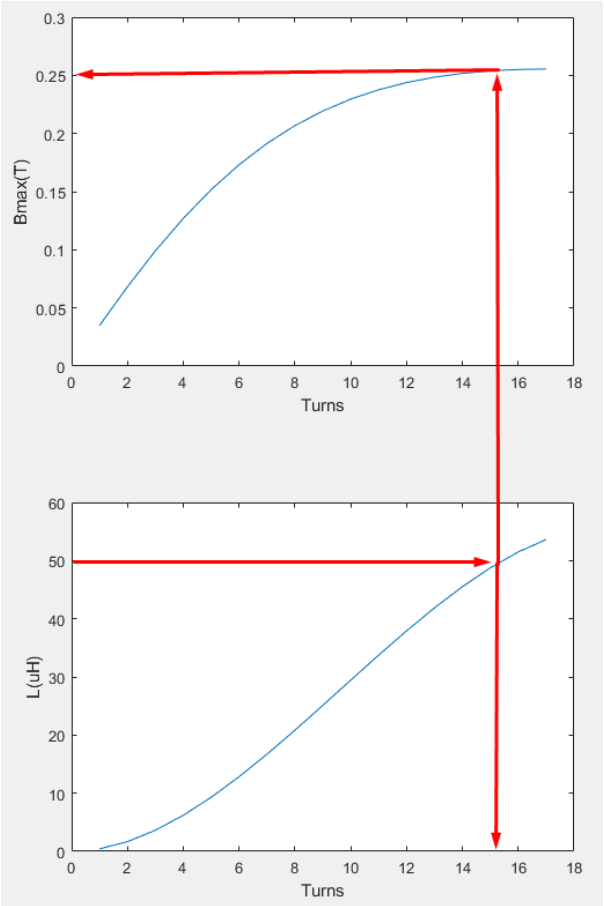



*Figure 71 Turns to Bmax and Inductance diagram*

As we can see we are at the limit of the saturation point of the material, but we are able to obtain the desired 50uH of inductance with 15 turns. There's a couple of things that we must check

before we can confirm that we can use this core. The first is to check what conductor size we need. In this case Micrometals also provides with a reference of what cable to use. They recommend litz AWG 14 wire with 50 strands per turn. This is equivalent to 50 wires of 1.63mm in diameter each and with a cross section of $2.08\ mm^2$ per wire. The total cross section of the wire bundle will be:

$$A_{total} = 50 \cdot 2.08mm^2 = 104mm^2$$

*( 21 )*

The mean length per turn of the winding is 46cm (data given in the datasheet), so the total length of the wire bundle will be 690cm. With these values we can compute the resistance of the wire bundle using the following equation:

$$R = \rho \cdot \frac{L_{total}}{A_{total}} = 1.94 \cdot 10^{-8}\ [\Omega \cdot m] \cdot \frac{0.69\ [m]}{0.104 \cdot 10^{-3}[m^2]} = 1.29\ [m\Omega]$$

*( 22 )*

Note that we are considering the resistivity of copper at 60 Cº. This is close enough to the value provided by Micrometals of $1.32\ [m\Omega]$. With the resistance and the known maximum current, we can calculate the losses in the copper conductors. We will not consider the skin effect or the proximity effect due to the use of Litz wire.

The losses can be calculated like:

$$P_{copper} = I_{max}^2 \cdot R = 280^2[A] \cdot 1.32[m\Omega] = 104\ [W]$$

*( 23 )*

We must also calculate if the turns we want to use are physically capable of fitting in the core. In our case the winding window area is $75cm^2$ and we need 15 turns of 50 cables of 1.63mm diameter. We cannot use the direct sum of the cross-sectional area because of the stacking factor for the cylindrical cables. The maximum packing factor for cylindrical cables is 90.7%.

$$A_{cables} = 15 \cdot 104 \cdot 0.907\ [mm^2] = 14.15\ [cm^2]$$

*( 24 )*

Now that we know that the cables fit, we can calculate the losses on the core. To do so we will make use of the core loss equation provided by the datasheet.

$$P_{loss_{core}}[W] = \frac{80000[Hz]}{\frac{7.89 \cdot 10^9}{B_{pk}^3} + \frac{7.11 \cdot 10^8}{B_{pk}^{2.3}} + \frac{8.98 \cdot 10^6}{Bpk^{1.65}}} + 2.85 \cdot 10^{-14} \cdot B_{pk}^2 \cdot 80000^2 \cdot 1.8 = \ 60[W]$$

*( 25 )*

Where $B_{pk} = 220\ [G]$. Now we have all terms calculated for our inductance.

# SWITCH SIZING

## MOSFET SIZING

Shifting focus to the selection and characterization of switches and reverse current limiting diodes, it's crucial to establish the operational parameters that these components must handle, particularly in terms of current flow and reverse voltage. Given the system's adoption of high switching frequencies, which facilitates tighter component sizing and improved efficiency, the choice of Silicon Carbide (SiC) technology emerges as a compelling option.

Silicon Carbide technology stands out for its superior performance characteristics in high-frequency power electronics applications. SiC components, including switches and diodes, offer exceptional thermal conductivity, high-temperature resilience, and increased energy efficiency compared to traditional silicon-based components. These attributes make SiC technology particularly suitable for handling the increased demands of high switching frequencies, including the ability to withstand higher reverse voltages and efficiently conduct the anticipated current levels.

The decision to utilize SiC components necessitates a careful analysis of the system's electrical requirements. This includes determining the maximum current that the switches and diodes will need to conduct, as well as the peak reverse voltage they must tolerate. These parameters are critical for ensuring that the chosen components can operate reliably under the system's typical and extreme conditions, without succumbing to thermal or electrical overstress. We will proceed to simulate and display both the current on each branch of the CSI and the reverse blocking voltage of both the switch and the diode:

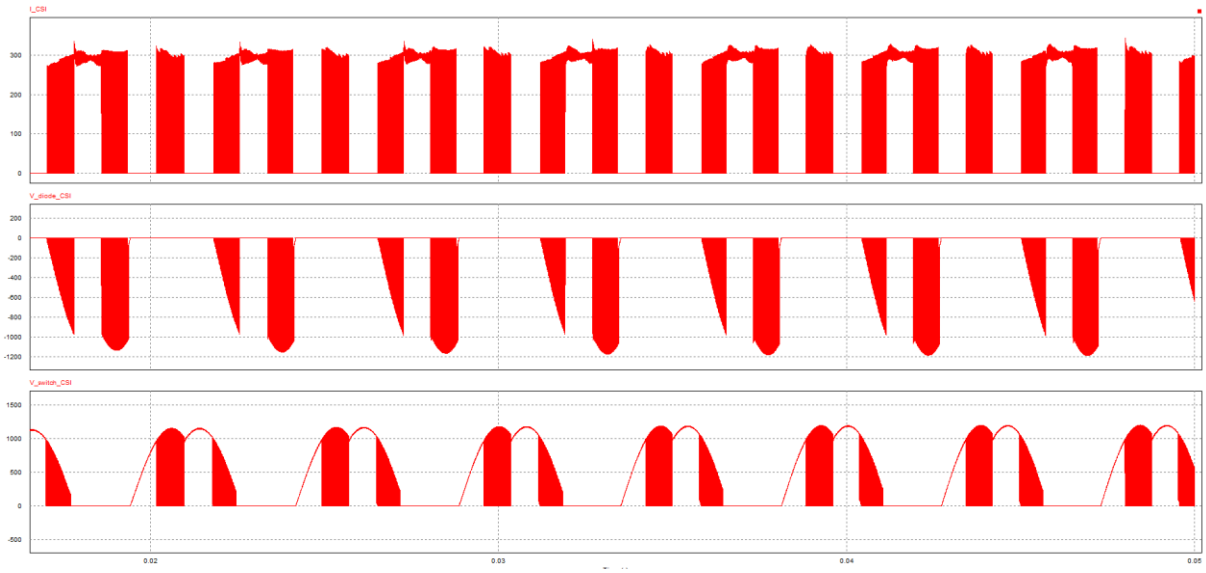



*Figure 72 Switch characterization parameters*

From these simulations we can tell that the maximum repeated current through the branch is 310 A and the maximum reverse voltage that both the switch and the diode have to withstand is around the 1200V mark.

With this values in mind we can use the catalog of known brands, such as Wolfspeed to choose the components that suit our needs. For the switches we will opt for the CAB400M12XM3 SiC Power Half-Bridge Module. This module can withstand up to 1200V of Vds and up to 317A at a temperature of 90 ºC, making it a very solid candidate.

We could also have chosen a different path and instead of choosing a power half-bridge we could have chosen a single mosfet, moreover, we could have chosen multiple mosfets such that their combination in parallel was able to withstand the current load, making sure that every one of them could achieve the reverse blocking voltage required. This however, would need to be tested to ensure synchronization between the switching of the parallel mosfets, as any deviation will result in one of them suffering from overcurrent.

## DIODE SIZING

In selecting reverse blocking current diodes to complement the switching MOSFETs, the criteria are stringent, requiring the capability to withstand a reverse blocking voltage of 1200V and manage an RMS current of around 170A. Given the high demands placed on these components, sourcing a single diode that meets these specifications can be challenging. To navigate this difficulty, a practical solution involves employing multiple diodes in parallel. This strategy ensures that the RMS current load is evenly distributed across the diodes, alleviating the stress on any single component and enhancing the overall system reliability.

The approach of paralleling diodes necessitates finding diodes each capable of withstanding around 50A. By configuring four or more such diodes in parallel for each branch, the system can achieve the required 170A RMS current capacity while maintaining the 1200V reverse blocking voltage criterion. This method not only solves the challenge of meeting the high current and voltage specifications but also introduces redundancy, improving the system's fault tolerance.

Opting to use multiple diodes in parallel requires careful consideration of their thermal management and equal current sharing. Diodes with closely matched characteristics should be selected to ensure uniform current distribution and to prevent thermal runaway, where a hotter diode carries more current and becomes even hotter. Moreover, this approach may influence the design of the PCB layout or the choice of heat sinking solutions, as effective heat dissipation becomes crucial when multiple high-power diodes are used in close proximity.

One option for these conditions is the DH60-14A from IXYS. This model can withstand 1400V reverse voltage and 60A of RMS forward current. Our suggestion will be to set 4 of this model diodes in parallel to achieve the necessary current capabilities. This model is also an affordable option that can serve to reduce the overall cost of the inverter.

# SUMMARY

In this comprehensive document, we have successfully achieved the overarching goals of dissecting and understanding the operational principles of a current source inverter (CSI), a crucial component in advanced power conversion systems. The study began with an exploration of the foundational mechanisms that are the bases on how the CSI's works, setting the stage for the subsequent design and implementation processes.

A key aspect of our project involved the development and integration of a DC-DC current-controlled buck converter. This converter served as a pre-stage, functioning effectively as a virtual current source. Its role was critical in ensuring a stable and reliable supply of current for the subsequent stages of the inverter system, acting as the key current source for the CSI.

Further, we adopted and implemented the current Space Vector Pulse Width Modulation (SVPWM) technique. This modulation strategy was instrumental in achieving PWM-modulated three-phase current sinusoidal signals. The use of SVPWM not only facilitated the generation of high-fidelity sinusoidal currents but also addressed several challenges typically associated with PWM systems. The resolution of these issues was vital for the smooth operation of the inverter and its valid functionality in non-ideal situations.

Additionally, an extensive study on the values of the passive components necessary for the system’s implementation was conducted. This involved a meticulous selection process where each component was chosen based on its performance characteristics and compatibility with the overall system design. The selection process was informed by both theoretical calculations and simulation models.

Real-life components were then sourced and integrated into the design to validate the theoretical and simulation-based findings. This practical implementation phase is crucial in transitioning the project from a conceptual stage to a functional prototype, thereby demonstrating the viability and effectiveness of the designed inverter in real-world applications.

The culmination of this project has not only resulted in a working design of a current source inverter but has also expanded our understanding of how such inverters operate. The knowledge acquired through this venture is of high value, providing clear insights into the intricacies of CSI technology and its applications. The successful completion of these goals underscores the efficacy of our approach and the potential of our design to contribute to advancements in power conversion technologies. This document serves as both a detailed account of our journey and a resource for future endeavors in the field of current source inverter design and inverter technology in general.

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