UNIVERSITAT POLITÈCNICA DE VALÈNCIA

DEPARTAMENTO DE INGENIERÍA ELECTRÓNICA

UNIVERSITAT POLITÈCNICA DE VALÈNCIA

Dept. of Electronic Engineering

Development of a LoRa-based communications payload for CubeSat

Master's Thesis

Master's Degree in Electronic Systems Engineering

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ACADEMIC YEAR: 2023/2024

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Cite this work:

```bibtex
@phdthesis{dpmj-master-thesis-2024,
  author = "Juan Del Pino Mena and Jorge Daniel Martínez Pérez and Vicente Enrique Boria Esbert",
  title = "Development of a LoRa-based communications payload for CubeSat",
  school = "Universitat Politècnica de València",
  year = "2024",
  month = "September",
  address = "Camí de Vera, s/n, 46022 València, Valencia, Spain",
  type = "Master's Thesis"
}
```


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Juan Del Pino Mena

Juan Del Pino Mena was born in 2000 in Arriate, Málaga, Spain. He graduated with a Bsc in Telecommunications Engineering from the University of Granada (UGR) in 2022. There he was a member of the GranaSat electronics group and participated in the technical support team for the Esero CanSat Spain 2022 competition. His bachelor's thesis was awarded as the best telecom. bachelor's thesis in Andalucía in 2022 and as the best telecom. bachelor's thesis in the electronic systems category in Spain in 2023. He is currently studying for a double Masters in Telecommunications Engineering and Electronic Systems Engineering at the Polytechnic University of Valencia (UPV). This thesis completes the latter. Since 2022, he has held the position of Hardware and Payload Engineer at Pluton UPV, a student team developing a CubeSat for which the payload developed in this thesis is intended. Since 2024, he is also a researcher at the Microwave Applications Group (GAM/MAG) of the Institute of Telecommunications and Multimedia Applications (iTEAM-UPV).

Jorge Daniel Martínez Pérez

Jorge Daniel Martínez was born in Murcia, Spain, in 1979. He received the Telecommunication Engineering degree and the PhD in Electrical Engineering from the Universitat Politècnica de València (UPV) in 2002 and 2008, respectively. In 2002, he joined the Department of Electronic Engineering. In 2007, he was a visiting researcher at XLIM CNRS-Université de Limoges, France, working on the design and fabrication of RF MEMS components at MINACOM group. He was appointed as an Assistant Professor in UPV in 2009 and was promoted to an Associate Professor in 2012. He is currently the Deputy Director of the Department of Electronic Engineering and a Member of the I3M Research Institute at UPV, where he is the Head of the Laboratory for High Frequency Circuits (LCAF). His current research interests are focused on reconfigurable microwave components, passive devices in planar and SIW technologies, and multi-layer fabrication for microwave and millimeter-wave. He has authored or co-authored more than 80 publications in journals and international conferences and he serves as an Associate Editor for IEEE Microwave and Wireless Components Letters, and reviewer for the IEEE Transactions on Microwave Theory and Techniques and IEEE Microwave and Wireless Components Letters.

Vicente Enrique Boria Esbert

Vicente E. Boria Esbert was born in Valencia, Spain, in 1970. He received the Degree in Telecommunications and PhD in Telecommunications from the Universitat Politécnica de València (UPV) in 1993 and 1997, respectively. In 1993, he joined the Communications Department, where he has been a Full Professor since 2003. In 1995 and 1996 he was a trainee in the European Space Research and Technology Centre (ESTEC-ESA). He has authored or coauthored ten chapters in technical textbooks, 180 articles in international journals, and over 200 papers in international conference proceedings. His current research interests include the analysis and automated design of passive components, left-handed and periodic structures, and the simulation and measurement of power effects in passive waveguide systems. Dr. Boria Esbert is a member of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S), the IEEE Antennas and Propagation Society (IEEE AP-S), the European Microwave Association (EuMA) and the Technical Committees of the IEEE-MTT International Microwave Symposium and the European Microwave Conference. He acts as a regular reviewer of the most relevant IEEE and IET technical journals in his areas of interest. He was an Associate Editor of IEEE Microwave and Wireless Components Letters and Electronics Letters (IET). He also serves as a Subject Editor (Microwaves) for Electronics Letters (IET) and as an Editorial Board Member for International Journal of RF and Microwave Computer-Aided Engineering.

Development of a LoRa-based communications payload for CubeSat

Keywords:

CubeSat, EDP, Engineering Design Process, EGSE, Electrical Ground Support Equipment, Embedded System, Estigia, Gateway, IoT, Internet of Things, LEO, Low-Earth Orbit, Link Budget, LoRa, Mixed-Signal, Nano-Satellite, PCB, Printed Circuit Board, Payload, Pluton UPV, RF, Radio-Frequency, Simulation, Space Communications, Transceiver

Abstract:

This master's thesis covers the development of a communications payload suitable for space, to be embarked on a CubeSat type nano-satellite flying in Low-Earth Orbit (LEO). The design integrates LoRa transceivers, proving the capabilities of this technology for long range, low power and low cost communications.

LoRa is a Low-Power Wide-Area Network (LPWAN) technology oriented to the Internet of Things (IoT). The LoRa structure can be point-to-point or star. In the star topology, the hub acts as a gateway to servers on the Internet.

This thesis has been developed as part of *Estigia*, the first satellite of Pluton UPV, a CubeSat team of students of the Universitat Politècnica de València (UPV). The project has counted with the collaboration of the Microwave Applications Group (MAG), member of the Institute of Telecommunications and Multimedia Applications (iTEAM-UPV).

The objective of the *Estigia* mission is to enable users on the ground to directly communicate with a chatbot running on the CubeSat, using their smartphones and low-cost LoRa-based mini-Ground Stations (GS). The purpose of this master's thesis is to implement the necessary communications hardware on the satellite.

This project is divided into three PCBs: a module, a motherboard labeled *Carrier*, and an Electrical Ground Support Equipment (EGSE) auxiliary board.

The payload consists of two modules and the Carrier. The modules adhere to the mPCIe form factor and act as LoRa gateway. The Carrier follows the CubeSat-PC/104 and serves as the electrical and mechanical interface with the rest of the satellite.

The EGSE provides a test hardware for the payload, emulating the interaction with the CubeSat On-Board Computer (OBC), Electrical Power System (EPS) and the second payload of the CubeSat. At the same time, it acts as a LoRa end device to test the performance of the communications system.

The working methodology is based on the Engineering Design Process (EDP). This master's thesis represents the first phase of the project, planned to be continued in a second master's thesis. This document addresses the conception of the devices, through their specification, design and implementation in CAD and EDA tools, while taking into account manufacturing and verification considerations.

Prior to the design of the electronics, a stage of analysis and simulations of the communications system is carried out, focused on the evaluation of the Earth-satellite channel at the link budget level, as well as a review of the current international regulations.

The ultimate aim of this project is the demonstration by the author of the multidisciplinary knowledge, the capacity for analysis and synthesis inherent to engineering, as well as the documentation of the entire process.

Desarrollo de una payload de comunicaciones LoRa para CubeSat

Palabras clave:

CubeSat, EDP, Engineering Design Process, EGSE, Electrical Ground Support Equipment, Embedded System, Estigia, Gateway, IoT, Internet of Things, LEO, Low-Earth Orbit, Link Budget, LoRa, Mixed-Signal, Nano-Satellite, PCB, Printed Circuit Board, Payload, Pluton UPV, RF, Radio-Frequency, Simulation, Space Communications, Transceiver

Resumen:

El presente Trabajo de Fin de Máster (TFM) abarca el desarrollo de una carga útil (*payload*) de comunicaciones adecuada para espacio, con el objetivo de ser embarcada en un nano-satélite tipo CubeSat que vuela en órbita baja (LEO). El diseño pretende demostrar la eficacia de LoRa para las comunicaciones de largo alcance, baja potencia y bajo coste.

LoRa es una tecnología *Low-Power Wide-Area Network* (LPWAN) orientada al *Internet of Things* (IoT). La estructura de LoRa puede ser punto a punto o en estrella. En la topología en estrella, el concentrador ejerce la función de *gateway* hacia Internet.

Este TFM se ha desarrollado como parte de *Estigia*, el primer satélite de Pluton UPV, un equipo de estudiantes de la Universitat Politècnica de València (UPV). El proyecto ha contado con la colaboración del Grupo de Aplicaciones de las Microondas (GAM), miembro del Instituto de Telecomunicaciones y Aplicaciones Multimedia (iTEAM-UPV).

El objetivo de la misión *Estigia* es que los usuarios en tierra puedan comunicarse directamente con un *chatbot* ejecutándose en el CubeSat, usando para ello sus *smartphones* y mini-estaciones terrenas de bajo coste basadas en LoRa. El fin de este TFM es implementar el *hardware* de comunicaciones necesario en el satélite.

Este proyecto está dividido en tres PCBs: un módulo, una placa madre llamada *Carrier* y una placa auxiliar denominada *Electrical Ground Support Equipment* (EGSE).

La *Payload* está compuesta por dos módulos y el *Carrier*. Los módulos tienen factor de forma mPCIe y sirven de *gateway* LoRa, mientras que el *Carrier* sigue el estándar CubeSat-PC/104 y ejerce de interfaz eléctrica y mecánica con el resto del satélite.

El EGSE proporciona un *hardware* de testeo para la *payload*, emulando su interacción con el *On-Board Computer* (OBC), el *Electrical Power System* (EPS) y la otra *payload* integrada en el CubeSat. A su vez, ejerce de *end device* LoRa para comprobar el desempeño del sistema de comunicaciones.

La metodología de trabajo empleada se basa en el *Engineering Desing Process* (EDP). Este TFM representa la primera fase del proyecto, previsto para ser continuado en un segundo trabajo de fin de máster. En este documento se aborda la concepción de los dispositivos, su especificación y diseño e implementación en herramientas CAD y EDA, teniendo en cuenta consideraciones de fabricación y verificación.

Previo al diseño de la electrónica se realiza una etapa de análisis y simulaciones del sistema de comunicaciones, centrada en la evaluación del canal Tierra-satélite a nivel de *link budget*; así como un repaso a la normativa internacional vigente.

Este proyecto tiene como fin último la demostración de los conocimientos multidisciplinares, la capacidad de análisis y síntesis propios de la ingeniería, y la documentación de todo el proceso.

Desenvolupament d'una payload de comunicacions LoRa per a CubeSat

Paraules clau:

CubeSat, EDP, Engineering Design Process, EGSE, Electrical Ground Support Equipment, Embedded System, Estigia, Gateway, IoT, Internet of Things, LEO, Low-Earth Orbit, Link Budget, LoRa, Mixed-Signal, Nano-Satellite, PCB, Printed Circuit Board, Payload, Pluton UPV, RF, Radio-Frequency, Simulation, Space Communications, Transceiver

Resum:

El present Treball de Fi de Màster (TFM) abasta el desenvolupament d'una *payload* de comunicacions adequada per a ús espacial, amb l'objectiu de ser embarcada en un nanosatèl·lit tipus CubeSat que vola en òrbita baixa (LEO). El disseny pretén demostrar l'eficàcia de LoRa per a les comunicacions de llarg abast, baixa potència i cost reduït.

LoRa és una tecnologia *Low-Power Wide-Area Network* (LPWAN) orientada al *Internet of Things* (IoT). L'estructura de LoRa pot ser punt a punt o en estrella. En la topologia en estrella, el concentrador exercix la funció de *gateway* cap a servidors en Internet.

Aquest TFM s'ha desenvolupat com a part d'*Estigia*, el primer satèl·lit de Pluton UPV, un equip d'estudiants de la Universitat Politècnica de València (UPV). El projecte ha comptat amb la col·laboració del Grup d'Aplicacions de les Microones (GAM), membre de l'Institut de Telecomunicacions i Aplicacions Multimèdia (iTEAM-UPV).

L'objectiu de la missió *Estigia* és que els usuaris en terra puguen comunicar-se directament amb un *chatbot* executant-se al CubeSat, emprant per a això els seus telèfons intel·ligents i mini-estacions terrestres de baix cost basades en LoRa. La finalitat d'aquest TFM és implementar el maquinari de comunicacions necessari en el satèl·lit.

Aquest projecte està dividit en tres PCBs: un mòdul, una placa mare denominada *Carrier* i una placa auxiliar de *Electrical Ground Support Equipment* (EGSE).

La *payload* està formada per dos mòduls i el *Carrier*. Els mòduls tenen factor de forma mPCIe i servixen de *gateway* LoRa, mentres que el *Carrier* seguix l'estàndard CubeSat-PC/104 i exercix d'interfície elèctrica i mecànica amb la resta del satèl·lit.

L'EGSE proporciona un maquinari de test per a la *payload*, emulant la interacció amb el *On-Board Computer* (OBC) i *Electrical Power System* (EPS)i l'altra *payload* integrada en el CubeSat. A més, exercix de *end device* LoRa per a comprovar l'acompliment del sistema de comunicacions.

La metodologia de treball emprada es basa en el *Engineering Desing Process* (EDP). Este TFM representa la primera fase del projecte, previst per a ser continuat en un segon treball de fi de màster. L'est document s'aborda la concepció dels dispositius, la seua especificació i disseny i implementació en ferramentes CAD i EDA, i tenint en compte consideracions de fabricació i verificació.

Previ al disseny de l'electrònica es realitza una etapa d'anàlisi i simulacions del sistema de comunicacions, centrada en l'avaluació del canal Terra-satèl·lit a nivell de *link budget*; així com un repàs a la normativa internacional vigent.

Este projecte té com a fi última la demostració per part de l'autor dels coneixements multidisciplinaris i la capacitat d'anàlisi i síntesi pròpia de l'enginyeria, així com la documentació de tot el procés.

Executive overview

The present Master's Thesis report titled "*Development of a LoRa-based communications payload for CubeSat*" develops in the text the following concepts, which are duly justified and discussed, focusing on the field of Electronic Systems Engineering:

Resumen ejecutivo

La presente memoria del Trabajo de Fin de Máster titulado "*Desarrollo de una payload de comunicaciones LoRa para CubeSat*" desarrolla en el texto los siguientes conceptos, debidamente justificados y discutidos, centrados en el ámbito de la Ingeniería en Sistemas Electrónicos:

Concept (ABET)	**Concepto (traducción)**	**Complies? (Y/N)**	**Where? (sections)**
1. Identify:	**1. Identificar:**		
1.1. Problem statement and opportunity	1.1. Planteamiento del problema y oportunidad	**Yes**	chapter 1, section 1.1, section 1.2
1.2. Constraints (standards, codes, needs, requirements & specifications)	1.2. Toma en consideración de los condicionantes (normas técnicas y regulación, necesidades, requisitos y especificaciones)	**Yes**	chapter 2, section 2.1, section 2.2, section 2.3, chapter 3, section 3.1, section 3.2
1.3. Setting of goals	1.3. Establecimiento de objetivos	**Yes**	chapter 1, section 1.1, section 1.4, section 1.3
2. Formulate:	**2. Formular:**		
2.1. Creative solution generation (analysis)	2.1. Generación de soluciones creativas (análisis)	**Yes**	chapter 2, section 2.4, chapter 3, section 3.1, section 3.2, section 3.3, chapter 4
2.2. Evaluation of multiple solutions and decision-making (synthesis)	2.2. Evaluación de múltiples soluciones y toma de decisiones (síntesis)	**Yes**	chapter 3, section 3.3, section 3.4, chapter 4
3. Solve:	**3. Resolver:**		
3.1. Fulfilment of goals	3.1. Evaluación del cumplimiento de objetivos	**Yes**	chapter 5, section 5.1
3.2. Overall impact and significance (contributions and practical recommendations)	3.2. Evaluación del impacto global y alcance (contribuciones y recomendaciones prácticas)	**Yes**	chapter 5, section 5.1, section 5.2, section 5.3, Appendix A

Agradecimientos

Este año ha sido para mí el que más me ha marcado personal y profesionalmente hasta ahora. He madurado mucho en muchos aspectos. Cada día me conozco un poco mejor. El mérito no es sólo mío, lo comparto con las geniales personas que me acompañan.

A mi hermana María y a mis padres Maru y Juan por imbuirme con su constante apoyo, cariño y risas que sé que siempre tendré.

A los viejos amigos, por todos los momentos que hemos pasado. Ojalá nos viéramos más a menudo. A los nuevos amigos, por recibirme en sus vidas como si los conociera desde siempre. A las personas que más tiempo me han aguantado este año en contra de su voluntad: Jaume y David. Devolvedme mis tuppers y poned el lavavajillas.

Gracias a mis compañeros del Grupo de Aplicaciones de las Microondas por su ayuda antes y durante el desarrollo de este proyecto, y por los deliciosos esmorzarets.

Gracias a todos los compañeros de Pluton UPV, sin su esfuerzo e iniciativa no existiría la misión. Formar parte de este grupo es una experiencia única. Gracias por la responsabilidad y confianza depositada en mí.

Muchas gracias a mis tutores Jorge Daniel Martínez y Vicente Boria, y también a María Bayarri y Ana Vidal por sus inestimables consejos. Su extraordinario trabajo y dedicación me han inspirado a llegar muy lejos.

Debo agradecer también el trabajo altruista de todas las personas, organizaciones y comunidades que hacen posible el acceso gratuito y libre a la cultura, la ciencia y la tecnología en Internet. Sin ellos el saber sería un lujo, y este trabajo irrealizable.

Muchas gracias a todos.

Me quiero asegurar
que mi sombrero está bien roto
y los rayos pueden entrar en mi cabeza

Te quiero conquistar
con el suave viento gratis y fresco
de mi abanico de cristal

Veneno

Kiko Veneno, Antonio Moreno, Ricardo Pachón,
Rafael Amador y Raimundo Amador

"*Los Delincuentes*", en el álbum *"Veneno"*, 1977

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Glossary

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A

ADCS Attitude Determination and Control System.
AI Artificial Intelligence.
AWGN Additie White Gaussian Noise.

B

BER Bit Error Rate.
BOM Bill Of Materials.
BPF Band Pass Filter.

C

CAD Computer-Aided Design.
CAN Controller Area Network.
CDS CubeSat Design Specification.
ChatBot A software designed to simulate human conversation through text or voice interactions.
CNR Carrier-to-Noise Ratio.
Conflict resource Natural resources whose systematic exploitation and trade in a context of conflict contribute to, benefit from or result in violations of human rights and international law.
COTS Commercial Off-The-Shelf.
CPU Central Processing Unit.
CR Coding Rate.
CRC Cyclic Redundancy Check.
CSKB CubeSat Kit Bus.
CSS Chirp Spread Spectrum.
CubeSat A type of Micro-Satellite or Nano-Satellite, composed of one or more standard cubic units of 10 cm side.

D

DRC Design Rule Check.

E

ECSS European Cooperation for Space Standardization.
EDA Electronic Design Automation.
EDP Engineering Desing Process
EGSE Electrical Ground Support Equipment.
Embedded System Electronic systems whose resources are limited and are sized for an specialized and restricted application.
EMC Electro-Magnetic Compatibility. The capability of electronic systems to operate in their intended electromagnetic environment within a defined margin of safety without suffering or causing unacceptable degradation as a result of EMI.
EMI Electro-Magnetic Interference. The process by disruptive electromagnetic energy is transmitted from one electronic device to another, via radiated or conducted paths.
ENIG Electroless Nickel Immersion Gold.
EPS Electrical Power System.
ESA European Space Agency.
ESD Electrostatic discharge.
ESR Equivalent Series Resistance.
ETSIT Escuela Técnica Superior de Ingeniería de Telecomunicación.

F

FEC Forward Error Correction
FFT Fast Fourier Transform
Form factor The size and shape of a PCB. The chassis, mounting hardware and standards are taken into account for defining a form factor.
FPU Floating Point Unit.
FR-4 Flame Retardant 4. Fiberglass-reinforced self-extinguishing epoxy laminate. Used as an insulator for PCBs for its fire resistance, nearly zero water absorption and high mechanical strength
FSCM Frequency Shift Chirp Modulation
FSPL Free Space Path Losses

G

Gateway A network device that acts as a bridge between different networks and provide interoperability between different network architectures.
GNSS Global Navigation Satellite System.
GPIO General-Purpose Input/Output.
GS Ground Station

H

HAL Hardware Abstraction Layer.

I

I2C Inter-Integrated Circuit
IC Integrated Circuits
IoT Internet of Things.
ISM Industrial, Scientific and Medical.
ITU International Telecommunication Union
ITU-R ITU Radiocommunication Sector
ITU/RR ITU Radio Regulations

J

JAXA Japan Aerospace Exploration Agency.
JTAG Joint Test Action Group.

L

LDO Low-DropOut regulator.

LDRO Low Data Rate Optimization.
LEO Low-Earth Orbit.
Link Budget A feasibility analysis of a communication link to evaluate reliable data transmission between two points. It accounts for all power gains and losses from the transmitter, through the medium, to the receiver.
LNA Low-Noise Amplifier.
LoRa Long Range. A proprietary LPWAN technology designed by Semtech Corp. for wireless communication over long distances.
LoRaWAN A communication protocol and system architecture designed by Semtech Corp. for IoT devices built on top of LoRa.
LoS Line of Sight.
LPF Low Pass Filter.
LPWAN Low-Power Wide-Area Network.

M

MAC Medium Access Control.
MCU Micro-controller unit.
Micro-controller A standalone computer which contains one or more CPU cores along with memory and peripherals on a single IC, meant for embedded devices.
Micro-Satellite A type of small satellite with a mass ranging from 10 to 100 kg.
Microwaves The name given to electromagnetic waves with frequencies between 300 MHz and 300 GHz.
Mixed-Signal The coexistence of both analog and digital signals in an electronic system.
MMCX Micro-Miniature Coaxial.
mPCIe Mini-PCI-express.

N

Nano-Satellite A type of small satellite with a mass ranging from 1 to 10 kg.
NASA National Aeronautics and Space Administration.
NC Not Connected.
NDA Non-Disclosure Agreement.
NF Noise Figure.

O

OBC On-Board Computer.
OC Over-current.
Open Source An initiative in which the developer licenses a software or resource to grant users the rights to use, change, make derived works and freely distribute the work and its source.
OV Over-voltage.

P

PA Power Amplifier.
Payload The primary mission-specific instruments or experiments that the satellite is designed to carry and operate in space.
PC/104 A Form factor for stackable and modular printed circuit boards for embedded systems.
PCB Printed Circuit Board. A rugged boards built on a dielectric substrate used to provide mechanical support and electrical connection between the components of a circuit.
PCI Peripheral Component Interconnect.
PCIe PCI-Express.
PFD Power Flux Density.
PG Power Good.
Pluton UPV A multidisciplinary project of students from the UPV whose objective is the design, assembly, validation and testing of a CubeSat.

R

RBF Remove Before Flight.
RF Radio-Frequency.
RoHS Restriction of Hazardous Substances.
Roscosmos Russian Federal Space Agency.

S

SDG Sustainable Development Goals.
SF Spreading Factor.
SFD Start Frame Delimiter.
SKU Stock Keeping Unit.
SMA Sub-Miniature version A.
SNR Signal-to-Noise Ratio.
SPI Serial Peripheral Interface.
STEM Science, Technology, Engineering, and Mathematics.
SWD Serial Peripheral Interface.
Switching noise The noise generated during the switching of electronic components. When current is drawn at high frequencies, the self-inductance of the package leads becomes significant, leading to voltage spikes and EMI.

T

TBD To Be Defined.
TBR To Be Resolved.
TCXO Temperature-Compensated XTAL.
Test Point A special pad used to inspect or inject signals on a circuit.
TLE Two-Line Element.
ToA Time-on-Air.
TT&C Telemetry, Tracking and teleCommand.

U

UART Universal Asynchronous Receiver-Transmitter.
UPV Universitat Politècnica de València.
USB Universal Serial Bus.

X

XPD Cross-Polarization Discrimination.
XTAL Crystal Oscillator.

Chapter 1

Introduction

This master's thesis represents the first part of a two-phase project. The complete project entails the comprehensive development of an engineering model for a space-grade, low-power, LoRa communications payload for a CubeSat-type nano-satellite, operating in low Earth orbit (LEO). LoRa is an acronym for *Long Range*, a proprietary protocol developed by Semtech for low-power, long-range wireless communications.

The complete project covers the full range of activities involved in the engineering design of an electronic device, including the initial conceptualization, the definition of requirements and specifications, the schematics and printed circuit board (PCB) design, fabrication, programming, testing, verification and validation. The project constitutes one of the two payloads to be deployed in *Estigia*, the first satellite of Pluton UPV, a CubeSat student team from the Universitat Politècnica de València (UPV) [1].

This first master's thesis in Electronic Systems Engineering addresses the definition of the problem, a review of the state of the art, an evaluation of the Earth-satellite radio link by simulation, the specification of a solution and its design process, while taking into consideration manufacturing and testing aspects. The development methodology adheres to the Engineering Design Process (EDP). The design of the devices, their functions and the development process are documented in detail in this report.

The second phase will be addressed in a master's thesis in Telecommunications Engineering. This thesis will address the topics of manufacturing, programming, testing, verification, validation, and potentially, further design iterations.

The engineering model designed in this thesis is modular. The aim of this strategy is to divide the development effort and facilitate the testing and debugging processes, design iterations and updates, introduce redundancy and fault tolerance.

The payload is divided into two distinct components: the *LoRa modules* and the *carrier*. The modules follow the mPCIe form factor [2]. They function as LoRa gateways, but instead of forwarding messages to the Internet, they are processed locally by the second payload of the satellite. Two modules are mounted in the carrier, for redundancy. The carrier serves as motherboard and provides electrical and mechanical support for the modules. It follows the *de facto* PC/104 standard [3], [4] and interfaces with the rest of the satellite via the CubeSat bus.

Additionally, an *electrical ground support equipment* (EGSE) auxiliary board has been designed to serve as a hardware testing platform for the payload.

The present master's thesis has been conducted with the help and funding of the Microwave Applications Group (MAG) [5], member of the Institute of Telecommunications and Multimedia Applications (iTEAM) of the Universitat Politècnica de València [6].

Figure 1.1 – Organizations that contributed to this thesis.

1

1.1 Motivation

This master's thesis aims to support the completion of Pluton UPV's *Estigia* mission by developing a LoRa communications payload as a direct-to-satellite narrowband IoT and LPWAN technology demonstrator.

From the perspective of Electronics Systems Engineering, this represents an opportunity to develop all the aspects of a space-grade electronic device from start to finish. A project of this magnitude necessitates a comprehensive understanding of telecommunications, electronics and printed circuit board design, as well as the regulations, standards and conventions that accompany the development of space electronics.

Moreover, this thesis will serve as a formative and professional experience for the author, with the incentive of being part of a student team and the possibility of establishing contacts with a range of companies and organizations across many sectors.

1.1.1 Pluton UPV and the Estigia mission

Pluton UPV is CubeSats team of students from the Universitat Politècnica de València (UPV). The project was established in May 2022 and currently comprises about 20 students from many engineering disciplines. The project is lead by Ana Vidal Pantaleoni and endorsed by Vicente Boria Esbert.

The goal of Pluton UPV is to participate in ESA *"Fly Your Satellite! Design Booster"*, a programme that aims to consolidate student CubeSats designs and provides manufacturing, integration, and validation support [7], [8]. Ultimately, Pluton UPV's goal is to train students in spacecraft development and inspire students to pursue careers in space, as well as to foster the space industry ecosystem within the university.

The team is currently in the early development stages of *Estigia*, its first satellite. *Estigia* is a two-unit (2 U) LEO CubeSat carrying an innovative payload consisting of an artificial intelligence (AI) chatbot and a direct-to-satellite LoRa communications system. The launch of *Estigia* is expected to take place in 2027. *Estigia*'s first payload is an AI executed locally at the spacecraft that will conduct text messaging conversations with users on Earth. The second payload enables this by implementing a LoRa Gateway to which users will connect using inexpensive, portable, non-traditional ground terminals called *mini-ground stations*. The chat interface will be provided by a smartphone application.

The primary objective of the mission is to demonstrate the feasibility of incorporating AI into a spacecraft and to evaluate the capabilities of LoRa for direct-to-satellite, narrowband Internet of Things (IoT) communication.

At Pluton UPV, the author belongs to the payload, hardware and communications departments. The responsibilities associated with the author's position include the supervision of the design of the in-house hardware and communications systems, the design of the electrical integration of all subsystems, as well as the development of the hardware for the LoRa communications payload, which is the subject of this master's thesis.

Figure 1.2 – Logos of the European Space Agency and the Fly Your Satellite! programme.

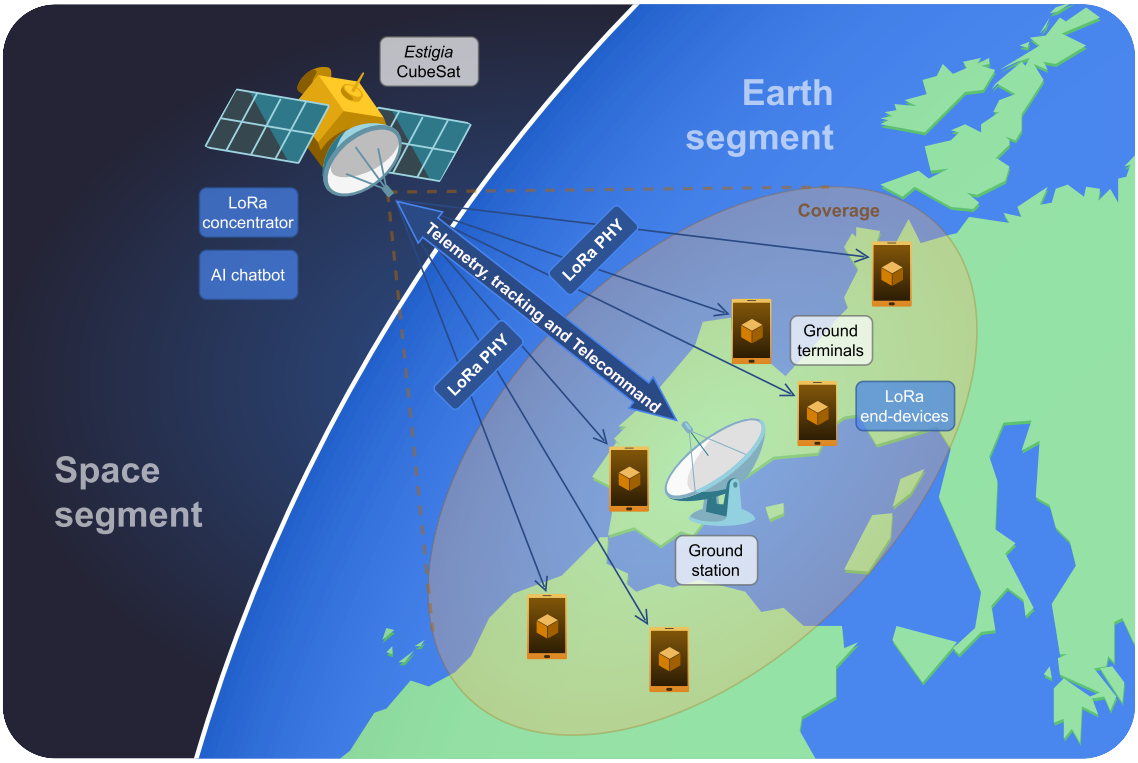


Figure 1.3 – Conceptual diagram of the Estigia mission.

Figure 1.4 – Simplified schematic of the devices and protocols involved in the users' segment.

1.1.2 Collaborators, sponsors, market and customers

Pluton UPV benefits from the support of numerous sponsors and collaborating institutions of a wide range of sectors. This thesis can be utilized as a means to strengthen existing ties or establish new contacts with companies and institutions, including PCB manufacturers, electronic components distributors, electronic instrumentation companies, and to ask for advice and consultancy to companies and research entities, as well as request access to testing facilities.

The Universitat Politècnica de València is currently the primary source of funding for Pluton UPV through the *Generación Espontánea* programme [9]. The present master's thesis has been conducted with the assistance and financial support of the Microwave Applications Group [5], a member of the iTEAM-UPV research institute [6]. In the course of this master's thesis, Altium Designer and the Altium 365 cloud service were employed, provided by Altium Ltd. as a sponsorship to Pluton UPV.

The mission is not for profit. However, various organizations may be interested in the technologies behind it, such as other CubeSat teams, students, professors, research groups, and universities. In the same way, companies may be interested in the product itself, or may seek advice and consultation on the technology.

1

1.2 State of the Art

Space has historically been associated with its landmark phase unfolded in the past century. Traditionally, space missions have been carried out by government or public agencies such as ESA, NASA, JAXA or Roscosmos. Public funding enabled the realization of missions with ambitious scientific, societal and geopolitical objectives, with minimal or no economic return except for spillover benefits on other industries [10], [11].

Traditional space missions make use of custom, sophisticated and well-tested technology which is designed to meet the highest quality standards and to comply with design and manufacturing normative. The large capital expenditures involved in traditional space missions have historically favored conservative and risk-averse methodologies that bound development to rigid systems engineering processes. Technical performance prevailed over economic efficiency [10], [12].

Satellite broadcasting, telephony and Global Navigation Satellite Systems (GNSS) are well-known and mature commercial space operations. Other private efforts have been limited to communications satellite constellations such as Teledesic, Globalstar, Iridium, OneWeb or Starlink, with varying degrees of commercial success [10].

In the 2000s and 2010s, after a push toward privatization, new business models for space companies emerged, leading to the so-called *"new space"*. Today, in addition to traditional public-funded endeavors, companies are executing for-profit space projects with public and private capital. *New space* actors seek economically viable space access, making extensive use of commercial off-the-shelf (COTS) components [10]–[13].

The *new space* field is a broad phenomenon that involves large system integrators, *start-ups*, government institutions and academia. *New space* activities include communications, remote sensing, space IoT, on-orbit services, space exploration, experimentation, education, space navigation, geolocation, Earth observation, meteorology, climate change monitoring, military, among others [14].

New space is supported by advances in miniaturized technology, novel development processes and risk management [10]. Among us the many advances, of particular relevance is the emergence of new satellite platforms such as micro-satellites and nano-satellites, of which CubeSats are the undisputed leader [11], [15]–[17].

1.2.1 CubeSats

A CubeSat is a satellite that conforms to the CubeSat Design Specification (CDS) [18]. The original CubeSat Design Specification was developed in 1999 by professor Jordi Puig-Suari from the California Polytechnic State University and professor Bob Twiggs, from the Stanford University Space Systems Development Laboratory. The standard describes satellites based on cubic units of approximately 10 cm side. This dimension was selected because it was deemed a reasonable working volume which provides sufficient surface for solar cells [19]. From this basic unit, many types of satellites of different sizes and weights are defined (Figure 1.6). The standard also defines the P-POD deployer, a container designed to carry and deploy CubeSats as a secondary payload while ensuring minimal risk to the primary payload and the launch vehicle [16].

Originally intended to promote satellite development in academic institutions, CubeSats have been adopted for science and commercial missions due to their compact size, lower cost and modular design [16], [20]. As of July 2024, about 2400 CubeSats have been launched [21] with hundreds announced every year (Figure 1.5).

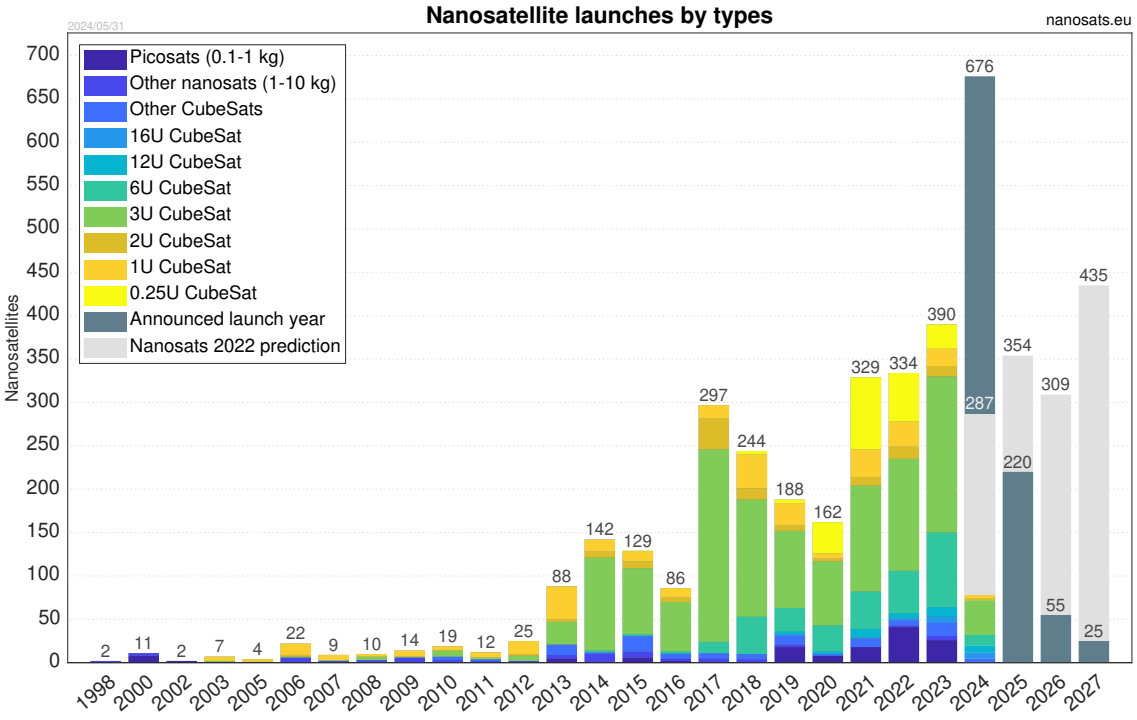
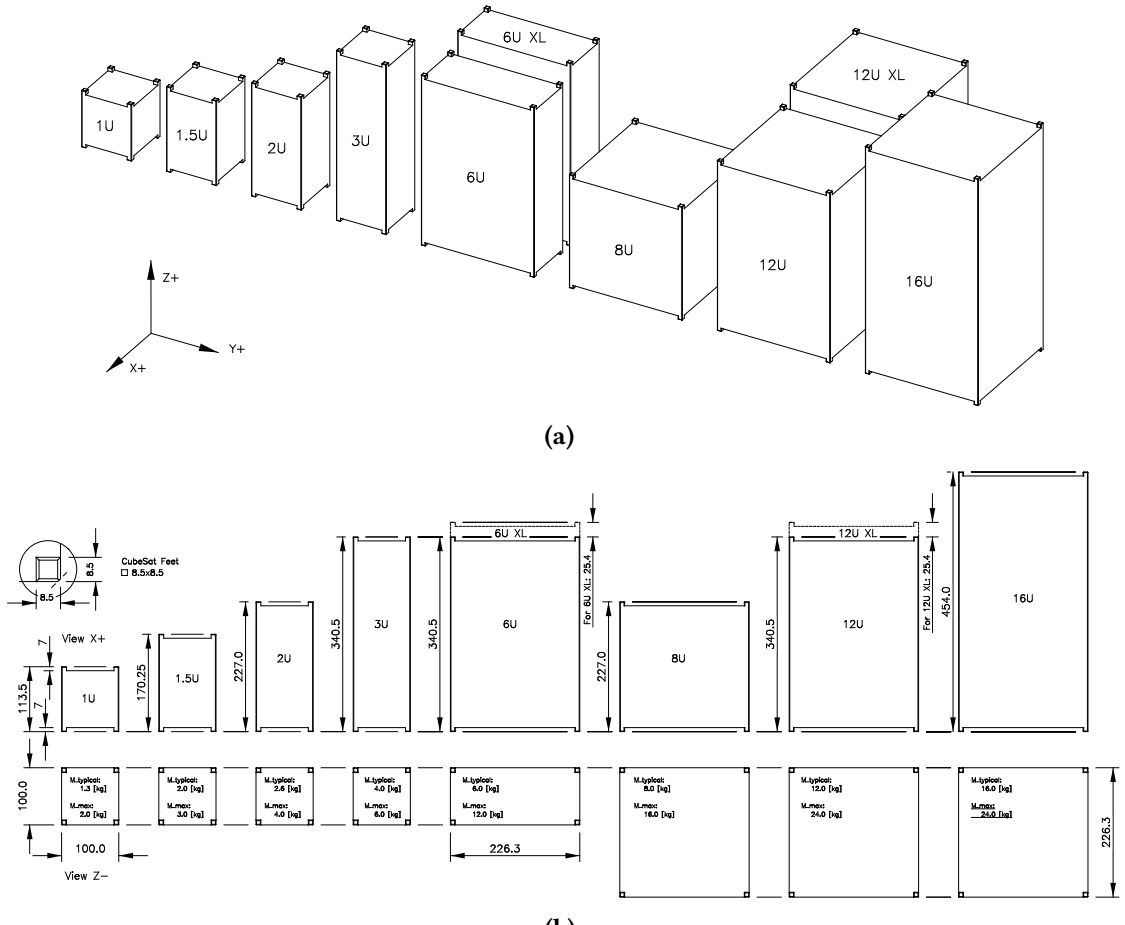


Figure 1.5 – Nano-satellite launches by year [17].



(a)

(b)

Figure 1.6 – Standard sizes of CubeSats. Units in mm. Extracted from [22] (modified).

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The CubeSat was conceived as an educational tool with a strong emphasis on innovation and risk-taking. Many non-educational entities have identified the potential of the risk-tolerant approach to facilitate rapid-development programmes [16]. Due to the brief development cycle, which can range from a few months to a few years [23], each individual flight is permitted a high tolerance for risk, as a series of flights will collectively achieve all programme objectives [16]. Many aspects of the risk-tolerant approach stem from the goal of keeping costs low enough to make failure tolerable. CubeSat make extensive use of commercial off-the-shelf (COTS) electronics to reduce costs.

1.2.1.1 The CubeSat electrical interface

The CDS does not define a specification for the electronics, allowing each mission to have its own unique solution tailored to its needs. However, as a consequence, there is currently a lack of interoperability between vendors of COTS components, requiring a per-mission customization. Vendor-locked ecosystems are common.

The most prevalent electrical standard is a stacked PCB-type connector called the CubeSat Kit Bus [13] (CSKB, or simply the *CubeSat Bus*) from Pumpkin Inc. [24]. This standard is widely used because the CubeSat Kit was one of the first products to publish a specification. The CubeSat Kit Bus is a PC/104-based electrical interface, which in turn is aimed at industrial embedded systems and avionics [3].

The CSKB establishes the mechanical interface, but does not define the pinout, protocols, or signals, which do not conform with the PC/104 standard. As a result of these limitations, numerous papers have proposed standardized and miniaturized CSKB alternatives [25]–[28]. However, these solutions have not been adopted as of today.

The community has made efforts to standardize the CubeSat Kit Bus through open source projects such as LibreSpace [29] or LibreCube [30], and defining CubeSat-specific protocols such as SpaceCAN [31]. Despite this, due to the lack of out-of-the-box interoperability between vendors, it is common practice to define per-mission custom pinouts.

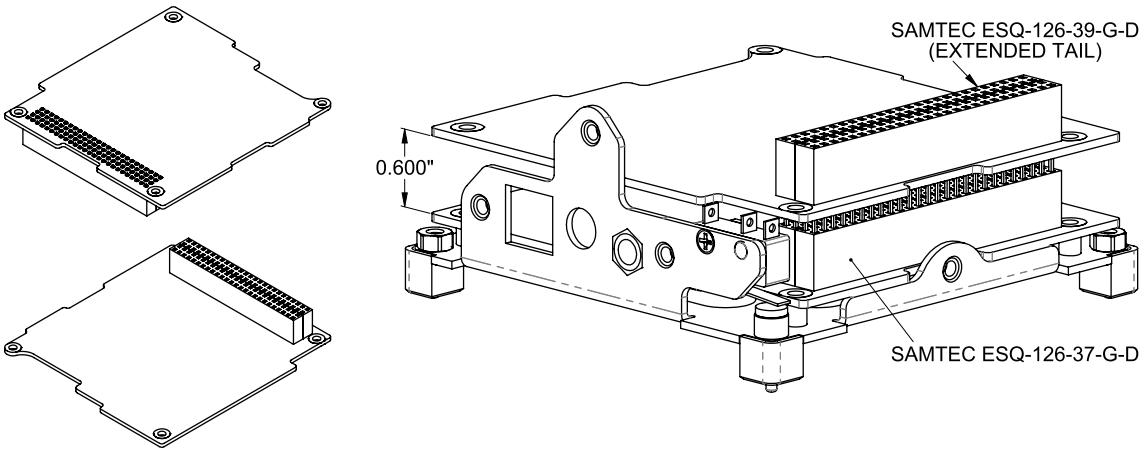

Figure 1.7 – Left: top and bottom view of the CubeSat Kit board. Right: CubeSat Kit example stack. Extracted from [24] (modified).

1.2.1.2 Typical CubeSat subsystems

- **The structure** is the mechanical support of the subsystems.
- **The On-Board Computer (OBC)** manages the satellite. The OBC ensures the correct processing, storage, and transmission of data and telemetry, processes the commands sent by the ground station and performs *housekeeping* tasks [32].
- **The Electrical Power System (EPS)** provides, stores, regulates, and distributes power. For power generation, the prevalent method is photovoltaic panels; and for power storage, lithium-ion and lithium-polymer batteries. The voltages and current ratings are subsystem, COTS, and mission dependent [33].
- **The Attitude Determination and Control System (ADCS)** determines the orientation (attitude) and spin rate of the spacecraft. It detumbles, stabilizes and points the satellite into a desired orientation. Cameras, instruments and antennas often require a specific pointing direction, with requirements for pointing accuracy, stability and rotation rate. Satellites also require a specific pointing for thermal control or power generation. The orientation can be determined by various types of sensors, such as gyroscopes, magnetometers, sun sensor or star trackers. Common actuators include *magnetorquers* and inertial wheels [34].
- **The Telemetry, Tracking and teleCommand (TT&C)** subsystem consists of the transceivers and antennas that provide the spacecraft with communication capabilities. Due to the critical nature of this subsystem, this radio is typically restricted to the CubeSat operator's ground station (GS), and it is not or only partially available to other users. For tracking, radio beacons are used. TT&C radios are traditionally low data rate and employ narrowband antennas [35].
- **The payload** performs the primary tasks for which the satellite was launched. It refers to the sensors, scientific instruments, equipment and/or experiments that the satellite is designed to operate in space. It is the primary mission element of a CubeSat and is distinct from the satellite's support systems, which are responsible for ensuring the CubeSat's operation and functionality.

1.2.2 Internet of Things, LPWAN and LoRa in space

The Internet of Things (IoT) has become an ubiquitous technology. IoT describes a network of sensors and actuators attached to real-world objects. It is widely used on Earth for a multitude of applications, including smart home, smart cities, metering and monitoring [36]. To address the exponential growth of IoT, Low Power Wide Area Networks (LPWAN) technologies have emerged. LPWAN is designed for low-cost, low-power IoT networks. LPWAN communications are characterized by the transmission of small chunks of data at low bit rates over narrowband channels, which enables extended communication ranges [36], [37].

LoRa is a popular LPWAN technology developed by Semtech Corporation and supported by the LoRa Alliance. LoRa is known for its remarkable performance in low signal-to-noise ratio (SNR) environments, which has attracted the attention of academia and industry [37]. LoRa is a proprietary Layer 1 wireless protocol and modulation technique based on Chirp Spread Spectrum (CSS) [38]. LoRa serves as the foundation for LoRaWAN, a medium access control (MAC), link, and network protocol [39]. A more detailed explanation is developed in section 2.3 (page 24).

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In recent years, satellite and IoT companies have recognized the business opportunities in enabling satellite IoT. Satellite IoT would allow devices located anywhere on Earth to exchange data, complementing terrestrial networks. This can be particularly useful in remote areas where infrastructure is lacking. Satellite IoT is becoming more accessible thanks to advances in the CubeSat ecosystem [40], [41]. The efficacy of IoT in space depends on the use of robust wireless protocols. LPWAN technologies such as LoRa are candidates due to their ability to cover vast areas with low power [40], [42].

Low-Earth orbit (LEO) satellites are attractive for IoT because of their ability to provide direct-to-satellite connectivity with short delays, compared to geostationary orbit (GEO) satellites [40]. This delay, on the order of a few milliseconds, is more than sufficient for IoT services. However, the orbital characteristics of LEO imply limited visibility and short passes [43]. The issue is being addressed through the use of large constellations [41]. This approach has raised concerns about its environmental impact, particularly on astronomy and astrophotography [44] and the risks posed to the space sector itself [45].

A number of companies, including Lacuna Space [46], Fossa Systems [47] and Wyld Networks [48], have already deployed global LoRa connectivity using LEO satellites. Other examples of LoRa CubeSats include Norby [49] and the Thingsat payload on the SatRev Stork [50]. Moreover, a community has formed around TinyGS [51], developed by the founders of Fossa Systems. TinyGS is a service in which radio amateur, LoRa-based, worldwide mini ground stations receive and decode beacons and telemetry from many different LoRa-enabled satellites and relay it to the TinyGS servers for public use.

1.3 Scope and methodology

This master's thesis, part of Pluton UPV's *Estigia* mission, presents the design of an engineering model for a space-grade LoRa communications payload to be embarked on a CubeSat flying in low-Earth orbit (LEO).

In light of the groups's lack of previous experience in satellite development and the constraints imposed by limited resources in terms of funding, facilities, human resources, and *know-how*, it is prudent to avoid overly complicated designs. This approach can mitigate potential risks during the development process such as delays or cost overruns.

The engineering model designed in this master's thesis employs a modular approach, as determined in discussion with Pluton UPV. The aim of this strategy is to divide the development effort and facilitate the testing and debugging processes. Modules can be updated independently, and in the event of a failure, only the affected module is replaced. Concurrently, an auxiliary board designated as Electrical Ground Support Equipment (EGSE), is to be designed to provide a test hardware platform for the payload.

This master's thesis, part of the Master's Degree in Electronic Systems (MUISE), represents the first phase of a planned two-phase project (see Figure 1.9). This initial master's thesis addresses the definition and analysis of the problem, a comprehensive literature review, and the conceptualization of a solution, including its detailed specifications and design. It also considers manufacturing and verification aspects. The methodology employed in this project is based on the Engineering Design Process (EDP), which is outlined in the following section.

The second phase will be addressed in a subsequent master's thesis. This will include manufacturing and assembly of the hardware, firmware programming, debugging, testing, verification and validation, feedback gathering and further design iteration.

1.3.1 Engineering Design Process

The work of an engineer is largely concerned with design. Design defines solutions for unsolved problems or gives new solutions to problems that have been previously addressed in a different manner. The creation of an effective design requires creativity, informed decision-making, and the ability to make compromises. Design is the culmination of a process that entails planning and effort, a work frequently achieved by breaking down the challenge into smaller, manageable components [52].

The Engineering Design Process (EDP) represents a series of steps that engineers typically follow in order to solve a problem. The EDP can be applied to the current project in accordance with the existing aerospace development methodologies [23], [53]–[55]. The development stages are shown in Figure 1.8.

- **Identify and define the problem**. Addressed in Chapter 1.
- **Perform a background research and analysis** to gain a comprehensive understanding of the context, state of the art, and to identify potential missteps. Chapter 1 and Chapter 2 develop this step.
- **Requirements engineering** is the process of defining the system's behavior, functions, and operating constraints. This is tackled in Chapter 3.
- **Brainstorming and feasibility assessment** of potential solutions, which are evaluated in terms of their advantages and disadvantages, discarding infeasible or non-compliant solutions. This is discussed in Chapter 2, Chapter 3 and Chapter 4.
- **Specify the device's architectural design**, as well as the technological solutions that will be employed. This point is developed in Chapter 3 and Chapter 4.
- **Development** consists on the implementation of the selected solution. Prototypes allow testing before production. This process appears in Chapter 4.
- **Test** the prototype, **verify** if it meets the requirements, and **validate** if the prototype provides an adequate solution to the problem, identifying design issues. This is planned for the second master's thesis.
- **Feedback and redesign.** The design process entails a series of iterations until a compliant solution is reached. Following the identification of issues during testing, modifications must be made. This will be addressed in the second master's thesis.
- **Communication of results.** Documentation is generated in each step, and the results of the iteration are shared. Both master's thesis will record the entire engineering process and results.

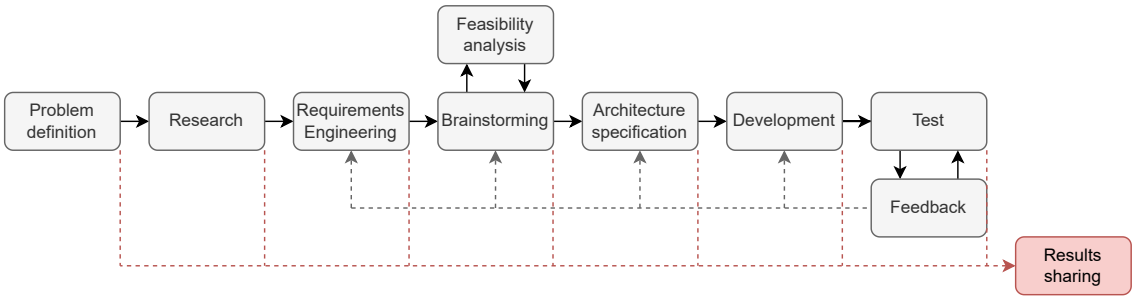

Figure 1.8 – The Engineering Design Process.

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1.4 Objectives

After introducing the motivation and scope of this master's thesis, the top-level objectives of the project are listed in Table 1.1. These goals are the expected results of the master's thesis in academic and professional terms.

Obj. ID	Objective description
O-1	To design a space-grade LoRa communications payload for the *Estigia* mission and an auxiliary board as electrical ground support equipment for testing the payload.
O-2	To become familiar with the CubeSat standard at the electrical level and its development process with external constraints.
O-3	To become proficient in mixed-signal, multi-layer printed circuit board designs and multi-board assemblies.
O-4	To gain experience with standards and regulations such as ITU/RR and ECSS.
O-5	To prove the student's capabilities of carrying out an engineering project and to document the entire process.
O-6	To put into practice the knowledge acquired during the double Master's degree in Telecommunications Engineering and Electronic Systems Engineering.
O-7	To successfully complete the master's thesis in Electronic Systems and lay the groundwork for the master's thesis in Telecommunications.

Table 1.1 – Principal top-level objectives of this project.

1.5 Project tasks and organization

The Gantt chart in Figure 1.9 illustrates the duration of each task within this first master's thesis. At the beginning of the project, a comprehensive review of the existing literature was conducted in order to identify relevant bibliography, precedents, and open-source designs.

Concurrently, simulations of the radio link were developed, which, in conjunction with the research, enabled the identification of requisites, constraints, and the hardware architecture. Then, the definition of the circuits and their documentation began. Following a review and subsequent corrections, the design of the printed circuit boards was carried out. All generated documentation has been organized in this report.

Figure 1.9 also illustrates the provisional schedule for the second master's thesis. The second phase is of a shorter duration despite having a greater number of ECTS. It is therefore crucial to develop as much material as possible during the first phase.

It is inherently difficult to estimate the time required for a project, particularly in the presence of external factors such as manufacturing, shipping, sponsorship, and access to testing facilities. Given the potential for unforeseen circumstances, the planned timeline may not be met, and a buffer of several months is added.

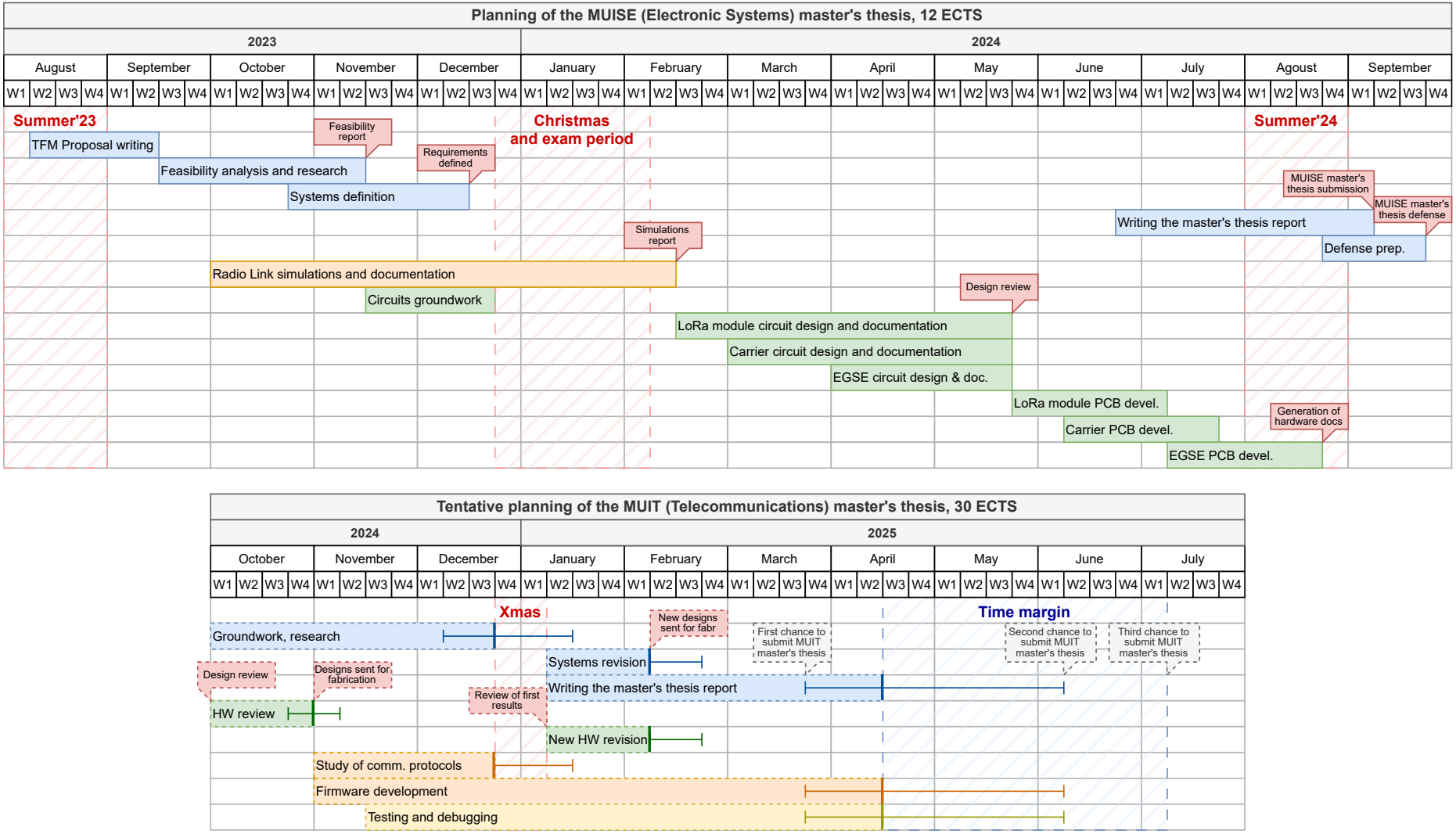

Figure 1.9 – Gantt chart illustrating the project's timeline. Includes the planning of the MUISE's thesis and a provisional schedule for the MUIT's thesis.

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1.6 Report structure

This document is divided into five chapters and five appendices. The chapters elaborate on the stages of development of the devices, while the appendices provide supplementary materials related to the project.

1. **Chapter 1: Introduction.** The initial chapter establishes a foundation for the subject matter, and delineates the project's objectives and motivations.
2. **Chapter 2: The radio link.** This chapter presents a comprehensive study of the Earth-satellite radio-frequency link, addressing telecommunications norms, link budget simulations, and an in-depth examination of the LoRa protocol and its configuration. This chapter provides an in-depth analysis of the design constraints that must be overcome for the communication system to function optimally.
3. **Chapter 3: Specifications.** The objective of this chapter is to define the requirements that the electronics must fulfill. Once they have been established, a hardware architecture is proposed, with the selection of the most relevant components. The specifications serve as the basis for the subsequent design.
4. **Chapter 4: Design.** This chapter provides a complete description of the system design, including the electronic circuits and the printed circuit board, in accordance with manufacturing considerations.
5. **Chapter 5: Conclusions and future lines.** This chapter concludes the primary content of this master's thesis. First, a review of the achieved milestones and requisites is conducted, and future lines of work are established. Additionally, this chapter reflects on improvements, corrections and addresses other lines that have emerged from the development process.

A. **Appendix A: Sustainable Development Goals.** This appendix demonstrates the alignment of this project with the Sustainable Development Goals.

B. **Appendix B: Project costs.** This addenda provides a detailed account of the costs associated with this project.

C. **Appendix C: Circuit schematics.** The complete circuit schematics of the three developed boards are provided in this appendix.

D. **Appendix D: Printed Circuit Boards.** Includes prints of the three PCBs.

Chapter 2

The radio link

Before designing the electronics, it is necessary to define the characteristics of the radio frequency communication, so that the requirements can be established.

In this chapter, an analysis of the telecommunications regulations is conducted, the basics of LoRa are explained, and a link budget analysis is performed.

2.1 Telecommunications regulations

One of the key issues to be considered in the early stages of a small satellite programme is the selection of radio frequencies. The ITU Radiocommunication Sector (ITU-R) administers the RF spectrum, defining the various radio communication services, allocating frequency bands to them, specifying technical conditions for its use, and laying down procedures for frequency assignment [56], [57].

Until recently, small satellites have operated under the permissive legal framework provided by the ITU-R for amateur satellite services. However, they are now assigned services in the regular service regime and are processed in the same way as large satellites [57], [58], in compliance with Article 5 of the ITU Radio Regulations (ITU/RR) [59].

There is no license-free nor ISM band for any space service allocation [60]: all satellites require ITU approval of frequencies. Since satellite operators cannot directly initiate applications for use of frequencies, they must apply for ITU-recognized operating rights through their national institutions [57], [61]. In Spain, the *Secretaría de Estado de Telecomunicaciones e Infraestructuras Digitales* is the competent body for processing orbit-spectrum appeals to the ITU [62].

2.1.1 Sub-GHz frequency bands allocation for small satellites

Only sub-gigahertz bands intended for use in space will be considered, in view of:

1. To make the communications system compatible with existing commercial LoRa transceivers, which typically operate in the sub-GHz bands [63]–[67].
2. To simplify and reduce the complexity and cost of the communications hardware.
3. To reduce the Free Space Path Losses (FSPL), which are dependent on frequency (see section 2.2: Link budget simulations, page 15).

In the ITU/RR allocation tables, various types of space services are defined for satellites: space operations, weather monitoring satellite, space exploration satellite, Earth observation satellite, and amateur-satellite. Satellites that are used for commercial purposes can apply for other types of allocations such as telecommunications, remote sensing or geolocation [58]. Most non-geostationary small satellites operate in the frequencies that do not require coordination [68]. The typical sub-GHz frequency bands allocated for small satellites are shown in Table 2.1.

The amateur satellite service (EA) is a special case. Like the amateur service itself, it is defined for the purposes of training, communication and research by radio amateurs, *i.e.* authorized individuals interested in radio technology and without pecuniary interest [69]. The frequency allocation for the amateur-satellite service is shown in Table 2.2.

2

Band	Service	Symbol*	Type
401.0 – 403.0 MHz	Earth exploration satellite service (Earth-Space)	EW	Primary
401.0 – 402.0 MHz	Space operation service (Space-Earth)	ET	Primary
449.75 – 450.25 MHz	Space operation service (Earth-Space) Space research service	ET EH	Secondary, See note 5.28 and 9.21 [59]

Table 2.1 – Typical Sub-GHz frequency band allocations for small satellites [58], [70]. *Symbols identify station classes. EW: space station in the earth exploration-satellite service; ET: space station in the space operation service; EH: space research space station.

Band	Wavelength	Type	Note
28.0 – 29.0 MHz	10 m	Primary	Used primarily with the 144 MHz band
144.0 – 146.0 MHz Sat: 145.794 – 146.0 MHz	2 m	Primary	In heavy use (Figure 2.1)
435.0 – 438.0 MHz	70 cm	Secondary Note 5.282	

Table 2.2 – Sub-GHz frequency band allocations for amateur-satellite services [58], [71].

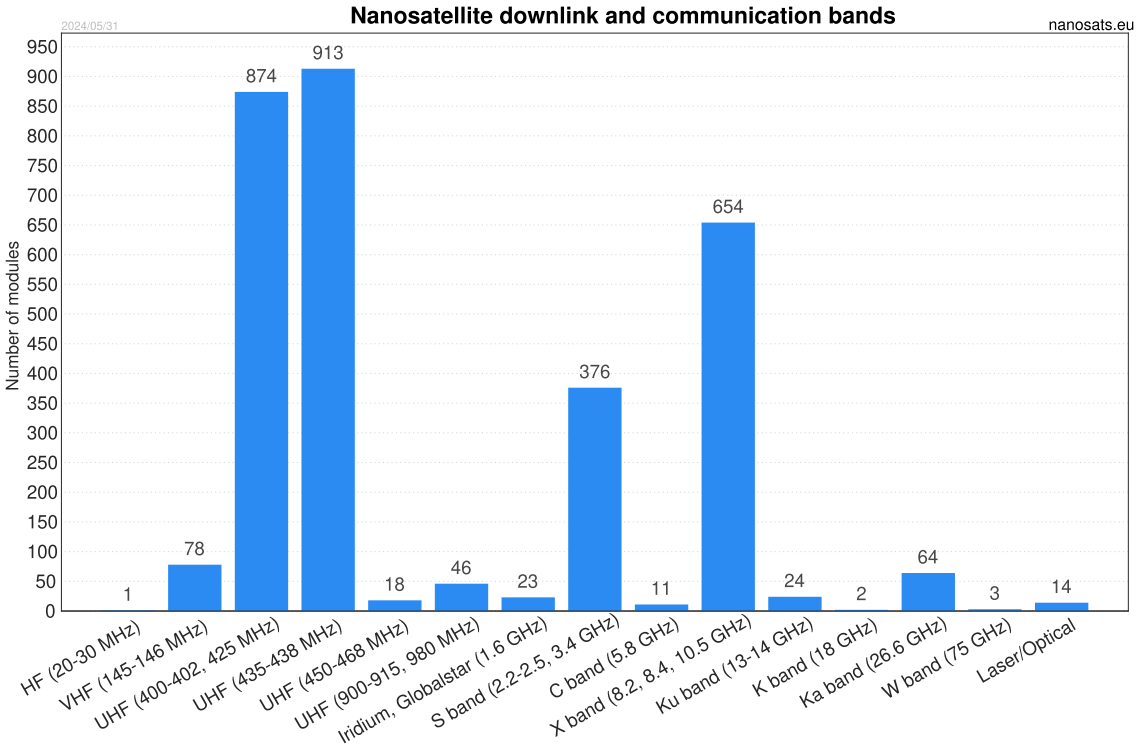


Figure 2.1 – Number of communication modules per frequency bands in nano-satellites [72].

2.1.2 Selecting the operating frequency

The nature of the *Estigia* mission makes it suitable for the amateur service. Of the three bands shown in Table 2.2, the 435 – 438 MHz band is the most interesting option.

This frequency range is a sweet spot: it is available in the three ITU-R regions [59], off-the-shelf LoRa transceivers can be used without modification, it suffers from relatively low FSPL, and its wavelength allows the use of cheap, medium-sized wire antennas while circuits can be relatively miniaturized.

Another advantage is that it does not overlap with the 433.05 – 434.79 MHz ISM band, which is congested and prone to interference. However, it is still one of the most overcrowded bands, as can be seen in Figure 2.1. On this frequency band, amateur-satellite use is secondary, and it may be required to free up channels for the primary service. It is also important to ensure that the station does not cause harmful interference to the other of services allocated in the frequency band [59].

In addition, the Telemetry, Tracking and teleCommand (TT&C) unit of the *Estigia* CubeSat will be operating in the same frequency band, which can lead to shared-medium conflicts. To avoid the complexity of managing the shared medium, it has been proposed to physically separate the communication systems. In this regard, the feasibility of using the 863 – 870 MHz band will be assessed in the next section.

Despite the drawbacks, the 435 – 438 MHz band finally has been chosen to apply for the *Estigia* mission. LoRa has good interference rejection, and the communications system will operate at low power to reduce interference to other services. However, its limitations and potential issues should always be kept in mind.

2.2 Link budget simulations

A link budget is an accounting of all the gains and losses encountered in the transmission of a signal. The link budget is an essential tool in the design and dimensioning of earth-space communications systems, as it enables feasibility and performance analysis of transmissions between the satellite and a ground station (GS). The results will allow the requirements for the communications systems to be defined, so that it can be assessed the characteristics of the antennas, low-noise amplifiers (LNA), power amplifiers (PA) or insertion losses, among others.

The ITU-R P.618 [73] is an ITU recommendation that provides guidelines for predicting the propagation conditions and attenuation due to atmospheric factors, particularly for satellite and space communication systems.

Many works have presented analytical solutions to the link budget for earth-space communication systems based on the ITU-R recommendations [74], [75], including IoT and narrowband systems [40], [76], and even in the particular case of LoRa [77].

In this project, however, a simulation-based approach is proposed. The results are equivalent to those obtained with hand calculations, but without approximations and with the advantages of computation such as easy data manipulation, automation, optimizations and sweeps.

MatLab has a Satellite Communications Toolbox since version R2021a [78], which allows modeling, simulation, and analysis of satellite communication systems and links. The toolbox includes capabilities for link budget analysis, waveform generation, antenna design, and orbit modeling and propagation, among others.

The developed MatLab script is an all-in-one solution for automatic link assessment tool for a LEO satellite: it propagates a given orbit via a `.tle` file and computes access intervals in a given simulation time, azimuth, elevation and range for the ground station, received signal strength, Carrier-to-Noise Ratio (CNR), latency, Doppler frequency shift, Doppler frequency rate, free space path losses (FSPL) and atmospheric losses using digital models of the ITU-R P618, P836, P837 and P840 recommendations [79].

2.2.1 Orbit and ground station

For a plausible satellite orbit, a TLE file generated internally by Pluton UPV is used, dated December 2023. Other work by colleagues of the team is focused on studying, optimizing and obtaining orbits taking into account the balance of sun and eclipse, energy budget, temperature, number of passes and pass duration [80], [81]. It should be noted that while this orbit is not final, it serves to demonstrate the link budget feasibility, since it shows both worst and best cases.

The coordinates of the ground operator are particularized for the new station located at the UPV-ETSIT's roof: 39°28'11.10" N, 0°22'38.60" E. This novel station is currently operated by the Microwave Applications Group (MAG), member of the Institute of Telecommunications and Multimedia Applications (iTEAM-UPV) [75].

Figure 2.2 shows a 3D scenario of the propagated orbit in a near vertical pass over Valencia. This pass is the one for which the results will be shown below, since it allows the evaluation of both minimum elevation (thus maximum range between the GS and the satellite) and maximum elevation (minimum distance).

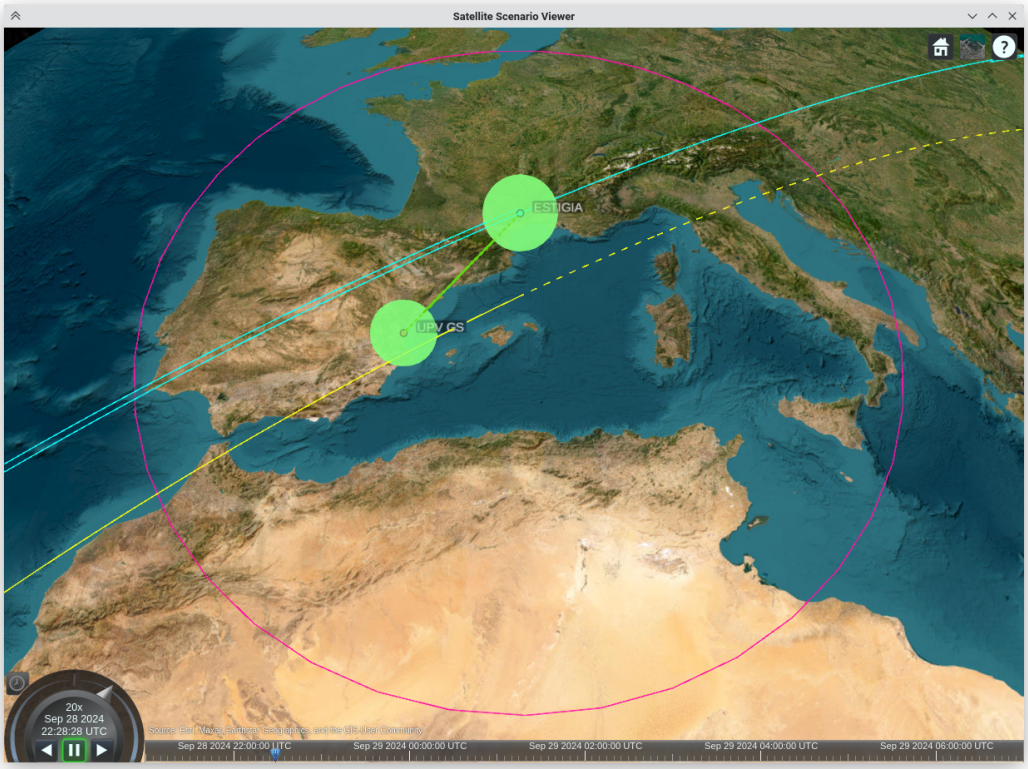


Figure 2.2 – 3D visualization of the simulated orbit for the link budget. The blue line represent the orbit trajectory, the yellow line the trace of the satellite on the surface of the Earth, and the magenta circle the coverage area with the given elevation (calculated using [43]).

2.2.2 Simulation parameters and assumptions

Table 2.3 lists the simulation parameters passed to the script. Several simulation cases have been devised to assess several key parameters. In particular, the feasibility of 435 MHz and 868 MHz carriers has been evaluated, with different transmit powers and noise figures at the ground station. In this way, the link budget is evaluated for the case of using a *high quality* (HQ) ground terminal and a *low quality* (LQ) terminal. A summary of the simulated cases is given in Table 2.4.

- **Central frequency.** Varies according to the simulated case. 435 MHz was chosen as the representative frequency of the 435 – 438 MHz band; idem for 868 MHz for the 863 – 870 MHz band.
- **Bandwidth.** 125 kHz is the selected bandwidth for LoRa. See section 2.3.3: Selecting LoRa radio parameters, page 27.
- **Minimum elevation.** Access is defined as the intervals at which the satellite and the ground station are in line of sight (LoS), that is, when the ground station elevation is greater than the minimum elevation. A larger minimum elevation angle increases the received power and CNR in the LoS extremes. This comes at the cost of less observation time. 10º has been considered an absolute minimum. Below this, obstacles such as buildings or land relief often impede communication.
- **Transmission power.** The RF power emitted. Varies with the simulation case. For cases 2 and 4 (LQ terminal) the maximum output power of 22 dBm (158 mW) of the SX127x series has been considered [63]. For cases 1 and 3 (HQ terminal), the power is increased to 30 dBm (1 W) with the use of an additional PA.
- **Antenna gain.** A measure of an antenna's ability to direct energy in a specific direction. 0 dB means that the antenna is considered to be isotropic, an ideal antenna that radiates electromagnetic energy uniformly in all directions.
- **Insertion losses.** Currently unknown. In order to establish a safety margin, it is estimated as 3 dB in both the transmitting and receiving paths.
- **Receiver sensitivity.** the minimum signal strength that the receiver can detect. −137 dBm is the reported sensitivity of commercial LoRa transceivers for the configuration described in section 2.3.3: Selecting LoRa radio parameters, page 27.
- **Noise figure.** Quantifies the degradation of the SNR as a signal passes through a component. For commercial LoRa receivers it is estimated as 6 dB [82]. This value was used for cases 2 and 4 (LQ terminal). The noise figure is highly dependent on the first element in the chain, and can be improved by introducing a LNA before the receiver. For cases 1 and 3, a high quality (HQ) receiver is used and assumed to have a noise figure of 3 dB.
- **Antenna physical temperature.** The temperature of the antenna itself. Contributes to noise. Temperature can vary greatly in orbit. 350 K has been considered as a worst case in Pluton UPV's studies.
- **Antenna noise temperature.** Quantifies the noise power received by an antenna from external sources in terms of an equivalent temperature. For the ground station antenna 290 K is considered the worst-case, whereas for the satellite is 2340 K as it receives a lot of interference from Earth [77].

Element	Parameter	Value	Units	Notes
RF Band	Center frequency	[Case 1, 2]: 435 [Case 3, 4]: 868	MHz	See section 2.2.2
	Bandwidth	125	kHz	See section 2.3.3
Ground Station	Latitude	39.48943	°N	
	Longitude	-0.34230	°E	
	Altitude	50	m	Above Earth's surface
	Minimum elevation	10	degrees	
	Transmission power	[Case 1, 3]: 30 [Case 2, 4]: 22	dBm	See section 2.2.2
	Antenna gain	0	dBi	Isotropic antenna
	TX insertion losses	3	dB	Estimated, placeholder
	RX insertion losses	3	dB	Estimated, placeholder
	Receiver sensitivity	-137	dBm	See section 2.3.3
	Receiver noise figure	[Case 1, 3]: 3 [Case 2, 4]: 6	dB	See section 2.2.2
	Antenna physical temp.	300	K	Room temperature.
	Antenna noise temp.	290	K	Uplink worst case [77]
Satellite	Altitude	400	km	Above Earth's surface
	Transmission power	30	dBm	
	Antenna gain	0	dBi	Isotropic antenna
	TX insertion losses	3	dB	Estimated, placeholder
	RX insertion losses	3	dB	Estimated, placeholder
	Receiver sensitivity	-137	dBm	See section 2.3.3
	Receiver noise figure	3	dB	Estimated, placeholder
	Antenna physical temp.	350	K	Estimated maximum temperature when in direct sunlight
	Antenna noise temp.	2340	K	Electromagnetically busy environment [77]

Table 2.3 – Link budget simulation parameters.

Case	Frequency	GS TX power	GS RX NF	Description
1	435 MHz	30 dBm	3 dB	High-quality (HQ) ground terminal.
2	435 MHz	22 dBm	6 dB	Low-quality (LQ) ground terminal.
3	868 MHz	30 dBm	3 dB	High-quality (HQ) ground terminal.
4	868 MHz	22 dBm	6 dB	Low-quality (LQ) ground terminal.

Table 2.4 – Summary of the link budget simulation cases.

2.2.3 Results

2.2.3.1 Access intervals, azimuth, elevation and slant range

Access is defined as the periods at which the satellite and the ground station are in line-of-sight. The link simulation runs during access intervals. The attached results are for a single near-vertical pass over Valencia. The situation is quasi-optimal, with almost 80° of maximum elevation and a pass duration of 6 min 10 s.

In Figure 2.3, the azimuth (horizontal angle) and elevation (vertical angle) are plotted for the ground station to track the satellite. The slant range is the distance that separates the satellite from the ground station. The satellite appears over the horizon with a minimum elevation of 10°, and constitutes the worst case, when the distance is maximum (1400 km) and the transmission must cross the atmosphere diagonally (see Figure 2.5).

2.2.3.2 Latency and Doppler frequency shift

Latency is defined as the time it takes for a signal to travel from the transmitter to the receiver. It depends directly on the distance between the communication peers. As it can be seen in Figure 2.4, the latency is in the range from 1.3 ms to 4.7 ms at worst, so it will be instantaneous in the eyes of human operators. Sources of delay between sending a message and receiving a response are addressed in section 2.3.6: Data budget and medium access control (page 32) and section 2.4: Discussion (page 33).

The maximum Doppler shift occurs when the satellite appears on the horizon, since its relative velocity is at its maximum [83]. For the 435 MHz carrier it is about ±10 kHz, while for the 868 MHz carrier it is ±20 kHz (Figure 2.4). As expected, the deviation is the same in relative terms (23 ppm). The maximum Doppler rate (the change in frequency per unit of time) is greater at the apogee (see Figure 2.5) [83]. The effect of the Doppler shift and Doppler rate on LoRa combinations is assessed in section 2.3.5: Frequency error sources and frequency stability (page 30).

2.2.3.3 Atmospheric propagation losses

The MatLab script employs the ITU-R P.618 recommendation [73] to estimate the atmospheric losses expected near Valencia. These losses are based on stochastic models and require a parameter of *exceedance*. Exceedances are statistical occurrences where specific atmospheric conditions cause losses to exceed a given threshold. They are represented as percentages of time, indicating how often certain loss values are surpassed. Exceedances have been set to the worst-case values of the model. But since the carrier frequencies are in the sub-GHz range, atmospheric losses are minimal.

The following attenuation sources are considered. Results are listed in Table 2.5.

- **Gaseous attenuation** represents the attenuation due to molecular absorption by atmospheric gases, primarily oxygen and water vapor. It is estimated at 0.176 dB.
- **Cloud and fog attenuation** is estimated to be 0.007 dB.
- **Rain attenuation** is estimated at 0.024 dB.
- **Attenuation due to tropospheric scintillation** accounts for signal fluctuations caused by atmospheric turbulence in the troposphere. It is the most important source of atmospheric attenuation, at 0.562 dB

The total atmospheric propagation losses amount to 0.990 dB.

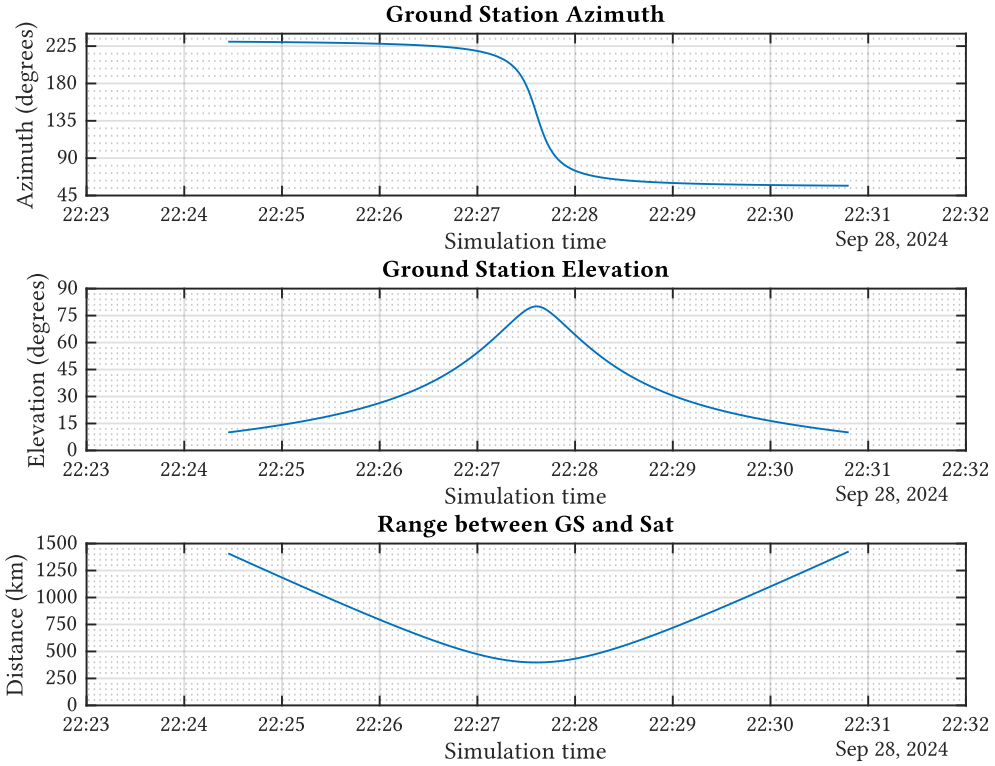


Figure 2.3 – Link simulation: azimuth, elevation and slant range.

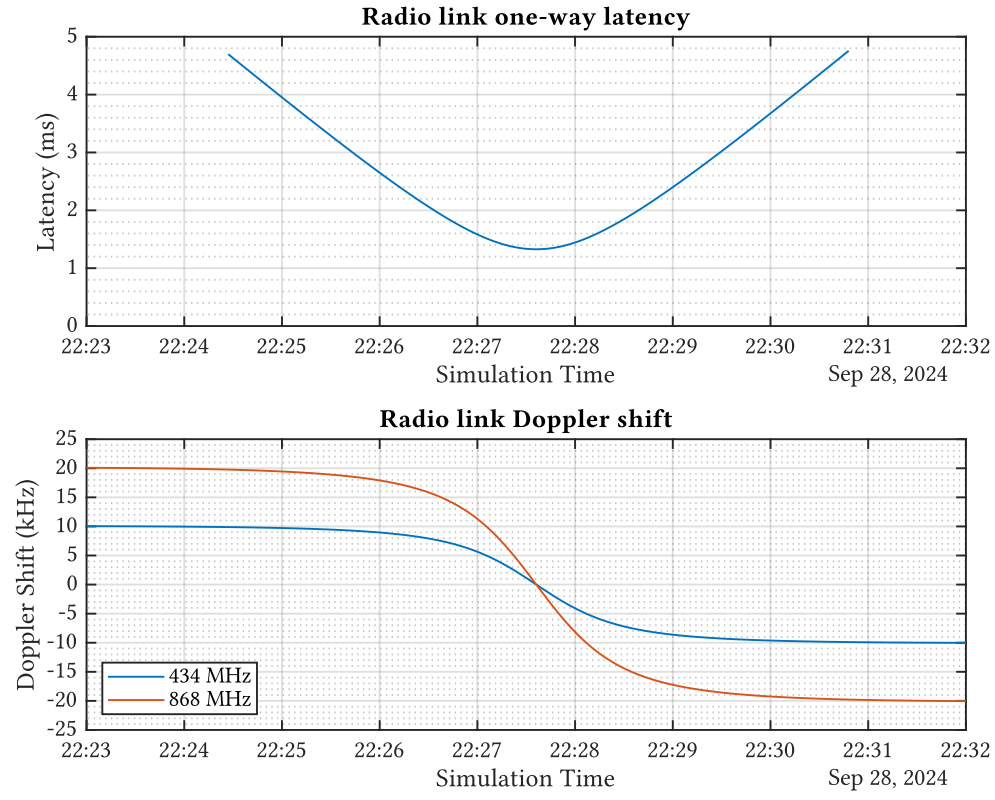


Figure 2.4 – Link simulation: one-way latency and Doppler shift.

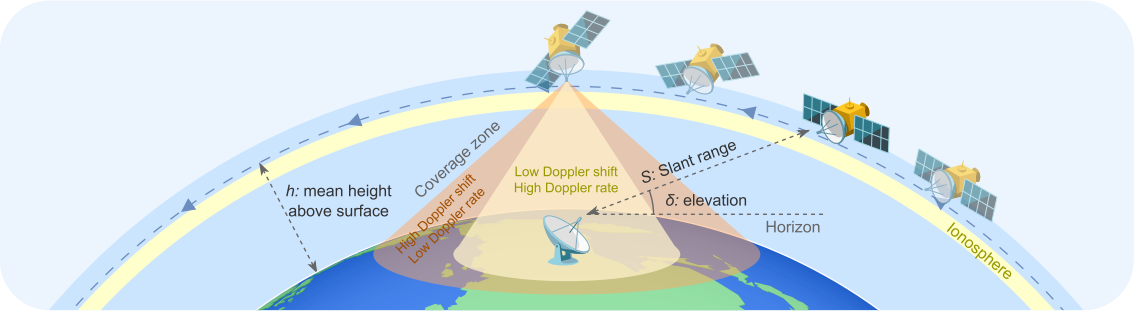


Figure 2.5 – Orbit geometry drawing.

Attenuation	Value (worst-case)	Comments
Gaseous attenuation	0.176 dB	
Cloud and fog attenuation	0.007 dB	Negligible
Rain attenuation	0.024 dB	Negligible
Tropospheric scintillation attenuation	0.562 dB	
Polarization loss (Faraday rotation)	3.0 dB	Manually picked
Free-Space Path Loss	[435 MHz]: 148.2 dB [868 MHz]: 154.2 dB	
TX insertion loss	3 dB	Estimation, placeholder
RX insertion loss	3 dB	Estimation, placeholder
Total	[435 MHz]: **158.2 dB** [868 MHz]: **164.2 dB**	

Table 2.5 – Summary of worst-case attenuation in the link budget.

2.2.3.4 Polarization losses

Electromagnetic waves that propagate in the Earth's ionosphere are subjected to the so-called Faraday effect, in which the wave's polarization is rotated under the influence of a magnetic field along the direction of wave propagation. If circularly polarized antennas are used, rotational losses are avoided, since they are invariant under rotation [83]. The CubeSat for the *Estigia* mission is expected to use circularly polarized antennas on both the ground segment and the satellite.

Polarization losses are currently not simulated by the Satellite Communication Toolbox. To cover the worst case, a maximum loss of 3 dB is chosen, which corresponds to the fact that only one of the components of the circular polarization reaches the receiver.

Additionally, the simulation provides the cross-polarization discrimination (XPD). XPD is a measure of the ability of an antenna to discriminate between signals of different polarizations. Simulations yield an XPD of 72.6 dB, which is excellent.

2.2.3.5 Free space path losses

The most significant contributor to attenuation is the Free-Space Path Loss (FSPL), given that the communication is established with line of sight (without multipath that can cause fading) and wide-beamwidth wire antennas are employed (wherein the radio wave is spread, not confined in a beam). At minimum elevation, the FSPL losses are approximately 148.2 dB for a carrier frequency of 435 MHz and 154.2 dB for 868 MHz. At the apogee they are 137.2 dB for 435 MHz and 143.3 dB for 868 MHz.

2.2.3.6 Received signal strength and compliance assessment

Once all loss contributors have been evaluated, the power balance is performed to determine the signal power at the receiver. Compliance is achieved when the received signal strength is greater than the receiver sensitivity (−137 dBm, as described in section 2.3.3, page 27) plus a security margin of 3 dB [56]. The simulation curves are shown in Figure 2.6 and the worst-case results are summarized in Table 2.6. The sensitivity requirements are only met in one out of four of the test combinations.

Since the satellite's transmit power remains constant, the 6 dB difference seen in downlink between the carriers is only due to the FSPL. The 868 MHz carrier is nearly compliant, but not regarded as reliable, as it sits just in the safety margin. It is encouraging to note that the 435 MHz carrier still has 5.8 dB of headroom.

In uplink, the use of low-quality terminals results in a 8 dB reduction in received signal power at the satellite due to the difference in transmit power. Consequently, the communication time is reduced to 4 min 40 s for 435 MHz and only 1 min 40 s for 868 MHz.

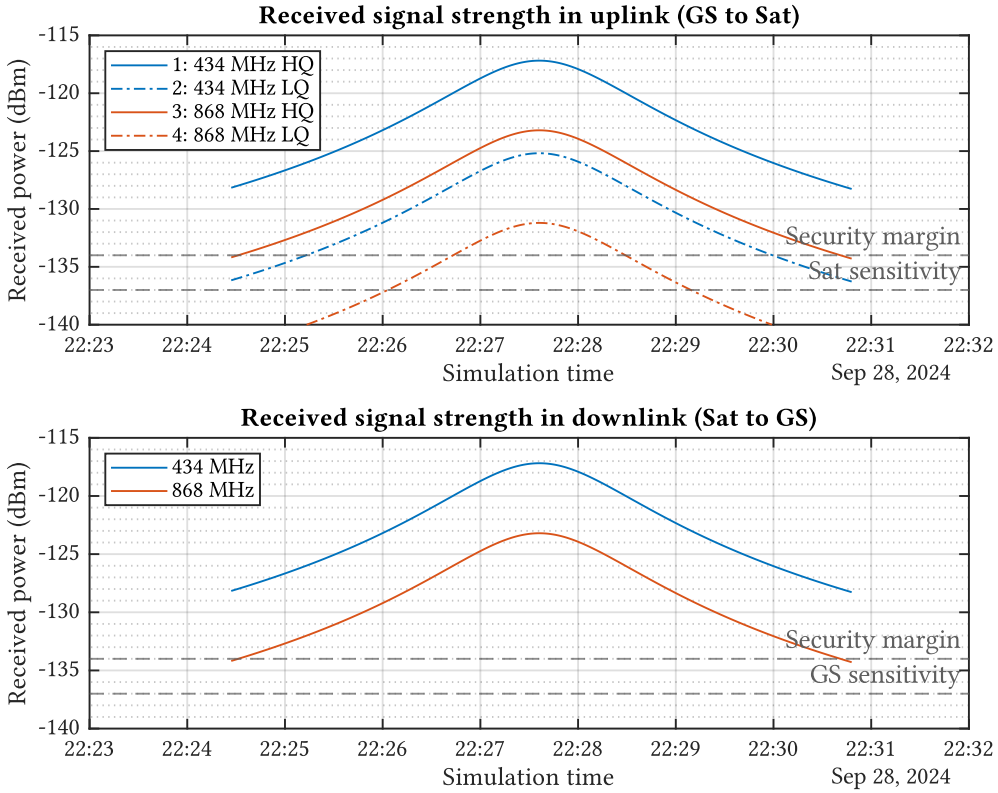


Figure 2.6 – Received signal power in uplink and downlink and compliance assessment.

Case	Frequency	TX power	Total losses	Received power	Compliance
1	435 MHz	30 dBm	158.2 dB	-128.2 dBm	**Yes**
2	435 MHz	22 dBm	158.2 dB	-136.2 dBm	**No**
3	868 MHz	30 dBm	164.2 dB	-134.2 dBm	**No**
4	868 MHz	22 dBm	164.2 dB	-142.2 dBm	**No**

Table 2.6 – Balance of power and losses for the worst case in the link budget and compliance assessment. Note: Compliance if $P_{RX} \geq S_{RX} + M$, sensitivity $S_{RX} = -137$ dB, margin $M = 3$ dB.

2.2.3.7 Carrier-to-Noise Ratio and compliance assessment

Carrier-to-Noise Ratio (CNR) is a measure of the quality of a link, defined as the ratio of the power of the modulated carrier signal to the power of noise within the receiver's bandwidth. CNR Compliance is achieved when the CNR at the receiver is greater than the minimum (−20 dB, see section 2.3.3, page 27) plus a security margin of 3 dB.

The simulation curves are plot in Figure 2.7 and the worst-case results are summarized in Table 2.7. In downlink, the CNR requirement is met in three out of four test cases due to the higher transmission power. In the uplink, only case 1 is compliant, where the 435 MHz carrier is used along the high quality terminal.

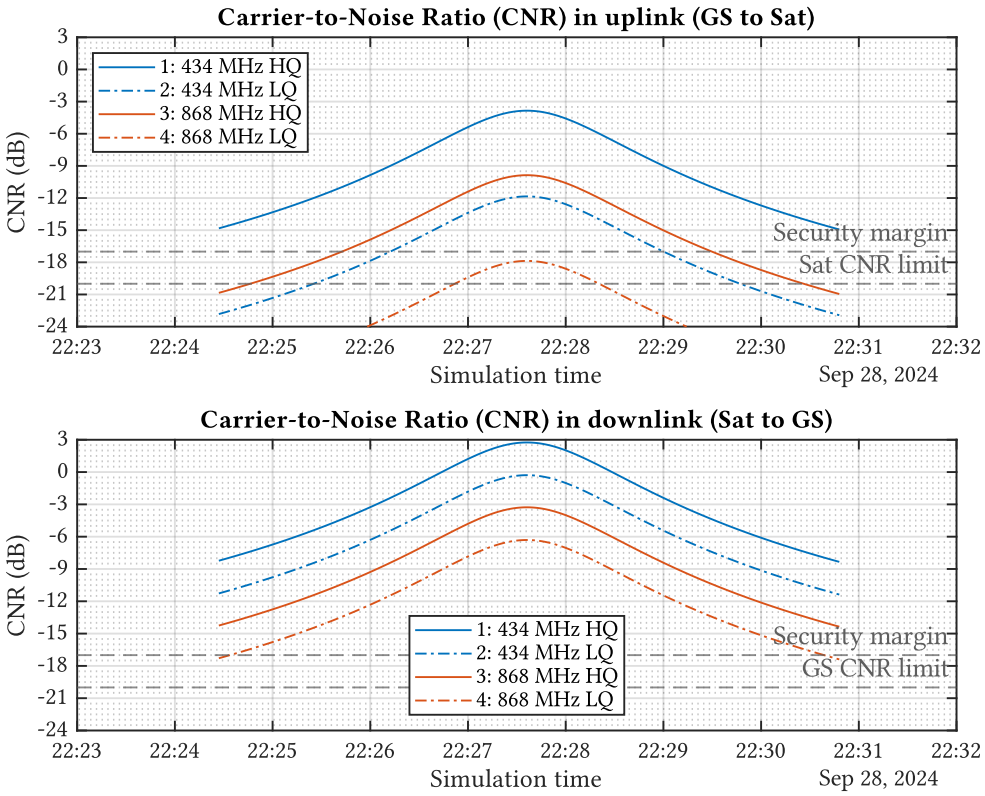


Figure 2.7 – Carrier-to-Noise Ratio in uplink and downlink and compliance assessment.

Direction	Case	Freq.	TX pwr	RX NF	Tot. loss	CNR	Compliance
Downlink TX: Sat RX: GS	1	435 MHz	30 dBm	3 dB	158.2 dB	-8.2 dB	**Yes**
	2	435 MHz	30 dBm	6 dB	158.2 dB	-11.3 dB	**Yes**
	3	868 MHz	30 dBm	3 dB	164.2 dB	-14.3 dB	**Yes**
	4	868 MHz	30 dBm	6 dB	164.2 dB	-17.3 dB	**No**
Uplink TX: GS RX: Sat	1	435 MHz	30 dBm	3 dB	158.2 dB	-14.8 dB	**Yes**
	2	435 MHz	22 dBm	3 dB	158.2 dB	-20.8 dB	**No**
	3	868 MHz	30 dBm	3 dB	164.2 dB	-22.8 dB	**No**
	4	868 MHz	22 dBm	3 dB	164.2 dB	-28.8 dB	**No**

Table 2.7 – Carrier-to-Noise Ratio for the worst case in the link budget and compliance assessment. Note: Compliance if $\mathrm{CNR}_{\mathrm{RX}} \geq \mathrm{CNR}_{\mathrm{lim}} + M$, limit CNR $\mathrm{CNR}_{\mathrm{lim}} = -20$ dB, margin $M = 3$ dB.

2.3 LoRa

LoRa is a proprietary wireless physical layer protocol (PHY). LoRaWAN is a communication protocol and network architecture. It defines the system architecture and communication protocols for LoRa networks. This section will present an overview of the fundamental principles of LoRaWAN and the LoRa modulation, along with a selection of the essential parameters required for LoRa PHY.

2.3.1 The LoRaWAN network architecture

Figure 2.8 shows the mainstream LoRaWAN network architecture. The LoRaWAN protocol controls the whole LoRa network and provides a data interface to the application server. There are three main entities in a LoRaWAN network [37], [39]:

- **The network server** manages the entire network. It is responsible for data consolidation, routing and security between end devices and application servers.
- **Gateways** serve as intermediaries, forwarding messages between end devices and the network server, and typically have no built-in intelligence. Because of this, gateways can consist of inexpensive hardware.

  Gateways typically have an IP backhaul over Ethernet, Wi-Fi or cellular networks. The network server communicates with the gateway using a traditional Internet connection, while the end devices communicate with the gateway by using LoRa.
- **End devices**, also known as nodes, are the edge IoT entities.

  End devices broadcast packets through LoRa PHY without assuming which gateway will receive them, and multiple gateways can receive the same packet without a performance penalty.

  Roaming from cell to cell is not required, no hand-off procedure is required. By default, LoRa uses Aloha as medium access control [84].

All components and protocols of the upper layers of the LoRaWAN network are available in open source implementations [37], but not the LoRa physical layer.

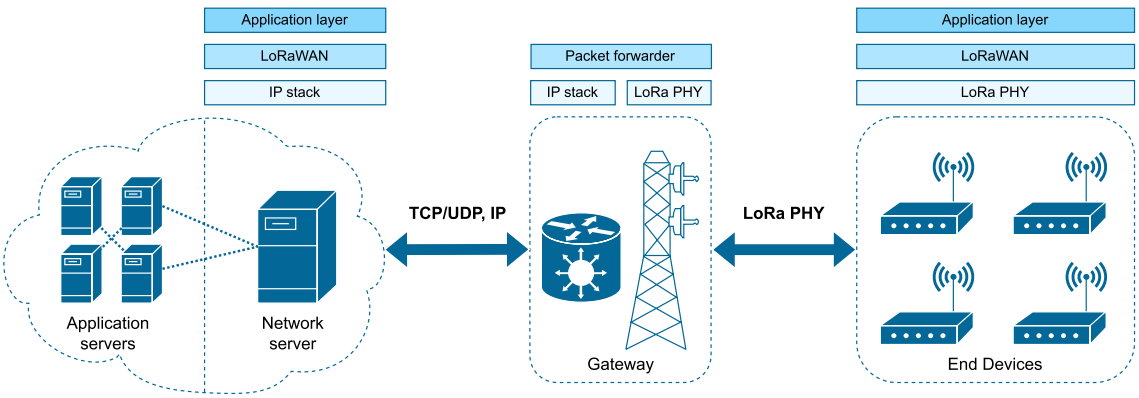


Figure 2.8 – Typical architecture of a LoRaWAN network and layer stack. The gateway forwards packet transmission requests from the server to the end devices and LoRa packets from the terminals to the network server. The radio link is the LoRa PHY, and the connection to the server is typically over an IP backbone. Based on [37], [84].

2.3.2 LoRa PHY

LoRa has been reverse engineered and described in several works [37], [38], [84]–[87], with varying degrees of success.

LoRa PHY employs a variation of the Chirp Spread Spectrum (CSS) modulation, which has been formally described in the literature by the term *Frequency Shift Chirp Modulation* (FSCM) [38]. The basic unit of communication is called *chirp*. A chirp is a frequency-swept sinusoidal carrier signal. If the frequency increases with time, it is an *up chirp*, otherwise it is a *down chirp*. The start frequency of the cyclically shifted symbol encodes the data. Figure 2.9 shows the base unshifted chirp and an arbitrary symbol.

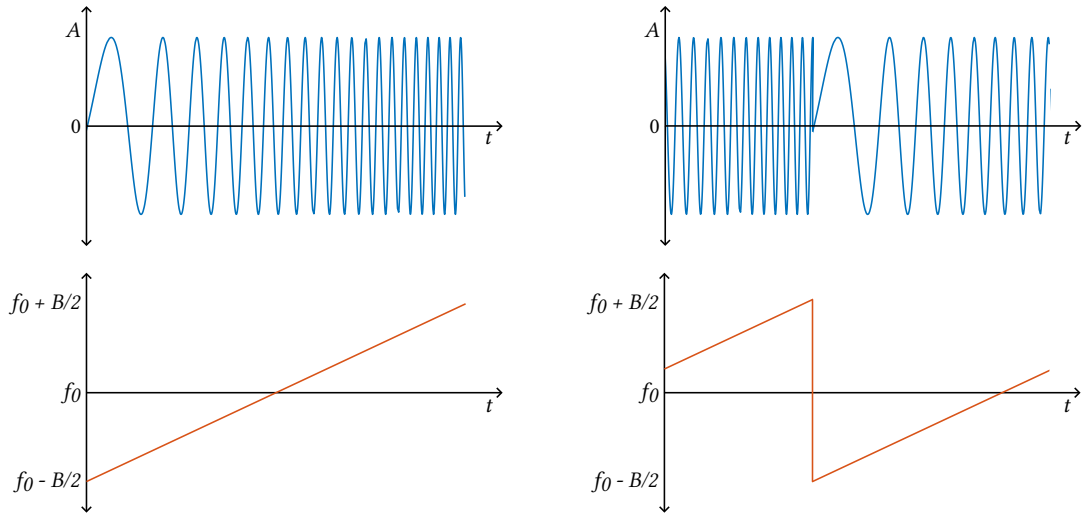
An up-chirp c can be mathematically represented in complex baseband as [37], [38]:

$$c(t, f_0) = A \cdot e^{\left(2\pi j \cdot \left[f_0 + \frac{B}{2T} \cdot t\right] \cdot t\right)} \tag{2.1}$$

where A is the amplitude, f_0 is the start frequency at $t = t_0$, B is the bandwidth and T is the symbol period. A down chirp is the conjugate c^*. Chirps are orthogonal to each other, *id est*, their cross-correlation is zero. The demonstration is non-trivial, and has been proved by [38]. The number of bits encoded by a symbol is equal to the spreading factor (SF). The SF satisfies $2^{\mathrm{SF}} = B \cdot T$. There are at most 2^{SF} combinations of up-chirps.

Figure 2.10 shows the spectrogram of a LoRa message. It has three parts [37]:

- **The preamble** is a series of base up-chirps for window alignment, followed by two more up-chirps symbols that specify the network ID.
- **The start frame delimiter (SFD)** is 2.25 down-chirps that mark the start of the data symbols.
- **The data symbols** include the header, the payload, and the payload CRC.



(a) Base up-chirp symbol.

(b) Arbitrary shifted up-chirp symbol

Figure 2.9 – Graphical representation in the time and time-frequency domains of a base up-chirp and an arbitrary symbol in bandpass.

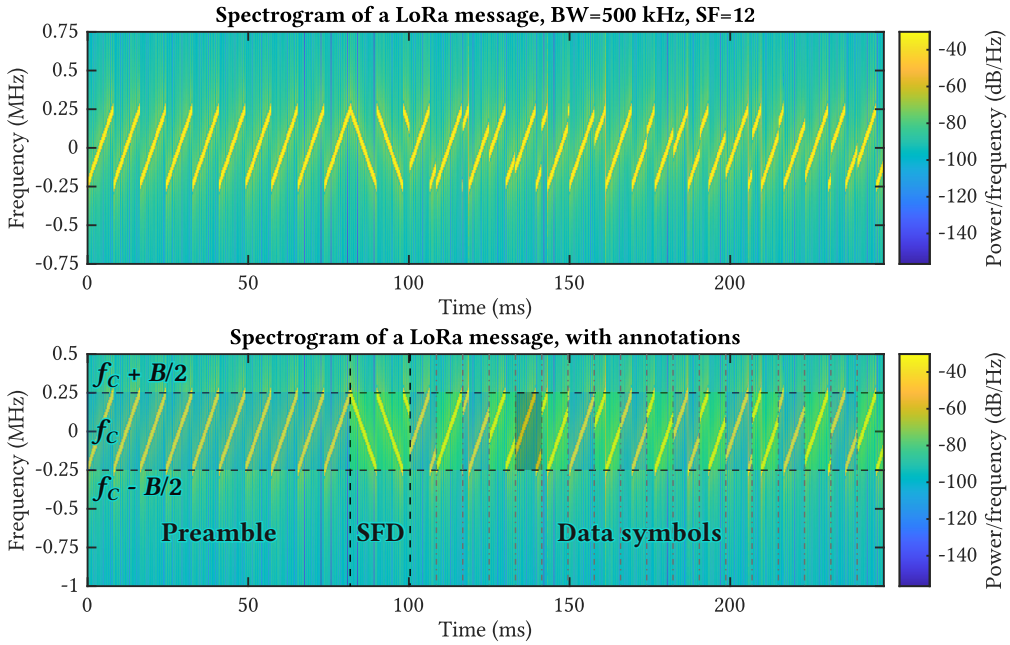


Figure 2.10 – Spectrogram of a LoRa message simulated in MatLab. Below, the message is annotated with the different parts of the frame: preamble, Start Frame Delimiter (SFD) and the data symbols. Notice how the chirps occupy all the available bandwidth. Simulator: [88].

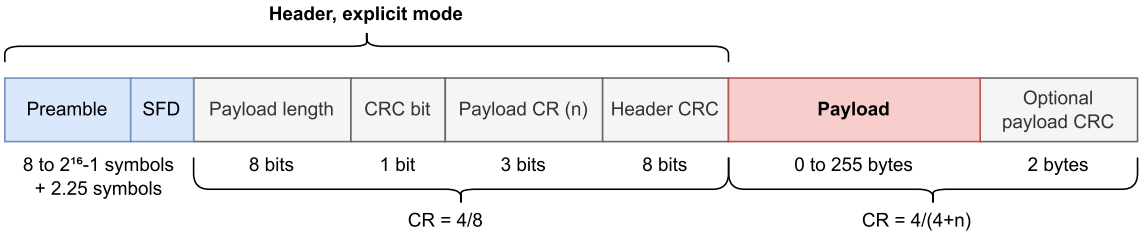


Figure 2.11 – LoRa PHY frame structure in explicit header mode. In implicit mode, only the preamble, SFD and payload are present. Based on [63], [84].

Figure 2.11 illustrates a LoRa PHY frame. The frame comprises a header, a payload, and, optionally, a 2-byte cyclic redundancy check (CRC) performed on the payload.

The header is not required in *implicit* mode. In *explicit* mode, an 8-bit field defines the length of the payload, a CRC bit indicates whether the optional payload CRC is present, a 3-bit field contains the coding rate (CR) used to encode the payload, and an 8-bit CRC is calculated on the header.

The payload ranges in size from 0 to 255 bytes. If using LoRaWAN, it encapsulates a LoRaWAN MAC frame [39], [84].

2.3.2.1 Demodulation and decoding

Figure 2.12 shows a diagram of the method for demodulation and decoding of LoRa.

LoRa receivers perform similarity checks of the incoming symbol in windows. Initially, the symbols of an incoming message and the receiver window are randomly misaligned. The preamble is then demodulated as if it were data symbols. The receiver will encounter the same symbol multiple times in a row, which alerts it. The value of the demodulated preamble symbols indicates the receiver how many samples it is misaligned from the message, and the window is adjusted for the incoming data symbols [38].

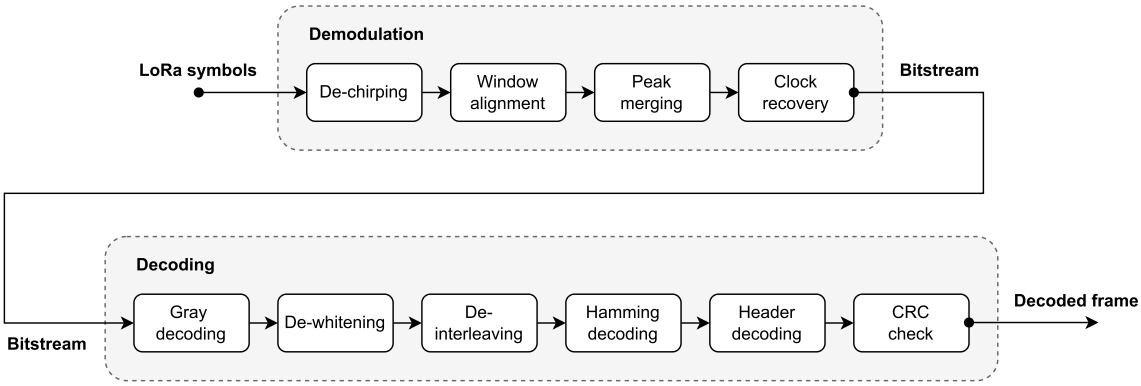


Figure 2.12 – Procedure for the demodulation and decoding of LoRa symbols. Based on [37].

To identify the incoming symbol, it would be necessary to perform a maximum likelihood analysis. Doing correlation similarity checks of the incoming symbol with the 2^{SF} possibilities is computationally burdensome. Instead, LoRa uses a mathematical trick to substitute the correlation by the FFT while yielding the optimum result [38].

First, it multiplies each received chirp with a base down-chirp. This operation is referred to as *dechirping*. Then, it performs the FFT, translating symbols to peaks in the frequency domain [37], [38]. *Peak merging* is an alternative enhanced method proposed in [37] to avoid distortions in the FFT resulting from phase misalignment occurring at the frequency discontinuities.

LoRa applies multiple coding techniques, see Figure 2.12. Symbols are coded using gray coding, a Hamming code of coding rate (CR) 4/5, 4/6, 4/7 or 4/8, and interleaving are introduced as forward error correction (FEC). A random sequence is used to whiten the data before being transmitted [37], [63]. This sequence is only known by official hardware but it has been reverse-engineered [37], [87], [88].

2.3.3 Selecting LoRa radio parameters

As demonstrated in section 2.2: Link budget simulations (page 15), losses of the order of 150 dB are typical in Earth-LEO radio links. Therefore, it is essential to optimize the available link budget. LoRa PHY can be adjusted to prioritize robustness over data rate. This section will assess the suitability of various configurations for the given scenario:

- **The spreading factor (SF)** sets the chirp rate and thus directly controls the speed of data transmission. SF is defined in the range from 6 to 12. A high SF is suitable for long distances because it improves the receiver's sensitivity. The drawback is increased power consumption and longer time-on-air. For every increase in spreading factor, the symbol rate is halved. Lower SF mean higher transmission rates and vice-versa. See Table 2.8 for the effect of SF on other parameters.

  In order to achieve extremely long ranges, high SF must be employed, which inevitably results in very low bitrates. As evidenced by the results of the section 2.2: Link budget simulations (page 15), it can be assured that the SF must be in the range of 10 to 12 to respect the established limits.

  The spreading factor also modifies the Doppler immunity of the receiver, see section 2.3.5: Frequency error sources and frequency stability (page 30).

  Spreading factors can also be used to control congestion, since they are orthogonal, *i. e.*, signals modulated with different spreading factors will not collide [82].

- **The bandwidth** (B) can be selected from three standard bandwidths: 125 kHz, 250 kHz or 500 kHz [89]. A larger bandwidth allows for higher data rates, but also spreads the transmitted power over a wider area, increasing the background noise power picked by the receiver, and thus worsens the SNR and the sensitivity.

  As it has been proved in section 2.2 (page 15), sensitivity and SNR are critical parameters with scarce margin. Therefore, 125 kHz is selected as the optimal value.

- **Receiver sensitivity** (S) is a function of the bandwidth, noise figure (NF) and the minimum required SNR [82]:

$$S = P_N + 10 \cdot \log_{10} B + \mathrm{NF} + \mathrm{SNR}_{\mathrm{min}} \tag{2.2}$$

  where P_N is the thermal noise power defined at $T = 293\,\mathrm{K}$ (20 °C) in a normalized bandwidth of 1 Hz:

$$P_N|_{\mathrm{dBm}} = 10 \cdot \log_{10}(kT) + 30 \approx -174\,\mathrm{dBm} \tag{2.3}$$

  where k is the Boltzmann constant ($1.380\,649 \times 10^{-23}\,\mathrm{J/K}$).

  In the absence of a noise figure, we will select 6 dB, which is a typical value for a LoRa receiver [63], [82]. It is possible to enhance the NF by incorporating an additional, previous LNA stage.

  On the other hand, the minimum required SNR depends on the selected SF, as illustrated in Table 2.8. The SNR values indicated in the table are Semtech's specification for an unknown bit error rate (BER) [63]. Figure 2.13 depicts the ideal BER as a function of SNR over an additive white gaussian noise (AWGN) channel for various spreading factors.

- **Coding rate (CR).** LoRa adds Forward Error Correction (FEC) to endure short interferences by encoding 4 bit data chunks with redundancies of $n = [1, 2, 3, 4]$ additional bits. The rise in CR decreases the data rate.

  Given the low bitrate, the addition of high redundancy will only exacerbate the problem. Accordingly, the decision was made to maintain a CR = 4/5 ($n = 1$).

- **Data rate.** The achievable transmission speed, in bits per second [82]:

$$R_b = \frac{\mathrm{SF} \cdot \left(\frac{4}{4+n}\right)}{\left(\frac{2^{\mathrm{SF}}}{B}\right)} \tag{2.4}$$

  where n is the number of redundancy bits added by the coding rate. See Table 2.8 for a summary of the achievable bitrates depending on the rest of the parameters.

- **Low Data Rate Optimization (LDRO).** When sending packets with a considerable symbol period (SF $\geq$ 11), LDRO mode must be enabled for better stability [63]. LDRO reduces the modulation alphabet to allow better synchronization and tracking on the receiver. It also increases the tolerance to multipath delays [89].

- **Header mode** shall be explicit, to include the header in the message and benefit from the built-in functionality and error detection capabilities within the LoRa ICs.

Spreading factor (SF)	Minimum SNR	Bitrate ($CR = 4/5, B = 125$ kHz)	Sensitivity ($B = 125$ kHz, $NF = 6$ dB)
6	-5.0 dB	9375 bps	-122 dBm
7	-7.5 dB	5468 bps	-124 dBm
8	-10.0 dB	3125 bps	-127 dBm
9	-12.5 dB	1757 bps	-129 dBm
10	-15.0 dB	976 bps	-132 dBm
11	-17.5 dB	537 bps	-134 dBm
12	-20.0 dB	292 bps	-137 dBm

Table 2.8 – Relation of the spreading factor with the minimum required SNR, bitrate and sensitivity for a coding rate $CR = 4/5$, bandwidth $B = 125$ kHz and noise figure $NF = 6$ dB. The SNR values are Semtech's specification for an unknown BER [63].

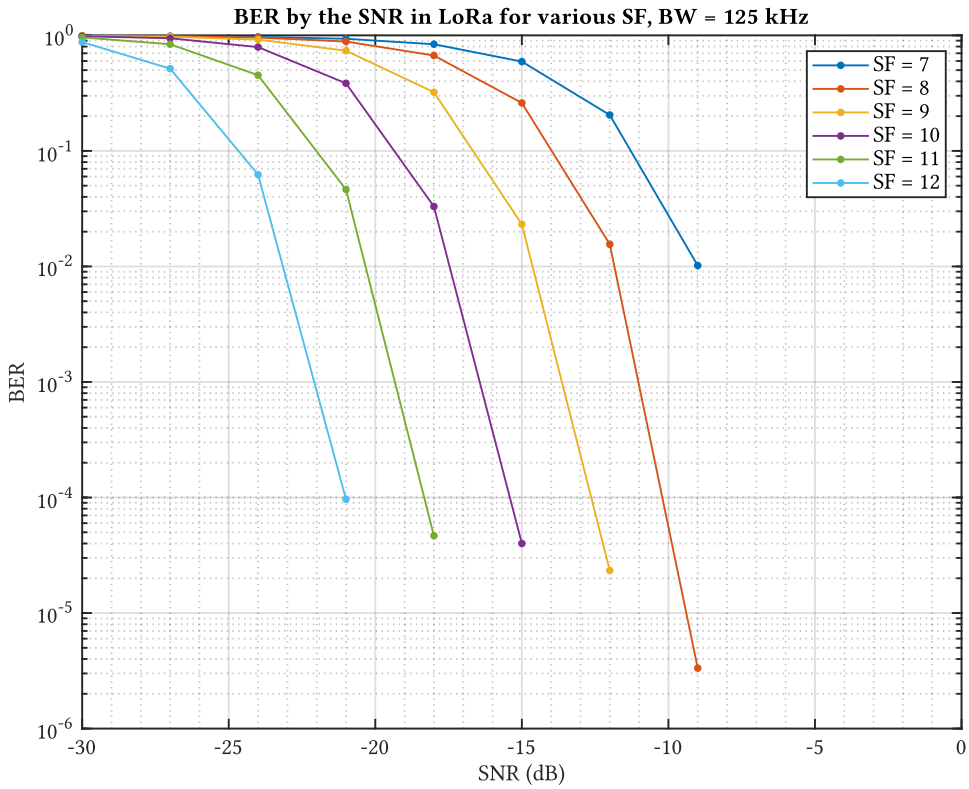


Figure 2.13 – Simulation of the ideal bit error rate (BER) achieved in LoRa as a function of signal-to-noise ratio SNR over an additive white gaussian noise (AWGN) channel for various spreading factors (SF) and a fixed bandwidth of $B = 125$ kHz.

2.3.4 Time-on-air

Time-on-air (ToA) is the duration of LoRa packet while being transmitted [82]. It is the sum of the duration of the preamble, start frame delimiter (SFD) and data symbols:

$$\begin{aligned} T_{\text{pkt}} &= T_{\text{pre}} + T_{\text{SFD}} + T_{\text{data}} \\ T_{\text{pkt}} &= \left(n_{\text{pre}} + 2 + 2.25 + n_{\text{data}}\right) \cdot T_{\text{s}} \end{aligned} \tag{2.5}$$

where the symbol period is $T_s = 2^{\text{SF}}/B$ and the number of data symbols is [84], [90]:

$$n_{\text{data}} = 8 + \max\left[\text{ceil}\left(\frac{8 \cdot n_{\text{payl}} - 4 \cdot \text{SF} + 8 + 16 + 20 \cdot b_{\text{H}}}{4(\text{SF} - 2 \cdot b_{\text{LDRO}})}\right) \cdot (n_{\text{CR}} + 4) \quad , \quad 0\right] \tag{2.6}$$

where the $n_{\text{payl}} = 255$ bytes is the payload length, $n_{\text{CR}} = 1$ is the coding-added redundancy bits, $b_{\text{H}} = 1$ indicates wether the header is present or not, and $b_{\text{LDRO}} = [0, 1]$ indicates if Low Data Rate Optimization (LDRO) is active (mandatory for $SF \geq 11$).

The results of the time-on-air analysis are presented in Table 2.10 with the aforementioned configuration for a range of spreading factors and bandwidths.

2.3.5 Frequency error sources and frequency stability

The maximum allowed frequency error is a quarter of the bandwidth, regardless of the LoRa IC [91]. For the worst case of 125 kHz, the maximum tolerated drift is 31.2 kHz.

Frequency of operation is $f_c = 435$ MHz. Standard-quality 32 MHz TCXO crystals with a ±25 ppm drift are used in the mini ground stations, as it is typical in end devices [92]. The satellite employs GNSS-grade 32 MHz crystals with a ±5 ppm tolerance [93].

Table 2.9 enumerates the sources of frequency error. The sum is 23.1 kHz, which affords a margin of 8.1 kHz with respect to the 31.2 kHz limit. In the hardware design sections, crystals will be selected according to these results.

In addition to this analysis, we must calculate whether if the frequency stability requirements during packet transmission are satisfied. The SX127x series allow a maximum Doppler drift during a packet transmission of [42], [91]:

$$\Delta f_{\text{d,pkt,max}} = \frac{L \cdot B}{3 \cdot 2^{\text{SF}}} \tag{2.7}$$

Where $L = 16$ if LDRO is enabled and $L = 1$ otherwise. The maximum permissible Doppler drifts are listed in Table 2.10. The most restrictive scenario occurs when SF = 12. In order to assess compliance, it is necessary to calculate the overall change in frequency from the beginning to the end of a packet, which is defined as [42]:

$$\Delta f_{\text{d,pkt}}(t) = f_{\text{d}}(t + T_{\text{pkt}}) - f_{\text{d}}(t) \tag{2.8}$$

where $f_{\text{d}}(t)$ is the Doppler frequency shift (see section 2.2.3.2, page 19) and T_{ptk} is the ToA. Figure 2.14 depicts the Doppler frequency rate for various spreading factors and bandwidths. As the ToA increases, the Doppler rate of a packet also increases.

The limits are exceeded in $B = 125$ kHz for SF ≥ 11, even with the LDRO flag enabled, which restricts us to using SF = 10 or lower. With $B = 500$ kHz issues are completely avoided. However, this situation presents a challenge in terms of the link budget. In section 2.4 (page 33), the results are discussed and solutions are proposed.

Source	Tolerance @ 435 MHz	Frequency drift
Gateway XTAL	±5 ppm	±2.2 kHz
End device XTAL	±25 ppm	±10.9 kHz
Doppler shift	±23 ppm	±10.0 kHz
	Total drift:	**±23.1 kHz**

Table 2.9 – List of contributions to frequency error.

B	SF	LDRO	Bitrate	Symbol period	ToA	Limit packet Doppler	Worst packet Doppler	Compliance
500 kHz	10	Off	3.9 kbps	2.1 ms	0.6 s	2604 Hz	101 Hz	**Yes**
	11	On	2.1 kbps	4.1 ms	1.3 s	1302 Hz	250 Hz	**Yes**
	12	On	1.1 kbps	8.2 ms	2.3 s	651 Hz	428 Hz	**Yes**
125 kHz	10	Off	976 bps	9.2 ms	2.3 s	651 Hz	372 Hz	**Yes**
	11	On	537 bps	16.4 ms	5.0 s	325 Hz	929 Hz	**No**
	12	On	292 bps	32.8 ms	9.0 s	168 Hz	1670 Hz	**No**

Table 2.10 – Time-on-air and maximum allowed Doppler drift for different spreading factors and bandwidths, using $CR = 4/5$, explicit header, payload of 255 bytes and 8 preamble symbols.

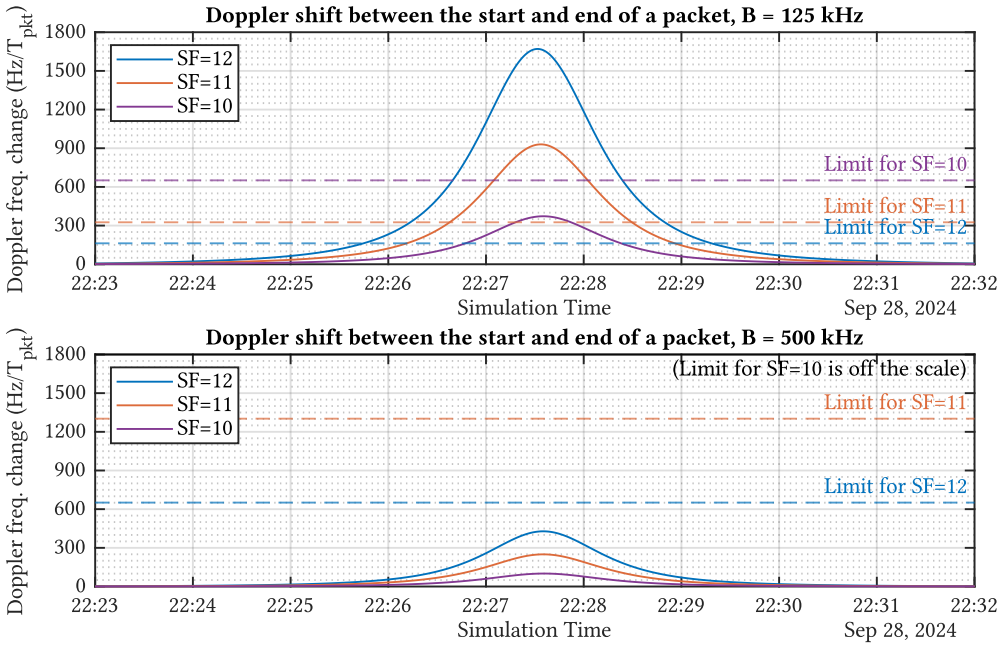


Figure 2.14 – Simulation of the absolute Doppler frequency change between the start and end of the transmission of a packet, for different spreading factors.

2.3.6 Data budget and medium access control

The data budget is the analysis of the amount of data that can be sent over a communication link. The data budget in a LoRa network is a complex topic that cannot be solved with analytical expressions due to the many variables involved [94]–[96]. This section is limited to an introduction to the problem and some initial approximations.

LoRaWAN defines 3 types of devices according to their medium-access control (MAC): class A, B and C. Class A devices use ALOHA for the uplink and after sending a frame, a end device listens during a short window. Class B devices use slotted ALOHA and are synchronized using beacons sent by the gateway to schedule additional windows for downlink. Class C devices are always listening, except when transmitting.

In LoRa, different data rates are orthogonal to each other and can coexist. It is possible to exchange multiple frames on the network simultaneously without collision, provided that each is sent with different spreading factors and/or bandwidths [82].

The satellite LoRa gateway is implemented by a SX1302 IC (see section 3.3: Hardware architecture, page 41). The SX1302 embeds different receiver modems [93]:

1. 8 multi-SF modems handling a SF from 5 to 12 and a fixed bandwidth of 125 kHz.
2. 8 multi-SF modems handling a SF from 5 to 10 and a fixed bandwidth of 125 kHz.
3. 1 multi-BW modem handling 125, 250 or 500 kHz. and a single, fixed SF.

Each modem can be assigned to a different frequency channel and, because they are orthogonal, channels with different SFs can overlap. In modem types 1 and 2, all SFs are demodulated in parallel [93]. In the context of the mission, SX1302's type 1 modems can decode SF 10, 11 and 12 packets simultaneously, while type 2 modems can only operate on SF 10. Lower SF packets are highly unlikely to reach the satellite.

The SF 11 and 12 configuration with a bandwidth of 125 kHz does not meet the Doppler rate requirements, and the SF 10 may not satisfy the power balance in the entire access window, but for the purpose of evaluating the possible configurations, these facts are ignored. Another limitation is the half-duplex mode and the single transmit channel in the SX1302, which results in disparate uplink and downlink capacities.

The limited access window results in a high concurrent usage by many users. If the ground terminals are correctly assigned a frequency and spreading factor, the SX1302 could theoretically detect 32 packets from 32 different users sent simultaneously: type 1 modems would decode spreading factors 10, 11 and 12 on 8 channels, while type 2 modems would decode SF 10 on 8 completely different channels. The total used bandwidth is $125\,\text{kHz/ch} \cdot 16\,\text{ch} = 2\,\text{MHz}$, which fits in the selected $435 - 438\,\text{MHz}$ band.

The ToA of packets differ due to different spreading factors (see Table 2.10). Once received, packets are placed in a FIFO queue for processing. Generating a response takes the chatbot about 7 s [97]. In the worst case, an unlucky user would wait:

$$2 \cdot T_{\text{air, SF=12}} + T_{\text{FIFO, } n=31} + T_{\text{proc}} = 2 \cdot 9\,\text{s} + 31 \cdot 7\,\text{s} + 7\,\text{s} = 242\,\text{s} \equiv 4\,\text{min}\ 2\,\text{s} \tag{2.9}$$

This is suboptimal, even without considering collisions in a user pool larger than 32. The current solution is not scalable. Reducing the processing time and the ToA is crucial. Slotted ALOHA or novel scheduling algorithms such as SALSA [41] should be implemented. Rate limits should be incorporated into the ground stations for further collision avoidance. The results are discussed in the next section.

2.4 Discussion

The design of a radio link is a delicate balance between many variables, including transmission speed, power, noise, complexity and cost. The developed simulations offer a convenient means of reassessing potential changes in orbit, LoRa or link parameters.

The power balance of the link budget results demonstrate that communication between ground and low orbit at low power is feasible with LoRa without the use of directive antennas or tracking. However, it comes at the cost of an extremely low bitrate. Moreover, additional hardware such as extra LNA and PA are required in both the ground and space segments to compensate for the deficiencies of the LoRa modems. High-quality custom-built hardware is necessary, as many off-the-shelf LoRa modules will be unable to work with the current constraints. Pluton UPV has already started the development of a prototype for the ground terminals in accordance with these results.

Isotropic antennas are considered in the simulations to evaluate a worst case, since the radiating elements of the *Estigia* mission are not yet defined. To increase the link budget, it would be of interest to design antennas for the ground terminals with ~ 2 dBi of gain and a wide beamwidth ($\sim 150^{\circ}$) so that users do not have to point to the satellite. An assessment of the antenna systems is currently being conducted by Pluton UPV.

The main challenges to be addressed are access, bitrate, and Doppler, and they are interdependent. Given the limited time per pass, it is crucial to optimize response time. The primary contributor to delay is the on-board AI, which will be addressed through software optimizations, parallel processing, and hardware enhancements to the AI payload. The second contributing factor is the extremely low bitrate, which results in a time-on-air time of up to 9 seconds per 255-byte packet. Long transmissions present a variety of problems, including Doppler rate issues, high channel utilization, increased power consumption, higher collision probability and reduced user capacity per pass.

It is necessary to enhance the bitrate and reduce the time-on-air by adjusting the LoRa parameters. This will inevitably reduce the available link budget. It is important to acknowledge that the performed link budget is pessimistic and conservative; therefore, trade-offs can be made. A set of possible remedies are discussed below:

- While maintaining a bandwidth of 125 kHz, reducing the SF to 10 would greatly increase the data rate and reduce the time-on-air, thus solving other problems mentioned above. However, it will also degrade the sensitivity and SNR.
- Automatic bitrate adjustment, also known as Adaptive Data Rate (ADR), adds overhead and complexity and is not advised for mobile devices [98].
- Increasing the bandwidth enhances the data rate and Doppler immunity at the cost of SNR and sensitivity. However, this is not feasible since LoRa gateways lack the capability of parallel decoding of 250 kHz and 500 kHz channels.
- Another option is to limit the payload length to reduce the time on air. Long messages would be split into multiple packets. This would solve Doppler rate problems but increase overhead, delay, and collision probability.
- An alternative solution would be to use the LR11xx series [65] instead of the SX127x on the end devices, which present a higher level of immunity to Doppler [91], removing a variable from the problem. This option has not been considered in this project at this time due to its recent introduction to the market and the current lack of first and third party documentation and open source implementations.

Chapter 3

Specifications

Once the objectives have been defined and the radio link constraints have been examined, the specification process can commence. The specification settles the requirements, limitations and functions of the device under development at varying levels of abstraction. The requirements are the foundation for the design strategy. Once an iteration is completed, the requirements must be validated. It is not expected that all of the requirements outlined here will be met by the end of this first master's thesis.

3.1 Payload requirements

A requirement specification is a set of requirements that a product must satisfy. A functional specification describes the functions a product is expected to perform [99]. This section defines the requirement specification and functional requirements that the payload must fulfill. The specifications are arranged in Table 3.1, following the guidelines and good practices found in [100].

3.1.1 Mission-specific scope and requirements

As part of Pluton UPV's *Estigia* mission, this device shall be designed to be used in a CubeSat platform flying in LEO, and shall enable users on the ground to communicate with the satellite via short text messages using LoRa as physical layer protocol. The device, its functions, and the design process shall be documented in detail, including schematics, prints, diagrams, blueprints, reports, and manuals.

Given the group's lack of prior experience in satellite development and limited resources, overly complex designs will be avoided, in order to mitigate risks such as delays or cost overruns. The group decided that the engineering model should have a modular approach to segment the development effort and facilitate the debugging process. This way, parts can be updated independently, and if one of the modules fails, only that module is replaced.

3.1.2 Communications

3.1.2.1 Protocols

The layer 1 protocol is LoRa PHY with explicit header. A layer 2 protocol, either LoRaWAN based or custom, shall be inserted in the payload field to encapsulate the text messages. This aspect has yet to be defined (TBD) by Pluton UPV.

3.1.2.2 Frequency allocation and power limits

The 435 – 438 MHz band has been chosen to apply for the *Estigia* mission, as studied in section 2.1: Telecommunications regulations (page 13).

According to ITU-R regulations, the power flux density (PFD) for the amateur-satellite service in the specified band must not exceed $-187\,\mathrm{dB/(m^2{\cdot}Hz)}$ [59], [101]. With the current orbit and radio link assumptions, the PFD is estimated to be $-204\,\mathrm{dB/(m^2{\cdot}Hz)}$. However, the definitive study of power limits will await the full definition of the radiating elements of the mission and are marked as to be resolved (TBR).

3.1.2.3 Radio link requirements

In accordance with the results of section 2.2: Link budget simulations (page 15) and the section 2.3.3: Selecting LoRa radio parameters (page 27), the requisite power output is 30 dBm, the sensitivity shall reach −137 dBm with $B = 125$ kHz and SF 12. Additionally, the device shall ensure a noise figure (NF) of 3 dB or less, and shall maintain insertion losses of 3 dB or less in the receiving and transmitting paths in all the operating band.

The system shall allow reconfiguration of the carrier frequency, output power, bandwidth, SF, LDRO, CR, preamble length, network ID, LoRa PHY header and header mode.

3.1.3 Microcontroller

In order to process the radio data and interface with the rest of the satellite, an intermediary is required. The most simple approach is to use a microcontroller (MCU).

In accordance with the preferences of Pluton UPV, the MCU should be an ST Microelectronics STM32. In order to process incoming data, it is estimated that a microcontroller with an ARM Cortex M4 or superior should be used, with a clock speed of at least 32 MHz, 512 kB of Flash memory, and 256 kB of RAM. These assumptions are made based on existing hardware designs [102]–[106].

The required peripherals are two CAN (for SpaceCAN [31]), two SPI and two I2C (one SPI and I2C per LoRa module), one USB and one UART (serial interface with a PC) and one SWD (debug and programming). See section 3.3: Hardware architecture (page 41) for more details. Peripherals shall be allocated avoiding pin collisions. The MCU shall monitor the electronics and diagnose problems through the remaining GPIOs.

3.1.4 Power system and consumption constraints

The device shall be equipped with a power conversion and distribution system sized for its requirements. Power for the motherboard is provided by a 5 V rail that can be derived from either the USB or the CubeSat bus. The power conversion should be done using DC/DC converters for efficiency. Special attention shall be given to filtering its switching noise. The maximum power consumption during operation shall be limited to 5 W. The payload shall implement a shutdown mode and a sleep mode.

3.1.5 Form factor

The payload will be divided in two PCBs: A module will implement the LoRa gateway and a motherboard will interface with the rest of the CubeSat. The modules shall meet the mPCIe form factor (Figure 3.1). The motherboard shall conform to the CSKB PC/104 form factor [3], [4], [24] (Figure 3.2), the *de facto* standard for CubeSats [13].

3.1.6 Interfaces

3.1.6.1 Radio-Frequency ports

RF I/O ports shall use a female MMCX, a widely-used coaxial socket [13], [108].

3.1.6.2 Programming and debug

The devices should be easy to program and debug by using proven technologies such as SWD or JTAG. The debug port will be a FTSH-105 compatible male header, and optionally a TC2030. In addition, test points shall be made available for relevant signals.

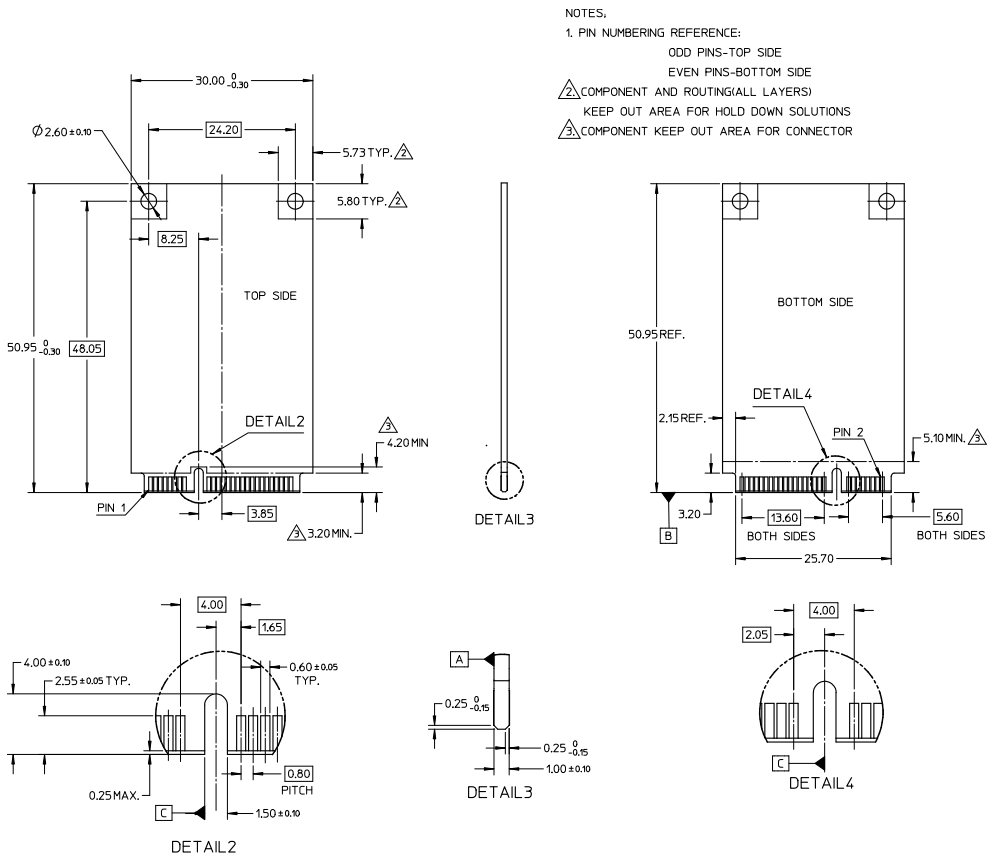


Figure 3.1 – mPCIe PCB form factor. Units in mm. Extracted from [107] (modified).

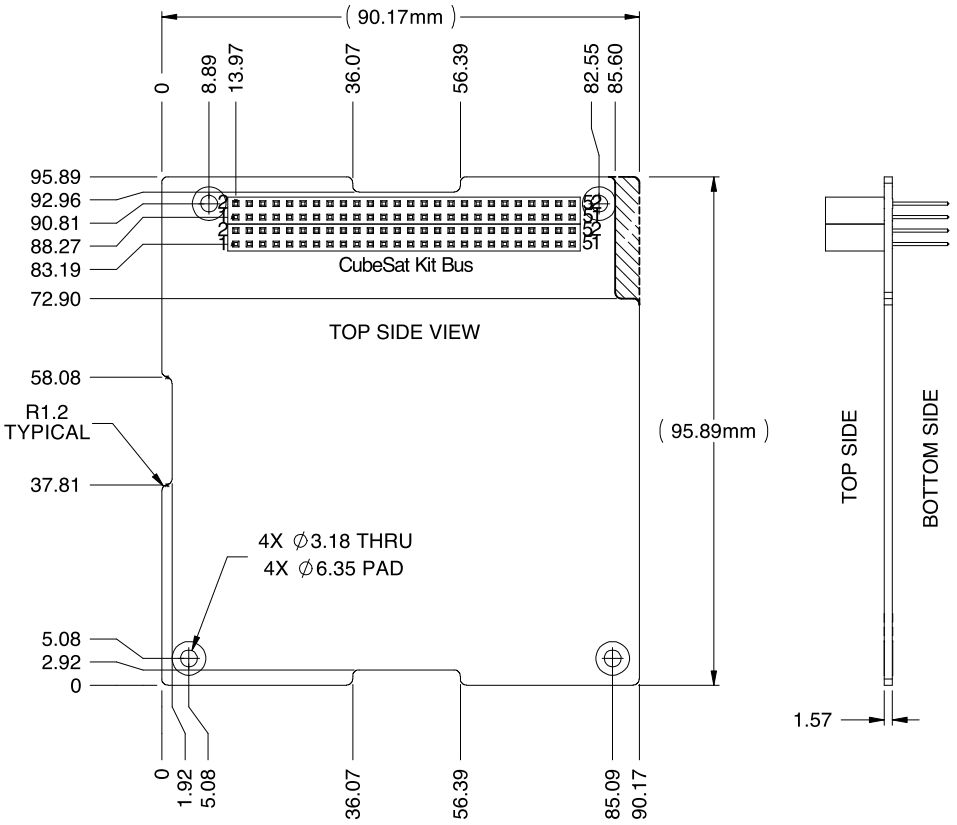


Figure 3.2 – CubeSat CSKB PC/104 form-factor. Units in mm. Extracted from [24] (modified).

3.1.6.3 Interconnections between boards

A PC/104, CSKB-compatible, Samtec SSQ-126-04-like connector [109] will be utilized as the CubeSat bus headers. It is a regrettable fact that there is a lack of standardization in the CubeSat bus pinout, protocols, and signals. It is customary in this sector to define custom-made pinout per-mission. The LibreCube board specification of 2022 will be used as basis [110], [111]. The pinout is specified in Table 3.8 (section 3.5, page 51). This definition takes into account the rest of the hardware to be embarked, which are currently under NDA. Conversely, a customized pinout will be defined for the modules' mPCIe connector (see Table 3.7 in section 3.5, page 51). The mPCIe standard is only respected in terms of the form factor.

The pinouts are subject to change if required.

3.1.7 Protection systems

Sensitive electronics should be shielded from radiation as measure against electromagnetic interference (EMI), ensuring electromagnetic compatibility (EMC) with the rest of the satellite's components.

Methods shall be implemented to prevent electrostatic discharges (ESD) from damaging the electronics through the external ports. Over-current and over-voltage protection measures shall be put in place. Each PCB shall contain at least one temperature sensor.

3.1.8 Materials

Even if the developed engineering model is not going to be tested in space conditions, certain considerations must be taken into account in its materials.

The PCB substrate shall be rated for $T_g \geq 453\,\mathrm{K}$ (180 °C). Due to the relatively large wavelength of the carrier frequency, the substrate can be FR-4 without degrading the signal. PCB surface finish should be electroless nickel immersion gold (ENIG). Aluminum of the RF shields should be anodized. All materials shall adhere to the Restriction of Hazardous Substances (RoHS) normative [112] and shall be safe to manipulate.

3.2 EGSE requirements

The Electrical Ground Support Equipment (EGSE) is an auxiliary system that will be connected to the payload, exclusively designed for its testing. The EGSE will transmit control signals that imitate the actual satellite traffic generated by the OBC or the AI payload. This enables for the execution of tests to verify and validate the functionality of the LoRa payload. Additionally, it will contain a LoRa end-device transceiver to simulate a ground terminal. The RF path will be configurable in attenuation to emulate the FSPL.

To reuse design efforts and given the similarity of the technical requirements, the EGSE will utilize a MCU identical to the one used in the payload. The communication and debug ports will be identical.

The system is also responsible for powering the payload via the CubeSat bus, for which it needs a method of power measurement and control. The power consumption of the EGSE is not constrained, but it should consume no more than 5 W.

The EGSE PCB is not subject to the constraints imposed by space conditions and can make use of standard materials and components.

The EGSE-specific requirements are summarized in Table 3.2.

Area	Req. ID	Requirement Description
Mission	P-1	To develop an engineering model of the LoRa Communications Payload for the *Estigia* CubeSat.
	P-1.1	It should integrate off-the-shelf electronic components and use standard procedures and practices for the manufacturing and assembly.
	P-1.2	The product and functions and the design process shall be documented in the form of schematics, prints, diagrams and reports.
Comms	P-2	To design a communications system that functions as a LoRa PHY gateway and it is capable of Earth-LEO communications.
	P-2.1	The device shall meet the international communications normative.
	P-2.1.1	The device shall operate at the 435 − 438 MHz frequency band.
	P-2.1.2	[TBR] The PFD shall not exceed $-187\,\mathrm{dB/(m^2{\cdot}Hz)}$.
	P-2.2	The device shall fulfill operating parameters in order to provide the adequate link quality studied on the link budget.
	P-2.2.1	The device shall present a noise figure (NF) of 3 dB or less.
	P-2.2.2	The device shall have insertion losses of 3 dB or less in RX and TX.
	P-2.2.3	The device shall be capable of emitting an RF power of 30 dBm or more, before taking into account insertion losses.
	P-2.2.4	The receiver sensitivity shall reach −137 dBm when configured with a bandwidth of 125 kHz and a spreading factor of 12.
	P-2.2.5	The device shall maintain its RF properties in the whole operation band and with a bandwidth of 125 kHz, 250 kHz or 500 kHz.
	P-2.3	The device must allow reconfiguration of its parameters: carrier frequency, output power, bandwidth, SF, LDRO, CR, preamble length, network ID, LoRa PHY header and header mode.
Mechanical	P-3	To provide a compliant device with existing mechanical standards and the space environment.
	P-3.1	The hardware design of the payload will follow a modular approach of two interconnected printed circuit boards. A module will implement the LoRa gateway and a motherboard will interface with the satellite.
	P-3.1.1	The motherboard shall meet the CubeSat PC/104 CSKB form factor.
	P-3.1.2	The modules shall meet the mPCIe form factor.
	P-3.2	[TBR] PCB substrate shall be rated for $T_g \geq 453\,\mathrm{K}$ (180 °C)
	P-3.3	All screws shall follow the metric standard, hexagonal or *torx*.
Electrical	P-4	To design circuit boards that implement the required functionality and are suitable for the space environment.
	P-4.1	The PCB ports will adhere to the following standards.
	P-4.1.1	A SSQ-126-04-compatible connector will be used for the CubeSat bus. The pinout will be custom, but based on the LibreCube spec.
	P-4.1.2	A mPCIe connector will be used for the module-motherboard interconnection. The pinout will be custom.
	P-4.1.3	RF input/output port shall use a MMCX female socket connector.
	P-4.1.4	SWD port shall use a FTSH-105-compatible connector.
	P-4.1.5	Test points shall be provided for the purpose of inspecting the power rails and other relevant signals.
	P-4.1.6	One or more serial interfaces will be made accessible via ports.
	P-4.2	The MCU should be an STM32, ARM Cortex M4 or superior, with a clock speed of at least 32 MHz, 512 kB of Flash memory, and 256 kB of RAM.
	P-4.2.1	The required peripherals in the MCU are: 2xCAN, 2xSPI, 2xI2C, 1xUSB, 1xUART and 1xSWD. Each peripheral shall be located in independent pins.
	P-4.2.2	The microcontroller shall have access to signals which allow to monitor the electronics and diagnose problems.
	P-4.3	The device shall be equipped with a power conversion and distribution system that is tailored to its specific requirements.

Continued on next page

Table 3.1 – Requirement description for the payload.

Continued from previous page

Area	Req. ID	Requirement Description
Electrical	P-4.3.1	[TBR] The power consumption in operation shall not exceed 5 W.
	P-4.3.2	The device shall be equipped with a sleep and a shutdown mode.
	P-4.3.3	The motherboard power supply is fed using a 5 V rail, which may be derived from either the USB or the CubeSat bus.
	P-4.3.4	The power conversion should be performed using DC/DC converters with special attention to filtering noise.
	P-4.4	The device shall implement onboard protection systems.
	P-4.4.1	Sensitive electronics should be shielded.
	P-4.4.2	ESD protections shall be implemented in the external ports.
	P-4.4.3	The device shall implement OC and OV protections.
	P-4.4.4	Each PCB shall contain at least one temperature sensor.
	P-4.4	In the modules, GND will be connected to the mounting holes. In the motherboard, the mounting holes will be isolated.
	P-4.5	Two modules will be mounted in the same motherboard.
	P-4.6	[TBR] Circuit elements should exhibit low tolerances and should be resilient to temperatures of 100 °C or more.
	P-4.7	Components and fabrication shall adhere to the RoHS normative.
	P-4.8	Manufactured electronics shall not emit abrasive, toxic or harmful substances and shall not be dangerous to manipulate.
	P-4.9	All board perforations shall be through-hole. The use of blind, buried or tented vias is prohibited.

Table 3.1 – Requirement description for the payload.

Area	Req. ID	Requirement Description
EGSE	E-1	To develop the EGSE, a support equipment for testing the Payload.
	E-1.1	The EGSE shall meet mission requirements P-1.1 and P-1.2.
	E-1.2	The EGSE shall meet communications requirements P-2.1.1, P-2.2, P-2.2.1, P-2.2.2, P-2.2.3, P-2.2.4, P-2.2.5 & P-2.2.6.
	E-1.3	The EGSE shall share the same CubeSat bus pinout as the payload.
	E-1.4	The EGSE shall provide mechanical support for the payload.
	E-1.5	PCB substrate will be standard FR-4
	E-1.5.1	PCB substrate shall be rated for $T_g \geq 423\,\text{K}$ (150 °C)
	E-1.6	The EGSE shall fulfill P-4.1.1, P-4.1.3, P-4.1.4, P-4.1.5 and P-4.1.6
	E-1.7	The MCU should be the same model as the Payload's (Req. P-5.2)
	E-1.7.1	The required peripherals in the MCU are: 2xCAN, 1xSPI, 1xI2C, 1xUSB, 1xUART and 1xSWD. Each peripheral shall be located in independent pins.
	E-1.8	The EGSE shall implement the hardware of a LoRa end-device.
	E-1.8.1	The EGSE shall incorporate a chain of variable attenuators to simulate FSPL from a minimum of 40 dB up to 120 dB or more.
	E-1.9	The device shall be equipped with a power conversion and distribution system sized to its requirements.
	E-1.9.1	The motherboard power supply is fed using a 5 V rail from either a USB and shall feed 5 V to the payload.
	E-1.9.2	Current sense and power switches must be implemented to monitor and control the power supply to the payload.
	E-1.9.3	The power conversion should be performed using DC/DCs.
	E-1.9.4	The EGSE power consumption should not exceed 5 W.
	E-1.10	The EGSE shall met requirements P-4.4.2 and P-4.4.3
	E-1.11	Mounting holes will be isolated.
	E-1.12	The EGSE shall adhere to requirements P-4.7 and P-4.8

Table 3.2 – Requirement description for the EGSE.

3.3 Hardware architecture

This section addresses the hardware architecture and the arrangement of the electronics. The architecture is the result of an iterative process of requirements engineering and component selection, with feedback from circuits and PCB design, which will be covered in Chapter 4 (page 53). Component selection is discussed in section 3.4 (page 45).

3.3.1 High-level systems definition

A high-level block diagram defines the relationships between the subsystems and organizes the design hierarchically. The payload is situated within the context of the satellite in Figure 3.3. The issue of how to provide shared access to the satellite antenna for both the LoRa payload and TT&C falls outside the scope of this thesis. Figure 3.3 also delineates the division into three PCBs, and summarizes the main functions and components to be allocated in each board. Subsequent sections tackle the block diagrams of each board. The power distribution system is outlined in Figure 3.5. The component selection is explained in detail in section 3.4 (page 45). The pinout of the mPCIe and CSKB connectors is defined in section 3.5 (page 51).

3.3.1.1 LoRa gateway modules

Figure 3.4a shows the architecture of the modules. This diagram is based on Semtech's reference designs [102]–[106]. The hardware architecture of a LoRa gateway comprises a baseband processor (the SX1302 [93]) and two transceivers (the SX1250s [66]). One of the transceivers serves both as a transmitter and receiver, while the other is a receiver only. The SX1250s are connected to the baseband processor via an SPI and an I/Q (in-phase and quadrature) data interface. The same 32 MHz crippled sine wave oscillator powers the transceivers, and subsequently the clock passes to the SX1302.

The RF stage consists of simple blocks. At the output, only an impedance matching of the output port to the additional power amplifier is required. At the input, a low-noise amplifier restores the attenuated RF signal while adding minimal noise. The signal is then split into two equal-power signals by a 3 dB power splitter. Before entering each SX1250 transceiver, a *balun* transforms the signal from single-ended to balanced and performs an impedance-matching. The design is half-duplex, and an RF switch controlled by the SX1302 toggles between transmit and receive mode.

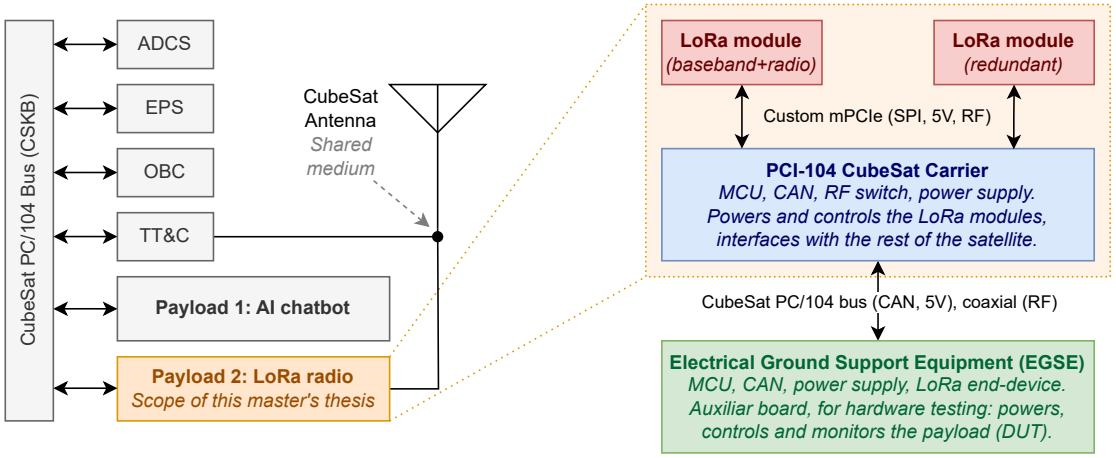


Figure 3.3 – High level block diagram of the CubeSat subsystems and high level block diagram of the LoRa communications payload and EGSE.

A temperature sensor is integrated into each module. The sensor should be positioned in close proximity to the primary heat sources, to ensure that meaningful data is collected. The module provides access to its interfaces via an mPCIe board-edge connector, as well as via a low-technology debug port.

The power system onboard the modules consists of a set of low-noise DC/DC converters, which fed the electronics their needed voltage rails.

All the electronics onboard the module are covered by an EMI shield.

3.3.1.2 CubeSat PC/104 carrier

Figure 3.4b shows the block diagram of the carrier board. The design revolves around the microcontroller unit (MCU). It acts as an intermediary between the LoRa gateways and the rest of the satellite. It arbitrates which module is enabled and which has access to the radio channel. Although only one of the modules will be active at any given time, one SPI peripheral and one I2C are reserved for each module for redundancy.

On the other hand, the CAN peripheral is connected to a pair of transceivers that act as an intermediary between the MCU and the CAN bus, necessary to adapt to the current, voltage and impedance of the bus. The MCU also has external interfaces (UART, USB and SWD) for monitoring, programming and debugging.

The carrier power system is similar to that of the LoRa gateway modules. It is implemented using low-noise, efficient DC/DC converters. The ability to monitor its own power consumption is added, as well as protection systems against overcurrent, overvoltage and reverse polarity; and a power multiplexer to perform priority power muxing.

Two temperature sensors are installed on the carrier, one in an activity zone and one at one end of the board.

3.3.1.3 Electrical Ground Support Equipment

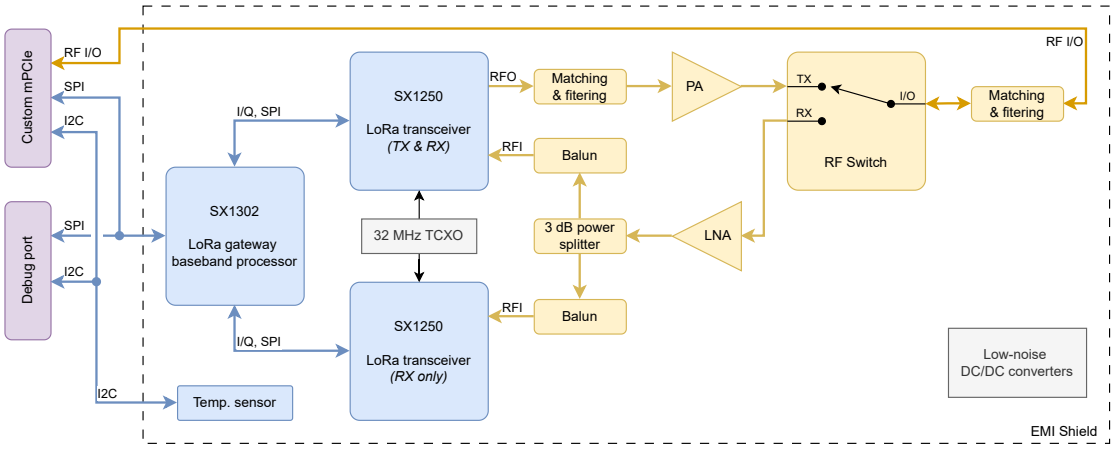
Figure 3.4c illustrates the electrical ground support equipment architecture, which is a variation of the carrier structure. The EGSE incorporates the electronics of a LoRa end-device, accompanied by supplementary test hardware and quality-of-life enhancements.

An SX1276 [63] implements the LoRa functions. The RF stage next to the transceiver is a structure similar to that seen in the modules, where an LNA and a PA extend the capabilities of the commodity LoRa IC. However, as can be seen, instead of connecting the transceiver output directly to an RF port, a more complex structure is implemented.

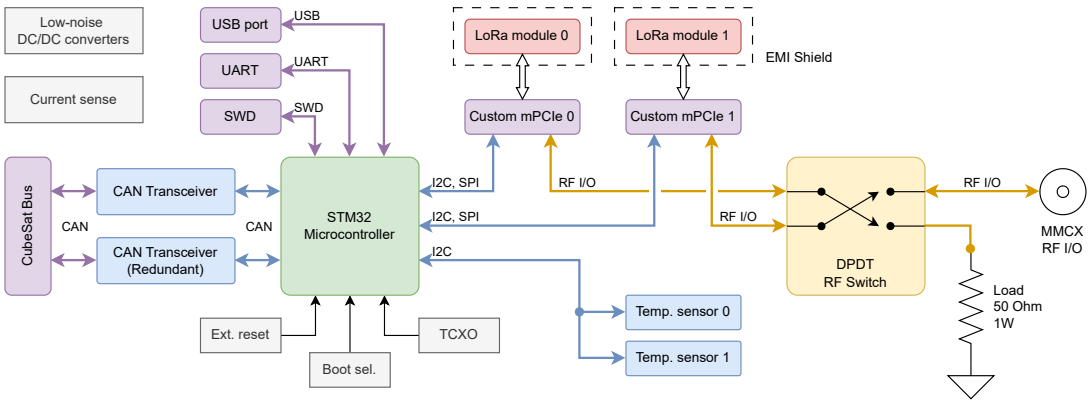
The RF input/output port of the DUT (device under test, the port that connects to the payload) is attenuated to prevent damage to the transceivers. The maximum power allowed at the input of the LoRa SX1250 and SX1276 transceivers is 10 dBm [63], [66]. Since the selected LNAs introduce a gain of up to 20 dB (see section 3.4, page 45), the power at the input of the LNAs should not exceed −10 dBm. Since the expected output power of the transceivers is 30 dBm, at least 40 dB of attenuation is required between the transceivers to not exceed the maximum input power.

In order to test the transceivers under conditions similar to those of the Earth-to-satellite radio link, at least 120 dB of additional attenuation must be achievable using variable attenuators. Since the power to be dissipated is high, the total attenuation is implemented in several successive stages, consisting of fixed and variable attenuators.

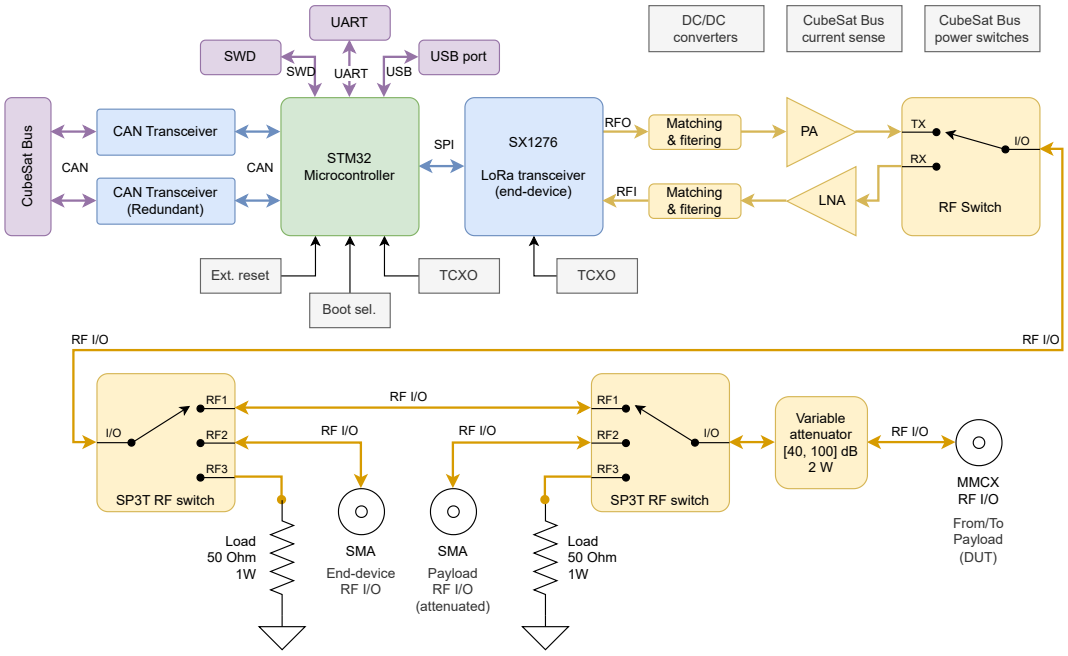
Additionally, RF switches are added to route the signal from the end-device and payload to a matched load or SMA ports, for convenience.



(a) High-level block diagram of the payload's LoRa modules.



(b) High-level block diagram of the payload's carrier board.



(c) High-level block diagram of the EGSE.

Figure 3.4 – An initial, high-level block diagram of the payload and EGSE electronics.

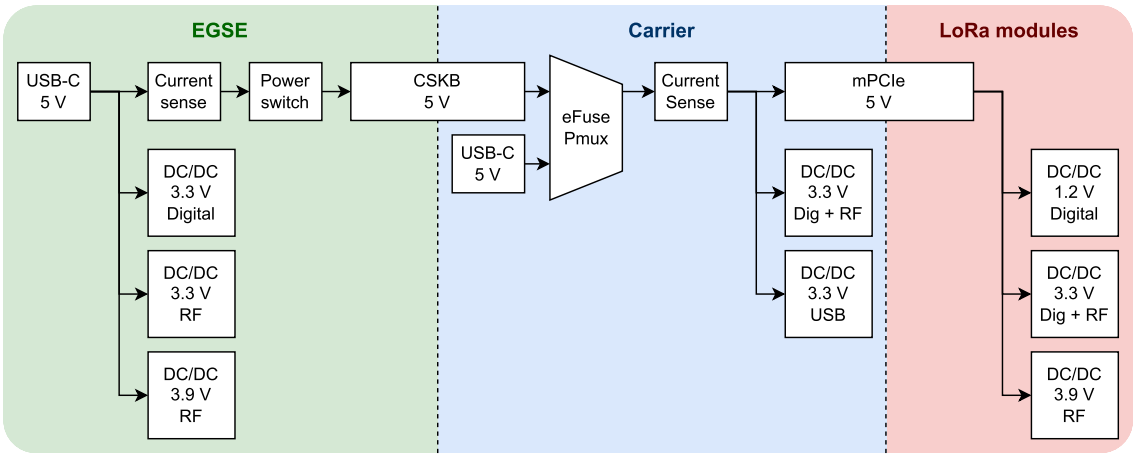


Figure 3.5 – Diagram of the power distribution system of the Payload and EGSE.

3.3.2 Physical arrangement of the electronics

The mechanical architecture of the payload is divided into a carrier or motherboard that mounts two LoRa modules or daughterboards for redundancy. The EGSE will be connected to the payload via the CSKB headers and an RF port. A conceptual representation of the proposed multi-board arrangement can be observed in Figure 3.6. The colour scheme (red modules, blue carrier and green EGSE) will be maintained throughout this document for easy identification of each board.

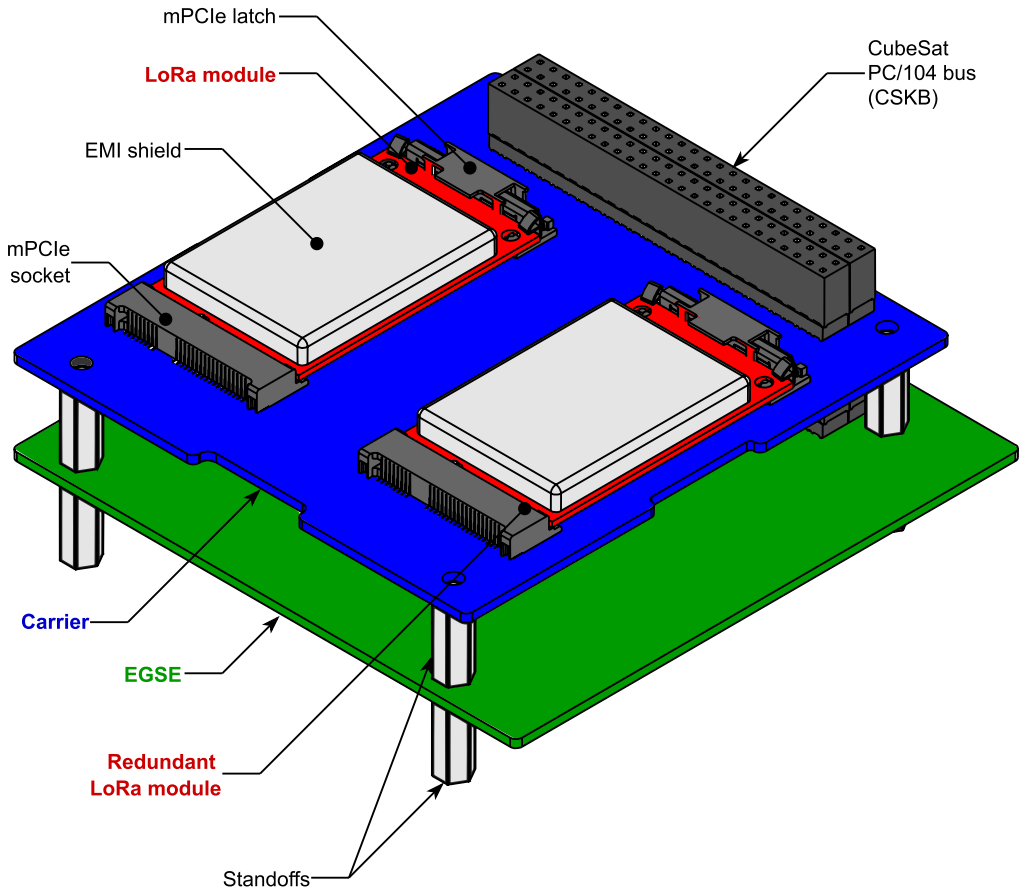


Figure 3.6 – Mockup of the assembled payload and EGSE.

3.4 Component selection

This section presents a selection of potential components for the application, balancing technical specifications, power consumption, price, availability and complexity of implementation. In general, surface mount devices (SMD) are preferred over through-hole devices (THD) for compactness and lower parasitics. THD parts are relegated to components that require mechanical mounting firmness.

To simplify the development process, many common, non-critical parts in the design –such as passives, diodes, and transistors– will be sourced from the Celestial Altium Library [113], a highly regarded repository of high-quality symbols and footprints.

3.4.1 LoRa gateway modules

3.4.1.1 Baseband processor

A LoRa gateway always follow the same hardware architecture: a LoRa Core digital baseband processor plus two LoRa Core RF transceivers. [102]–[106].

The baseband processor (Figure 4.2) is responsible for transforming the I/Q data received from the transceivers into a LoRa frame byte array. It also controls the transceiver reset signals, and manages the RF switch control signals for half-duplex operation. The available baseband processors not meant for picocells are the Semtech SX1301/2/3 chips. The SX1301 is the first generation of LoRa baseband processors. It has a considerable power draw and thus it poses a thermal design challenge [114]. The SX1302/3 are the second iteration, cutting down current consumption [93]. The only difference is that the SX1303 introduces fine timestamping for network-based geolocation, which the payload does not make use of. Since a lot of reference designs employ the SX1302 [102]–[106], it is devised as the most advantageous. Besides, the SX1302/3 are pin-to-pin compatible.

3.4.1.2 LoRa core transceivers

The transceivers transform LoRa messages into I/Q data and vice-versa. The baseband processor requires special LoRa modems, different from the ones used in the end-devices.

The options are the Semtech SX1250 (for all the sub-GHz bands), SX1255 (400 – 510 MHz), SX1257 (860 – 1000 MHz) and SX1258 (779 – 787 MHz). The last two are discarded because they do not support the 435 MHz band. The SX1255 offers a maximum output power of 5 dBm, whereas the SX1250 can output up to 22 dBm. The SX1250 and SX1255 use different packaging and are not pin-to-pin compatible. Each transceiver has its peculiarities: for example, the SX1250 uses balanced RX input and single-ended TX output, and in the case of the SX1255 is the opposite [66], [67].

Both modems are adequate for the job, but they require different hardware configurations. However, the choice was made when the link requirements were not completely clear: the 868 MHz band was still being considered as an option, and the need for an additional PA was being assessed. In light of the uncertainty, the SX1250 was selected.

3.4.1.3 Oscillator for the LoRa Core chips

Following Semtech's recommendations, a GNSS-grade, clipped sinewave, 32 MHz ± 0.5 ppm TCXO is employed in the gateway [92], [93], [115]. Many options are adequate, such as the ECS-TXO-20CSMV4-320-AY, Pletronics UCF4027035GG005000-32.0M or the ABRACON FT2MNTUM-32.0-T1. The latter is chosen for its higher availability.

3.4.1.4 RF front-end module

A front-end module is a collection of integrated circuits that perform the initial analog processing of radio signals. They typically include a low-noise amplifier (LNA) for the receive path, a power amplifier (PA) for the transmit path, and a switch to share the antenna between the transmitter and receiver. Front-end modules are very convenient to reduce the space used by the RF circuitry and to reduce the complexity of the circuit.

Front-end modules typically target higher frequencies than the 435 MHz band, such as the 868 MHz ISM band or the 2.4 GHz/5.8 GHz ISM/Bluetooth/Wi-Fi bands. Other drawbacks are that they typically have limited LNA and PA gain and output power less than 1 W due to their intended use and limited thermal dissipation. Semtech uses the SKY66420-11 and the SKY66423-11 ICs in some reference designs [103], [104], but they do not support the required frequency band. Other market leaders are Qorvo and Qualcomm. However, Qorvo does not have a bi-directional device that includes the band of interest, while Qualcomm specializes in Bluetooth, Wi-Fi, 4G and 5G bands.

The Skyworks SKY65366-21 is the only front-end module in its catalogue that fully meets the requirements. The operating frequency range is 400 MHz to 510 MHz, it has an output power of 30 dBm (1 W), a maximum LNA gain of 21 dB, a noise figure of 1.8 dB, and 2 dB of insertion loss. The maximum LNA input power is 5 dBm and the maximum PA input power is 15 dBm. All paths are internally matched to 50 Ω [116].

3.4.1.5 RF power splitter

Since there are two receivers, the signal must be split equally. Semtech designs use a Y-junction, which has abysmal return loss and no isolation [103], [104].

A 3 dB power divider is used in the design to improve performance. Microstrip implementations, such as Wilkinson dividers, are simple and have good RF characteristics. However, they are not feasible in this design because the needed $\lambda/4$ lines are 7.5 cm in length. An integrated device must be used instead. There are many technologies, with different properties and sizes. Low-profile dividers are designed for higher frequencies due to wavelength, and often have high insertion loss, low return loss, or poor isolation.

Mini-Circuits is a notable manufacturer of this market niche. While it offers a comprehensive catalogue, the footprints for the low-loss sub-GHz component series are considerable, which presents a challenge in the context of space-constrained LoRa modules. The ADP-2-4+ and JPS-2-1N+ are two viable options for consideration. The ADP-2-4+ is a 10 MHz to 1000 MHz splitter with 0.5 dB of insertion loss and a voltage standing wave ratio (VSWR) of 1.36 and 22 dB isolation, which is deemed acceptable. The JPS-2-1N+ is a 350 MHz to 550 MHz splitter with 0.25 dB insertion loss, with excellent impedance matching (VSWR $\leq$ 1.04, equivalent to -34 dB of S_{11}) and isolation of 43 dB.

An alternative, low-profile but subpar option is the Anaren PD0409J5050S2HF, which has mediocre return loss (10 dB), 0.7 dB of insertion loss, and poor isolation (10 dB).

Despite the space constraints, the preferred JPS-2-1N+ was able to fit into the design.

3.4.1.6 Temperature sensor

Existing LoRa gateway designs use the STTS751-0DP3F temperature sensor from ST Microelectronics, an inexpensive, low profile, low power, I2C temperature sensor with a range of -40 °C to 125 °C and an accuracy of ±0.5 °C [117]. This sensor is sufficient, and thus is integrated into both the LoRa modules and the carrier.

3.4.1.7 Power system

Once the main components have been selected, the power system can be dimensioned. The required voltage rails for the LoRa module's electronics are 1.2 V, 3.3 V, and 3.9 V. They will all be sourced from a 5 V rail using DC/DC converters.

The estimated maximum power consumption of the LoRa modules is detailed in Table 3.3, with a total of 4.4 W. The power consumption figures for each voltage rail allow the proper sizing of the DC/DC converters. Converters capable of delivering at least 1 A, and 1 MHz of minimum switching frequency are selected for all voltages.

Power management integrated circuits (PMICs) can provide multiple voltage rails, saving real state on the board. An example is the Texas Instruments TPS65266, a chip containing three buck converters capable of delivering 2 A each.

Another option is to use three standalone DC/DC converters. Devices such as the Microchip MIC22205, Texas Instruments TLV62569 or the Diodes Inc. AP3402 are adequate. However, it is preferable to use low-noise DC/DC converters, especially for powering the RF electronics. For reference, the LibreSpace SatNOGS CubeSat communication board [118] employs the TPS62912. The TPS62912 is a 2 A, low noise and low ripple buck converter with ferrite bead filter compensation and a selectable switching frequency of 1 or 2.2 MHz [119]. This chip is considered the optimal choice for this application.

Apart from series resistors in the digital I/Os, the LoRa modules do not include onboard protections against reverse polarity, overvoltage, overcurrent or ESD, due to RF performance, space constraints, and the intended application (a daughterboard should not directly expose any interfaces). Special care must be taken when handling them.

Component	**Description**	**Max. current consumption (mA)**				**Power**
		1.2 V	**3.3 V**	**3.9 V**	**5.0 V**	**cons. (mW)**
SX1302	LoRa BB processor	85	1			105.3
SX1250	LoRa transceiver (x2)		107			706.2
SKY65366-21	Front-end module		20	880		3498
FT2MNTUM	TCXO Oscillator		2.5			8.25
(Various)	LEDs		2	2	2	24.4
TPS62912	DC/DC converter (x3)				5	75
Total current consumption (mA)		**85**	**239.5**	**882**	**17**	
Total power consumption (mW)		**102**	**790.35**	**3439.8**	**85**	**4417.15**

Table 3.3 – LoRa modules: Power estimation for power supply sizing.

3.4.2 CubeSat PC/104 carrier

3.4.2.1 Microcontroller

The primary functions of the MCU are to configure the LoRa chips, to arbitrate the modules, to manage the LoRa packet forwarding, and to handle the low-speed communication peripherals. Therefore, a relatively low-power microcontroller is sufficient. Semtech reference designs [102]–[105] use the ST Microelectronics STM32L412, an ultra-low-power, one-core ARM Cortex-M4 MCU. However, it lacks the CAN peripheral. Nevertheless, the STM32L4 series is promising because it already meets many requirements in terms of performance, peripherals and power consumption.

The STM32L4 family is capable of operating at clocks up to 80 MHz and includes a floating-point unit (FPU). They support several communication interfaces, including SPI, I2C, USB and UART. Higher-end models also feature CAN. The devices are powered by a single supply voltage between 1.7 V and 3.6 V. The current consumption ranges from 80 to 100 µA/Hz in run mode. Moreover, they are available in a variety of packages, including LQFP32, UQFN32, LQFP48, UQFN48, LQFP64, and LQFP100 packages, among others. The STM32L4 family is pin-to-pin compatible with the rest of the STM32 series.

The choice is straightforward, as the sole SKU with two CAN peripherals and USB with non-overlapping pins is the STM32L496 (see Table 3.4). Of the available variants, the STM32L496RGT3 (LQFP64) is the optimal choice, as it has 1 MB of flash memory and is rated for a temperature range of −40 to 125 °C [120].

Line	Flash (kB)	RAM (kB)	USB	Number of peripherals				
				SPI	UART	USART	I2C	CAN
STM32L496	512 to 1024	320	OTG	3	2	3	3	2
STM32L476	256 to 1024	128	OTG	3	2	3	3	1
STM32L475	128 to 1024	128	OTG	3	2	3	3	1
STM32L452	256 to 512	160	Device	3	1	3	4	1
STM32L433	128 to 256	64	Device	3	0	3	3	1
STM32L432	128 to 256	64	Device	3	0	3	3	1
STM32L412	64 to 128	40	Device	2	0	3	3	0

Table 3.4 – Comparison of the STM32L4 series.

3.4.2.2 Oscillator for the microcontroller

Many quartz oscillators meet the requirements for the low-speed external (LSE) XTAL for the MCU. The chosen model is the ABS07-32.768KHZ-9-1-T, a 32.768 kHz ± 10 ppm crystal. The microcontroller is expected to use its Multi-Speed Internal (MSI) RC oscillator, which is powered by the external 32.768 kHz clock. The MSI oscillator is software-trimmable and can generate frequencies up to 48 MHz to supply the system clock, eliminating the need for a high-speed external crystal (HSE) [120]. 48 MHz is expected to provide the required processing power while reducing the MCU power consumption.

3.4.2.3 CAN transceivers

CAN transceivers are required as an intermediary between the physical layer of the CAN bus and the digital serial interface of the MCU's CAN peripherals. To support SpaceCAN [31], two transceivers are required. The requirements for the transceiver are that it supports CAN Flexible Data-Rate (CAN FD), which supports communication up to 8 Mbps, and that the chip has integrated ESD protection and a shutdown mode for power saving. Two options were selected: the TCAN341x series from Texas Instruments and the MCP254x series from Microchip. Finally, the MCP2542FDT-E/MF is selected for its lower price, smaller footprint, and convenient pin assignment [121].

3.4.2.4 RF switch

The selected double pole double throw (DPDT) switch is a SKY13396-397LF, a 0.4 GHz to 3.0 GHz switch with 0.4 dB of insertion loss, 25 dB of isolation and 20 dB of return loss, and an input power up to 39 dBm (3 W). An alternative is the SKY13699-21.

3.4.2.5 Power system

The required voltage for the electronics of the carrier is 3.3 V. The estimated power consumption is detailed in Table 3.5, with a total consumption of 0.3 W. Despite the lower power consumption, the design will use the same low-noise TPS62912 DC/DC converters for BOM consolidation and ease of implementation.

The selected power monitor is the Texas Instruments INA232, a high-side, 16 bit, current and voltage sensor with I2C. Other similar options are the INA219 and INA226.

The Texas Instruments TPS259470A IC was selected as the eFuse and power multiplexer to select the power supply for the payload between the CSKB header and the USB Type-C. The TPS259470A also provides reverse polarity, short circuit, overcurrent, overvoltage and ESD protection. All digital ports are protected by TVS diodes and/or resistors, except for the CAN bus, whose transceivers have a built-in ESD protection.

Component	Description	Max. I consumption (mA)		Power cons. (mW)
		3.3 V	5.0 V	
STM32L496	MCU. 91 uA/MHz. 48 MHz	4.4		14.52
ABS07	XTAL Oscillator	2.5		8.25
Various	LEDs	2	2	16.6
MCP2542	CAN transceiver	70		231
TPS62912	DC/DC converter (x2)		5	25
Total current consumption		**78.9**	**7**	
Total power consumption		**260.37**	**35**	**295.37**

Table 3.5 – Carrier: Power estimation for power supply sizing.

3.4.3 Electrical Ground Support Equipment

The EGSE has analogous requirements to those of the preceding boards, and thus it reuses many components: MCU, CAN transceivers, DC/DC converters, and so forth. Consequently, this section will focus on the remaining decisions specific to the EGSE.

3.4.3.1 LoRa end-device transceiver

Semtech offers a broad family of LoRa modems. The models targeted for outdoor use are the SX127x, SX126x and LR11xx. Same-series devices are pin-to-pin compatible.

The main difference between the SX127x devices is that the SX1272/3 transceivers operate in the 860–1000 MHz band, while the SX1276/7/8/9 support al the sub-GHz bands and offer improved sensitivity [63]. Thus. the SX1276/7/8/9 modems are the appropriate choice. The successor of the SX127x, the SX126x series, is very similar to the SX127x. The major advantage over the SX127x is the higher interference rejection [64]. The SX126x series is also suitable for the application.

The RF characteristics of the LR11xx series are very similar to the two previous families [65]. However, they include support for the Long Range Frequency Hopping Spread Spectrum (LR-FHSS) modulation and a Wi-Fi scanner. They also offer a higher level of immunity to Doppler than the SX127x and SX126x [91]. The LR11xx series is promising, but given its recent market entry and limited design resources, the more established SX127x modem is selected instead. The modem will be re-evaluated in the future.

3.4.3.2 RF switches

The chosen single pole triple throw (SP3T) switch for the EGSE is the SKY13373-460LF, a 0.1 GHz to 8.0 GHz switch with 0.35 dB of insertion loss, 40 dB of isolation, 17.5 dB of return loss, and a maximum input power of 39 dBm. Other candidates are the Infineon BGS13SN8 and the Skyworks SKY13582-676LF.

3.4.3.3 RF attenuators

The RF attenuation chain is divided into a first, low attenuation (3 dB + 30 dB), high power (33 dBm, 2 W) stage implemented by fixed attenuators; and a second, variable attenuation (0 − 120 dB), low power (0 dBm, 1 mW) stage.

The fixed 3 dB attenuator must be able to handle up to 1 W of dissipated power. For this task, the Mini-Circuits YAT-3A+ chip is used. An alternative is the Vishay/Barry ATC2010CT-0300JN-93T. The fixed 30 dB attenuator must also be able to dissipate 1 W of power, and the YAT-30A+ is used. Another option is the Anaren XRA10AA30SES.

The variable attenuators are four digitally-controlled Mini-Circuits DAT-31R5A-PP+ attenuators, each offering 0−31.5 dB of attenuation in 0.5 dB steps plus 1.5 dB of insertion loss. Other options include the Qorvo QPC6614SR and Renesas F1912NCGI8.

3.4.3.4 Power system

The EGSE requires 3.3 V and 3.9 V apart from the 5 V supplied from the USB. The estimated power consumption is detailed in Table 3.6, the total is 4.2 W. The EGSE will employ the TPS62912 DC/DC converters, as well as the INA232 power monitor.

The payload consumes a maximum of 4.7 W[1], and thus the needed current supplied through the 5 V rail will not exceed 1 A continuous. The EGSE is equipped with a power switch, which enables the user to control the activation and deactivation of the payload. This task is carried out by a Microchip MIC94080YFT, a tiny, high-side load switch that supports up to 2 A of continuous current. Alternative ICs include the Diodes Inc. AP221448, AP22800, and the Texas Instruments TPS22967.

Component	Description	Max. I consumption (mA)			Power cons. (mW)
		3.3 V	3.9 V	5.0 V	
STM32L496	MCU, 91 µA/MHz, 48 MHz	4.4			14.52
SX1276	LoRa transceiver	107			353.1
SKY65366-21	Front-end module	20	880		3498
FT2MNTUM	TCXO Oscillator	2.5			8.25
ABS07	XTAL Oscillator	2.5			8.25
Various	LEDs	2	2	2	24.4
MCP2542	CAN transceiver	70			231
TPS62912	DC/DC converter (x2)			5	50
Total current consumption		**208.4**	**882**	**12**	
Total power consumption		**687.72**	**3439.8**	**60**	**4187.52**

Table 3.6 – EGSE: Power estimation for power supply sizing.

[1]This figure is the sum of the power consumption of the carrier and only one module, since both cannot be activated at the same time.

3.5 Connector pinouts

The pinout for the mini-PCI-express is presented in Table 3.7. There are significant discrepancies with the mPCIe standard, with only the I2C, GND and power pins remaining consistent (albeit with 5 V instead of 3.3 V).

The RF I/O is routed through the mPCIe connector surrounded by GND traces. Given that the wavelength of the 435 MHz is of the order of 30 cm on the circuit board medium, the discontinuity of the connector is small and the reflections and losses are expected to be minimal. This approach is sub-optimal, but it was selected as the simplest and most cost-effective solution.

The CSKB pinout is shown in Table 3.8. The pinout is based on the 2022 LibreCube board specification [110], which is better suited to the needs of the Estigia satellite than the current 2024 revision [4].

Apart from the absence of the CAN A and CAN B buses physically repeated in the H1_B and H2_B headers (which are occupied by functions of other subsystems), it follows the standard perfectly. The payload uses only the pins it needs, the rest remain unconnected (NC). The pinout includes the remove before flight (RBF) and emergency kill pins. The `RBF` pin is a safety mechanism that prevents accidental activation of the subsystem before launch, whereas the `KILL` pin shuts down the power supply and is intended to be used in the event of an emergency or critical failure.

Top side			Bottom side		
LoRa module	**mPCIe spec**	**Pin No.**		**mPCIe spec**	**LoRa module**
GND	WAKE#	1	2	3.3V	5V
RFIO	COEX1	3	4	GND	GND
GND	COEX2	5	6	1.5V	
	CLKREQ#	7	8	UIM_PWR	
GND	GND	9	10	UIM_DATA	
	REFCLK-	11	12	UIM_CLK	RADIO_CLK_OUT
	REFCLK+	13	14	UIM_RESET	RESET
GND	N/C or GND	15	16	UIM_VPP	ENABLE
Mechanical key					
	UIM_C8_RSV	17	18	GND	GND
	UIM_C4_RSV	19	20	W_DISABLE#	
GND	GND	21	22	PERST#	
	PERn0	23	24	3.3V	5V
	PERp0	25	26	GND	GND
GND	GND	27	28	+1.5V	
GND	GND	29	30	SMB_CLK	I2C_SCL
	PETn0	31	32	SMB_DATA	I2C_SDA
	PETp0	33	34	GND	GND
GND	GND	35	36	USB_D-	
GND	GND	37	38	USB_D+	
5V	3.3V	39	40	GND	GND
5V	3.3V	41	42	LED_WWAN#	PG1V2
GND	GND	43	44	LED_WLAN#	PG3V3
MCU_SPI_CLK	Reserved*	45	46	LED_WPAN#	PG3V9
MCU_SPI_MISO	Reserved*	47	48	+1.5V	
MCU_SPI_MOSI	Reserved*	49	50	GND	GND
MCU_SPI_NSS	Reserved*	51	52	+3.3V	5V

Table 3.7 – The modules' mPCIe pinout versus the mPCIe electromechanical standard [2].

LoRa payload	LibreCube 2022	H1_A
CAN_A_L	CAN_A_L	H1_1
CAN_A_H	CAN_A_H	H1_3
	UART_1A_TX	H1_5
	UART_1A_RX	H1_7
	UART_2A_TX	H1_9
	UART_2A_RX	H1_11
	ENA_LCL_1	H1_13
	ENA_LCL_2	H1_15
	ENA_LCL_3	H1_17
	ENA_LCL_4	H1_19
		H1_21
		H1_23
5V	5V	H1_25
		H1_27
		H1_29
	CHARGE	H1_31
GND	GND	H1_33
	PWR_LCL_1	H1_35
	PWR_LCL_2	H1_37
	PWR_LCL_3	H1_39
	PWR_LCL_4	H1_41
	PWR_LCL_5	H1_43
	PWR_LCL_6	H1_45
	PWR_LCL_7	H1_47
	PWR_LCL_8	H1_49
		H1_51

H1_B	LibreCube 2022	LoRa payload
H1_2	CAN_A_L	
H1_4	CAN_A_H	
H1_6	UART_1A_TX	
H1_8	UART_1A_RX	
H1_10	UART_2A_TX	
H1_12	UART_2A_RX	
H1_14	ENA_LCL_5	
H1_16	ENA_LCL_6	
H1_18	ENA_LCL_7	
H1_20	ENA_LCL_8	
H1_22		
H1_24		
H1_26	5V	5V
H1_28		
H1_30		
H1_32	CHARGE	
H1_34	GND	GND
H1_36	PWR_LCL_1	
H1_38	PWR_LCL_2	
H1_40	PWR_LCL_3	
H1_42	PWR_LCL_4	
H1_44	PWR_LCL_5	
H1_46	PWR_LCL_6	
H1_48	PWR_LCL_7	
H1_50	PWR_LCL_8	
H1_52		

LoRa payload	LibreCube 2022	H2_A
CAN_B_L	CAN_B_L	H2_1
CAN_B_H	CAN_B_H	H2_3
	UART_1B_TX	H2_5
	UART_1B_RX	H2_7
	UART_2B_TX	H2_9
	UART_2B_RX	H2_11
		H2_13
		H2_15
		H2_17
		H2_19
		H2_21
		H2_23
5V	5V	H2_25
		H2_27
GND	GND	H2_29
GND	GND	H2_31
		H2_33
		H2_35
RBF_NO	RBF_NO	H2_37
KILL_NO	KILL_NO	H2_39
RBF_COM	RBF_COM	H2_41
KILL_COM	KILL_COM	H2_43
	VBAT	H2_45
		H2_47
		H2_49
		H2_51

H2_B	LibreCube 2022	LoRa payload
H2_2	CAN_B_L	
H2_4	CAN_B_H	
H2_6	UART_1B_TX	
H2_8	UART_1B_RX	
H2_10	UART_2B_TX	
H2_12	UART_2B_RX	
H2_14		
H2_16		
H2_18		
H2_20		
H2_22		
H2_24		
H2_26	5V	5V
H2_28		
H2_30	GND	GND
H2_32	GND	GND
H2_34		
H2_36		
H2_38	RBF_NO	RBF_NO
H2_40	KILL_NO	KILL_NO
H2_42	RBF_COM	RBF_COM
H2_44	KILL_COM	KILL_COM
H2_46	VBAT	
H2_48		
H2_50		
H2_52		

Table 3.8 – The payload's CSKB pinout versus the LibreCube 2022 board specification [110].

Chapter 4

Design

4.1 Schematic capture

4.1.1 LoRa gateway modules

Figure 4.1 depicts the low-level block diagram of the LoRa gateway modules. In the Altium Designer EDA software, each block represents a schematic sheet. The main components in the LoRa modules are the baseband processor and the RF front-end. The RF front-end in turn is divided into the LoRa transceivers and a front-end module.

The complete schematic sheets are included in section C.1, page 122.

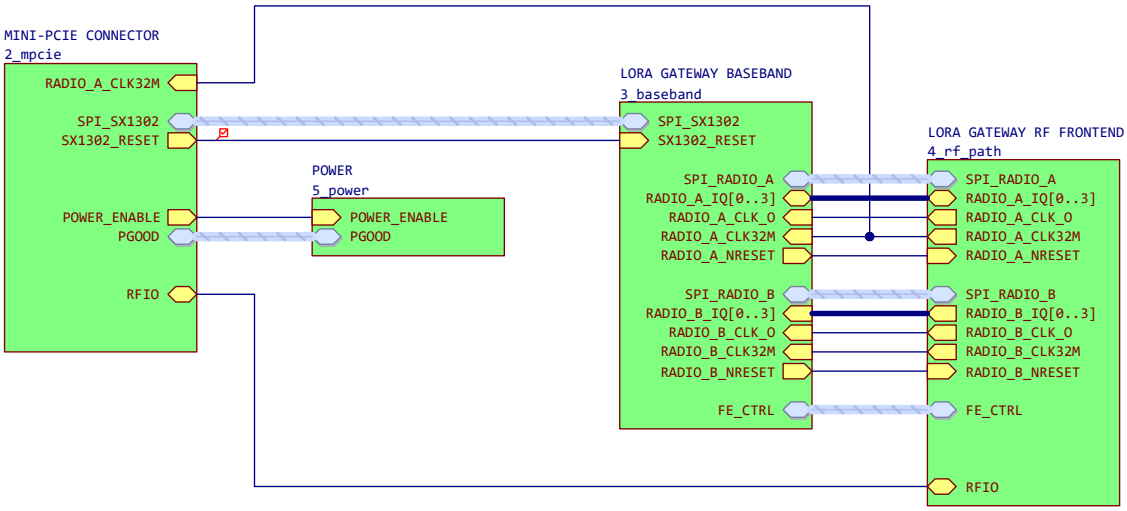


Figure 4.1 – Low-level diagram of the LoRa gateway modules.

4.1.1.1 LoRa core baseband processor

As explained in section 3.4.1.1 (page 45), the baseband processor transforms the I/Q data from the transceivers into a LoRa frame byte array and vice versa. It has a dedicated SPI and I/Q interface connected directly to each transceiver. It also controls the transceiver reset signals and manages the RF switch control signals for half-duplex operation. The 32 MHz clock is provided by the LoRa transceivers themselves.

The baseband processor also provides an SPI interface for configuration and data exchange with a *host*. A pull-up resistor is placed on the chip select pin (`NSS/CSN`) to prevent accidental selection of the baseband processor upon MCU reset. The I/Q interface contains optional series termination resistors that may be required for signal integrity.

The IC is powered by a 1.2 V *'core'* and a 3.3 V *'I/O'* rails. One 1 nF and 1 µF decoupling capacitors are allocated per power pin, with an extra 1 µF capacitor for pin 5 [103].

Hardware design guidelines and programming guides for the SX130x chips are notably lacking. The functionality of the `GPIO` and `RADIO_CTRL` pins is not described, and the closest publicly available resource is an undocumented hardware abstraction layer (HAL) [122]. Therefore, it was decided to keep the same pin configuration as the reference designs [103], [104].

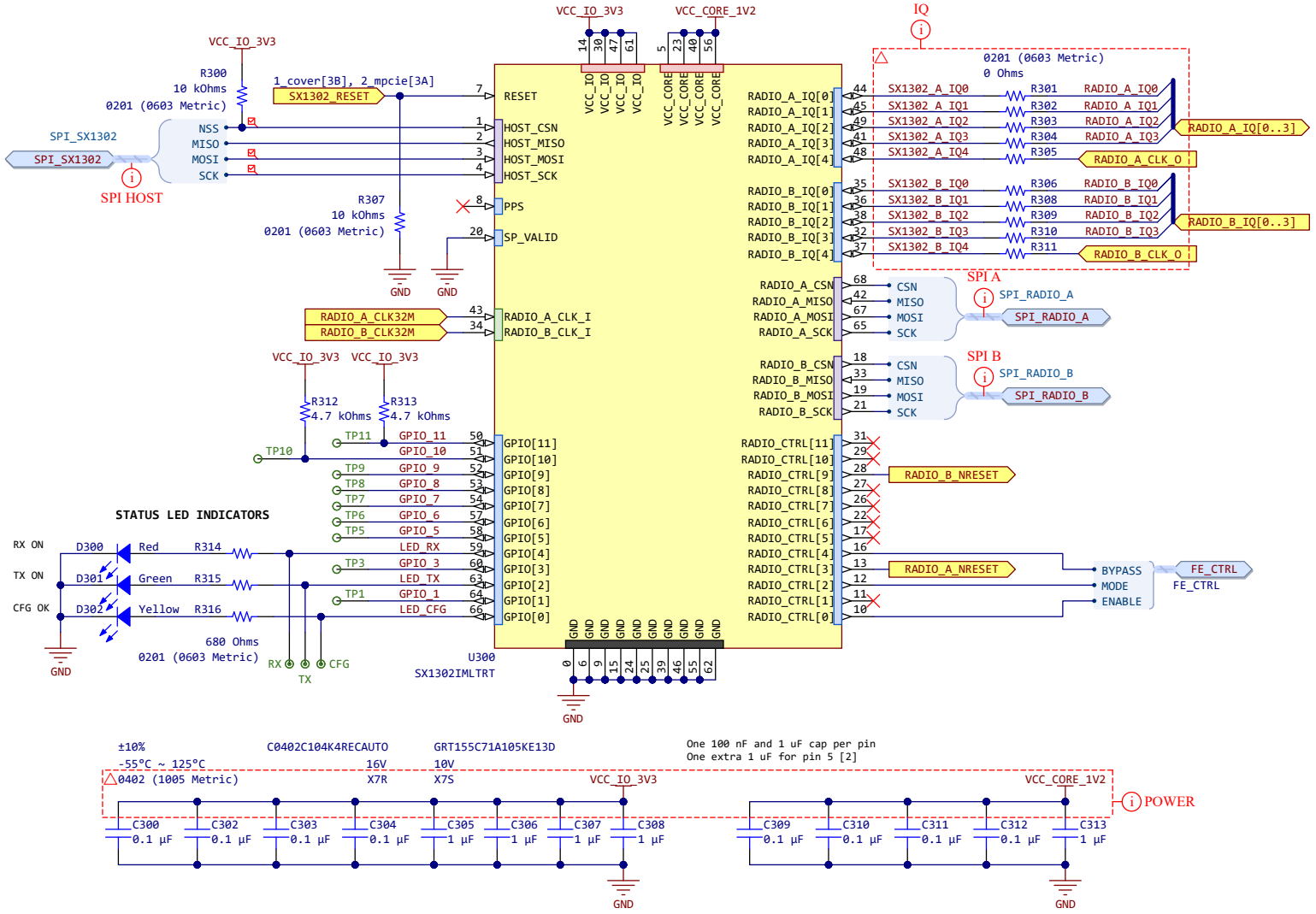


Figure 4.2 – LoRa module: Schematic of the LoRa core baseband processor.

4.1.1.2 LoRa core transceivers and RF front-end

The Figure 4.8 shows the schematic of the RF part. The schematic consists of the SX1250 transceivers, a power splitter, a front-end module, and several passive networks.

- **The SX1250 transceivers** appear in Figure 4.8a. One transceiver is transmitter and receiver, whereas the other is only a receiver and its output path is not routed. Both transceivers are driven by an FT2MNTUM-32.0-T1, a 32 MHz ± 0.5 ppm, GNSS-precision, clipped-sine wave TCXO (Figure 4.8b). The oscillator output is connected to the `XTA` pins of each transceiver via a series 10 pF DC-blocking capacitor and a 220 Ω resistor to reduce the clock amplitude [92], [93], [123].

  SX1250 transceivers use their integrated LDO regulator or their DC/DC converter to generate an internal power rail. The DC/DC is used in this design for its lower power consumption [66]. Consequently, the `DCC_SW` and `VREG` pins are populated with a 15 µH power inductor and a 470 nF capacitor as recommended [66].
- **The JPS-2-1N+ power splitter** (Figure 4.8c) is a passive device that evenly splits the RF power from the front-end module while maintaining high branch isolation, good return loss and low insertion loss (see section 3.4.1.5, page 46).
- **The SX1250 LNA matching network and balun** (Figure 4.8d) converts the single-ended input signal to balanced. The only input impedance specification for the SX1250 is a single-point optimal source impedance, $Z_{S,\text{opt}} = 74 + j134\,\Omega$ at 868 MHz [66]. Lacking a better figure[1], the impedance is transformed into a $R||C$ network, assuming that the behavior will be the same at 435 MHz:

$$\begin{aligned} Z_{\text{LNA}} = Z^*_{S,\text{opt}} = 74 - j134\,\Omega \;\; @ \;\; f = 868\,\text{MHz} \\ R_S \approx 74\,\Omega \;\; ; \;\; C_S \approx 1.37\,\text{pF} \\ Q = \omega \cdot C_P \cdot R_P = (\omega \cdot C_S \cdot R_S)^{-1} = 3.62 \;\; @ \;\; f = 435\,\text{MHz} \\ R_P = R_S \cdot (1+Q^2) \approx 1.04\,\text{k}\Omega \;\; ; \;\; C_P = C_S \cdot Q^2/(1+Q^2) \approx 1.24\,\text{pF} \end{aligned} \tag{4.1}$$

  The proposed 4-element balun can theoretically provide perfect π rad phase balance between the positive and negative inputs, thus optimizing LNA conversion gain and receiver sensitivity [124]. The balun is designed at 435 MHz as follows:

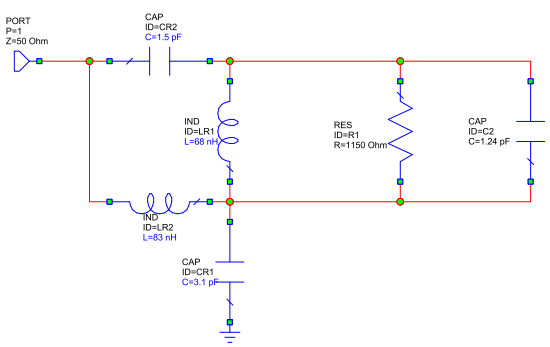
$$\begin{aligned} L_{\text{R2}} = \left(\sqrt{\text{Re}[Z_{in}] \cdot R_{\text{LNA}}}\right)/\omega \approx 83.6\,\text{nH} \\ C_{\text{R2}} = 1/(\omega^2 \cdot L_{\text{R2}}) \approx 1.61\,\text{pF} \\ C_{\text{R1}} = 2 \cdot C_{\text{R2}} \approx 3.06\,\text{pF} \\ L_{\text{LNA}} = 1/(\omega^2 \cdot C_{\text{P}}) \approx 108.4\,\text{nH} \\ L_{\text{R1}} = (L_{\text{LNA}} \cdot 2L_{\text{R2}})\,/(L_{\text{LNA}} + 2L_{\text{R2}}) \approx 65.8\,\text{nH} \end{aligned} \tag{4.2}$$

  After several simulations, the following commercial values have been settled:

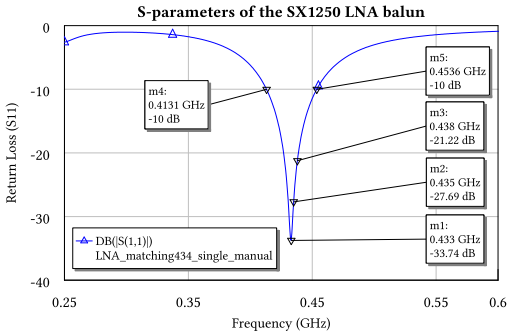
$$L_{\text{R1}} = 68\,\text{nH} \quad ; \quad L_{\text{R2}} = 82\,\text{nH} \quad ; \quad C_{\text{R1}} = 3.1\,\text{nH} \quad ; \quad C_{\text{R2}} = 1.5\,\text{nH} \tag{4.3}$$

  The simulations in Figure 4.3 prove that the impedance is matched. The results in Figure 4.4 demonstrate the π rad phase balance.

[1] Since the manufacturer does not provide this data, it will be necessary to characterize the transceivers. See section 5.3.1: Discussion on design flaws and improvements, page 102.

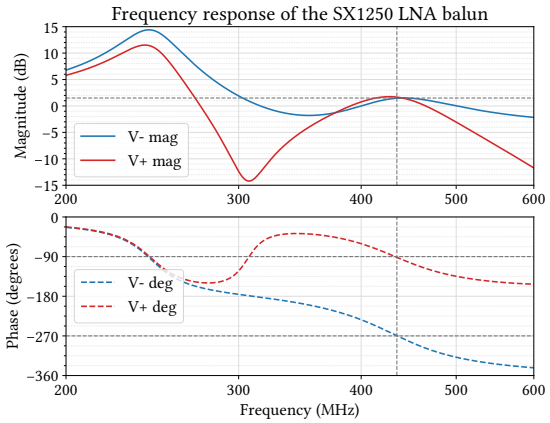


(a) Four-element balun design circuit.

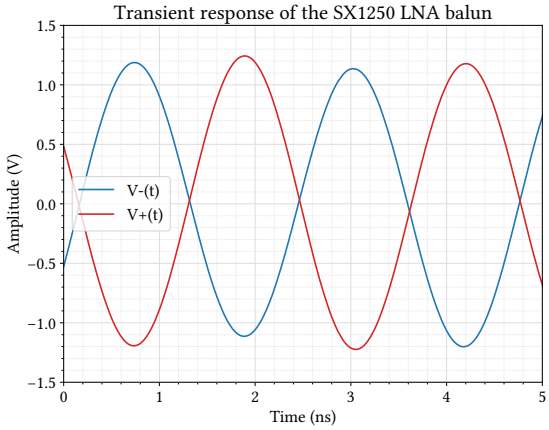


(b) Transmission (S_{21}) and reflection (S_{11}) coefficients of the balun of the receiver.

Figure 4.3 – LoRa module: Simulations of the receiver LNA balun.

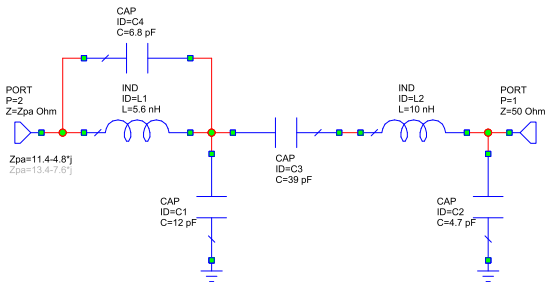


(a) Frequency response.

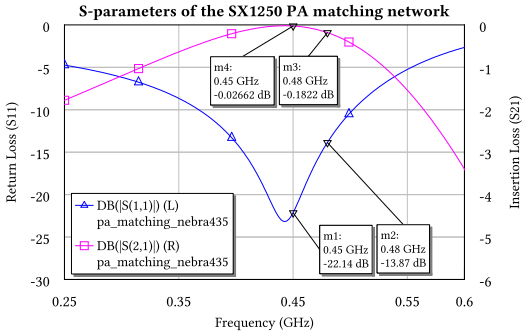


(b) Transient response.

Figure 4.4 – LoRa module: Simulation of the phase balance of the receiver balun.



(a) PA matching network.



(b) Transmission (S_{21}) and reflection (S_{11}) coefficients of the power amplifier matching network.

Figure 4.5 – LoRa module: S-param simulations of the RX balun and TX matching network.

- In the case of **the PA output matching network**, the manufacturer does not provide a measurement that can be used to inform the design, assuming that the designer will characterize the transceivers[2]. Consequently, the output PA matching network is based on the existing reference designs', scaled to 435 MHz and following the guidance set out in Semtech's RF design guidelines [125], [126].

  Figure 4.8e illustrates the matching network topology and stages, and Figure 4.5 presents the S-parameter simulations of the circuit.

- **The RF front-end module** schematics are drawn in Figure 4.9. The SKY65366-21 circuit is based on its typical application design [116].

  A resistor connected to `RBIAS` configures the LNA gain. By default, it is shorted to GND for maximum gain. For maximum PA gain, pin `VPC` is set to 2.25 V with a voltage resistor, taking into account the 50 kΩ input impedance of the `VPC` pin.

  The `BYPASS` pin truth table of the SKY65366-21 is inverted from the SKY6642x `CPS` pin used in the reference designs [103], [104]. Due to the aforementioned lack of SX1302 programming documentation, a 0 Ω resistor is provided to short `BYP` to ground to disable the bypass mode completely if necessary.

  The SKY65366-21 is powered by a filtered 3.3 V and 3.9 V rail, with the 3.9 V rail feeding the RF circuitry and thus consuming the most power [116].

- The front-end module is accompanied by **a 3rd order Chebyshev band pass filter (BPF)** and **an LC low pass filter (LPF)**. The filters were designed using the Cadence AWR Design Environment iFilter tool.

  The filters suppress higher order harmonics and image frequencies. The BPF type and order were chosen as a compromise between insertion loss and selectivity. The BPF has a center frequency of 435 MHz with a bandwidth of 50 MHz and 1 dB maximum insertion loss (Figure 4.6a) and a minimum return loss of 20 dB.

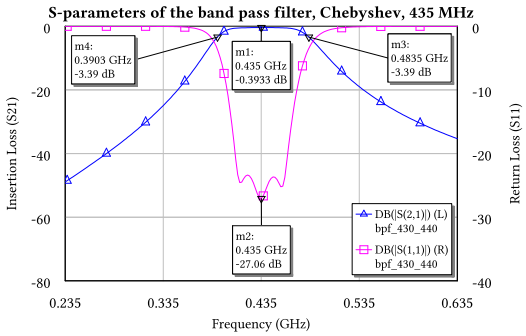
  The LPF also serves as an antenna matching network. The −3 dB cutoff frequency is 600 MHz, and has around 0.1 dB of insertion loss at 435 MHz (Figure 4.6b).

Surface Acoustic Wave (SAW) filters are widely utilized in reference designs within the receiver chain, and normally placed before the Low Noise Amplifier (LNA) [103], [104]. Despite their efficacy in narrowband filtering, they also introduce significant insertion losses, the order of 3-5 dB. This level of insertion loss is not compatible with the requirements of this mission.

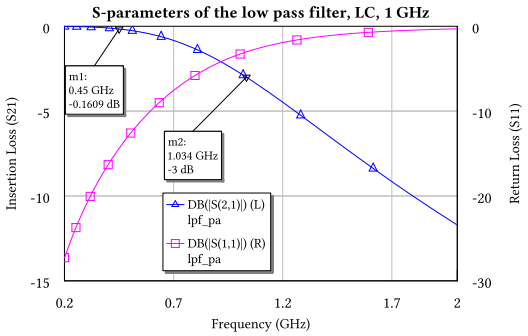
Additional simulations are performed to assess the characteristics of the entire receiver chain of the LoRa modules. The simulated circuit is shown in Figure 4.7. The simulation accounts for the gain and loss of the receiver chain from the antenna input to just before entering the balun. The RF I/O port of the mPCIe connector is modeled as an ideal 50 Ω port. The signal passes through the low-pass and band-pass filters described above, and enters the RF front-end module. The RF front-end module is modeled taking into account its insertion loss and the gain of the LNA, with accurate parameters from the datasheet [116]. The power splitter is modelled as a 3 dB loss in addition to its intrinsic insertion loss.

The complete chain gives us about 14 dB of gain in a wide passband. Matching in this band is good, with about 20 dB return loss.

[2] See section 5.3.1: Discussion on design flaws and improvements, page 102.

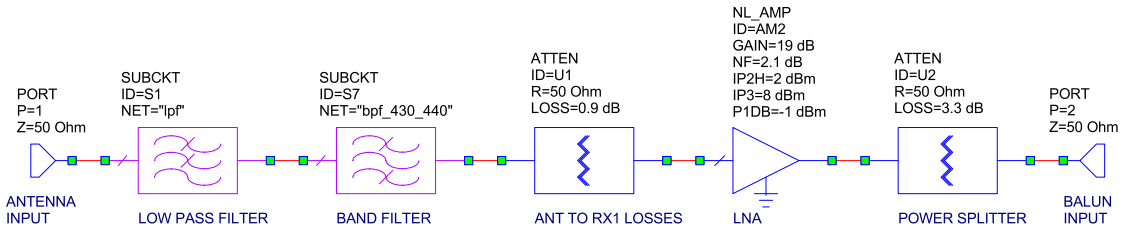


(a) S-parameters of the BPF.

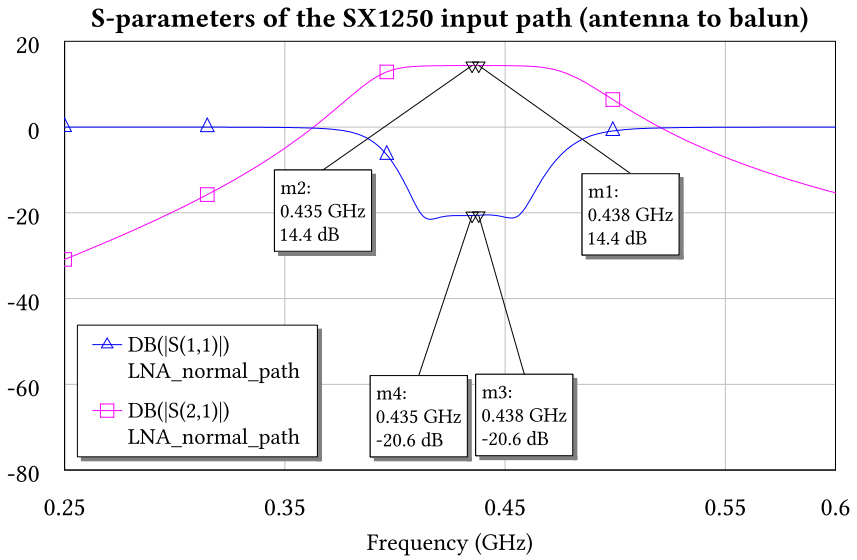


(b) S-parameters of the low pass filter.

Figure 4.6 – S-parameter simulations of the band pass and low pass filters.



(a) Simulated circuit of the receiver chain.



(b) S-parameters of the complete receiver chain of the module.

Figure 4.7 – LoRa module: Simulations of the receiver chain.

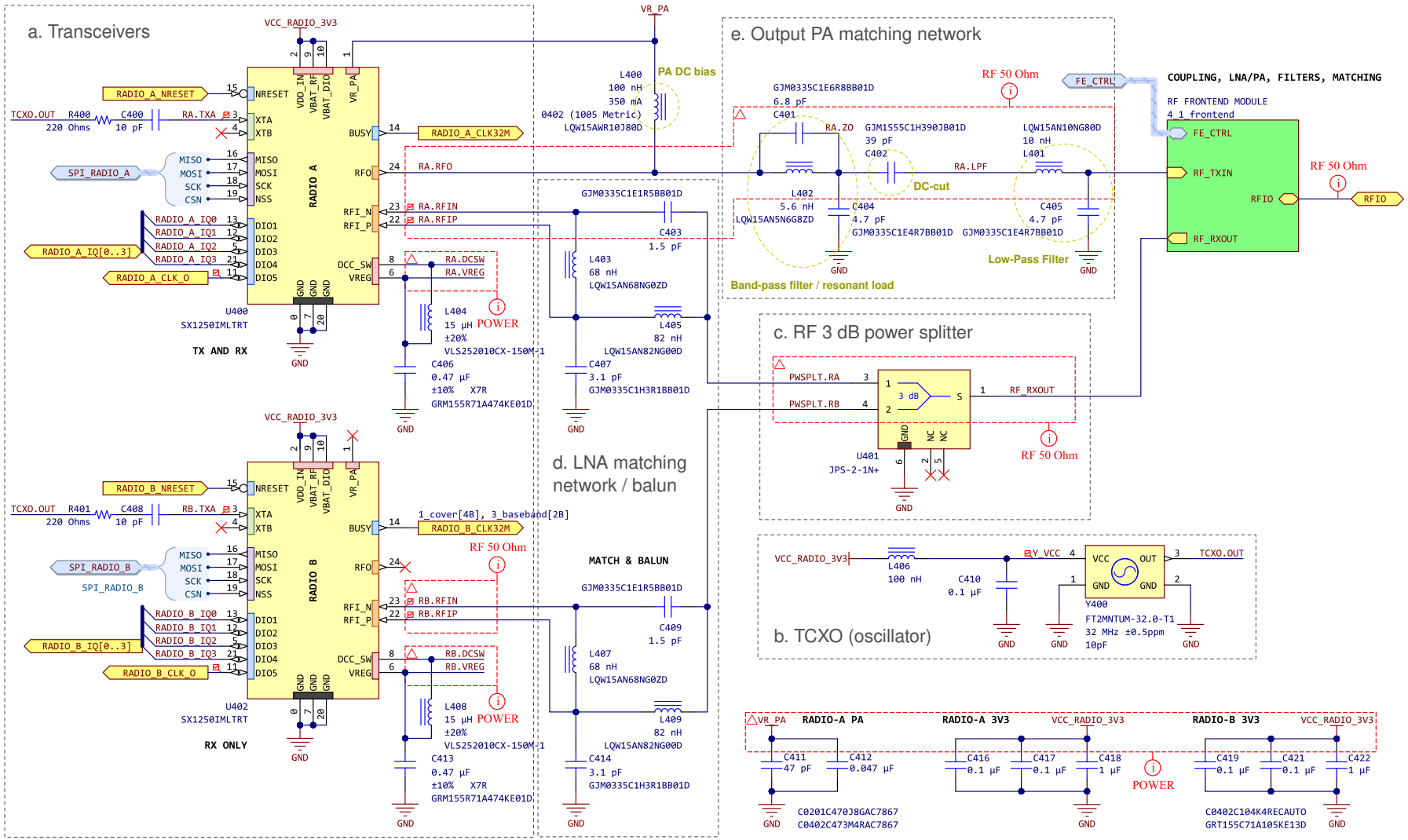


Figure 4.8 – LoRa module: Schematic of the LoRa core transceivers, power splitter and oscillator.

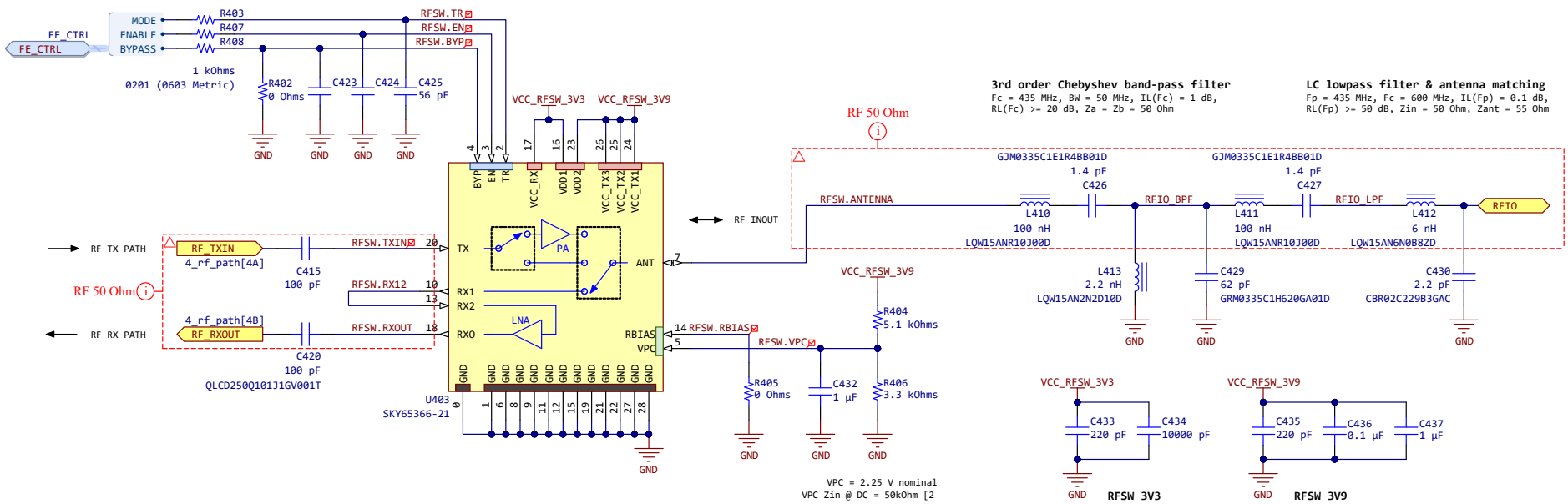


Figure 4.9 – LoRa module: Schematic of the RF front-end module and the band-pass and low pass filters.

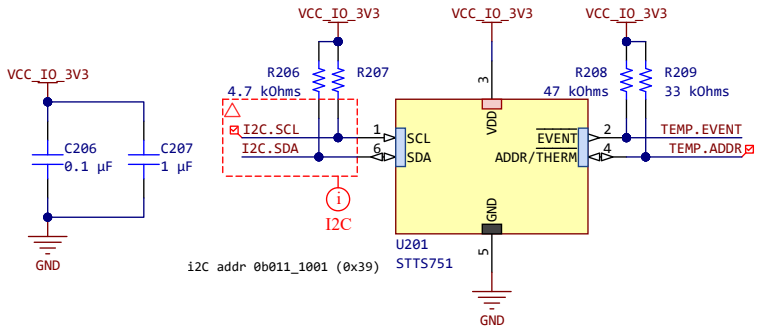


Figure 4.10 – LoRa module: Schematic of the temperature sensor.

4.1.1.3 Temperature sensor

The STTS751-0DP3F temperature sensor is easy to configure (Figure 4.10). The I2C bus is terminated by two parallel (and optional) 4.7 kΩ resistors. The 33 kΩ pull-up resistor in pin `ADDR` configures the i2C address as `0b011_1001` (`0x39`). The `EVENT` output is open-drain and requires a pull-up resistor, although the `EVENT` signal is not used [117].

4.1.1.4 Ports

The main communication interface of the modules is the mPCIe port, which is drawn in Figure 4.11. It adheres to the pinout definition presented in Table 3.7 (section 3.5, page 51). In addition to the mPCIe port, another low-technology header is provided to facilitate the probing of I2C and SPI bus signals.

As external interfaces, 100 Ω series resistors are incorporated into all digital signals to safeguard integrated circuits from the effects of small loads and short circuits. The 5 V power net is partially protected from over-voltage and electrostatic discharges by means of a RCLAMP0561PQTCT TVS diode clamp. The mPCIe port has a 100 nF decoupling capacitor per power pin and a larger 1 µF to stabilize the supply.

4.1.1.5 Power system

The power system for the modules consists of three TPS62912 low-noise, low-ripple buck converters which generate the 1.2 V, 3.3 V and 3.9 V rails. The circuit topology follows the typical application circuit with ferrite bead compensation [119].

The switching frequency can be chosen for high efficiency (1 MHz) or low noise (2.2 MHz). However, there are considerations for minimum duty cycle and on-time [119]:

$$\begin{aligned} D \approx V_o/(V_i \cdot \eta) \;\; [\text{worst case: } V_o = 1.2\,\text{V},\; V_i = 5.7\,\text{V},\; \eta = 1] \;\; D_{\text{min}} \approx 0.211 \\ t_{\text{on,min}} \approx D_{\text{min}}/f_{\text{max}} \overset{f_{\text{max}}=2.2\,\text{MHz}}{\Longrightarrow} t_{\text{on,min}} \approx 95\,\text{ns} \end{aligned} \tag{4.4}$$

Since $t_{\text{on,min}} \geq 70\,\text{ns}$ all converters can be configured for 2.2 MHz to minimize noise.

Feedback resistors set the output voltage according to the resistor divider equation:

$$V_{\text{fb}} = V_{\text{o}} \cdot \frac{R_2}{R_1 + R_2} \quad \Longrightarrow \quad R_1 = R_2 \cdot \left(\frac{V_o}{V_{\text{fb}}} - 1 \right) \tag{4.5}$$

Where $V_{\text{fb}} = 0.8\,\text{V}$ is the feedback voltage, fixed by the converter. According to the manufacturer, to minimize noise, $R2$ should be equal or lower than 5 kΩ [119]. For the feedback network, ±1 % tolerance resistors are used (see Figure 4.12).

The 2.2 MHz switching frequency requires the use of a 2.2 µH inductor. The inductor is shielded, has low series resistance, and its saturation current is over-dimensioned. Optimal output capacitor values depend on f_{sw} and V_o [119].

The *power good* (PG) open-drain output informs of power supply issues. The `PG` pin is in high impedance when $V_{\text{fb}} \geq 95\,\%$, and it is driven low when $V_{\text{fb}} \leq 90\,\%$.

The three converters perform a sequential power-up: first the 1.2 V rail is settled, and then the 3.3 V and 3.9 V voltages. This is necessary to avoid a power supply sequencing issue on the SX1302 which can cause an uncontrolled in-rush current [127]. To implement said sequential power-up, the `EN/SYNC` pins of the 3.3 V and 3.9 V converters are connected to the `PG` output of the 1.2 V converter.

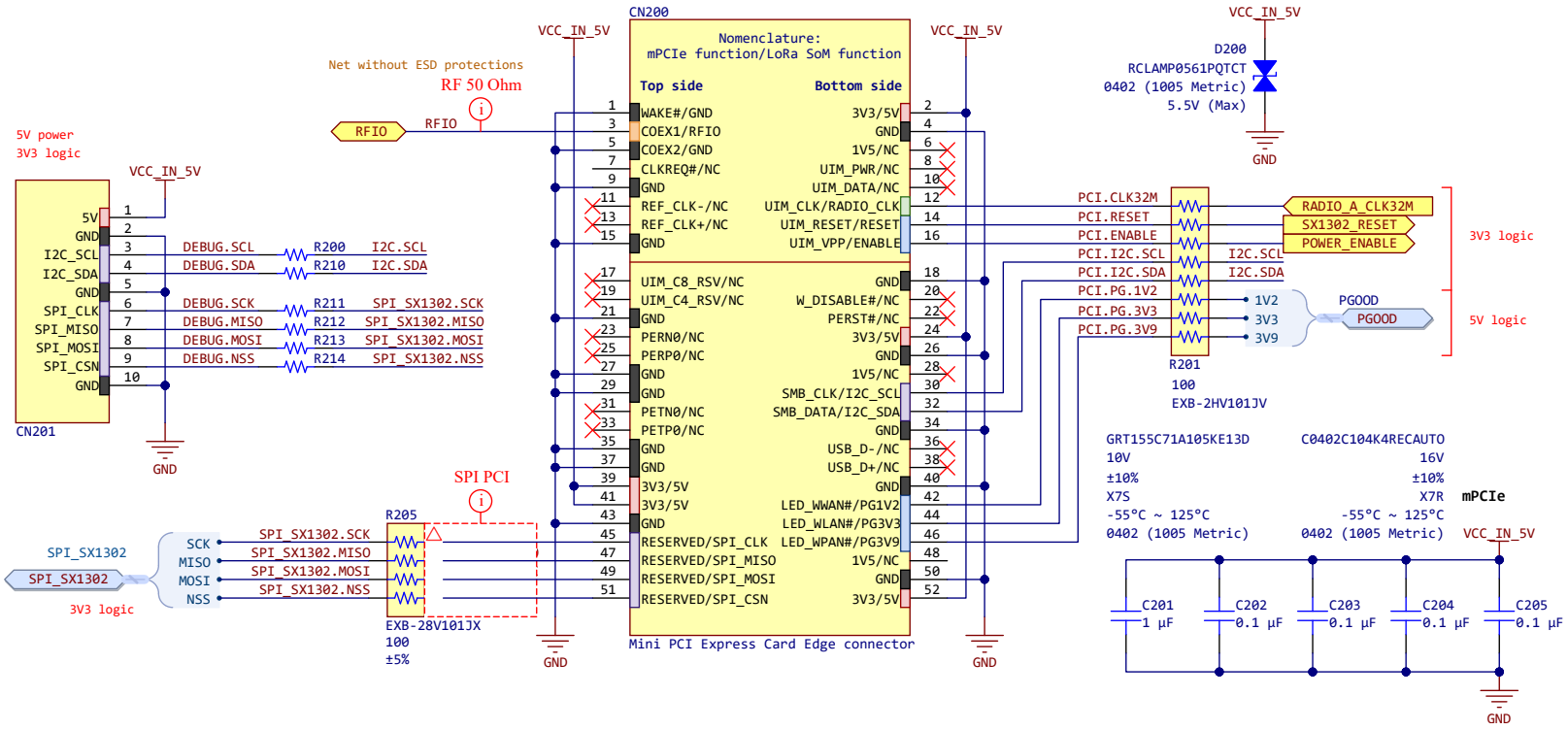


Figure 4.11 – LoRa module: Schematic of the mini-PCI-express port and the debug port.

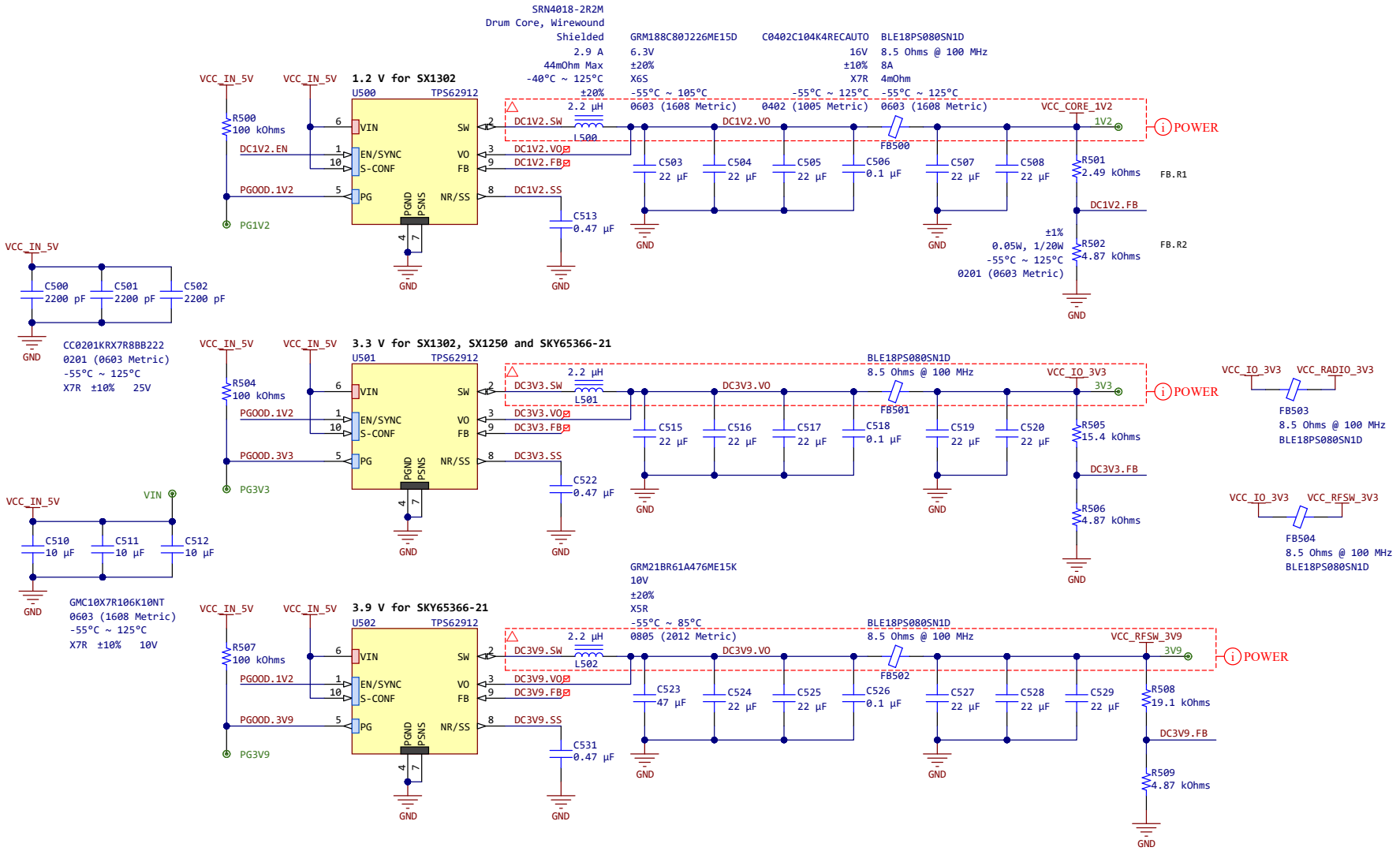


Figure 4.12 – LoRa module: Schematic of the DC/DC converters.

4.1.2 CubeSat PC/104 carrier

Figure 4.13 shows the low-level block diagram of the carrier board. The central component is the microcontroller. It manages the LoRa modules, arbitrates the RF path, interfaces with the satellite through the CSKB, and oversees the status of the power system. The MCU exposes ports for programming and debugging.

The complete schematic sheets are attached in section C.2, page 128.

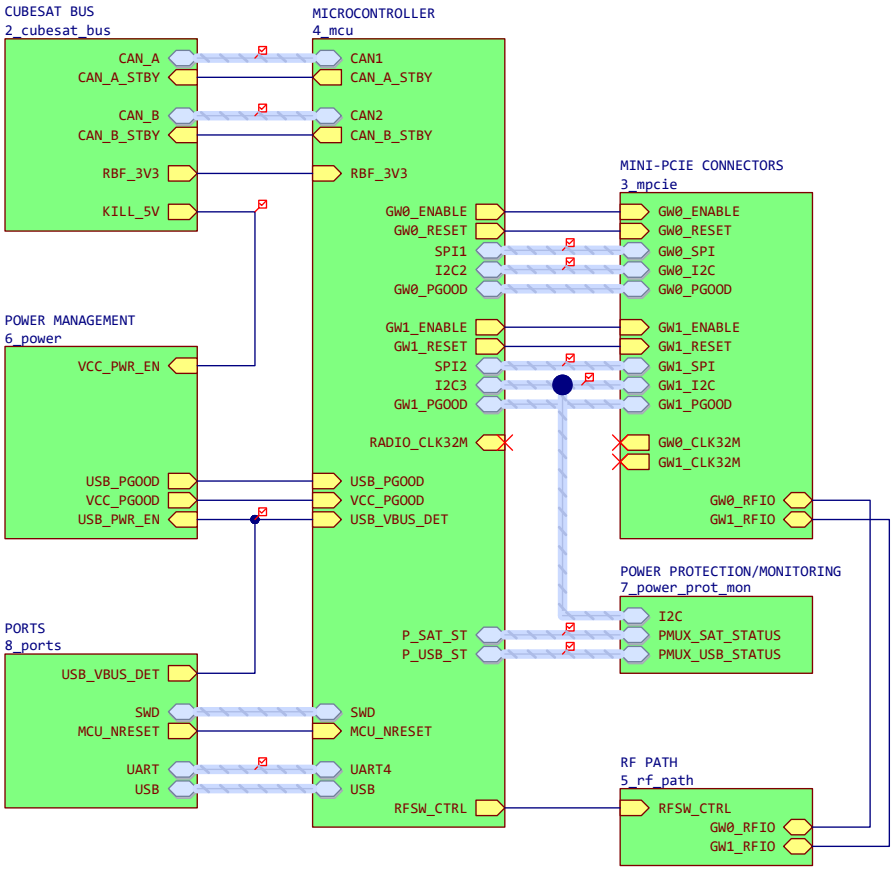


Figure 4.13 – Low-level diagram of the CubeSat Carrier.

4.1.2.1 Micro-controller unit

The circuit for the STM32L496RGT3 microcontroller is illustrated in Figure 4.14. Due to the extensive number of pins on the microcontroller unit, it is divided into several symbols, according to its region: ports A, B and C, power, and other pins.

The selection of the pins is based on the pin definition tables of the STM32L496 datasheet [120], with the objective of avoiding peripheral collisions while performing an optimal pin allocation for the subsequent PCB routing. This is a long and iterative process. The sheet symbol contains a multitude of pre-defined interfaces, rendering it readily reusable by the EGSE. All pins are utilized, with only a few remaining unconnected. This proves the microcontroller is optimally-suited for its use case.

The MCU uses a single 3.3 V power supply. In this design, the independent power supply for the USB peripheral is enabled only when a USB is connected, to reduce power consumption. For decoupling capacitors, a 100 nF capacitor is placed for each `VDD` pin, plus a large 4.7 µF decoupling capacitor for power supply stability [128].

A reset button and a boot select switch are provided [129]. The button is de-bounced with a capacitor and pull-up resistor.

The MCU clock is provided by a 32.768 kHz ± 10 ppm ABS07-32.768KHZ-9-1-T crystal oscillator. The microcontroller is expected to use its Multi-Speed Internal R-C oscillator (MSI) powered by the 32.768 kHz clock. The MSI can supply the system clock up to 48 MHz [120]. The circuit implementation follows the STM32 design guidelines [130]. Two series resistors are placed if necessary for signal integrity and clock power reduction. The capacitors provide the optimal load capacitance for the XTAL. If needed, they can be swapped by other values.

4.1.2.2 CAN transceivers

The MCP2542FDT-E/MF CAN transceivers (Figure 4.15) are intermediaries between the CAN physical layer and the microcontroller. They interface with the MCU via its dedicated CAN peripheral. The CAN bus is terminated by a parallel 120 Ω resistor for signal integrity. The transceivers are powered by the main 3.3 V supply and are enabled/disabled by its `STBY` signal [121].

4.1.2.3 RF switch

The SKY13396-397LF RF switch selects which LoRa module has access to the RF I/O port, and connects the other module to a 50 Ω load (Figure 4.16). The inputs and outputs pins are coupled with 100 pF capacitors. The 3.3 V power supply is filtered with a ferrite bead, and a 100 nF and 10 nF bypass capacitors are placed as recommended [131].

4.1.2.4 Power system

The power system in the carrier is composed of two eFuse power multiplexers, a current sensor and two low-noise DC/DC converters.

- **The TPS25947 eFuses** provide protection against electrostatic discharge, reverse polarity, overcurrent and overvoltage, and perform **power multiplexing** [132].

  When the primary power source (the CubeSat supply) is present and within the valid range, the primary device path powers `OUT` regardless of the status of the auxiliary power supply (the USB). The auxiliary device is kept off by forcing its `OVLO` pin high with the `AUXOFF` signal from the primary. After the primary supply voltage falls outside the user-defined operating range, the primary device de-asserts `AUXOFF`, which turns on the the auxiliary path.

- **The INA232 current sensor** measures the current consumption of the entire payload. The design follows the high-side-sensing typical circuit [133]. The value of the shunt resistor depends on the value of the maximum current to be sensed and the sense voltage. Setting a maximum sense voltage of 20.48 mV for minimum power dissipation, and considering a maximum current of 2 A (twice the expected):

$$R_{\text{shunt}} < V_{\text{sense}}/I_{\text{max}} = 10.24\,\text{m}\Omega \;\Rightarrow\; R_{\text{shunt}} = 10\,\text{m}\Omega\;;\; P_{\text{shunt,max}} \approx 42\,\text{mW} \quad (4.6)$$

- **The two DC/DC converters** output 3.3 V each,with one serving as the main supply and the other powers the MCU's USB peripheral. The converters adhere to the same configuration as previously illustrated in the modules (section 4.1.1.5, page 61). Consequently, their schematic is not elaborated upon in this section.

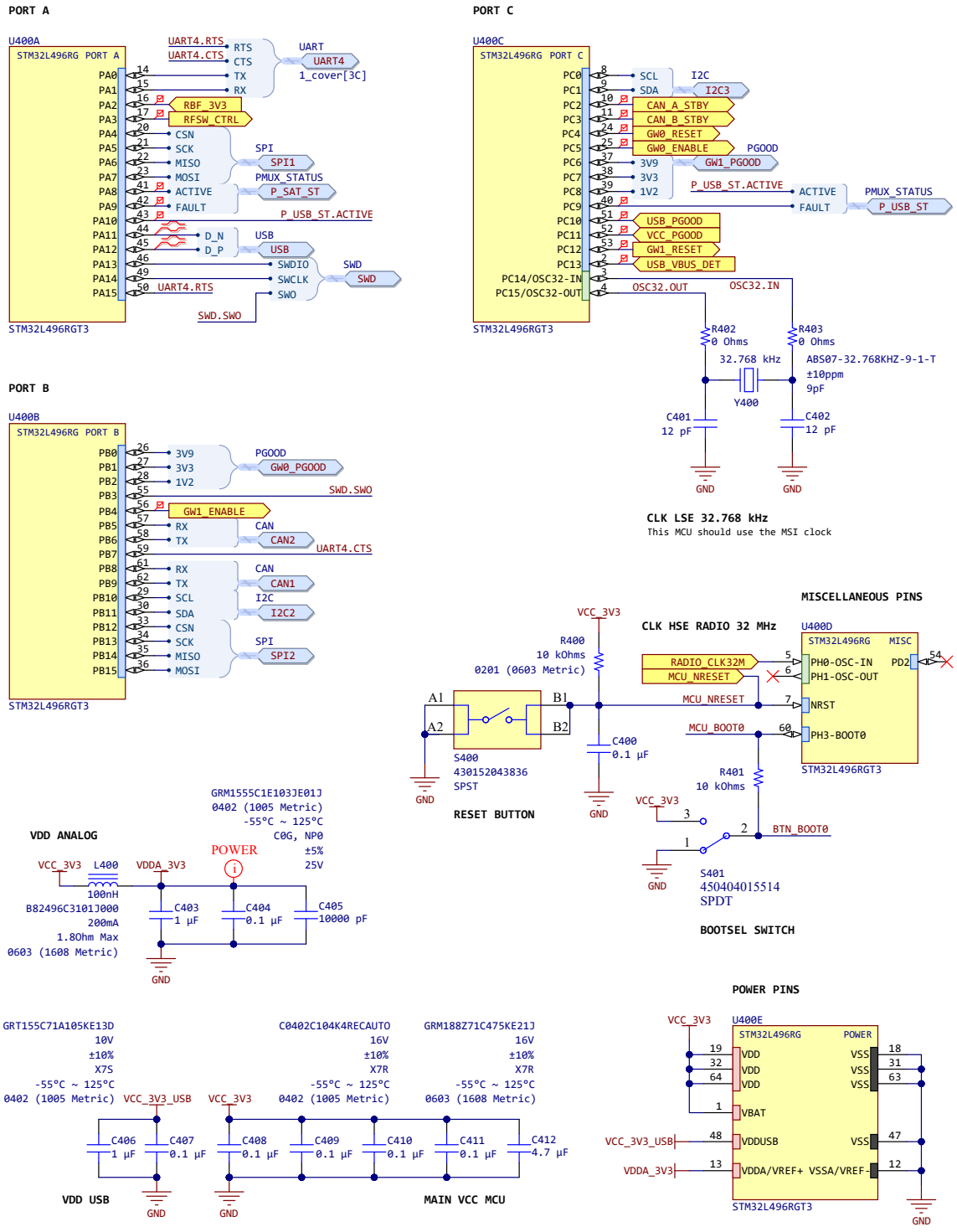


Figure 4.14 – Carrier: Schematic of the microcontroller unit.

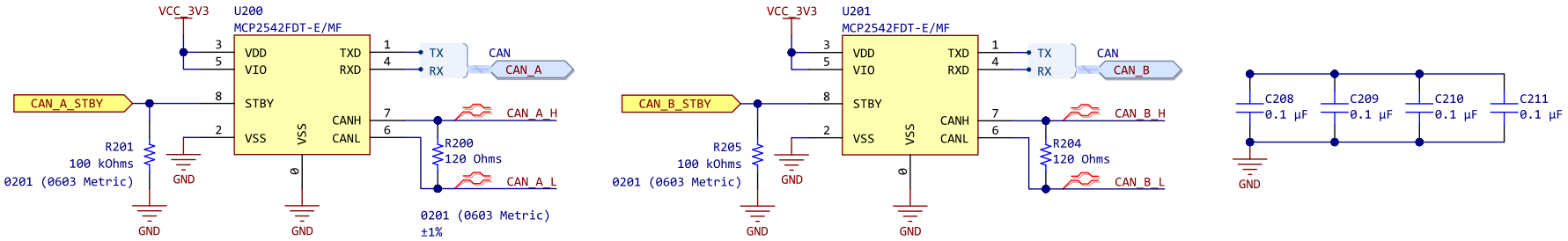


Figure 4.15 – Carrier: Schematic of the CAN transceivers.

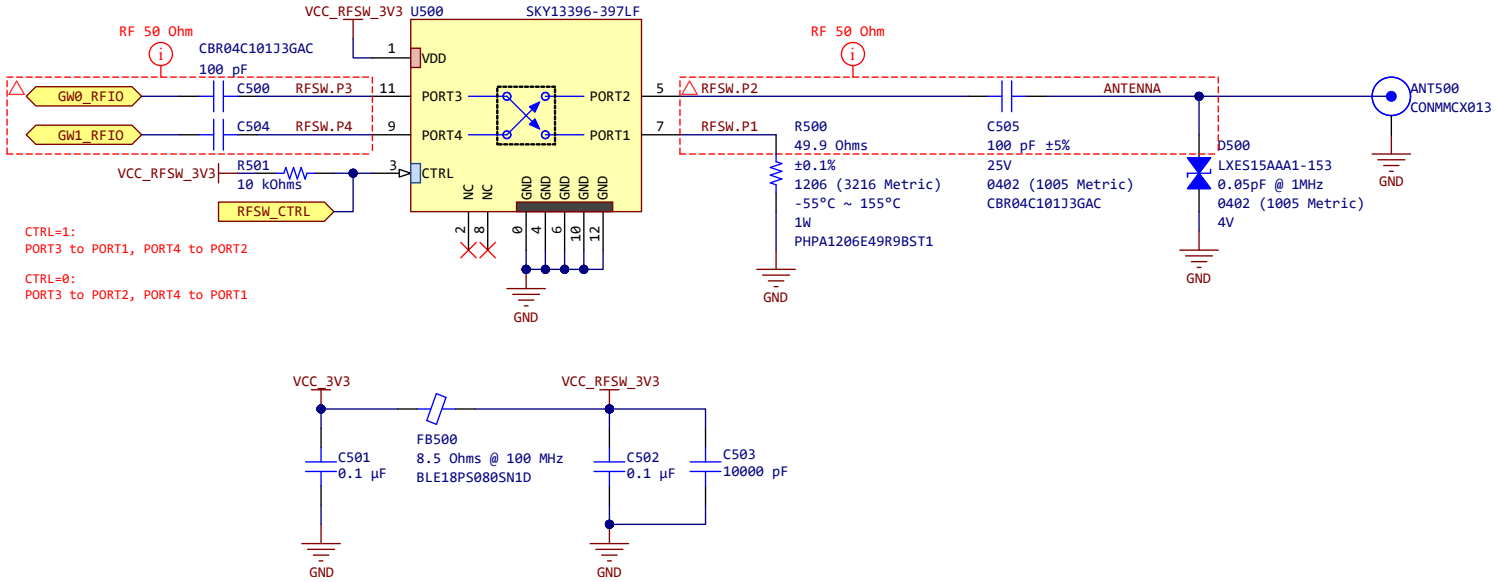


Figure 4.16 – Carrier: Schematic of the RF switch.

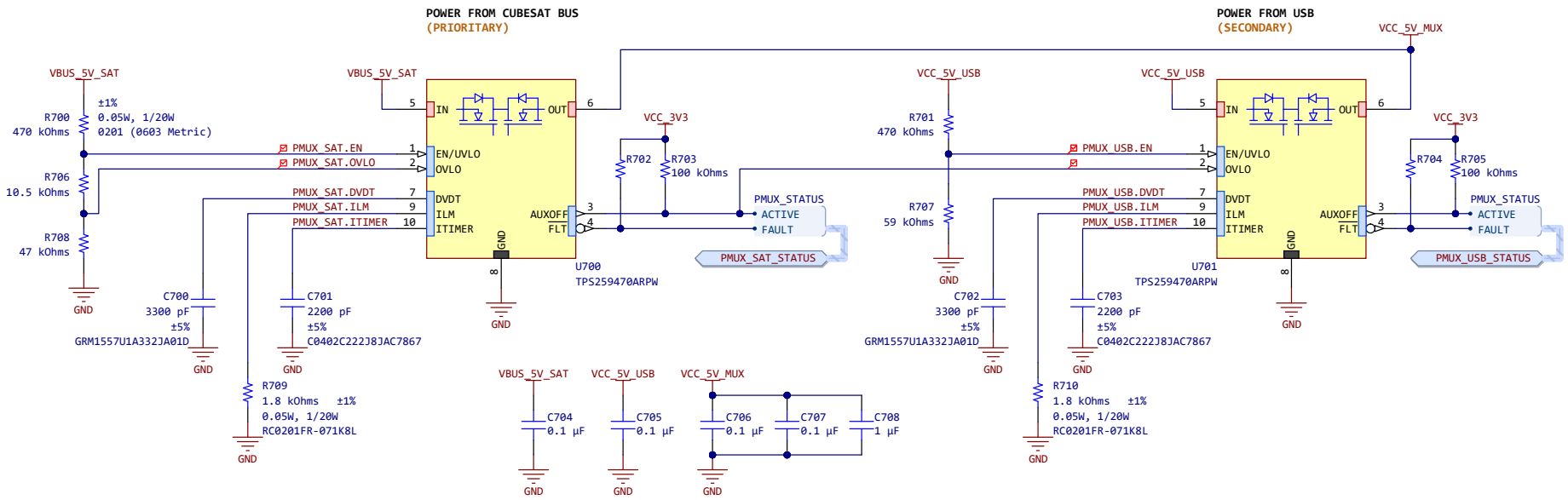


Figure 4.17 – Carrier: Schematic of the eFuse power multiplexor.

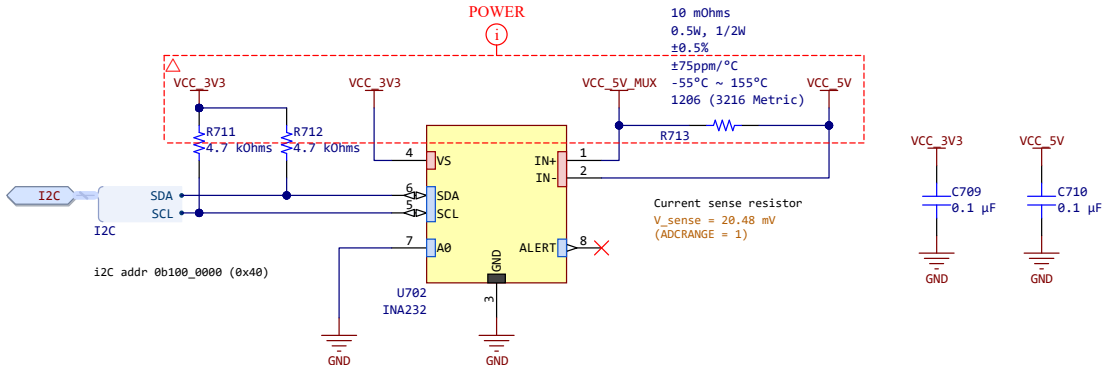


Figure 4.18 – Carrier: Schematic of the current sense.

4.1.2.5 Ports

- **The CubeSat Kit Bus (CSKB) port** circuit is shown in Figure 4.19a. It follows the pinout defined in Table 3.8. Most pins remain unconnected (NC). The power rails of the CubeSat headers contain basic protection against overvoltage and electrostatic discharge (ESD) by means of a TVS diode. Each power pin has a 100 nF decoupling capacitor, plus an additional 1 µF and 47 µF for supply stability.

  The `RBF` and `KILL` signals are expected to operate on 5 V logic. The `KILL` signal can be routed directly to the `ENABLE` pin of the DC/DC power converters for a complete shutdown of the entire payload. On the other hand, the `RBF` signal must be translated to 3.3 V logic for the microcontroller. A simple PMOS level shifter is implemented in Figure 4.19b.

- **The Single-Wire Debug (SWD) port** is wired as in Figure 4.20a. Two types of ports are provided: a FTSH-105 (10-pin, 2 rows x 5 columns, 1.27 mm-pitch male header) and an alternative Tag-Connect TC2030-ICD *pin-to-pad* connector.

- **The Universal Asynchronous Receiver-Transmitter (UART) port** is wired as in Figure 4.20b. It directly exposes a UART serial interface on the microcontroller. This bus can be used for debugging purposes or for direct communication with the OBC or other payload.

- **The Universal Serial Bus (USB) port** is implemented as in Figure 4.20c. The USB port is protected against overvoltage and electrostatic discharge (ESD) by the USBLC6-2SC6 IC, which contains low-capacitance TVS diodes for the power and data lines. For correct implementation of the USB standard, two 5.1 kΩ resistors are placed in parallel on pins `CC1` and `CC2`.

  The 5 V USB power rail is filtered by a ferrite bead and some decoupling capacitors. `USB_VBUS_DET` allows the MCU to detect when the USB port is connected.

- **The Mini PCI Express (mPCIe) connectors** appear in Figure 4.21. The wiring is very similar to that of the modules (compare with Figure 4.11).

4.1.2.6 Temperature sensors

The carrier has two STTS751-0DP3F temperature sensors (Figure 4.22), the same model used in the LoRa modules. One of them is placed in the center of the board, close to the major heat sources, while the other is placed in an extreme part of the board to assess the board temperature itself, without the influence of the nearby heat sources.

Each sensor is configured for the same address, but wired on separate I2C buses for collision avoidance and redundancy. The 12 kΩ pull-up resistor in pin `ADDR` sets the address to `0b100_1001` (`0x49`).

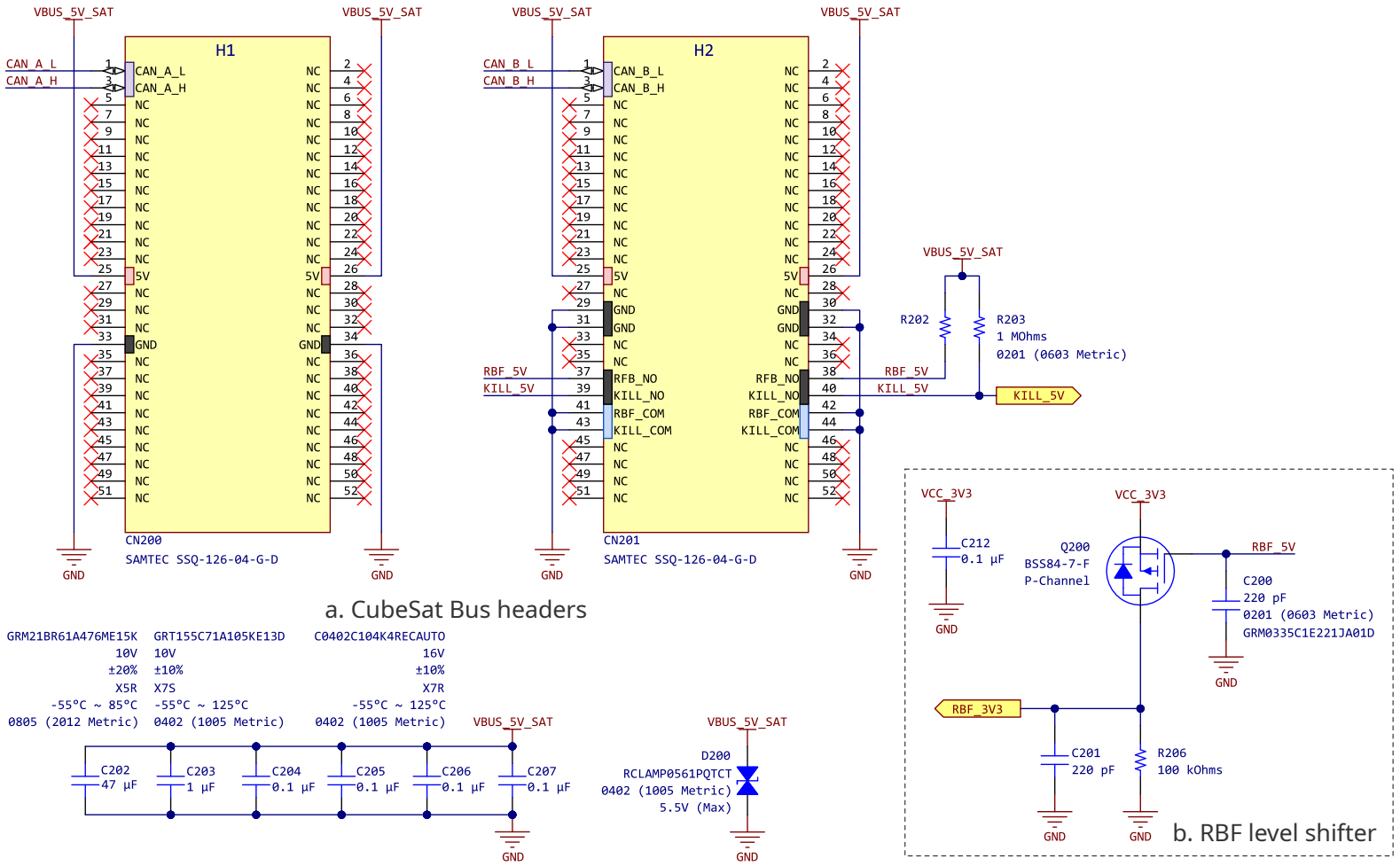


Figure 4.19 – Carrier: Schematic of the CubeSat Bus port.

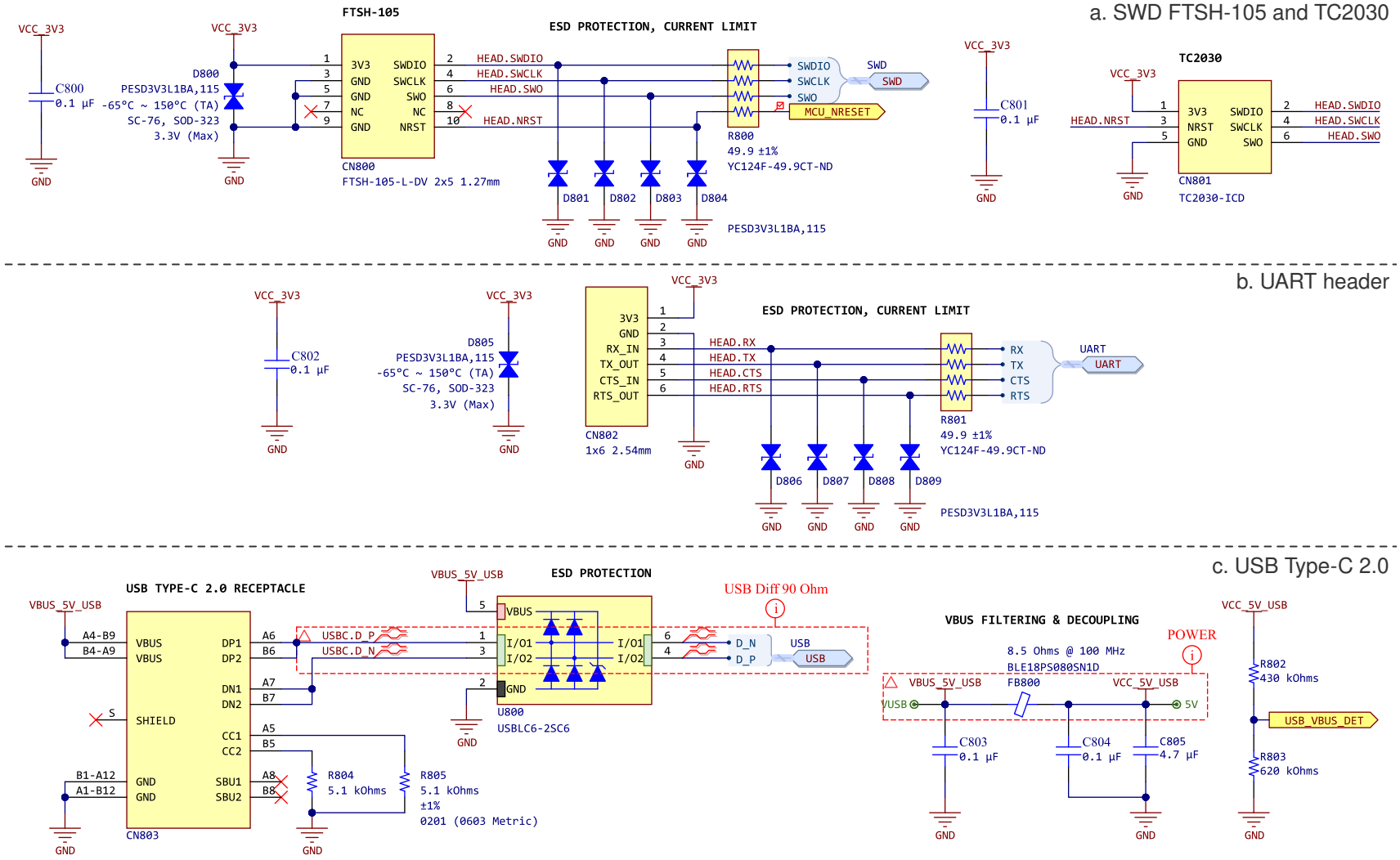


Figure 4.20 – Carrier: Schematic of the SWD, UART and USB ports.

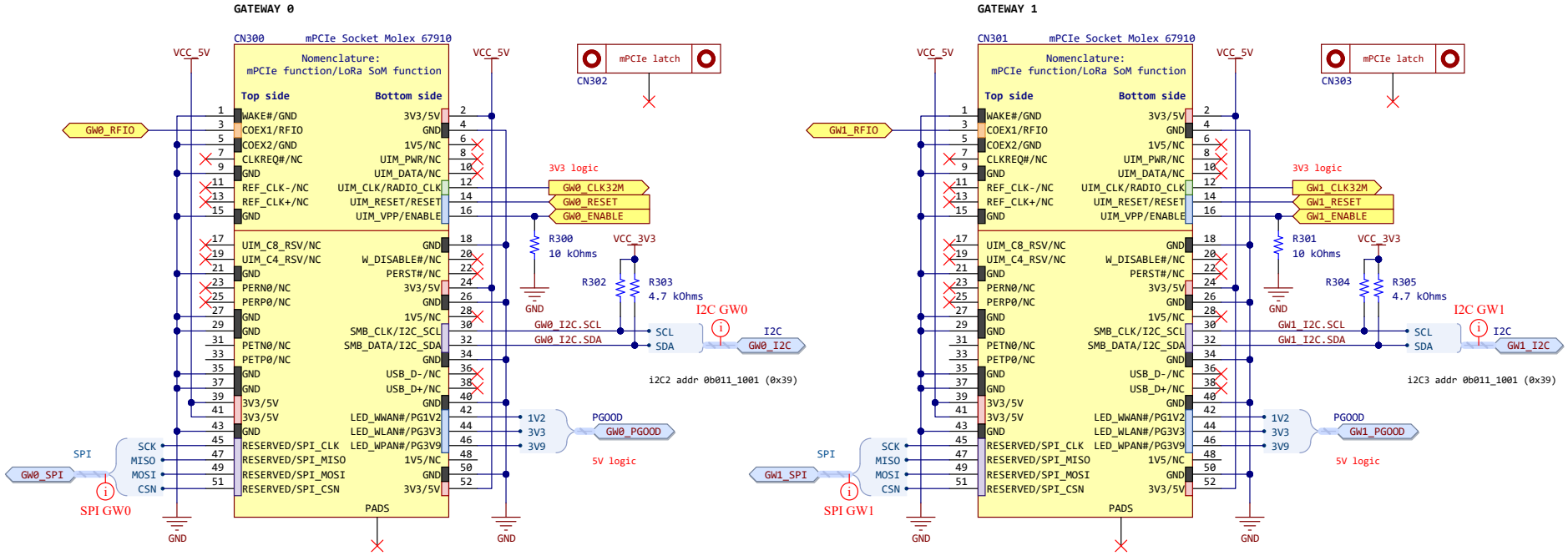


Figure 4.21 – Carrier: Schematic of the mPCIe ports.

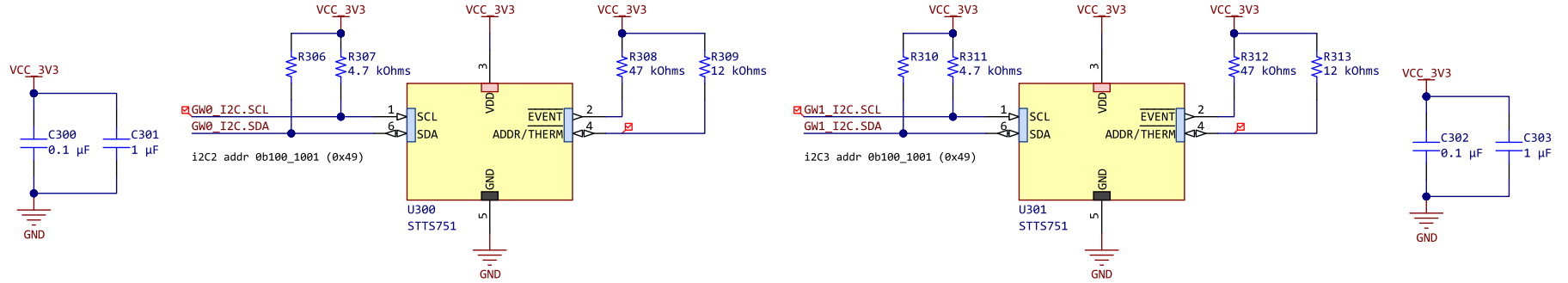


Figure 4.22 – Carrier: Schematic of the temperature sensors.

4.1.3 Electrical Ground Support Equipment

Figure 4.23 shows the block diagram of the schematics of the Electrical Ground Support Equipment (EGSE). As with the carrier, the design revolves around the microcontroller, which oversees the board via its peripherals and GPIOs. The EGSE connects to the payload via the CSKB header and an RF port. The EGSE integrates a LoRa end-device transceiver and associated RF circuitry to evaluate the payload's performance.

As many circuits are analogous to those previously described in section 4.1.1 (page 53) and 4.1.2 (page 64), the schematics of the MCU, CAN transceivers, ports, and the power system are not discussed in this section. Instead, the focus is on the RF chain specific to this PCB. The complete schematics are attached in section C.3 (page 136).

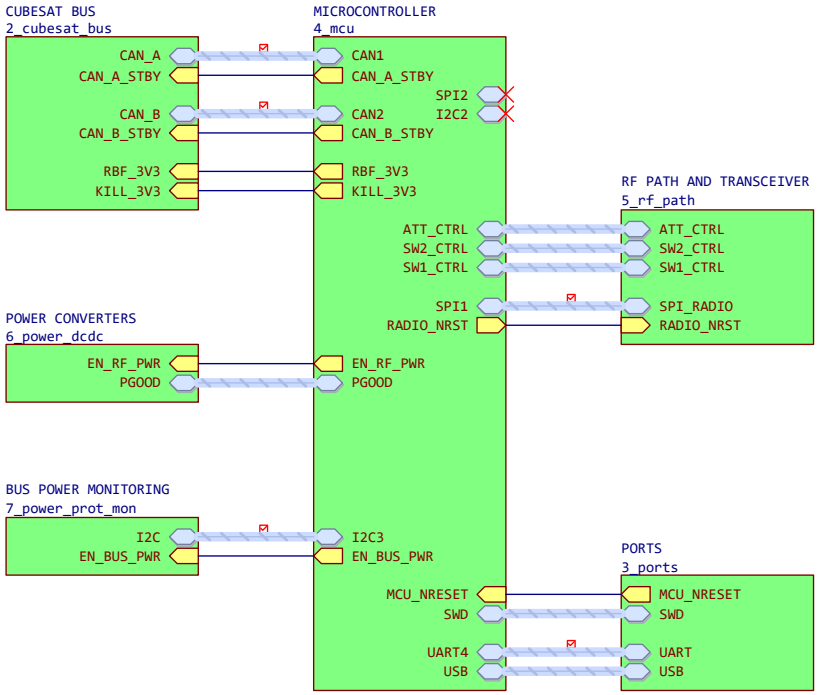


Figure 4.23 – Low-level diagram of the electrical ground support equipment (EGSE).

4.1.3.1 Radio-Frequency block chain

The RF chain is composed of several blocks, as illustrated in Figure 4.26. From left to right and top to bottom, the blocks are:

- **The transceiver block** comprises the SX1276 LoRa end-device transceiver and associated electronics.
- **The frontend module** consists of a SKY65366-21 LNA + PA + RF switch, in a configuration very similar to the schematics described in section 4.1.1.2 (page 55).
- **The RF switches** (Figure 4.29) route the signal from the end device transceiver and/or payload to each other, a matched 50 Ω load, or an SMA port.
- **The attenuator block** attenuates the RF signal to prevent damage to the EGSE and payload transceivers when they are directly connected.
- **The Chebyshev bandpass filter and the LC lowpass filter** are identical to those described in section 4.1.1.2 (page 55).

- Finally, before the antenna port, the design includes a **DC-block capacitor** and a low-capacitance **TVS diode** for ESD protection.

4.1.3.2 LoRa end-device transceiver

The SX1276 transceiver appears in Figure 4.27a. The design is based on Semtech's reference designs [134], [135]. The SX1276 directly connects with the microcontroller via a SPI interface. The transceiver is driven by an FT2MNTUM-32.0-T1 TCXO (Figure 4.27b), the same 32 MHz ± 0.5 ppm XTAL as the modules, to compact the bill of materials (BOM).

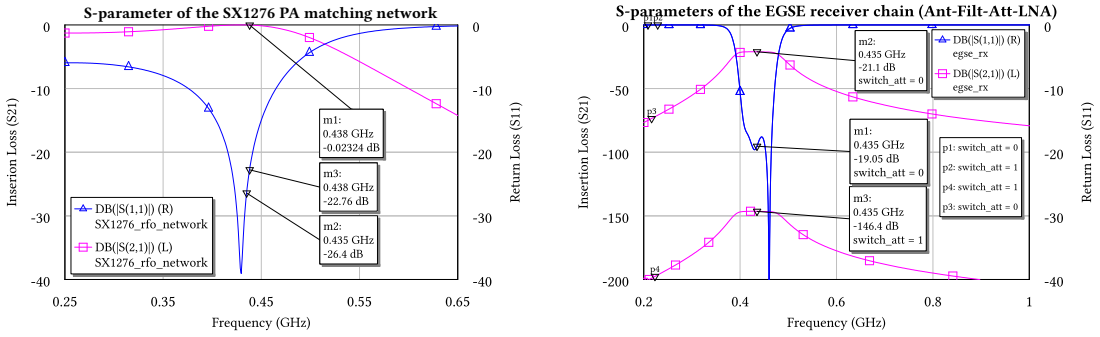
The circuit includes several passive networks for filtering and impedance matching:

- In contrast with the SX1250, the SX1276 input is single-ended, thus obviating the necessity for the implementation of a balun [63], and only **a matching network is required** (Figure 4.27c). As with the SX1250, the input impedance is not characterized by Semtech. The topology and values are based on the reference design [134], [135]. The components are placeholders, and the values are expected to change after the transceivers are characterized[3].
- **The PA matching network** adapts the 50 Ω line impedance to the optimal for the power amplifier. The manufacturer provides a single figure for 435 MHz, $Z_{opt} = 65.2 - j1.7\,\Omega$, for an unspecified output power [135]. The circuit topology in Figure 4.27d is based on the recommended designs [134], [135]. While component values are feasible, they are placeholders until properly tested.

4.1.3.3 RF attenuators

The attenuator chain is composed of two stages. The first stage of attenuators is composed of the Mini-Circuits YAT-3A+ and YAT-30A+ chips, which dissipate the most power in the chain and protect the RF ICs by limiting the input RF power to a safe level. The second stage consists of four Mini-Circuits DAT-31R5A-PP+ variable attenuators. These simulate the FSPL and together provide 6 dB to 132 dB of attenuation.

Simulations of the complete receiver chain are attached in Figure 4.24, taking into account the maximum and minimum attenuation paths chosen by switches (see Figure 4.25). Impedance matching is good in the band of interest and transmitted power reaches the expected values, considering the presence of the attenuators and the LNA.



(a) Simulation of the PA matching network.

(b) Receiver chain simulation, both paths.

Figure 4.24 – EGSE: S-param simulations of the receiver chain and PA matching network.

[3] See section 5.3.1: Discussion on design flaws and improvements, page 102.

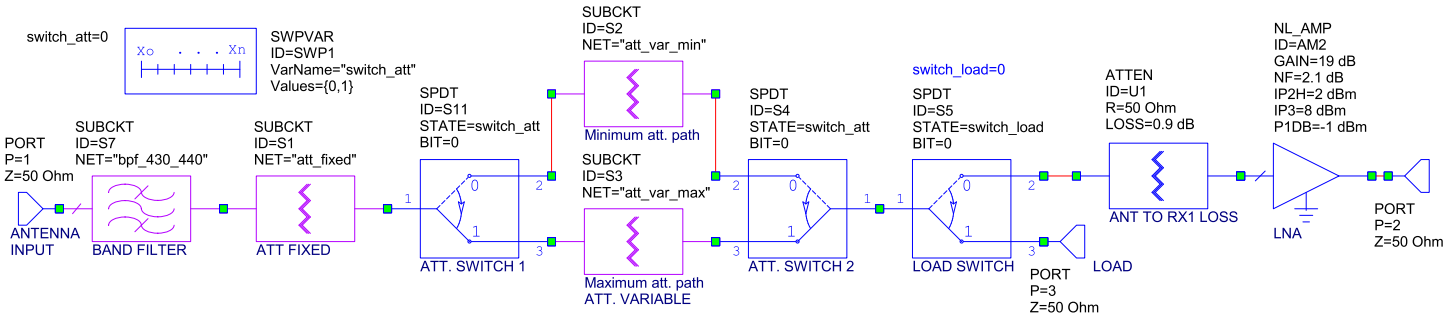


Figure 4.25 – EGSE: Schematic of the filtering of the control signals for the RF chain.

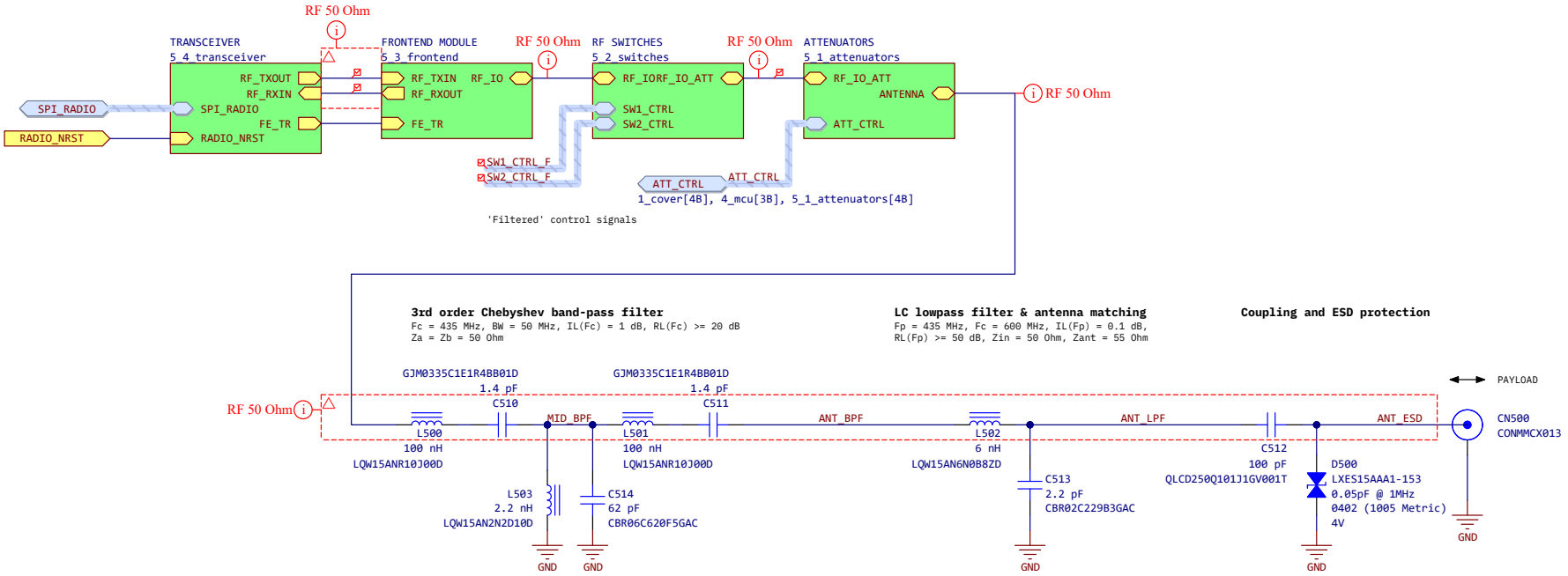


Figure 4.26 – EGSE: Schematic of the RF chain.

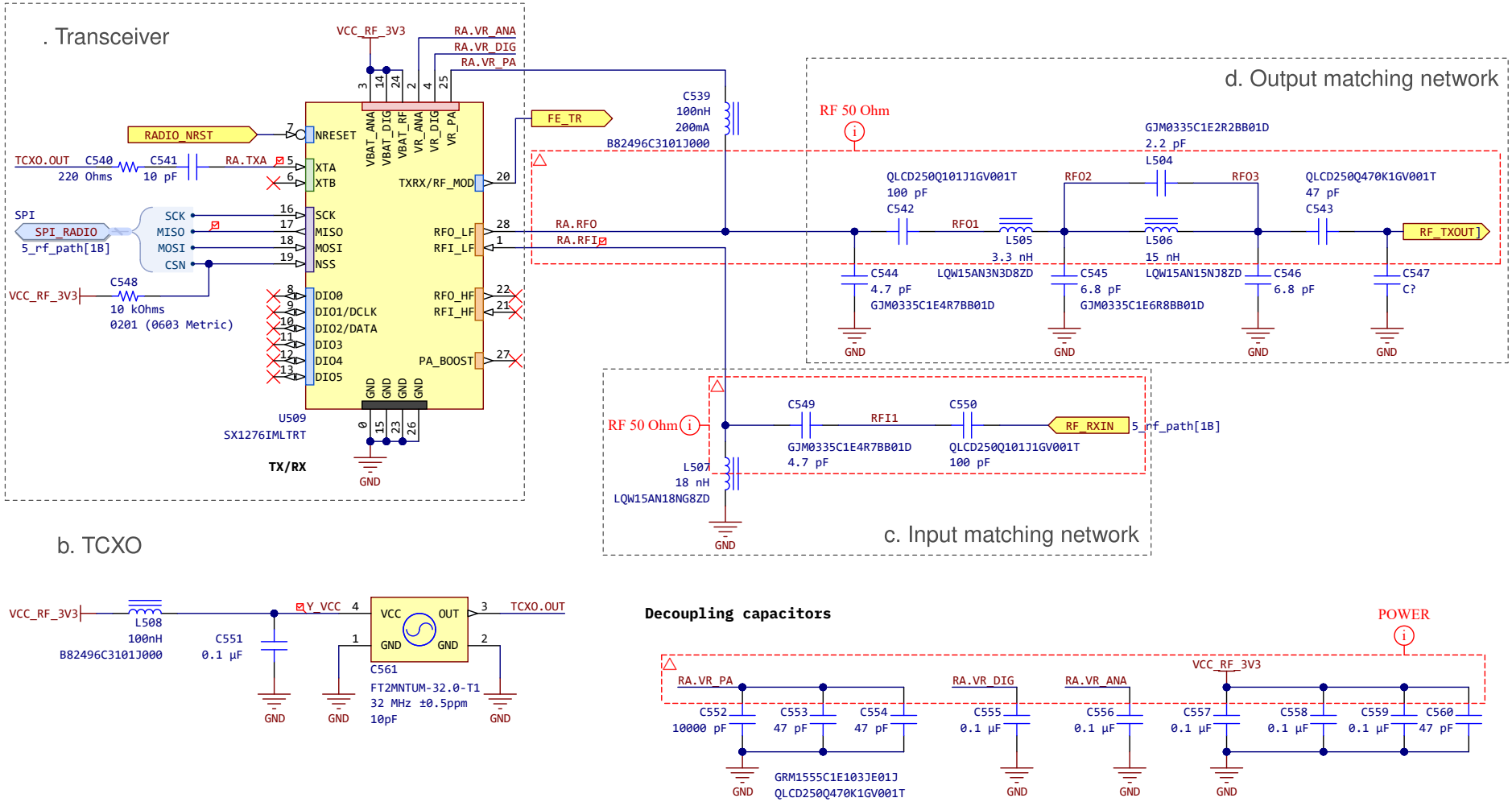


Figure 4.27 – EGSE: Schematic of the LoRa end-device transceiver and oscillator.

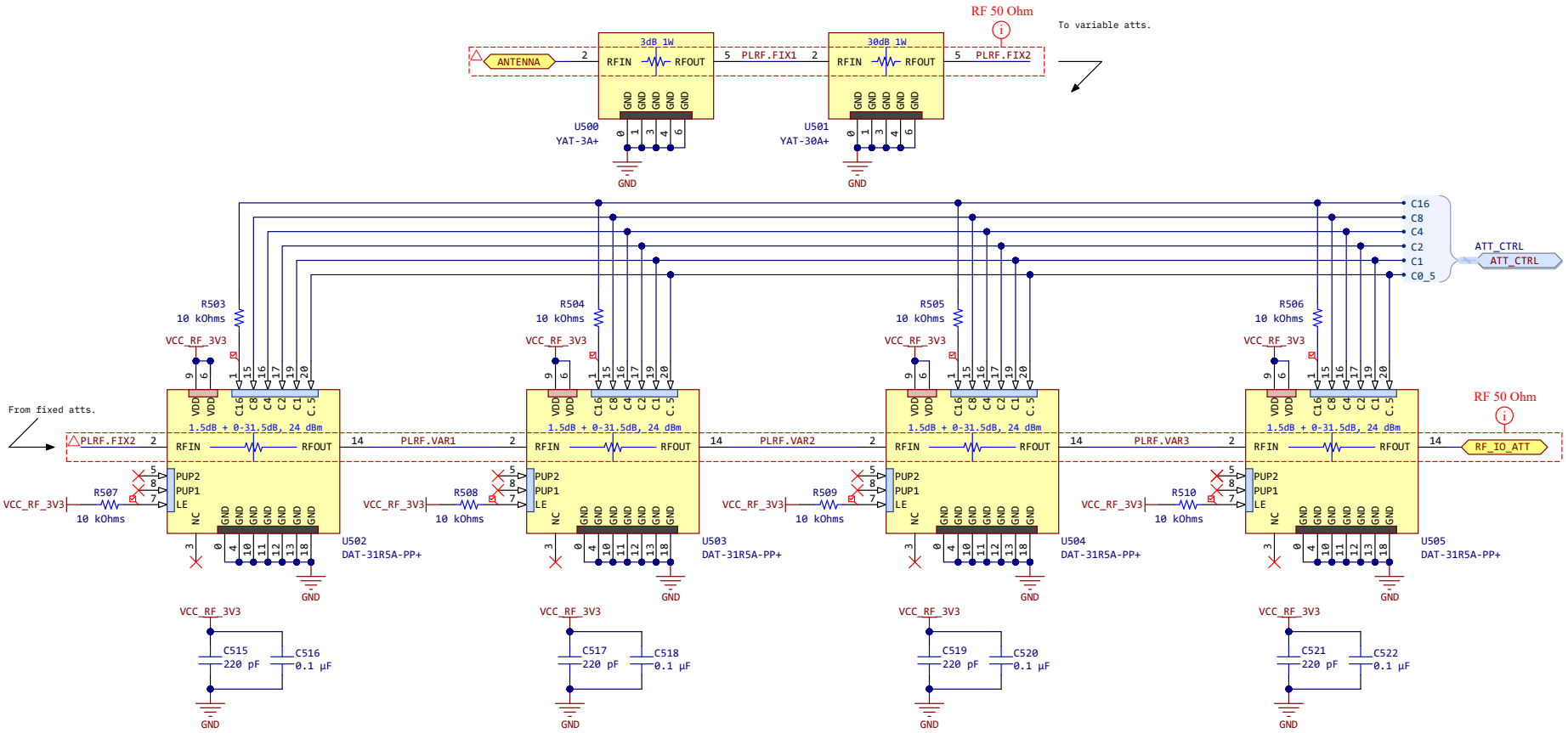


Figure 4.28 – EGSE: Schematic of the RF attenuators chain.

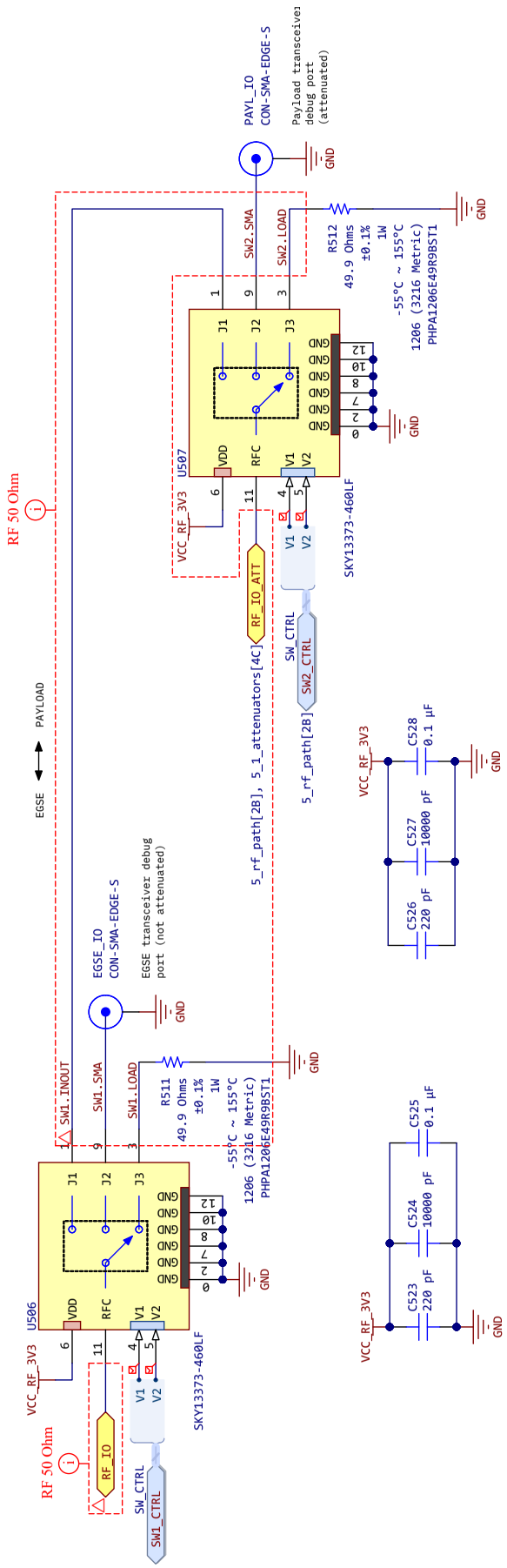


Figure 4.29 – EGSE: Schematic of the RF switches.

4.2 Printed circuit board design

4.2.1 Design rules

PCB editors allows the declaration of design rules according to design and manufacturing constraints: trace widths, clearances, hole sizes, etc. These rules form an instruction set for the Design Rule Checker (DRC), which assists the engineer in attaining producible designs. It is anticipated that the PCBs will be manufactured by Circuit Labs S.A. Therefore, we must adhere to the manufacturer's materials [136], capabilities [137], and tolerances [138]. PCBs will adhere to the rules of the Class 6 manufacturing process. These rules were manually imported into Altium Designer.

4.2.2 Stackups

The modules follow the mPCIe form factor and must have a total PCB thickness of 1 mm. Due to the inherent complexity of the LoRa modules –a compact, dense, mixed-signal design with controlled impedance constraints–, it has been determined that a 6-layer stackup is a sufficient and optimal choice (building no. 160 [139]). The substrate will be Isola PCL 370HR, a high-T_g FR-4. This material is suitable for prototyping without the outlay of more specialized substrates. [136]. The stackup is shown in Figure 4.30a.

The carrier follows the CSKB form factor. The stackup is 6 layers, 1.6 mm thick (building no. 424 [139]), see Figure 4.30b. The thickness gives the board rigidity, and the 6-layer stackup reduces the distance between a signal layer and its ground plane, achieving low impedance with thin microstrip traces, necessary for small IC footprints. The substrate is Isola PCL 370HR FR-4. The EGSE uses the same stackup as the carrier, since the requirements are similar, facilitating BOM consolidation and PCB panelization.

All boards follow the following layer assignment:

L1 Top layer, signal, microstrip, for digital and RF, controlled-impedance signals.

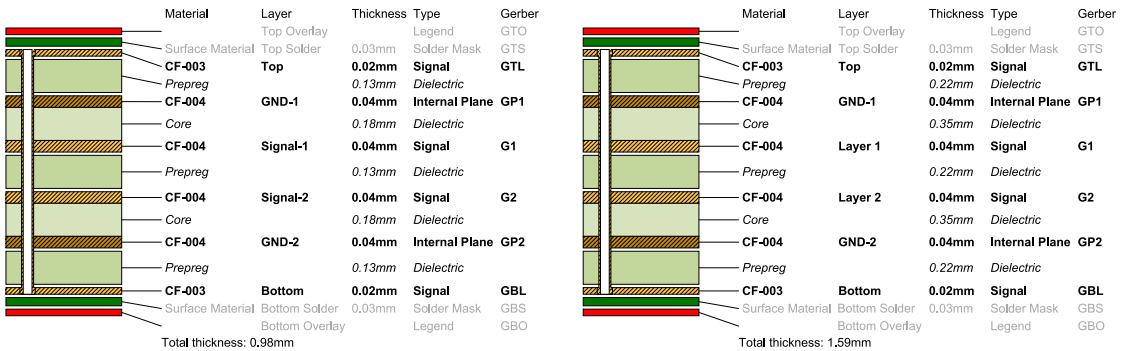
L2 GND plane.

L3 Internal signal layer, stripline, for non-critical digital signals.

L4 Internal layer for the distribution of the power rails using planes/polygons.

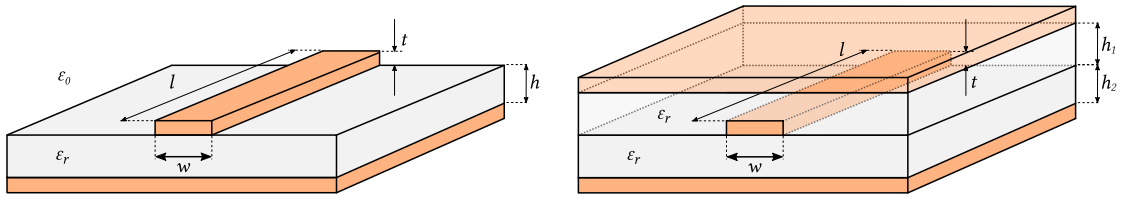
L5 GND plane.

L6 Bottom layer, signal, microstrip.



(a) Stackup for the modules (no. 160). **(b)** Stackup for the carrier/EGSE (no. 424).

Figure 4.30 – Modules, carrier and EGSE PCB stackups.



(a) Structure of a microstrip.

(b) Structure of a stripline.

Figure 4.31 – Structure of a microstrip and a stripline. ε_o is the dielectric constant of vacuum, and ε_r the dielectric constant of the substrate; w, l and t are the conductor dimensions; and h the substrate height. Modified from [140].

4

4.2.3 Trace width, controlled impedance and via sizes

Tools such as WCalc [141], QUCStrans [142], KiCAD PCB calculator [143], Saturn PCB Toolkit [144] or Altium Designer can determine the trace width needed to achieve a given impedance based on mathematical models of microstrip and stripline (see Figure 4.31). Table 4.1 summarizes the trace width for each net class. Controlled-impedance signals are routed in the outer layers, as stripline models tend to be less accurate in stackups with few ground planes because reference planes are not clearly defined [145].

For the power traces, a 0.3 mm trace is estimated to handle 1.2 A of current for a temperature increase of 10 K in both stackups, while a 0.5 mm trace can handle up to 1.7 A. These figures have been calculated using Saturn PCB Toolkit [144].

In terms of vias, the design will use only thru-hole, non-tented vias for reliability. Tented vias can cause problems with outgassing under vacuum [145]. Two types of vias are employed: a *small* via, designed for fanout and routing of signals, at the limit of the manufacturer's class 6 specifications [138]; and a *regular* via with a larger hole and higher current rating, intended for power routing (see Table 4.2).

Net class	**Target impedance**	**Trace width** (mm)							
		Modules				**Carrier and EGSE**			
		Ext. layers		**Int. layers**		**Ext. layers**		**Int. layers**	
		Min.	Pref.	Min.	Pref.	Min.	Pref.	Min.	Pref.
RF	50 Ω	–	0.41	–	–	–	0.23	–	–
USB	(diff pair*) 90 Ω	–	–	–	–	–	0.27	–	–
CAN	–	–	–	–	–	–	0.20	–	–
Power	–	0.30	0.50	0.30	0.50	0.30	0.50	0.30	0.50

Table 4.1 – Trace widths in each net class. Impedance is calculated using Altium Designer. Min: minimum trace width, Pref: preferred trace width. *Conductor spacing: 0.13 mm

Via	d (mm)	**Annular ring** (mm)		h (mm)	Z (Ω)	L (nH)	C (pF)	f_r (GHz)	I (A)
		Ext. lay.	**Int. lay.**						
Small	0.2	0.1	0.15	1.0	22	0.7	1.5	6.9	0.9
				1.6	23	1.3	2.5	4.1	1.3
Regular	0.3	0.15	0.15	1.0	26	0.8	1.2	8.8	1.1
				1.6	27	1.4	2.0	6.7	1.6

Table 4.2 – Via sizes and ratings. d: hole diameter, h: height, Z: AC impedance, L: inductance, C: capacitance, f_r: self-resonant freq., I: rated current. Calculated using Saturn PCB Toolkit.

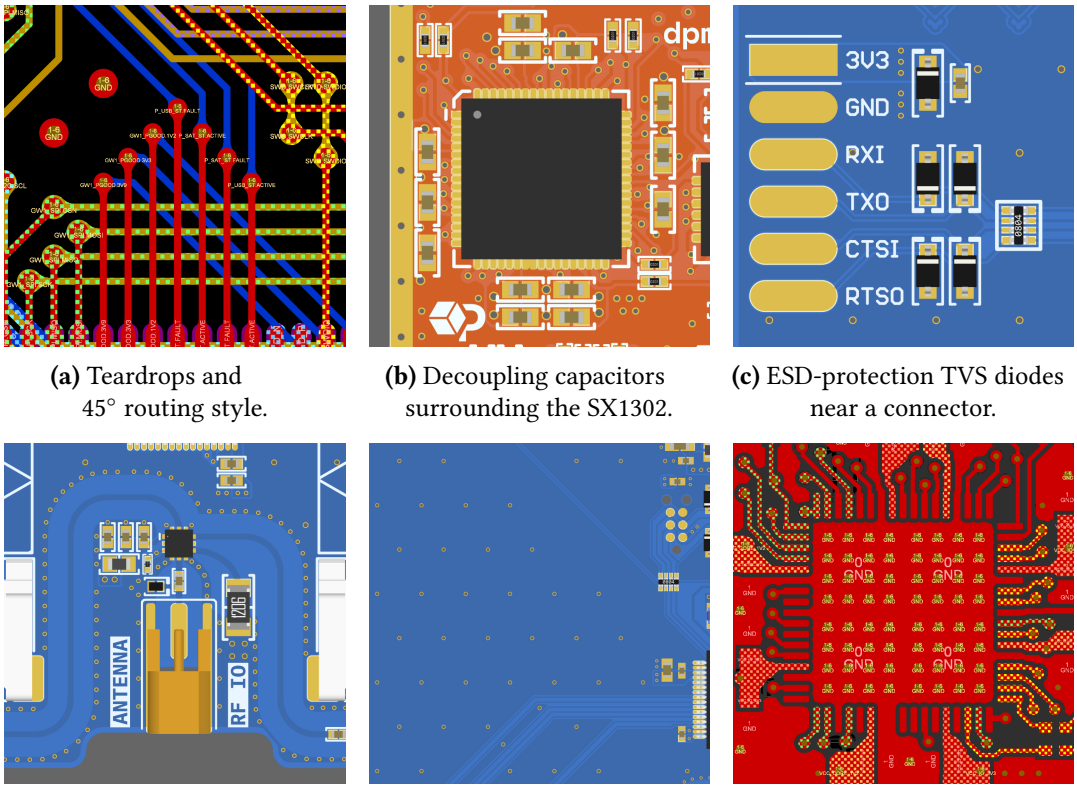
4.2.4 Best practices

This section details best practices and conventions used throughout the development of the three PCBs to avoid common manufacturing problems, noise, and EMI.

- **Controlled impedance tracks are routed on a single layer**, without vias [145].
- Despite the relatively low speed of interfaces, **tolerance rules for trace length** are incorporated into bus lines such as USB, CAN, and SPI to prevent time-of-arrival related issues. Track length should be minimized when possible [145].
- **Trace routing angle** is not a significant concern, with the exception of microwave and high-speed signals, where they can radiate at sharp turns [123], [146], [147]. Therefore, it has been decided to maintain a routing angle of 45° as the default for digital signals, and rounded corners for RF signals (see Figure 4.32a and 4.32d).
- **Ground planes** provide a good quality reference and allow the traces to be designed as microstrip or stripline (see Figure 4.31). The chosen 6-layer stackup ensures the presence of continuous and close reference planes in all signal layers (see Figure 4.30). To be effective, a ground plane must be combined with good return path management techniques such as via stitching and shielding. The same ground plane is used for the power, RF and digital, rather than separate planes, to avoid discontinuities [146]–[150]. Good layout, zoning and routing practices are used instead (see section 4.2.5: Overview of the printed circuit boards, page 83).
- **Via shielding** is a technique in which one or more rows of vias are placed along a signal trace (Figure 4.32d). The use of via shielding has been shown to reduce crosstalk and EMI and is widely used to shield RF traces [123], [147]
- **Via stitching** (Figure 4.32e) is used to connect large areas of copper assigned to ground on different layers to create a strong vertical electrical (and thermal) connection through the board, maintaining low impedance and short return loops for the best possible ground quality. Via stitching also connects areas of copper that might otherwise be isolated from their network [123]. This helps keep circuit loops small, with low parasitic inductance and therefore low coupling [147], [148].
- **Thermal relief pad and vias** (Figure 4.32f). The thermal relief pad offers both thermal relief and a solid ground reference to the chip. Thermal vias provide an excellent means of conducting heat from the components to the internal copper planes, thereby distributing heat across the board [115], [123], [151].
- **Teardrops** are copper fillets that extend from the trace to a pad or via, increasing the strength of the connection to thermal and mechanical stress (Figure 4.32a). This feature is beneficial when design objects are small and mitigates the adverse effects of drill wander and layer misalignment during fabrication [152], [153].
- **Crosstalk, clearance and zones.** Non-critical signals, such as low-speed buses, may be routed together in bundles disregarding crosstalk between them. In the case of critical signals, which require high-quality signal integrity (*e.g.*:, RF, high-speed, clocks, and so forth), clearance is provided to avoid crosstalk. Zone management is employed to separate power, RF and digital circuitry [145]–[148], [150].
- **Power is routed using polygons and oversized traces** (see Figure 4.36a, 4.41a and 4.46a), to properly respond to sudden increases in power consumption, avoiding voltage drops or trace heating due to reduced path resistivity [123], [150].

- **ESD-protection circuits are placed near the ports** to avoid further propagation of the electro-static discharge, as shown in Figure 4.32c [147], [154].
- The carrier employs **plated, insulated mounting holes with head landings**. The plating and head landings protect against mechanical stress. The isolation prevents noise injection as the CubeSat structure can act as an inadvertent antenna [155]. CubeSat subsystems typically expose ground through their I/O interfaces, so there is no ground isolation between them and ground loops can form. This issue is irremediable, as it depends on the COTS. Single-point grounding has been identified as the most advantageous option for *Estigia* in terms of EMC [155].
- **Decoupling capacitors** are a common and effective technique for noise and ripple filtering on power traces. Decoupling capacitors are located close to the power pins of a chip to reduce loop inductance (see Figure 4.32b). They provide a charge reserve that is physically close to the chip and supplies energy to it during pulsed power draws; preventing the supply voltage from decaying [123], [146], [147].

  Large capacitors are good power reservoirs and good low-frequency filters, but they are not effective at high frequencies, and have a slow charge constant, thus increasing power-on inrush current. For digital chips, decoupling capacitors are usually the order of 100 nF (exact values are not critical), which offers a good compromise between size, capacity and frequency response. It is a common practice to place several capacitors in parallel with different sizes and capacities to reduce their equivalent series resistance (ESR) and filter a broad spectrum [147].



(a) Teardrops and 45° routing style.

(b) Decoupling capacitors surrounding the SX1302.

(c) ESD-protection TVS diodes near a connector.

(d) Via shielding and round routing style.

(e) Via stitching in the carrier PCB.

(f) Thermal pad and vias in the SX1302's footprint.

Figure 4.32 – Details of good practices employed in the design of the PCBs.

4.2.5 Overview of the printed circuit boards

This section reviews the layout and routing of the three developed PCBs. These are the result of multiple iterations of component placement and routing. The design revisions presented here have zero electrical rule check (ERC) violations and zero warnings.

4.2.5.1 LoRa modules

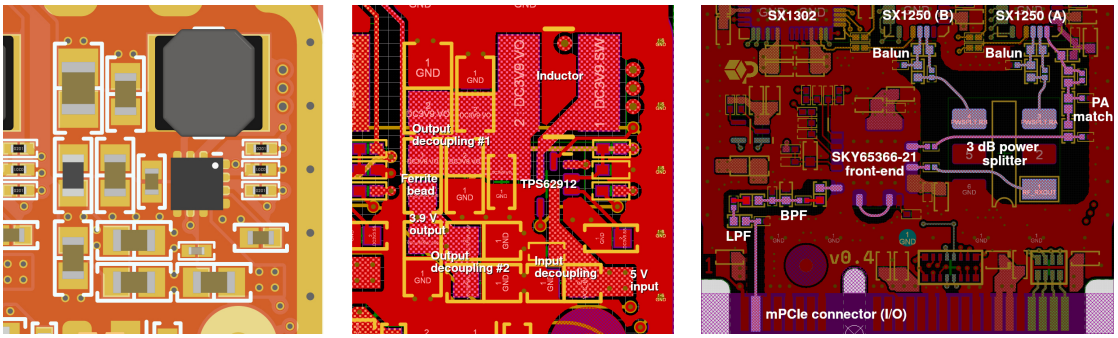
The design of the boards is inspired by Semtech's LoRa gateway reference designs [102]–[105] and Nebra's open source LoRa mPCIe gateway [106]. The design adheres to the specifications set forth by Semtech for RF and PCB design [123], [125].

The LoRa modules are divided into three distinct zones: RF, digital, and power. The RF stage is situated close to the mPCIe port to minimize losses and noise coupling from other zones. Given that the LoRa ICs are the intermediary between the digital and RF stages, they are positioned in the center. The potentially most noisy stage, power, is relegated to the far end of the board. In the mPCIe port, the left portion of the upper layer is reserved for the RF I/O signal, while the right is allocated for digital signals.

Most of the components are in the top layer to facilitate assembly and soldering. The bottom layer contains only the optional series resistors for the debug port. The debug port and the test points are realized with unpopulated pads in the bottom layer. This placement allows these pads to be connected with pogo pins for future debugging[4]. Test points are close to the circuit they are relevant to. This placement allows these pads to be connected with pogo pins for future debugging. The result of having almost every component in the top layer is that the LoRa modules are space constrained, and consequently the layout has been compacted to the maximum.

The layout of the DC/DC converter (Figure 4.33a) follows the recommendations by Texas Instruments [119], [156], although it has been compacted and the optional clearance for the inductor for noise reduction is not present. The layout of the RF stage is shown in Figure 4.33b. Whenever possible, the RF signals have clearance from other components and the top ground polygon pour to avoid affecting the RF traces.

All relevant layer prints of the LoRa modules are shown in Figure 4.34. However, the internal ground planes and drill drawings are of limited interest to the reader. In the following sections, only the top, bottom, and internal signal copper layers, as well as the solder masks and overlay layers, are presented, as shown in Figure 4.35 and 4.36. See section D.1 (page 150) for the complete PCB prints of the LoRa modules.



(a) DC/DC converters. **(b)** RF path.

Figure 4.33 – LoRa modules: Layout and routing of the DC/DC converters and RF path.

[4] See the breakout board in section 5.3.1: Discussion on design flaws and improvements, page 102.

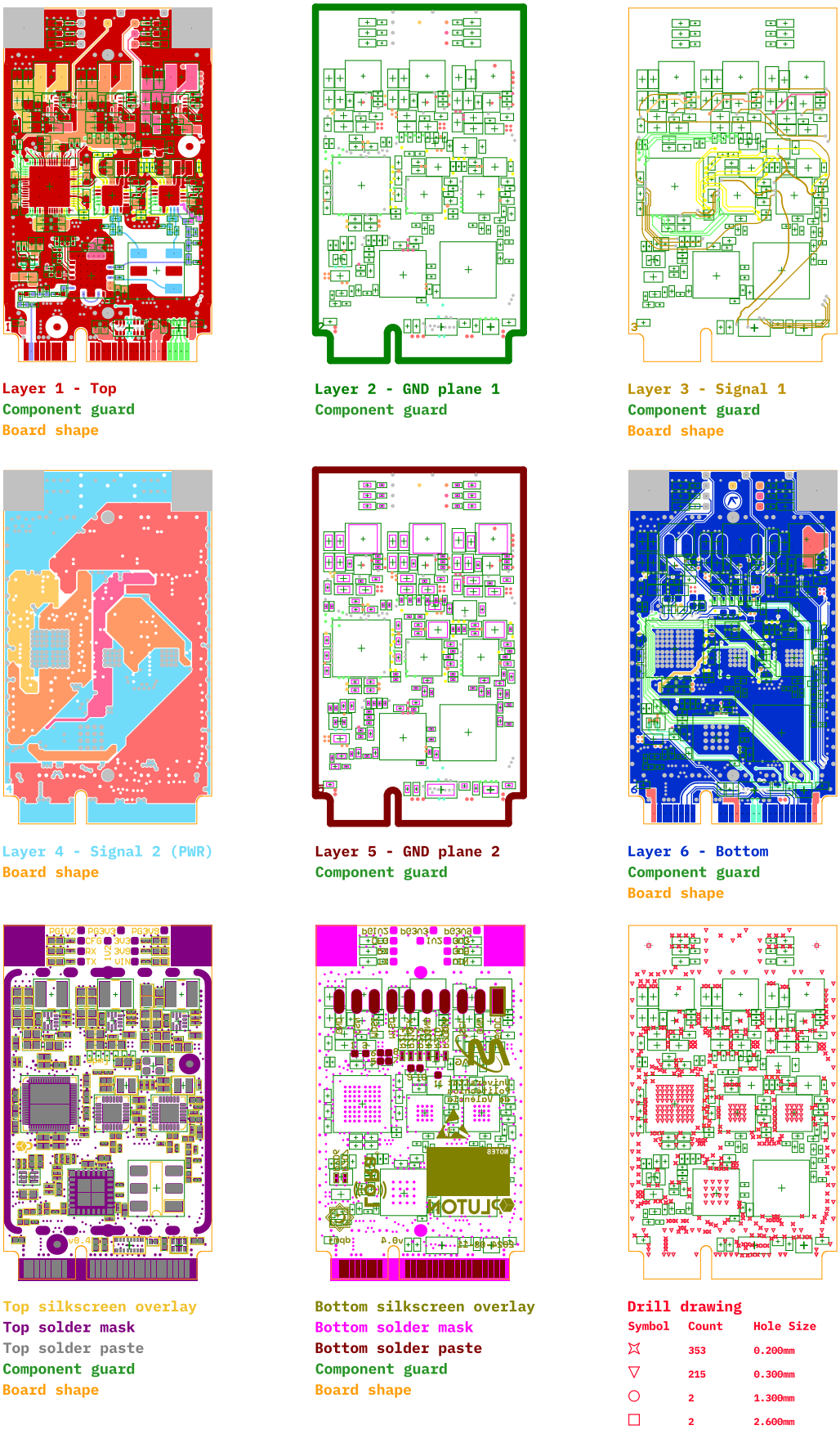
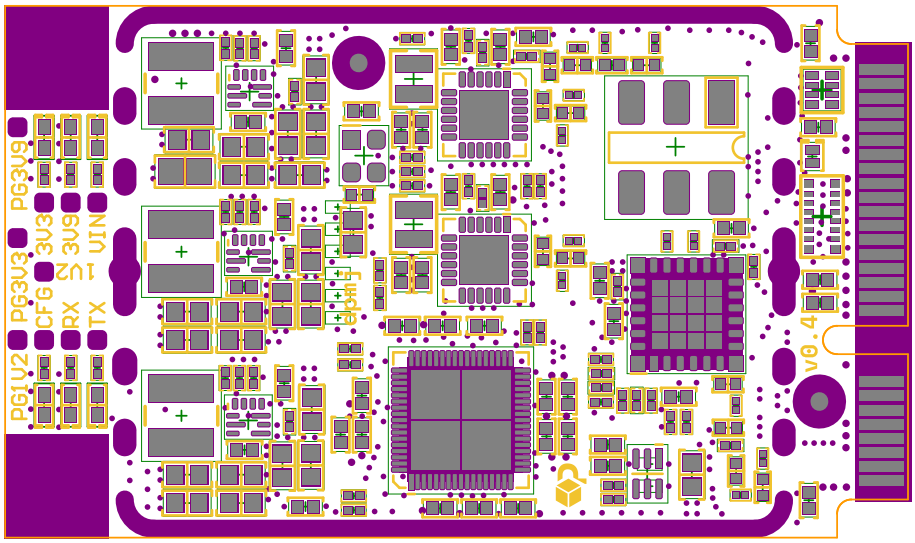
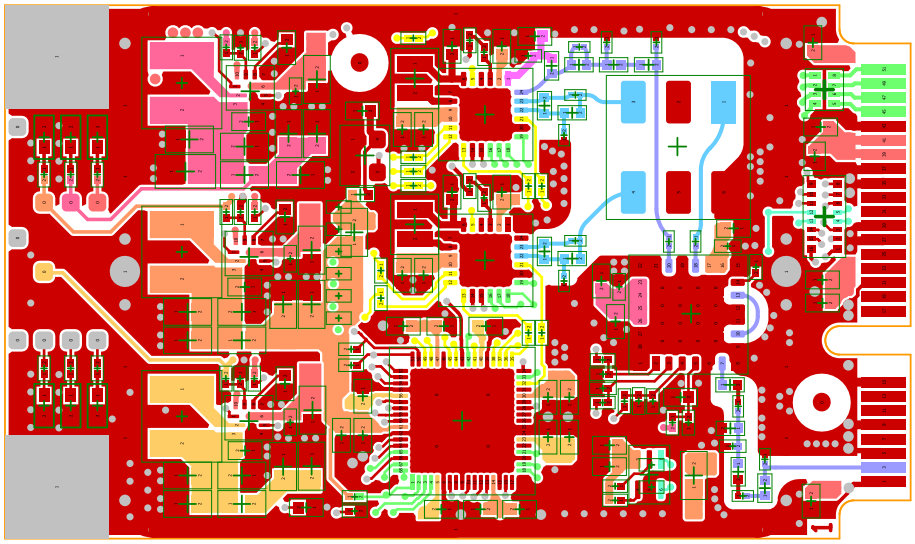


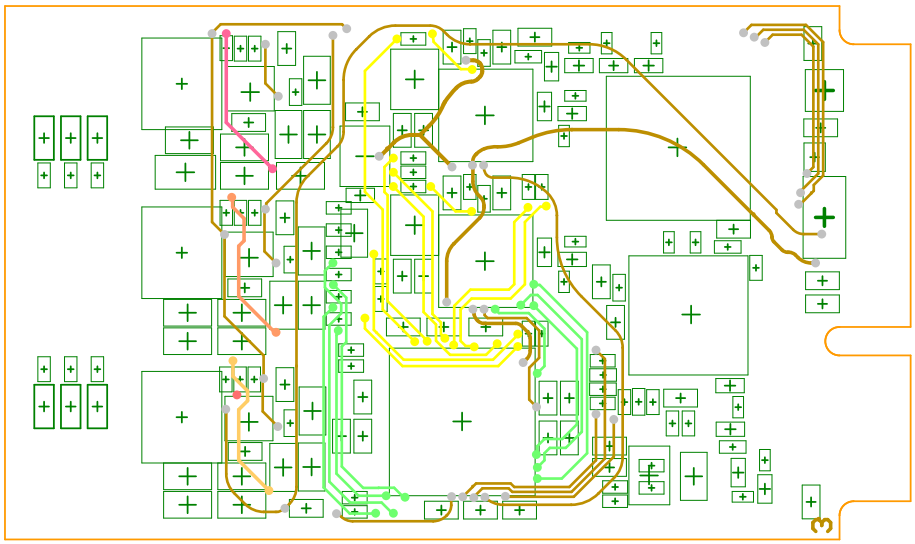
Figure 4.34 – LoRa module: PCB prints, all layers, silkscreen and drills. Not to scale. GND layers are shown with a thick line and do not appear filled when exporting PCB prints from Altium.



(a) Top silkscreen, top solder mask, top paste, board shape and guard.

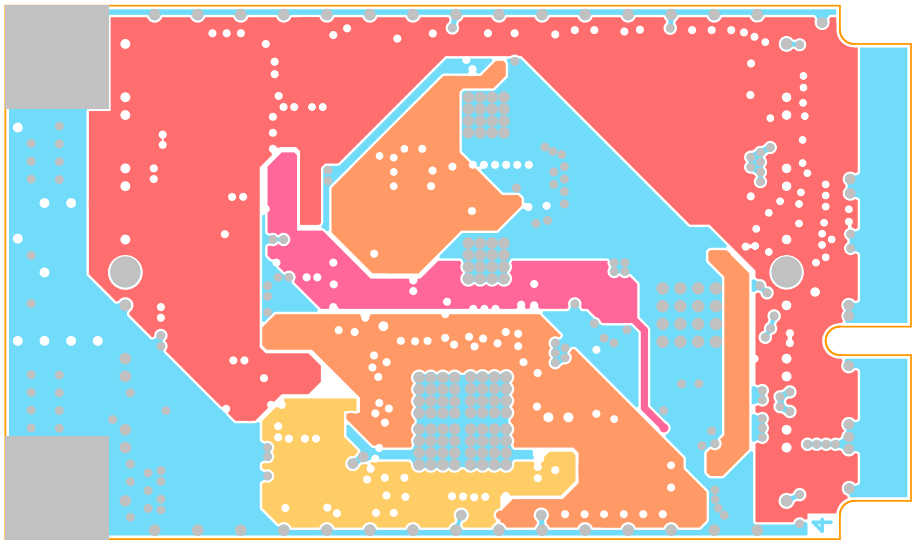


(b) Top copper layer (L1) , board shape and component guard.

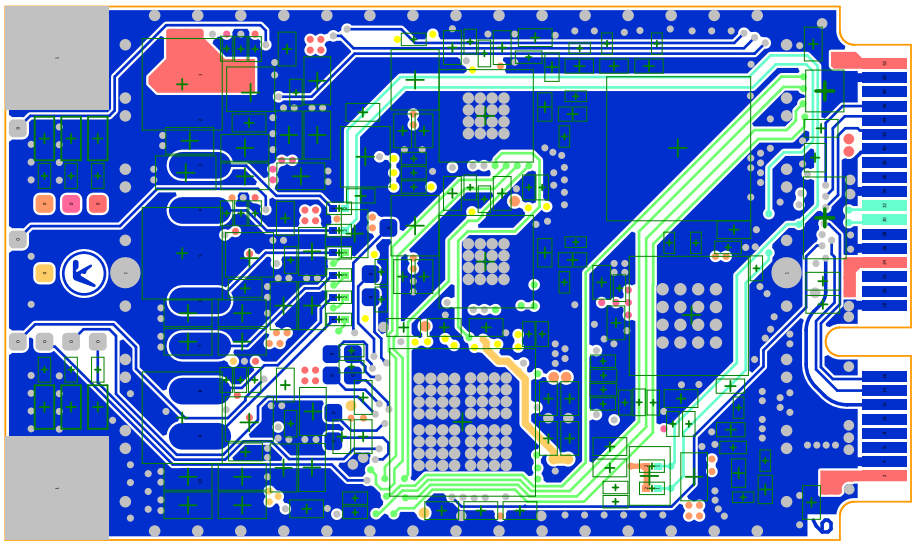


(c) Signal 1 internal layer (L3), board shape and component guard.

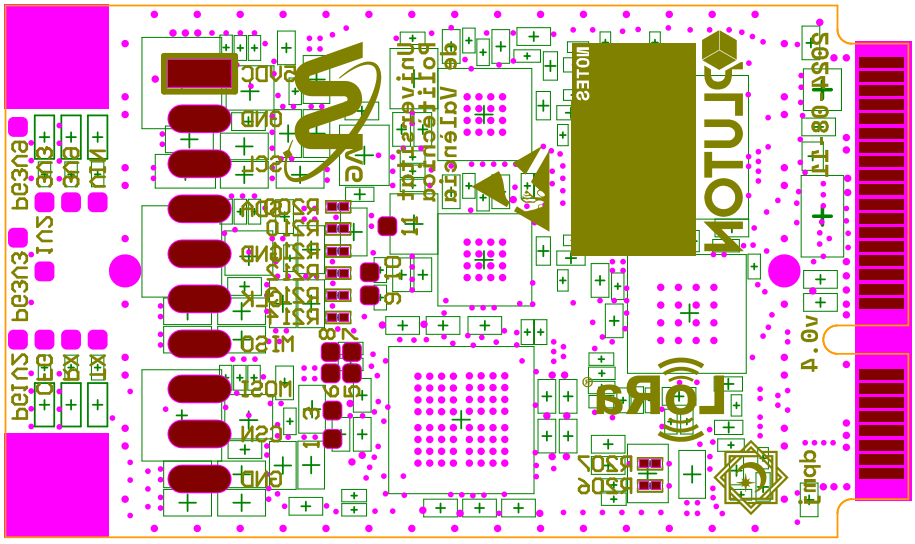
Figure 4.35 – LoRa module: PCB prints. Top copper (L1), silkscreen, solder, and signal 1 (L3).



(a) Signal 2 internal layer (L4, power routing) and board shape.

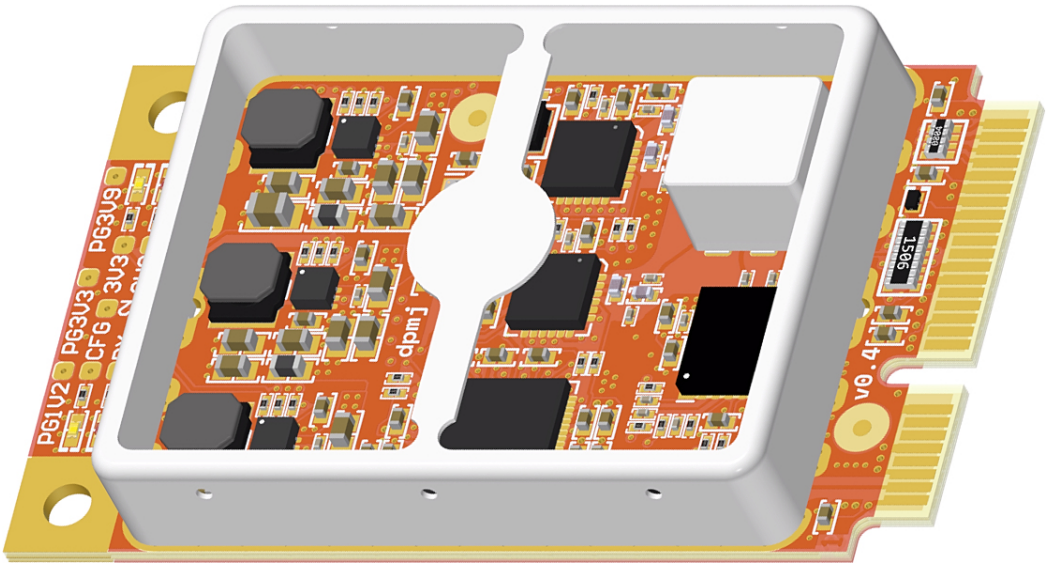


(b) **Bottom copper layer (L6)** , **board shape** and **component guard**.

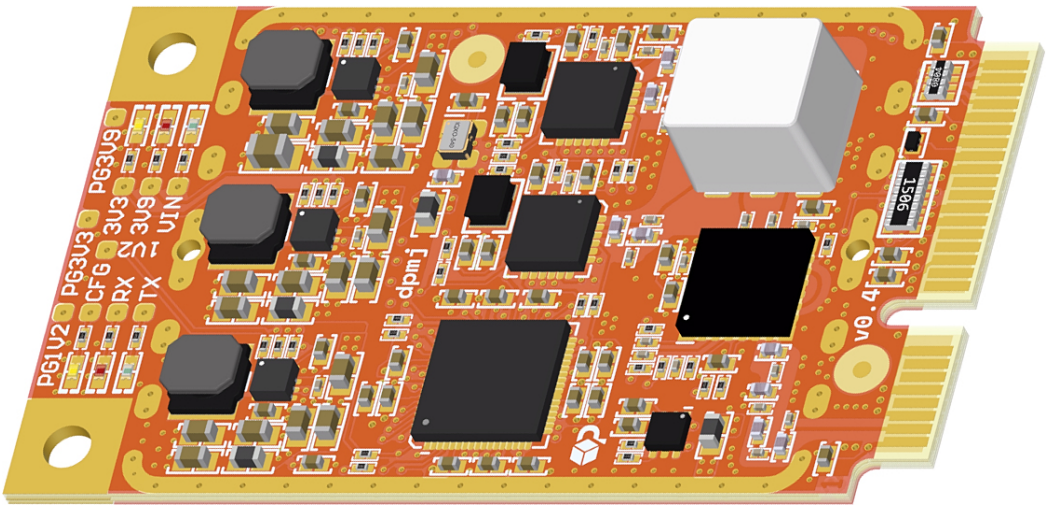


(c) **Bottom silkscreen**, **solder mask**, **paste**, **board shape** and **guard**.

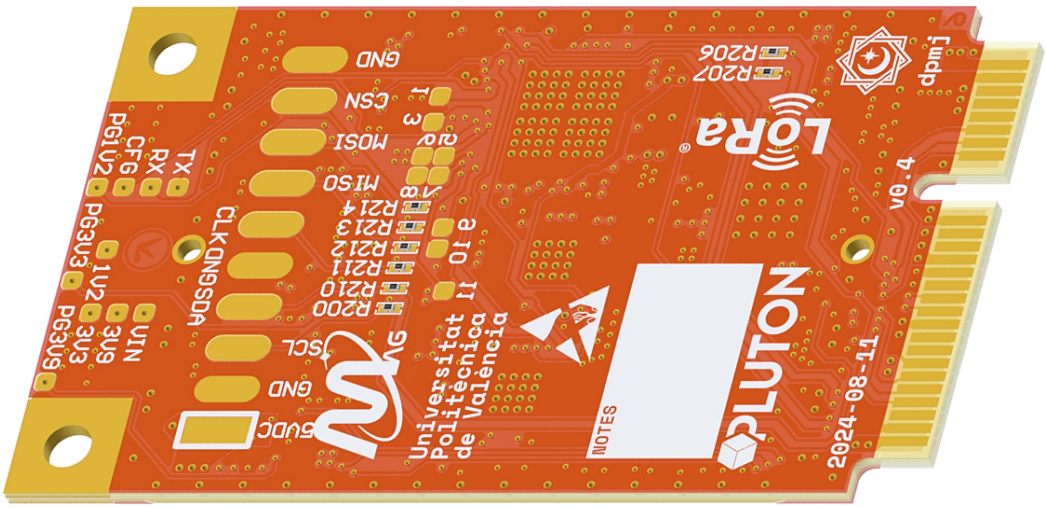
Figure 4.36 – LoRa module: PCB prints. Bottom copper (L6), silkscreen, solder, and signal 2 (L4).



(a) Top-side view, with EMI shield.



(b) Top-side view, without EMI shield.



(c) Bottom-side view.

Figure 4.37 – LoRa module: PCB renders.

4.2.5.2 CubeSat PC/104 carrier

The layout of the carrier is constrained by the CSKB PC/104 form factor, which dictates the position of the CubeSat headers and four mounting holes. To accommodate the routing of cables to the sides of the PCB, the dimensions of the board have been slightly reduced. The layout of the carrier is relatively straightforward. As with the modules, the carrier is divided into three distinct zones: RF, digital, and power. Again, most of the components are in the top layer, which makes assembly easier. There are no components underneath the mPCIe modules, except for a few small resistors.

The mPCIe connectors are situated in close proximity to the MMCX RF I/O port, with the objective of prioritizing the routing of the RF signals, minimizing losses and noise coupling. The RF signals are afforded clearance and are generously shielded.

The microcontroller is situated in a central position on the board, allowing for convenient access to all signals. The debug ports have been positioned close to the MCU, although this has resulted in a suboptimal placement due to the limited available space.

The CAN transceivers are placed in close vicinity to the CAN pins of the CubeSat headers. The reset button and boot-select switch are located in the bottom-left corner of the board. The USB port is placed on the top-left side of the board. On the bottom layer there are pads to accommodate a low-technology debug port.

The power stage is located near the headers, as recommended [3]. The layout of the DC/DC converter follows the manufacturer's recommendations [119]. This board has more space for the layout and therefore the clearance area for the inductor is respected (see Figure 4.38). Figure 4.39 shows the routing of the power multiplexers.

As with the modules, in the following pages the reader can find prints of the the most relevant PCB layers (Figure 4.40, 4.41 and 4.42) as well as PCB renders (Figure 4.43).

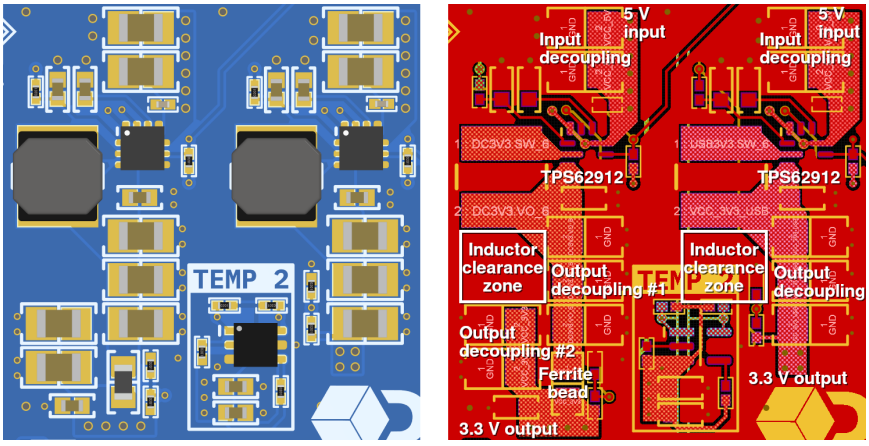


Figure 4.38 – Carrier: Layout and routing of the DC/DC converters.

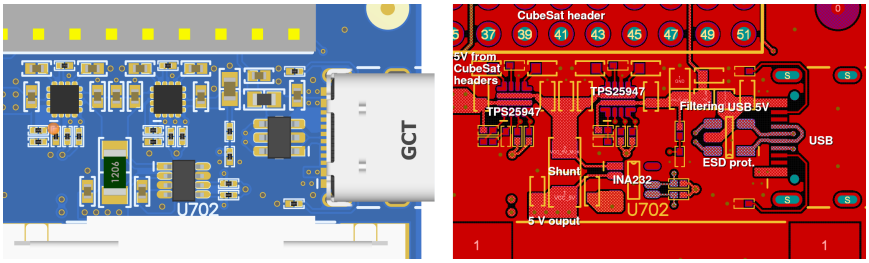
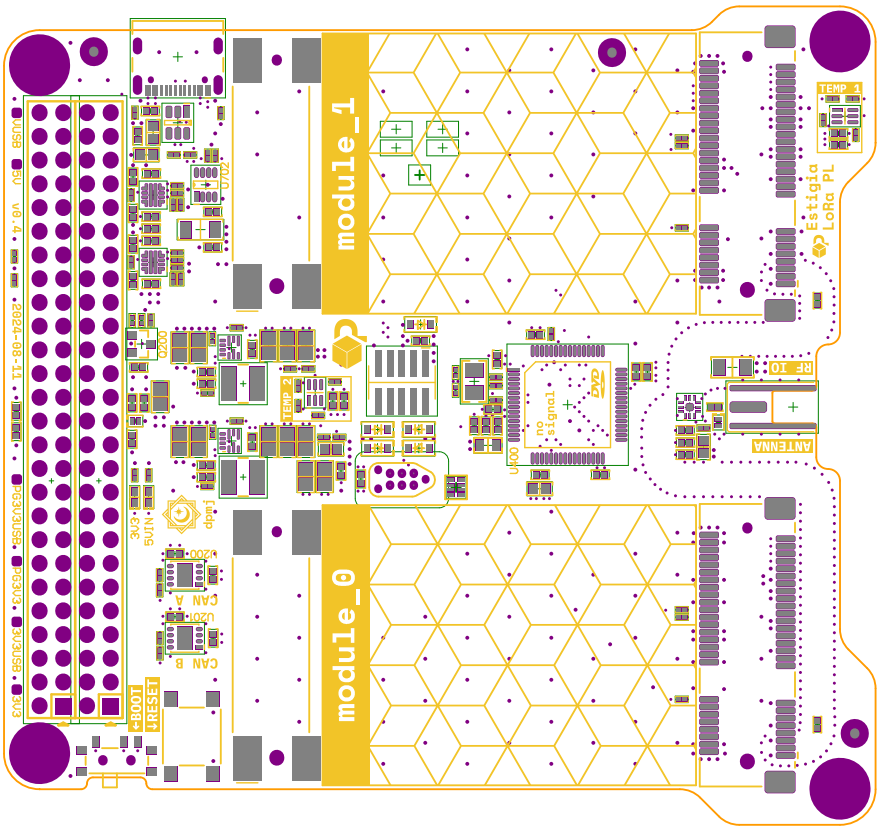
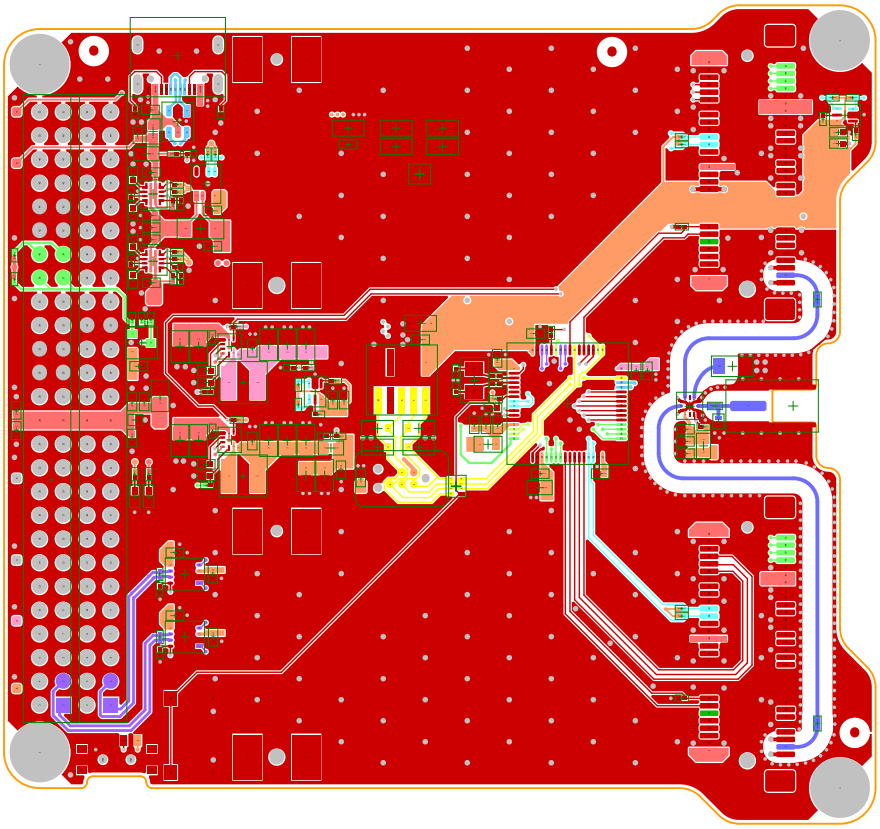


Figure 4.39 – Carrier: Layout and routing of the USB and eFuses/power multiplexers.

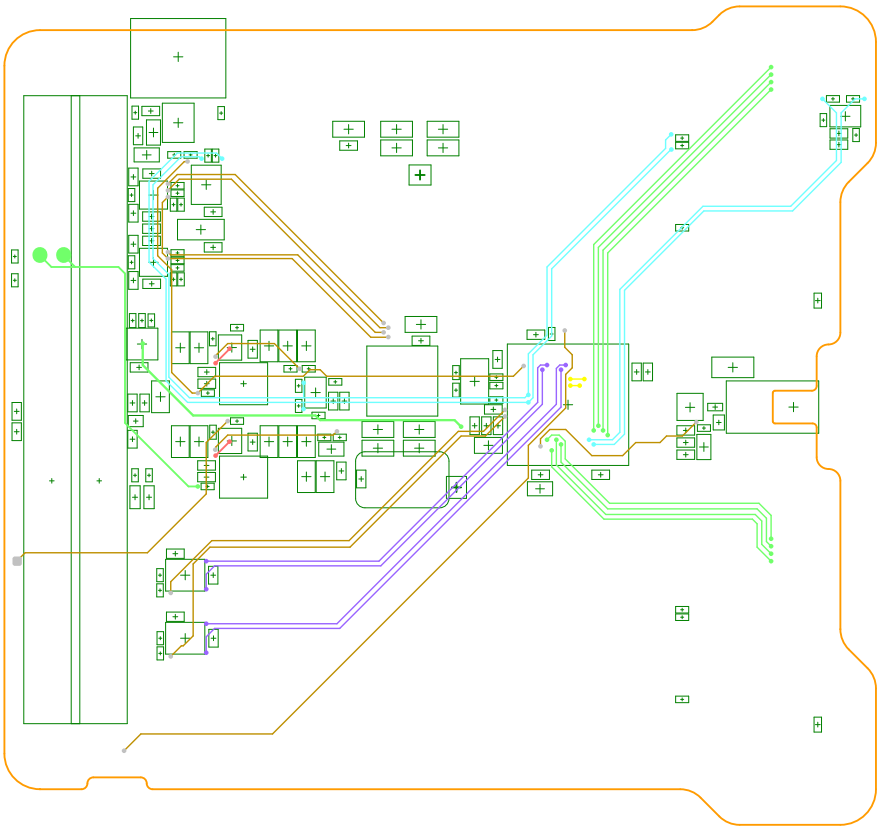


(a) Top silkscreen, top solder mask, top paste, board shape and guard.

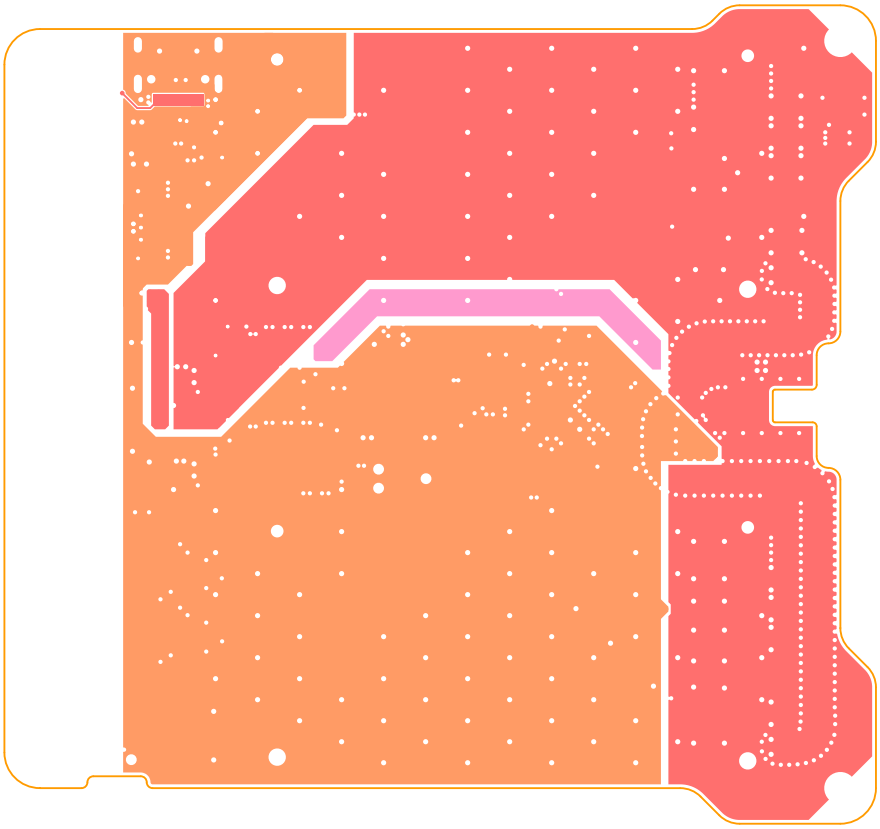


(b) Top copper layer (L1) , board shape and component guard.

Figure 4.40 – Carrier: PCB prints. Top copper (L1), silkscreen, solder and paste.

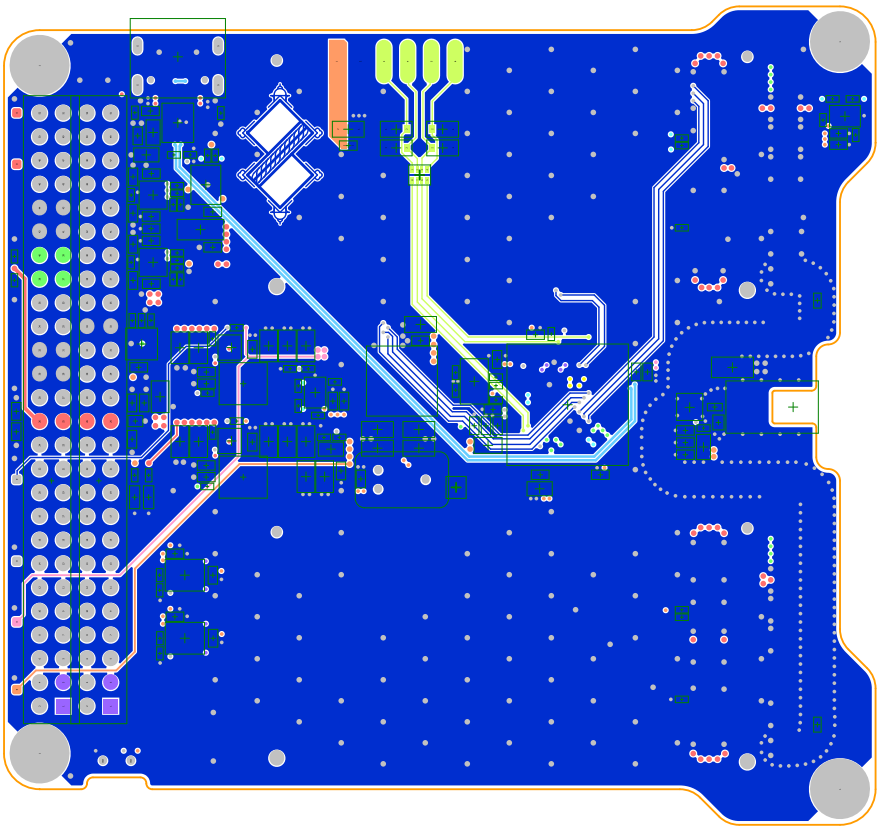


(a) Signal 1 internal layer (L3), board shape and component guard.

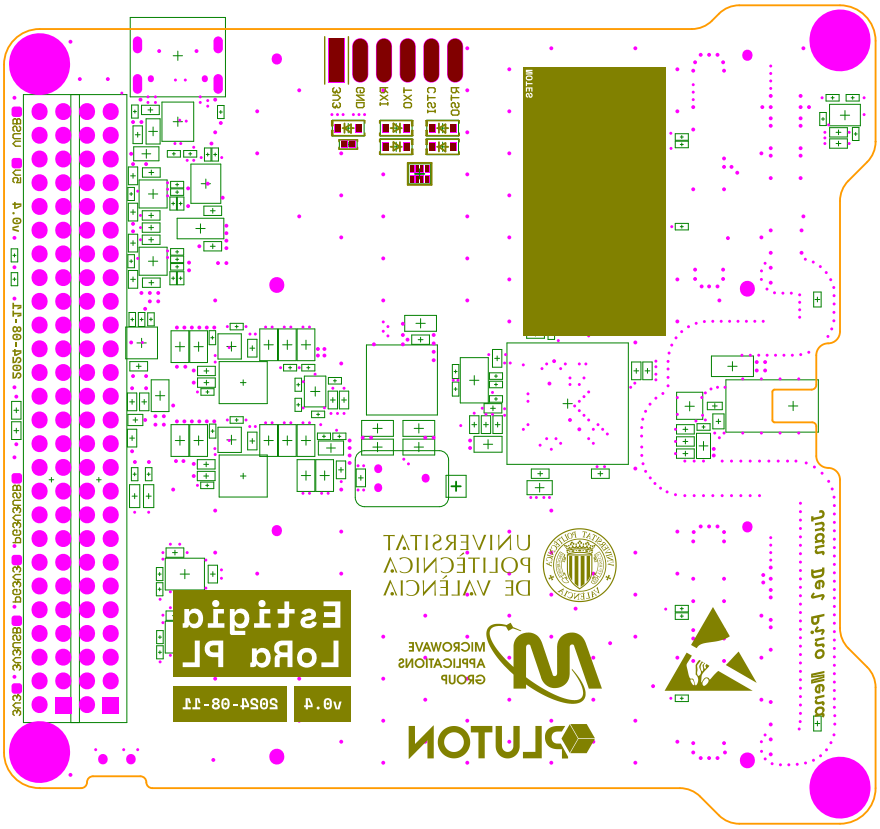


(b) Signal 2 internal layer (L4, power routing) and board shape.

Figure 4.41 – Carrier: PCB prints. Internal signal layers (L3, L4).

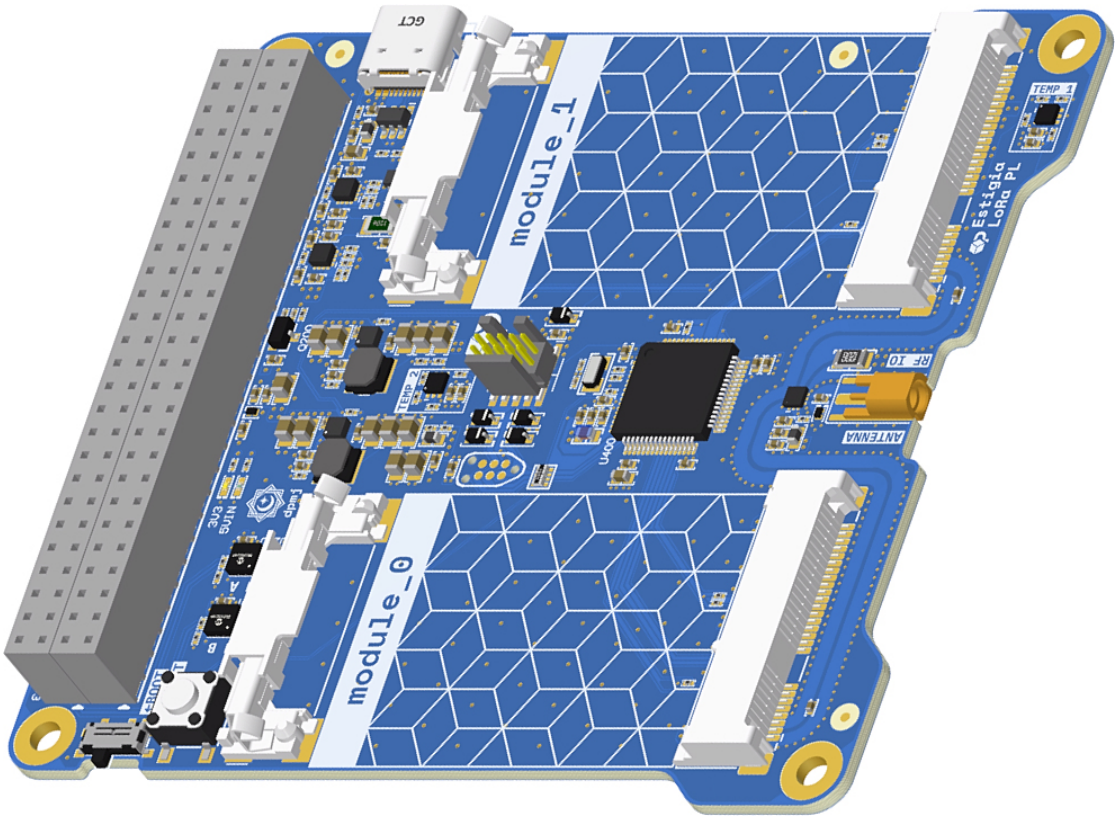


(a) Bottom copper layer (L6) , board shape and component guard.

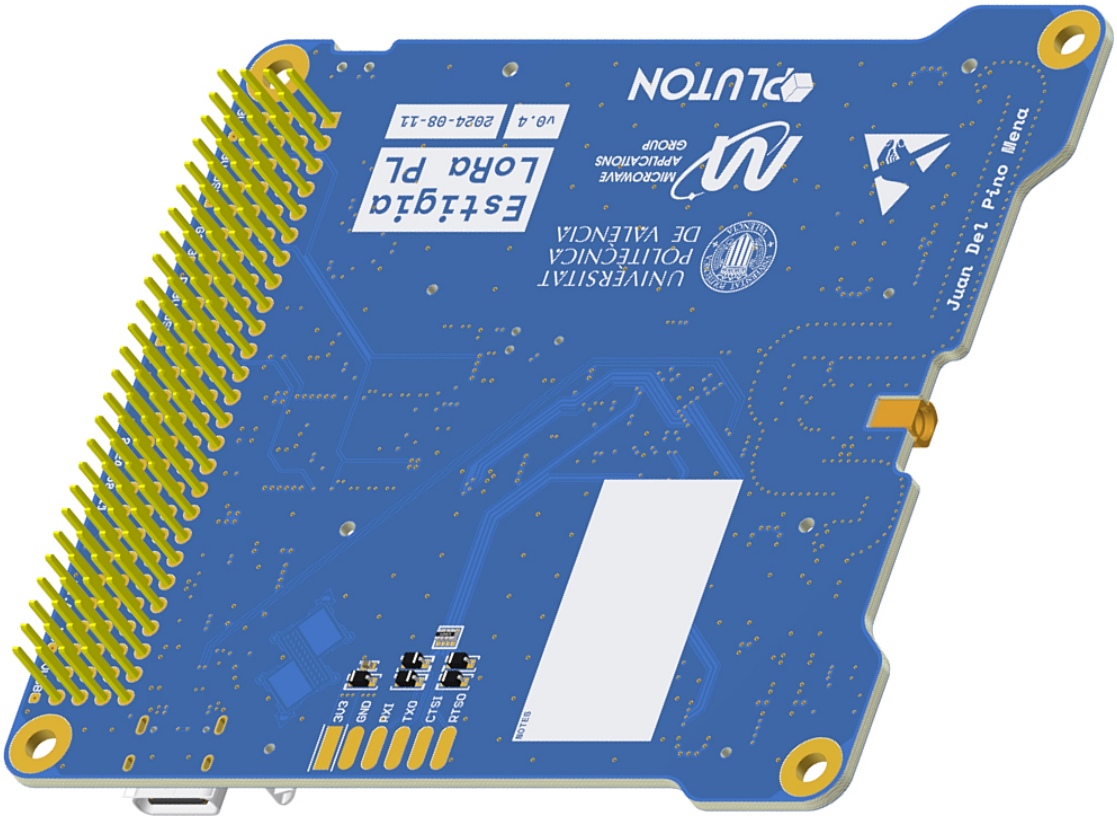


(b) Bottom silkscreen, solder mask, paste, board shape and guard.

Figure 4.42 – Carrier: PCB prints. Bottom copper (L6), silkscreen, solder and paste.



(a) Top-side view.



(b) Bottom-side view.

Figure 4.43 – Carrier: PCB renders.

4.2.5.3 Electrical Ground Support Equipment

The EGSE follows a custom form factor and layout. It features a CSKB-compatible electrical and mechanical interface, and additional mounting holes are provided in a convenient 110 × 110 mm grid to mount PCB standoffs and/or to secure the board to a surface. The location of the connectors is similar to the carrier, although an effort has been made to place them in accessible locations.

The EGSE inherits best practices, layouts and routing techniques from previous board designs. All components are on the top layer. The routing of the power and digital stages is reminiscent of that of the carrier. The position of the MCU is less centric, far away from the RF circuitry. The reset button and boot select switch are located on the same side as the majority of the interfaces. The power stage layout is analogous to that of the previous section.

The RF section may appear more intricate due to its large area and multitude of components, yet its parts are easier to navigate than the module's congested design. The RF ports are situated at a considerable distance from the digital interfaces. Special consideration has been given to the routing of digital signals in close proximity to the RF circuitry, exposing the minimum necessary area on the top layer (see Figure 4.44).

In the following pages the reader can find prints of the the most relevant PCB layers in Figure 4.45, 4.46 and 4.47. Renders of the PCB are available in Figure 4.48.

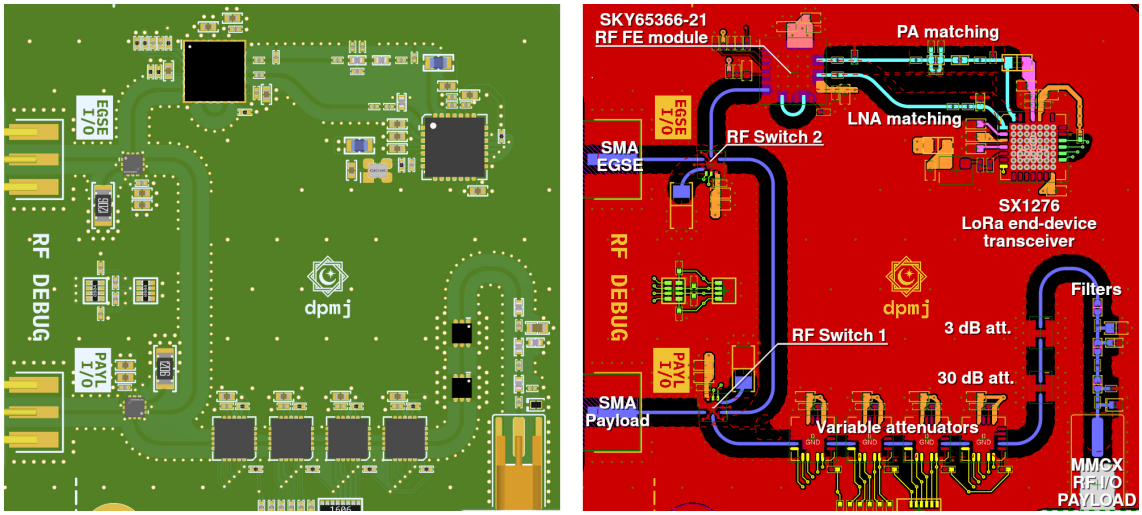
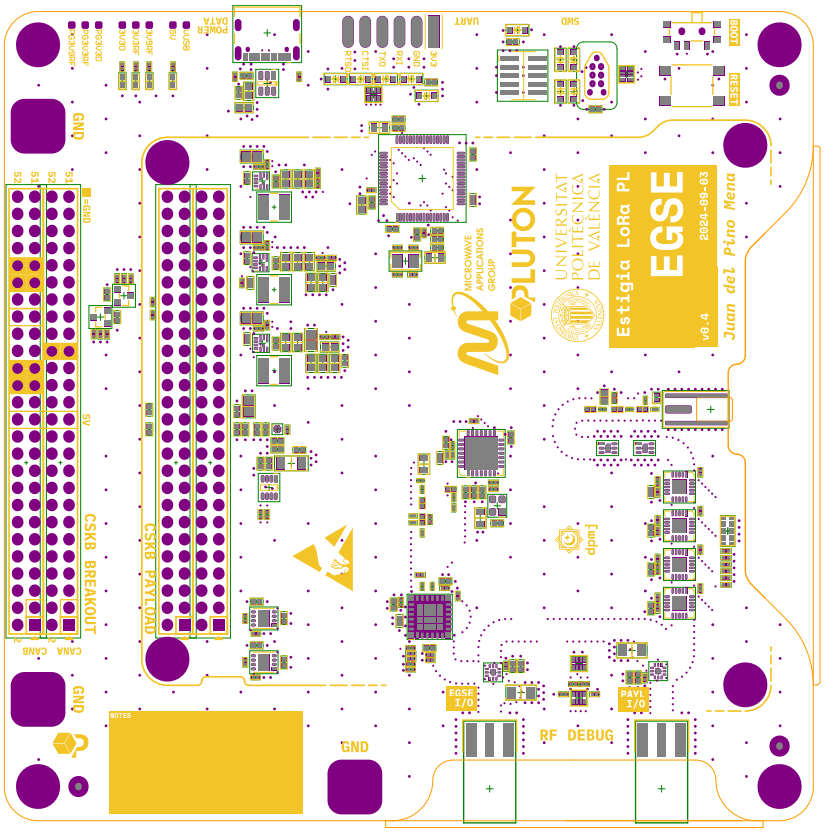
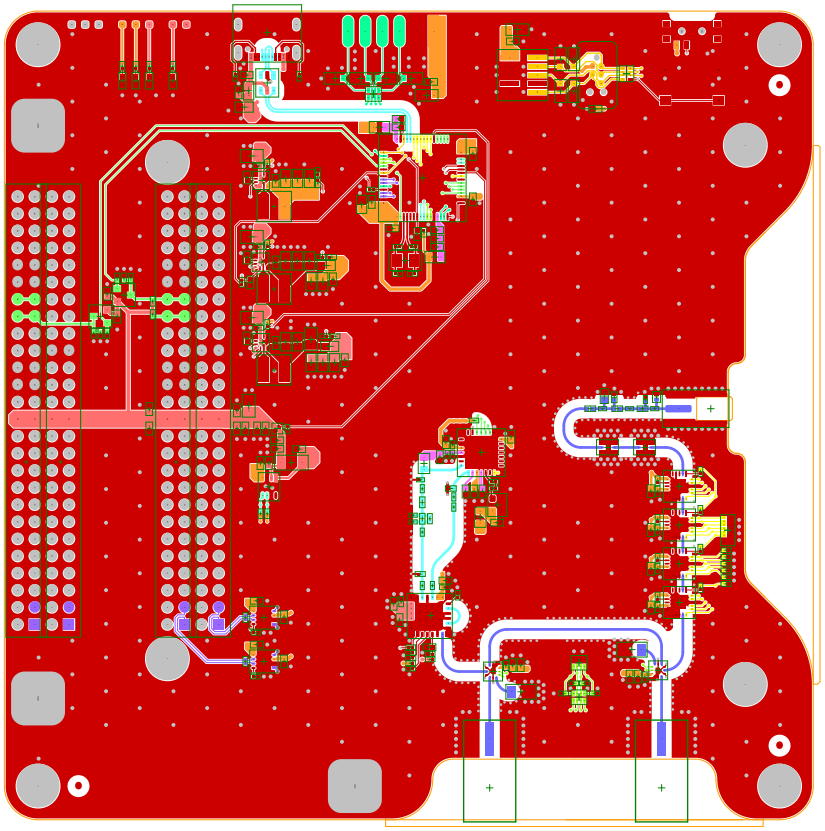


Figure 4.44 – Detail of the layout and routing of the RF stage.

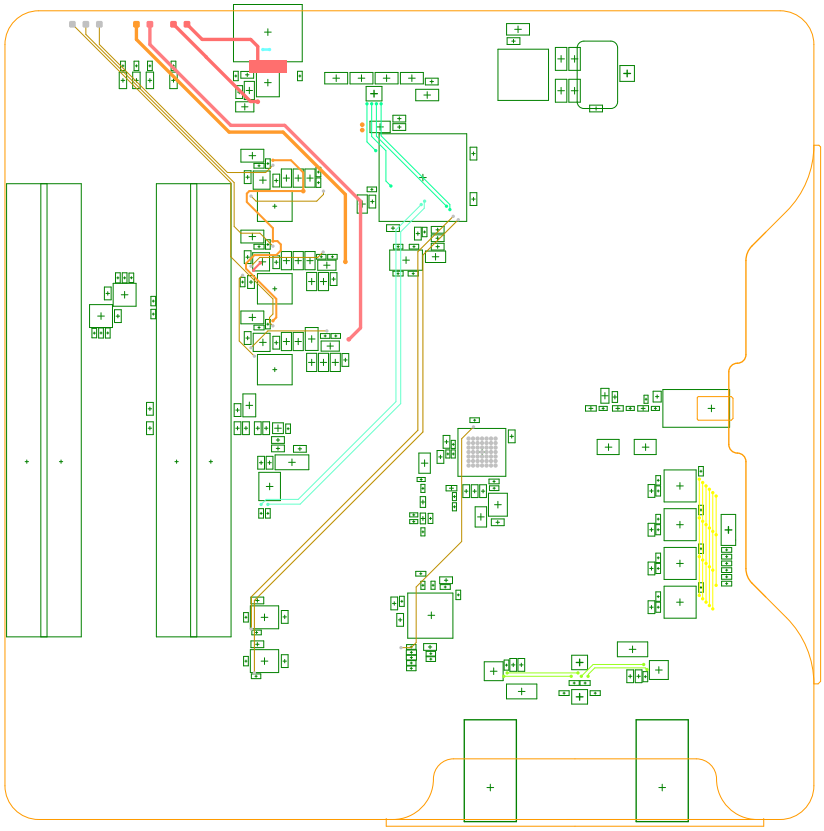


(a) Top silkscreen, top solder mask, top paste, board shape and guard.

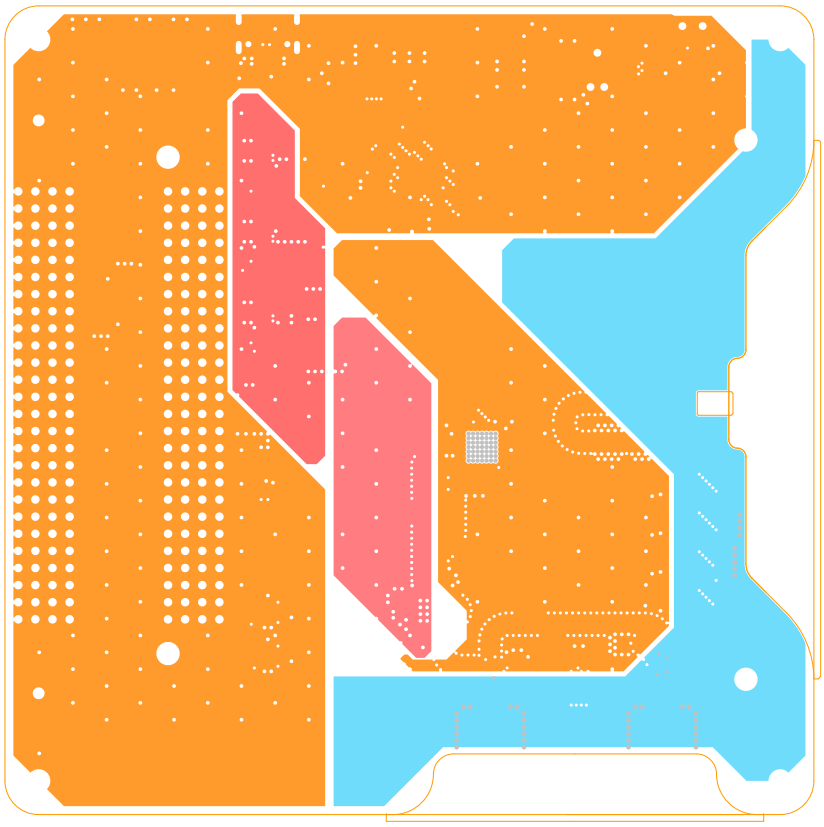


(b) Top copper layer (L1) , board shape and component guard.

Figure 4.45 – EGSE: PCB prints. Top copper (L1), silkscreen, solder and paste.

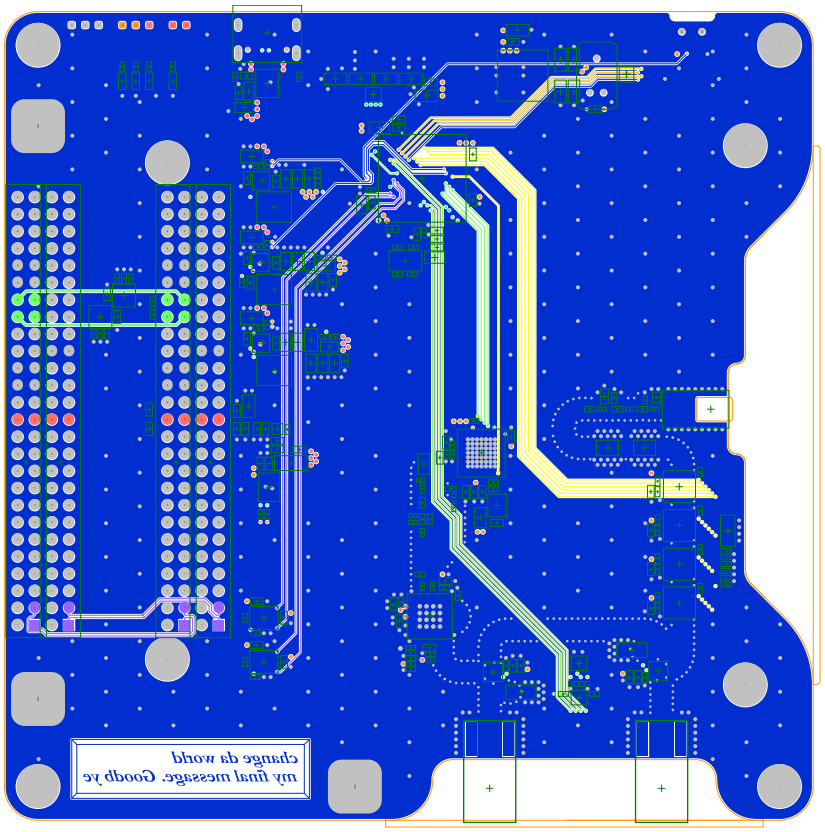


(a) Signal 1 internal layer (L3), board shape and component guard.

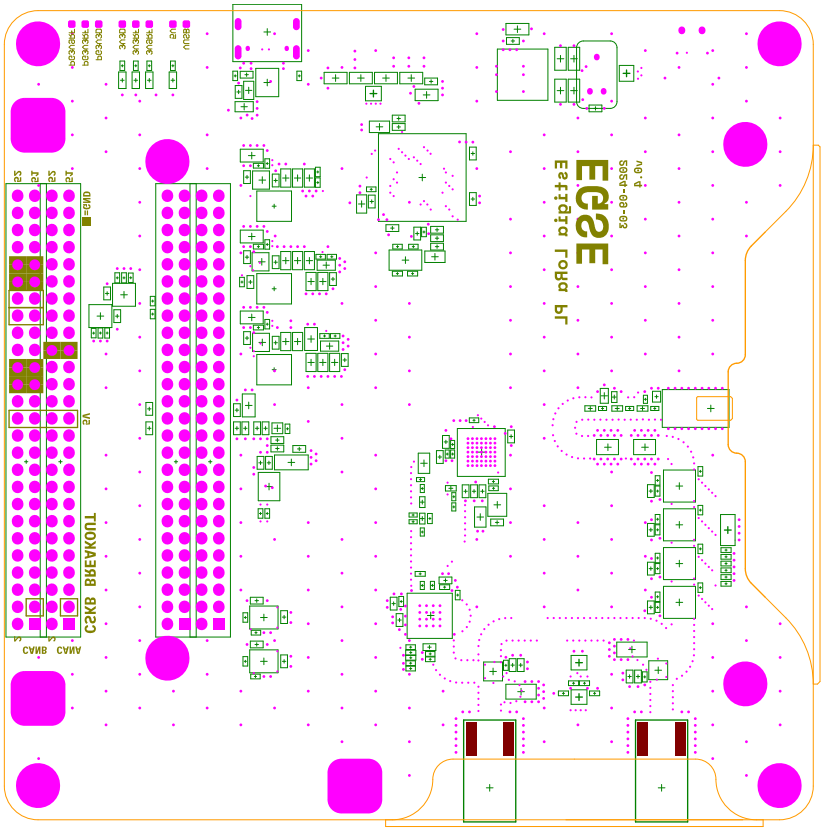


(b) Signal 2 internal layer (L4, power routing) and board shape.

Figure 4.46 – EGSE: PCB prints. Internal signal layers (L3, L4).

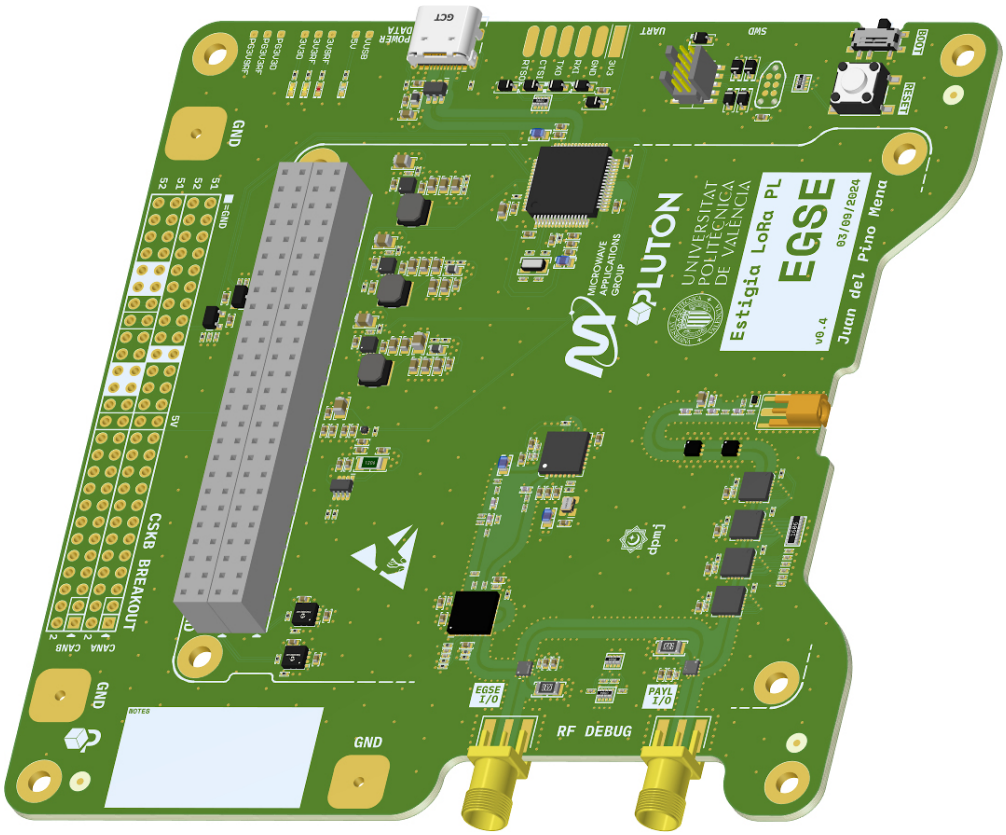


(a) Bottom copper layer (L6) , board shape and component guard.

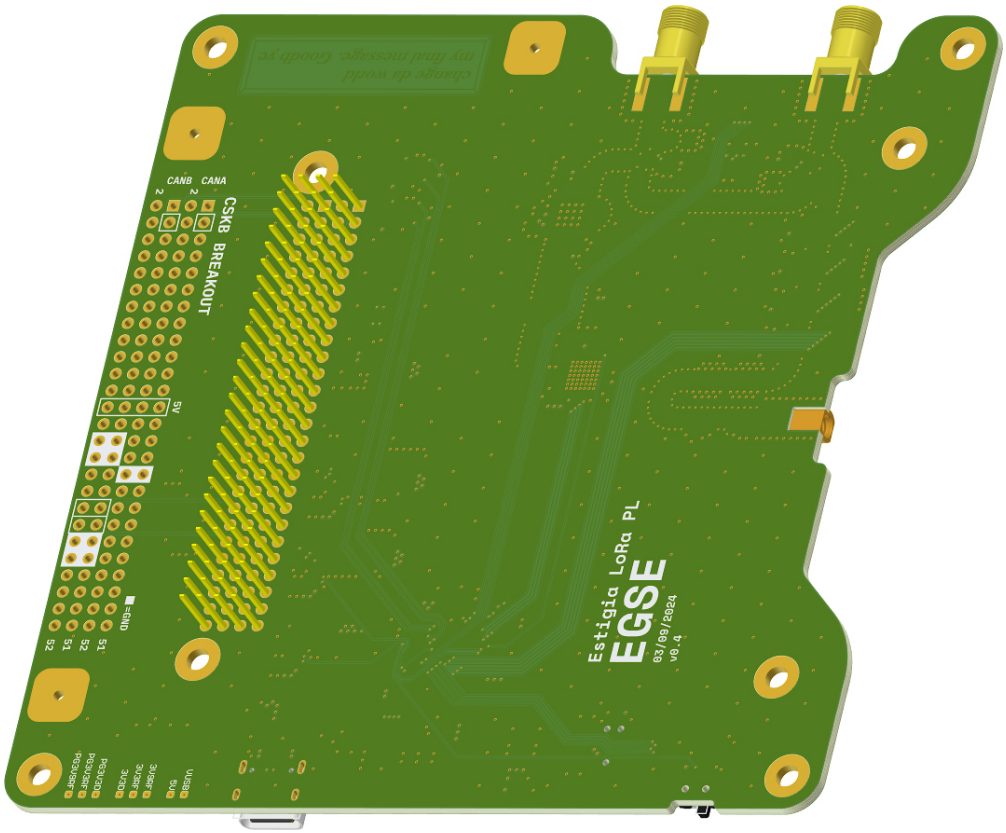


(b) Bottom silkscreen, solder mask, paste, board shape and guard.

Figure 4.47 – EGSE: PCB prints. Bottom copper (L6), silkscreen, solder and paste.



(a) Top-side view

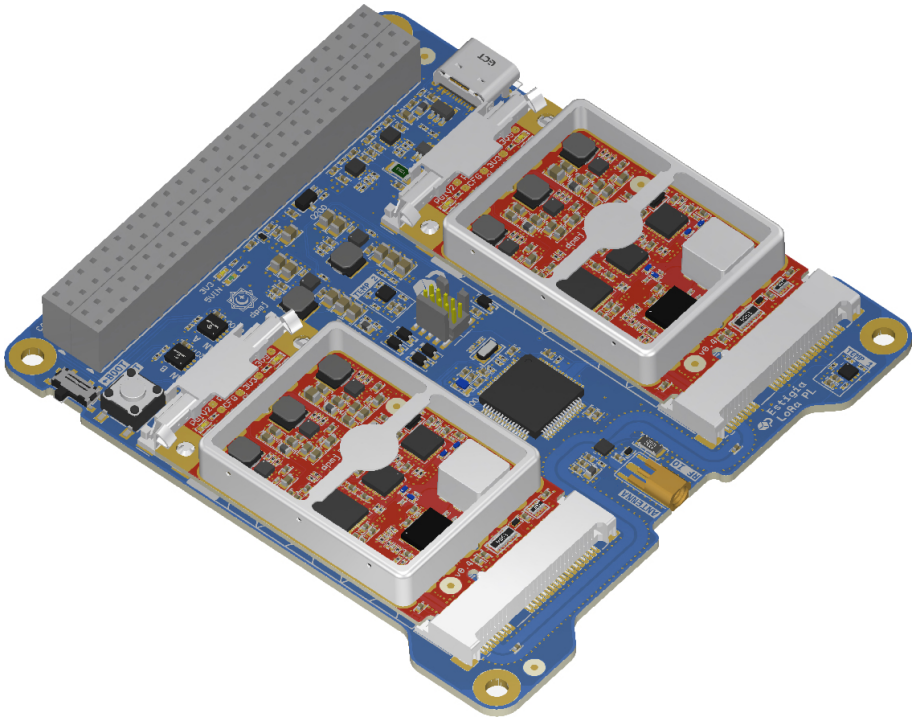


(b) Bottom-side view

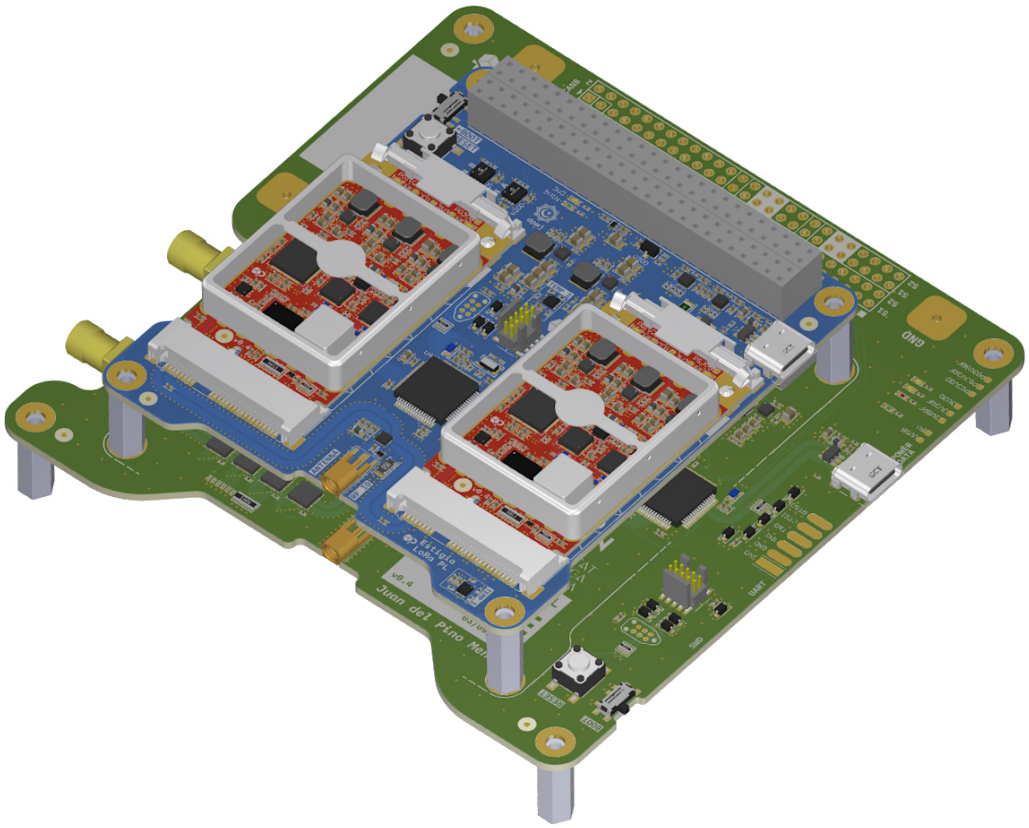
Figure 4.48 – EGSE: PCB renders.

4.2.6 Assembly

Finally, Figure 4.49 presents renders of the assembly of the payload and the EGSE.



(a) Modules and carrier.



(b) Modules, carrier and EGSE.

Figure 4.49 – Assembly: multi-board renders.

Chapter 5

Conclusions and future lines

This final chapter provides a review of the project's milestones and a personal assessment of the project's overall success. It also presents an examination of the remaining challenges, offering a self-assessment of shortcomings and areas for improvement. Finally, it reflects on the trajectory the project should take, considering the lessons learned.

5.1 Achieved milestones

This master's thesis presents a comprehensive review of the state of the art, motivation, novelty, and methodology of the project. Subsequently, an exhaustive and replicable simulation study of the Earth-satellite radio link was analyzed. This study led to the assessment of the feasibility of the communications system, and a discussion of its constraints, limitations and challenges. This process was indispensable for the establishment of the requirements. These requirements are based on the project's objectives, normative and operative constraints, and are organized in a thoughtful manner.

During this project, it became necessary to gain familiarity with the CubeSat ecosystem and development process, while being subjected to external constraints. In this process, experience was gained with standards and regulations such as ITU/RR and ECSS.

This master's thesis tackles the design of three mixed-signal, multi-layer printed circuit boards, to be assembled together. Based on existing designs and precedents, the most appropriate alternatives and circuit topologies were selected, with fabrication considerations taken into account. Designs are implemented in professional CAD and EDA software. The design process was meticulously documented.

The present report completes the first hardware design iteration of the LoRa communications payload for the *Estigia* mission, along with the development of an auxiliary board for testing the payload. This project successfully applies the knowledge acquired during the double Master's degree in Telecommunications Engineering and Electronic Systems Engineering. This first stage lays the foundation for the author's subsequent master's thesis in Telecommunications Engineering.

A detailed evaluation of the fulfillment of the requirements by the payload and EGSE can be found in Table 5.1 and Table 5.2, respectively. Out of a total of 47 payload requirements, 32 (68 %) are fully compliant, 9 (19 %) are partially compliant and 6 (13 %) are not verified. In the case of the EGSE, 16 (80 %) out of 20 are compliant, 2 (10 %) are partially compliant and 2 (13 %) are not verified. It should be noted, however, that some requirements are composites of others. Therefore, a more accurate representation would be that from a total of 33 requirements, 22 (67 %) are compliant, 2 (6 %) are partially compliant and 9 (27 %) are not verified.

The previous assessment indicates a completion rate of about two-thirds. As stated in Chapter 3: Specifications (page 35), after each iteration is completed, the requirements must be validated. It was not anticipated that all requirements would be fulfilled in this initial stage; rather, they are needed to indicate the direction of the design. Additionally, their evaluation provides a record of the development status.

With all of the above in mind, it can be confidently said that all of the main objectives set out in this master's thesis have been met.

Req. ID	Req. description (shortened)	Compliance	Justification
P-1	To develop an engineering model of the LoRa Comms payload	**Partially**	Not yet manufactured
P-1.1	To integrate COTS and use standard procedures for the manufacturing	**Partially**	COTS are used, but the device is not yet manufactured.
P-1.2	The device, functions and the design process are documented	**Yes**	This report and its addendum
P-2	To design a LoRa gateway capable of Earth-LEO communications.	**Partially**	The design is finished, but its performance has not been verified.
P-2.1	The device shall meet the international communications normative.	**Partially**	Designed to do so, not verified.
P-2.1.1	Operates at 435 – 438 MHz	**Yes**	By design.
P-2.1.2	PFD ≤ -187 dB/(m^2·Hz).	**Partially**	In theory, but not verified
P-2.2	The device meets link quality.	–	Not verified
P-2.2.1	Noise figure of 3 dB or less.	–	Not verified
P-2.2.2	Insertion losses of 3 dB or less.	–	Not verified
P-2.2.3	Output power of 30 dBm or more.	–	Not verified
P-2.2.4	The sensitivity shall reach -137 dBm	–	Not verified
P-2.2.5	Maintain RF properties in band	–	Not verified
P-2.3	Parameters reconfiguration	**Yes**	Transceivers are configurable.
P-3	Mechanically compliant device	**Yes**	See below
P-3.1	Payload modular hardware design	**Yes**	By design
P-3.1.1	The carrier is CSKB-compatible.	**Yes**	By design
P-3.1.2	The modules are mPCIe.	**Yes**	By design
P-3.2	PCB substrate $T_g \geq 453$ K (180 °C)	**Yes**	Selected substrate is compliant.
P-3.3	All screws are metric [...]	**Yes**	By design
P-4	PCBs implement the required functions and are space-suitable.	**Yes**	The payload design is complete.
P-4.1	PCB ports are standard.	**Yes**	See below
P-4.1.1	CubeSat bus: SSQ-126-04 [...]	**Yes**	By design
P-4.1.2	Module-carrier: mPCIe [...]	**Yes**	By design
P-4.1.3	RF I/O: MMCX socket.	**Yes**	By design
P-4.1.4	SWD: FTSH-105-compatible.	**Yes**	Plus an optional TC2030.
P-4.1.5	Test points shall be provided.	**Yes**	By design
P-4.1.6	One or more serial interfaces will be made accessible via ports.	**Yes**	Modules: SPI and I2C port. Carrier: USB and UART ports.
P-4.2	The MCU should be an STM32 [...]	**Yes**	Selected: STM32L496RGT6
P-4.2.1	The required peripherals in the microcontroller [...]	**Yes**	All required peripherals are available and allocated.
P-4.2.2	The MCU shall have access to signals to monitor the electronics.	**Yes**	Signals connected to GPIOs
P-4.3	The device has a power system.	**Yes**	Power conversion & distribution.
P-4.3.1	The power consumption in operation shall not exceed 5 W.	**Partially**	Compliant according to calculations, but not verified
P-4.3.2	The device shall be equipped with a sleep and a shutdown mode.	**Partially**	Hardware is ready, but not firmware.
P-4.3.3	The carrier is fed using a 5 V rail from the USB or the CubeSat bus.	**Partially**	Designed to do so, not verified.
P-4.3.4	The power conversion should use DC/DC converters, filtering noise.	**Yes**	Use of Low-Noise DC/DC converters with filtering.
P-4.4	The device shall implement onboard protection systems.	**Yes**	By design
P-4.4.1	Sensitive electronics are shielded.	**Yes**	A shield covers the LoRa gateway

Continued on next page

Table 5.1 – Assessing the achievement of the payload requirements.

Continued from previous page

Req ID	Req. description (shortened)	Compliance	Justification
P-4.4.2	ESD protections shall be implemented in the external ports.	**Yes**	External ports have TVS diodes, capacitors and resistors
P-4.4.3	The device shall implement OC and OV protections.	**Yes**	OV: protection ICs and diodes. OC: current sense and eFuse.
P-4.4.4	Each PCB shall contain at least one temperature sensor.	**Yes**	One in each module, two in the carrier.
P-4.4	Mounting holes connected to GND in modules, isolated in carrier	**Yes**	By design
P-4.5	Two modules will be mounted in the same motherboard.	**Yes**	Two modules are mounted. Arbitration measures are placed.
P-4.6	Components are low-tolerance and resilient to 100 °C or more.	**Partially**	Not all COTS components are rated for 100 °C or more
P-4.7	RoHS compliance.	**Yes**	In components and fabrication.
P-4.8	Manufactured electronics shall not emit abrasive, toxic or harmful [...]	**Yes**	No dangerous or emissive substances are employed.
P-4.9	All perforations are through-hole.	**Yes**	By design

Table 5.1 – Assessing the achievement of the payload requirements.

Req. ID	Req. description (shortened)	Compliance	Justification
E-1	To design the EGSE	**Yes**	EGSE design is complete.
E-1.1	The EGSE meets P-1.1 and P-1.2.	**Partially**	P-1.1: not manufactured. P-1.2: documented in this report
E-1.2	Meets P-2.1.1, P-2.2, P-2.2.1, P-2.2.2, P-2.2.3, P-2.2.4, P-2.2.5 & P-2.2.6.	–	Not verified
E-1.3	The EGSE shares the payload's CubeSat bus pinout.	**Yes**	By design
E-1.4	The EGSE provides mechanical support for the payload.	**Yes**	By design
E-1.5	PCB substrate will be standard FR-4	**Yes**	By design
E-1.5.1	PCB substrate $T_g \geq 423\,\text{K}$ (150 °C)	**Yes**	Selected substrate is compliant.
E-1.6	The EGSE meets P-4.1.1, P-4.1.3, P-4.1.4, P-4.1.5 & P-4.1.6	**Yes**	Connectors follow requirements.
E-1.7	The MCU should be the same model as the Payload's (Req. P-5.2)	**Yes**	By design
E-1.7.1	Required MCU peripherals [...]	**Yes**	All required peripherals are available and allocated.
E-1.8	The EGSE shall implement the hardware of a LoRa end-device.	**Yes**	Includes a SX1276 end-device
E-1.8.1	The EGSE shall incorporate variable attenuators to simulate FSPL	**Yes**	Implemented by fixed and variable attenuators
E-1.9	The device has a power system.	**Yes**	By design
E-1.9.1	The EGSE is fed from 5 V [...]	**Yes**	By design
E-1.9.2	PL current sense and power control.	**Yes**	By design
E-1.9.3	Power conv. using DC/DCs.	**Yes**	By design
E-1.9.4	Consumption 5 W or less.	–	Not verified
E-1.10	The EGSE meets P-4.4.2 and P-4.4.3	**Yes**	By design
E-1.11	Mounting holes will be isolated.	**Yes**	By design
E-1.12	The EGSE meets P-4.7 and P-4.8	**Yes**	Design meets RoHS.

Table 5.2 – Assessing the achievement of the EGSE requirements.

5.2 Personal assessment

This master's thesis, which spanned almost a full year, required considerable effort on my part but proved to be very rewarding. My experience throughout this project has been positive in terms of academic, professional, and personal growth. I am pleased to have integrated a significant amount of effort and multidisciplinary methodologies into a project that merges electronics and telecommunications.

This master's thesis is of a considerable scope. One could argue that it represents a workload more typical of a development team, rather than a single student. Initially, I felt overwhelmed by the project, but with patience and perseverance I was able to overcome the challenges. I am particularly proud of my achievements in the hardware design, given that until a year ago I had only designed simple, two-layer circuit boards.

Still, there are certain areas that I would have liked to have explored in more depth. In particular, I would have liked to have conducted a more rigorous analysis of the RF electronics and assembled a first prototype before submitting the first master's thesis. However, due to delays –largely the result of my own miscalculations– these goals could not be met. I hope that the lessons learned will lead to more accurate planning for the second master's thesis. That being said, I am encouraged by the foundation and technical confidence the project has provided me.

I consider the results of this initial design phase to be more than satisfactory, given that I started from scratch. From a professional standpoint, I feel that I have matured considerably by being actively involved in both a CubeSat student team and an R&D institute. At the beginning of my research, I was less familiar with technical concepts such as space technology, PCB design, and LoRa than I am now. But I also developed soft skills such as teamwork, comradeship, and team management. I am grateful for the opportunity to work with Pluton UPV and its sponsors.

I would like to thank the CubeSat and LoRa hardware communities. Their dedication, reverse engineering and open-source initiatives are invaluable in ecosystems where documentation is scarce, vendor-locked, and non-standardized.

As a by-product of this master's thesis, I have made available the LaTeX template which gives format to this report under an open-source license.

Last but not least, I sincerely hope that Pluton UPV's *Estigia* will be successful and that my work has contributed to it.

5.3 Lessons learned and future lines

Once recognized the merits and the achievements of this master's thesis, this section contains suggestions for improvement based on self-criticism and the experience gained during the development of the project. This allows new perspectives to be established, to advance the project in the right direction and avoid repeating mistakes.

5.3.1 Discussion on design flaws and improvements

In this section, the most questionable design decisions and known flaws are discussed.

- Before manufacturing, **more detailed RF and electromagnetic simulations should be performed.** In addition, insertion loss and reflections in the mPCIe should be simulated. This has been overlooked until now due to the significant wavelength at 435 MHz (see section 3.5: Connector pinouts, page 51).

In order to optimize the matching networks and baluns, first **it is necessary to accurately characterize the LoRa transceivers** with a spectrum analyzer and a vector network analyzer (VNA), measuring the optimum load impedance of the transmitter and the input reflection coefficient of the input [125], [126].

- Electrical performance is not the sole factor to be considered: **a thermal analysis is also necessary to evaluate the feasibility of the thermal design of the boards.** Indeed, this is a crucial analysis that should have been conducted in parallel with the layout. In the case of the carrier, it is not anticipated to be a problem, since its integrated circuits do not consume much power, and the board has a considerable thermal inertia. However, one module can consume up to 4.4 W, which can lead to significant thermal challenges. These challenges become evident when one considers that the modules should operate in vacuum and have an EMI shield, which eliminates convection and restricts infrared emissions, respectively [151].
- In the same line, it is a possibility that the mPCIe form factor is simply insufficient in terms of size for the electronics, which are **space-constrained**, which also contributes to the thermal problem discussed above. In order to reclaim area in the modules, it may be possible to reduce the space allocated for the power system. One approach would be to utilize a Power Management Integrated Circuit (PMIC) *in lieu* of three discrete DC/DC converters of the current design. Optionally, the 3.3 V regulator could be eliminated if the modules were to utilize the 3.3 V rail from the carrier instead of the 5 V rail.
- During the development of this master's thesis, it became increasingly clear that **the scope was too ambitious** for the time, resources, manpower and experience at my disposal. The expectations were too optimistic.

  In the near future, rather than producing the three PCBs at once, it would be wise to **adopt a modest, safe and methodical approach**. The strategy is to develop, manufacture, test, and verify different stages of the project gradually and individually in small evaluation boards before integrating them into fully-fledged PCBs.

  This strategy promotes a robust development process. It allows for the division of labor, facilitates comparing design alternatives, enables the identification of problems at each stage, and ensures that all parts function properly prior to integration. All while leveraging on the existing designs, documentation, experience, and other outcomes of this master's thesis.
- According to this logic, the first complete board to be manufactured should be the LoRa gateway modules, along with **a new auxiliary breakout board to test the modules**. This auxiliary PCB takes advantage of the modular design to provide an interface for the LoRa gateway modules to breadboards or development kits, making testing and debugging easier. See Figure 5.1 for a mockup of the breakout board with an example STM32 Nucleo F411RE development kit attached to it.

  The breakout board would allow the LoRa gateway modules to be tested in a simple and reliable hardware platform, removing from the equation the possible hardware and firmware issues related to the carrier and EGSE. This platform would also provide a smoother entry into firmware development, as there is almost no documentation on how to configure the chips of a LoRa gateway. This setup could also provide valuable insight into resolving hardware bugs before the carrier and EGSE are even manufactured.

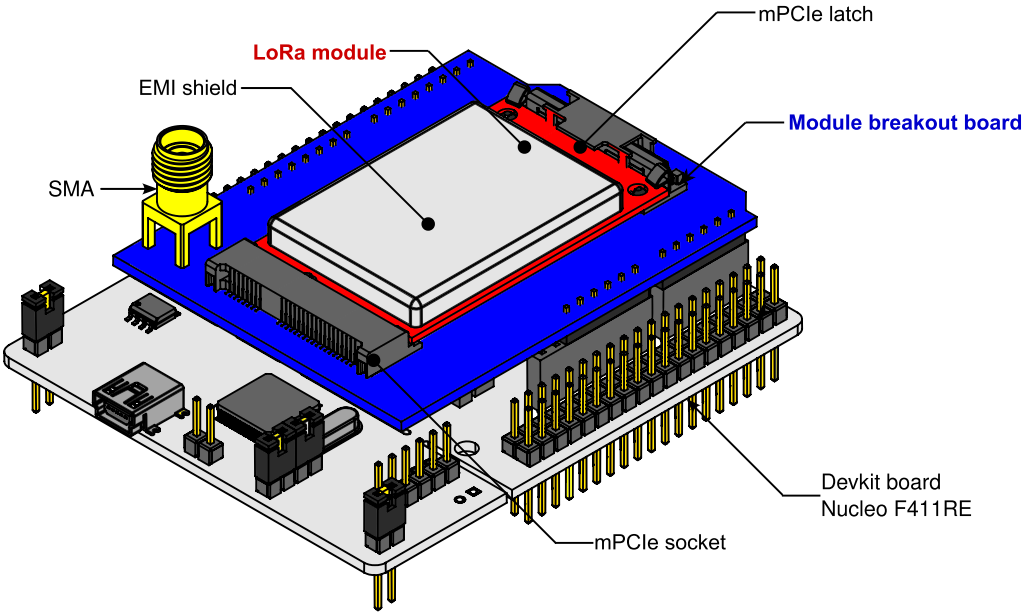


Figure 5.1 – Mockup of the LoRa module breakout board with a sample Nucleo devkit attached.

5.3.2 Discussion on future lines

This thesis is a first approximation for an *engineering model* (EM), a proof of concept to gain experience, to be testable and easy to debug. The ultimate goal of the project is to develop a *flight model* (FM) that will carry all the development efforts and lessons learned into a fully functional and space-qualified CubeSat communications board and its associated EGSE. This section discusses the next steps to be taken. An early Gantt chart of the second phase of the project was shown in Figure 1.9 (section 1.5, page 10).

- The first step is **to review and fix the known flaws** discussed in the previous section. Then, the designs are then sent to manufacturing. Once the boards arrive, they are soldered and assembled.
- While waiting for the manufacturing and shipping, the **firmware development should start**. It is also necessary to study and define the communications protocol encapsulated inside the LoRa frame, as well as the medium access control (MAC).
- Then, **each board will be tested, verified and validated in a controlled laboratory environment**. This step is particularly important and is expected to take a considerable amount of time, as it involves verifying all evaluation boards independently, comparing design alternatives, and issues are sure to arise.
- **New prototypes will be developed** in the medium to long term. A hardware revision will address bugs found during testing. This revision should also evaluate deeper design changes, such as integrating all of the payload's electronics on a single PCB for improved RF performance, reduction of mechanical and electrical failure points, and cost savings (see Appendix B: Project costs, page 115).
- In the long term, it would be beneficial to **test the boards in test chambers**, such as anechoic chambers for electromagnetic compatibility (EMC); vacuum and temperature chambers to simulate the space environment; and vibration and shock analysis to test the ability to withstand a rocket launch. These tests can provide valuable information about significant oversights and design flaws. However, this depends on the scarce availability of test chambers.

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Appendix A

Sustainable Development Goals

The Sustainable Development Goals (SDG) are a set of seventeen goals aimed at fostering peace and prosperity for people and the planet [157], [158]. The following list justifies the alignment of this work with the corresponding SDG. Table A.1 summarizes the affinity with each SDG.

4. Quality education. Academic institutions often struggle to provide students with practical training. Pluton UPV aims to help university students by building a spacecraft with the help of professors and researchers. This master's thesis will serve as documentation, know-how and training for the next members of Pluton UPV. This project also contributes to SDG 4 through the deposit of this thesis in the institutional library of the UPV as open access. Furthermore, one of the main goals of *Estigia* –for which the subsystem developed in this thesis is crucial– is to provide secondary school students with hands-on learning experiences to learn about STEM by communicating with a CubeSat.

9. Industry, Innovation and Infrastructure. Advances in CubeSat technology are driving innovation and industry development. This project aims to demonstrate the technical feasibility of novel communications electronics on CubeSats and provides the space segment infrastructure for Earth-space communications.

10. Reduced inequality. One of the hallmarks of CubeSats is the democratization of access to space, making it available to a wider audience. *Estigia* is being built by students for everyone, to help reduce inequalities in access to education and technology. And this master's thesis plays an essential role in that goal by providing the satellite electronics for low-cost, low-power, long-distance communications.

12. Responsible consumption and production. This project aligns with SDG 12 as it deliberately selects components that do not rely on conflict resources such as tantalum.

17. Partnership for the goals. Pluton UPV maintains collaborative relationships with companies and institutions that also pursue the Sustainable Development Goals. Additionally, open-access publications inherently encourage knowledge-sharing and collaboration.

A

Sustainable Development Goal		Degree of relation			
SDG No.	**Name**	**High**	**Medium**	**Low**	**N/A**
1	No poverty				x
2	Zero hunger				x
3	Good health and wellbeing				x
4	Quality education	x			
5	Gender equality				x
6	Clean water and sanitation				x
7	Affordable and clean energy				x
8	Decent work and economic growth				x
9	Industry, Innovation and Infrastructure	x			
10	Reduced inequality			x	
11	Sustainable cities and communities				x
12	Responsible consumption and production		x		
13	Climate action				x
14	Life below water				x
15	Life on land				x
16	Peace, justice and strong institutions				x
17	Partnership for the goals			x	

Table A.1 – Relationship of this project with the SDGs of the 2030 Agenda.

Appendix B

Project costs

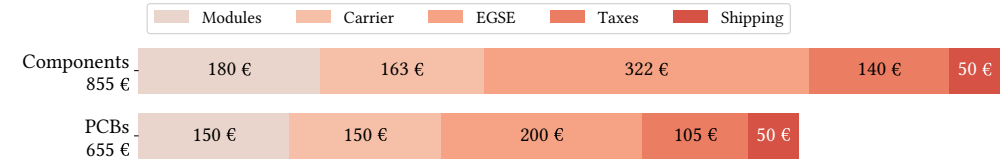
This appendix details the project costs, taking into account the labor and manufacturing costs, assuming that two units of each board are produced. Table B.1 and Figure B.1 summarize the project costs. Table B.2, B.3 and B.4 list the bill of materials (BOM) of the module, carrier and of the EGSE, respectively. Component prices are as of 2024-08-31.

The PCB manufacturing costs are estimated prior to a request for quotation, for 5 units. Shipping costs are also an estimate. Materials are taxed at 21 % VAT/IVA. With approximately 850 hours of work and a gross salary of about 10 €/h, the labor cost is 8500 €. The total project costs are estimated at 10009.80 €.

This budget does not include electricity, equipment (computers, labs), or software. All software used is either sponsored (Altium Designer, Altium 365), student-licensed (AWR, MatLab, SolidWorks), freeware (LTSpice, Saturn PCB toolkit), or free open source (KiCAD, QUCS, Git, TexLive, LibreOffice, Inkscape, GIMP, VSCodium, Jupyter Lab).

(a) Total project cost breakdown: labor and manufacturing.

(b) Breakdown of manufacturing costs: Components and PCBs.



(c) Component and PCB cost breakdown.

Figure B.1 – Bar chart illustrating the costs of the project.

Item	Components (€/u)	Units	Total components cost (€)	Total PCBs cost (€)*	Sum (€)
Modules	90.03	2	180.06	150.00	330.06
Carrier	81.31	2	162.62	150.00	312.62
EGSE	161.22	2	322.44	200.00	522.44
Subtotal (€):			**665.12**	**500.00**	**1165.12**
Value-Added Tax (VAT/IVA) (21 %)			139.68	105.00	244.68
Subtotal with VAT (€):			**804.80**	**605.00**	**1409.80**
Shipping (€)			50.00	50.00	100.00
Subtotal with VAT and shipping (€):			**854.80**	**655.00**	**1509.80**
Labor, 10 €/h, 850 h (€):					**8500.00**
Total cost (€):					**10009.80**

Table B.1 – Breakdown of the project costs. *Estimated cost for 5 PCBs.

B

#	Designator	Qty	Value	Tol.	P/N	Manuf.	€/u	Supplier
1	C201, C207, C305, C306, C307, C308, C313, C418, C422, C437	10	1 uF	10 %	GRT155C71A105KE13D	Murata	0.089	DigiKey
2	C202, C203, C204, C205, C206, C300, C332, C330, C304, C309, C310, C311, C312, C410, C416, C417, C419, C421, C436, C506, C514, C518, C526	23	0.1 uF	10 %	C0402C104K4RECAUTO	KEMET	0.093	DigiKey
3	C400, C408	2	10 pF	±2 %	GJM0335C1E100GB01D	Murata	0.099	DigiKey
4	C401	1	6.8 pF	±.1 pF	GJM0335C1E6R8BB01D	Murata	0.090	DigiKey
5	C402	1	39 pF	±5 %	GJM1555C1H390JB01D	Murata	0.130	DigiKey
6	C403, C409	2	1.5 pF	±.1 pF	GJM0335C1E1R5BB01D	Murata	0.090	DigiKey
7	C404, C405	2	4.7 pF	±.1 pF	GJM0335C1E4R7BB01D	Murata	0.090	DigiKey
8	C406, C413	2	470 nF	±10 %	GRM155R71A474KE01D	Murata	0.360	DigiKey
9	C407, C414	2	3.1 pF	±.1 pF	GJM0335C1H3R1BB01D	Murata	0.090	DigiKey
10	C411	1	47 pF	±5 %	C0201C470J8GAC7867	KEMET	0.090	DigiKey
11	C412	1	47 nF	±20 %	C0402C473M4RAC7867	KEMET	0.090	DigiKey
12	C415, C420	2	100 pF	±5 %	QLCD250Q101J1GV001T	Johanson	0.130	DigiKey
13	C423, C424, C425	3	56 pF	±2 %	GRM0335C1H560GA01D	Murata	0.090	DigiKey
14	C426, C427	2	1.4 pF	±.1 pF	GJM0335C1E1R4BB01D	Murata	0.090	DigiKey
15	C429	1	62 pF	±2 %	GRM0335C1H620GA01D	Murata	0.090	DigiKey
16	C430	1	2.2 pF	±.1 pF	CBR02C229B3GAC	KEMET	0.150	DigiKey
17	C432	1	1 uF	±10 %	CL05A105KO5NNNC	Samsung	0.090	DigiKey
18	C433, C435	2	220 pF	±5 %	GRM0335C1H221JA01D	Murata	0.090	DigiKey
19	C434	1	10 nF	±5 %	GRM1555C1E103JE01J	Murata	0.140	DigiKey
20	C500, C501, C502	3	2.2 nF	±10 %	CC0201KRX7R8BB222	Yageo	0.090	DigiKey
21	C503, C504, C501, C507, C508, C515, C516, C517, C519, C520, C524, C525, C527, C528, C529	15	22 uF	±20 %	GRM188C80J226ME15D	Murata	0.136	DigiKey
22	C510, C511, C512	3	10 uF	±10 %	GMC10X7R106K10NT	Cal-Chip	0.410	DigiKey
23	C513, C522, C531	3	470 nF	±10 %	CGA2B1X7S1C474K050BC	TDK	0.230	DigiKey
24	C523	1	47 uF	±20 %	GRM21BR61A476ME15K	Murata	0.600	DigiKey
25	D200	1			RCLAMP0561PQTCT	Semtech	0.420	DigiKey
26	D201, D301	2	Green		EAST10052GA0	Everlight	0.310	DigiKey
27	D202, D302	2	Yellow		FHY1105P-TR	Stanley	0.310	DigiKey
28	D203, D300	2	Red		EAST10053RA0	Everight	0.310	DigiKey
29	FB500, FB501, FB502, FB503, FB504	5	8.5 Ohm @ 100 MHz		BLE18PS080SN1D	Murata	0.280	DigiKey
30	L400, L406	2	100 nH	±5 %	LQW15AWR10J80D	Murata	0.240	DigiKey
31	L401	1	10 nH	±2 %	LQW15AN10NG80D	Murata	0.210	DigiKey
32	L402	1	5.6 nH	±2 %	LQW15AN5N6G8ZD	Murata	0.210	DigiKey
33	L403, L407	2	68 nH	±2 %	LQW15AN68NG0ZD	Murata	0.180	DigiKey
34	L404, L408	2	15 uH	±20 %	VLS252010CX-150M-1	TDK	0.340	DigiKey
35	L405, L409	2	82 nH	±2 %	LQW15AN82NG00D	Murata	0.130	DigiKey
36	L410, L411	2	100 nH	±5 %	LQW15ANR10J00D	Murata	0.130	DigiKey
37	L412	1	6 nH	±0.1 nH	LQW15AN6N0B8ZD	Murata	0.210	DigiKey
38	L413	1	2.2 nH	±0.5 nH	LQW15AN2N2D10D	Murata	0.140	DigiKey
39	L500, L501, L502	3	2.2 uH	±20 %	SRN4018-2R2M	Bourns	0.380	DigiKey
40	R200, R210, R211, R212, R213, R20, R20, R214, R301, R302, R303, R304, R305, R306, R308, R309, R310, R311, R402, R405	18	0 Ohm		AC0201JR-070RL	Yageo	0.090	DigiKey

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Table B.2 – LoRa module: bill of materials.

Continued from previous page

#	Designator	Qty	Value	Tol.	P/N	Manuf.	Price	Supplier
41	R201	1	100 Ohm	±5 %	EXB-2HV101JV	Panasonic	0.280	DigiKey
42	R202, R314, R315, R316	4	680 Ohm	±5 %	RC0201JR-07680RL	Yageo	0.090	DigiKey
43	R203	1	750 Ohm	±5 %	RC0201JR-07750RL	Yageo	0.090	DigiKey
44	R204	1	1.5 kOhm	±5 %	CRCW02011K50JNED	Vishay	0.090	DigiKey
45	R205	1	100 Ohm	±5 %	EXB-28V101JX	Panasonic	0.090	DigiKey
46	R206, R207, R312, R313	4	4.7 kOhm	±1 %	AC0201FR-074K7L	Yageo	0.090	DigiKey
47	R208	1	47 kOhm	±1 %	AC0201FR-0747KL	Yageo	0.090	DigiKey
48	R209	1	33 kOhm	±1 %	CRCW020133KOFKED	Vishay	0.140	DigiKey
49	R300, R307	2	10 kOhm	±1 %	AF0201FR-0710KL	Yageo	0.090	DigiKey
50	R400, R401	2	220 Ohm	±1 %	RC0201FR-07220RL	Yageo	0.090	DigiKey
51	R403, R407, R408	3	1 kOhm	±1 %	RC0201FR-071KL	Yageo	0.090	DigiKey
52	R404	1	5.1 kOhm	±1 %	ERJ-1GNF5101C	Panasonic	0.090	DigiKey
53	R406	1	3.3 kOhm	±1 %	ERJ-1GJF3301C	Panasonic	0.140	DigiKey
54	R500, R504, R507	3	100 kOhm	±1 %	RC0201FR-13100KL	Yageo	0.090	DigiKey
55	R501	1	2.49 kOhm	±1 %	AC0201FR-072K49L	Yageo	0.090	DigiKey
56	R502, R506, R509	3	4.87 kOhm	±1 %	RC0201RR-074K87L	Yageo	0.090	DigiKey
57	R505	1	15.4 kOhm	±1 %	RC0201FR-0715K4L	Yageo	0.090	DigiKey
58	R508	1	19.1 kOhm	±1 %	RC0201FR-0719K1L	Yageo	0.090	DigiKey
59	SH1	1			MS375-10F	Masach	1.940	DigiKey
60	SH1 (cover)	1			MS375-10C	Masach	1.370	DigiKey
61	U201	1			STTS751-0DP3F	STM	1.390	DigiKey
62	U300	1			SX1302IMLTRT	Semtech	24.09	DigiKey
63	U400, U402	2			SX1250IMLTRT	Semtech	9.020	DigiKey
64	U401	1			JPS-2-1N+	Mini Circuits	8.720	DigiKey
65	U403	1			SKY65366-21	Skyworks	2.550	DigiKey
66	U500, U501, U502	3			TPS62912RPUR	Texas I	1.960	DigiKey
67	Y400	1		±0.5 ppm	FT2MNTUM-32.0-T1	Fox Electr.	2.550	DigiKey

Table B.2 – LoRa module: bill of materials.

#	Designator	Qty	Value	Tol.	P/N	Manuf.	€/u	Supplier
1	ANT500	1			CONMMCX013	TE Con.	3.099	DigiKey
2	C200, C201	2	220 pF	±5 %	GRM0335C1E221JA01D	Murata	0.090	DigiKey
3	C202	1	47 uF	±20 %	GRM21BR61A476ME15K	Murata	0.600	DigiKey
4	C203, C301, C303, C403, C406, C708	6	1 uF	±10 %	GRT155C71A105KE13D	Murata	0.089	DigiKey
5	C204, C205, C206, C207, C208, C209, C210, C211, C212, C300, C302, C400, C404, C407, C408, C409, C40, C411, C501, C502, C603, C606, C611, C613, C614, C774, C705, C700, C707, C709, C710, C800, C801, C802, C803, C804	36	0.1 uF	±10 %	C0402C104K4RECAUTO	KEMET	0.093	DigiKey
6	C401, C402	2	12 pF	±1 %	CBR02C120F3GAC	KEMET	0.070	DigiKey
7	C405, C503	2	10 nF	±5 %	GRM1555C1E103JE01J	Murata	0.140	DigiKey
8	C412, C805	2	4.7 uF	±10 %	GRM188271C475KE21J	Murata	0.040	DigiKey
9	C500, C504, C505	3	100 pF	±5 %	CBR04C101J3GAC	KEMET	0.020	DigiKey
10	C600, C601, C602, C604, C605, C608, C609, C610	8	22 uF	±20 %	C2012X7S1A226M125AC	TDK	0.230	DigiKey
11	C607, C612	2	0.47 uF	±10 %	CGA2B1X7S1C474K050BC	TDK	0.230	DigiKey
12	C615, C616, C618, C619	4	10 uF	±10 %	C2012X7S1E106K125AC	TDK	0.110	DigiKey
13	C617, C620	2	2200 pF	±10 %	CC0201KRX7R8BB222	Yageo	0.090	DigiKey

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Table B.3 – Carrier: bill of materials.

Continued from previous page

#	Designator	Qty	Value	Tol.	P/N	Manuf.	Price	Supplier
14	C700, C702	2	3300 pF	±5 %	GRM1557U1A332JA01D	Murata	0.090	DigiKey
15	C701, C703	2	2200 pF	±5 %	C0402C222J8JAC7867	KEMET	0.020	DigiKey
16	CN200, CN201	2			SSQ-126-04-G-D	Samtec	9.290	DigiKey
17	CN300, CN301	2			679101002	Molex	2.430	DigiKey
18	CN302, CN303	2			480994000	Molex	1.550	DigiKey
19	CN800	1			FTSH-105-L-DV	Samtec	1.680	DigiKey
20	CN803	1			USB4105-GF-A	GCT	0.730	DigiKey
21	D200	1			RCLAMP0561PQTCT	Semtech	0.420	DigiKey
22	D500	1			LXES15AAA1-153	Murata	0.040	DigiKey
23	D600	1	Green		EAST10052GA0	Everight	0.310	DigiKey
24	D601	1	Yellow		FHY1105P-TR	Stanley	0.310	DigiKey
25	D800, D801, D802, D803, D804, D805, D806, D807, D808, D809	10			PESD3V3L1BA,115	Nexperia	0.060	DigiKey
26	FB500, FB600, FB800	3	8.5 Ohm @ 100 MHz		BLE18PS080SN1D	Murata	0.280	DigiKey
27	L400	1	100 nH	±5 %	B82496C3101J000	TDK	0.160	DigiKey
28	L600, L601	2	2.2 uH	±20 %	SRN4018-2R2M	Bourns	0.380	DigiKey
29	Q200	1			BSS84-7-F	Diodes Inc	0.020	DigiKey
30	R200, R204	2	120 Ohm	±1 %	CRCW0201120RFNED	Vishay	0.090	DigiKey
31	R201, R205, R206, R600, R604, R702, R703, R704, R705	9	100 kOhm	±1 %	RC0201FR-13100KL	Yageo	0.090	DigiKey
32	R202, R203	2	1 MOhm	±5 %	CRCW02011M00JNED	Vishay	0.090	DigiKey
33	R300, R301, R400, R401, R501, R608, R609	7	10 kOhm	±1 %	AF0201FR-0710KL	Yageo	0.090	DigiKey
34	R302, R303, R304, R305, R306, R307, R310, R311, R711, R712	10	4.7 kOhm	±1 %	AC0201FR-074K7L	Yageo	0.090	DigiKey
35	R308, R312	2	47 KOhm	±1 %	AC0201FR-0747KL	Yageo	0.090	DigiKey
36	R309, R313	2	12 kOhm	±1 %	CRCW020112K0FNED	Vishay	0.090	DigiKey
37	R402, R403	2	0 Ohm		AC0201JR-070RL	Yageo	0.090	DigiKey
38	R500	1	49.9 Ohm	±.1 %	PHPA1206E49R9BST1	Vishay	1.850	DigiKey
39	R601, R606	2	15.4 kOhm	±1 %	RC0201FR-0715K4L	Yageo	0.090	DigiKey
40	R602	1	1.5 kOhm	±5 %	CRCW02011K50JNED	Vishay	0.100	DigiKey
41	R603, R607	2	4.87 kOhm	±1 %	RC0201FR-074K87L	Yageo	0.090	DigiKey
42	R605	1	680 Ohm	±5 %	RC0201JR-07680RL	Yageo	0.090	DigiKey
43	R700, R701	2	470 kOhm	±1 %	RC0201FR-13470KL	Yageo	0.090	DigiKey
44	R706	1	10.5 kOhm	±1 %	RC0201FR-0710K5L	Yageo	0.090	DigiKey
45	R707	1	59 kOhm	±1 %	RC0201FR-0759KL	Yageo	0.090	DigiKey
46	R708	1	47 kOhm	±1 %	RC0201FR-0747KL	Yageo	0.090	DigiKey
47	R709, R710	2	1.8 kOhm	±1 %	RC0201FR-071K8L	Yageo	0.090	DigiKey
48	R713	1	10 mOhm	±.5 %	L4T12FR010DER	Ohmite	0.080	DigiKey
49	R800, R801	2		±1 %	YC124-FR-0749R9L	Yageo	0.030	DigiKey
50	R802	1	430 kOhm	±1 %	ERJ-1GNF4303C	Panasonic	0.090	DigiKey
51	R803	1	620 kOhm	±1 %	ERJ-1GNF6203C	Panasonic	0.090	DigiKey
52	R804, R805	2	5.1 kOhm	±1 %	AC0201FR-075K1L	Yageo	0.090	DigiKey
53	S400	1			430152043836	Würth	0.500	DigiKey
54	S401	1			450404015514	Würth	0.710	DigiKey
55	U200, U201	2			MCP2542FDT-E/MF	Microchip	0.980	DigiKey
56	U300, U301	2			STTS751-0DP3F	STM	1.390	DigiKey
57	U400	1			STM32L496RGT3	STM	13.19	DigiKey
58	U500	1			SKY13396-397LF	Skyworks	1.000	DigiKey
59	U600, U601	2			TPS62912RPUR	Texas I	1.960	DigiKey
60	U700, U701	2			TPS259470ARPWR	Texas I	1.320	DigiKey
61	U702	1			INA232AIDDFR	Texas I	2.220	DigiKey
62	U800	1			USBLC6-2SC6	STM	0.310	DigiKey
63	Y400	1	32.768 kHz	±10 ppm	ABS07-32.768KHZ-9-1-T	Abracon	1.440	DigiKey

Table B.3 – Carrier: bill of materials.

#	Designator	Qty	Value	Tol.	P/N	Manuf.	€/u	Supplier
1	C200, C201, C202, C215	4	220 pF	±5 %	GRM0335C1E221JA01D	Murata	0.090	DigiKey
2	C203, C620	2	47 µF	±20 %	GRM21BR61A476ME15K	Murata	0.600	DigiKey
3	C204, C403, C406, C538, C704, C706	6	1 µF	±10 %	GRT155C71A105KE13D	Murata	0.130	DigiKey
4	C205, C206, C207, C208, C209, C210, C211, C212, C213, C214, C400, C404, C407, C408, C409, C410, C411, C516, C518, C520, C522, C525, C528, C537, C551, C555, C556, C557, C558, C559, C606, C611, C615, C618, C621, C627, C700, C701, C702, C703, C705, C800, C801, C802, C803, C804	46	0.1 µF	±10 %	C0402C104K4RECAUTO	KEMET	0.090	DigiKey
5	C401, C402	2	12 pF	±1 %	CBR02C120F3GAC	KEMET	0.090	DigiKey
6	C405, C524, C527, C535, C552	5	10000 pF	±5 %	GRM1555C1E103JE01J	Murata	0.090	DigiKey
7	C412, C805	2	4.7 µF	±10 %	GRM188Z71C475KE21J	Murata	0.090	DigiKey
8	C500, C501, C502, C503, C504, C505, C506, C507, C508, C509, C529, C530	12	56 pF	±2 %	GRM0335C1H560GA01D	Murata	0.090	DigiKey
9	C510, C511	2	1.4 pF	±.1 pF	GJM0335C1E1R4BB01D	Murata	0.090	DigiKey
10	C512, C531, C532, C542, C550	5	100 pF	±5 %	QLCD250Q101J1GV001T	Johanson	0.090	DigiKey
11	C513	1	2.2 pF	±0.1 pF	CBR02C229B3GAC	KEMET	0.090	DigiKey
12	C514	1	62 pF	±1 %	CBR06C620F5GAC	KEMET	0.090	DigiKey
13	C515, C517, C519, C521, C523, C526, C534, C536	8	220 pF	±5 %	GRM0335C1H221JA01D	Murata	0.090	DigiKey
14	C533	1	1 µF	±10 %	CL05A105KO5NNNC	Samsung	0.090	DigiKey
15	C539, L400, L508	3	100nH	±5 %	B82496C3101J000	TDK	0.320	DigiKey
16	C540	1	220 Ohm	±1 %	RC0201FR-07220RL	Yageo	0.090	DigiKey
17	C541	1	10 pF	±2 %	GJM0335C1E100GB01D	Murata	0.090	DigiKey
18	C543, C553, C554, C560	4	47 pF	±10 %	QLCD250Q470K1GV001T	Johanson	0.090	DigiKey
19	C544, C549	2	4.7 pF	±.1 pF	GJM0335C1E4R7BB01D	Murata	0.090	DigiKey
20	C545, C546	2	6.8 pF	±.1 pF	GJM0335C1E6R8BB01D	Murata	0.090	DigiKey
21	C547	1	2.2 pF	±0.1 pF	GJM0335C1E2R2BB01D	Murata	0.090	DigiKey
22	C548, R400, R401, R503, R504, R505, R506, R507, R508, R509, R510, R514, R603	13	10 kOhm	±1 %	AF0201FR-0710KL	Yageo	0.090	DigiKey
23	C561	1	32 MHz	±.5 ppm	FT2MNTUM-32.0-T1	Fox Electr.	2.550	DigiKey
24	C600, C601, C602	3	2200 pF	±10 %	CC0201KRX7R8BB222	Yageo	0.090	DigiKey
25	C603, C604, C605, C612, C613, C614, C616, C617, C622, C623, C624, C625, C626	13	22 µF	±20 %	GRM188C80J226ME15D	Murata	0.136	DigiKey
26	C607, C608, C609	3	10 µF	±10 %	C2012X7S1E106K125AC	TDK	0.110	DigiKey

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Table B.4 – EGSE: bill of materials.

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#	Designator	Qty	Value	Tol.	P/N	Manuf.	Price	Supplier
27	C610, C619, C628	3	0.47 µF	±10 %	CGA2B1X7S1C474K050BC	TDK	0.230	DigiKey
28	CN200, CN202	4			SSQ-126-04-G-D	Samtec	9.290	DigiKey
29	CN500	1			CONMMCX013	TE Con.	3.099	DigiKey
30	CN800	1			FTSH-105-L-DV	Samtec	1.680	DigiKey
31	CN803	1			USB4105-GF-A	GCT	0.730	DigiKey
32	D500	1			LXES15AAA1-153	Murata	0.040	DigiKey
33	D600	1	Green		EAST10052GA0	Everlight	0.310	DigiKey
34	D601, D602	2	Yellow		FHY1105P-TR	Stanley	0.310	DigiKey
35	D603	1	Red		EAST10053RA0	Everlight	0.310	DigiKey
36	D800, D801, D802, D803, D804, D805, D806, D807, D808, D809	10			PESD3V3L1BA,115	Nexperia	0.420	DigiKey
37	EGSE_IO, PAYL_IO	2			CON-SMA-EDGE-S	RF Solutions	2.360	DigiKey
38	FB600, FB601, FB800	3	8.5 Ohm @ 100 MHz		BLE18PS080SN1D	Murata	0.280	DigiKey
39	L500, L501	2	100 nH	±5 %	LQW15ANR10J00D	Murata	0.130	DigiKey
40	L502	1	6 nH	±.1nH	LQW15AN6N0B8ZD	Murata	0.210	DigiKey
41	L503	1	2.2 nH	±.5nH	LQW15AN2N2D10D	Murata	0.140	DigiKey
42	L504	1	2.2 pF	±.1 pF	GJM0335C1E2R2BB01D	Murata	0.090	DigiKey
43	L505	1	3.3 nH	±.5nH	LQW15AN3N3D8ZD	Murata	0.180	DigiKey
44	L506	1	15 nH	±5 %	LQW15AN15NJ8ZD	Murata	0.180	DigiKey
45	L507	1	18 nH	±2 %	LQW15AN18NG8ZD	Murata	0.210	DigiKey
46	L600, L601, L602	3	2.2 µH	±20 %	SRN4018-2R2M	Bourns	0.380	DigiKey
47	Q200, Q201	2			BSS84-7-F	Diodes	0.220	DigiKey
48	R200, R204	2	120 Ohm	±1 %	CRCW0201120RFNED	Vishay	0.090	DigiKey
49	R201, R205, R206, R207, R600, R604, R611, R703	8	100 kOhm	±1 %	RC0201FR-13100KL	Yageo	0.090	DigiKey
50	R202, R203	2	1 MOhm	±5 %	CRCW02011M00JNED	Vishay	0.090	DigiKey
51	R402, R403, R515, R517	4	0 Ohm		AC0201JR-070RL	Yageo	0.090	DigiKey
52	R500	1	1 kOhm	±5 %	EXB-28V102JX	Panasonic	0.090	DigiKey
53	R501	1	4.7 kOhm	±5 %	EXB-28V472JX	Panasonic	0.090	DigiKey
54	R502	1	10 kOhm	±5 %	YC248-JR-0710KL	Yageo	0.250	DigiKey
55	R511, R512	2	49.9 Ohm	±.1 %	PHPA1206E49R9BST1	Vishay	1.850	DigiKey
56	R513	1	1 kOhm	±1 %	AC0201FR-071KL	Yageo	0.090	DigiKey
57	R516	1	5.1 kOhm	±1 %	ERJ-1GNF5101C	Panasonic	0.170	DigiKey
58	R518	1	3.3 kOhm	±1 %	ERJ-1GJF3301C	Panasonic	0.170	DigiKey
59	R601	1	2.49 kOhm	±1 %	AC0201FR-072K49L	Yageo	0.090	DigiKey
60	R602, R606, R613	3	4.87 kOhm	±1 %	RC0201FR-074K87L	Yageo	0.090	DigiKey
61	R605	1	15.4 kOhm	±1 %	RC0201FR-0715K4L	Yageo	0.090	DigiKey
62	R607, R608	2	680 Ohm	±5 %	RC0201JR-07680RL	Yageo	0.090	DigiKey
63	R609	1	750 Ohm	±5 %	RC0201JR-07750RL	Yageo	0.090	DigiKey
64	R610	1	1.5 kOhm	±5 %	CRCW02011K50JNED	Vishay	0.090	DigiKey
65	R612	1	19.1 kOhm	±1 %	RC0201FR-0719K1L	Yageo	0.090	DigiKey
66	R700, R701	2	4.7 kOhm	±1 %	AC0201FR-074K7L	Yageo	0.090	DigiKey
67	R702	1	10 mOhm	±.5 %	L4T12FR010DER	Ohmite	0.400	DigiKey
68	R800, R801	2		±1 %	YC124-FR-0749R9L	Yageo	0.310	DigiKey
69	R802, R803	2	5.1 kOhm	±1 %	AC0201FR-075K1L	Yageo	0.090	DigiKey
70	S400	1			430152043836	Würth	0.500	DigiKey
71	S401	1			450404015514	Würth	0.710	DigiKey
72	U200, U201	2			MCP2542FDT-E/MF	Microchip	0.980	DigiKey
73	U400	1			STM32L496RGT3	STM	13.19	DigiKey
74	U500	1			YAT-3A+	Mini Circuits	4.090	DigiKey
75	U501	1			YAT-30A+	Mini Circuits	4.090	DigiKey
76	U502, U503, U504, U505	4			DAT-31R5A-PP+	Mini Circuits	7.260	DigiKey
77	U506, U507	2			SKY13373-460LF	Skyworks	1.110	DigiKey
78	U508	1			SKY65366-21	Skyworks	2.550	DigiKey
79	U509	1			SX1276IMLTRT	Semtech	9.050	DigiKey
80	U600, U601, U602	3			TPS62912RPUR	Texas I	1.960	DigiKey
81	U700	1			INA232AIDDFR	Texas I	2.220	DigiKey
82	U701	1			MIC94080YFT	Microchip	0.410	DigiKey
83	U800	1			USBLC6-2SC6	Diodes	0.310	DigiKey
84	Y400	1	32.768 kHz	±10 ppm	ABS07-32.768KHZ-9-1-T	Abracon	1.440	DigiKey

Table B.4 – EGSE: bill of materials.

Appendix C

Circuit schematics

The following pages contain the complete circuit schematics of the three developed printed circuit boards. The schematics are self-contained and include notes about their operation. For a more detailed explanation of how the schematics should be interpreted, please refer to section 4.1: Schematic capture.

To locate the schematics of each PCB, please refer to the table of contents below:

PROJECT:

LoRa Comms Payload: System-on-Module

PART OF THE MASTER'S THESIS:

"Development of a LoRa-based communications payload for CubeSat"

MASTER'S DEGREE IN ELECTRONIC SYSTEMS ENGINEERING
POLYTECHNIC UNIVERSITY OF VALENCIA
ACADEMIC COURSE 2023/2024

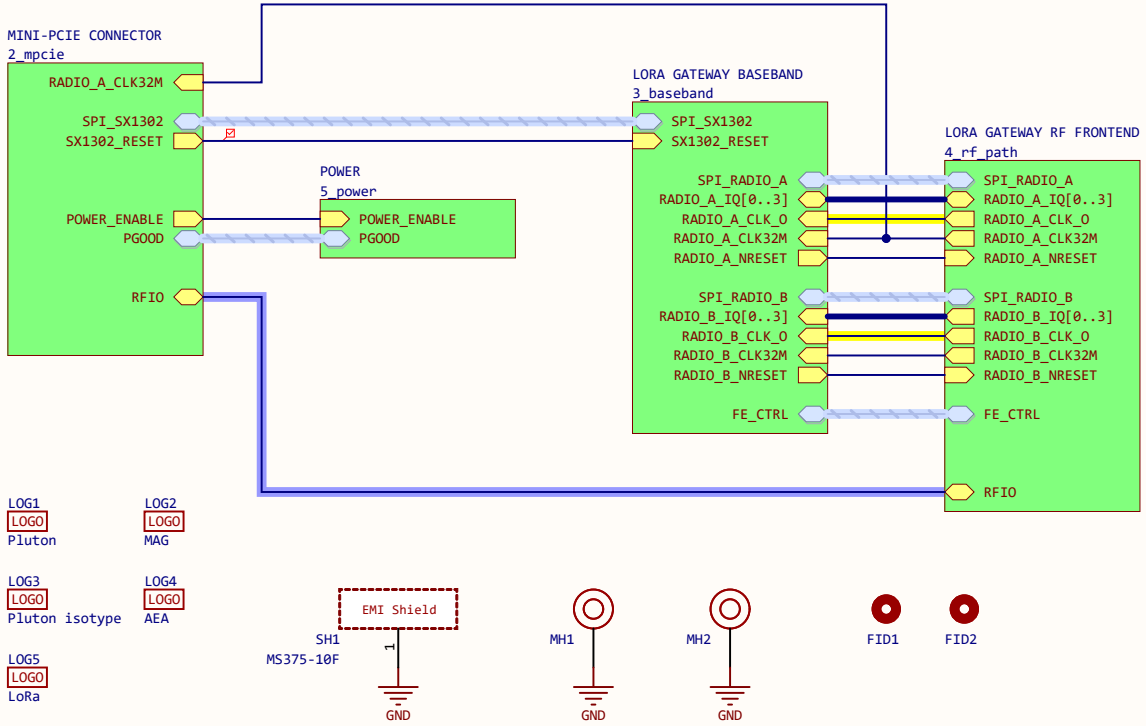
AUTHOR:

Juan Del Pino Mena

SUPERVISORS:

Jorge Daniel Martínez Pérez
DEPARTMENT OF ELECTRONIC ENGINEERING

Vicente Enrique Boria Esbert
DEPARTMENT OF COMMUNICATIONS



DEVELOPED IN PROUD COLLABORATION WITH:

UNIVERSITAT POLITÈCNICA DE VALÈNCIA
GENERACIÓN ESPONTÁNEA
TELECOM UPV VLC
DEPARTAMENTO DE INGENIERÍA ELECTRÓNICA
iTEAM Instituto de Telecomunicaciones y Aplicaciones Multimedia
MICROWAVE APPLICATIONS GROUP

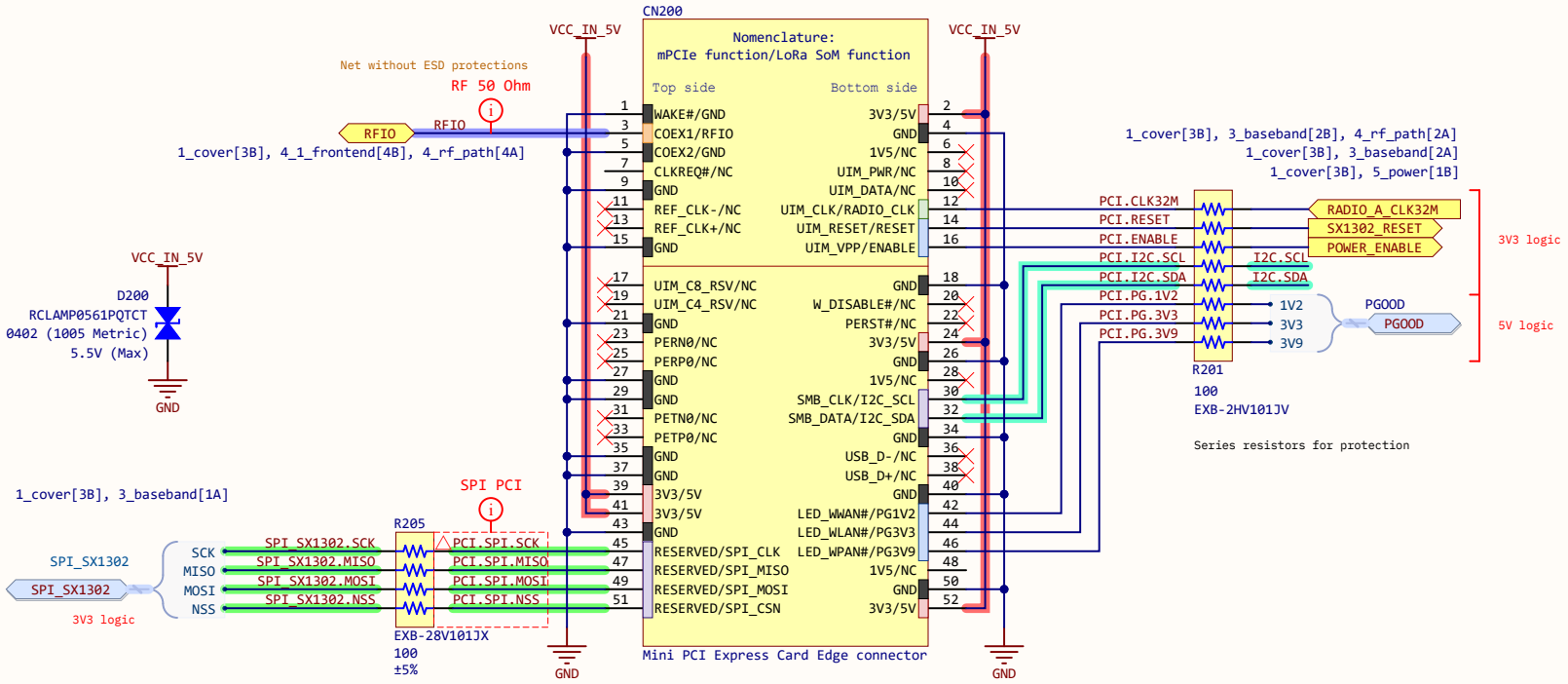
Notes:

System-on-Module device with mPCIe form factor containing a LoRa gateway and RF frontend, with output via MMCX connector.

Title: *Cover and Block Diagram*		**Author:** Juan Del Pino Mena	**Pluton UPV** *Universitat Politècnica de València (UPV) Camí de Vera, València Spain*
Prj: Estigia comms payload - LoRa Gateway SoM		**Approved:** --	
		Prj. revision: 0.4	
		Variant: [No Variations]	
Date: 2024-08-11 13:32:40	**Last modified:** 2024-08-11	**Altium version:** 24.3.1.35	
Size: A4	Sheet 1 of 6	**License:** --	
File: 1_cover.SchDoc		**Git Hash:** 33fbb304962290060a8401dcbf550be183a479c3 [Locally Modified]	

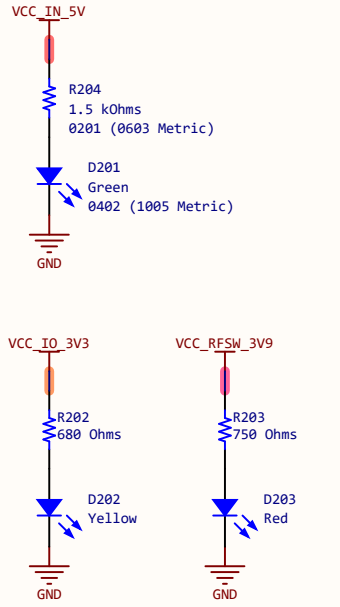
PLUTON

Mini-PCI-express card edge connector

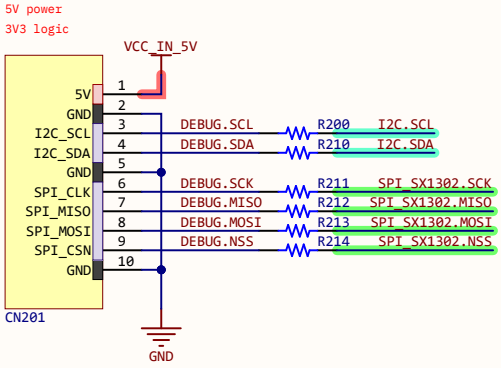


Power LED indicators

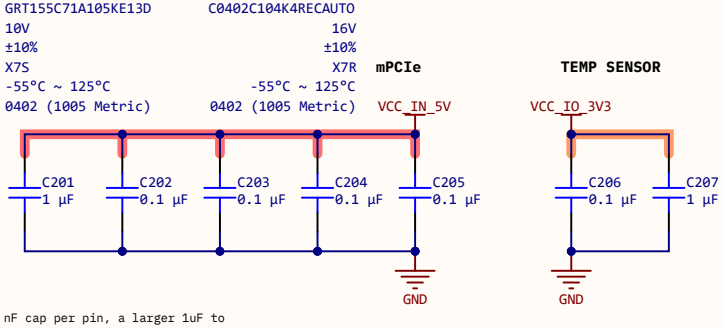
1V2 does not have an indicator since is too low voltage to lit a LED



Debug ports

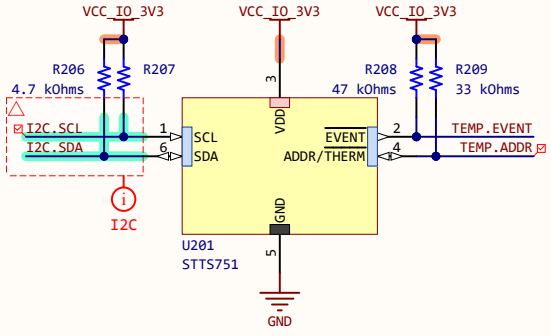


Decopling capacitors



One 100 nF cap per pin, a larger 1uF to stabilize supply. Place near the mPCIe pins.

Temperature sensor



i2C addr 0b011_1001 (0x39)

Notes:

The mPCIe connector is used in a non-standard configuration, neither the signals, nor the supply voltages. DO NOT CONNECT TO A REGULAR MPCIE SOCKET.

[1] Texas Instruments Inc. TXB0104 datasheet, SCES650J, 10-2020

[2] STMicroelectronics Inc. STTS751 datasheet, DocID 16483, Rev 7, 05-2019

Title:	***Mini-PCIe and thermal sensor***	**Author:**	Juan Del Pino Mena
		Approved:	--
Prj:	Estigia comms payload - LoRa Gateway SoM	**Prj. revision:**	0.4
		Variant:	[No Variations]
Date:	2024-08-11 13:32:41	**Last modified:**	2024-08-11
Size:	A4	Sheet 2 of 6	**Altium version:** 24.3.1.35
File:	2_mpcie.SchDoc	**License:**	--
		Git Hash:	41b6ea28c7eaa4a034106408df395347186357a6 [Locally Modified]

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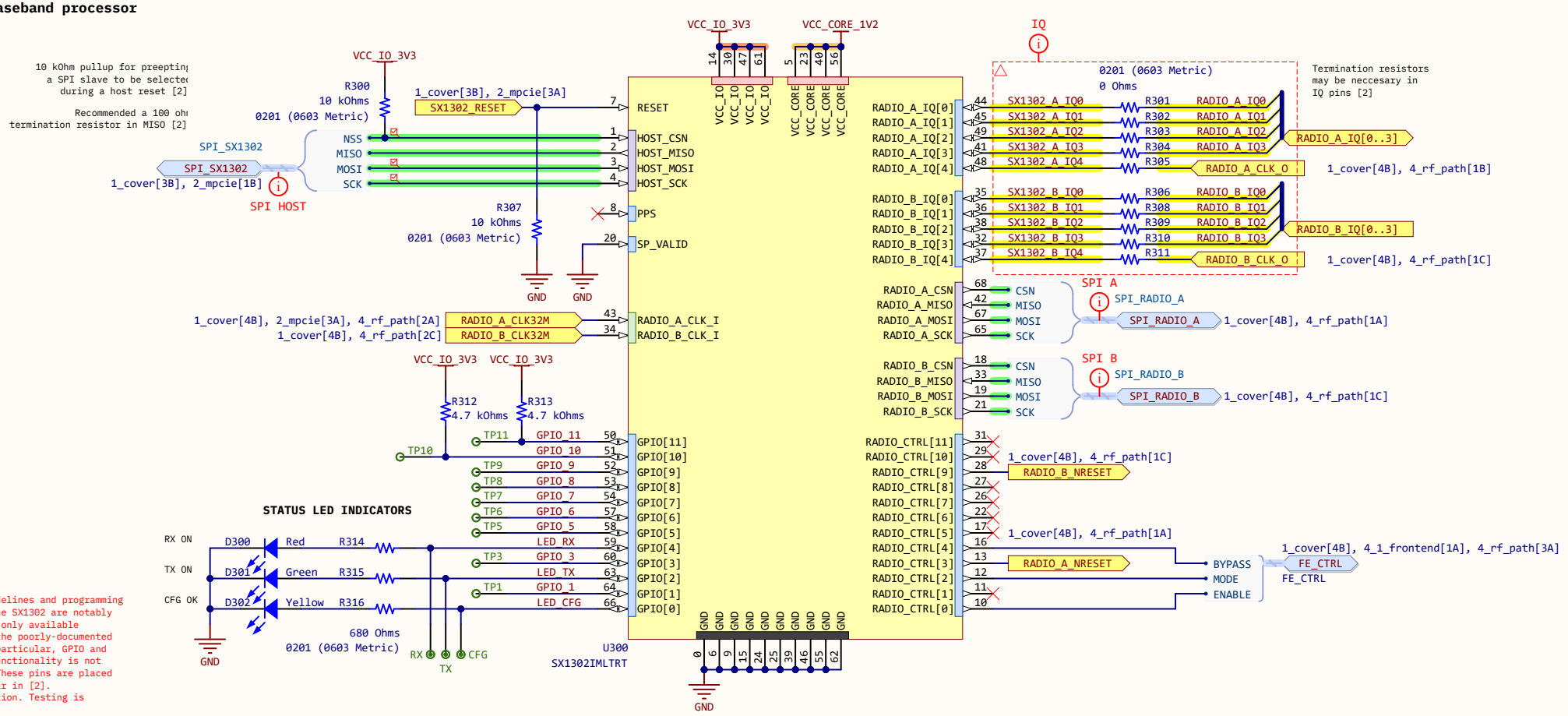
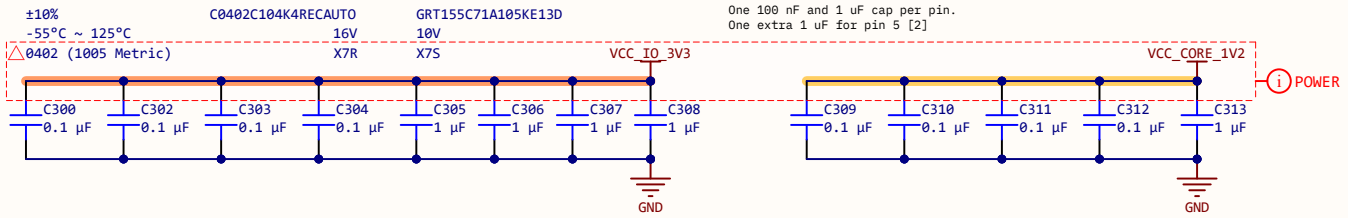
Camí de Vera, València
Spain

SX1302 baseband processor



Decoupling capacitors



Notes:

[1] Semtech Inc. SX1302 LoRa Gateway Baseband Processor Datasheet, DS.SX1302.W.APP, v1.2, 10-2020
[2] Semtech Inc. SX1302 Corecell Reference Design with SX1250 RF Front-Ends, PCB_E539V01A, 01-2020
[3] Semtech Inc. SX1302 Hardware Abstraction Layer repo, https://github.com/Lora-net/sx1302_hal

Title: *LoRa Baseband processor*		**Author:** Juan Del Pino Mena	
		Approved: --	
Prj: Estigia comms payload - LoRa Gateway SoM		**Prj. revision:** 0.4	
		Variant: [No Variations]	
Date: 2024-08-11 13:32:41	**Last modified:** 2024-08-11	**Altium version:** 24.3.1.35	
Size: A4	Sheet 3 of 6	**License:** --	
File: 3_baseband.SchDoc		**Git Hash:** 41b6ea28c7eaa4a034106408df395347186357a6 [Locally Modified]	

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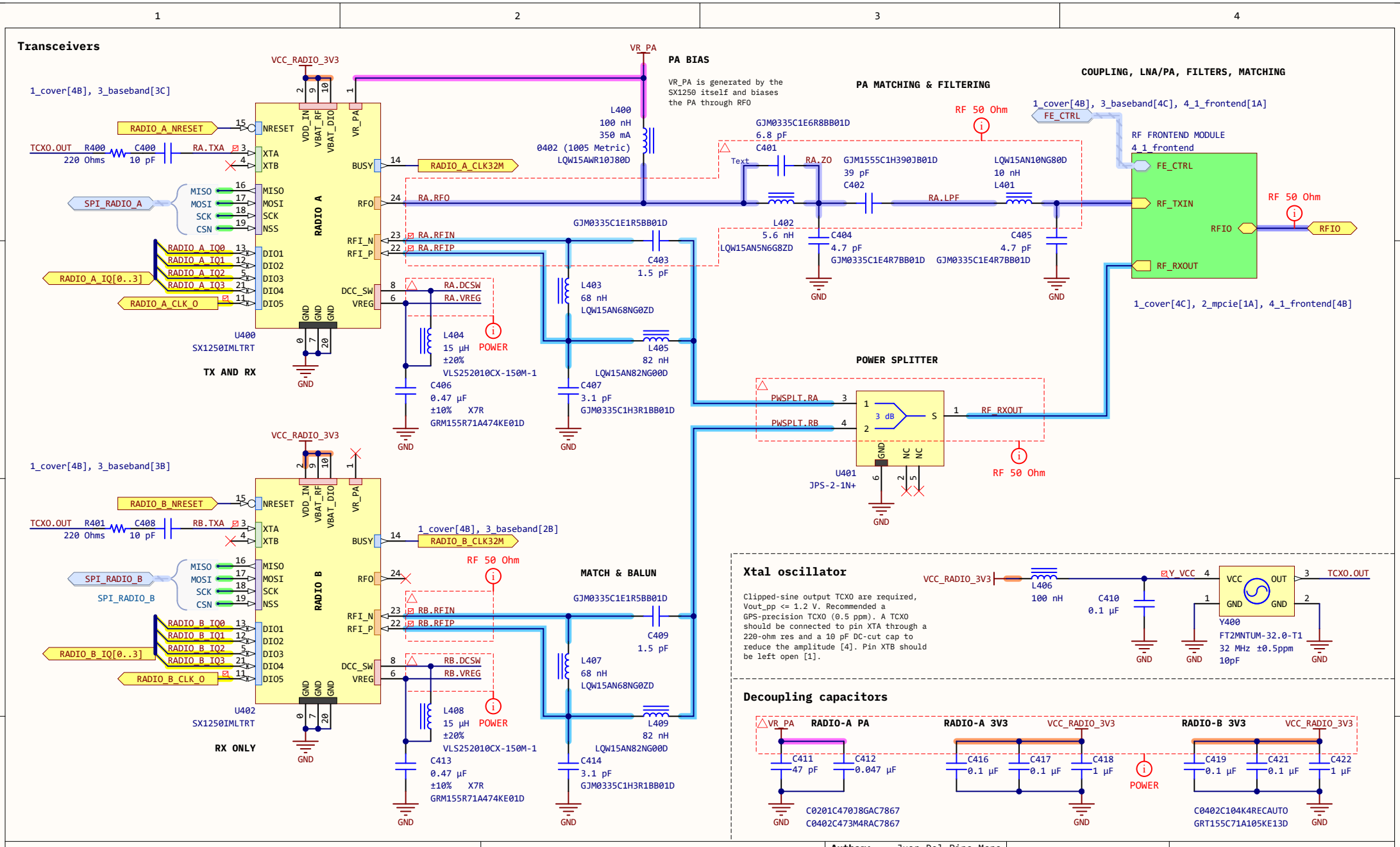

Notes:

[1] Semtech Inc. SX1302 LoRa Gateway Baseband Processor Datasheet, DS.SX1302.W.APP, v1.2, 10-2020
[2] Semtech Inc. SX1302 Corecell Reference Design with SX1250 RF Front-Ends, PCB_E539V01A, 01-2020
[3] Semtech Inc. SX1250 Multi-band Sub-GHz RF Front End Datasheet, DS.SX1250.W.APP, v1.2, 09-2019
[4] Semtech Inc. PCB Design Guidelines, AN1200.66, v1.1, 09-2022
[5] Semtech Inc. SX1261/2 Reference Design Explanation, AN1200.40, v1.1, 05-2018
[6] Silicon Labs Inc. Si446x/Si4362 RX LNA Matching, AN643, v0.4, 2014

Title: *LoRa Transceivers*		**Author:** Juan Del Pino Mena	
Prj: Estigia comms payload - LoRa Gateway SoM		**Approved:** --	
		Prj. revision: 0.4	
Date: 2024-08-11 13:32:42	**Last modified:** 2024-08-11	**Variant:** [No Variations]	
Size: A4	Sheet 4 of 6	**Altium version:** 24.3.1.35	
File: 4_rf_path.SchDoc		**License:** --	
		Git Hash: 41b6ea28c7eaa4a034106408df395347186357a6 [Locally Modified]	

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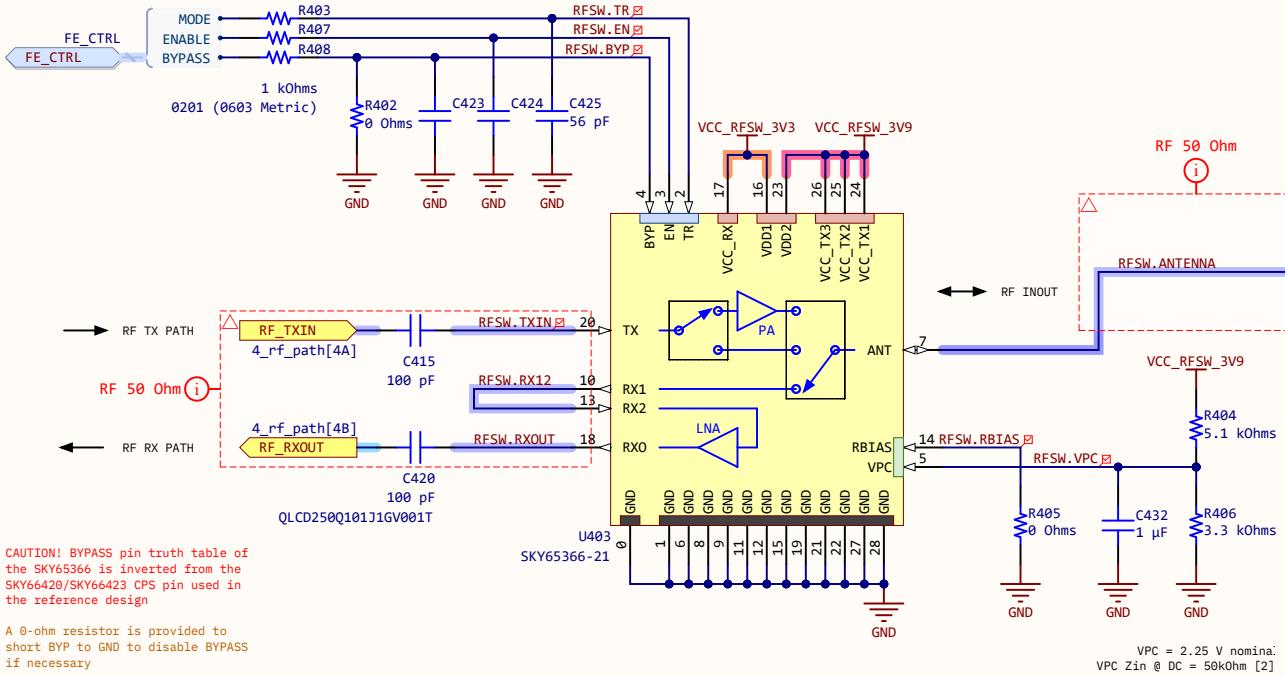
RF Frontend module

4_rf_path[4A], 3_baseband[4C], 4_rf_path[3A]

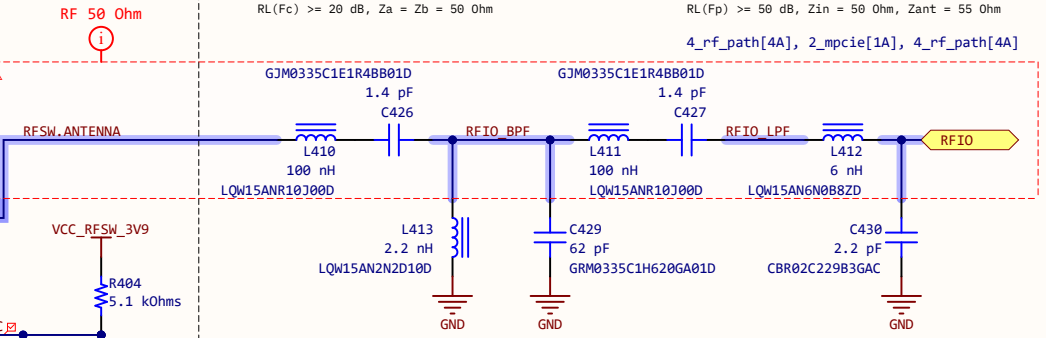


Band Filtering, antenna matching and ESD protection

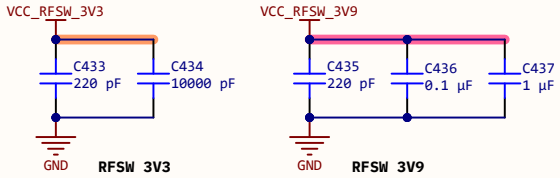
3rd order Chebyshev band-pass filter
Fc = 435 MHz, BW = 50 MHz, IL(Fc) = 1 dB,
RL(Fc) >= 20 dB, Za = Zb = 50 Ohm

LC lowpass filter & antenna matching
Fp = 435 MHz, Fc = 600 MHz, IL(Fp) = 0.1 dB,
RL(Fp) >= 50 dB, Zin = 50 Ohm, Zant = 55 Ohm

4_rf_path[4A], 2_mpcie[1A], 4_rf_path[4A]



Decoupling capacitors



Notes:

[1] Semtech Inc. SX1302 Corecell Reference Design with SX1250 RF Front-Ends, PCB_E539V01A, 01-2020
[2] Skyworks Inc. SKY65366-21 400 MHz Tx/Rx Front-End Module, 203146E, 10-2020

Title:	*RF FrontEnd module*
Prj:	Estigia comms payload - LoRa Gateway SoM
Date:	2024-08-11 13:32:42
Last modified:	2024-08-11
Size:	A4
Sheet	5 of 6
File:	4_1_frontend.SchDoc

Author:	Juan Del Pino Mena
Approved:	--
Prj. revision:	0.4
Variant:	[No Variations]
Altium version:	24.3.1.35
License:	--
Git Hash:	41b6ea28c7eaa4a034106408df395347186357a6 [Locally Modified]

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Camí de Vera, València
Spain

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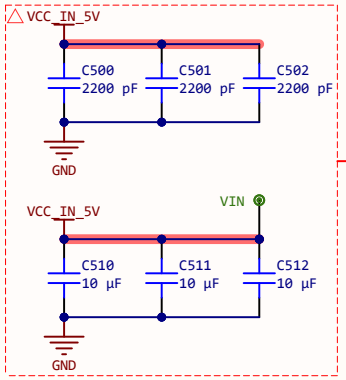
Decoupling capacitors

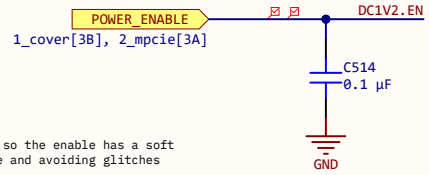


CC0201KRX7R8BB222
0201 (0603 Metric)
-55°C ~ 125°C
X7R ±10% 25V

GMC10X7R106K10NT
0603 (1608 Metric)
-55°C ~ 125°C
X7R ±10% 10V

One 2.2 nF plus one 10 uF per converter

Enable input

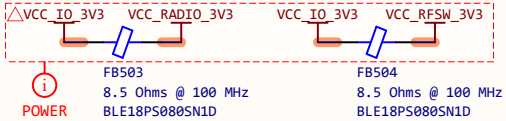


LPF so the enable has a soft rise and avoiding glitches

Power Good output

CAUTION! Power good signals are working in the 1V2 logic voltage.

Filtering the 3V3 rail



The TPS62912 PG pin is in high Z when V(FB) >= 95%, and driven low when V(FB) <= 90% . The open-drain pin requires a pullup. The PG signal is used for sequencing of multiple rails by connecting to the EN pin of other converters [1].

To ensure control of all digital IOs during the power-up/down of the SX1302 and avoid an inrush current, the 1.2 V rail shall be enabled before 3.3 V at start-up [2].

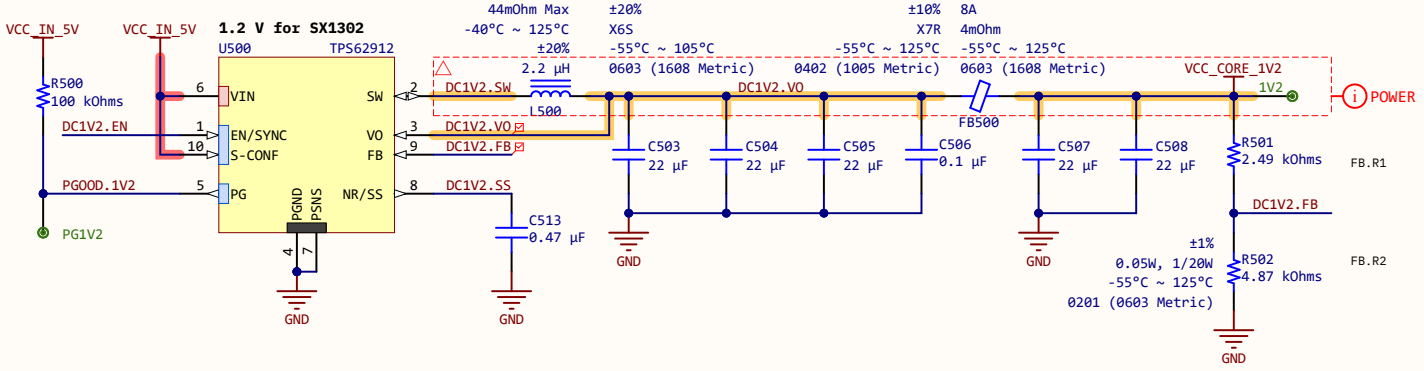
Low noise DC/DC converters

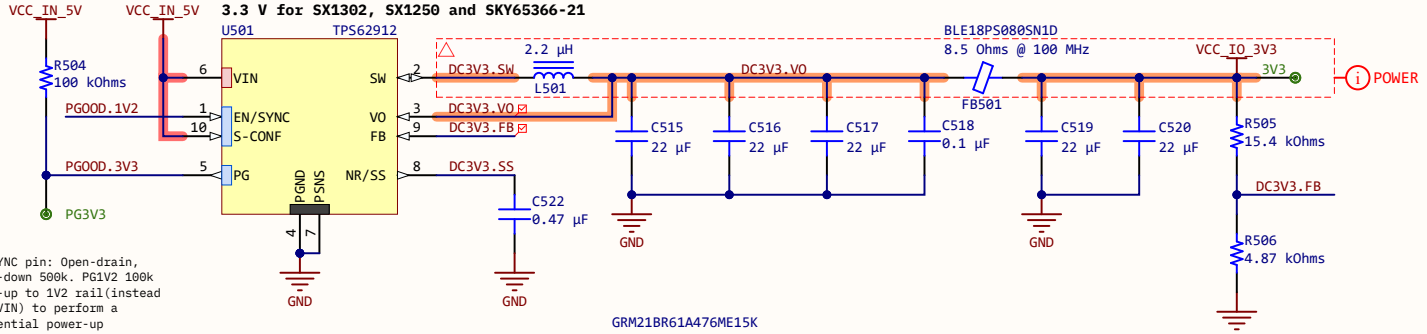
SRN4018-2R2M
Drum Core, Wirewound
Shielded
2.9 A
44mOhm Max
-40°C ~ 125°C

GRM188C80J226ME15D
6.3V
±20%
X6S
-55°C ~ 105°C

C0402C104K4RECAUTO
16V
±10%
X7R
-55°C ~ 125°C

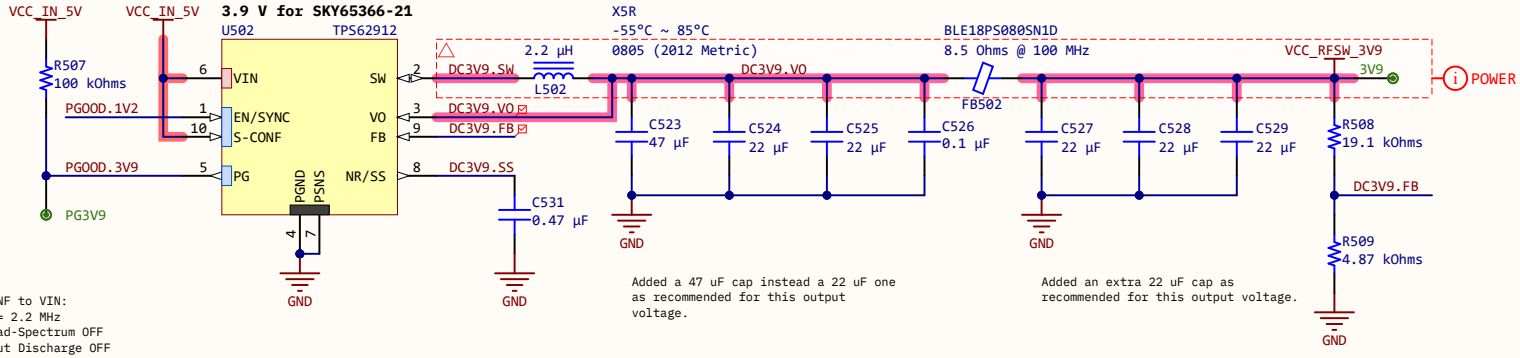
BLE18PS080SN1D
8.5 Ohms @ 100 MHz
8A
4mOhm
-55°C ~ 125°C





EN/SYNC pin: Open-drain, pull-down 500k. PG1V2 100k pull-up to 1V2 rail(instead of 5VIN) to perform a sequential power-up

GRM21BR61A476ME15K
10V
±20%
X5R
-55°C ~ 85°C



S-CONF to VIN:
Fsw = 2.2 MHz
Spread-Spectrum OFF
Output Discharge OFF
Sync OFF

Added a 47 uF cap instead a 22 uF one as recommended for this output voltage.

Added an extra 22 uF cap as recommended for this output voltage.

Notes:

Power supply based on low-noise DC/DC converters with sequential power-up.
[1] Texas Instruments Inc. TPS62912/3 datasheet, SLVSFP4B, 03-2021
[2] Semtech Inc. Errata Note Corecell PCB #e539v01e Reference Design, Rev 1.0, 03-2020

Title: *Power supply*		**Author:** Juan Del Pino Mena	**Pluton UPV**
Prj: Estigia comms payload - LoRa Gateway SoM		**Approved:** --	*Universitat Politècnica de València (UPV)*
Date: 2024-08-11 13:32:42	**Last modified:** 2024-08-11	**Prj. revision:** 0.4	*Camí de Vera, València*
Size: A4	Sheet 6 of 6	**Variant:** [No Variations]	*Spain*
File: 5_power.SchDoc		**Altium version:** 24.3.1.35	
		License: --	
		Git Hash: 41b6ea28c7eaa4a034106408df395347186357a6 [Locally Modified]	

PROJECT:

LoRa Comms Payload: Cubesat Carrier

PART OF THE MASTER'S THESIS:

"Development of a LoRa-based communications payload for CubeSat"

MASTER'S DEGREE IN ELECTRONIC SYSTEMS ENGINEERING
POLYTECHNIC UNIVERSITY OF VALENCIA
ACADEMIC COURSE 2023/2024

AUTHOR:

Juan Del Pino Mena

SUPERVISORS:

Jorge Daniel Martínez Pérez
DEPARTMENT OF ELECTRONIC ENGINEERING

Vicente Enrique Boria Esbert
DEPARTMENT OF COMMUNICATIONS

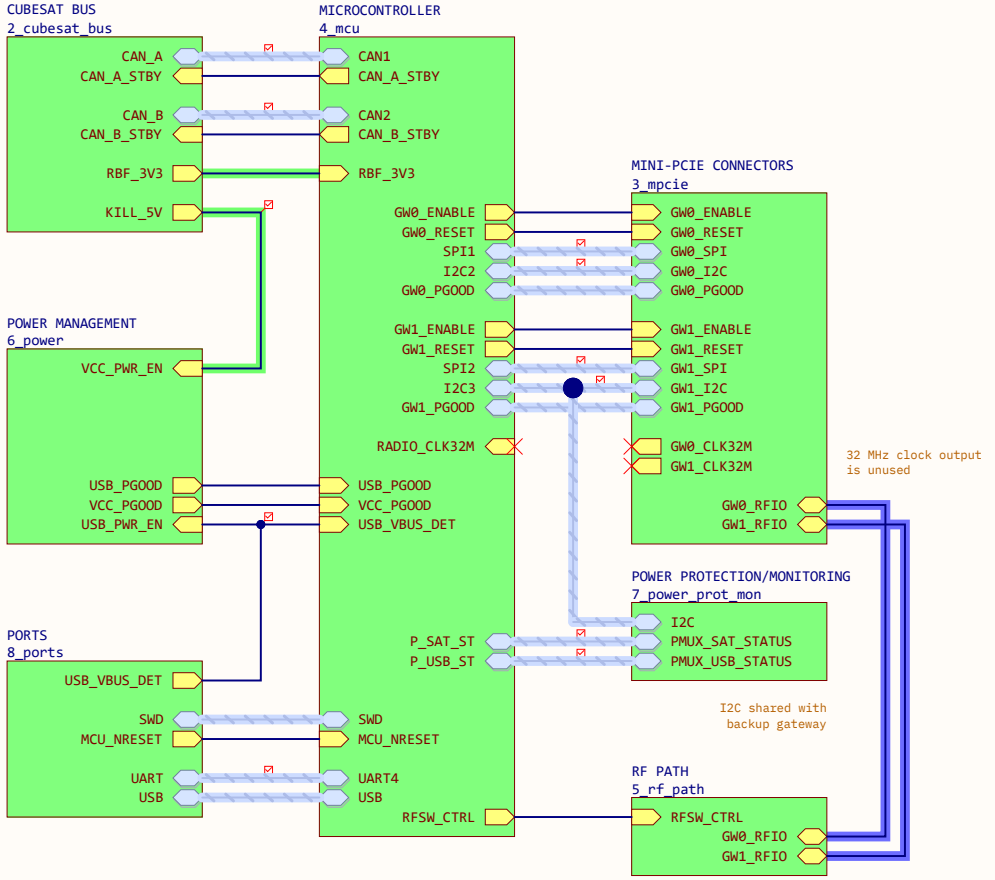
RBF is read by the MCU. Payload operation shall not start when RBF=0

When KILL=0 the payload enters shutdown mode, the power supply is disabled.

LOG100 LOGO Pluton
LOG102 LOGO Pluton isotype
LOG101 LOGO Pluton iso small
LOG103 LOGO AEA
LOG104 LOGO UPV
LOG105 LOGO MAG large

FID100 FID101 FID102

MH100 M3 MH101 M3 MH102 M3 MH103 M3



DEVELOPED IN PROUD COLLABORATION WITH:

UNIVERSITAT POLITÈCNICA DE VALÈNCIA
GENERACIÓN ESPONTÁNEA
TELECOM UPV VLC
DEPARTAMENTO DE INGENIERÍA ELECTRÓNICA
iTEAM Instituto de Telecomunicaciones y Aplicaciones Multimedia
MICROWAVE APPLICATIONS GROUP

Notes:

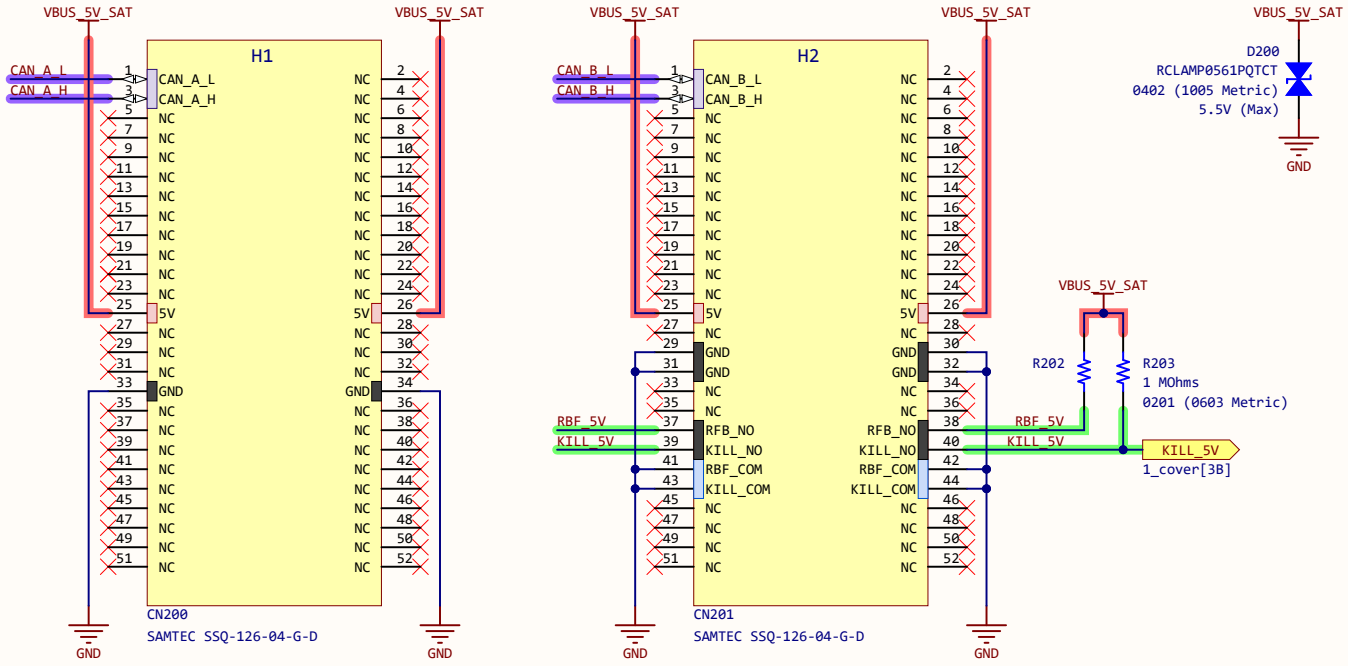
This board provides mechanical and electrical support for the LoRa gateway modules.
It consists of a PCI-104 board with two mPCIe sockets where the modules are inserted. The on-board microcontroller arbitrates these modules and acts as an intermediary between the modules and the rest of the satellite, with which it communicates using SpaceCAN.

Title:	*Cover and block diagram*
Prj:	Estigia Comms Payload - Cubesat carrier
Date:	2024-08-11 13:33:56
Last modified:	2024-08-11
Size:	A4
Sheet	1 of 8
File:	1_cover.SchDoc
Author:	Juan Del Pino Mena
Approved:	*
Prj. revision:	0.4
Variant:	[No Variations]
Altium version:	24.3.1.35
License:	--
Git Hash:	8e980d747e300d217102f3d6dbc5ec10b92cd1fb [Locally Modified]

Pluton UPV
Universitat Politècnica de València (UPV)
Camí de Vera, València
Spain

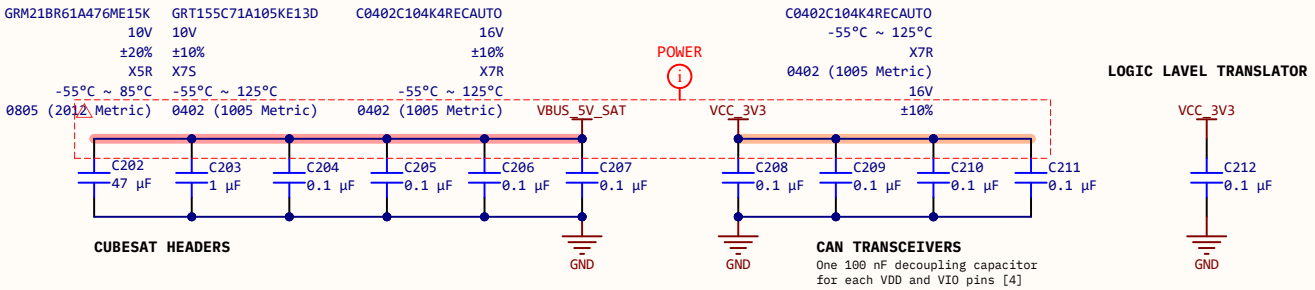
PLUTON

CubeSat Bus PCI-104 connectors

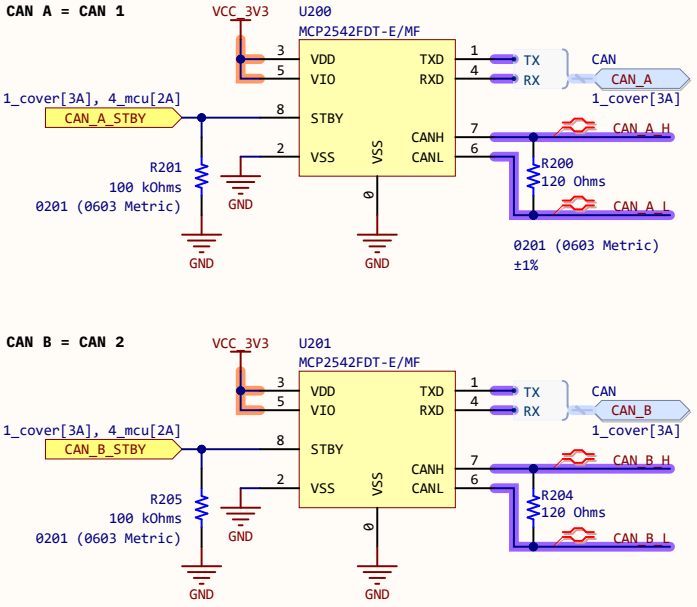


KILL: Global killswitch (NORMAL_OP=1, SHUTDOWN=0)
RBF: Remove Before Flight switch (NORMAL_OP=1, SHUTDOWN=0)
KILL_COM, RBF_COM: The respective switch common voltage

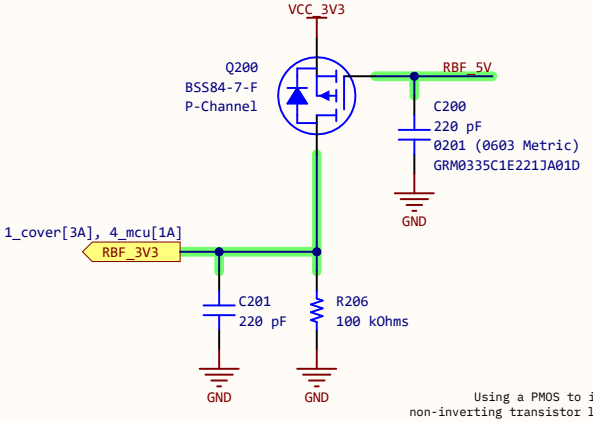
Decoupling capacitors



CAN transceivers



Unidirectional logic level translation



Using a PMOS to implement a non-inverting transistor logic. Gate input, to avoid loading the line.

Notes:

[1] LibreCube Board Spec. https://librecube.gitlab.io/standards/board_specification/ (04-2024)
[2] LibreCube SpaceCAN Spec. https://librecube.gitlab.io/standards/spacecan/ (04-2024)
[3] LibreCube PC104 pinout spreadsheet
https://docs.google.com/spreadsheets/d/1N1JiXR-5huo--XefjsvC9CI1hiS9xMNosTZhUcuxiQ0 (04-2024)
[4] Microchip Inc. MCP2542FD/4FD MCP2542WFD/4WFD datasheet, DS20005514C, 2020

Title: *CubeSat bus interface*		**Author:**	Juan Del Pino Mena
		Approved:	*
Prj: Estigia Comms Payload - Cubesat carrier		**Prj. revision:**	0.4
		Variant:	[No Variations]
Date: 2024-08-11 13:33:57	**Last modified:** 2024-08-11	**Altium version:**	24.3.1.35
Size: A4	Sheet 2 of 8	**License:**	--
File: 2_cubesat_bus.SchDoc		**Git Hash:**	8e980d747e300d217102f3d6dbc5ec10b92cd1fb [Locally Modified]

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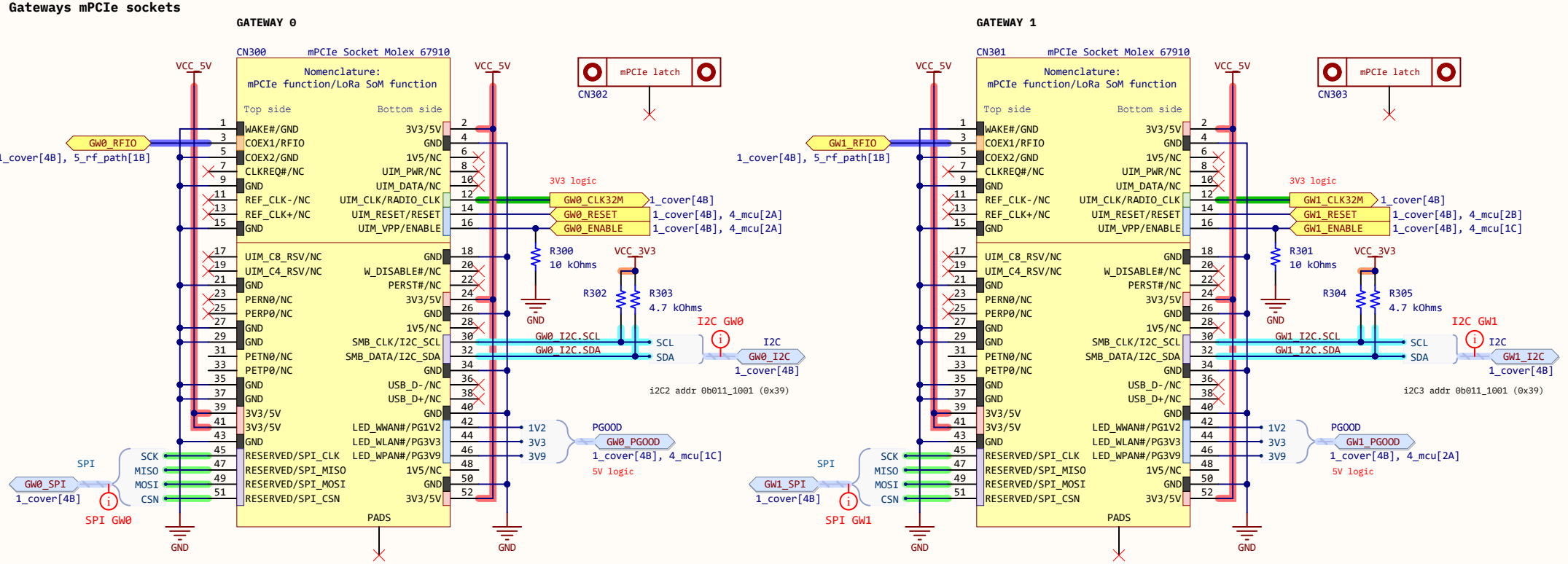
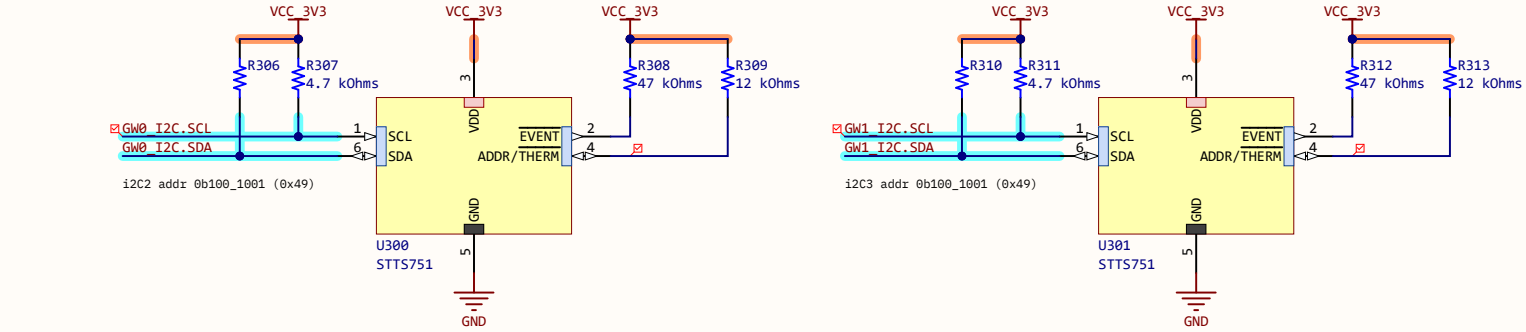
Camí de Vera, València
Spain

PLUTON

Gateways mPCIe sockets

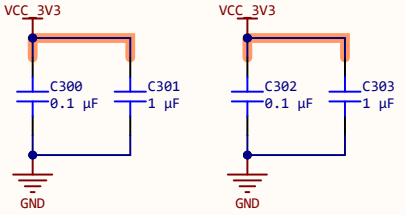


Temperature sensors



To be distributed throughout the board

Decoupling caps

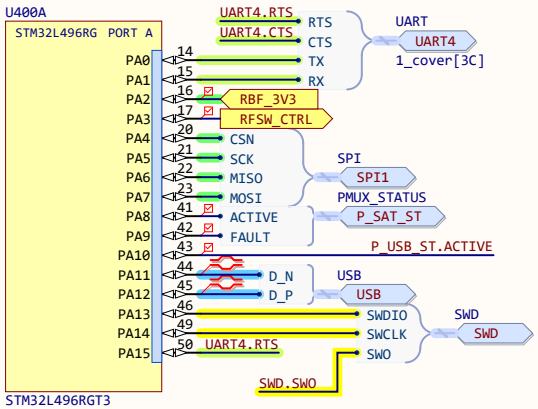


Notes:

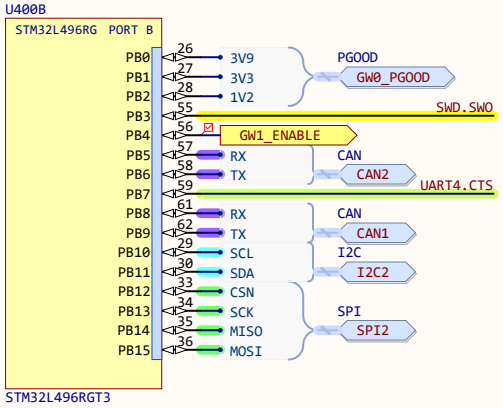
Title: *Mini-PCIe connectors*		**Author:** Juan Del Pino Mena	**Pluton UPV** *Universitat Politècnica de València (UPV) Camí de Vera, València Spain*
Prj: Estigia Comms Payload - Cubesat carrier		**Approved:** *	
		Prj. revision: 0.4	
		Variant: [No Variations]	
Date: 2024-08-11 13:33:57	**Last modified:** 2024-08-11	**Altium version:** 24.3.1.35	
Size: A4	Sheet 3 of 8	**License:** --	
File: 3_mpcie.SchDoc		**Git Hash:** 8e980d747e300d217102f3d6dbc5ec10b92cd1fb [Locally Modified]	

I/O Ports

PORT A



PORT B



CAN A = CAN 1
CAN B = CAN 2

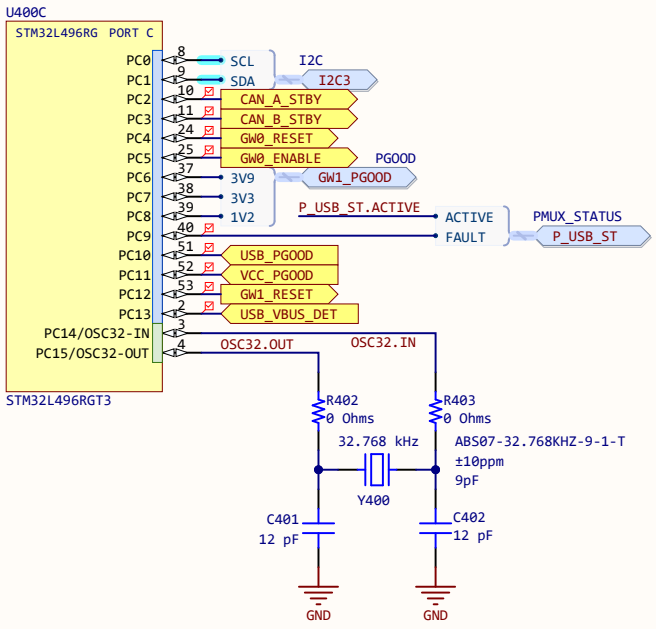
Altium warns about "net connection problems" when a bi-directional pin is connected to a input or output port. Ignore warning.

Many interfaces are defined and made available into the sheet symbol, so this sheet can be re-used easily between designs. Some peripherals are used both by the Carrier and EGSE, whereas others are only used in one of them.

PORT C

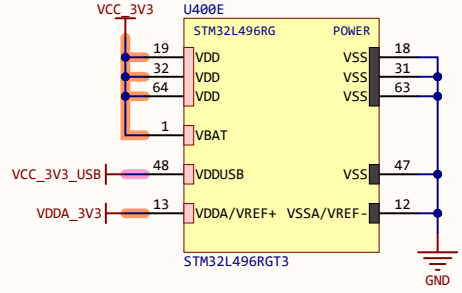
CAUTION! GW0 and GW1 can be enabled simultaneously but cannot be active at the same time!. See 5_rf_path

RESET signals are strongly pulled down in the mPCIe modules, but ENABLE signals are weakly pulled low.



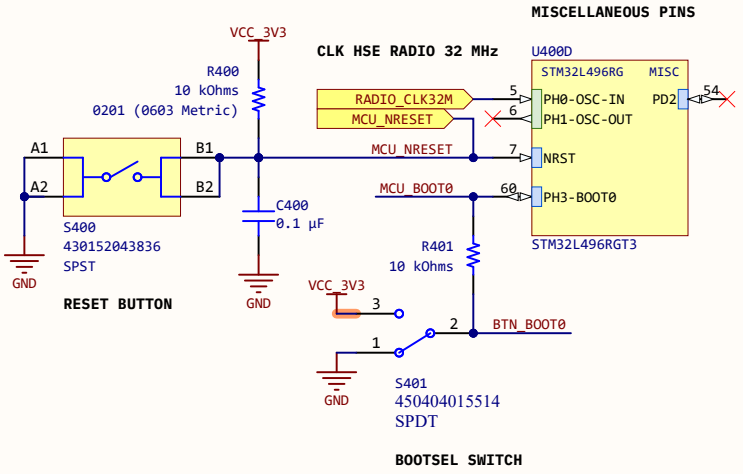
CLK LSE 32.768 kHz
This MCU should use the MSI clock

POWER PINS

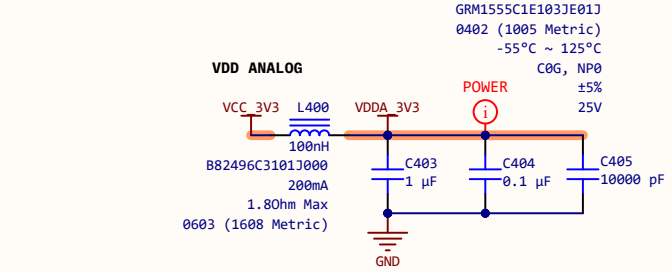


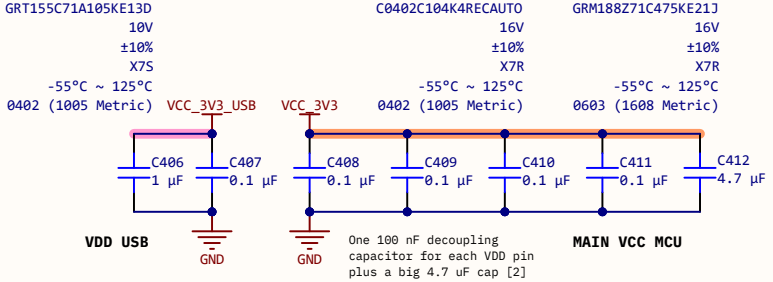
Reset button and boot selection dip switch

MISCELLANEOUS PINS



Filtering & decoupling





Notes:

[1] STMicroelectronics Inc. STM32L496xx Datasheet, DS11585, Rev 17, 11-2022
[2] STMicroelectronics Inc. Getting started with STM32L4/L4+ hardware dev., AN4555, Rev 9, 11-2022
[3] STMicroelectronics Inc. Oscillator design guide for STM32 MCUs, AN2687, Rev 19, 04-2023

Title:	*Microcontroller*
Prj:	Estigia Comms Payload - Cubesat carrier
Date:	2024-08-11 13:33:57
Last modified:	2024-08-11
Size:	A4
Sheet	4 of 8
File:	4_mcu.SchDoc
Author:	Juan Del Pino Mena
Approved:	*
Prj. revision:	0.4
Variant:	[No Variations]
Altium version:	24.3.1.35
License:	--
Git Hash:	8e980d747e300d217102f3d6dbc5ec10b92cd1fb [Locally Modified]

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Camí de Vera, València
Spain

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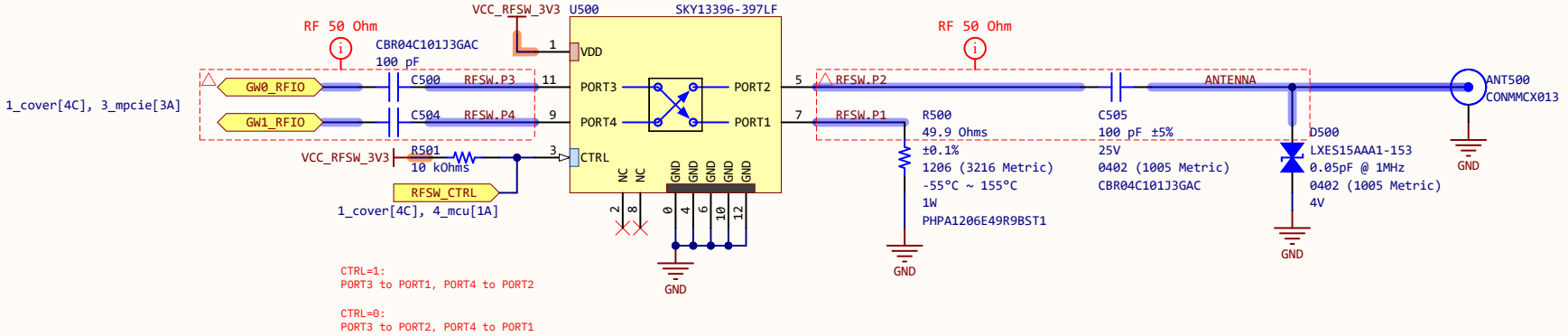
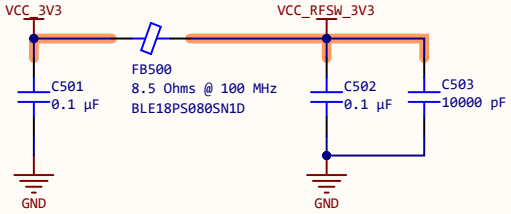
RF connectors, switch and load



Decoupling capacitors and supply filtering

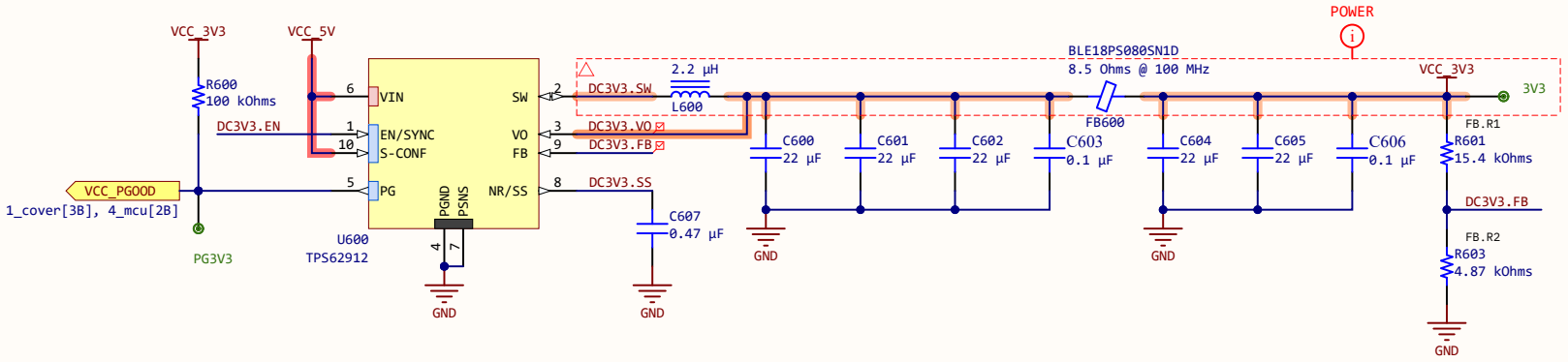


Notes:

Selects which module has access to the antenna, and connects the other one to a 50-ohm load.
[1] Skyworks Inc. SKY13396-397LF 400 MHz RO 3000 MHz DPDT Switch Module, 201475H, 7-2017

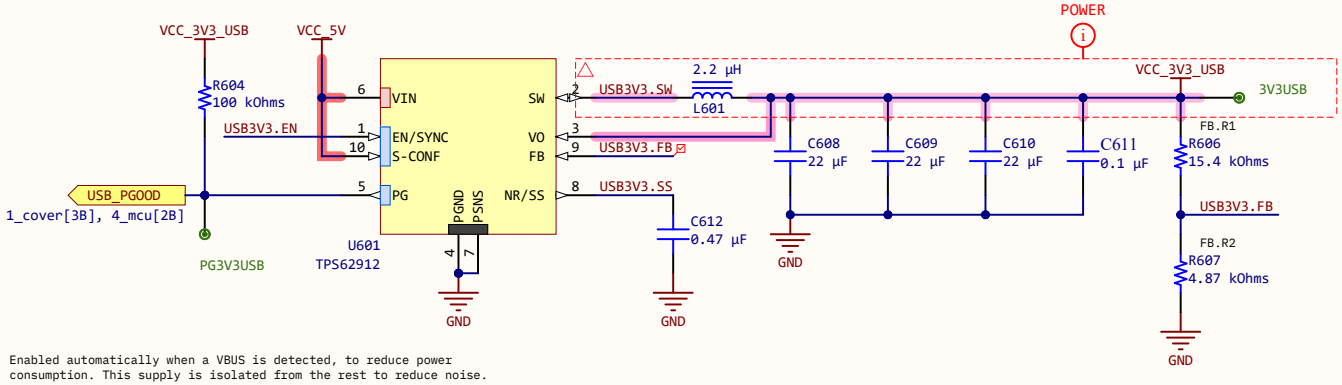
Title: *RF path selection*		**Author:** Juan Del Pino Mena	**Pluton UPV**
Prj: Estigia Comms Payload - Cubesat carrier		**Approved:** *	*Universitat Politècnica de València (UPV)*
		Prj. revision: 0.4	*Camí de Vera, València*
		Variant: [No Variations]	*Spain*
Date: 2024-08-11 13:33:58	**Last modified:** 2024-08-11	**Altium version:** 24.3.1.35	
Size: A4	Sheet 5 of 8	**License:** --	
File: 5_rf_path.SchDoc		**Git Hash:** 8e980d747e300d217102f3d6dbc5ec10b92cd1fb [Locally Modified]	

Low noise DC/DC converter - 3.3 V for MCU, CAN



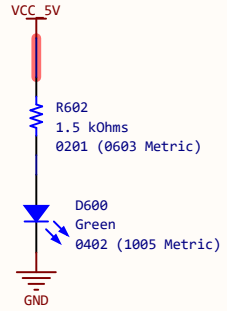
Main power supply

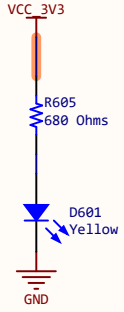
DC/DC converter - dirty 3.3 V for the MCU-USB peripheral



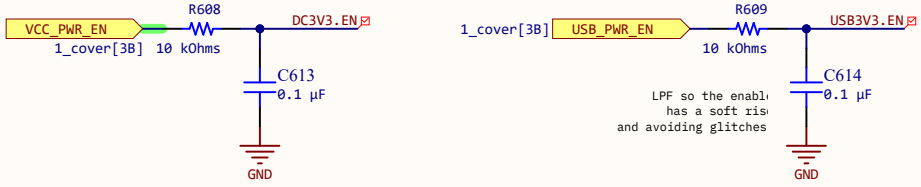
Enabled automatically when a VBUS is detected, to reduce power consumption. This supply is isolated from the rest to reduce noise.

Power LED indicator



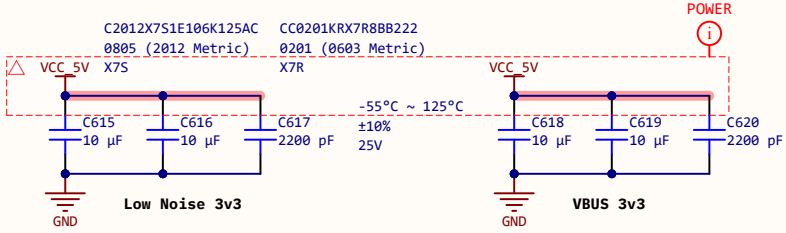


Enable input



Power supply tied to the global killswitch. When KILL=0, the payload enters shutdown mode: the power supply is disabled and all the components in the board are shut down.

Decoupling capacitors



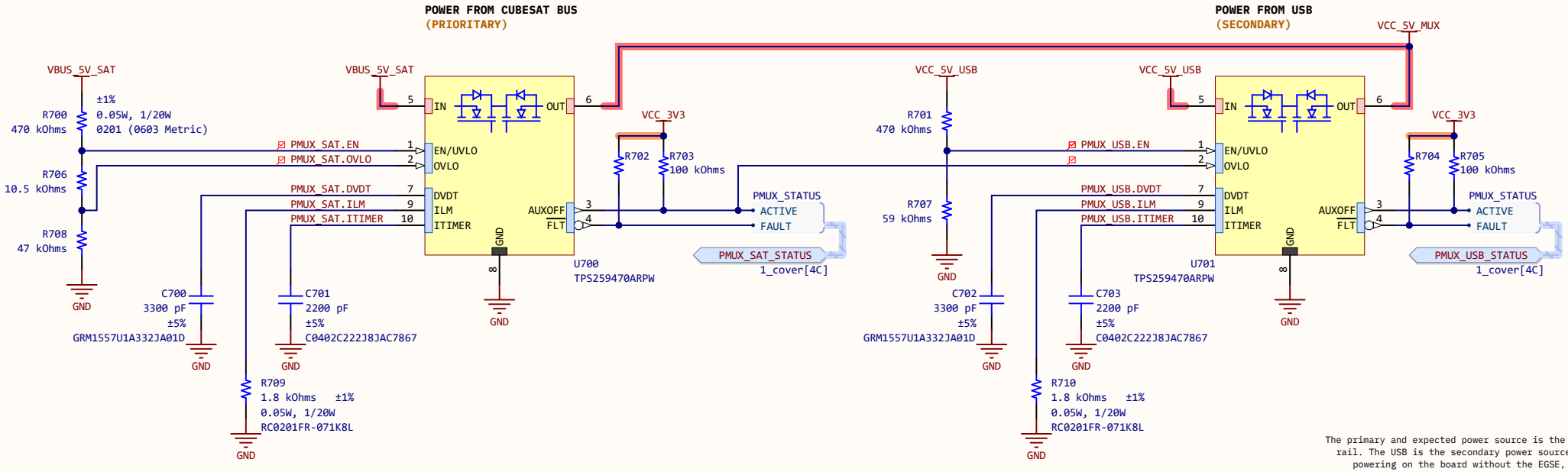
Notes:

[1] Texas Instruments Inc. TPS62912/3 datasheet, SLVSFP4B, 03-2021
[2] Texas Instruments Inc. INA232 datasheet, SBOSAA2, 12-2022

Title: *Power management*		**Author:** Juan Del Pino Mena	**Pluton UPV**
Prj: Estigia Comms Payload - Cubesat carrier		**Approved:** *	*Universitat Politècnica de València (UPV)*
		Prj. revision: 0.4	*Camí de Vera, València*
Date: 2024-08-11 13:33:58	**Last modified:** 2024-08-11	**Variant:** [No Variations]	*Spain*
Size: A4	Sheet 6 of 8	**Altium version:** 24.3.1.35	
File: 6_power.SchDoc		**License:** --	
		Git Hash: 8e980d747e300d217102f3d6dbc5ec10b92cd1fb [Locally Modified]	

eFuse and power multiplexor

Priority power muxing, reverse current/polarity protection,
over-current, over-voltage protection.



The primary and expected power source is the Cubesat bus rail. The USB is the secondary power source and allows powering on the board without the EGSE, for example

Voltage, current and power monitor

R_SHUNT selection (early power budget estimation)

Carrier power consumption: 0.33 W (max)
LoRa SoM power consumption: 4.62 W (tx); 0.58 W (rx)

Expected total power consumption: [0.9 W, 5 W]
Thus, at V_cc = 5 V : current consumption: [0.18 A, 1 A]

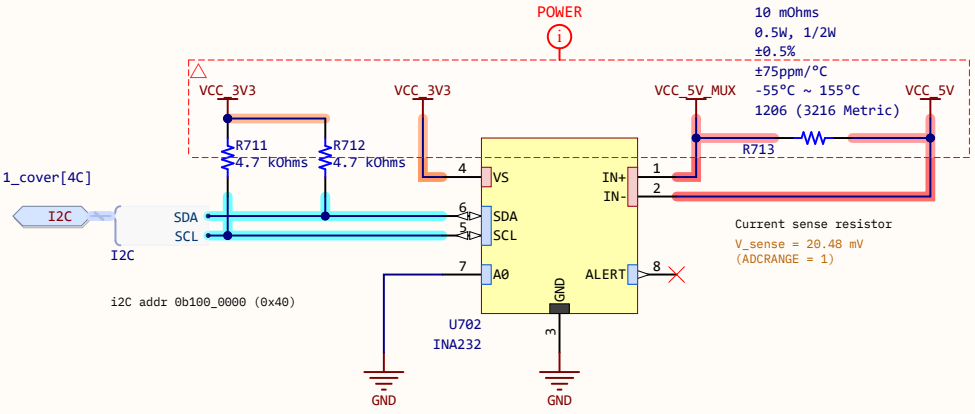
Account for an instantaneous peak current consumption of double the maximum: I_peak = 2 A

For minimum voltage drop, V_sense = 20.48 mV (INA232 cfg)

R_shunt < V_sense / I_peak = 10.24 mOhm

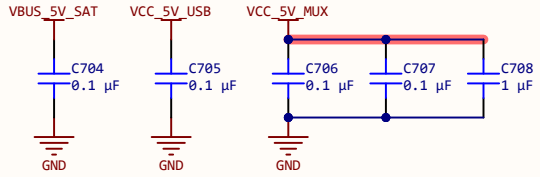
Power dissipated on R_shunt: 42 mW

R_shunt = 10 mOhm, tolerance <=0.5 %, power >= 0.1 W

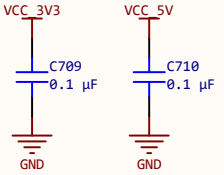


Decoupling capacitors

TPS259470A



INA232



Notes:

Title:		**Author:** Juan Del Pino Mena
Prj: Estigia Comms Payload - Cubesat carrier		**Approved:** *
		Prj. revision: 0.4
		Variant: [No Variations]
Date: 2024-08-11 13:33:58	**Last modified:** 2024-08-11	**Altium version:** 24.3.1.35
Size: A4	Sheet 7 of 8	**License:** --
File: 7_power_prot_mon.SchDoc		**Git Hash:** 8e980d747e300d217102f3d6dbc5ec10b92cd1fb [Locally Modified]

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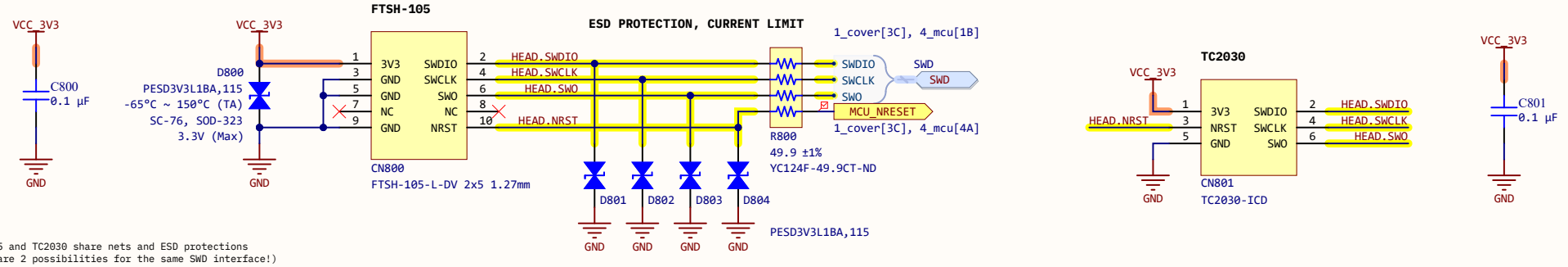
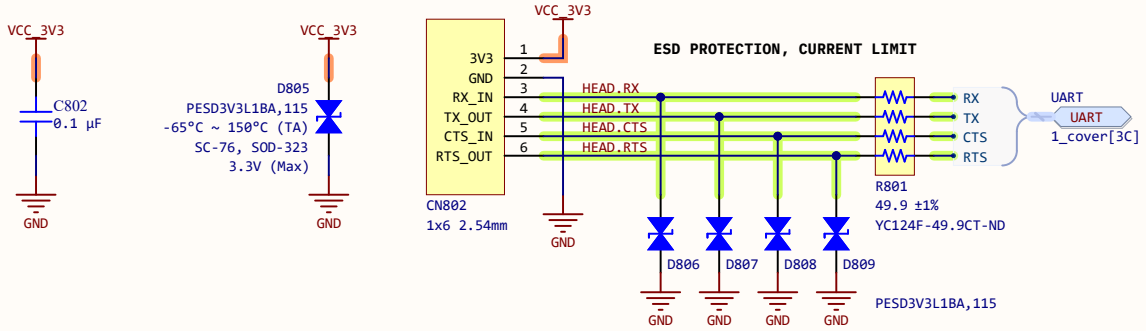
SWD



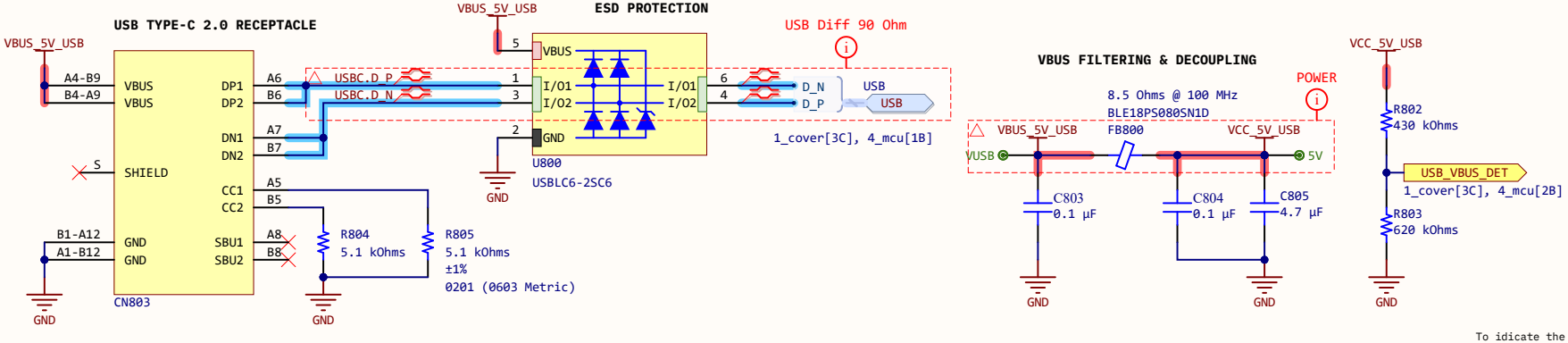
FTSH-105 and TC2030 share nets and ESD protections
(there are 2 possibilities for the same SWD interface!)

UART



CAUTION: UART SIGNALS ALREADY CROSSED!
Compatible serial adapter pinout:
1:3V3, 2:GND, 3:TXD, 4:RXD, 5:RTS, 6:CTS

USB



USB-C 2.0 interface. Pull down resistors on CC pins make the connector behave electrically as an USB type B, device only, which sinks up to 15 W (5V, 3A max).

This USB can be used for both power and comms

To idicate the microcontroller when to enable the USB peripheral

Notes:

Miscellaneous connectors: Debug, UART, USB. With ESD protections.
[1] STMicroelectronics Inc. STLINK-V3MINIE debugger/programmer User Manual, UM2910, Rev 3, 04-2024
[2] Tag-connect, ARM-CTX (20-pin ARM to TC2030) adapter for SWD datasheet.
[3] Tag-connect, TC2030-IDC datasheet, Rev B, 05-2019
[4] STMicroelectronics Inc. AN4879, Rev 6,

Title: *Miscellaneous ports*		**Author:**	Juan Del Pino Mena
Prj: Estigia Comms Payload - Cubesat carrier		**Approved:**	*
		Prj. revision:	0.4
		Variant:	[No Variations]
Date: 2024-08-11 13:33:59	**Last modified:** 2024-08-11	**Altium version:**	24.3.1.35
Size: A4	Sheet 8 of 8	**License:**	--
File: 8_ports.SchDoc		**Git Hash:**	8e980d747e300d217102f3d6dbc5ec10b92cd1fb [Locally Modified]

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PROJECT:

LoRa Comms Payload: Electrical Ground Support Equipment

PART OF THE MASTER'S THESIS:

"Development of a LoRa-based communications payload for CubeSat"

MASTER'S DEGREE IN ELECTRONIC SYSTEMS ENGINEERING
POLYTECHNIC UNIVERSITY OF VALENCIA
ACADEMIC COURSE 2023/2024

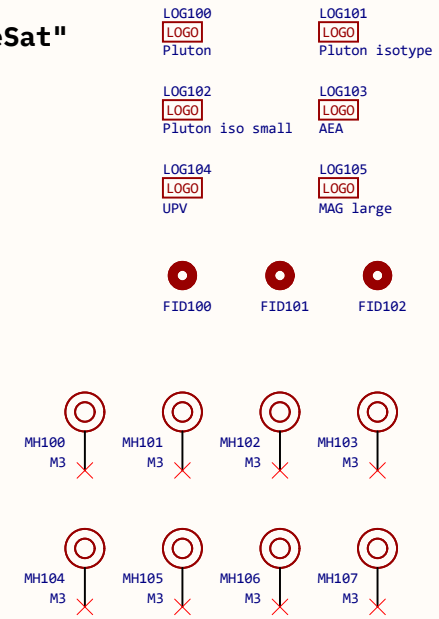
AUTHOR:

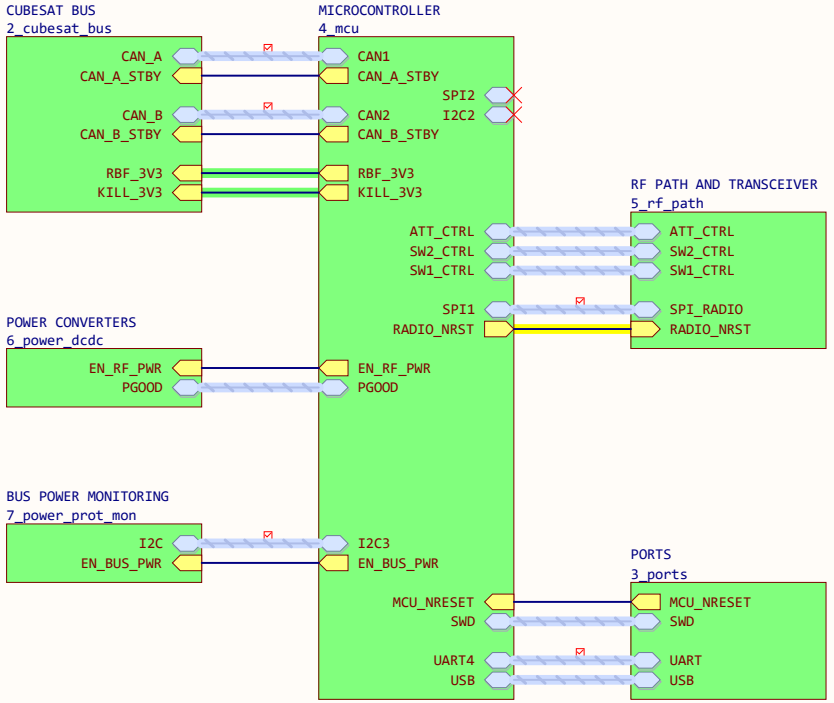
Juan Del Pino Mena

SUPERVISORS:

Jorge Daniel Martínez Pérez
DEPARTMENT OF ELECTRONIC ENGINEERING

Vicente Enrique Boria Esbert
DEPARTMENT OF COMMUNICATIONS





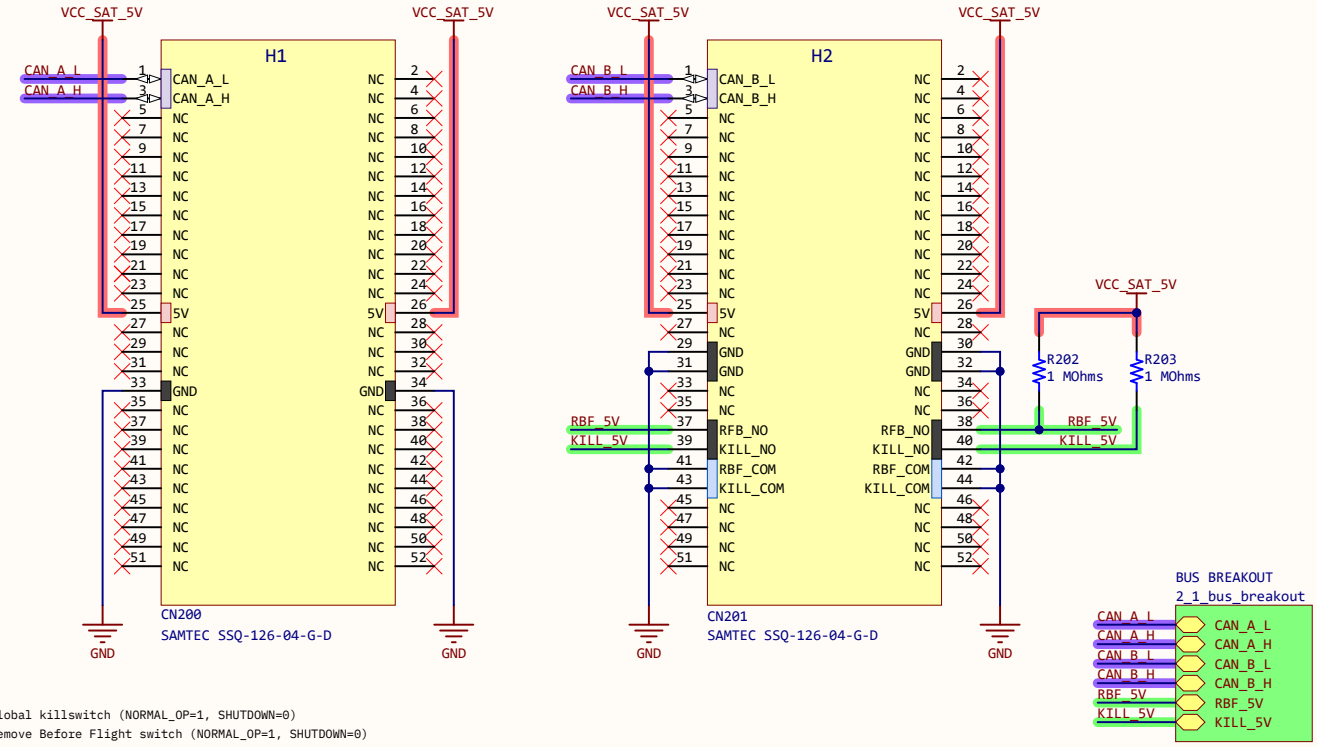
DEVELOPED IN PROUD COLLABORATION WITH:

Notes:

This project consists of an Electrical Ground Support Equipment board. It is used to program, power and test the payload. It contains a microcontroller symmetrical to the carrier, a PCI-104 bus interface to emulate communication with an OBC, and an RF sink with a LoRa transceiver and variable attenuators, simulating propagation losses.

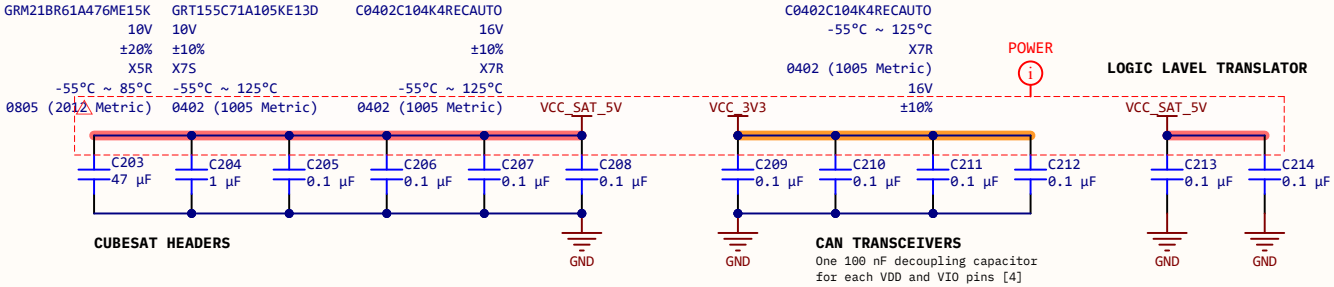
Title: *Cover and block diagram*		**Author:** Juan Del Pino Mena	**Pluton UPV** *Universitat Politècnica de València (UPV) Camí de Vera, València Spain*
Prj: Estigia Comms Payload - EGSE		**Approved:** *	
		Prj. revision: 0.4	
Date: 03/09/2024 19:56:42	**Last modified:** 03/09/2024	**Variant:** [No Variations]	
Size: A4	Sheet 1 of 12	**Altium version:** 24.3.1.35	
File: 1_cover.SchDoc		**License:** --	
		Git Hash:	

CubeSat Bus PCI-104 connectors

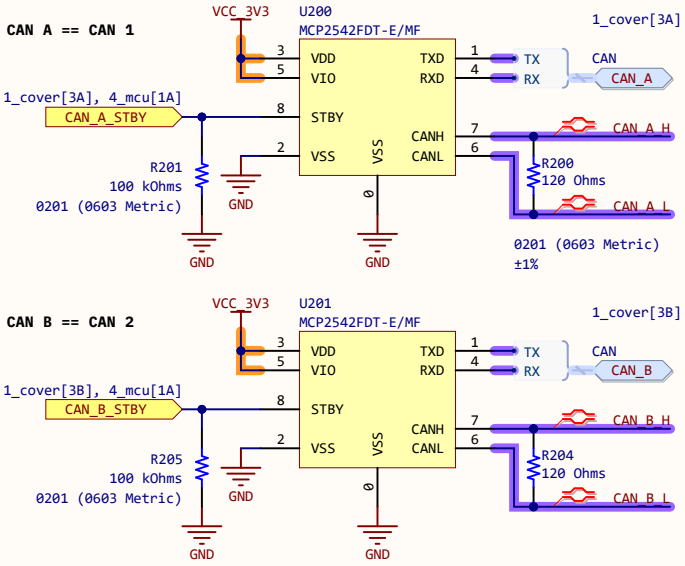


KILL: Global killswitch (NORMAL_OP=1, SHUTDOWN=0)
RBF: Remove Before Flight switch (NORMAL_OP=1, SHUTDOWN=0)
KILL_COM, RBF_COM: The respective switch common voltage

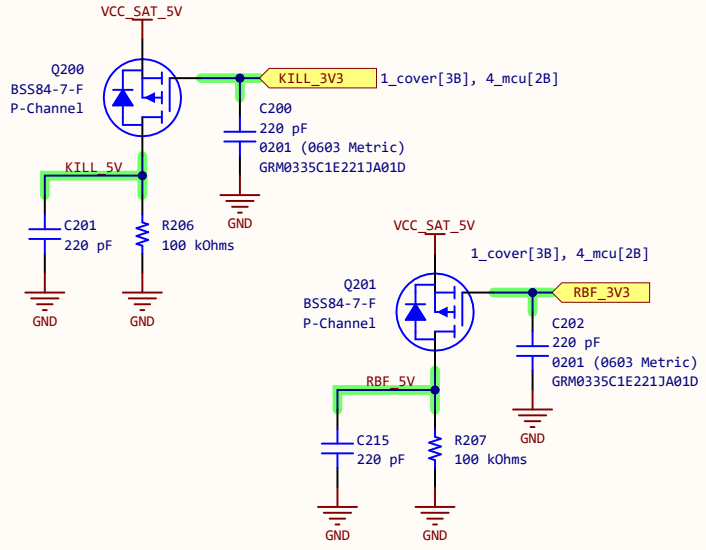
Decoupling capacitors



CAN transceivers



Logic level translator



Notes:

[1] LibreCube Board Spec. https://librecube.gitlab.io/standards/board_specification/ (04-2024)
[2] LibreCube SpaceCAN Spec. https://librecube.gitlab.io/standards/spacecan/ (04-2024)
[3] LibreCube PC104 pinout spreadsheet
https://docs.google.com/spreadsheets/d/1N1JiXR-5huo--XefjsvC9CI1hiS9xMNosTZhUcuxiQ0 (04-2024)
[4] Microchip Inc. MCP2542FD/4FD MCP2542WFD/4WFD datasheet, DS20005514C, 2020

Title:	*CubeSat Bus interface*	**Author:**	Juan Del Pino Mena
		Approved:	*
Prj:	Estigia Comms Payload - EGSE	**Prj. revision:**	0.4
		Variant:	[No Variations]
Date:	03/09/2024 19:56:43	**Last modified:**	11/08/2024
Size:	A4	Sheet 2 of 12	**Altium version:** 24.3.1.35
File:	2_cubesat_bus.SchDoc	**License:**	--
		Git Hash:	

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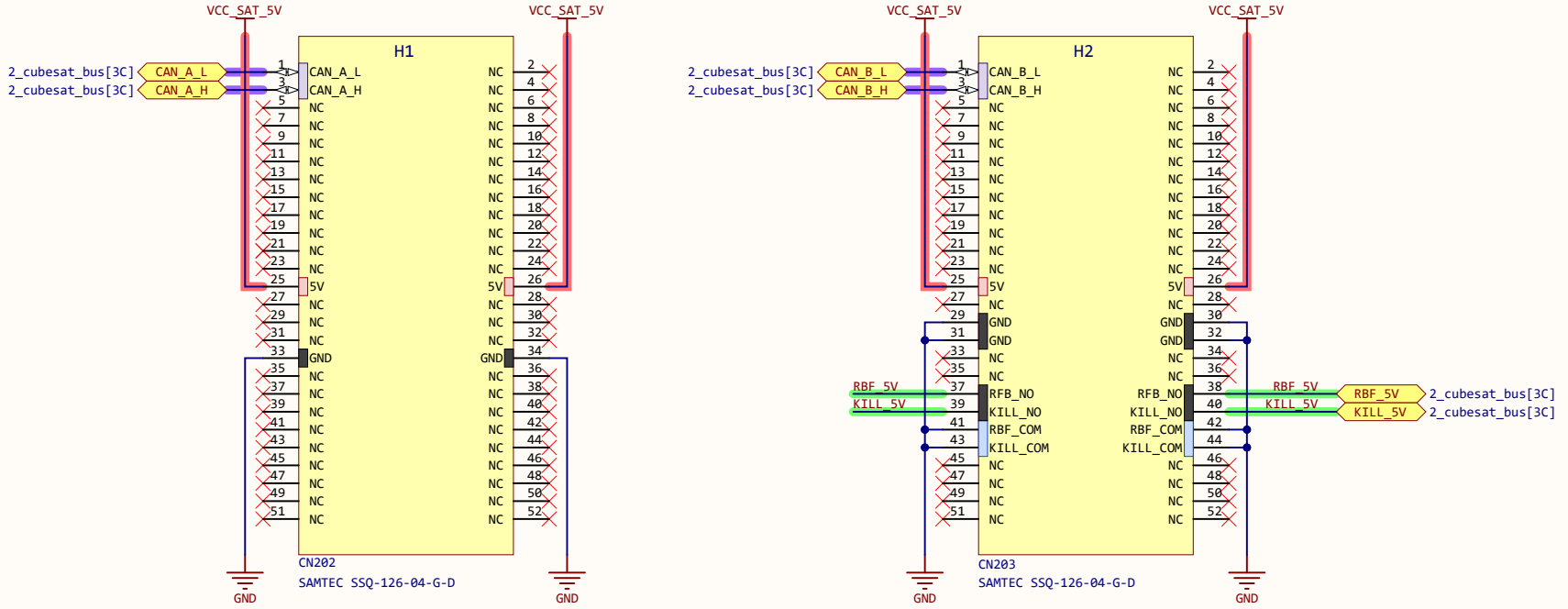
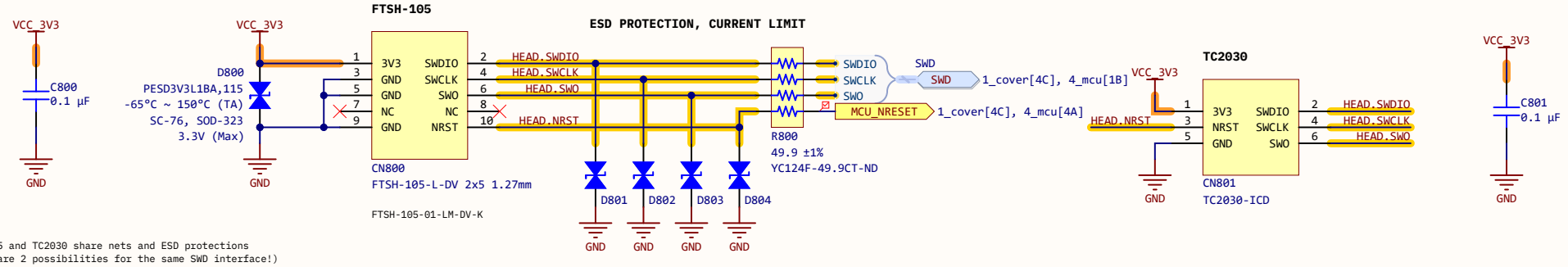


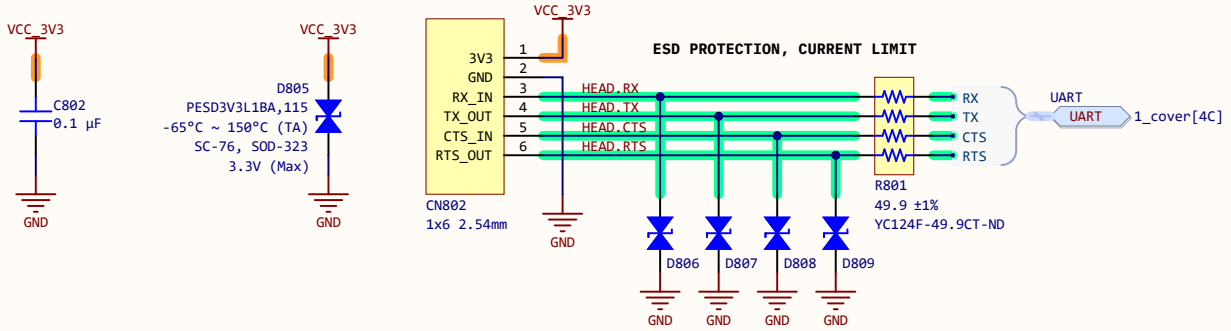
Notes:	**Title:** ***CubeSat Bus Breakout***	**Author:** Juan Del Pino Mena	**Pluton UPV** *Universitat Politècnica de València (UPV) Camí de Vera, València Spain*
	Prj: Estigia Comms Payload - EGSE	**Approved:** *	
		Prj. revision: 0.4	
		Variant: [No Variations]	
	Date: 03/09/2024 19:56:44 **Last modified:** 11/08/2024	**Altium version:** 24.3.1.35	
	Size: A4 Sheet 3 of 12	**License:** --	
	File: 2_1_bus_breakout.SchDoc	**Git Hash:**	

SWD



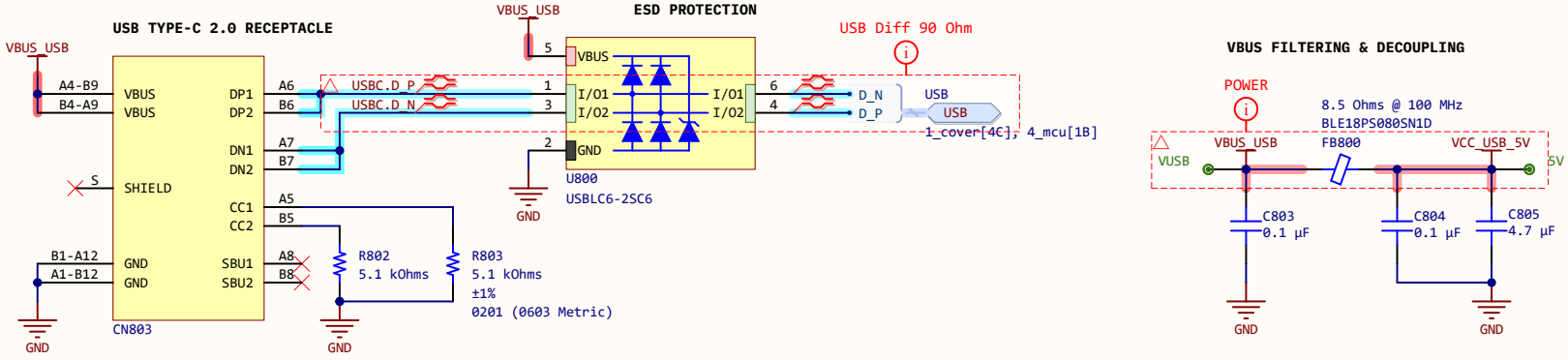
FTSH-105 and TC2030 share nets and ESD protections
(there are 2 possibilities for the same SWD interface!)

UART



CAUTION: UART SIGNALS ALREADY CROSSED!
Compatible serial adapter pinout:
1:3V3, 2:GND, 3:TXD, 4:RXD, 5:RTS, 6:CTS

USB



USB-C 2.0 interface. Pull down resistors on CC pins make the connector behave electrically as an USB type B, device only, which sinks up to 15 W (5V, 3A max).

This USB is used for both power and comms

Notes:

Miscellaneous connectors: Debug, UART, USB. With ESD protections.
[1] STMicroelectronics Inc. STLINK-V3MINIE debugger/programmer User Manual, UM2910, Rev 3, 04-2024
[2] Tag-connect, ARM-CTX (20-pin ARM to TC2030) adapter for SWD datasheet.
[3] Tag-connect, TC2030-IDC datasheet, Rev B, 05-2019
[4] STMicroelectronics Inc. AN4879, Rev 6,

Title: *Ports*		**Author:** Juan Del Pino Mena	
		Approved: *	
Prj: Estigia Comms Payload - EGSE		**Prj. revision:** 0.4	
		Variant: [No Variations]	
Date: 03/09/2024 19:56:44	**Last modified:** 02/09/2024	**Altium version:** 24.3.1.35	
Size: A4	Sheet 4 of 12	**License:** --	
File: 3_ports.SchDoc		**Git Hash:**	

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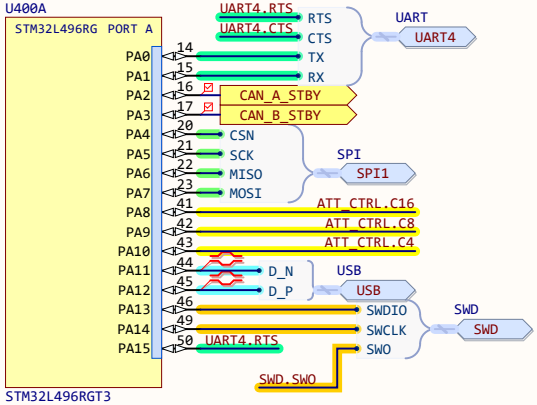
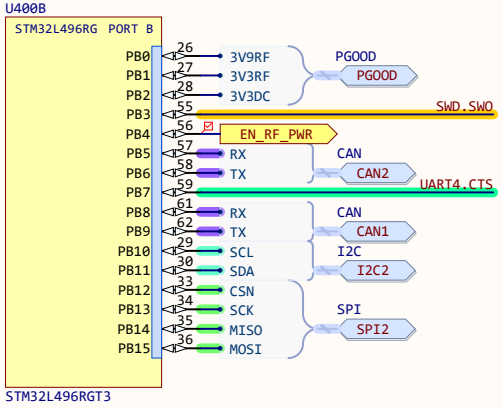
I/O Ports

PORT A



PORT B

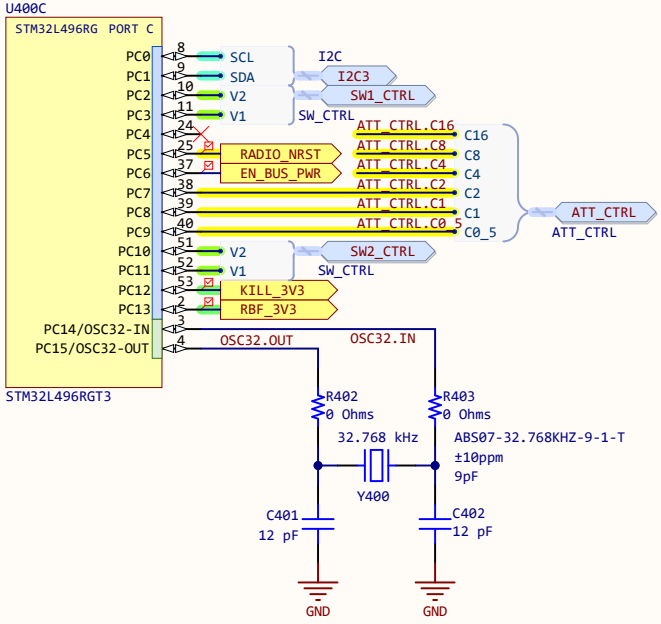


CAN A = CAN 1
CAN B = CAN 2

Altium warns about "net connection problems" when a bi-directional pin is connected to a input or output port. Ignore warning.

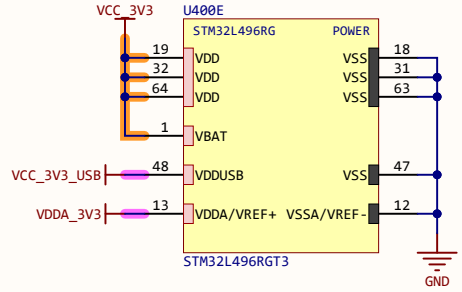
Many interfaces are defined and made available into the sheet symbol, so this sheet can be re-used easily between designs. Some peripherals are used both by the Carrier and EGSE, whereas others are only used in one of them.

PORT C

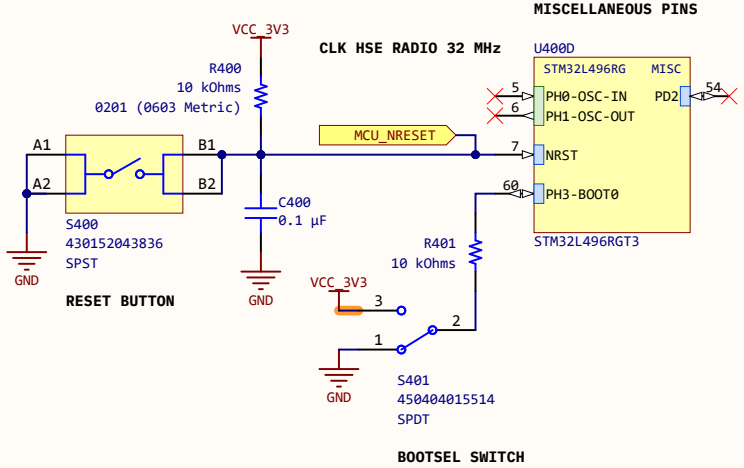


CLK LSE 32.768 kHz
This MCU should use the MSI clock

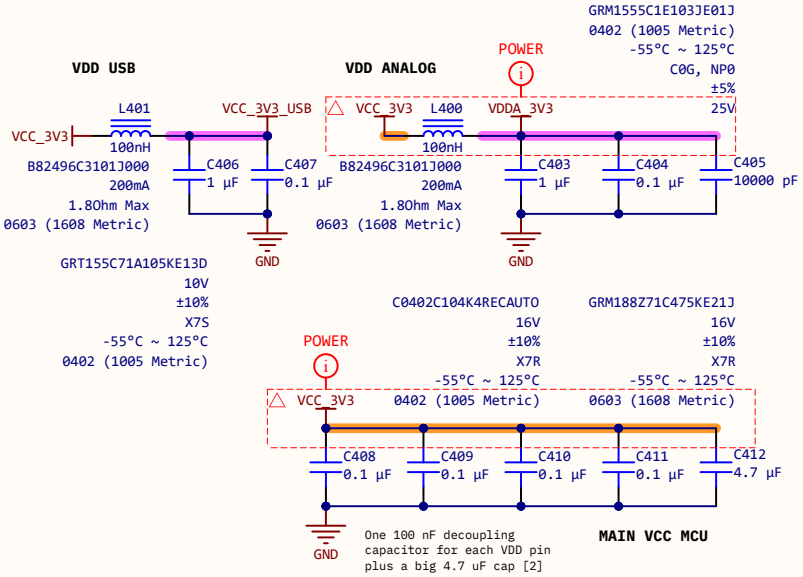
POWER PINS



Reset button and boot selection dip switch



Filtering & decoupling



Notes:

[1] STMicroelectronics Inc. STM32L496xx Datasheet, DS11585, Rev 17, 11-2022
[2] STMicroelectronics Inc. Getting started with STM32L4/L4+ hardware dev., AN4555, Rev 9, 11-2022
[3] STMicroelectronics Inc. Oscillator design guide for STM32 MCUs, AN2687, Rev 19, 04-2023

Title:	*Microcontroller*
Prj:	Estigia Comms Payload - EGSE
Date:	03/09/2024 19:56:44
Last modified:	03/09/2024
Size:	A4
Sheet	5 of 12
File:	4_mcu.SchDoc
Author:	Juan Del Pino Mena
Approved:	*
Prj. revision:	0.4
Variant:	[No Variations]
Altium version:	24.3.1.35
License:	--
Git Hash:	

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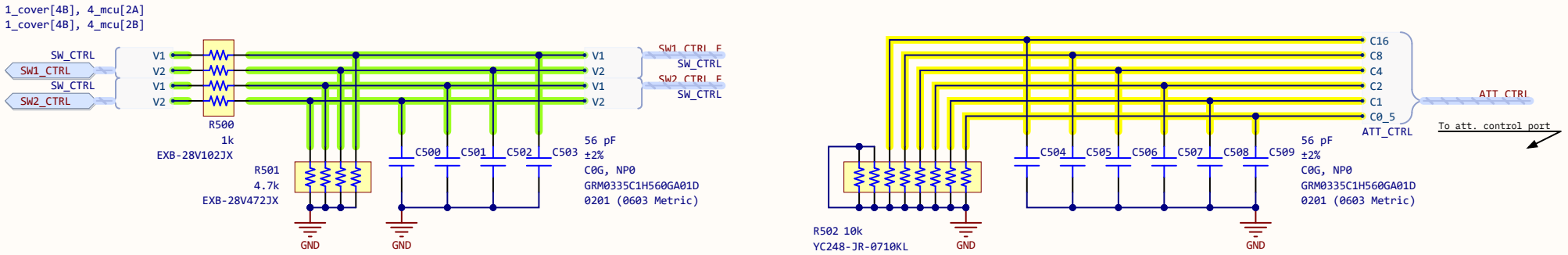
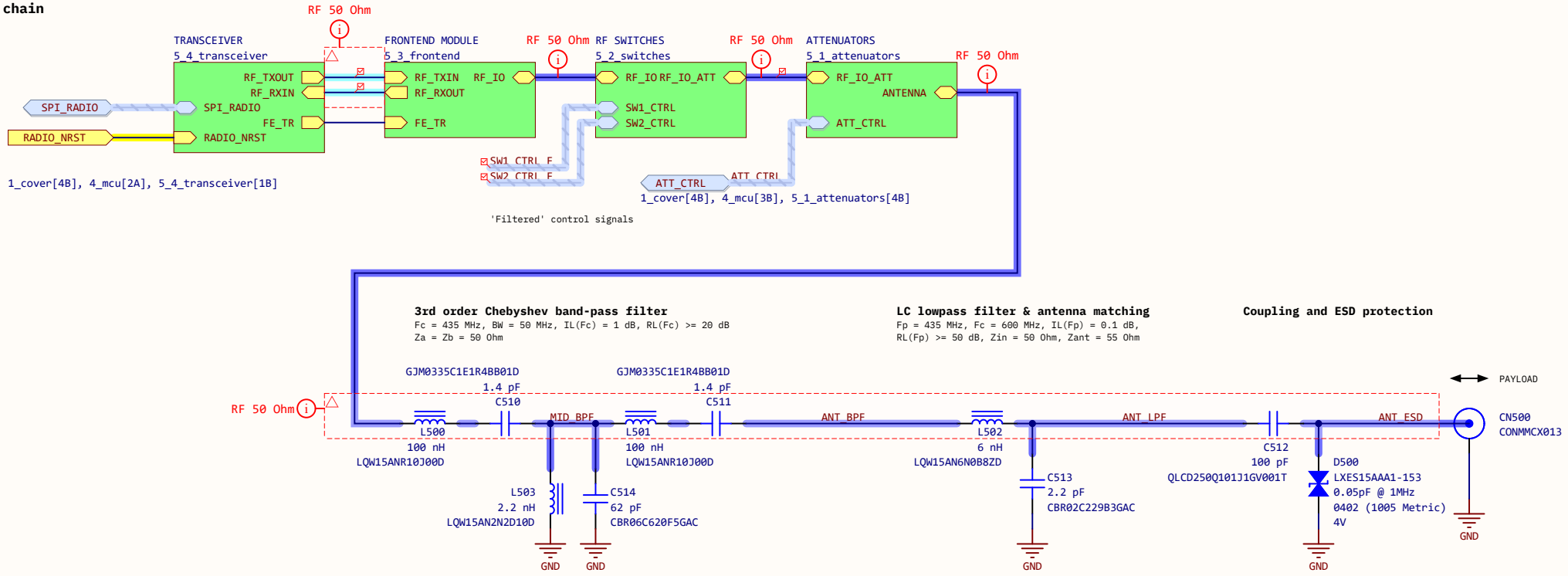
Filtering of control signals



Voltage divider needed because SKY13373-460LF
logic only supports 1.6 to 3.0 V

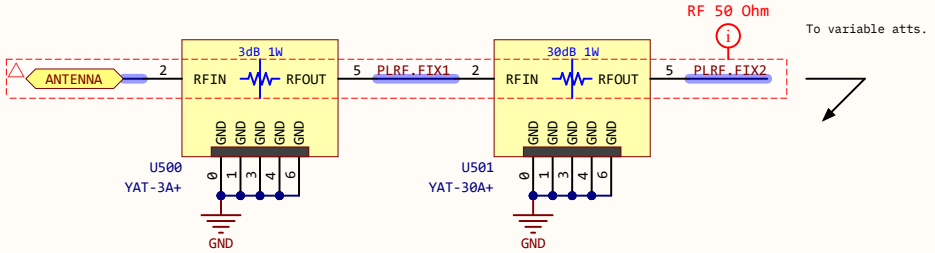
RF chain



Notes:	**Title:** *RF path and LoRa transceiver*	**Author:** Juan Del Pino Mena	**Pluton UPV**
		Approved: *	*Universitat Politècnica de València (UPV)*
	Prj: Estigia Comms Payload - EGSE	**Prj. revision:** 0.4	*Camí de Vera, València*
		Variant: [No Variations]	*Spain*
	Date: 03/09/2024 19:56:44 **Last modified:** 02/09/2024	**Altium version:** 24.3.1.35	
	Size: A4 Sheet 6 of 12	**License:** --	
	File: 5_rf_path.SchDoc	**Git Hash:**	

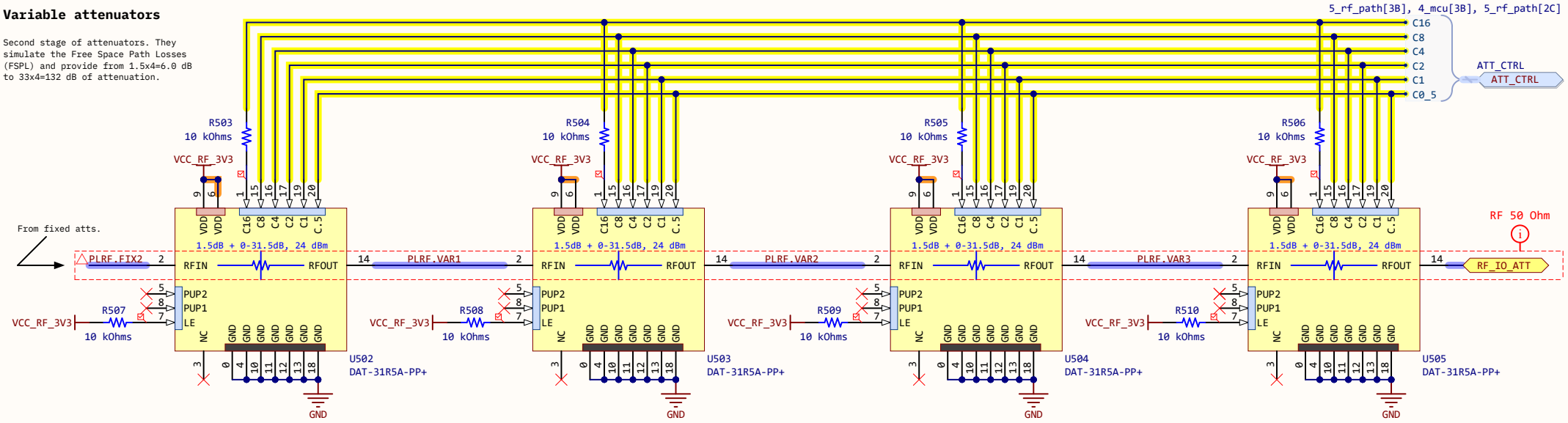
Fixed attenuators

First stage of attenuators. They dissipate the most power in the chain (up to 2W), and protect the RF ICs limiting the input RF power to a safe level.



Variable attenuators

Second stage of attenuators. They simulate the Free Space Path Losses (FSPL) and provide from 1.5x4=6.0 dB to 33x4=132 dB of attenuation.



Decoupling caps

Notes:

[1] Mini-Circuits Inc. YAT-30A+ datasheet, ECO-011434, REV. A, 01-2022
[2] Mini-Circuits Inc. YAT-3A+ datasheet, ECO-011434, REV. A, 01-2022
[3] Mini-Circuits Inc. DAT-31R5A-PP+ datasheet, M164761, REV. C, 05-2020

Title: *RF Attenuators*		**Author:** Juan Del Pino Mena	
		Approved: *	
Prj: Estigia Comms Payload - EGSE		**Prj. revision:** 0.4	
		Variant: [No Variations]	
Date: 03/09/2024 19:56:44	**Last modified:** 02/09/2024	**Altium version:** 24.3.1.35	
Size: A4	Sheet 7 of 12	**License:** --	
File: 5_1_attenuators.SchDoc		**Git Hash:**	

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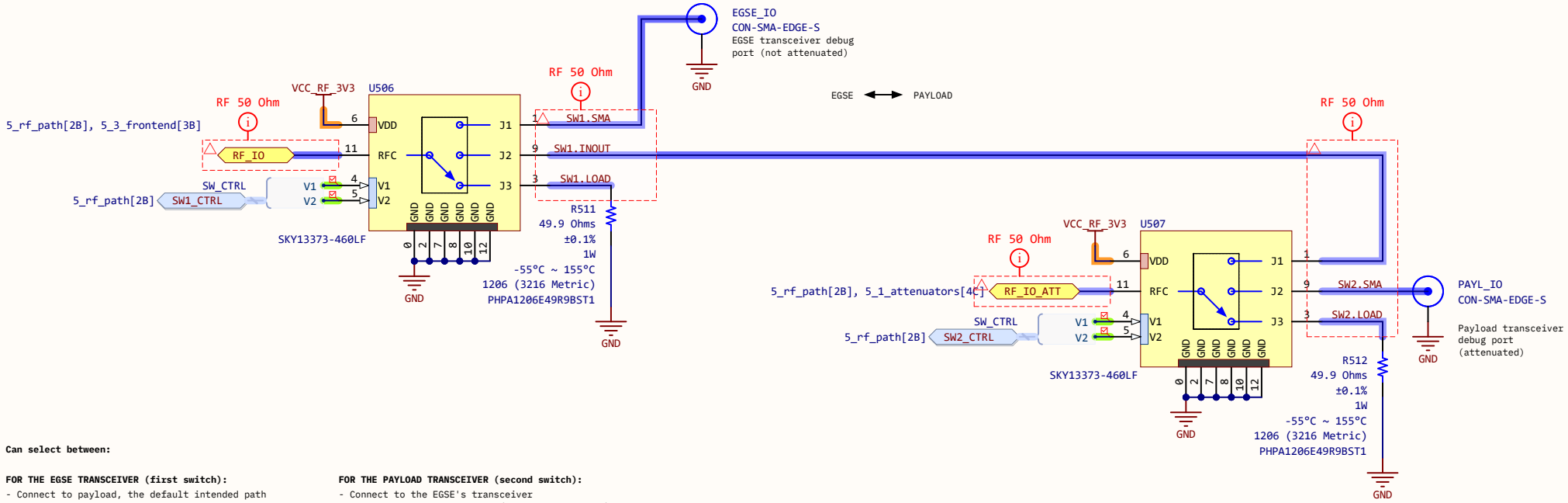
RF path selection switches



Can select between:

FOR THE EGSE TRANSCEIVER (first switch):

- Connect to payload, the default intended path through the attenuators to the payload's transceiver
- Connect to a SMA connector, rendering the transceiver's signal available for debugging purposes.
- Connect to 50-ohm load, to sink the rf signal if not used.

MMCX to payload, general-purpose SMA, 50-ohm load

FOR THE PAYLOAD TRANSCEIVER (second switch):

- Connect to the EGSE's transceiver
- Connect to a SMA connector (after attenuation!), rendering the transceiver output available for an antenna, an analyzer, etc.
- Connect to 50-ohm load, to sink the rf signal if not used.

Decoupling capacitors

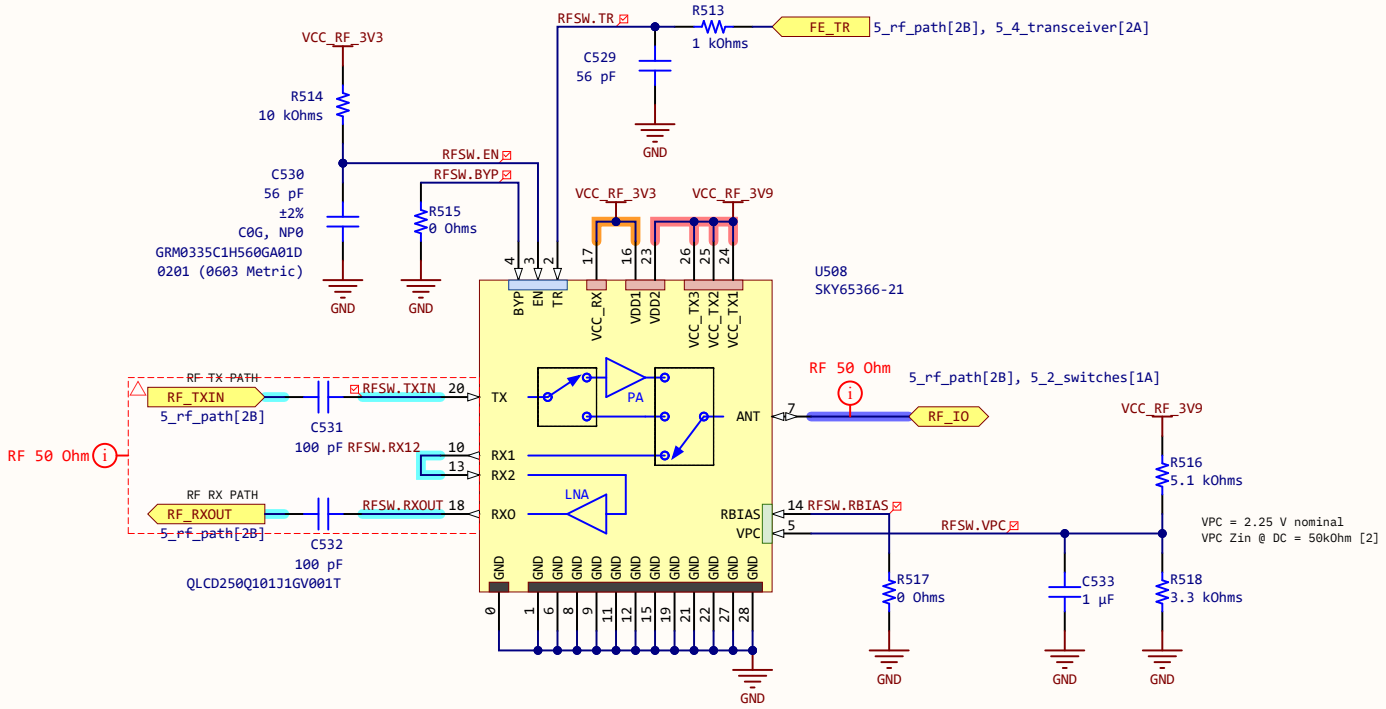
Notes:

[1] Skyworks Inc. SKY13373-460LF Datasheet, 201264O, 05-2016

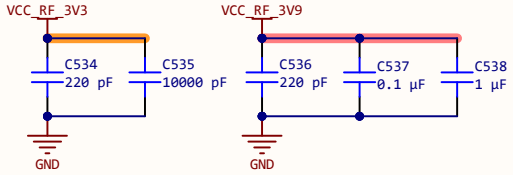
Title: *RF Switches*		**Author:** Juan Del Pino Mena	**Pluton UPV**
Prj: Estigia Comms Payload - EGSE		**Approved:** *	*Universitat Politècnica de València (UPV)*
		Prj. revision: 0.4	*Camí de Vera, València*
Date: 03/09/2024 19:56:45	**Last modified:** 03/09/2024	**Variant:** [No Variations]	*Spain*
Size: A4	Sheet 8 of 12	**Altium version:** 24.3.1.35	
File: 5_2_switches.SchDoc		**License:** --	
		Git Hash:	

RF Front-End module (Switch + LNA + PA)

Front-end module always enabled, never bypassed.



Decoupling capacitors



Notes:

[1] Semtech Inc. SX1302 Corecell Reference Design with SX1250 RF Front-Ends, PCB_E539V01A, 01-2020
[2] Skyworks Inc. SKY65366-21 400 MHz Tx/Rx Front-End Module, 203146E, 10-2020

Title:	***RF Front-end module***
Prj:	Estigia Comms Payload - EGSE
Date:	03/09/2024 19:56:45
Last modified:	03/09/2024
Size:	A4
	Sheet 9 of 12
File:	5_3_frontend.SchDoc

Author:	Juan Del Pino Mena
Approved:	*
Prj. revision:	0.4
Variant:	[No Variations]
Altium version:	24.3.1.35
License:	--
Git Hash:	

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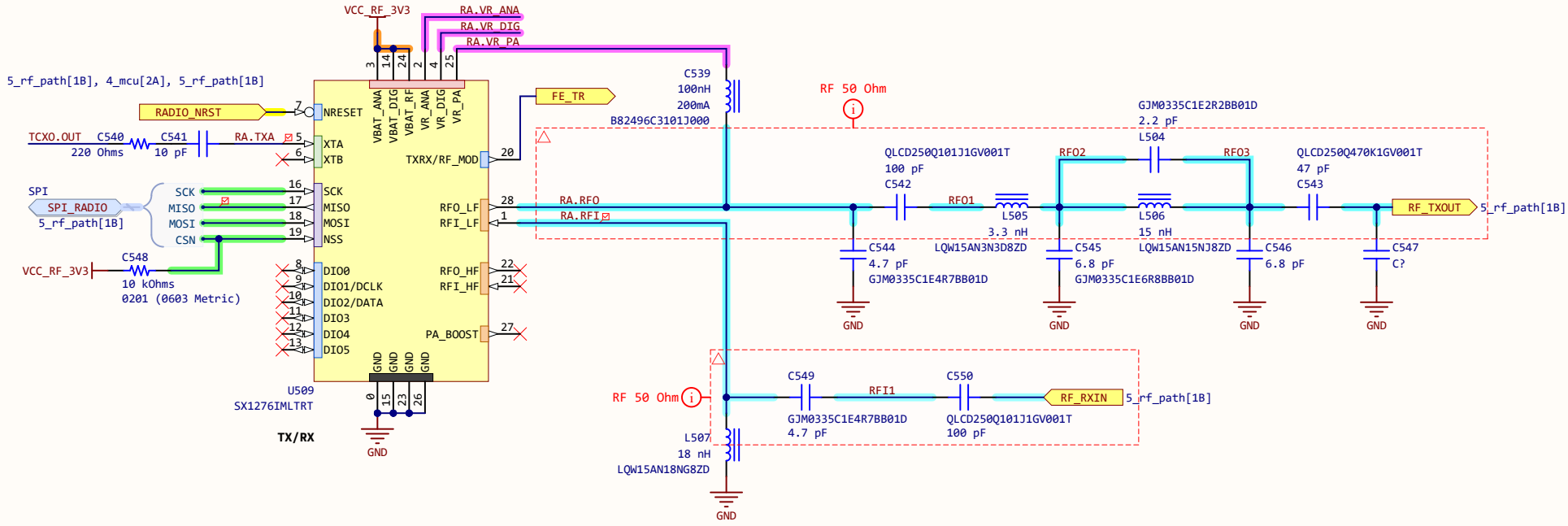
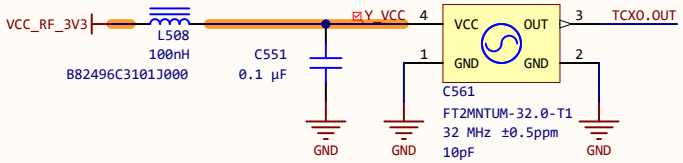
LoRa Node Transceiver

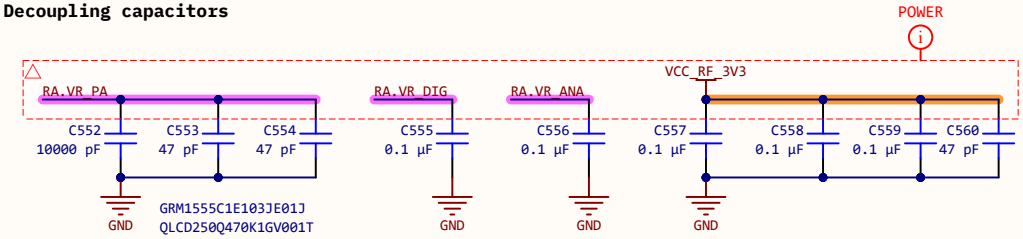


Xtal oscillator

Clipped-sine output TCXO are required, Vout_pp <= 1.2 V. Recommended a GPS-precision TCXO (0.5 ppm). A TCXO should be connected to pin XTA through a 220-ohm res and a 10 pF DC-cut cap to reduce the amplitude [4]. Pin XTB should be left open [1].



Decoupling capacitors

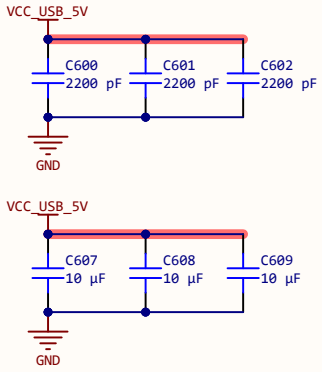


Notes:

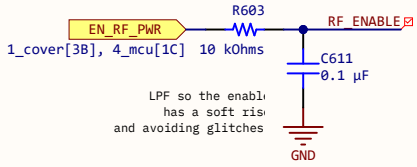
[1] Semtech Inc. SX127x datasheet, Rev 7, 05-2020
[2] Semtech Inc. SX127x reference design overview, AN1200.19, 12-2014
[3] Semtech Inc. SX1276 433/915 MHz reference design SX1276MB1LAS, PCB_E311V02A, v1a, 02-2015

Title: *LoRa node transceiver*		**Author:** Juan Del Pino Mena	**Pluton UPV**
Prj: Estigia Comms Payload - EGSE		**Approved:** *	*Universitat Politècnica de València (UPV)*
Date: 03/09/2024 19:56:45	**Last modified:** 02/09/2024	**Prj. revision:** 0.4	*Camí de Vera, València*
Size: A4	Sheet 10 of 12	**Variant:** [No Variations]	*Spain*
File: 5_4_transceiver.SchDoc		**Altium version:** 24.3.1.35	
		License: --	
		Git Hash:	

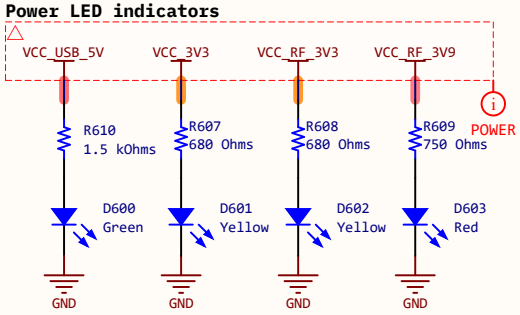
Decoupling capacitors



Enable RF supply



Power LED indicators



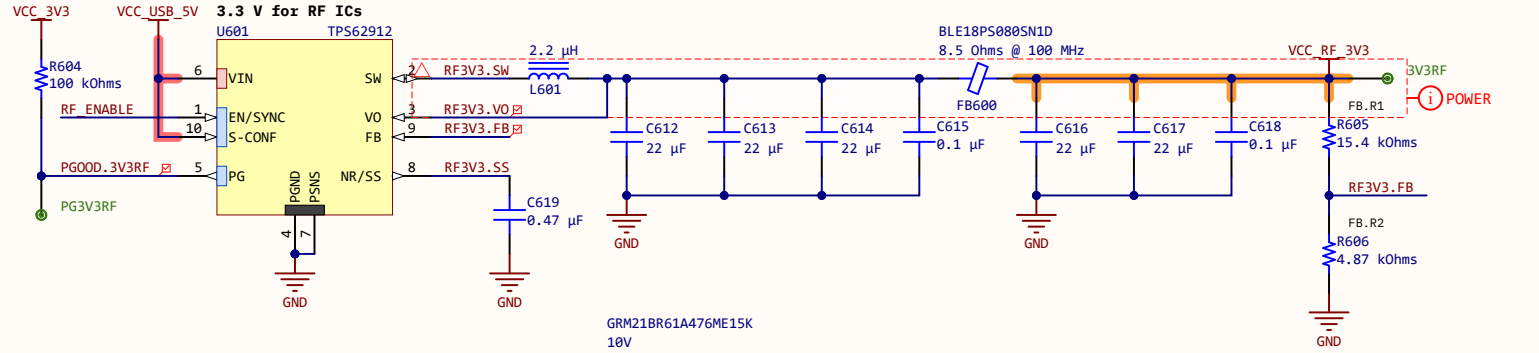
The TPS62912 PG pin is in high Z when V(FB) >= 95%, and driven low when V(FB) <= 90% . The open-drain pin requires a pullup. The PG signal is used for sequencing of multiple rails by connecting to the EN pin of other converters [1].

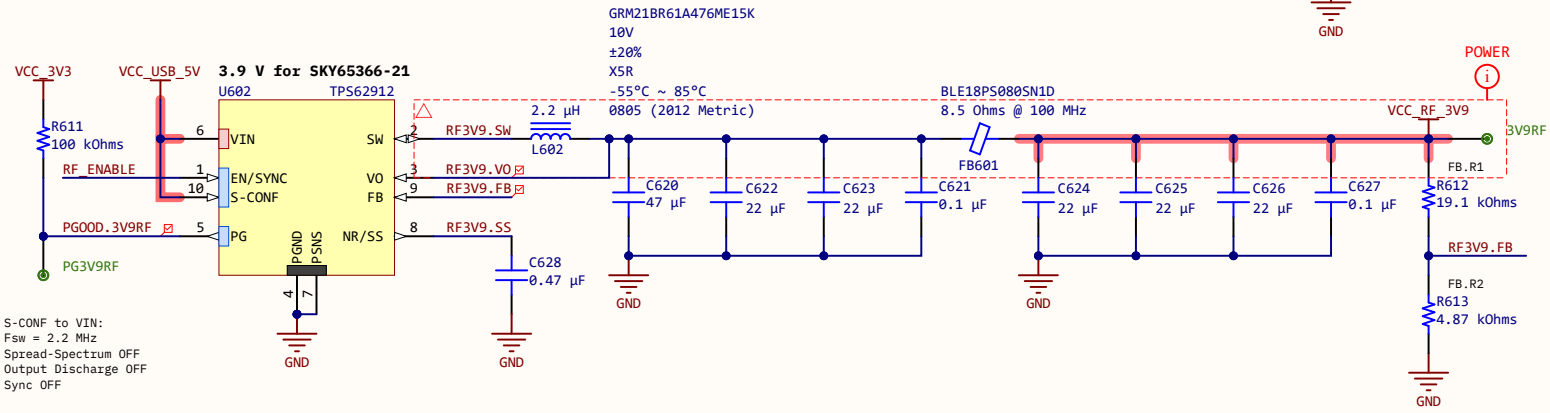
To ensure control of all digital IOs during the power-up/down of the SX1302 and avoid an inrush current, the 1.2 V rail shall be enabled before 3.3 V at start-up [2].

Low noise DC/DC converters

POWER GOOD OUTPUT

CAUTION! Power good signals are working in the digital 3V3 rail





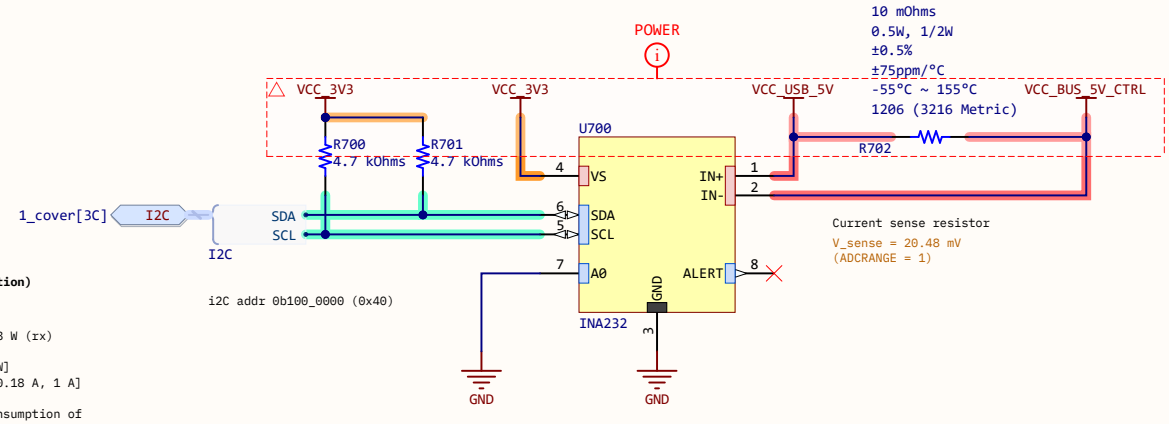
Notes:

Power supply based on low-noise DC/DC converters.
[1] Texas Instruments Inc. TPS62912/3 datasheet, SLVSFP4B, 03-2021
[2] Semtech Inc. Errata Note Corecell PCB #e539v01e Reference Design, Rev 1.0, 03-2020

Title: *Power management*		**Author:** Juan Del Pino Mena	**Pluton UPV**
Prj: Estigia Comms Payload - EGSE		**Approved:** *	*Universitat Politècnica de València (UPV)*
Date: 03/09/2024 19:56:45	**Last modified:** 31/08/2024	**Prj. revision:** 0.4	*Camí de Vera, València*
Size: A4	Sheet 11 of 12	**Variant:** [No Variations]	*Spain*
File: 6_power_dcdc.SchDoc		**Altium version:** 24.3.1.35	
		License: --	
		Git Hash:	

Voltage, current and power monitor

Power measurement excludes EGSE's own consumption. It only monitors the payload's.



R_SHUNT selection (early power budget estimation)

Carrier power consumption: 0.33 W (max)
LoRa SoM power consumption: 4.62 W (tx); 0.58 W (rx)

Expected total power consumption: [0.9 W, 5 W]
Thus, at V_cc = 5 V : current consumption: [0.18 A, 1 A]

Account for an instantaneous peak current consumption of double the maximum: I_peak = 2 A

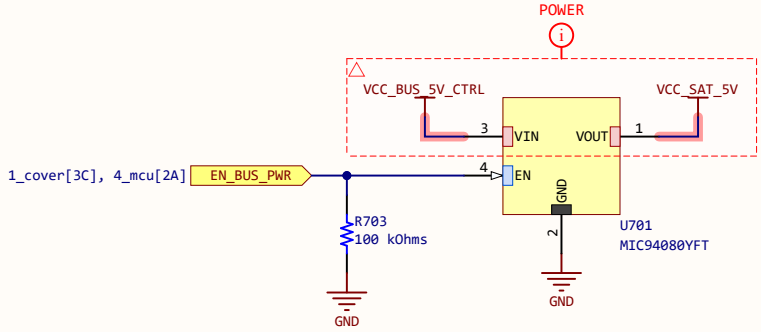
For minimum voltage drop, V_sense = 20.48 mV (INA232 cfg)

R_shunt < V_sense / I_peak = 10.24 mOhm

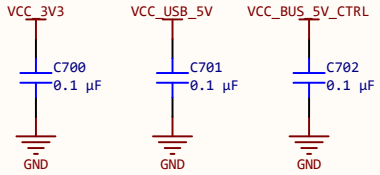
Power dissipated on R_shunt: 42 mW

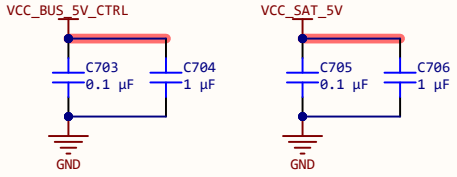
R_shunt = 10 mOhm, tolerance <=0.5 %, power >= 0.1 W

Load power switch



Decoupling capacitors





Notes:

[1] Texas Instruments Inc. INA232 datasheet, SBOSAA2, 12-2022
[2] Semtech Inc. Errata Note Corecell PCB #e539v01e Reference Design, Rev 1.0, 03-2020
[3] Microchip Inc. MIC94080/1/2/3/4/5 datasheet, DS20006118A, 2019

Title:	*Bus power control & monitoring*
Prj:	Estigia Comms Payload - EGSE
Date:	03/09/2024 19:56:46
Last modified:	11/08/2024
Size:	A4
Sheet	12 of 12
File:	7_power_prot_mon.SchDoc
Author:	Juan Del Pino Mena
Approved:	*
Prj. revision:	0.4
Variant:	[No Variations]
Altium version:	24.3.1.35
License:	--
Git Hash:	

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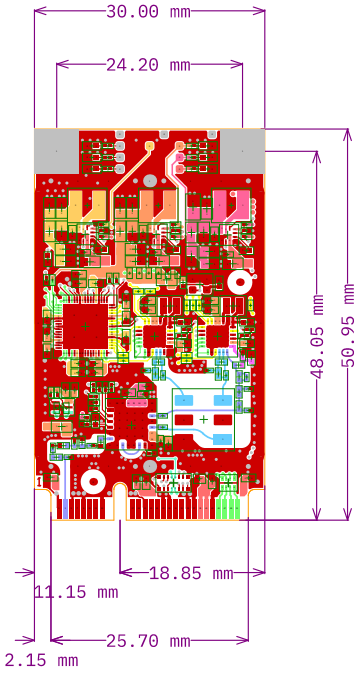
Appendix D

Printed Circuit Boards

The following pages contain prints of the most relevant layers of the three developed printed circuit boards. For a more detailed explanation of the PCBs, please refer to section 4.2: Printed circuit board design.

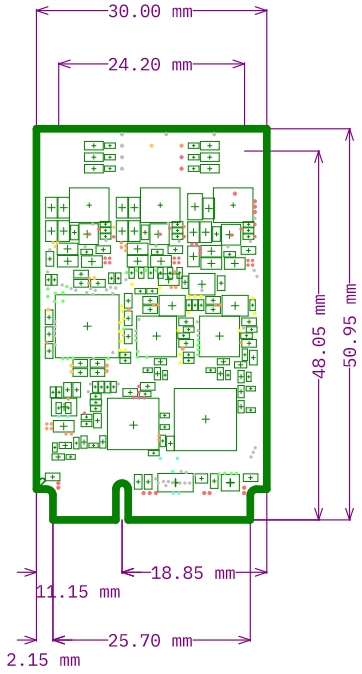
Refer to the table of contents below to locate the PCB prints for each board:



Layer	Name	Material	Thickness	Constant	Gerber
	Top Overlay				GTO
	Top Solder	SM-001	0.025mm	4	GTS
1	Top	CF-003	0.018mm		GTL
	PP-top	PP-008	0.130mm	4.1	
2	GND-1	CF-004	0.035mm		GP1
	Core-1	Core-009	0.180mm	4.5	
3	Signal-1	CF-004	0.035mm		G1
	PP-mid	PP-008	0.130mm	4.1	
4	Signal-2	CF-004	0.035mm		G2
	Core-2	Core-009	0.180mm	4.5	
5	GND-2	CF-004	0.035mm		GP2
	PP-bottom	PP-008	0.130mm	4.1	
6	Bottom	CF-003	0.018mm		GBL
	Board Layer Stack Bottom Solder	SM-001	0.025mm	4	GBS
	Board Layer Stack Bottom Overlay				GBO

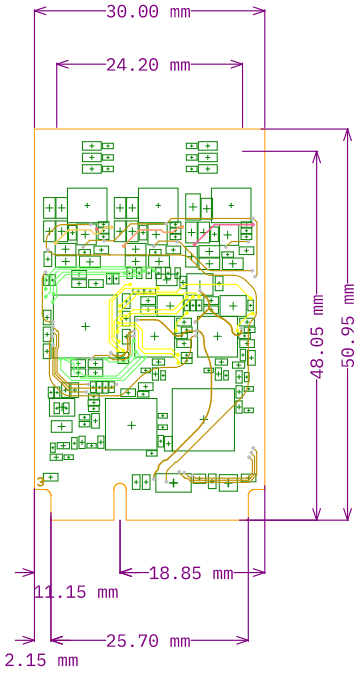
Total board thickness: 0.976mm

Pluton UPV		PLUTON
Project: Estigia comms payload - LoRa Gateway SoM		
Layer: Top Board Shape Component Guard Dimension		
Engineer: Juan Del Pino Mena		
Date: 2024-08-11	Revision: 0.4	Size: A4



Layer	Name	Material	Thickness	Constant	Gerber
	Top Overlay				GTO
	Top Solder	SM-001	0.025mm	4	GTS
1	Top	CF-003	0.018mm		GTL
	PP-top	PP-008	0.130mm	4.1	
2	GND-1	CF-004	0.035mm		GP1
	Core-1	Core-009	0.180mm	4.5	
3	Signal-1	CF-004	0.035mm		G1
	PP-mid	PP-008	0.130mm	4.1	
4	Signal-2	CF-004	0.035mm		G2
	Core-2	Core-009	0.180mm	4.5	
5	GND-2	CF-004	0.035mm		GP2
	PP-bottom	PP-008	0.130mm	4.1	
6	Bottom	CF-003	0.018mm		GBL
	Board Layer Stack Bottom Solder	SM-001	0.025mm	4	GBS
	Board Layer Stack Bottom Overlay				GBO
Total board thickness:			0.976mm		

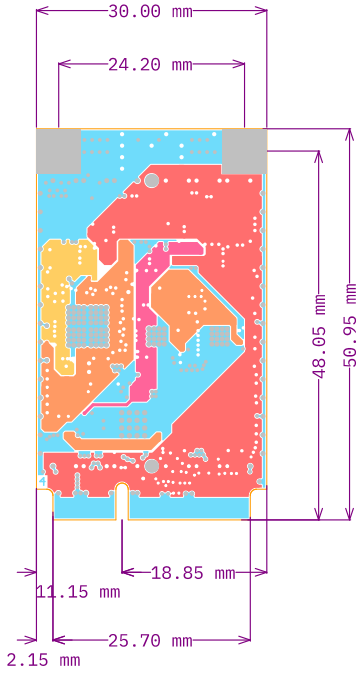
Pluton UPV		PLUTON
Project: Estigia comms payload - LoRa Gateway SoM		
Layer: GND-1 Board Shape Component Guard Dimension		
Engineer: Juan Del Pino Mena		
Date: 2024-08-11	Revision: 0.4	Size: A4



Layer	Name	Material	Thickness	Constant	Gerber
	Top Overlay				GTO
	Top Solder	SM-001	0.025mm	4	GTS
1	Top	CF-003	0.018mm		GTL
	PP-top	PP-008	0.130mm	4.1	
2	GND-1	CF-004	0.035mm		GP1
	Core-1	Core-009	0.180mm	4.5	
3	Signal-1	CF-004	0.035mm		G1
	PP-mid	PP-008	0.130mm	4.1	
4	Signal-2	CF-004	0.035mm		G2
	Core-2	Core-009	0.180mm	4.5	
5	GND-2	CF-004	0.035mm		GP2
	PP-bottom	PP-008	0.130mm	4.1	
6	Bottom	CF-003	0.018mm		GBL
	Board Layer Stack Bottom Solder	SM-001	0.025mm	4	GBS
	Board Layer Stack Bottom Overlay				GBO

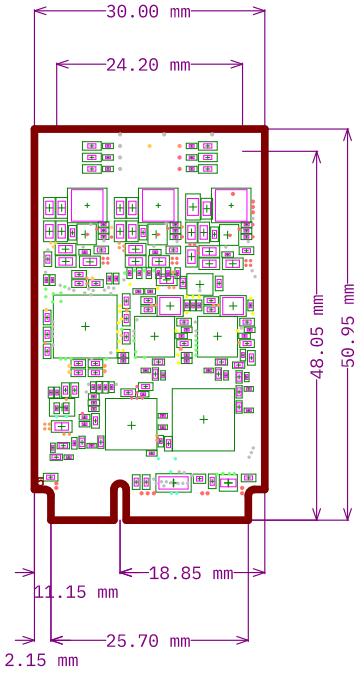
Total board thickness: 0.976mm

Pluton UPV		PLUTON
Project: Estigia comms payload - LoRa Gateway SoM		
Layer: Signal-1 Board Shape Component Guard Dimension		
Engineer: Juan Del Pino Mena		
Date: 2024-08-11	Revision: 0.4	Size: A4



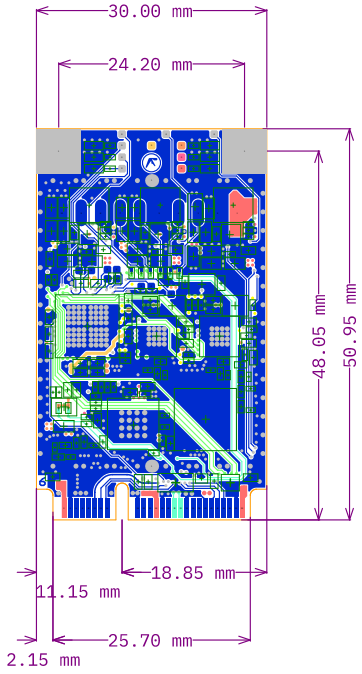
Layer	Name	Material	Thickness	Constant	Gerber
	Top Overlay				GTO
	Top Solder	SM-001	0.025mm	4	GTS
1	Top	CF-003	0.018mm		GTL
	PP-top	PP-008	0.130mm	4.1	
2	GND-1	CF-004	0.035mm		GP1
	Core-1	Core-009	0.180mm	4.5	
3	Signal-1	CF-004	0.035mm		G1
	PP-mid	PP-008	0.130mm	4.1	
4	Signal-2	CF-004	0.035mm		G2
	Core-2	Core-009	0.180mm	4.5	
5	GND-2	CF-004	0.035mm		GP2
	PP-bottom	PP-008	0.130mm	4.1	
6	Bottom	CF-003	0.018mm		GBL
	Board Layer Stack Bottom Solder	SM-001	0.025mm	4	GBS
	Board Layer Stack Bottom Overlay				GBO
Total board thickness:			0.976mm		

Pluton UPV		PLUTON
Project: Estigia comms payload - LoRa Gateway SoM		
Layer: Signal-2 Board Shape Dimension		
Engineer: Juan Del Pino Mena		
Date: 2024-08-11	Revision: 0.4	Size: A4



Layer	Name	Material	Thickness	Constant	Gerber
	Top Overlay				GTO
	Top Solder	SM-001	0.025mm	4	GTS
1	Top	CF-003	0.018mm		GTL
	PP-top	PP-008	0.130mm	4.1	
2	GND-1	CF-004	0.035mm		GP1
	Core-1	Core-009	0.180mm	4.5	
3	Signal-1	CF-004	0.035mm		G1
	PP-mid	PP-008	0.130mm	4.1	
4	Signal-2	CF-004	0.035mm		G2
	Core-2	Core-009	0.180mm	4.5	
5	GND-2	CF-004	0.035mm		GP2
	PP-bottom	PP-008	0.130mm	4.1	
6	Bottom	CF-003	0.018mm		GBL
	Board Layer Stack Bottom Solder	SM-001	0.025mm	4	GBS
	Board Layer Stack Bottom Overlay				GBO
Total board thickness:			0.976mm		

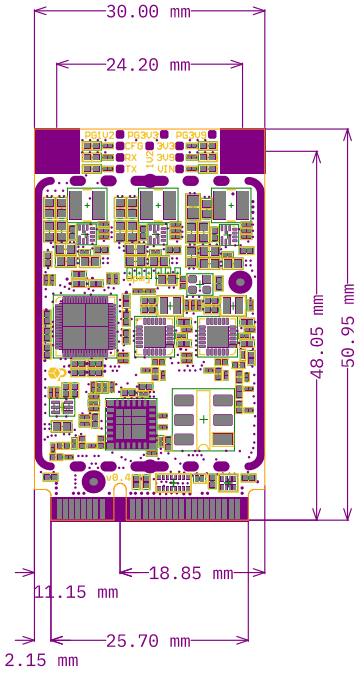
Pluton UPV		PLUTON
Project: Estigia comms payload - LoRa Gateway SoM		
Layer: GND-2 Board Shape Component Guard Dimension		
Engineer: Juan Del Pino Mena		
Date: 2024-08-11	Revision: 0.4	Size: A4



Layer	Name	Material	Thickness	Constant	Gerber
	Top Overlay				GTO
	Top Solder	SM-001	0.025mm	4	GTS
1	Top	CF-003	0.018mm		GTL
	PP-top	PP-008	0.130mm	4.1	
2	GND-1	CF-004	0.035mm		GP1
	Core-1	Core-009	0.180mm	4.5	
3	Signal-1	CF-004	0.035mm		G1
	PP-mid	PP-008	0.130mm	4.1	
4	Signal-2	CF-004	0.035mm		G2
	Core-2	Core-009	0.180mm	4.5	
5	GND-2	CF-004	0.035mm		GP2
	PP-bottom	PP-008	0.130mm	4.1	
6	Bottom	CF-003	0.018mm		GBL
	Board Layer Stack Bottom Solder	SM-001	0.025mm	4	GBS
	Board Layer Stack Bottom Overlay				GBO

Total board thickness: 0.976mm

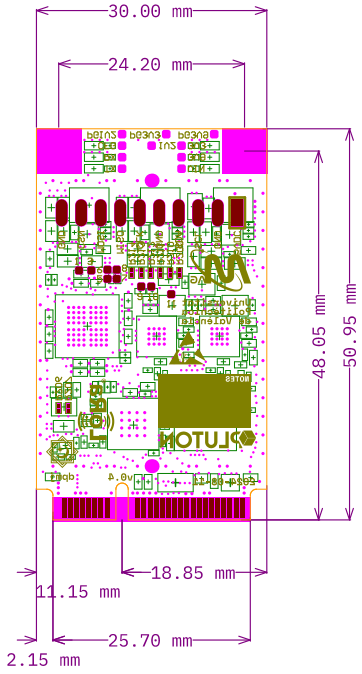
Pluton UPV		PLUTON
Project: Estigia comms payload - LoRa Gateway SoM		
Layer: Bottom Board Shape Component Guard Dimension		
Engineer: Juan Del Pino Mena		
Date: 2024-08-11	Revision: 0.4	Size: A4



Layer	Name	Material	Thickness	Constant	Gerber
	Top Overlay				GTO
	Top Solder	SM-001	0.025mm	4	GTS
1	Top	CF-003	0.018mm		GTL
	PP-top	PP-008	0.130mm	4.1	
2	GND-1	CF-004	0.035mm		GP1
	Core-1	Core-009	0.180mm	4.5	
3	Signal-1	CF-004	0.035mm		G1
	PP-mid	PP-008	0.130mm	4.1	
4	Signal-2	CF-004	0.035mm		G2
	Core-2	Core-009	0.180mm	4.5	
5	GND-2	CF-004	0.035mm		GP2
	PP-bottom	PP-008	0.130mm	4.1	
6	Bottom	CF-003	0.018mm		GBL
	Board Layer Stack Bottom Solder	SM-001	0.025mm	4	GBS
	Board Layer Stack Bottom Overlay				GBO

Total board thickness: 0.976mm

Pluton UPV		PLUTON
Project: Estigia comms payload - LoRa Gateway SoM		
Layer: Top Paste Top Overlay Board Shape Component Guard Top Solder Dimension		
Engineer: Juan Del Pino Mena		
Date: 2024-08-11	Revision: 0.4	Size: A4

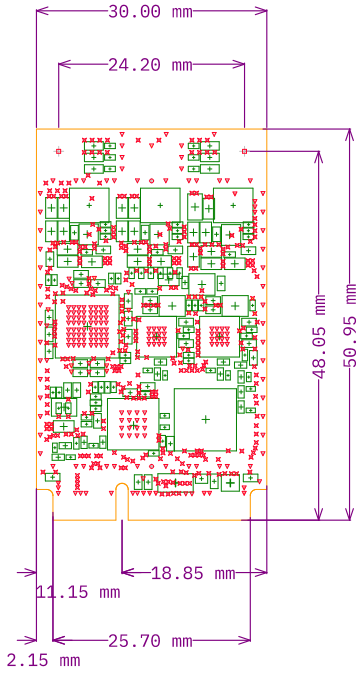


Layer	Name	Material	Thickness	Constant	Gerber
	Top Overlay				GTO
	Top Solder	SM-001	0.025mm	4	GTS
1	Top	CF-003	0.018mm		GTL
	PP-top	PP-008	0.130mm	4.1	
2	GND-1	CF-004	0.035mm		GP1
	Core-1	Core-009	0.180mm	4.5	
3	Signal-1	CF-004	0.035mm		G1
	PP-mid	PP-008	0.130mm	4.1	
4	Signal-2	CF-004	0.035mm		G2
	Core-2	Core-009	0.180mm	4.5	
5	GND-2	CF-004	0.035mm		GP2
	PP-bottom	PP-008	0.130mm	4.1	
6	Bottom	CF-003	0.018mm		GBL
	Board Layer Stack Bottom Solder	SM-001	0.025mm	4	GBS
	Board Layer Stack Bottom Overlay				GBO

Total board thickness: 0.976mm

Pluton UPV		PLUTON
Project: Estigia comms payload - LoRa Gateway SoM		
Layer: Bottom Paste Board Shape Board Layer Stack Bottom Overlay Board Layer Stack Bottom Solder		
Engineer: Juan Del Pino Mena		
Date: 2024-08-11	Revision: 0.4	Size: A4

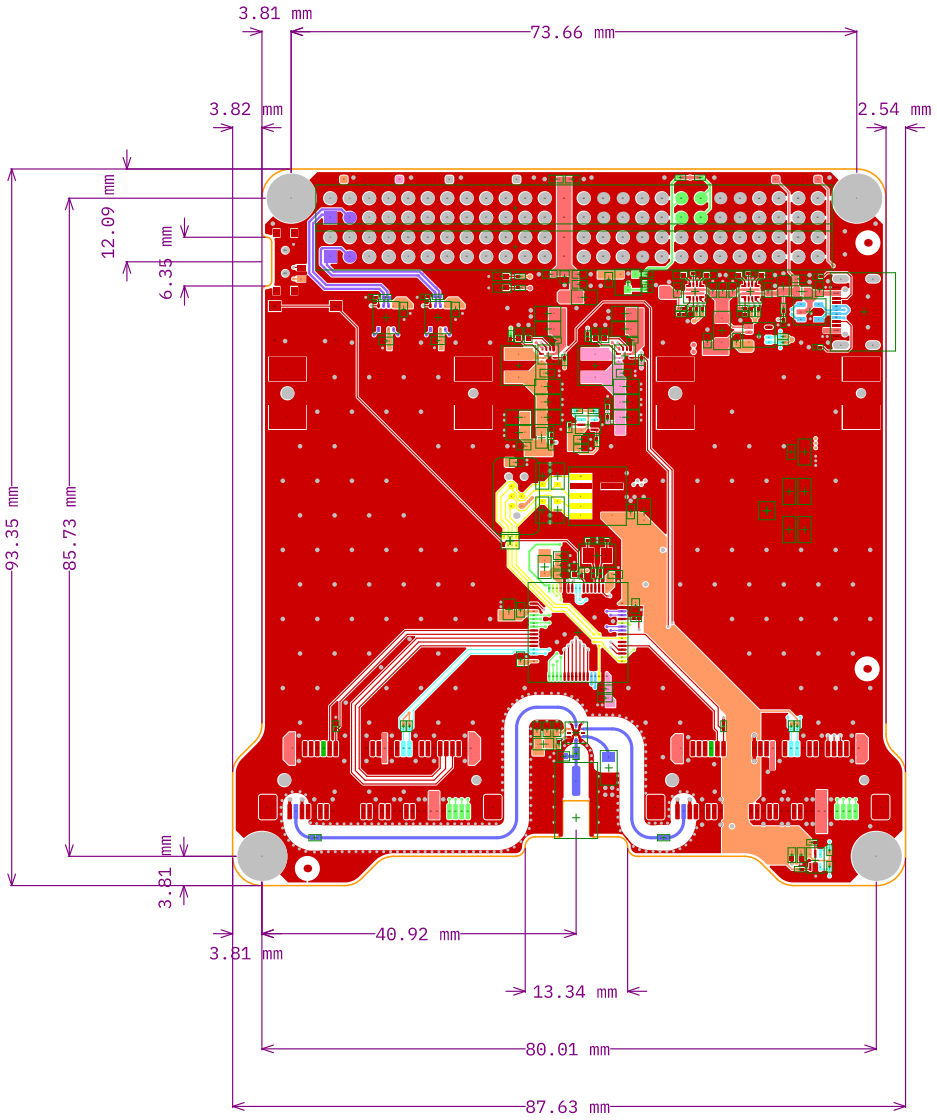
Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template
⛝	353	0.200mm	PTH	Round	Top - Bottom	Via	Rounded	v40h20_lib
▽	215	0.300mm	PTH	Round	Top - Bottom	(Mixed)	(Mixed)	(Mixed)
○	2	1.300mm	PTH	Round	Top - Bottom	Pad	Rounded	c170h130p0
□	2	2.600mm	PTH	Round	Top - Bottom	Pad	Rectangle	s580h260
	572 Total							



Layer	Name	Material	Thickness	Constant	Gerber
	Top Overlay				GTO
	Top Solder	SM-001	0.025mm	4	GTS
1	Top	CF-003	0.018mm		GTL
	PP-top	PP-008	0.130mm	4.1	
2	GND-1	CF-004	0.035mm		GP1
	Core-1	Core-009	0.180mm	4.5	
3	Signal-1	CF-004	0.035mm		G1
	PP-mid	PP-008	0.130mm	4.1	
4	Signal-2	CF-004	0.035mm		G2
	Core-2	Core-009	0.180mm	4.5	
5	GND-2	CF-004	0.035mm		GP2
	PP-bottom	PP-008	0.130mm	4.1	
6	Bottom	CF-003	0.018mm		GBL
	Board Layer Stack Bottom Solder	SM-001	0.025mm	4	GBS
	Board Layer Stack Bottom Overlay				GBO

Total board thickness: 0.976mm

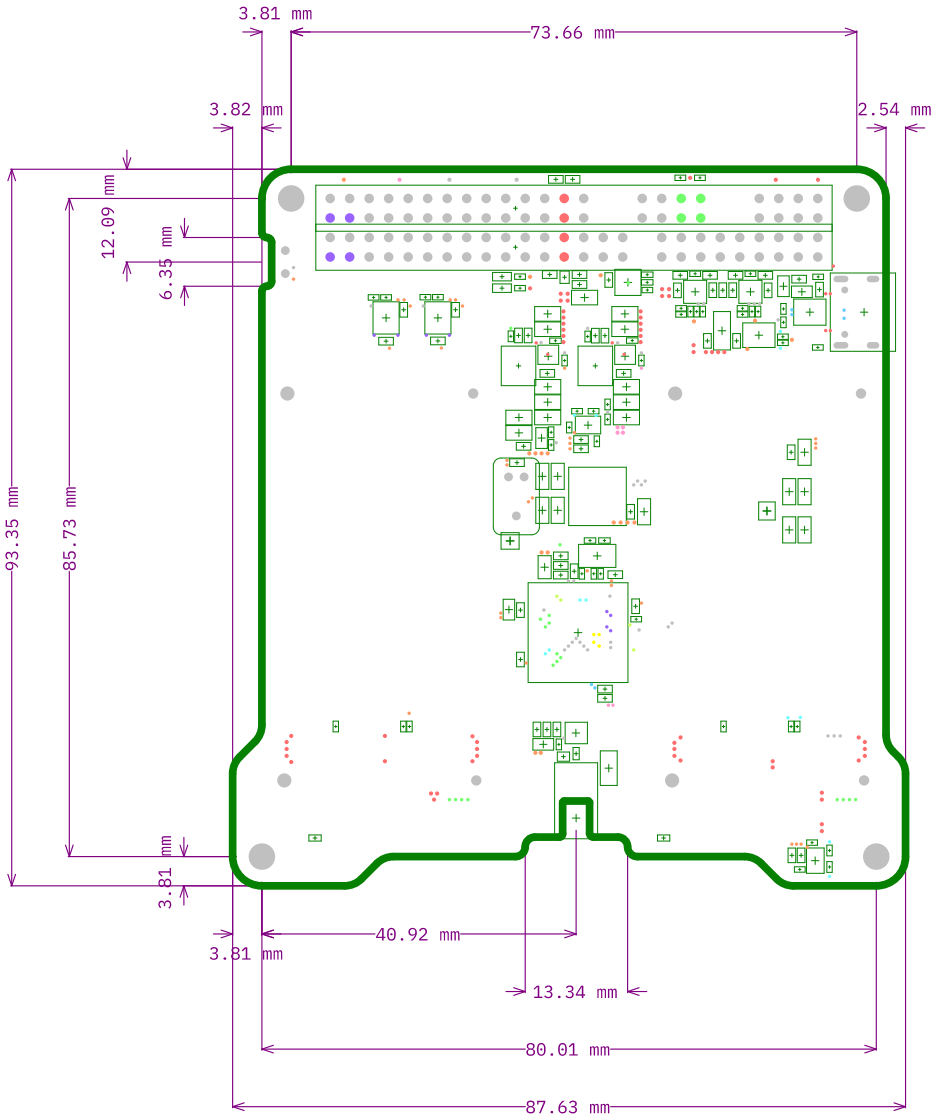
Pluton UPV		PLUTON
Project: Estigia comms payload - LoRa Gateway SoM		
Layer: Board Shape Component Guard Drill Drawing Drill Guide Dimension		
Engineer: Juan Del Pino Mena		
Date: 2024-08-11	Revision: 0.4	Size: A4



Layer	Name	Material	Thickness	Constant	Gerber
	Top Overlay				GTO
	Top Solder	SM-001	0.025mm	4	GTS
1	Top	CF-003	0.018mm		GTL
	PP-top	PP-008	0.220mm	4.1	
2	GND-1	CF-004	0.035mm		GP1
	Core 1	Core-009	0.350mm	4.5	
3	Layer 1	CF-004	0.035mm		G1
	PP-mid	PP-008	0.220mm	4.1	
4	Layer 2	CF-004	0.035mm		G2
	Core 2	Core-009	0.350mm	4.5	
5	GND-2	CF-004	0.035mm		GP2
	PP-bottom	PP-008	0.220mm	4.1	
6	Bottom	CF-003	0.018mm		GBL
	Board Layer Stack Bottom Solder	SM-001	0.025mm	4	GBS
	Board Layer Stack Bottom Overlay				GBO

Total board thickness: 1.586mm

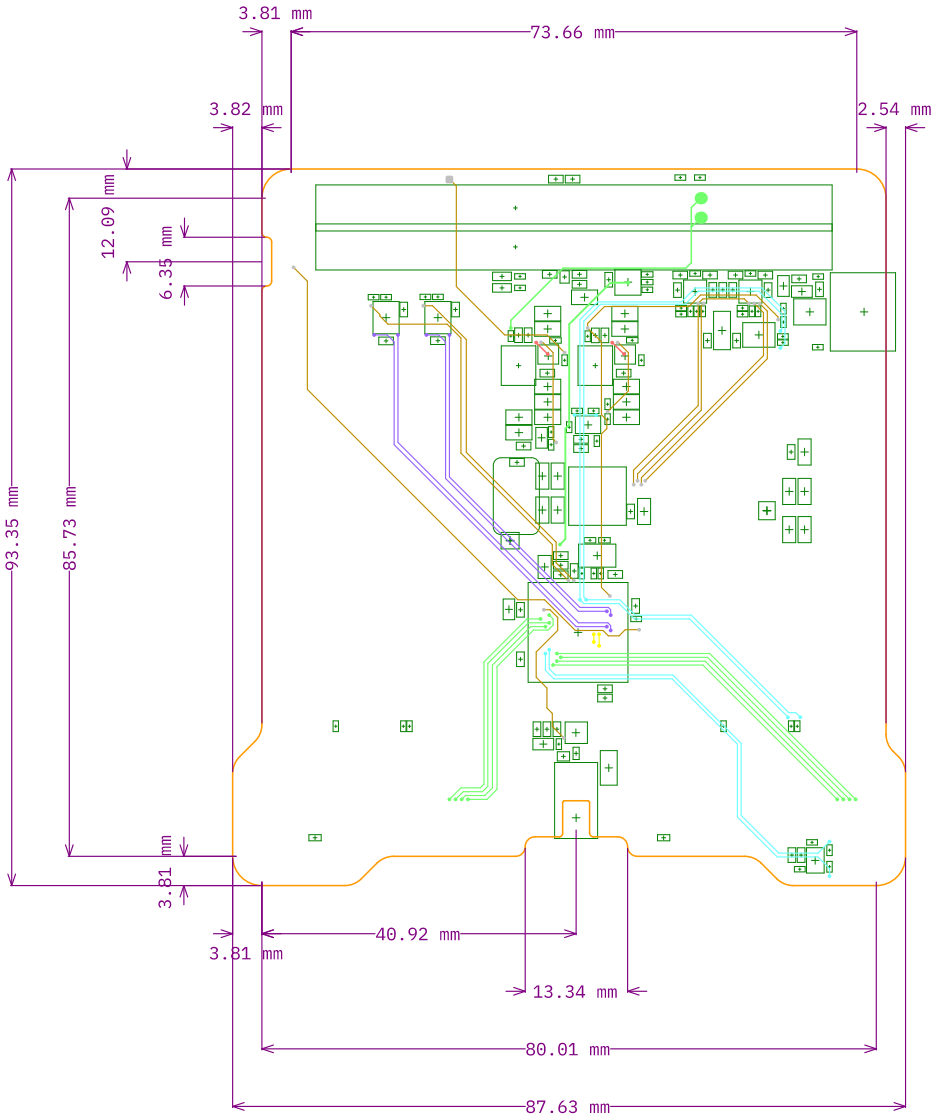
Pluton UPV		PLUTON
Project: Estigia Comms Payload - Cubesat carrier		
Layer: Component Guard Board Shape Component Guard Dimension		
Engineer: Juan Del Pino Mena		
Date: 2024-08-11	Revision: 0.4	Size: A4



Layer	Name	Material	Thickness	Constant	Gerber
	Top Overlay				GTO
	Top Solder	SM-001	0.025mm	4	GTS
1	Top	CF-003	0.018mm		GTL
	PP-top	PP-008	0.220mm	4.1	
2	GND-1	CF-004	0.035mm		GP1
	Core 1	Core-009	0.350mm	4.5	
3	Layer 1	CF-004	0.035mm		G1
	PP-mid	PP-008	0.220mm	4.1	
4	Layer 2	CF-004	0.035mm		G2
	Core 2	Core-009	0.350mm	4.5	
5	GND-2	CF-004	0.035mm		GP2
	PP-bottom	PP-008	0.220mm	4.1	
6	Bottom	CF-003	0.018mm		GBL
	Board Layer Stack Bottom Solder	SM-001	0.025mm	4	GBS
	Board Layer Stack Bottom Overlay				GBO

Total board thickness: 1.586mm

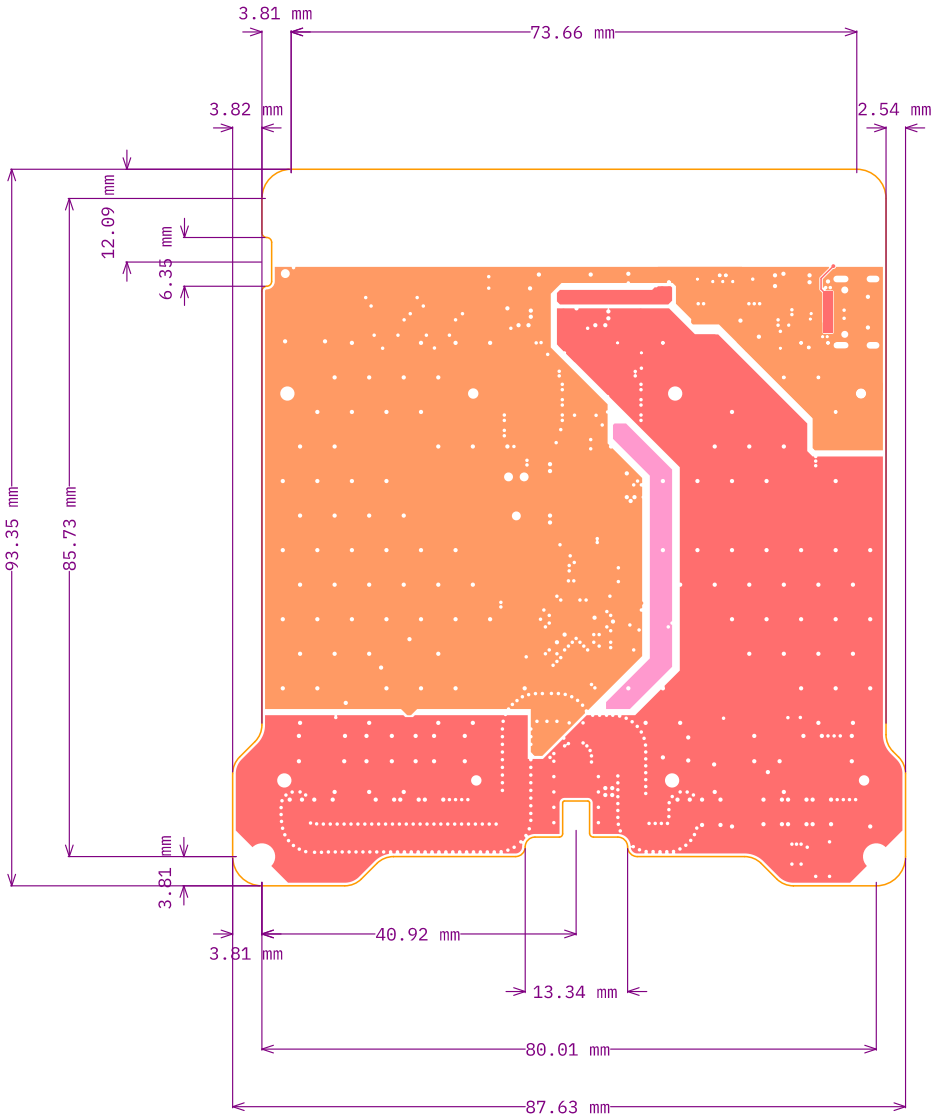
Pluton UPV		PLUTON
Project: Estigia Comms Payload - Cubesat carrier		
Layer: Board Shape Component Guard Component Guard Dimension		
Engineer: Juan Del Pino Mena		
Date: 2024-08-11	Revision: 0.4	Size: A4



Layer	Name	Material	Thickness	Constant	Gerber
	Top Overlay				GTO
	Top Solder	SM-001	0.025mm	4	GTS
1	Top	CF-003	0.018mm		GTL
	PP-top	PP-008	0.220mm	4.1	
2	GND-1	CF-004	0.035mm		GP1
	Core 1	Core-009	0.350mm	4.5	
3	Layer 1	CF-004	0.035mm		G1
	PP-mid	PP-008	0.220mm	4.1	
4	Layer 2	CF-004	0.035mm		G2
	Core 2	Core-009	0.350mm	4.5	
5	GND-2	CF-004	0.035mm		GP2
	PP-bottom	PP-008	0.220mm	4.1	
6	Bottom	CF-003	0.018mm		GBL
	Board Layer Stack Bottom Solder	SM-001	0.025mm	4	GBS
	Board Layer Stack Bottom Overlay				GBO

Total board thickness: 1.586mm

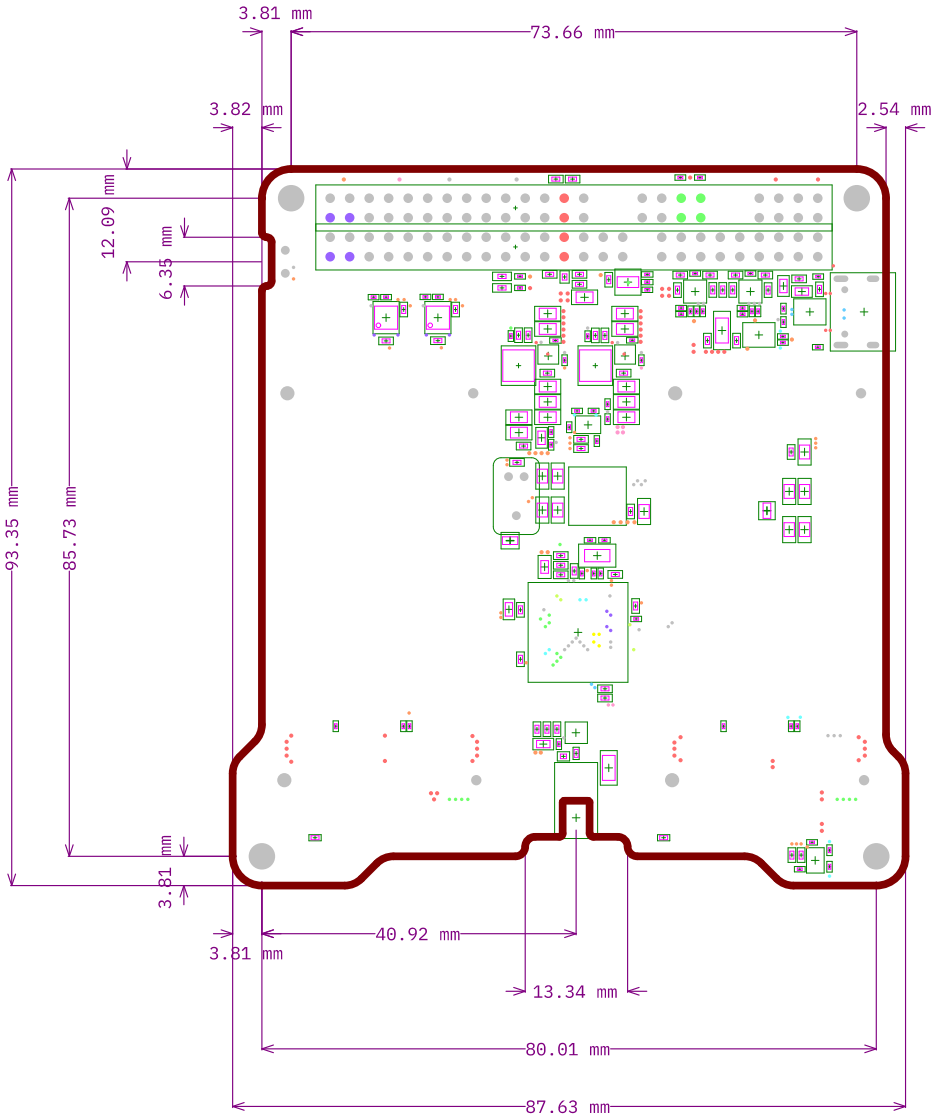
Pluton UPV		PLUTON
Project: Estigia Comms Payload - Cubesat carrier		
Layer: Board Shape Component Guard Component Guard Dimension		
Engineer: Juan Del Pino Mena		
Date: 2024-08-11	Revision: 0.4	Size: A4



Layer	Name	Material	Thickness	Constant	Gerber
	Top Overlay				GTO
	Top Solder	SM-001	0.025mm	4	GTS
1	Top	CF-003	0.018mm		GTL
	PP-top	PP-008	0.220mm	4.1	
2	GND-1	CF-004	0.035mm		GP1
	Core 1	Core-009	0.350mm	4.5	
3	Layer 1	CF-004	0.035mm		G1
	PP-mid	PP-008	0.220mm	4.1	
4	Layer 2	CF-004	0.035mm		G2
	Core 2	Core-009	0.350mm	4.5	
5	GND-2	CF-004	0.035mm		GP2
	PP-bottom	PP-008	0.220mm	4.1	
6	Bottom	CF-003	0.018mm		GBL
	Board Layer Stack Bottom Solder	SM-001	0.025mm	4	GBS
	Board Layer Stack Bottom Overlay				GBO

Total board thickness: 1.586mm

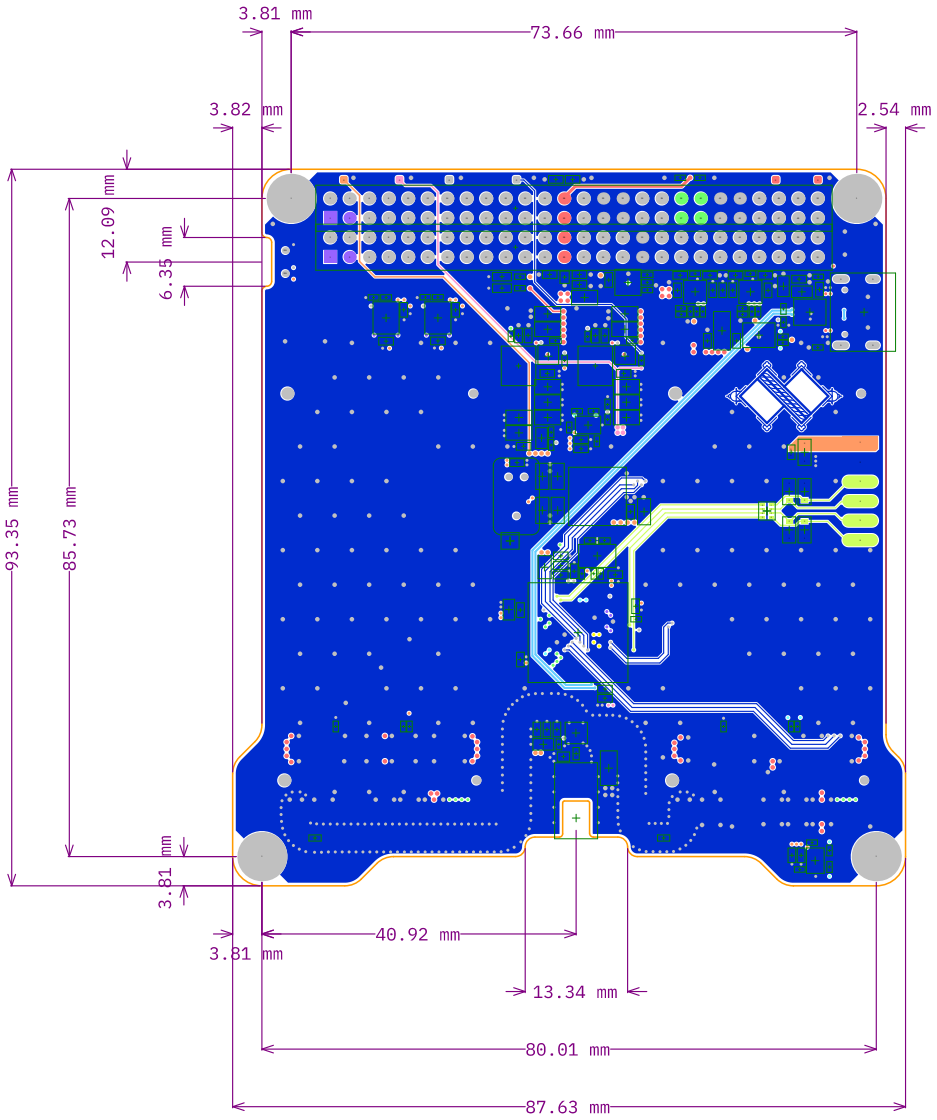
Pluton UPV		PLUTON
Project: Estigia Comms Payload - Cubesat carrier		
Layer: Board Shape Layer 2 Dimension		
Engineer: Juan Del Pino Mena		
Date: 2024-08-11	Revision: 0.4	Size: A4



Layer	Name	Material	Thickness	Constant	Gerber
	Top Overlay				GTO
	Top Solder	SM-001	0.025mm	4	GTS
1	Top	CF-003	0.018mm		GTL
	PP-top	PP-008	0.220mm	4.1	
2	GND-1	CF-004	0.035mm		GP1
	Core 1	Core-009	0.350mm	4.5	
3	Layer 1	CF-004	0.035mm		G1
	PP-mid	PP-008	0.220mm	4.1	
4	Layer 2	CF-004	0.035mm		G2
	Core 2	Core-009	0.350mm	4.5	
5	GND-2	CF-004	0.035mm		GP2
	PP-bottom	PP-008	0.220mm	4.1	
6	Bottom	CF-003	0.018mm		GBL
	Board Layer Stack Bottom Solder	SM-001	0.025mm	4	GBS
	Board Layer Stack Bottom Overlay				GBO

Total board thickness: 1.586mm

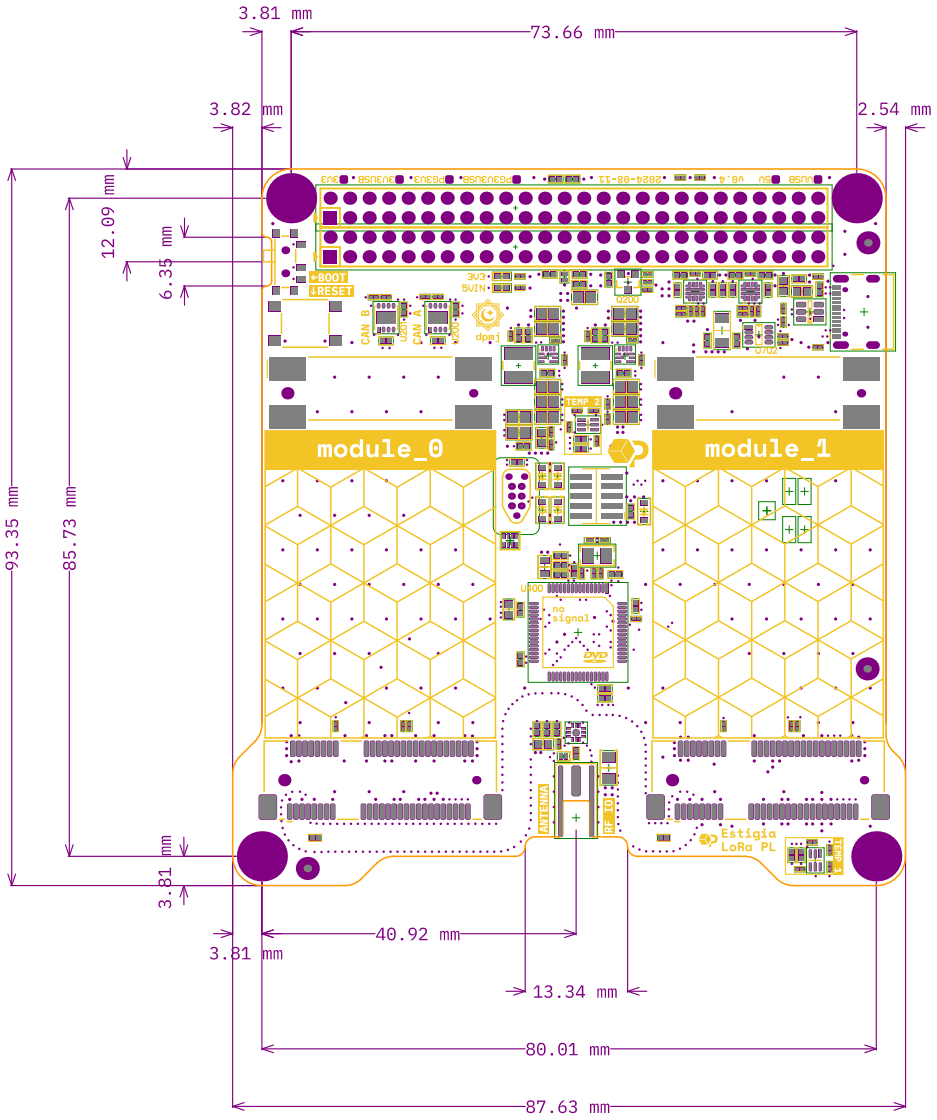
Pluton UPV		PLUTON
Project: Estigia Comms Payload - Cubesat carrier		
Layer: Component Guard Board Shape Component Guard Dimension		
Engineer: Juan Del Pino Mena		
Date: 2024-08-11	Revision: 0.4	Size: A4



Layer	Name	Material	Thickness	Constant	Gerber
	Top Overlay				GTO
	Top Solder	SM-001	0.025mm	4	GTS
1	Top	CF-003	0.018mm		GTL
	PP-top	PP-008	0.220mm	4.1	
2	GND-1	CF-004	0.035mm		GP1
	Core 1	Core-009	0.350mm	4.5	
3	Layer 1	CF-004	0.035mm		G1
	PP-mid	PP-008	0.220mm	4.1	
4	Layer 2	CF-004	0.035mm		G2
	Core 2	Core-009	0.350mm	4.5	
5	GND-2	CF-004	0.035mm		GP2
	PP-bottom	PP-008	0.220mm	4.1	
6	Bottom	CF-003	0.018mm		GBL
	Board Layer Stack Bottom Solder	SM-001	0.025mm	4	GBS
	Board Layer Stack Bottom Overlay				GBO

Total board thickness: 1.586mm

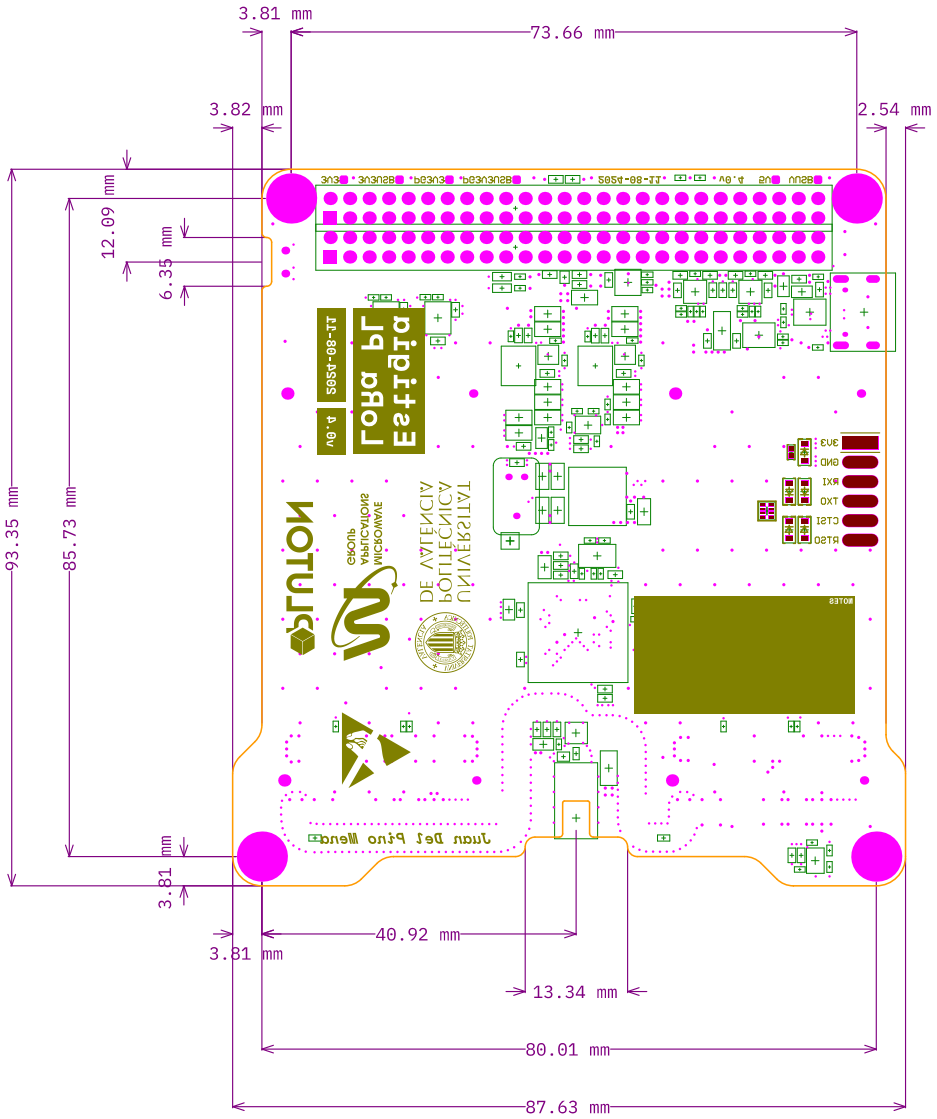
Pluton UPV		PLUTON
Project: Estigia Comms Payload - Cubesat carrier		
Layer: Board Shape Component Guard Component Guard Dimension		
Engineer: Juan Del Pino Mena		
Date: 2024-08-11	Revision: 0.4	Size: A4



Layer	Name	Material	Thickness	Constant	Gerber
	Top Overlay				GTO
	Top Solder	SM-001	0.025mm	4	GTS
1	Top	CF-003	0.018mm		GTL
	PP-top	PP-008	0.220mm	4.1	
2	GND-1	CF-004	0.035mm		GP1
	Core 1	Core-009	0.350mm	4.5	
3	Layer 1	CF-004	0.035mm		G1
	PP-mid	PP-008	0.220mm	4.1	
4	Layer 2	CF-004	0.035mm		G2
	Core 2	Core-009	0.350mm	4.5	
5	GND-2	CF-004	0.035mm		GP2
	PP-bottom	PP-008	0.220mm	4.1	
6	Bottom	CF-003	0.018mm		GBL
	Board Layer Stack Bottom Solder	SM-001	0.025mm	4	GBS
	Board Layer Stack Bottom Overlay				GBO

Total board thickness: 1.586mm

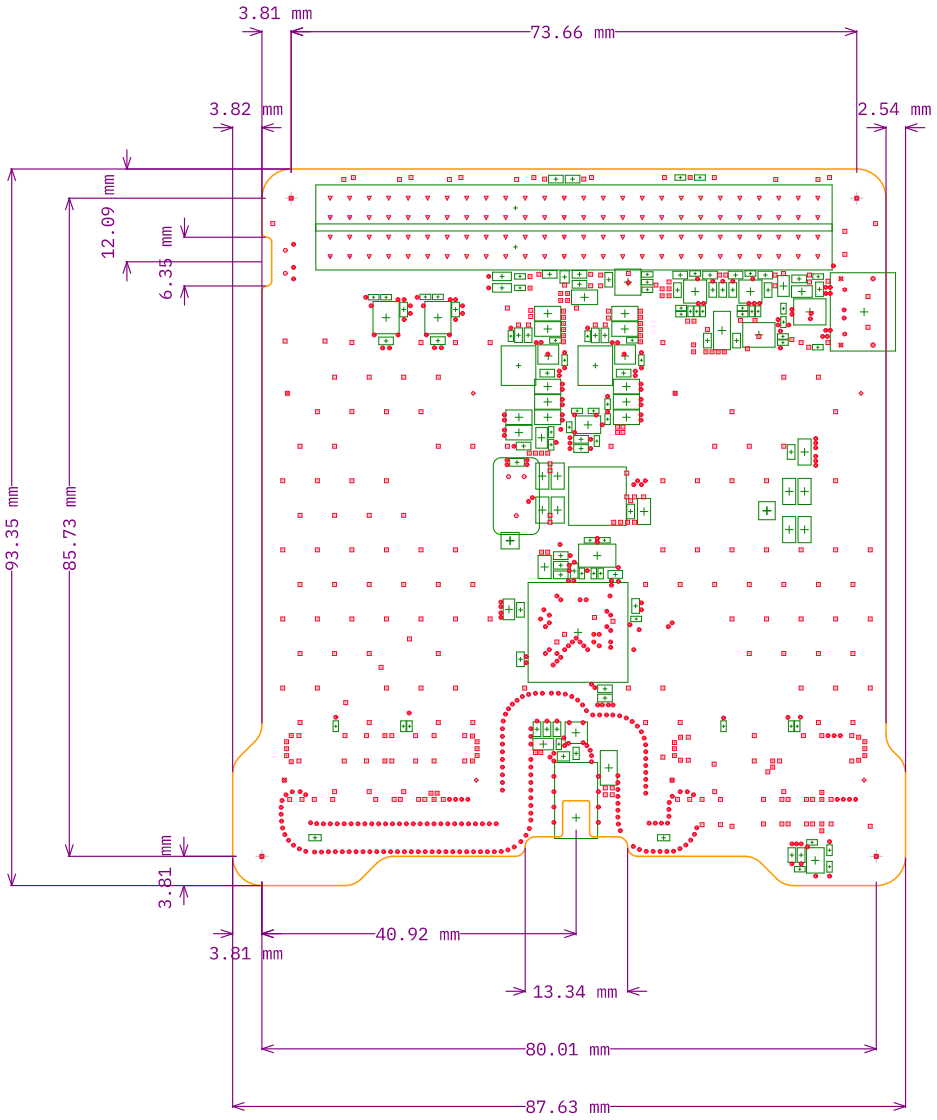
Pluton UPV		PLUTON
Project: Estigia Comms Payload - Cubesat carrier		
Layer: Component Guard Board Shape Component Guard Top Solder Dimension		
Engineer: Juan Del Pino Mena		
Date: 2024-08-11	Revision: 0.4	Size: A4



Layer	Name	Material	Thickness	Constant	Gerber
	Top Overlay				GTO
	Top Solder	SM-001	0.025mm	4	GTS
1	Top	CF-003	0.018mm		GTL
	PP-top	PP-008	0.220mm	4.1	
2	GND-1	CF-004	0.035mm		GP1
	Core 1	Core-009	0.350mm	4.5	
3	Layer 1	CF-004	0.035mm		G1
	PP-mid	PP-008	0.220mm	4.1	
4	Layer 2	CF-004	0.035mm		G2
	Core 2	Core-009	0.350mm	4.5	
5	GND-2	CF-004	0.035mm		GP2
	PP-bottom	PP-008	0.220mm	4.1	
6	Bottom	CF-003	0.018mm		GBL
	Board Layer Stack Bottom Solder	SM-001	0.025mm	4	GBS
	Board Layer Stack Bottom Overlay				GBO

Total board thickness: 1.586mm

Pluton UPV		PLUTON
Project: Estigia Comms Payload - Cubesat carrier		
Layer: Board Shape, Board Layer Stack Bottom Overlay, Board Layer Stack Bottom Solder		
Engineer: Juan Del Pino Mena		
Date: 2024-08-11	Revision: 0.4	Size: A4



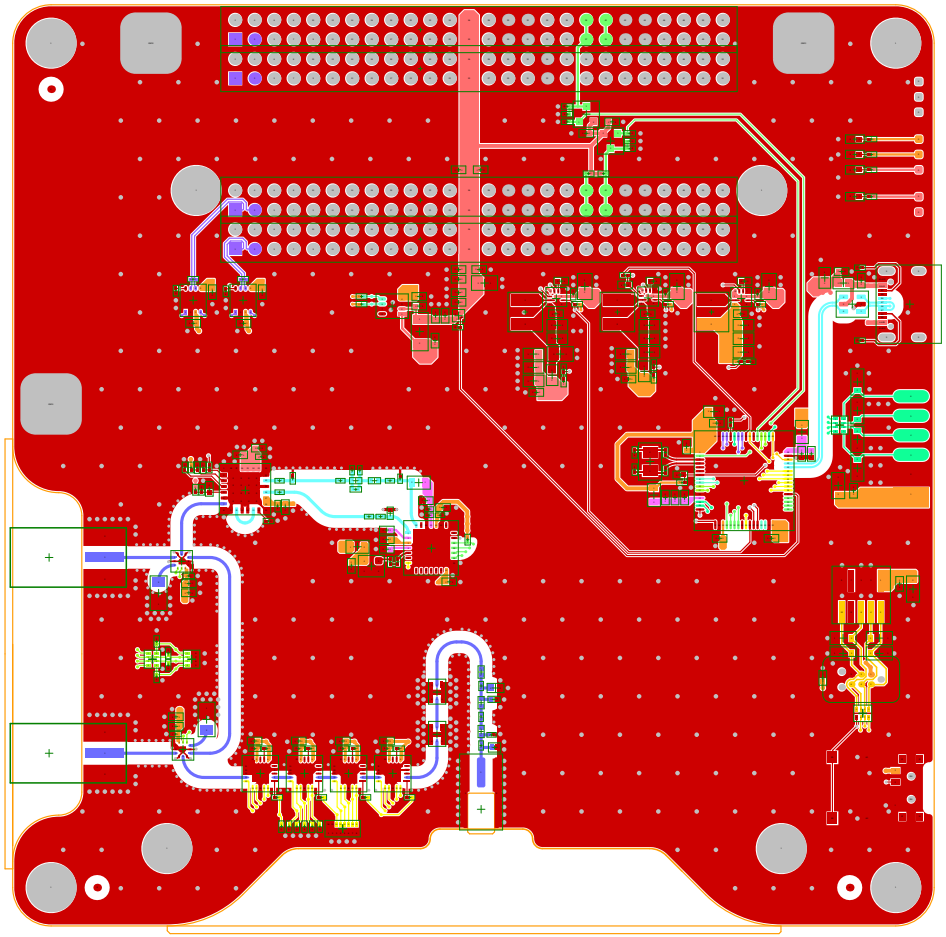
Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template
◎	397	0.200mm	PTH	Round	Top - Bottom	Via	Rounded	(Mixed)
□	323	0.300mm	PTH	Round	Top - Bottom	(Mixed)	(Mixed)	(Mixed)
☆	2	0.650mm	NPTH	Round	Top - Bottom	Pad	Rounded	c65hn65m65p0
○	5	0.900mm	NPTH	Round	Top - Bottom	Pad	Rounded	(Mixed)
▽	104	1.000mm	PTH	Round	Top - Bottom	Pad	(Mixed)	(Mixed)
◇	4	1.100mm	NPTH	Round	Top - Bottom	Pad	Rounded	c110hn110m110p0
⌖	2	1.400mm	PTH	Slot	Top - Bottom	Pad	Rounded Rectangle	r100_180h140_60r50m100_180p0
⊠	4	1.600mm	NPTH	Round	Top - Bottom	Pad	Rounded	c160hn160m160p0
⌑	2	1.700mm	PTH	Slot	Top - Bottom	Pad	Rounded Rectangle	r100_210h170_60r50m100_210p0
⧈	4	3.200mm	PTH	Round	Top - Bottom	Pad	Rounded	c640h320_503323056
	847 Total							

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

Layer	Name	Material	Thickness	Constant	Gerber
	Top Overlay				GTO
	Top Solder	SM-001	0.025mm	4	GTS
1	Top	CF-003	0.018mm		GTL
	PP-top	PP-008	0.220mm	4.1	
2	GND-1	CF-004	0.035mm		GP1
	Core 1	Core-009	0.350mm	4.5	
3	Layer 1	CF-004	0.035mm		G1
	PP-mid	PP-008	0.220mm	4.1	
4	Layer 2	CF-004	0.035mm		G2
	Core 2	Core-009	0.350mm	4.5	
5	GND-2	CF-004	0.035mm		GP2
	PP-bottom	PP-008	0.220mm	4.1	
6	Bottom	CF-003	0.018mm		GBL
	Board Layer Stack Bottom Solder	SM-001	0.025mm	4	GBS
	Board Layer Stack Bottom Overlay				GBO

Total board thickness: 1.586mm

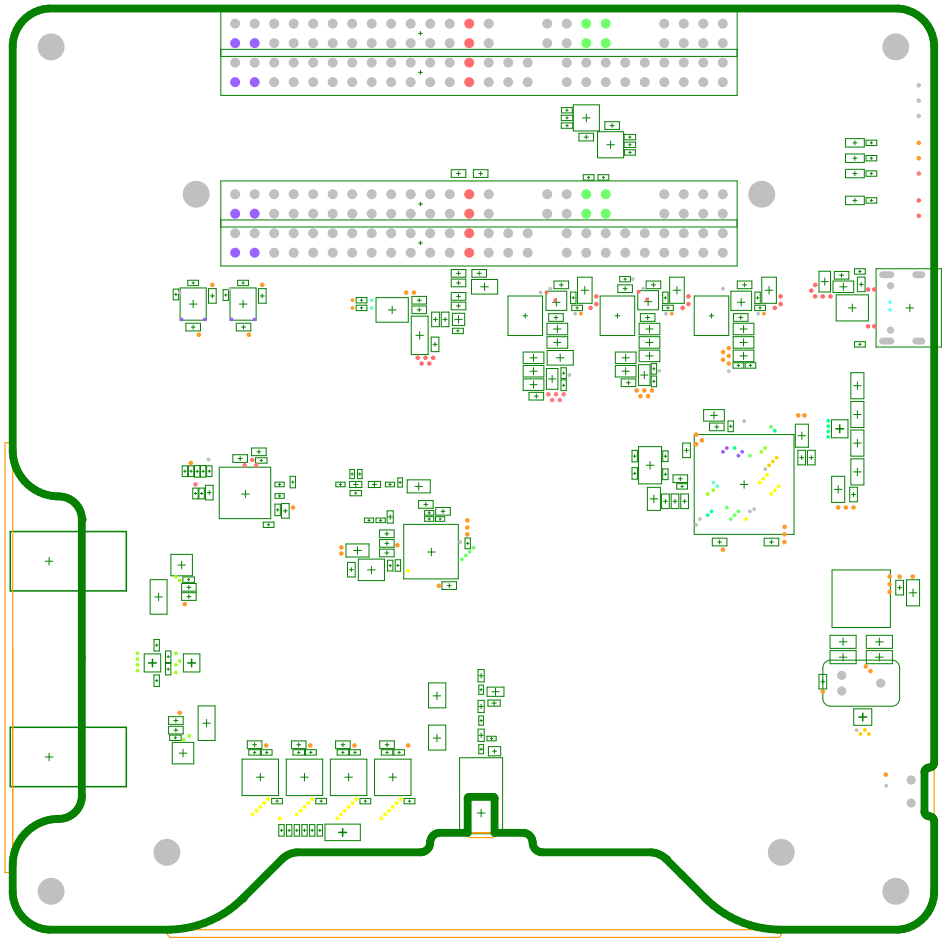
Pluton UPV		PLUTON
Project: Estigia Comms Payload - Cubesat carrier		
Layer: Board Shape Component Guard Drill Drawing Drill Guide Dimension		
Engineer: Juan Del Pino Mena		
Date: 2024-08-11	Revision: 0.4	Size: A4



Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.025mm	4	
1	Top Layer	CF-004	0.018mm		
	Dielectric-1	PP-006	0.220mm	4.1	
2	GND-1	CF-004	0.035mm		
	Core-1	Core-035	0.350mm	4.7	
3	INT-SIG-1	CF-004	0.035mm		
	Dielectric-2	PP-006	0.220mm	4.1	
4	INT-SIG-2	CF-004	0.035mm		
	Core-2	Core-035	0.350mm	4.7	
5	GND-2	CF-004	0.035mm		
	Dielectric-3	PP-006	0.220mm	4.1	
6	Bottom Layer	CF-004	0.018mm		
	Bottom Solder	SM-001	0.025mm	4	
	Bottom Overlay				

Total board thickness: 1.586mm

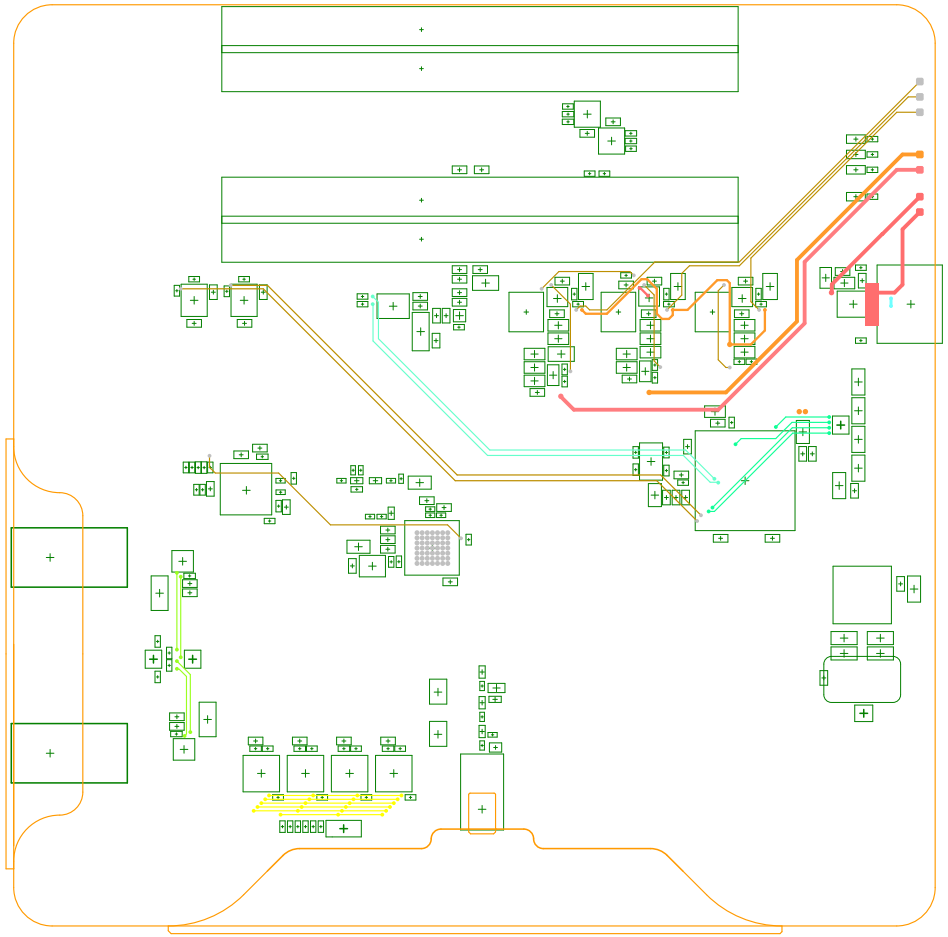
Pluton UPV		
Project: Estigia LoRa Comms PL - mPCIe SoM		
Layer: Board Shape Component Guard Component Guard Dimension		
Engineer: Juan Del Pino Mena		
Date: 2024-09-03	Revision: 0.3	Size: A4



Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.025mm	4	
1	Top Layer	CF-004	0.018mm		
	Dielectric-1	PP-006	0.220mm	4.1	
2	GND-1	CF-004	0.035mm		
	Core-1	Core-035	0.350mm	4.7	
3	INT-SIG-1	CF-004	0.035mm		
	Dielectric-2	PP-006	0.220mm	4.1	
4	INT-SIG-2	CF-004	0.035mm		
	Core-2	Core-035	0.350mm	4.7	
5	GND-2	CF-004	0.035mm		
	Dielectric-3	PP-006	0.220mm	4.1	
6	Bottom Layer	CF-004	0.018mm		
	Bottom Solder	SM-001	0.025mm	4	
	Bottom Overlay				

Total board thickness: 1.586mm

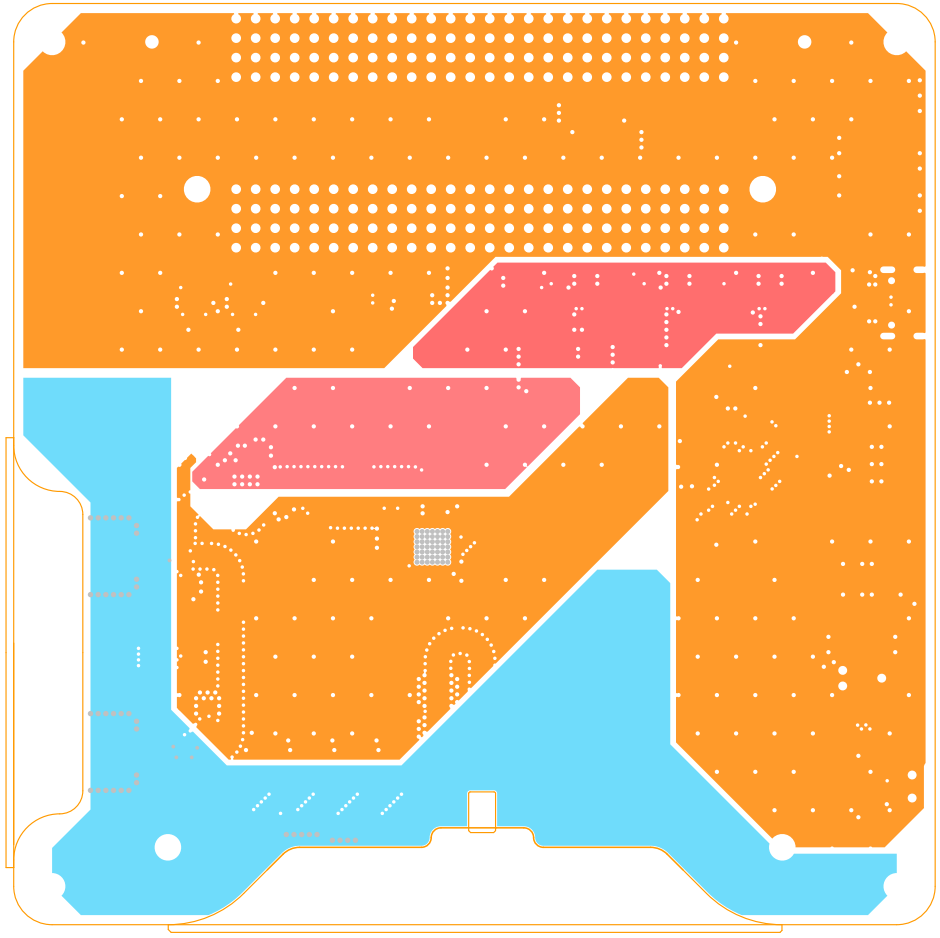
Pluton UPV		
Project: Estigia LoRa Comms PL - mPCIe SoM		
Layer: Board Shape Component Guard Component Guard Dimension		
Engineer: Juan Del Pino Mena		
Date: 2024-09-03	Revision: 0.3	Size: A4



Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.025mm	4	
1	Top Layer	CF-004	0.018mm		
	Dielectric-1	PP-006	0.220mm	4.1	
2	GND-1	CF-004	0.035mm		
	Core-1	Core-035	0.350mm	4.7	
3	INT-SIG-1	CF-004	0.035mm		
	Dielectric-2	PP-006	0.220mm	4.1	
4	INT-SIG-2	CF-004	0.035mm		
	Core-2	Core-035	0.350mm	4.7	
5	GND-2	CF-004	0.035mm		
	Dielectric-3	PP-006	0.220mm	4.1	
6	Bottom Layer	CF-004	0.018mm		
	Bottom Solder	SM-001	0.025mm	4	
	Bottom Overlay				

Total board thickness: 1.586mm

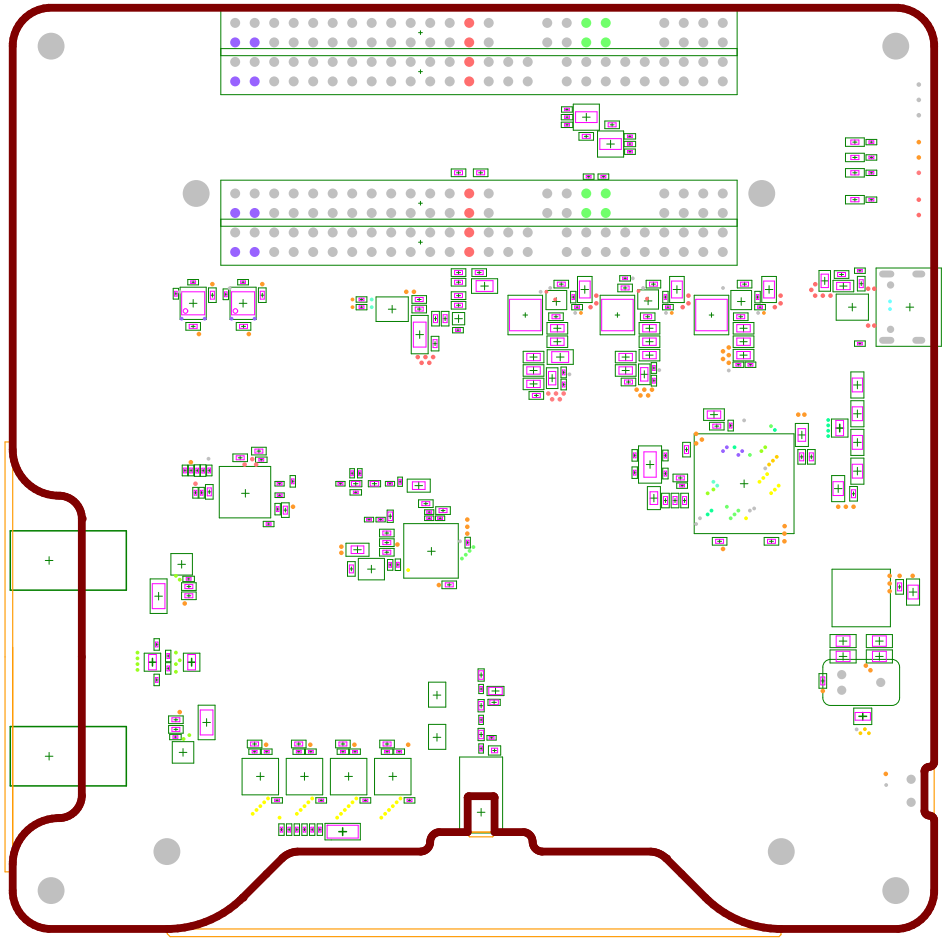
Pluton UPV		
Project: Estigia LoRa Comms PL - mPCIe SoM		
Layer: Board Shape Component Guard Component Guard Dimension		
Engineer: Juan Del Pino Mena		
Date: 2024-09-03	Revision: 0.3	Size: A4



Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.025mm	4	
1	Top Layer	CF-004	0.018mm		
	Dielectric-1	PP-006	0.220mm	4.1	
2	GND-1	CF-004	0.035mm		
	Core-1	Core-035	0.350mm	4.7	
3	INT-SIG-1	CF-004	0.035mm		
	Dielectric-2	PP-006	0.220mm	4.1	
4	INT-SIG-2	CF-004	0.035mm		
	Core-2	Core-035	0.350mm	4.7	
5	GND-2	CF-004	0.035mm		
	Dielectric-3	PP-006	0.220mm	4.1	
6	Bottom Layer	CF-004	0.018mm		
	Bottom Solder	SM-001	0.025mm	4	
	Bottom Overlay				

Total board thickness: 1.586mm

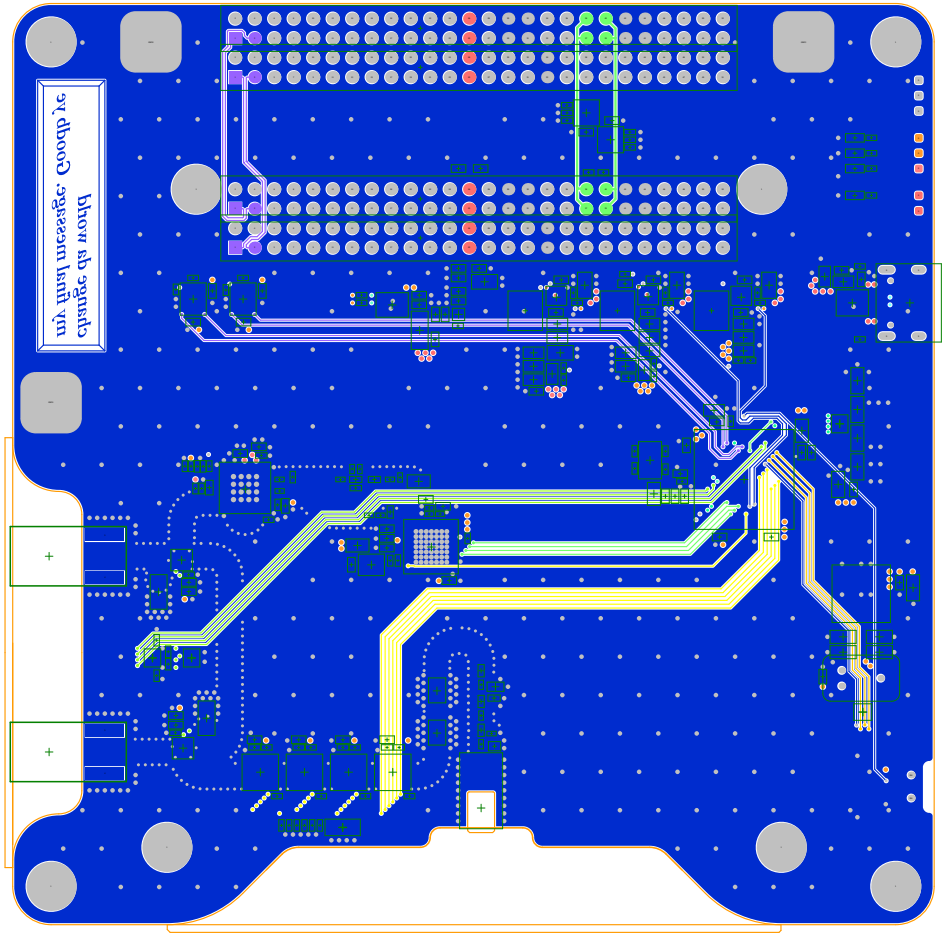
Pluton UPV		
Project: Estigia LoRa Comms PL - mPCIe SoM		
Layer: Board Shape INT-SIG-2 Dimension		
Engineer: Juan Del Pino Mena		
Date: 2024-09-03	Revision: 0.3	Size: A4



Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.025mm	4	
1	Top Layer	CF-004	0.018mm		
	Dielectric-1	PP-006	0.220mm	4.1	
2	GND-1	CF-004	0.035mm		
	Core-1	Core-035	0.350mm	4.7	
3	INT-SIG-1	CF-004	0.035mm		
	Dielectric-2	PP-006	0.220mm	4.1	
4	INT-SIG-2	CF-004	0.035mm		
	Core-2	Core-035	0.350mm	4.7	
5	GND-2	CF-004	0.035mm		
	Dielectric-3	PP-006	0.220mm	4.1	
6	Bottom Layer	CF-004	0.018mm		
	Bottom Solder	SM-001	0.025mm	4	
	Bottom Overlay				

Total board thickness: 1.586mm

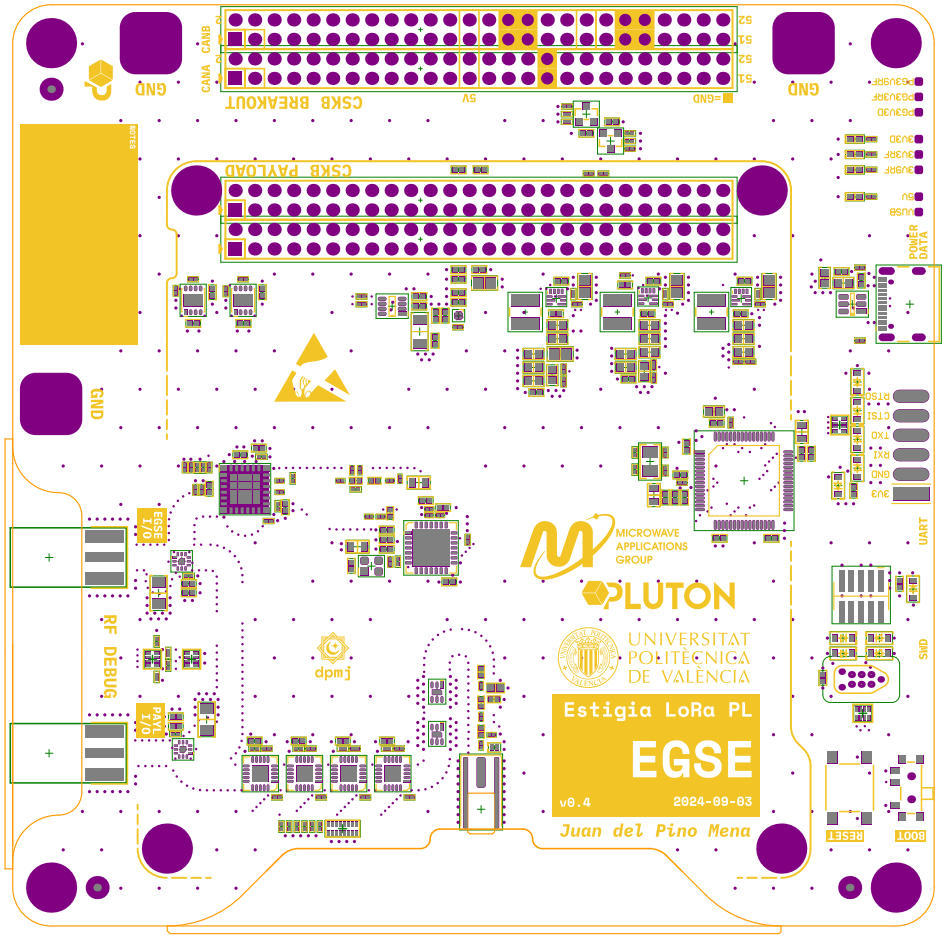
Pluton UPV		
Project: Estigia LoRa Comms PL - mPCIe SoM		
Layer: Board Shape Component Guard Component Guard Dimension		
Engineer: Juan Del Pino Mena		
Date: 2024-09-03	Revision: 0.3	Size: A4



Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.025mm	4	
1	Top Layer	CF-004	0.018mm		
	Dielectric-1	PP-006	0.220mm	4.1	
2	GND-1	CF-004	0.035mm		
	Core-1	Core-035	0.350mm	4.7	
3	INT-SIG-1	CF-004	0.035mm		
	Dielectric-2	PP-006	0.220mm	4.1	
4	INT-SIG-2	CF-004	0.035mm		
	Core-2	Core-035	0.350mm	4.7	
5	GND-2	CF-004	0.035mm		
	Dielectric-3	PP-006	0.220mm	4.1	
6	Bottom Layer	CF-004	0.018mm		
	Bottom Solder	SM-001	0.025mm	4	
	Bottom Overlay				

Total board thickness: 1.586mm

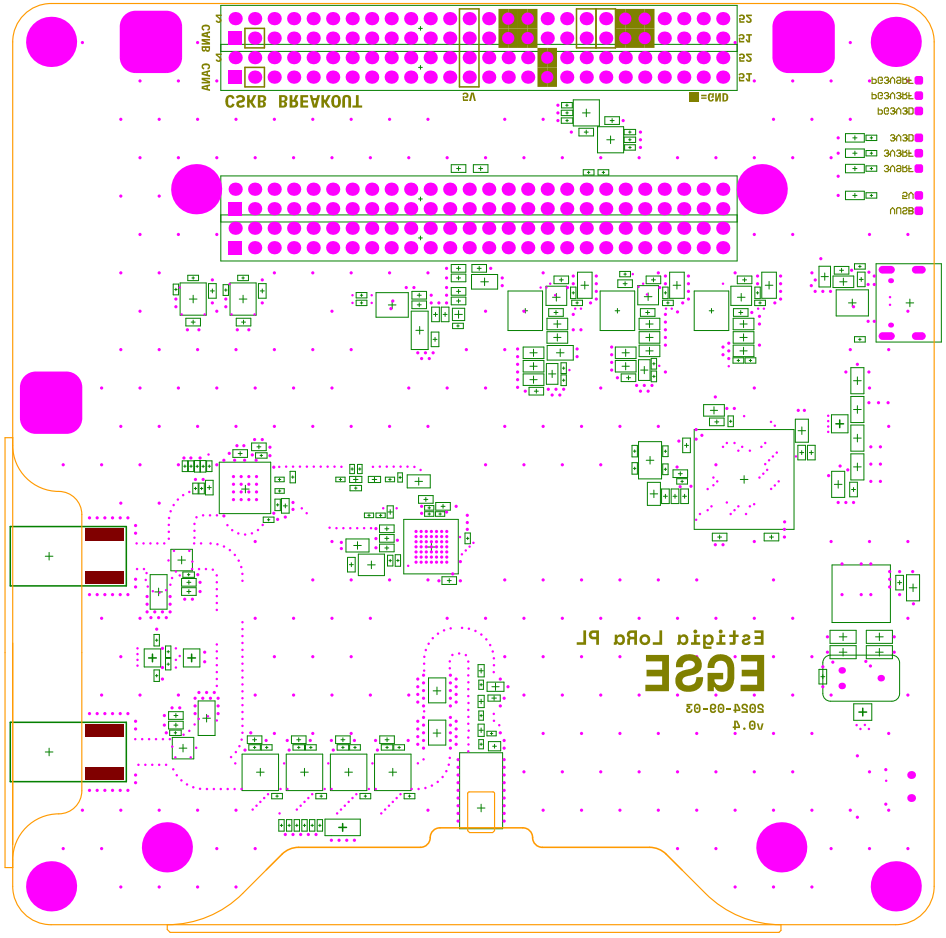
Pluton UPV		
Project: Estigia LoRa Comms PL - mPCIe SoM		
Layer: Board Shape Component Guard Component Guard Dimension		
Engineer: Juan Del Pino Mena		
Date: 2024-09-03	Revision: 0.3	Size: A4



Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.025mm	4	
1	Top Layer	CF-004	0.018mm		
	Dielectric-1	PP-006	0.220mm	4.1	
2	GND-1	CF-004	0.035mm		
	Core-1	Core-035	0.350mm	4.7	
3	INT-SIG-1	CF-004	0.035mm		
	Dielectric-2	PP-006	0.220mm	4.1	
4	INT-SIG-2	CF-004	0.035mm		
	Core-2	Core-035	0.350mm	4.7	
5	GND-2	CF-004	0.035mm		
	Dielectric-3	PP-006	0.220mm	4.1	
6	Bottom Layer	CF-004	0.018mm		
	Bottom Solder	SM-001	0.025mm	4	
	Bottom Overlay				

Total board thickness: 1.586mm

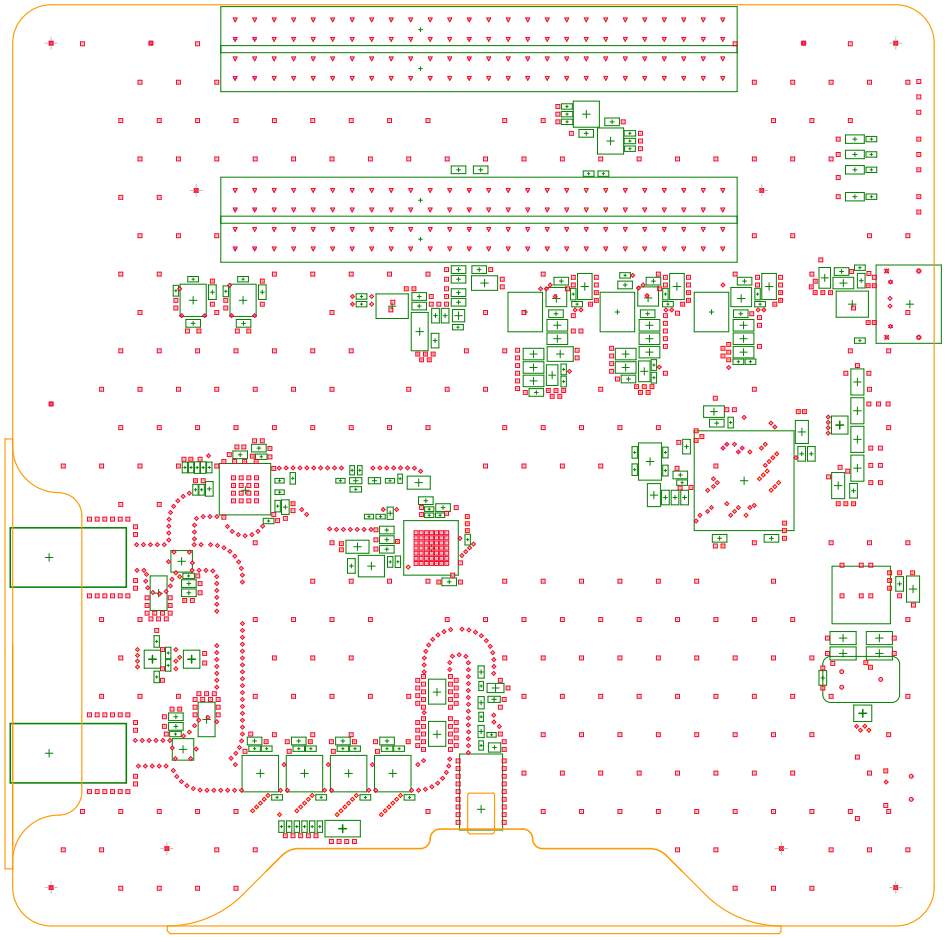
Pluton UPV		
Project: Estigia LoRa Comms PL - mPCIe SoM		
Layer: Board Shape Component Guard Top Solder Dimension		
Engineer: Juan Del Pino Mena		
Date: 2024-09-03	Revision: 0.3	Size: A4



Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.025mm	4	
1	Top Layer	CF-004	0.018mm		
	Dielectric-1	PP-006	0.220mm	4.1	
2	GND-1	CF-004	0.035mm		
	Core-1	Core-035	0.350mm	4.7	
3	INT-SIG-1	CF-004	0.035mm		
	Dielectric-2	PP-006	0.220mm	4.1	
4	INT-SIG-2	CF-004	0.035mm		
	Core-2	Core-035	0.350mm	4.7	
5	GND-2	CF-004	0.035mm		
	Dielectric-3	PP-006	0.220mm	4.1	
6	Bottom Layer	CF-004	0.018mm		
	Bottom Solder	SM-001	0.025mm	4	
	Bottom Overlay				

Total board thickness: 1.586mm

Pluton UPV		
Project: Estigia LoRa Comms PL - mPCIe SoM		
Layer: Board Shape, Bottom Paste, Bottom Solder, Top Overlay, Bottom Overlay, Dimension		
Engineer: Juan Del Pino Mena		
Date: 2024-09-03	Revision: 0.3	Size: A4



Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.025mm	4	
1	Top Layer	CF-004	0.018mm		
	Dielectric-1	PP-006	0.220mm	4.1	
2	GND-1	CF-004	0.035mm		
	Core-1	Core-035	0.350mm	4.7	
3	INT-SIG-1	CF-004	0.035mm		
	Dielectric-2	PP-006	0.220mm	4.1	
4	INT-SIG-2	CF-004	0.035mm		
	Core-2	Core-035	0.350mm	4.7	
5	GND-2	CF-004	0.035mm		
	Dielectric-3	PP-006	0.220mm	4.1	
6	Bottom Layer	CF-004	0.018mm		
	Bottom Solder	SM-001	0.025mm	4	
	Bottom Overlay				

Total board thickness: 1.586mm

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template	Description	Hole Tolerance (+)	Hole Tolerance (-)
	2	0.650mm	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c65hn65m65p0			
	2	1.400mm	PTH	Slot	Top Layer - Bottom Layer	Pad	Rounded Rectangle	r100_180h140_60r50m100_180p0			
	2	1.700mm	PTH	Slot	Top Layer - Bottom Layer	Pad	Rounded Rectangle	r100_210h170_60r50m100_210p0			
	3	1.500mm	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded Rectangle	s800h150r200			
	5	0.900mm	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded	(Mixed)			
	8	3.200mm	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c640h320_503323056			
	208	1.000mm	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)			
	332	0.200mm	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	(Mixed)	(Mixed)		
	691	0.300mm	PTH	Round	Top Layer - Bottom Layer	(Mixed)	(Mixed)	(Mixed)	(Mixed)		
	1253 Total										

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

Pluton UPV		
Project: Estigia LoRa Comms PL - mPCIe SoM		
Layer: Board Shape Component Guard Drill Drawing Drill Guide Dimension		
Engineer: Juan Del Pino Mena		
Date: 2024-09-03	Revision: 0.3	Size: A4