OMHI 2012: First International Workshop on On-chip Memory Hierarchies and Interconnects: Organization, Management and Implementation

Julio Sahuquillo, María E. Gómez, and Salvador Petit

Universitat Politècnica de València, Spain

Foreword

Current CMPs include high amounts of on-chip memory storage, organized either as caches or main memory to avoid the huge latencies of accessing off-chip DRAM memory. To address internal data access latencies, a fast on-chip network interconnects the memory hierarchy within the processor chip. As a consequence, performance, area, and power consumption of current chip multiprocessors (CMPs) are highly dominated by the on-chip memory hierarchy and interconnect design. This problem aggravates with the increasing number of cores since a wider and likely deeper on-chip memory hierarchy is required.

Regarding implementation, on-chip cache hierarchies have been typically built employing Static Random Access Memory (SRAM) technology, which is the fastest existing electronic memory technology. However, for current and future technology nodes SRAM presents important design challenges in terms of density and leakage currents as well as manufacturing variation issues, so that it is unlikely the implementation of future cache hierarchies using only SRAM, especially in the context of chip multiprocessors (CMPs). Instead, alternative technologies (e.g. eDRAM or MRAM), which are less prone to failures and address leakage as well as density by design, are being explored in large CMPs.

To take advantage of these complex hierarchies, efficient management is required. This includes, among others, thread allocation policies, cache management strategies, and NoC designs, both in 2D and 3D, involving heterogeneous technologies for memory storage and NoC communications.

The goal of the OMHI workshop is to be a forum for engineers and scientists to address the aforementioned challenges, and to present new ideas for future on-chip memory hierarchies and interconnects focusing on organization, management and implementation.

The contributions of this year nicely reflect the three key points of the workshop?s spectrum. The organizers of the workshop would like to thank all the authors for all their very interesting contributions. In this edition, we were able to accept six submissions that were grouped in two sessions. In addition, the organizers were proud to present Professor Ramon Canal as keynote speaker, who gave a interesting talk focusing on the key topics of the workshop entitled "The Memory Hierarchy in the Many-Core Era: Friend or Foe?" which jointly with the paper sessions finally resulted in a nice and very exciting one-day program.

The chairs would like to thank the Euro-Par organizers, the members of the program committee for their reviews and feedback, Ramon Canal and the high number of attendees. Based on the positive feedback of all of them, we plan to continue the OMHI workshop in conjunction with Euro-Par 2013.

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Julio Sahuquilo
María E. Gómez
Salvador Petit