Efficient and Accurate Design of Passive Devices in Substrate Integrated Waveguide Technology and their Tapered Transitions from Microstrip Lines

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Abstract

In this paper, a strategy for the efficient design of passive devices in substrate integrated waveguide (SIW) technology is presented and validated with the analysis of several devices and the real design of filters in different topologies. In addition, a procedure for accurately designing tapered microstrip-to-substrate integrated waveguide transitions is described.

Keywords: Design strategy, substrate integrated waveguide, tapered transitions, EM analysis, microwave filters.

1. Introduction

THE interest on the relatively new type of transmission line called Substrate Integrated Waveguide (SIW) is constantly increasing. In such a circuit, the vertical walls of a traditional waveguide are emulated by two rows of metallic posts embedded in a dielectric substrate, which is covered with conducting sheets on the top and bottom sides. This low cost realization of the traditional waveguide circuit inherits the merits from both the microstrip for easy integration and the waveguide for low radiation loss. Furthermore, it is possible to use this new technology for making many devices such as antennas, filters, multiplexers, etc [1]–[3]. For these reasons, the efficient analysis and design of SIW devices becomes a new challenge that is being object of intense research in the last few years [4].

The design strategy here presented relies on three main pillars: efficient and good designs of filters in waveguide technology using the full-wave electromagnetic software simulation tool called FEST3D [5], mapping from the waveguide design to SIW technology, and efficient SIW simulation tool for the optimization phase. This SIW simulation tool is based on a new hybrid technique plus fast frequency sweep for the efficient and accurate analysis of SIW devices [6].

This hybrid design procedure has been tested with the design of several microwave filters with different specifications and topologies. Particularly, four SIW filters have been designed using different coupling structures: two posts, decentered posts and H-plane irises. In all cases a good design that fulfills the specifications has been efficiently obtained. The results prove the efficiency and accuracy of the design process, thus encouraging its future use for designing filters in these or other topologies.

However, in order to connect active circuits to SIW or to measure S-parameters, mounting SMA connectors and a microstrip to SIW transition is

required (see Fig.1). A commercial electromagnetic simulation tool (HFSS) has been used to simulate the microstrip transitions, whereas the hybrid method of [6] has been employed for the analysis of the SIW part of the structure.

In [7] a general equation to design the width W of the taper is proposed. However, the criterion for selecting the best length L could be improved. A previous study in order to calculate a theoretical value of L and W is highly interesting, as it will be useful as an initial point prior to the optimization. In this paper, a theoretical improvement of [8] which uses the small reflection approximation, different tapered shapes [9] and a new design strategy are proposed. This design strategy consists on several phases. First of all, the circuit will be split into three parts as shown in Fig. 1. This will be followed with the calculation of the initial point with the new design equations, a parametric analysis in the surrounding points of the initial point and a final optimization phase with a full-wave simulator. Afterwards, the frequency response of the central part will be calculated with the hybrid method for SIW analysis described in [6] and, finally, a cascade connection of the scattering matrices of the three different blocks will be done with an efficient technique [10].

2. Designs in waveguide technology

Filter design in rectangular waveguide is a field in which our research group has a mature experience, having developed, or helping to develop highly efficient and accurate analysis and design techniques and tools, such as the full-wave electromagnetic software simulation tool called FEST3D [5].

FEST3D is an efficient software tool for the accurate analysis and synthesis of passive components based on waveguide technology including high power effects. Its synthesis capabilities include low-pass, band-pass and dual-mode filter synthesis. This software obtains fast and accurate results because it is basically based on an integral equation technique efficiently solved by the Method of Moments. Additionally, the Boundary Integral-Resonant Mode Expansion (BI-RME) method is employed for extracting the modal chart of complex waveguides with arbitrary cross-section. The combination of such methods ensures a high degree of accuracy, as well as reduced computational resources (in terms of CPU time and memory).

On this basis, FEST3D is able to simulate complex passive devices in extremely short times, of the order of seconds or few minutes, whereas general purpose software, based on segmentation techniques such as finite elements or finite differences, can spend hours for the same calculations.

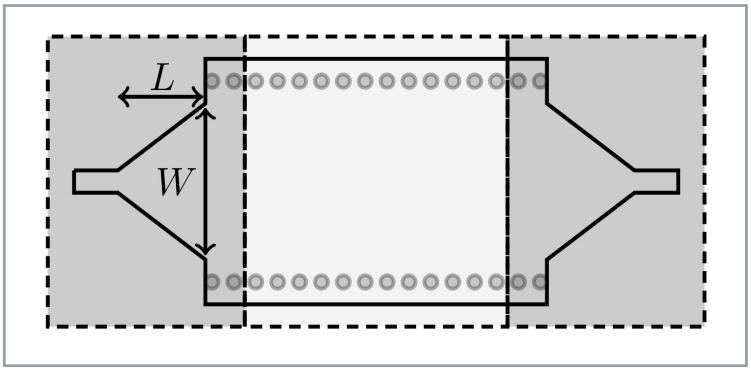

Figure 1. *Microstrip tapered waveguide*

Moreover, unlike mode-matching techniques, the electromagnetic algorithms employed in FEST3D minimize the problems of relative convergence leading to more confident results. Furthermore, the integral equation technique extracts part of the frequency dependent computations, thus allowing a lower computational time per frequency point when compared to standard mode-matching techniques.

In order to take advantage of such a good tool and the high knowledge and experience on the field of waveguide design, we have used FEST3D to obtain an initial point for the final SIW design.

It has been demonstrated that attenuation and dispersion characteristics in SIW are almost identical to its equivalent rectangular waveguide [11] [12] (see section III and Fig. 5). Thanks to it, it is quite easy to reuse some of the existent modeling and designing techniques for filters in rectangular waveguide when dealing with filters in SIW technology.

Proceeding in this way, the initial objective of designing four SIW filters with different specifications and topologies, whose layouts can be seen in Fig. 3, has been initially approached by designing their equivalent filters in waveguide technology (Fig. 2).

Table 1 shows the specifications for the four designs that are going to be presented, where N is the order of the filter, f0 is the central frequency, RL are the return losses in dB, BW is the relative fractional bandwidth, Att. is the out-band attenuation in dB (required at 6.5 and 7.5 GHz) and, finally, d is the diameter of the metallic rods in the SIW device (and so it is in the equivalent rectangular waveguide). At this point, in order to use the FEST3D toolbox for passband waveguide filter synthesis, it is necessary to choose a standard waveguide in which the synthesis will be made. According to the range of frequencies of interest, WR-137 has been the selected one.

1 Regarding to FEST3D software tool

The SIW technology is a compromise between waveguide and the classical planar circuits.

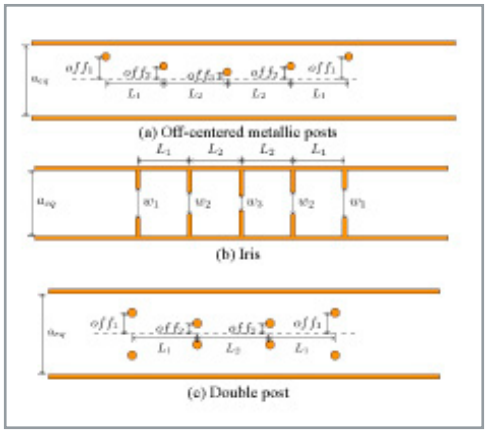

Figure 2. *Layout for the different filters topologies in their equivalent waveguides*

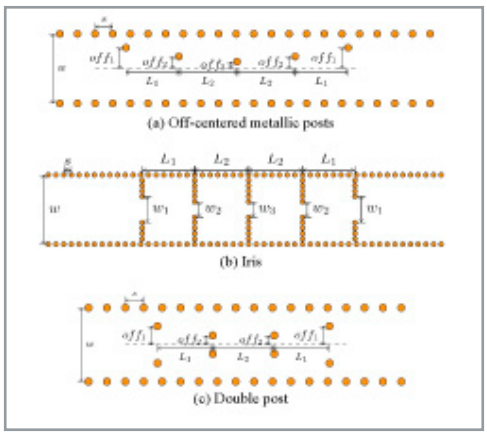

Figure 3. *Layout for the different topologies of SIW filters shown in Table 1*

There is just one detail left so that the software tool can run the synthesis. The possible rod diameters for a SIW device must belong to a discrete range due to the commercial drills available. So it is in the previous waveguide design that it is necessary to fix the diameter of the metallic posts so that in the SIW mapping stage the proper diameter is obtained. With this purpose, the first mapping expression will be introduced:

$$dim = dim' \cdot \sqrt{\frac{\varepsilon_r^{wav}}{\varepsilon_r^{SIW}}} \tag{1}$$

where *dim'* is any dimension in the waveguide design, ε_r^{wav} is the electric permittivity inside the waveguide (typically equal to 1) and ε_r^{SIW} is the electric permittivity of the substrate used for the SIW implementation of the design. This expression will be used in section III to map any dimension dim' to the correspondent dim in the SIW device, but here it will be used the other way round, calling it inverse mapping.

FILTER SPECIFICATIONS							
	Topolog.	**N**	f_0 (GHz)	L_{ret}(dB)	**% BW**	**Att.**(dB)	d (mm)
Filter a	Off-cent.	4	7	20	5	20	3
Filter b	Iris	4	7	25	3	40	1
Filter c	Double	3	7	25	3	15	3
Filter d	Double	4	7	25	3	25	3

Table 1. *Specifications for four designs of SIW filters.*

The filter implementations in substrate integrated waveguide technology will be made for a substrate Rogers RO4003C™, being ε_r=3.55 the permittivity of the dielectric substrate, *h*=1.524mm (0.060") its height and *tanδ*=0.0027 its loss tangent, and *t*=35μm the covering copper thickness. Consequently, as we are looking for a radius equal to 1.5mm in SIW for filters **a**, **c** and **d**, and using eq. (1), the radius needed for the inner posts in the waveguide synthesis, is 2.826mm.

In filter **b**, the H-plane iris windows will be mapped to two rows of rods (see Fig. 3). So the thickness of the iris in the waveguide synthesis, x', corresponds approximately to the diameter of the rods in SIW (1mm) having done the inverse mapping, which is 1.884mm. Table 2 shows the dimensions of the synthesis results with FEST3D for the four equivalent waveguide filters whose specifications were shown in Table 1.

The design procedure is going to be followed as an example just with Filter **d**, whose transmission and reflection parameters obtained with FEST3D are shown in Fig. 4. The same procedure has been applied for designing filters a, b and c. The computational cost for 450 points of frequency has been just 4 sec, referred to an Intel® Core™ i5-760 Processor (8M Cache, 2.80 GHz).

Filter **a**	L_1'	L_2'	off_1'	off_2'	off_3'	r'
	22.6070	25.4855	7.9654	4.1806	3.2374	2.826
Filter **b**	L_1'	L_2'	w_1'	w_2'	w_3'	x'
	22.7812	25.2289	15.7884	9.7864	8.8703	1.8841
Filter **c**	L_1'	L_2'	off_1'	off_2'	-	r'
	25.4705	28.0089	11.4561	8.7043	-	2.8262
Filter **d**	L_1'	L_2'	off_1'	off_2'	off_3'	r'
	25.8340	28.6519	11.2922	8.4255	7.9401	2.826

Table 2. *Geometry in mm of filter designs in WR-137 (a = 34.85mm × b = 15.799mm)*

3. Mapping from waveguide

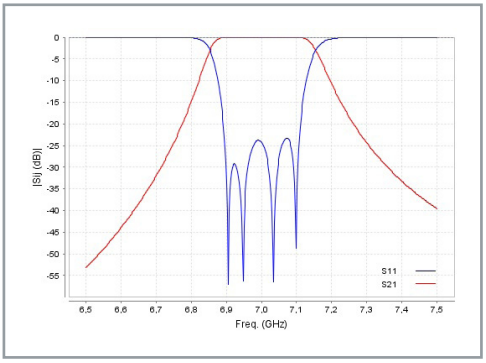

Figure 4. *S-parameters of the H-plane filter design in WR-137 with constant diameter double metallic rods (Filter **d**)*

design to SIW technology

The second stage in the design strategy will be the mapping from the waveguide design to SIW technology (Fig. 5). In order to do so, the well-known restrictions for the correct substrate integrated waveguide design [13] will be followed. If the diameter of the post and the distance between them are chosen properly, the energy leaking between consecutive posts is negligible.

As already mentioned in the previous section, the equivalent rectangular waveguide for a substrate integrated waveguide is one of the main concepts in the mapping procedure, and one of the main pillars of the design strategy here presented. As long as the radiation losses in the SIW structure are negligible, the two rows of via holes of the side walls of the SIW (separated a distance equal to w) can be substituted by authentic metallic walls separated a distance aeq, where aeq is the width of the equivalent rectangular waveguide. These two parameters, a_{eq} and w, are related with the following closed form expression [14],

$$\begin{aligned}\frac{a_{eq}}{w} &= \xi_1 + \frac{\xi_2}{\frac{s}{d} + \frac{\xi_1+\xi_2-\xi_3}{\xi_3-\xi_1}} \\ \xi_1 &= 1.0198 + \frac{0.3465}{\frac{w}{s} - 1.0684} \\ \xi_2 &= -0.1183 - \frac{1.2729}{\frac{w}{s} - 1.2010} \\ \xi_3 &= 1.0082 - \frac{0.9163}{\frac{w}{s} + 0.2152}\end{aligned} \tag{2}$$

where s is the repetition period of the via holes and d is their diameter. The equivalent waveguide width, $a_{eq'}$ can be calculated applying eq. (1)

$$a_{eq} = a' \cdot \sqrt{\frac{1}{3.55}} \tag{3}$$

where a'=34.85 mm (1.372") is the width of the standard rectangular waveguide WR-137 used in the waveguide designs in section II.

Observing (2), it comes out that the correlation between w and a_{eq} is supposed to be independent from the working frequency. But in order to avoid a potential radiation problem some restrictions must be considered [15,13,16]:

where λ_c is the wavenumber inside the SIW

$d < 0.2\lambda_c$	$s \leq 2d$	$s < 0.25\lambda_c$	$s > 0.05\lambda_c$	$s > d$	$\frac{d}{w} < 0.4$	$\frac{w}{s} > 2.5$

Table 3. *Design rules for substrate integrated waveguides.*

dielectric substrate. Once chosen a valid s repetition period (the diameter of the via holes was previously fixed, see Table 1), it is now possible to find the value of w from eq. (2).

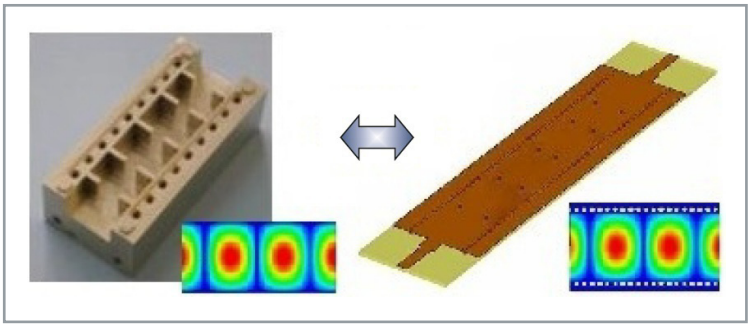

Figure 5. *Electric field distribution in substrate integrated waveguide (right) and in its equivalent rectangular waveguide (left).*

Filter **a**	L_1	L_2	off_1	off_2	off_3	r	s	w
	11.9985	13.5263	4.2276	2.2188	1.7182	1.5	5.3996	20.5673
Filter **b**	L_1	L_2	w_1	w_2	w_3	r	s	w
	13.0910	14.3901	4.1898	2.5970	2.3539	0.5	1.5	19.2698
Filter **c**	L_1	L_2	off_1	off_2	-	r	s	w
	13.5183	14.8656	6.0803	4.6198	-	1.5	5.4	20.5674
Filter **d**	L_1	L_2	off_1	off_2	off_3	r	s	w
	13.7113	15.2068	5.9933	4.4718	4.2142	1.5	5.1	20.6593

Table 4. *Mapping results for the geometry of the four designs.*

However, a parametric sweep in s (recalculating w for every s value) has been done so that the return losses are minimized in the whole bandwidth of interest for the empty substrate integrated waveguide. This previous study has been carried out for the four different designs, and the values of s and w shown in Table 4 are the best matches resulted from it.

At the end of this second stage of the design procedure, the results shown in Table 4 have been obtained for each of the four proposed filters. These values will be the initial points for the last optimization stage.

4. Efficient SIW simulation tool

Some of the recent contributions to the field of the analysis of substrate integrated waveguide devices are based on mode-matching and method of moments hybrid techniques that can be used to analyze any device that is fed through canonical waveguides. In general, those hybrid techniques are formulated by applying the equivalence theorem [17], so that the ports are replaced by a pair of unknown electric and magnetic current densities. A hybrid proposal that uses this pair of currents to achieve the equivalence [18,19] has been successfully applied to the analysis of several SIW [13,15,20] devices. Another recent contribution for the analysis of SIW circuits is based on the Boundary Integral - Resonant Mode Expansion (BI-RME) method [21-24].

We recently presented a Mode-Matching and Method of Moments hybrid technique to efficiently analyze substrate integrated waveguide based devices [25] which includes two different fast frequency sweep schemes to highly accelerate the solution of an arbitrary SIW device [6].

Microstrip to SIW transitions are required in order to measure the SIW device or connect it to active circuits.

In [25], as in [18], the metalized holes conforming the substrate integrated waveguide are characterized by means of cylindrical emergent spectra, implying an important computational advantage. But in [25] the port characterization is based just on a single electric current density, in opposition to the common strategy based on two equivalent sources, a pair of magnetic and electric current densities. This helps to reduce the computational cost, since the computation of the scattering parameters is much simpler, and makes possible the development of a fast sweep scheme in [6] as it includes the emergent modal weights, i.e. the scattering parameters, as unknowns of the method of moments system of equations. In that work, the efficiency and accuracy of a fast frequency sweep developed by means of an asymptotic waveform evaluation (AWE) [26] with the analysis in a single frequency point inside the bandwidth was tested. But also a better approximation of the response was developed for cases in which the bandwidth is so wide that AWE is not enough. It consists on using more than one single point to do this approximation, though the cost is proportionally increased. Those points can be found by using the technique known as complex frequency hopping (CFH) [27].

Thanks to the high efficiency of the method presented in [6] and used to analyze the filter in every optimization step, the last phase in the design process can be approached through direct optimization (using optimization algorithms such as the Nelder-Mead Simplex method and Gauss-Newton). But it is also possible due to the good initial point obtained after the two previous phases.

Step	1^{st}	2^{nd}	3^{rd}	**TOTAL**
Parameter	S_{21} (dB)	S_{11}	S_{11} (dB)	-
Norm	2	2	2	-
Algorithm	N-M Simplex	N-M Simplex	GNA	-
Simulations	101	101	12	210
Points	75	100	300	-
Time (s)	1374	1360	155	2889

Table 5. *Optimization procedure and computational costs of design for Filter d.*

	L_1	L_2	off_1	off_2	off_3
Mapping	13.7113	15.2068	5.9933	4.4718	4.2142
1^{st} **step**	13.7974	15.2219	6.0184	4.4879	4.2189
2^{nd} **step**	13.7125	15.2199	6.0159	4.4854	4.2303
3^{rd} **step**	13.6951	15.2056	6.0121	4.4850	4.2299

Table 6. *Evolution of optimization parameters for Filter* ***d****.*

Filter **a**	L_1	L_2	off_1	off_2	off_3	r	s	w
	11.3731	13.4463	4.4851	2.2030	1.6731	1.5	5.3996	20.5673
Filter **b**	L_1	L_2	w_1	w_2	w_3	r	s	w
	13.03741	14.3030	4.0374	2.4328	2.1945	0.5	1.5	19.2698
Filter **c**	L_1	L_2	off_1	off_2	-	r	s	w
	13.5125	14.8797	6.0953	4.6207	-	1.5	5.4	20.5674
Filter **d**	L_1	L_2	off_1	off_2	off_3	r	s	w
	13.6951	15.2056	6.0121	4.4850	4.2299	1.5	5.1	20.6593

Table 7. *Geometry in mm of the final SIW filter designs in RO4003*^{CTM}.

This technique can be applied to the analysis and design of substrate integrated waveguide devices, and it is highly competitive when compared to other method of moments and mode-matching hybrid formulations or when compared to reference commercial software.

Table 5 shows the optimization strategy steps, and computational costs for Filter d, referred to an Intel® Core™ i7-920 Processor (8M Cache, 2.66 GHz), where GNA stands for the Gauss-Newton algorithm and N-M simplex stands for Nelder-Mead simplex method.

In Table 6, we can observe the evolution of the five optimization parameters for Filter d after each step of the optimization procedure.

Finally, Table 7 and Fig. 6 show, respectively, the dimensions and the S-parameters of the four filters designed with the very efficient and highly accurate strategy presented in this paper. In all cases specifications have been achieved and the frequency responses are very close to their respective ideal Chebyshev one.

5. Improvements In The Design Of Tapered Microstrip-To-SIW Transitions

As already said in the introduction, in order to connect active circuits to SIW devices or to measure S-parameters, it is necessary to design tapered transitions from SIW to microstrip, so that the return losses are minimized. In this work, an improvement to theoretical design expressions is presented and a new design strategy is proposed.

A. The reflection factor with different tapered shapes

The main design parameters are the length, L, and the width, W, of the tapered transition. In [8], a theoretical method for the calculation of W is presented. Once W is known, the impedance Z_2 can be easily calculated by using the general equation of the impedance for a microstrip line [28].

The reflection factor of the transition between Z_1 (usually 50Ω) and Z2 (see Fig. 7) can be obtained by using the following expression [9]

$$\Gamma(\theta) = \frac{1}{2}\int_0^L e^{-2j\beta z}\frac{\mathrm{d}}{\mathrm{d}z} ln\left(\frac{Z}{Z_0}\right)\,\mathrm{d}z \tag{4}$$

In [9] some different impedance variation functions are proposed. Their dependence with the length L is represented in Fig. 8.

Each transition has different advantages and disadvantages respect to the others. Fig. 9 shows the reflection factor obtained for different designs for a transition between two microstrip lines of different impedances. These results are useful as

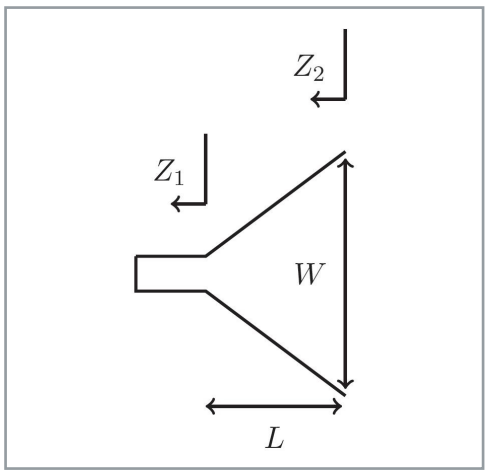

Figure 7. *Geometry of the tapered transition and impedances in the reference planes.*

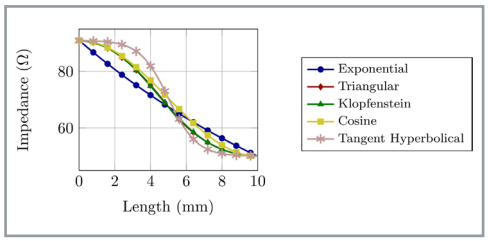

Figure 8. *Impedance vs. length for the analyzed transitions.*

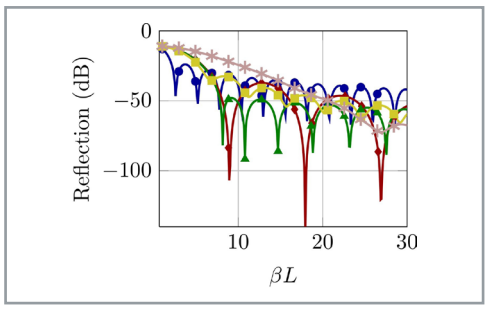

Figure 9. *Return losses vs. electrical length for the analyzed transitions.*

an initial point previous to a full-wave simulation. However, it is just an initial approximation for our transition design between microstrip and SIW, since modes propagating in microstrip lines are quasi-TEM, and we have a substrate integrated waveguide with TE modes propagating.

B. Design strategy

The design strategy to be followed in order to efficiently obtain a taper that minimizes the return losses in the transition between microstrip and substrate integrated waveguide consists of three different phases explained below.

• Initial Point Phase:
Choosing an appropriate initial point is essential in any optimization process. In order to calculate the width of the tapered transition, W, expression in [8] is applied. Figure 9 is used to select the best value for the initial length, L.

• Optimization Phase:
The optimization phase consists of two steps. In the first stage, a parametric analysis will be done by varying W of a microstrip line at the central frequency, in order to select the width that minimizes the return losses at that frequency. This parametric analysis is shown in Figs. 10 and 11 for a straight microstrip line. Furthermore, this width is supposed to be adequate for any kind of SIW device connected to the taper, as long as the substrate integrated waveguide remains the same.

Afterwards, we should run another parametric analysis, this time varying just the length of the transition, L, in order to find its best value (see Fig. 12 for the exponential shaped transition). In the second stage, an optimization using the simplex method will be done, taking the pair of values previously found as initial point. Finally, a multimodal analysis with at least five modes must be done in order to accurately connect the three matrices in the last phase.

• Cascade Connection Phase:
For this last phase, the matrix of the SIW device (see Fig. 1) is needed and, in order to do so, the hybrid method [6] already presented in section is going to be used. If a five modes matrix is obtained, we are prepared to efficiently connect the scattering matrices of the three blocks involved. The efficient technique [10] will be used for that purpose.

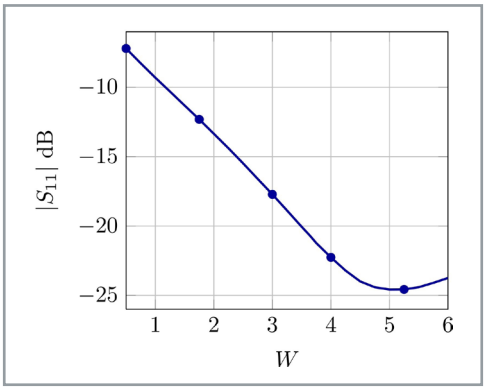

Figure 10. *Return loss vs. width of a straight microstrip line at the central frequency.*

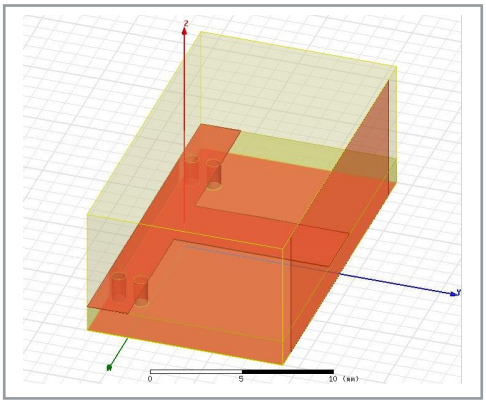

Figure 11. *3D model of a straight microstrip line.*

Equivalent waveguide designs are synthesized with FEST3D.

Some restrictions must be considered so that the potential radiation problem is avoided.

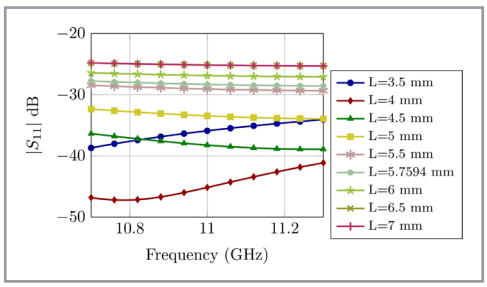

Figure 12. *Return losses for the parametric sweep varying L for the exponential shaped transition*

C. Results

The new design strategy has been successfully applied for designing a new tapered transition for a SIW filter whose characteristics can be found in [6]. This filter, designed for a Rogers RO4003™ substrate, has a central frequency f_0=11 GHz, and a bandwidth BW=600 MHz. Nevertheless, the same procedure can be used for the design of the transitions needed for any other device in SIW technology, such as the four filters previously presented.

The width of a 50 Ω microstrip line to the central frequency and for this kind of substrate has been calculated with [28], obtaining a width of 3.65 mm. The theoretical approach for W [8] is 2.9096 mm.

The result of the first stage of the optimization phase is shown in Fig. 10. The best value for the width is W=5 mm. The impedance for this width, calculated with [28], is Z_l = 40.7249 Ω. Then we choose a value for βL (Fig. 9) so that it corresponds to the first minimum for each of the five shapes that are going to be studied. Once we have a βL, the theoretical L is calculated with eq. (5).

$$\beta L = \frac{2\pi f}{c_0}\sqrt{\epsilon_r}L \tag{5}$$

Table 8 shows these initial values of L for each transition shape, and also the length suggested in [8], where the criterion followed is independent of the shape (eq. (6)).

$$L_{suggested} = \frac{\lambda}{4} = \frac{c_0}{4f_0\sqrt{\epsilon_r}} \tag{6}$$

$L_{Exp} = 5.7594$ mm	$L_{Cos} = 16.1262$ mm
$L_{Tri} = 19.1211$ mm	$L_{Klop} = 18.4300$ mm
$L_{Tan} = 59.8974$ mm	$L_{suggested} = 3.618$ mm

Table 8. *Initial point values for the transition lengths.*

The final lengths obtained after the optimization process can be seen in Table 9, the simulated return losses of the different tapered transitions are shown in Fig. 13, and the number of simulations needed and the number of frequency points evaluated in each simulation for the whole design strategy in Table 10.

In order to test the new design strategy, a classical transition from microstrip to SIW has

$L_{Exp} = 4.0653$ mm	$L_{Cos} = 4.4349$ mm
$L_{Tri} = 4.2400$ mm	$L_{Klop} = 4.4916$ mm
$L_{Tan} = 4.5002$ mm	

Table 9. *Final length values for the different shapes of tapered transitions.*

$L_{Exp} = 4.0653$ mm	$L_{Cos} = 4.4349$ mm
$L_{Tri} = 4.2400$ mm	$L_{Klop} = 4.4916$ mm
$L_{Tan} = 4.5002$ mm	

Table 10. *Computational costs for the taper design.*

$f = 11$	BW =600 MHz
$\varepsilon_r = 3.55$	$L_{\mu s} = 1.5$
$w_{siw} = 10.767$ mm	$l = 19.5$ mm

Table 11. *Parameters of the fabricated circuit*

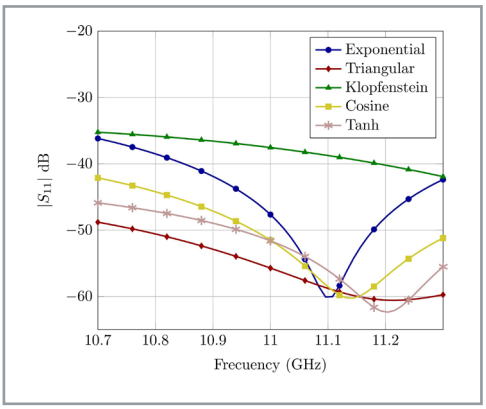

Figure 13. *Simulated return losses for the final design of tapered transitions.*

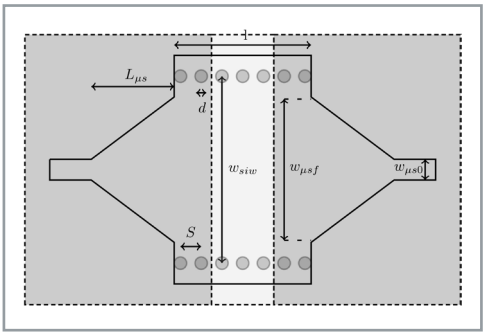

Figure 14. *Schematic of the fabricated circuit*

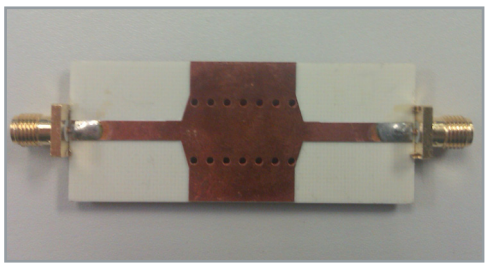

Figure 15. *Fabricated circuit.*

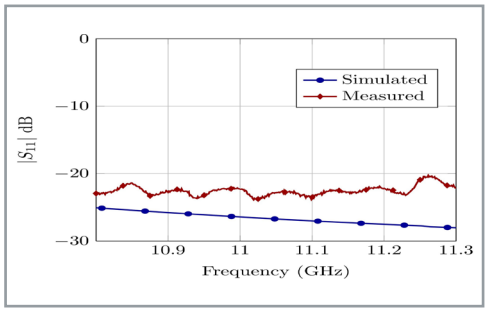

Figure 16. *Comparison between the simulated and measured return losses for the fabricated circuit seen in Fig. 15.*

been designed and the circuit of Fig. 14 has been fabricated (see Fig. 15). The main parameters of this circuit are shown in the table XI. Fig. 16 shows a comparison between measurements and simulated results.

6. Conclusions

A new design procedure for different topologies of filters in substrate integrated waveguide technology has been presented and tested with the design of four filters. It uses the dimensions of an equivalent waveguide design as an initial point. This initial structure in rectangular waveguide is mapped to substrate integrated waveguide technology and finally adjusted with an optimization process that uses a highly efficient simulation tool.

In order to fabricate and measure circuital parameters, a transition from microstrip to SIW must be designed. A new procedure to design transitions with different impedance variation functions has been presented, and the measurements for one of these transitions have been compared with simulated results.

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Biographies

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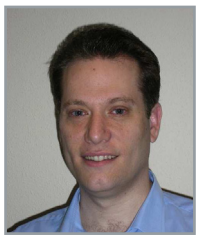

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