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Evaluation of a timing integrated circuit architecture for continuous crystal and SiPM based PET systems

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ABSTRACT: Improving timing resolution in positron emission tomography (PET), thus having fine time information of the detected pulses, is important to increase the reconstructed images signal to noise ratio (SNR) [1]. In the present work, an integrated circuit topology for time extraction of the incoming pulses is evaluated. An accurate simulation including the detector physics and the electronics with different configurations has been developed.

The selected architecture is intended for a PET system based on a continuous scintillation crystal attached to a SiPM array. The integrated circuit extracts the time stamp from the first few photons generated when the gamma-ray interacts with the scintillator, thus obtaining the best time resolution. To get the time stamp from the detected pulses, a time to digital converter (TDC) array based architecture has been proposed as in [2] or [3]. The TDC input stage uses a current comparator to transform the analog signal into a digital signal. Individually configurable trigger levels allow us to avoid false triggers due to signal noise. Using a TDC per SiPM configuration results in a very area consuming integrated circuit. One solution to this problem is to join several SiPM outputs to one TDC. This reduces the number of TDCs but, on the other hand, the first photons will be more difficult to be detected. For this reason, it is important to simulate how the time resolution is degraded when the number of TDCs is reduced. Following this criteria, the best configuration will be selected considering the trade-off between achievable time resolution and the cost per chip.

A simulation is presented that uses Geant4 for simulation of the physics process and, for the electronic blocks, spice and Matlab. The Geant4 stage simulates the gamma-ray interaction with the scintillator, the photon shower generation and the first stages of the SiPM. The electronics simulation includes an electrical model of the SiPM array and all the integrated circuitry that generates the time stamps. Time resolution results are analyzed using Matlab. The goal is to analyze the best resolution achievable with the SiPM and its degradation due to different circuitry configurations.

KEYWORDS: Gamma camera, SPECT, PET PET/CT, coronary CT angiography (CTA); Timing detectors; Electronic detector readout concepts (solid-state); Front-end electronics for detector readout

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Contents

1 Timing integrated circuit architecture

Improving timing resolution in positron emission tomography (PET), thus having fine time information of the detected pulses, is important to increase the reconstructed images signal to noise ratio (SNR). The information obtained from a precise time stamp of the detected pulses can be used to reduce false coincidence pulse rate and to perform time of flight PET [1, 4]. The selected topology aims at improving the time resolution of a PET system based on monolithic scintillation crystal detectors attached to SiPM arrays. Best time resolution is obtained from the first photons that have been generated when the gamma-ray interacts with the scintillator. The topology extracts the time stamp from the detected photons by means of a TDC array.

1.1 First photon timing

Considering an electronic and a SiPM detector without timing error there is one source on timing error that cannot be avoided, the scintillator. The statistical fluctuations in the time of emission of the low energy emitted photons due to a gamma ray interaction limit the system time resolution. This time resolution depends on the number of generated or detected photons, the scintillator fall time constant and the photon used for the time extraction. The time resolution is improved when the number of detected photons is high, the scintillator fall time constant is low and when the first detected photons are used for time extraction. For this reason, detecting the first photons is mandatory for TOF-PET.

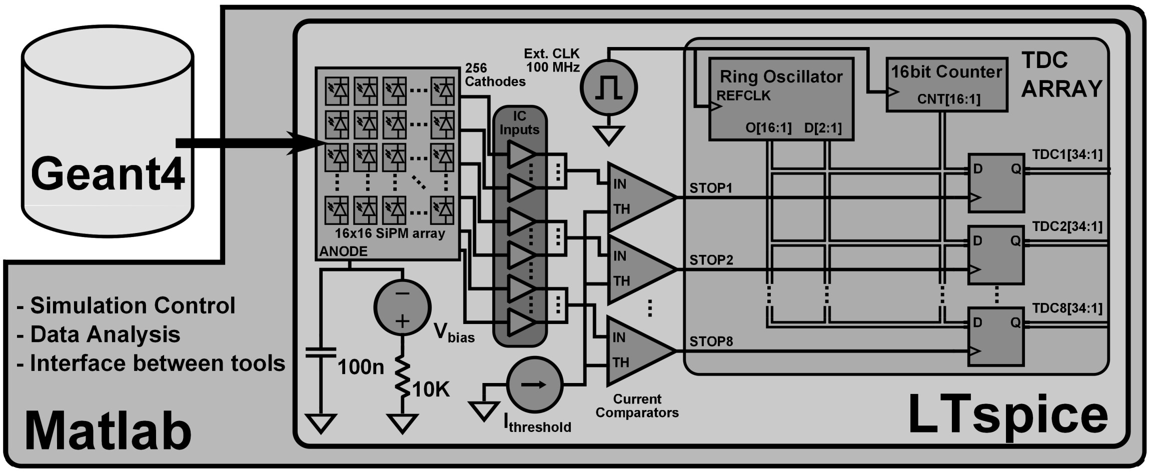

Figure 1. Developed simulation block diagram. The diagram shows the different simulation tools that have been used in each described block.

2 The simulation test bench

The simulation presented here is a mixed simulation that uses a Montecarlo Geant4 based simulator for the physics process and a spice based simulator (LTspice) for the electronic blocks [5]. All the simulation is controlled by Matlab. Matlab transforms the list of photons of each SiPM generated in Geant4 in PWL current sources (Piecewise linear current sources) that are read by the electronic simulator. In figure 1 there is a simulation block diagram showing the different blocks.

The LTspice simulation includes an accurate electrical model of the SiPM array and all the integrated circuitry that generates the time stamps. Each SiPM is attached to one IC input stage. Then, depending on the configuration selected, the signals are combined. The combined signals are compared with a fixed threshold to generate digital signals that are introduced in the TDC array.

2.1 The Geant4 simulation

The Geant4 stage simulates the gamma-ray interaction with the continuous LSO $49 \times 49 \times 10\,\mathrm{mm}^3$ scintillator, the photon shower generation and the first stages of the SiPM. It generates a list of photons that is detected in each of the 256 simulated SiPMs. The 256 SiPMs are distributed in a 16×16 array. The simulated SiPM model is the Hamamatsu s10362-11-050. The simulation considers the PDE (Photon detection efficiency) and the sensitive area due to the 16×16 SiPM array spatial distribution under the surface of the scintillator.

2.2 The SiPM spice model

The SiPM has been described using two different models as can be seen in figure 2. The model A [7] is more accurate than the model B [6, 8]. But the model A cannot be used to simulate several microcells activated at the same time. For this reason, model B has been selected for the LTspice simulation. Model A allows us to calculate the time of the avalanche that occurs when a photon interacts with the SiPM. That time is used in the model B to select the current duration

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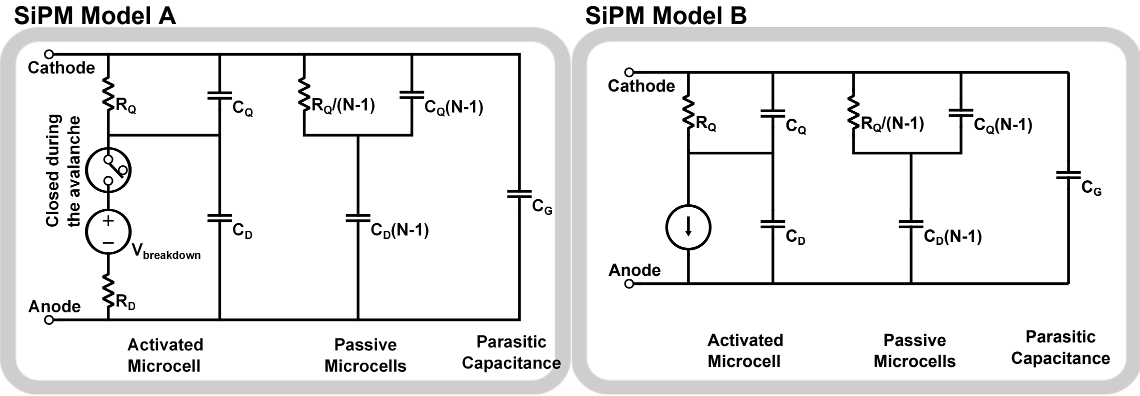

Figure 2. The two different SiPM spice models used at the present work.

when a photon is detected. The current value used for each photon is fixed by:

$$Q = (V_{\text{bias}} - V_{\text{breakdown}})(C_D + C_Q) \tag{2.1}$$

where Q is the charge generated for one photon, V_{bias} is the SiPM bias voltage, $V_{\text{breakdown}}$ is the SiPM breakdown voltage, C_D and C_Q are SiPM spice model parameters. Q determines the area value of the input current pulse from the SiPM spice model. The used parameters for Hamamatsu s10362-11-050 SiPM can be found in [6].

2.3 The proposed time to digital converter (TDC)

The selected architecture for the TDC array is based on a Ring Oscillator. The Ring oscillator is composed by a voltage controlled oscillator based on a delay line of 16 differential delay elements; a phase and frequency detector that evaluates phase and frequency variations between the generated clock and the reference external 100 MHz clock; and the charge pump, which, depending on the information from the phase and frequency detector, generates a signal that modifies the frequency of the voltage controlled oscillator. At the present work two different configurations are simulated, an 8 channel TDC and a single channel TDC.

3 Simulation results

Two different situations have been simulated:

- Single photon test: it simulates the time resolution obtained from single photons hitting the SiPM with a constant rate.

- Geant4 data test: it simulates a real setup where the SiPM array is attached to a LSO continuous crystal stimulated with a 511 KeV gamma ray point source.

3.1 Single photon test

For this simulation, 2250 single photons were generated with a 300 ms period constant rate. Matlab processes each photon to introduce the jitter error associated to the Hamamatsu s10362-11-050 (300 ps FWHM). Before that, Matlab generates the PWL source for a single SiPM.

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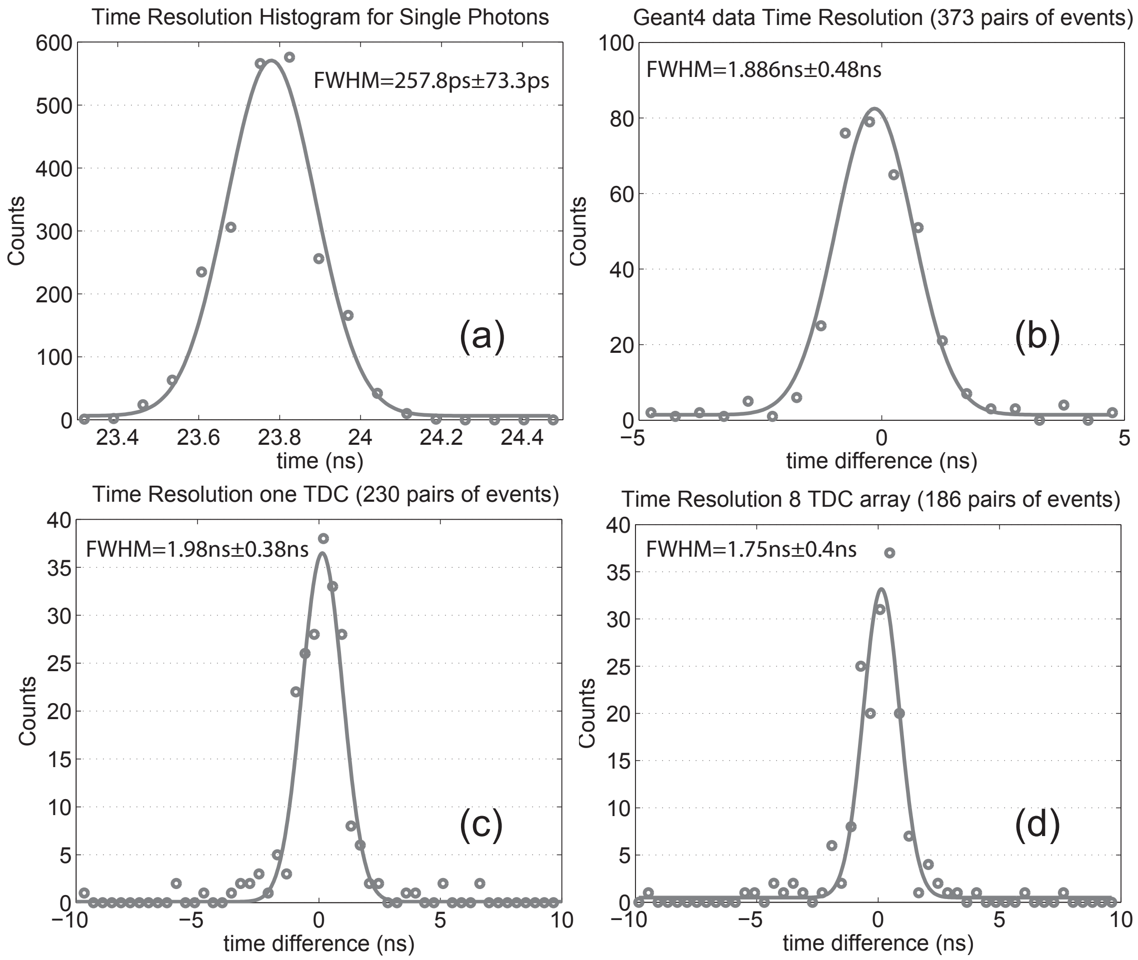

Figure 3. Results of the different test performed on the simulation test bench: (a) results for the single photon test; (b) time resolution of the Geant4 generated events; (c) results for the Geant4 test using a one channel TDC; (d) results for the Geant4 test using an 8 channel TDC.

The constant current threshold for the current comparator was fixed to 1 mA. The threshold is fixed at the minimum possible value over the expected signal noise. The idea was to get the best time resolution achievable with this architecture. For this task, just one of the TDC channels was used. For each photon, one time stamp was obtained. The measured timestamps were analyzed in Matlab. The results show the histogram generated considering the time difference between the generated time stamp and the reference time when the photons were generated.

The measured FWHM time resolution is $257.8\,\text{ps} \pm 73.3\,\text{ps}$, near the expected 300 ps (figure 3(a)).

3.2 Geant4 data test

This simulation evaluates the IC circuit architecture using Geant4 data as an input stimulus. For this simulation, two scenarios have been considered: a 256 SiPM array where all the signals are combined into one signal after the IC input stage and a 256 SiPM array where all the signals are divided in 8 groups of 32 signals. In the second case, the 32 signals of each group are combined into one signal generating the 8 needed signals. The first case evaluates the use of one channel TDC and the second case evaluates the use of an 8 channel TDC array. The comparator current threshold has been set in both cases to 1 mA.

As a reference, the result of the time resolution of the Geant4 data without being processed is FWHM $= 1.886\,\text{ns} \pm 0.48\,\text{ns}$ (figure 3(b)). The results obtained by both configurations follow perfectly the result of the Geant4 generated data. At the one channel TDC, the obtained time resolution was FWHM $= 1.98\,\text{ns} \pm 0.38\,\text{ns}$ (figure 3(c)) and, in the 8 channel TDC, the obtained time resolution was FWHM $= 1.75\,\text{ns} \pm 0.4\,\text{ns}$ (figure 3(d)). For both simulations, a Corei7 CPU with 4 GB RAM has been used. The 8 channel TDC simulation for the 186 pair of events was performed in 32.7 hours. The single channel simulation for the 230 pairs of events was performed in 22.3 hours.

4 Conclusions

As can be seen in the Geant4 data test, the original data has a bad resolution due to the low detection efficiency of the proposed detector. This is a handicap to perform time of flight PET with continuous scintillators and SiPM arrays. The proposed TDC architecture can reduce the problem trying to detect first arrival photons. In an ideal scenario, each SiPM will be attached to one TDC and, in this situation, the first triggered SiPM is used to timestamp the received event. This SiPM is the one triggered by the first generated photons, which have the lowest time error. The proposed architecture allows us to use the first triggered SiPM for timestamping.

In the Single photon test, the IC architecture does a good job measuring the resolution of sources with low timing error. For the Geant4 data test, the TDC obtains results near the best result that can be obtained with the detector configuration used.

The proposed simulation allows us to consider different scenarios. For this reason, it becomes a useful tool to validate the right architecture for the future IC development.

Acknowledgments

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