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An Acoustic Modem Featuring a Multi-Receiver and Ultra-Low Power

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Abstract

Wireless technology for underwater communication possesses a wide range of potential application, but it is still a relatively unexplored area in many aspects concerning modems physical design. A step towards future deployment of underwater networks is the reduction of power consumption. Therefore, asynchronous wakeup systems need to be integrated within the physical layer design while avoiding the use of additional transducers. This paper offers a practical and generic solution to adapt data reception and transmission together with asynchronous wakeup sub-systems in acoustic underwater modem architectures using a low power and low cost solution. The proposal has been implemented in a real prototype with success.

Keywords

1. Introduction

Underwater Sensor Networks (USN) possess a wide range of potential applications: oceanographic data collection, pollution monitoring, offshore exploration, disaster prevention, assisted navigation, tactical surveillance, and others [1] [2].

During the last decade, wireless technology for underwater communication has improved sufficiently to offer hope for the future. Of the wireless underwater alternatives, acoustic signals present less attenuation than optics or electromagnetic waves, being able to cover distances ranging from a few meters to several kilometers [3].

However, acoustic underwater technology is still a relatively unexplored area compared with its terrestrial counterparts. The differences with radio frequency communication (RF) are especially important with regard to the design and development of reliable transducer adapters for the modulation and demodulation circuits

(modems). Instead of antennas, underwater acoustic communication requires more expensive electro-acoustic transducers, thereby increasing the final price of the modem. Thus, in order to reduce costs, modems with only one transducer are desirable. However, designing the circuit may be problematic due to the number of input and output ports that need to be interconnected.

For example, in addition to the transmitter and receiver typically incorporated into the modem [4], Acoustic-Triggered Wake-Up (AT-WU) systems [5] [6] can be used in order to reduce the modem power consumption to one which is near the ideal optimum [7]-[9]. With an AT-WU system, the node remains idle until it detects a pre-defined Wake-Up (WU) signal in the water channel. This feature, sleep mode, saves considerable amounts of energy compared with protocols such as STEM, which are based on periodic channel checking [10]. Moreover, nodes must also be able to transmit a wake-up signal to neighboring nodes in order for the network to function appropriately.

However, few studies have been presented to the scientific community on AT-WU systems with power consumption below 1 mW. The most important example was presented in 2006 [6]: its architecture block diagram is shown in **Figure 1**. There are three main blocks, interconnected with a control logic block:

- Wake-up receiver. The AT-WU system needs specific hardware to detect the pre-defined wake-up signal. This block must dissipate as little energy as possible since it is continuously active [11].
- Data-receiver. Incoming data signals are processed and decoded.
- Transmitter. Both wake-up and data signals are modulated and sent out through the channel.

These three blocks represent the generic input and output ports needed in the design of a single-transducer modem with AT-WU capability. The key issue in designing such circuits is efficiency. Although power consumption in the architecture developed by Wills *et al*. in 2006 [6] and abstracted in **Figure 1** is relatively low (500 μW), the system presents two main drawbacks. On the one hand, it uses two separate transducers and, on the other, the TRF FET amplifier block is shared by both the wake-up receiver and the data-receiver block. This connection in cascade leads to a level of consumption that could be optimized with an improved parallel and independent block design.

To resolve these issues, this paper presents an innovative single-transducer modem architecture and a design methodology which successfully upgrade any modem with WU capability. This is the first time that this problem has been tackled with regard to underwater modems.

The rest of the paper is organized as follows. Section 2 presents a generic single-transducer interconnection scheme and the methodology to design circuits with AT-WU capability. Section 3 describes a practical case study of the ITACA modem. The results obtained from this approach are discussed in Section 4, while Section 5 summarizes the conclusions.

2. Interconnection Scheme

The solution contained in this paper is presented in **Figure 2**. This architecture uses a single transducer and decouples the three main blocks related to signal processing: the AT-WU receiver, the data-receiver and the transmitter.

These three blocks are inter-connected to a matching impedance network built using passive components in order to avoid dissipating extra power. Thus, this matching network is critical in the design and can be divided into two separate sub-blocks: impedance matching in transmission and in reception. Each block in **Figure 2** is described in following sections less the control logic that refers to the modem MPU (wake, data and data or wake are digital input and output MPU signals).

2.1. Passive Transmission Matching Network

Figure 3 shows the output stage of most power amplifier architectures. Q1 and Q2 constitute the push-pull stage present in AB-class and D-amplifiers, which are common architectures in acoustic modems [12]. This architecture allows an embedded transformer to boost electro-transducer applied voltage in order to attain higher communication distances [4].

As discussed in [13], acoustic signal strength can be maximized by inductors connected in parallel to the transducer output. However, as will be discussed below, this push-pull stage does not require any extra element when the transducer impedance is in close proximity with a resistor, without any reactive impedance component.

Figure 1. Block diagram of a modem design enhanced with an AT-WU system [6].

Figure 2. Block diagram of the proposed interconnection scheme.

Figure 3. Typical push-pull output stage of transmission power amplifiers.

2.2. Passive Reception Matching Network

The problem in signal reception, as shown in **Figure 4,** is how to split incoming signal power into two different subsystems, the AT-WU and the data-receiver, which have different electrical characteristics.

This problem is usually encountered in RF systems, but it is new for acoustic modems. To the best of our knowledge, there are no previous studies on single-transducer modems that embed an AT-WU receiver.

The use of Wilkinson dividers, together with impedance transformer networks and voltage limiters, has been

tested with positive results in many reliable RF solutions [14] and [15].

2.2.1. Wilkinson Divider

Figure 5 depicts the structure of the Wilkinson power divider [15] [16]. It is formed by two ideal transmission lines (T1,T2) of a certain length (T1ˡ,T2ˡ), and the isolation resistor (R1).

The power divider is optimal when signal reflection in the different ports and attenuation between the input and both outputs are minimal. In this way, input power is equally propagated throughout both outputs (out1 and out out2) with maximum isolation between both output ports. Assuming equal impedance of the elements connected to the Wilkinson Divider, as represented by Expression (1), the optimal divider can be calculated in Equations (2), (3) and (4) [15].

$$Z_{in} = Z_{out1} = Z_{out2} = Z_0 \tag{1}$$

$$Z_{T1} = Z_{T2} = Z_0\sqrt{2} \tag{2}$$

$$T1_l = T2_l = \frac{\lambda}{4} \tag{3}$$

$$R1 = 2Z_0 \tag{4}$$

However, the original Wilkinson divider structure shown in **Figure 5** is unsuitable for acoustic applications. For operating frequencies below 100 kHz, the length of the T1 and T2 transmission lines would be in the hundreds of meters. Thus, although the divider architecture is simple and possesses advantages, an alternative approach is needed.

Transmission lines can be replaced by equivalent discrete electronic components (**Figure 6**). Around the central frequency, the circuit behaves in the same way as the original transmission lines.

Assuming $\lambda/4$ length transmission lines, equivalence is shown in Equation (5) and (6) **Figure 7**.

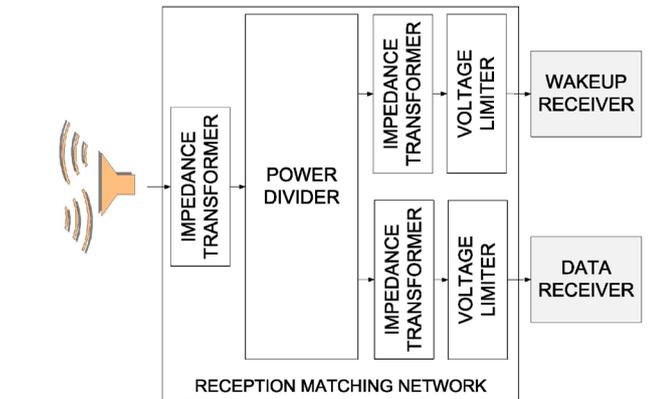$$C_1 = C_2 = \frac{1}{2\pi f_0 Z_T} \tag{5}$$

Figure 4. Block diagram of the overall matching network for reception.
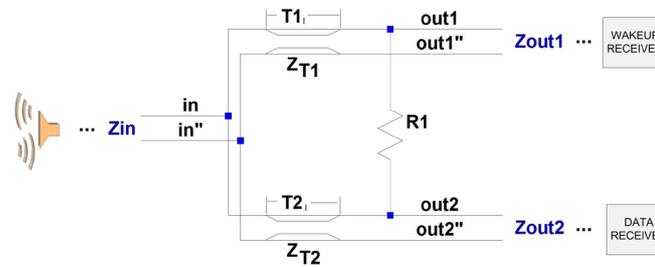

Figure 5. Wilkinson power divider generic diagram.

$$L_1 = \frac{Z_T}{2\pi f_0} \tag{6}$$

Thus, in accordance with Equations (2) and (3), $L_1 = L_2$ and $C_1 = C_2$ while $C_3 = C_1 + C_2$.

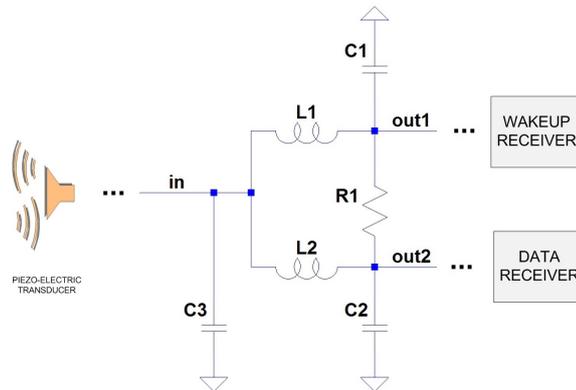### 2.2.2. Impedance Transformer Networks

In order to allow for differences in impedance among the three ports and to enable the design of optimal impedance transformer networks, the characteristic impedance Z_0 will be lower or equal to any interconnected port impedance. Thus, this design assumes Z_0 as the minimum impedance of the three ports (in port, out1 port and out2 port).

Impedance transformer networks are based on capacitor transformers, as depicted in **Figure 8**. For a narrow band around Z_0, the ratio between Z_{in} and Z_{out} is described by Equation (7). Additionally, the block carries out band-pass filtering.
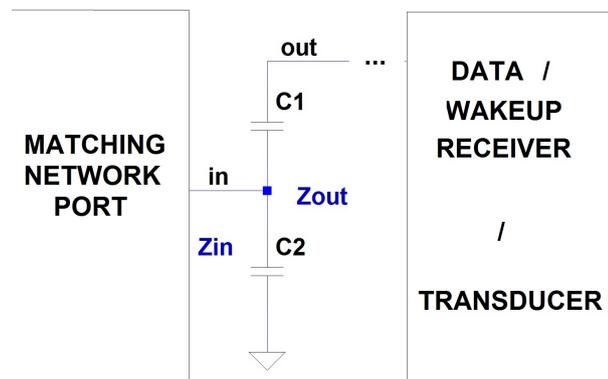
$$Z_{in} = Z_{out}\left(1+\left(\frac{C_2}{C_1}\right)^2\right) \tag{7}$$
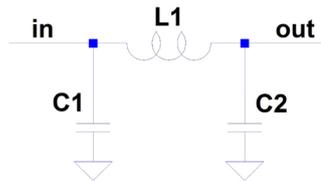
Figure 6. Transmission Line LC model.

Figure 7. Proposed Wilkinson power divider using discrete RLC components.

Figure 8. Capacitor-based impedance transformer.

2.2.3. Voltage Limiters

The Push-Pull output stage of the transmission power amplifier (the out signal shown in **Figure 3**) is directly connected to the in port in the proposed Wilkinson power divided depicted in **Figure 7**. Thus, the transmission power amplifier could cause unexpected high voltages at the highly sensitive AT-WU and data-receiver blocks. Voltage limiters appearing in **Figure 4** are detailed in **Figure 9**. Best results were obtained by placing limiters behind impedance transformers.

As a final consideration, R1 should be as high as possible in order to prevent unnecessary power dissipation during transmission periods. Otherwise, high impedance values could lead to unresolvable port condition mismatches.

3. Case Study: ITACA modem and ITACA AT-WU System Integration

The ITACA Institute has developed a low-cost, low-power and highly efficient underwater acoustic modem: the ITACA modem [5]. Its architecture is based on a microcontroller (MCU) that only consumes 24 mW in reception and 3 μW in the sleep state. It is capable of transmitting up to 100 m using frequency-shift keying (FSK) modulation at 1 kbps, while consuming 120 mW. The acoustic wake-up signal is transmitted using on-off keying (OOK), which is compatible with the FSK modulation used for regular transmissions. As a result, this modem also transmits the wake-up signal in the same frequency band as the regular data signal.

The modem architecture includes an AT-WU system that only draws 8 μW while idle, which, added to the 3 μW of the MCU in sleep mode, represents the lowest power consumption for such a system ever reported [9].

The overall layout described in this section is shown in **Figure 10**. The characteristic impedance Z_0 depends on the electro-acoustic transducer that sets the minimum impedance value of the inter-connection.

The ITACA modem is based on a commercial piezoelectric transducer, a HUMMINBIRD XP [17], making it a viable solution for the deployment of low-cost underwater acoustic networks. Piezoelectric transducer impedance can be described in terms of its RLC (Resistors, Inductors and Capacitors) model, which is shown in **Figure 11**. The reflection coefficient of single port elements (S11) obtained by a Vector Network Analyzer (VNA)
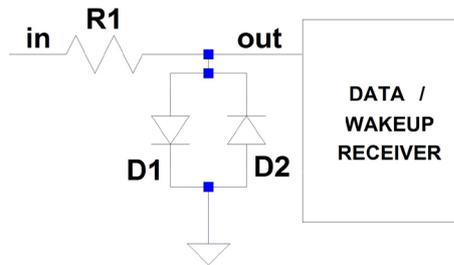
**Figure 9**. Capacitor-based impedance transformer.
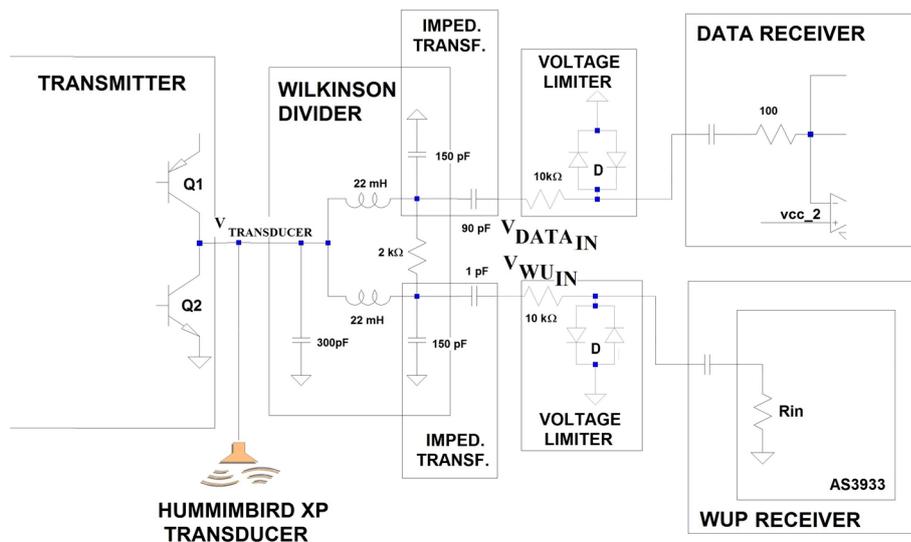
Figure 10. Final design of the ITACA modem with WU capability.

is applied to Equations (8), (9) and (10).

The closer S11 gets to 0, the more energy is transferred to the transducer. In **Figure 12** the magnitude of the selected HUMMINBIRD XP transducer frequency response is 85 kHz. Z_0 in (7) is the characteristic impedance of the VNA—50 Ω in the case of the HUMMINBIRD XP transducer. The impedance magnitude and phase are shown in **Figure 13**. RLC component values in **Figure 11** need to be calculated by means of Expressions (8), (9) and (10) as follows, in order to achieve equivalence with the expected transducer:

• Transducer impedance takes its minimum and maximum values on resonance (fr) and anti-resonance (fa) frequencies in **Figure 13**. Expression (8) defines the relationship of both frequencies. For frequencies below 70 kHz, the phase is nearly −π radians and the magnitude is inversely proportional to the frequency. This is consistent with capacitor behavior and, in this case, with C_2 in the RLC model. Once C_2 is calculated by means of Expression (9), C_1 can be deduced.

• L is deduced by means of Expression (7) while the resonant frequency (wr = 2πfr) depends on the known value of (fr).

• The resistor value is calculated by means of an empirical approach. Mean power dissipated by the piezoelectric transducer is modeled using the resistor power dissipation since dissipation from inductors and capacitors is negligible. A 1 kΩ resistor is still sufficiently accurate around the center frequency (85 kHz) [12]

$$S_{11} = \frac{Z - Z_0}{Z + Z_0} \tag{8}$$
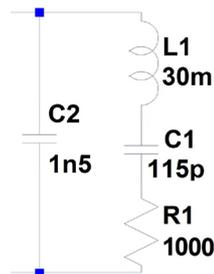
Figure 11. RLC model of the HUMMINBIRD XP piezoelectric transducer.
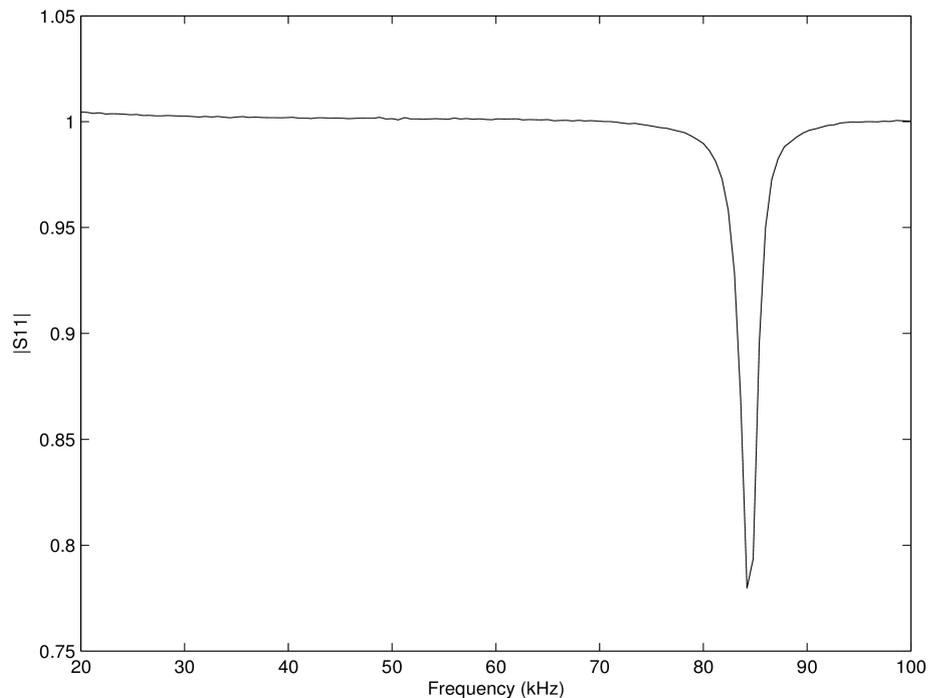
Figure 12. HUMMINBIRD XP transducer reflection coefficient measured using a VNA.

$$f_a = f_r \sqrt{\frac{C_1}{C_2} + 1} \tag{9}$$

$$w_r = 2\pi f_r = \frac{1}{\sqrt{L_1 \cdot C_1}} \tag{10}$$

Figure 12 shows the S_{11} experimental values for the HUMMINBIRD XP transducer. The RLC model values were calculated based on these results and the resistance calculated in [18]. Transducer impedance is 1 kΩ and the equivalent circuit is shown in **Figure 11**.

Figure 14 shows the data-receiver block whose operational frequency is 85 kHz. Two operational amplifiers are encapsulated inside a single chip, obtaining a 40 dB/decade 80 - 90 kHz band-pass filter with an 80 dB maximum gain and 4 mA of current drawn. The input impedance of this block is R1 and has been set to 10 kΩ in order to obtain a compromise between high input impedance, high amplifier gain and the amplifier bias point.

The AT-WU system is based on a commercial detector for Radio Frequency Identification (RFID) operation bands for electromagnetic wave-based networks. The main core is AS3933 from Austria Microsystems. **Figure 15** shows this component connected to the ITACA modem. The AS3933 input impedance is reconfigurable but best performance was achieved when it was set to 2 MΩ. Eventually, a capacitor should be connected in series to avoid circuit biasing modifications and performance losses.

Our experimental results demonstrated that the transmission power amplifier could be directly connected to the HUMMINBIRD XP piezoelectric transducer, according to the nearly resistive behavior of the transducer in the frequency range (around 85 kHz).

To design the Wilkinson divider, the minimum impedance comes from a piezoelectric transducer (1 kΩ), which establishes the characteristic impedance Z_0 and, consequently, the components of the divider: 22 mH inductors and 150/300 pF capacitors. As the AT-WU and data-receiver impedances are lower than Z_0, impedance
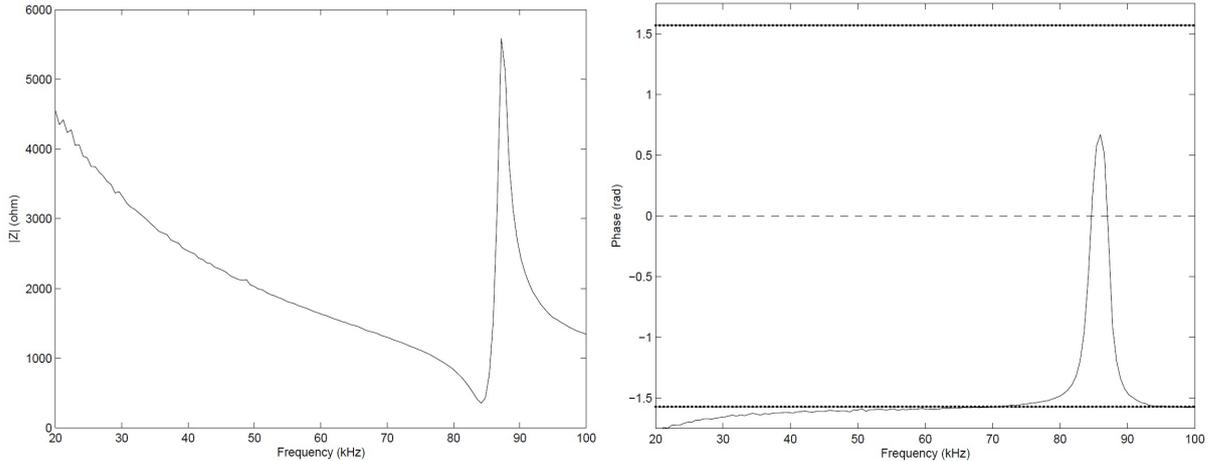

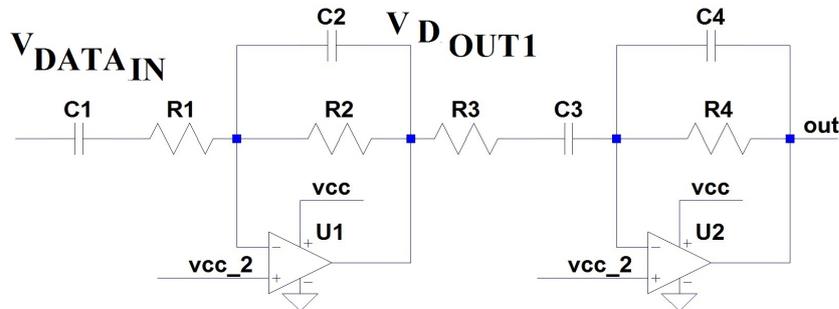**Figure 13**. Piezoelectric Transducer Impedance: Magnitude (left) and Phase (right).

Figure 14. Data reception amplifier based on operational amplifiers; vcc_2: supply voltage; vcc_2: half vcc_2 voltage.

transformers are necessarily added to the receivers. This stage has been merged with the output capacitor of the Wilkinson divider.

Finally, the resistor value selected for the voltage limiter is 10 kΩ. For the data-receiver, this element has been combined with the amplifier input resistor (now set to 100 Ω), whereas for the AT-WU receiver, this resistor is negligible since AS3933 input impedance is 2 MΩ.
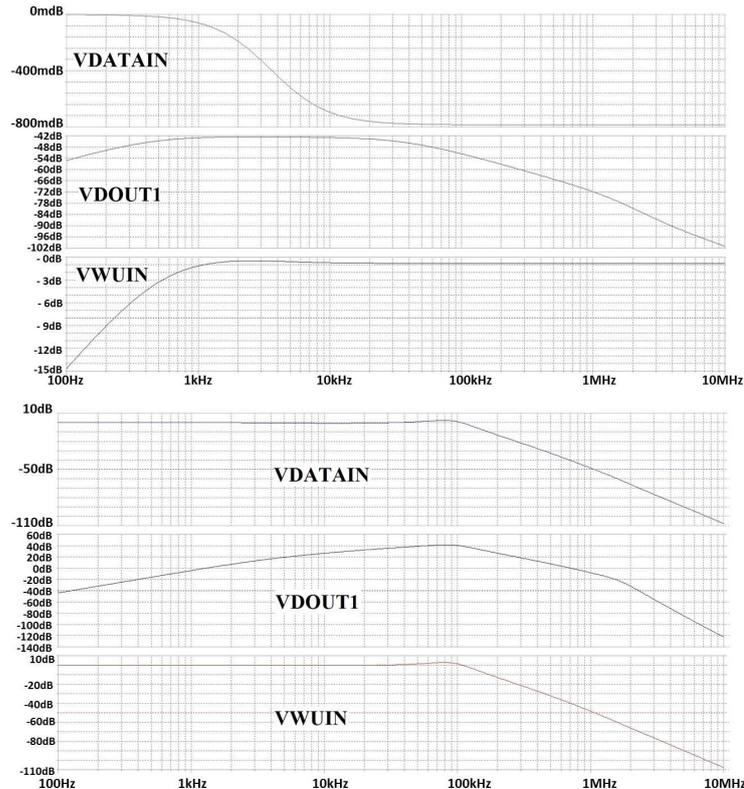
3.1. Simulation

The proposed circuit was simulated using SPICE-based electronic circuit simulation software: LTSPICE [19]. The voltage level in **Figure 10** was measured at four different nodes: the piezoelectric transducer (VTRANSDUCER), the input data (VDATAIN), the AT-WU receiver (VWUIN) and the first stage output voltage of the data-receiver amplifier (VDOUT1).

When the impedance is not balanced, the amplifiers are not correctly excited and their output level is lower than expected (40 dB gain per stage) regardless of the correct voltage input. The simulation results are as follows; Transmission is not detrimentally affected by the matching network. After inserting the proposed networks, the same performance is achieved as with the original modem [17]: 90% energy efficiency in simulation. On the reception side, the results without and with the proposed matching network are shown in **Figure 16**. Input vol-
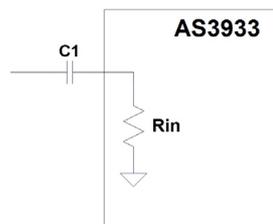
Figure 15. AS3933 connection diagram.

Figure 16. Simulation results.

tage increases in both receivers. At around 85 kHz (the ITACA modem operating frequency), the voltage level is 3dB higher when the matching network is used. The data-receiver amplifier is not correctly excited without the matching network. As shown in **Figure 16** right, VDOUT1 is expected to be 40 dB at around 85 kHz. However, as can be seen in **Figure 16** left, if both receivers are directly connected to the piezoelectric transducer, the voltage level is −42 dB. Thus, the Data-Receiver performance is seriously compromised without these impedance matching networks.

3.2. Prototype Implementation

Two modems were deployed in a 2.4 meter length water tank: transmitter (A) and receiver (B). The maximum transducer peak-peak voltage in transmission was set to 5 V. The experimental results were in sequence as follows:

1) Initially, on A side only the transmitter block was connected to the transducer. In B side, the transducer was not connected to the data-receiver nor to the WU receiver blocks. Thus, the received peak-peak voltage measured in B transducer was 220 mV.

2) Next, the proposed matching network proposed in **Figure 10** was connected only on A side to evaluate transmission losses. Peak-peak received voltage was still 220 mV on B, so the proposed design did not have any negative impact on transmission.

3) The data-receiver block was connected to the transducer on B side. Peak-peak voltage in reception was still 220 mV and the data signal was correctly decoded.

4) The AT-WU receiver block was connected to the transducer on B side, while the data-receiver block was disconnect on B side too. Peak-peak voltage in reception was 220 mV and the WU signal was correctly decoded.

5) Next, the data-receiver and AT-WU receiver blocks were both now connected to the piezoelectric on B side in parallel without any matching network. AT-WU signals were received, but the data was no longer decoded. Peak-peak input voltage for both receivers was still around 220 mV, but only noise could be found in the data receiver amplifier output (the 80 dB gain amplified noise when no actual data was received).

6) Finally, the proposed matching network was now connected on B side. Data and AT-WU signals were now correctly decoded. Peak-peak input voltage was still 220 mV. The different waves captured during the experiment are shown in **Figure 17**. The voltage level did not decrease, nor was distortion observed in the ports (*i.e.* in VTRANSDUCER, VDATAIN and VWUIN). The first stage of the data-receiver amplifier (VDOUT1) reached its maximum level (3.3 V) during this experiment.

Receiver sensitivity was checked with the matching network incorporated into the prototype. The original specifications were maintained: AT-WU receiver at 80 μV and the Data-Receiver at 30 μV.
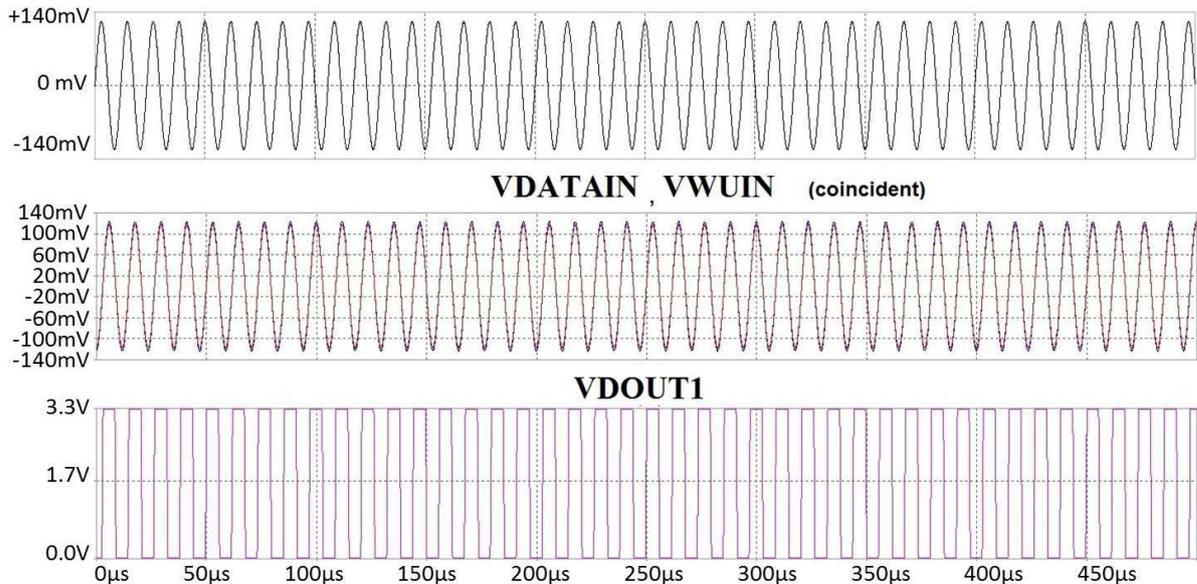
Figure 17. Voltage measurements in the final prototype.
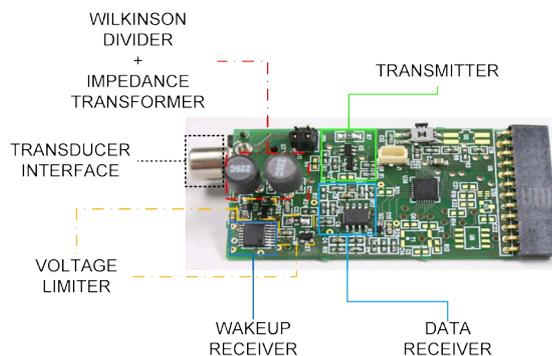
Figure 18. Final implementation of the ITACA modem prototype.

Power consumption did not increase either in reception or in sleep mode with the additional impedance network circuits. However, in transmission some extra power was consumed by the voltage limiters, specifically by their resistors (**Figure15**). It was possible to raise the output peak-peak voltage of the transmission power amplifier to 30 V to increase communication range. 12 mW extra were therefore dissipated when peak-peak voltage was increased up to 30 V and transmission power was 108 mW, constituting an 11% overhead in the worst case.

The final version of the prototype is shown in **Figure18**. The different matching network elements are highlighted.

4. Conclusions

A critical issue of Wireless Sensor Networks circuits is energy management. Current advances in underwater communication make a necessary reduction in power consumption. Asynchronous wakeup systems are a suitable solution when implemented as HW hearing circuits. These circuits avoid extra processing consumption on the main microcontroller that remains in sleep mode with "one eye open" [7].

However, wake-up circuits need to be integrated within the modem system while avoiding the use of additional transducers.

This paper offers a practical and generic solution for the purpose of adapting reception and transmission sub-systems in acoustic underwater modem architectures using a single-transducer. The paper has reviewed interconnection requirements and provides a methodology to design modems with AT-WU circuits that is extendable to VLSI circuits. As an example, the ITACA modem is a practical case study that implements a three-port interconnection bridge. The experiments performed with a real prototype demonstrate the suitability of the previously successful simulation.

Acknowledgements

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