Packaging and assembly for integrated photonics - a review of the ePIXpack photonics packaging platform

L. Zimmermann, G.B. Preve, T. Tekin, T. Rosin, K. Landles

***Abstract*—We review recent work done by the photonics packaging platform ePIXpack that serves the academic community with packaging & assembly developments in the area of integrated photonics. The paper includes recent examples of our packaging and assembly work, covering a broad range of technologies from silicon photonics to InP based devices.**

***Index Terms*— Hybrid integrated circuit packaging, Photonic integration, Silicon-on-insulator (SOI)**

I. Introduction

The need for next generation carrier networks with capacities of 100Gbit/s transmission rate and beyond is driven by ubiquitous internet access, video driven IP traffic, high-definition TV broadcast etc. [1, 2]. Networks will need to handle constantly increasing bandwidth, while the underlying fiber infrastructure naturally only undergoes slow changes. This requires advanced solutions for high transmission capacity, which eventually can only be provided by integrated photonics devices. One option is silicon photonics. Silicon-on-Insulator (SOI) is becoming an attractive passive optical integration platform due to its flexibility in terms of optical design. Thin SOI (~200nm) yields high-index contrast nanowaveguides [3] with ultrasmall bend radii, while slightly thicker material is well suited for Germanium integration [4]. 4µm SOI allows for fabrication of waveguides with very low loss and low polarization dependence [5]. Still larger waveguides (10µm) are ideally matched to standard fibers [6]. However, there still remain many challenges for silicon photonics to become an accepted technology in optical communications, e.g. integration of the source, efficient modulation, and polarization dependence.

A more mature and widely adopted technology in optical communications is based on InP photonics, which has proven to be up to high performance demands for a wide spectrum of applications including all aspects of optical communications (sources, modulators, detectors). The development of InP photonics with a higher degree of integration started in the last decade, but only in recent years these developments led to commercially deployed solutions [7]. Even nowadays, most available InP based devices show only a minor degree of integration.

Concluding from what we have said so far, a large part of present integrated photonics technology is still in the research phase, a view which is also supported by the considerable number of research projects in the field. This leads to a particular situation in terms of packaging and assembly of integrated photonics. Packaging is of utmost concern with regard to achievable module performance and eventual costs. In integrated photonics, packaging still has to overcome major challenges related to integration itself, such as large electrical and optical i/o count, high-performance RF packaging, or power dissipation. Most developments in integrated photonics are, however, conducted in the frame of medium to large scale publicly funded research projects that dedicate only a small part of their resources to packaging and assembly. The problem becomes apparent if researchers make use of the presently built technology platforms such as ePIXfab (silicon photonics) or JePPIX (InP photonics), who offer planar device technologies but cannot serve the packaging demands of their users.

Here we present an approach to solving the problem by a new way of conducting packaging or assembly R&D, which is similar (but on a smaller scale) to the setup used for foundry services in microelectronics, i.e. package development services. Our approach is a team-up of proven technology providers in the field of packaging and assembly, who gather under the roof of the service organization ePIXpack.

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II. EPIXPACK FOR PHOTONICS PACKAGING IN R&D

Packaging and assembly technologies are fundamental to making available and practically usable the results of advanced photonic research. At present, advanced packaging technologies are not easily available to most academic users as well as many research programs in advanced photonics. Apart from obvious difficulties for users to realize prototyping and fabricate testable components, this also leads to a very poor or even absent comprehension of the main packaging constraints and problems. It also increases the risk for making decisions on packaging technologies that might turn out very expensive or irreversible.

ePIXpack is geared towards offering full technical support to any kind of packaging requests from the lightwave community, utilizing some of the best packaging laboratories, technologies and expertise in Europe. The focus is on technical services for very early prototype photonic packaging & assembly demands (pre-prototypes & prototypes). The consortium provides a one-stop service to the external world, which gives access to a full spectrum of advanced packaging technologies (Fig. 1). The users has access to the ePIXpack services through the coordinator. The coordinator is available through the ePIXpack web interface [10]. Despite the core partners, ePIXpack also provides links to industrial partners who are prepared to provide fully commercial solutions.

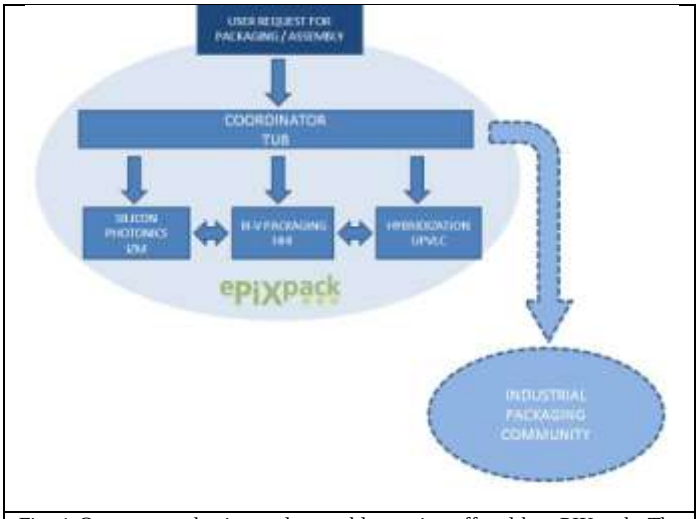

Fig. 1 One-stop packaging and assembly service offered by ePIXpack. The coordinator acts as interface to a broad packaging technology base.

ePIXpack is conceived as a closely interlinked structure, with the partners constantly interchanging their knowledge and utilizing respective facilities and labs to help developing the proper packaging processes. Each partner offers leadership in a specific technology, but may also count on the know-how and equipment of other partners, enabling a wider choice in terms of technologies and a better timing in terms of service. Services of ePIXpack include:

- fiber pigtailing (lensed, SSMF, PMF)
- assembly & hybridization
- RF packages

In the following we shall introduce ePIXpack by presenting some examples of recent work as well as providing an overview of available technologies inside the consortium.

III. PIGTAILING OF OPTICAL MOTHERBOARDS

New pigtailing and packaging solutions are required to achieve high flexibility but also satisfy the requirement of reduced cost at early stage R&D. In the following, we shall present the example of such an SOI pigtailing technology developed specifically for the testbed. The work was done at Optocap Ltd, and was based on close technical cooperation with TU Berlin. The first application was in all optical routing using SOI motherboards with hybrid integrated semiconductor optical amplifiers. The work was part of the developments of the European project BOOM [5], however conducted within the frame of the European packaging platform ePIXpack [6].

The BOOM wavelength routing concept is largely based on a 4µm SOI-motherboard technology. Since standardization reduces costs, we designed all SOI motherboards for equal size and equal fiber input and output pitch. Wire bonding allows for the required flexibility of electrical connections. In terms of device packaging, with differing product requirements, in terms of fibre in/out and electrical power requirement, a tailorable package format is desirable. This can also reduce NRE costs during initial testing. Optocap's bathtub package (Fig. 2) has configurable end-wall options, covering multi-fibre as well as electrical supply requirements. Internal interconnects are via wire-bond pedestals.

Fig. 2 (Left) Standard Optocap Bathtub Package, with four application specific end blanks, covering single and multiple fibre feedthroughs as well as electrical interconnects. (Right) Packaged device with 1-in 3-out configuration plus electrical connections.

A central issue is the power penalty due to the pigtailing process. Submicron precision can be achieved by active alignment procedures, but fixation of the fiber, shrinkage of adhesive during the curing process and thermal drift usually lead to the preference of welding processes for fiber fixation and that is why we have opted for this method.

Only active alignment can achieve the required precision of the pigtail. This is carried out by manipulating the fiber pigtail using sub-micron stepper motors. The fiber, pre-sealed into an external metal tube, is positioned using direct feedback from

the illuminated waveguide and, when optimized, is fixed in position using a laser spot welding system.

In Fig. 3 we compare the transmission signals through a 4x4 coupler before (pre) and after (post) the process of attaching the waveguide tile to the optical bench. Initial coupling was obtained with the tile mounted on a vacuum table, with lensed optical fibres introduced and aligned to input and output waveguide facets. The graphs show that a power penalty is incurred during the process. However, the penalty per channel is approximately 1dB, which testifies that the method of low temperature epoxy bonding to a planar lapped surface introduces minimal mechanical stress on the waveguide tile.

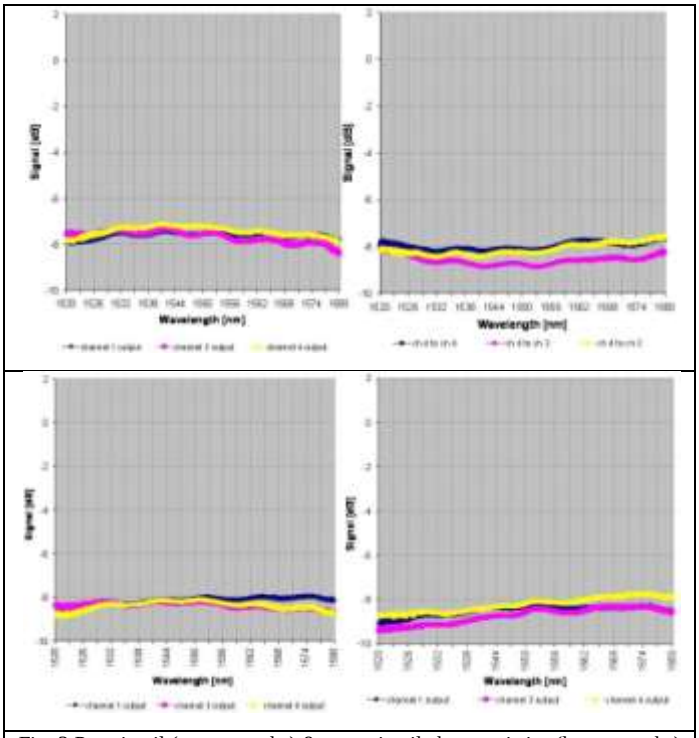

Fig. 3 Pre-pigtail (upper graphs) & post-pigtail characteristics (lower graphs) of 2 input channels of a 4x4 coupler. Insertion loss penalty is about 1dB across 4 pigtails.

IV. RF MODULE PACKAGING

Sending and receiving side of the internet Gbit-data stream are handled by the Fraunhofer HHI-Packaging Group. Some of the examples will be shown here.

A directly modulated laser was packaged in a cooled butterfly housing with lateral RF-input. A coplanar waveguide (CPW) on quartz led the signal from V-type connector to bond pad of laser, resulting in a 40 Gbit/s stream in the fiber. In Fig. 4 the module is fixed in a modified butterfly socket.

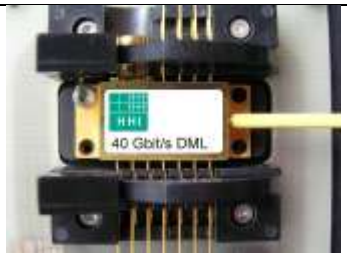

Fig. 4 Directly Modulated Laser (DML) in modified butterfly module and socket with lateral RF input

In special cases several RF connectors are necessary, as in Fig. 5 for cryptography based on chaotic sending of data (PICASSO) with three SMA-Connectors. A detail of the fiber-chip-coupling with a lensed fiber is depicted to the right.

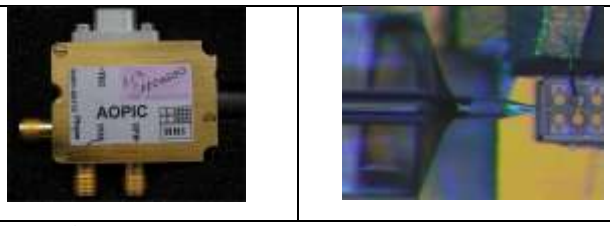

Fig. 5: (Left) PICASSO-Module with three SMA-connectors and (right) detail of fiber-chip-coupling.

Connecting 100 GHz signals is a difficult job, also for ultra-fast HHI-InP-based photodiodes (>100 GHz). But there is a vast experience in HHI in designing, fabricating and bonding CPW or MS (microstripline) connections in µm dimensions with low signal damping (e. g. MS with 0,43 dB/mm at 110 GHz).

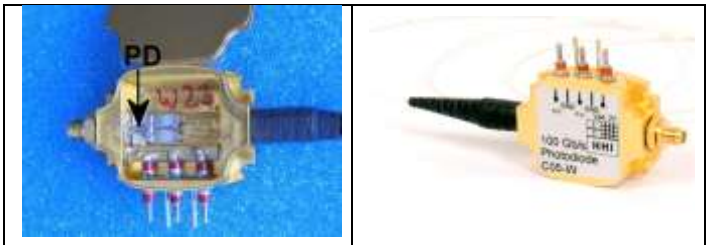

Fig. 6 Packaged InGaAs/InP-photodiode (PD, [11]) in housing with 110 GHz connector (FhG-HHI pin-PD-Module).

The PD module in Fig. 6 is butt coupled to the fiber and has a 110 GHz (1 mm, W-type) connector as output. RF measurements (see Fig. 7) with an optical heterodyn setup demonstrate available power, within 3 dB limits of up to 107 GHz.

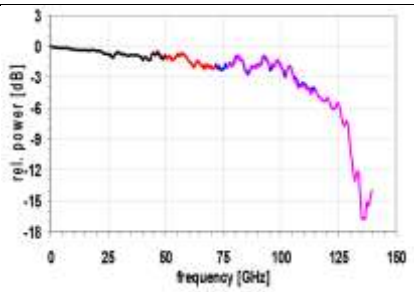

Fig. 7 Frequency response of FhG-HHI pin-PD-Module, -3 dB power at 107 GHz [12]

The only way of generating high-speed Gbit-data streams is the use of a modulator. Especially an InP Mach-Zehnder-Modulator is qualified due to its small size and small driving voltage. The packaging of the HHI´s own 40Gbit/s InP Mach-Zehnder-Modulator was done with a V-type connector connected with a CPW and very short bond wires to the chip and a double-sided lensed fiber coupling, see Fig. 8.

Fig. 8 40Gbit/s InP Mach-Zehnder-Modulator (FhG-HHI)

Due to the high quality of the module design the intrinsic performance of the InP modulator chip could be preserved which leads to the excellent RF performance shown in Fig. 9.

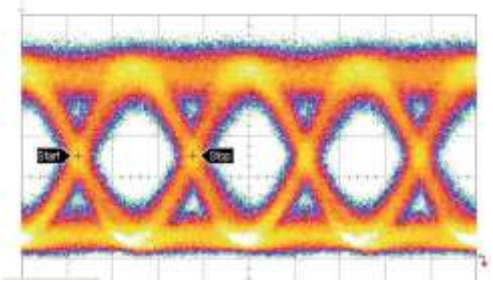

Fig. 9 Modulator Module RF Performance at 80 Gbit/s (1550nm): Extinction ratio: 9.5 dB, PRBS: 2^31-1, VPP: 2.8 V

All of the characterized RF packaging and fiber coupling techniques of the HHI-Packaging Group are ready to fulfill customer wishes. Module housings and RF connection schemes can be designed to fit the demands of the chip.

V. HYBRID OPTICAL AND ELECTRICAL ASSEMBLY

Innovative and reproducible hybridization technologies are necessary to fulfill the challenging requirements of future photonics components. In response to such necessities, the Valencia NTC Institute built up a complete packaging lab, particularly centered on the acquisition of equipments and technologies useful for the development and fulfillment of the objectives of advanced hybridization.

With partial help of European funding (FEDER), we have installed a complete line of packaging equipment. Inside the ePIXpack consortium we are particularly dedicated to the development of hybrid optical assembly and electrical assembly, with the use of a flip-chip die bonder FC150, an a ATV reflow oven, a PACTECH laser assisted reflow ball bumper as well more standard technologies using the FINETECH die placer and the TPT ball and wedge die bonder.

Following the ePIXpack concept of strong technical support and cooperation, we are able to develop advanced technologies in strict partnership with the requesting entities. We support technical choices and participate actively in the design phase that involves the choice of technology and is strict part of the success in the development.

Here we shall show a couple of examples of what we are currently working on, as subcontractor of the European Project BOOM.

We were asked to develop and optimize a repeatable flip-chip technology to attach an SOA chip in front of an SOI waveguide with an overall tolerance after bonding of +/- 1 micron or less. An 1250µm long SOA chip had to be placed on an SOI motherboard with gold-tin bumps, as is shown in an overall SEM image in Fig. 10.

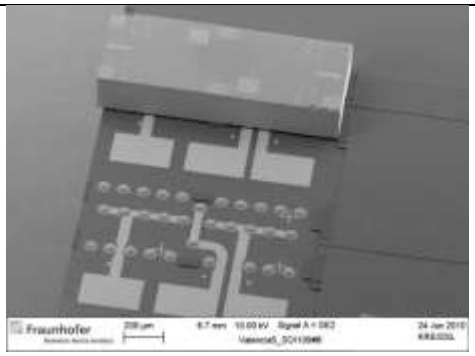

Fig. 10 Overall view of chip and integration area of the motherboard

AuSn bumps were realized in the BOOM consortium before the flip-chip process by sputter deposition and lift-off. Bumps had been shaped by a reflow process. We also tested the possibility to perform the reflow directly during the die-attach phase, obtaining first promising results.

The substrate had etched mesa properly designed to assure the optimum height of the SOA final position with respect to the tapered SOI waveguide. The remaining critical placements were therefore the placement along the optical axis and the lateral placement in front of the waveguide. In Fig. 11 we show a front view of the attachment area where the waveguide ends.

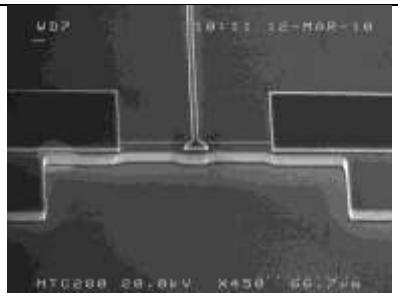

Fig. 11 Front view of the SOI waveguide before coupling.

Also critical was the position of the die itself. Standard flip-chip applications have fixtures that are designed so that the attachment area is at or near the center axis of the machine. In our case we had to deal with a position far away from the center, so we had to find solutions maintaining the proper reducing atmosphere in the chamber and, of course, perfect alignment (i.e. avoid major shifts after alignment).

We show in Fig. 12 and Fig. 13 SEM images with the best results after all the process (thermal, force and time profile) and fixture optimizations, both values below 1 micron. The repeatability was satisfactory. Especially in the optical axis direction we had consistent results with maximum variation below 2 microns.

We are currently working on the process to improve toward the submicron area with higher repeatability.

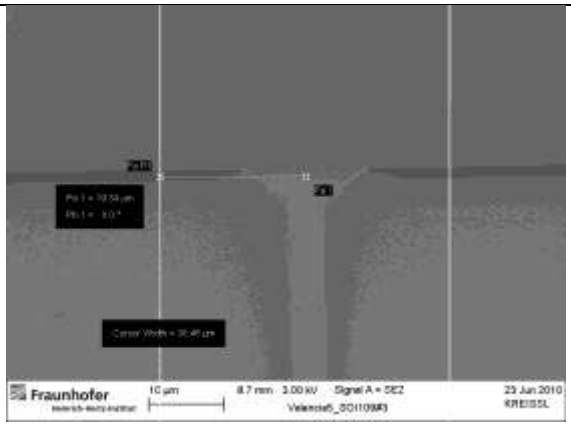

Fig. 12 Lateral placement misalignment below 1 micron

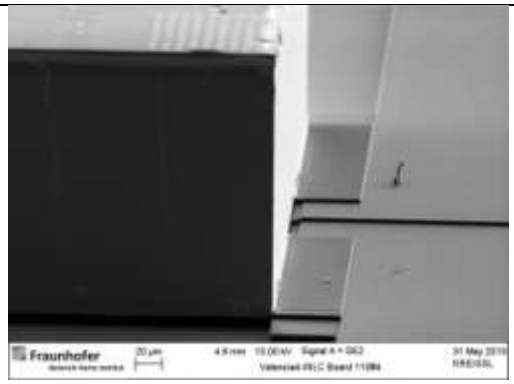

Fig. 13 Placement in direction of optical axis, misalignment ~1 micron

Another example of the ePIXpack contribution inside the BOOM project is the development of a process able to realize solder bumps utilizing SnAgCu solder balls of 40 microns diameter on various substrates and pad metallizations. For such development we utilize our PACTECH equipment that shoots the solder balls melting the material with laser assistance. Such technology is well established in production for 80 microns SnAgCu or AuSn solder balls, but is quite new and advanced for 40 microns SnAgCu solder balls. We worked on gold and aluminum metallization on silicon substrates. We developed the process and obtained very good preliminary results, in terms of wetting and placement as well as repeatability on SOI motherboards (see Fig. 14).

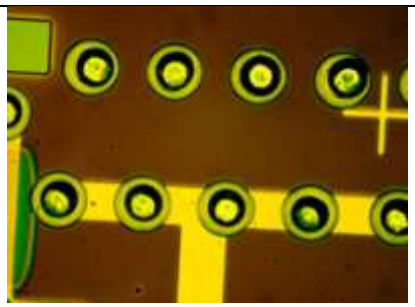

Fig. 14 Microscope image of solder bumps deposited by ejection bumping on SOI motherboards. The bumps are about 40µm in diameter, the pads have a diameter of 60µm.

The combination of proper pad design, proper metallization and bump metallurgy allows to realize even complex photonic geometries. The flexibility of our technology is therefore useful for various applications.

VI. TESTBED PACKAGING FOR SILICON PHOTONICS

There are two generic packaging concepts developed within the activities in order to provide a smart packaging of multiport passive silicon photonics devices and two provide the packaging of multiport electrically driven silicon photonics devices (g-Pack). Both concepts are based on coupling via waveguide gratings. Gratings have clear advantages such as

compatibility with planar processing, the possibility for wafer-level testing, and relatively large alignment tolerances. A drawback related to out-of-plane coupling is possible issues with mechanical stability and reliability while preserving at least partially the compactness of the underlying devices.

Coupling to silicon photonic wires through high-index contrast gratings is attractive because of the relaxed alignment tolerances compared to facet coupling while using standard single mode fibers. Simple one-dimensional grating couplers with a uniform fill factor, etched into a broad waveguide, achieve a coupling efficiency of around 30% with a 40nm 1dB bandwidth (per coupler) for a single polarization ([15]). These gratings have an alignment tolerance for a 1dB loss penalty of approximately ±2µm.

The fiber arrays based interconnection for cost effective, compact, smart silicon photonics packaging is shown in Fig. 15 without and with encapsulation. Hereto, commercial fiber array was used, consisting of a v-groove base, a glass lid and 8 fibers, where the front facet polishing angle was 8°. Measured typical alignment sensitivities 1 dB and 3 dB loss penalties in the lateral direction are provided, ±1µm in x-axis ±2µm in y-axis and ±2.5 in x-axis ±3.5 in y-axis respectively.

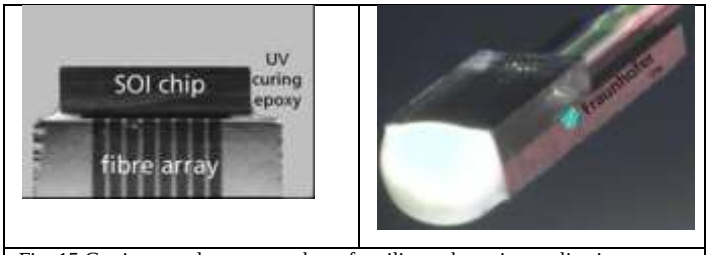

Fig. 15 Grating coupler array package for silicon photonics applications

The second generic packaging concept developed for silicon photonics is g-Pack [10]; it provides rigid fiber array coupling plus low-frequency electrical connections to ePIXfab [8] chips that feature a grating coupler array of standardized geometry. The standardized ePIXfab chips are already available. The package makes use of as much as possible commercially available components to reduce the final costs. Electrical connections are established by wire bonding to a commercial pin grid array (PGA) carrier. The top view of the schematic layout of g-Pack is depicted in Figure 16.

The approach of g-Pack is intended for use in testbed applications, i.e. at the stage before prototyping. Therefore, g-Pack does not offer hermetic housing or small footprint. Electrical connections are limited to low frequencies because of the choice of the ceramic carrier (PGA). The PGA is a commercially available, which is compatible with standard sockets to allow easy-plug operation and interchangeability of devices. The package is optimized for a large number of DC connections (>60). If temperature control or heat dissipation is required it should be implemented via the socket.

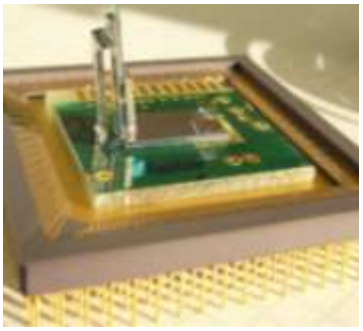

Fig. 16 g-Pack, side view. The pin grid array carrier was chosen to provide a large number of DC connects & to comply with standard socket dimensions.

As required by the grating couplers, the fiber array is mounted slightly tilted with an angle of 8° off the vertical. Commercial fiber arrays are available with standard single mode fibers and polarization maintaining fibers. The optical i/o count of the package can go up to 32.

VII. Future prospects of ePIXpack

The ePIXpack consortium will continue to work on concrete packaging solutions for the end-user. We shall also dedicate effort to packaging design solutions for our user community. We believe it is important to point out that ePIXpack will support the users having clear the whole picture of the different involved technologies, as well future system operations, not only speaking of packaging. This is guaranteed by the know-how and expertise of the partners of the consortium and it means to be able to differ from commercial partners, who are usually limited to small technology base. The best packaging solutions in fact arise when all the constraints and all the future applications are clearly understood and when it is possible to have access to a variety of process technologies.

The necessity of reorganizing the research landscape towards users and technology providers has been recognized in the integrated photonics community for a while. The concept has been developed quite far within the NoE ePIXnet, in which ePIXpack has its roots. The cooperation with technology providers such as ePIXfab, JePPIX or Nanophotonics ([16]) is already established, but will be further strengthened in the future.

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Lars Zimmermann received the Ph.D. degree from Katholieke Universiteit Leuven, Belgium, in 2003. In 1998, he joined IMEC where he worked on infrared detector arrays. In 2004, he joined the Technical University of Berlin (TU Berlin), where he worked on silicon waveguide and optical motherboard technology. Since 2006, he has been the Coordinator of the Photonic Packaging Platform ePIXpack. In 2008, he joined IHP, where he has been the Scientific Coordinator of the Joint Lab Silicon Photonics between IHP and TU Berlin. He heads the silicon photonics development team at IHP. His current research interests include electronic–photonic integration and integrated optics. Lars Zimmermann is teaching at TU Berlin.

Giovan Battista Preve has 20 years of experience working on packaging-related industrial R&D and production for optoelectronics, MEMS and sensors applications. He spent two years in Telettra/Alcatel working on high-RF components, 6 years in Italtel on optoelectronic components, including a couple of years at AT&T Bell Labs in Murray Hill (USA), 3 years at Gefran Sensors on MEMS and sensors activities and finally 7 years in Pirelli Labs again on optoelectronic components, as supervisor of the Back End Laboratories. In June 2008 he joined UPVLC-NTC as Packaging and Assembly Area Manager.

Thomas Rosin studied physics at the Technical University of Berlin and received the Ph.D. in 1982. He joined the Heinrich-Hertz-Institute in 1982 and was since involved in various research projects, including HDTV-TV Projection, 3D Free-Space Interconnections, Opto-Electronic Packaging, Multifiber Chip Coupling, and very high frequency applications (up to 160 GB/s). From 2001 to 2008 he was the head of the optical high frequency packaging group. Dr. Rosin is currently a Research Associate in the Optical Packaging Group, Photonic Components Department,. He is author and co-author of more than 30 scientific papers and 2 patents.

Tolga Tekin received his B.S. degree in Electronics and Telecommunications Engineering from Istanbul Technical University in 1992, his Dipl.-Ing. degree (M.S.) in Electrical Engineering from Technical University of Berlin in 1997, and his Ph.D. degree from Electrical Engineering and Computer Science at Technical University of Berlin in 2004. He was research scientist at Optical Signal Processing Department of Fraunhofer-Institute for Telecommunications Heinrich-Hertz-Institut (HHI), where he was engaged in advanced research on optical signal processing, 3R-regeneration, all-optical switching, clock recovery, and integrated optics. He conducted as a postdoctoral researcher at University of California research on components for O-CDMA and terabit router. He worked at Teles AG on phased array antennas and their components for skyDSL. He worked at Fraunhofer-Institute for Reliability and Microintegration (IZM), where he led projects on optical interconnects and silicon photonics packaging. He is currently with the Research Center of Microperipheric Technologies of Technical University of Berlin, where he is engaged in microsystems, photonic integrated system-in-package, photonic interconnects, and 3D heterogeneous integration research activities.

Kennedy Landles

In his engineering role at Optocap, Kennedy brings over twelve years experience in optoelectronic package design and manufacturing. His design/development experience covers optical isolator and laser diode module packaging, fibre coupling, WDM and Etalon products, Terahertz transmitters and PM products, as well as process development using laser weld and adhesive attach techniques.

Prior to joining Optocap, Kennedy provided engineering support and process development for new production introduction of passive optical modules at JDS Uniphase. He also worked in optical align processes at SDL Optics. Kennedy holds an Master of Science from the University of Victoria, BC, Canada, and a B.Sc.(Hons.) in Physics from Heriot-Watt University, Edinburgh, Scotland.