# Doctorat en Enginyeria Electrònica

**PADRE pixel read-out architecture for Monolithic Active Pixel Sensor for the new ALICE Inner Tracking System in TowerJazz 180 nm technology**

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July 19, 2017

A dissertation submitted to the University Polytechnic of València
for the degree of Doctor of Philosophy.

# Declaration

This dissertation is made of my own work, except where explicit reference is make to the work of others. It has not been submitted for another qualification to this or any other university.

Signature

# Acronyms

| | |
|---|---|
| ACORDE | ALICE COsmic Ray DEtector. |
| ADC | Analog to Digital Conversion. |
| ALICE | A Large Ion Collider Experiment. |
| ALPIDE | ALice PIxel DEtector. |
| ASICs | Application Specific Integrated Circuits. |
| ATLAS | A Toroidal LHC AparatuS. |
| CERN | European Organization for Nuclear Research. |
| CIS | CMOS Imaging Sensor process. |
| CDS | Correlated double sampling. |
| CMOS | Complementary metal-oxide-semiconductor. |
| CMS | Compact Muon Solenoid. |
| DAC | Digital-to-Analogue Converter. |
| DAQ | Data Acquisition. |
| DPRAM | Dual Port RAM. |
| ECAL | Crystal Electromagnetic Calorimeter. |
| ECC | Error Correction Coding. |
| ELT | Enclosed Layout Transistors. |
| EMCAL | ElectroMagnetic CALorimeter. |
| FE | FrontEnd. |
| FET | Field Effect Transistor. |
| FF's | Flip Flops. |
| FMD | Forward Multiplicity Detector. |
| FPC | Flexible Printed Circuit. |
| FPGA | Field Programmable Gate Array. |
| FSM | Finite State Machine. |
| GDSII | Graphic Database System II. |
| HCAL | Brass/Scintillator Hadron Calorimeter. |
| HDL | Hardware Description LAnguage. |
| HEP | High Energy Physics. |
| HFT | Heavy Flavor Tracker. |
| HMPID | High Momentum Particle Identification. |
| HPD | Hybrid pixels detectors. |
| IB | Inner Barrel. |
| IP | Interaction Point. |
| IPHC | Institut Pluridisciplinaire Hubert CURIEN |
| ITS | Inner Tracking System. |
| LHC | Large Hadron Collider. |
| LS2 | Long Shutdown 2. |

| | |
|---|---|
| MAPS | Monolithic Active Pixel Sensors. |
| MOSFET | Metal-Oxide-Semiconductor Field Effect Transistor. |
| MPW | Multi-Project Wafer. |
| NIEL | Non-Ionising Energy Loss. |
| NMOS | n-channel MOSFET. |
| OB | Outer Barrel. |
| p | Proton. |
| Pb | Lead. |
| PCB | Printed Circuit Board. |
| PHOS | PHOton Spectrometer. |
| PMD | Photon Multiplicity Detector. |
| PMOS | p-channel MOSFET. |
| QGP | Quark-Gluon Plasma. |
| RAM | Random-Access Memory. |
| RHIC | Relativistic Heavy Ion Collider. |
| RMS | Root Mean Square. |
| RTL | Resistor Transistor Logic. |
| SCT | SemiConductor Tracker. |
| SDD | Silicon Drift Detector. |
| SEE | Single Event Effects. |
| SET | Single Event Transient. |
| SEU | Single Event Upset. |
| $SiO_2$ | Silicon Dioxide. |
| SPD | Silicon Pixel Detector. |
| SPS | Super Proton Synchrotron. |
| SRAM | Static RAM. |
| SSD | Silicon Strip Detector. |
| STI | Shallow Trench Isolation. |
| TID | Total Ionising Dose. |
| TMR | Triple Modular Redundancy. |
| TOF | Time Of Flight. |
| TPC | Time Projection Chamber. |
| TRD | Transition Radiation Detector. |
| TRT | Transition Radiation Tracker. |
| ZDC | Zero Degree Calorimeter. |

# Resum

El subdetector ITS (Inner Tracking System) del detector ALICE (A Large Ion Collider Experiment) és un detector de vèrtex i és el detector mes proper al punt d'interacció. Es troba conformat per 3 tipus de subdetectors, dues capes de píxel de silici (Silicon Pixel Detectors), 2 capes d'acumulació de silici (Silicon Drift Detectors) i 2 capes de banda de Silici (Silicon Strip Detectors). La funció primària del ITS és identificar i rastrejar les partícules de baix moment transversal.

El detector ITS en les seues dues capes més internes estan equipades amb sensors de silici basats en píxels híbrids. Per a reemplaçar aquesta tecnologia de Píxels, el detector ITS actual serà reemplaçat per un nou detector d'una sola tecnologia, ampliant la seua resolució espacial i millorant el rastreig de traces. Aquest nou detector constarà de set capes de sensors de píxels actius monolítics (MAPS), les quals hauran de satisfer els requeriments de pressupost de materials i ser tolerants a majors nivells de radiació per als nous escenaris d'increments de lluminositat i majors taxes de col·lisions. Els sensors MAPS que integren el sensor d'imatge i els circuits de lectura es troben en la mateixa hòstia de silici, tenen grans avantatges en una bona resolució de posició i un baix pressupost material en termes de baix cost de producció.

TowerJazz ofereix la possibilitat d'una quàdruple-WELL aïllant els transistors pMOS que es troben en la mateixa nWELL evitant la competència amb l'elèctrode de recol·lecció, permetent circuits mes complexos i compactes per a ser implementats dins de la zona activa i a més posseeix una capa epitaxial d'alta resistivitat. Aquesta tecnologia proporciona una porta d'òxid molt prim limitant el dany superficial per la radiació fent-ho adequat per al seu ús dins de l'experiment ALICE. En els últims quatre anys s'ha dut a terme una intensiva R+D en MAPS en el marc de l'actualització del ITS d'A-LICE. Diversos prototips a petita escala s'han desenvolupat i provat

reeixidament amb rajos X, fonts radioactives i feixos de partícules. La tolerància a la radiació d'ALICE ITS és moderada amb una tolerància d'irradiació TID de 700 krad i NIEL d'$1\times 10^{13}$ 1MeV $n_{eq}$cm$^{-2}$, MAPS és una opció viable per a l'actualització del ITS.

La contribució original d'aquesta tesi és la implementació d'una nova arquitectura digital de lectura de píxels per a MAPS. Aquesta tesi presenta un codificador asíncron d'adreces (arquitectura basada en la supressió de zeros transmetent l'adreça dels píxels excitats denominada PADRE) per a l'arquitectura ALPIDE, l'autor també va fer una contribució significativa en l'assemblatge i verificació de circuits. PADRE és la principal recerca de l'autor, basada en un codificador de prioritat jeràrquica de quatre entrades i és una alternativa a l'arquitectura de lectura rolling-shutter.

A més dels prototips a petita escala, també s'han desenvolupat prototips a escala completa a les necessitats del detector ITS (15 mm i 30 mm) emprant un nou circuit de lectura basat en la versió personalitzada del circuit PADRE. El pALPIDEfs va ser el primer prototip a escala completa i es va caracteritzar obtenint un temps de lectura de la matriu per sota de 4 $\mu$s i un consum d'energia en l'ordre de 80 mWcm$^{-2}$. En general, els resultats obtinguts representen un avanç significatiu de la tecnologia MAPS quant al consum d'energia, velocitat de lectura, temps de recol·lecció de càrrega i tolerància a la radiació. El sensor pALPIDE2 ha demostrat ser una opció molt atractiva per al nou detector ITS, satisfent els requeriments en termes d'eficiència de detecció, fake-hit rate i resolució de posició, ja que el seu rendiment no pot aconseguir-se mitjançant prototips basats en l'arquitectura de lectura tradicionals com és el rolling-shutter dissenyat en la mateixa tecnologia. Per aquesta raó, la R+D en els prototips ALPIDE ha continuat amb l'objectiu d'optimitzar encara més el rendiment del sensor especialment en termes del temps mort i estudiar solucions en altres aspectes de sistemes d'integració.

L'últim circuit de ALPIDE, el pALPDIE3B, consumeix menys de 50 mW cm-2 amb una màxima taxa de transmissió d'1,2 Gbps i té una eficiència a la reconstrucció de traces superior al 99,95%. Amb un marge operatiu satisfactori després d'irradiació amb una fluència equivalent d'$\times 10^{13}$ 1 MeV $n_{eq}$cm$^{-2}$. A més, validant un consum d'energia per

sota de 50 mW cm$^{-2}$. I una resolució de posició d'uns 5 $\mu$m i una velocitat de lectura aproximada de 2 $mu$s, complint amb les especificacions ALICE ITS per a la seua actualització. Els resultats obtinguts de la caracterització del pALPIDE3B, la fase optimització dels circuits i de prototips es finalitza i dóna motiu a l'inici de la producció en massa del xip ALPIDE per a l'any 2017. El nou detector ITS s'instal·larà durant el segon gran aturada del LHC l'any 2020 en la caverna d'ALICE.

# Resúmen

El sub detector ITS (Inner Tracking System) del detector ALICE (A Large Ion Collider Experiment) es un detector de vértice y es el detector mas cercano al punto de interacción. Se encuentra conformado por 3 tipos de subdetectores, dos capas de pixel de silicio (Silicon Pixel Detectors), 2 capas de acumulación de silicio (Silicon Drift Detectors) y 2 capas de banda de Silicio (Silicon Strip Detectors). La función primaria del ITS es identificar y rastrear las partículas de bajo momentum transversal.

El detector ITS en sus dos capas más internas están equipadas con sensores de silicio basados en píxeles híbridos. Para reemplazar esta tecnología de Píxeles, el detector ITS actual será reemplazado por un nuevo detector de una sola tecnología, ampliando su resolución espacial y mejorando el rastreo de trazas. Este nuevo detector constará de siete capas de sensores de píxeles activos monolíticos (MAPS), las cuales deberán satisfacer los requerimientos de presupuesto de materiales y ser tolerantes a mayores niveles de radiación para los nuevos escenarios de incrementos de luminosidad y mayores tasas de colisiones.

Los sensores MAPS que integran el sensor de imagen y los circuitos de lectura se encuentran en la misma oblea de silicio, tienen grandes ventajas en una buena resolución de posición y un bajo presupuesto material en términos de bajo coste de producción.

TowerJazz ofrece la posibilidad de una cuádruple-WELL aislando los transistores pMOS que se encuentran en la misma nWELL evitando la competencia con el electrodo de recolección, permitiendo circuitos mas complejos y compactos para ser implementados dentro de la zona activa y además posee una capa epitaxial de alta resistividad. Esta tecnología proporciona una puerta de óxido muy delgado limitando el daño superficial por la radiación haciéndolo adecuado para su uso den-

tro del experimento ALICE. En los últimos cuatro años se ha llevado a cabo una intensiva I+D en MAPS en el marco de la actualización del ITS de ALICE. Varios prototipos a pequeña escala se han desarrollado y probado exitosamente con rayos X, fuentes radioactivas y haces de partículas. La tolerancia a la radiación de ALICE ITS es moderada con una tolerancia de irradiación TID de 700 krad y NIEL de $1 \times 10^{13}$ 1 MeV $n_{eq}cm^{-2}$, MAPS es una opción viable para la actualización del ITS.

La contribución original de esta tesis es la implementación de una nueva arquitectura digital de lectura de píxeles para MAPS. Esta tesis presenta un codificador asíncrono de direcciones (arquitectura basada en la supresión de ceros transmitiendo la dirección de los píxeles excitados denominada PADRE) para la arquitectura ALPIDE, el autor también hizo una contribución significativa en el ensamblaje y verificación de circuitos. PADRE es la principal investigación del autor, basada en un codificador de prioridad jerárquica de cuatro entradas y es una alternativa a la arquitectura de lectura rolling-shutter.

Además de los prototipos a pequeña escala, también se han desarrollado prototipos a escala completa a las necesidades del detector ITS (15 mm y 30 mm) empleando un nuevo circuito de lectura basado en la versión personalizada del circuito PADRE. El pALPIDEfs fue el primer prototipo a escala completa y se caracterizó obteniendo un tiempo de lectura de la matriz por debajo de 4 $\mu$s y un consumo de energía en el orden de 80 mWcm$^{-2}$. En general, los resultados obtenidos representan un avance significativo de la tecnología MAPS en cuanto al consumo de energía, velocidad de lectura, tiempo de recolección de carga y tolerancia a la radiación.

El sensor pALPIDE2 ha demostrado ser una opción muy atractiva para el nuevo detector ITS, satisfaciendo los requerimientos en términos de eficiencia de detección, fake-hit rate y resolución de posición, ya que su rendimiento no puede alcanzarse mediante prototipos basados en la arquitectura de lectura tradicionales como es el rolling-shutter diseñado en la misma tecnología. Por esta razón, la I+D en los prototipos ALPIDE ha continuado con el objetivo de optimizar aún más el rendimiento del sensor especialmente en términos del tiempo muerto y estudiar soluciones en otros aspectos de sistemas de integración.

El último circuito de ALPIDE, el pALPDIE3B, consume menos de 50 mW cm$^{-2}$ con una máxima tasa de transmisión de 1,2 Gbps y tiene una eficiencia a la reconstrucción de trazas superior al 99,95 %. Con un margen operativo satisfactorio después de irradiación con una fluencia equivalente de $1 \times 10^{13}$ 1 MeV n$_{eq}$cm$^{-2}$. Además, validando un consumo de energía por debajo de 50 mW cm$^{-2}$ y una resolución de posición de unos 5 $\mu$m y una velocidad de lectura aproximada de 2 $\mu$s, cumpliendo con las especificaciones ALICE ITS para su actualización.

Los resultados obtenidos de la caracterización del pALPIDE3B, la fase optimización de los circuitos y de prototipos se finaliza y da pie al inicio de la producción en masa del chip ALPIDE para el año 2017. El nuevo detector ITS se instalará durante el segundo gran parón del LHC en el año 2020 en la caverna de ALICE.

# Abstract

ALICE (A Large Ion Collider Experiment) is the heavy-ion experiment at the Large Hadron Collider (LHC) at CERN. As an important part of its upgrade plans, the ALICE experiment will schedule the installation of a new Inner Tracking System (ITS) during the Long Shutdown 2 (LS2) of the LHC. The new ITS layout will consist of seven concentric layers, $\approx 12.5$ Gigapixel camera covering about 10m$^2$ with Monolithic Active Pixel Sensors (MAPS). This choice of technology has been guided by the tight requirements on the material budget of 0.3% X/X$_0$ per layer for the three innermost layers and backed by the significant progress in the field of MAPS in recent years. The technology initially chosen for the ITS upgrade is the TowerJazz 180 nm CMOS Technology. It offers a standard epitaxial layer of 15 - 18 $\mu$m with a resistivity between 1 and 5 k$\Omega$ cm$^{-1}$ and a gate oxide thickness below 4 nm, thus being more robust to Total Ionizing Dose (TID).

The main subject of this thesis is to implement a novel digital pixel readout architecture for MAPS. This thesis aims to study this novel readout architecture as an alternative to the rolling-shutter readout. However, this must be investigated through the study of several chip readout architectures during the R&D phase. Another objective of this thesis is the study and characterization of TowerJazz, if it meets the Non-Ionizing Energy Loss (NIEL) and Single Event Effects (SEE) of the ALICE ITS upgrade program.

Other goals of this thesis are:

- Implementation of the top-down flow for this CMOS process and the design of multiple readouts for different prototypes up to the assembly of a full-scale prototype.

- Characterization of the radiation hardness and SEE of the chips submitted to fabrication.

- Characterization of full custom designs using analog simulations and the generation of digital models for the simulation chain needed for the verification process.

- Implementation and study of different digital readouts to meet the ITS upgrade program in integration time, pixel size and power consumption, from the conceptual idea, production and fabrication phase.

Chapter 1 is a brief overview of CERN, the LHC and the detectors complex. The ALICE ITS will be explained, focusing on the ITS upgrade in terms of detector needs and design constraints. Chapter 2 explains the properties of silicon detectors and the detector material and the principles of operation for MAPS. Chapters 3 and 4 describe the ALPIDE prototypes and their readout based on MAPS; this forms the central part of this work, including the multiple families of pixel detectors fabricated in order to reach the final design for the ITS. The ALPIDE3/pALPIDE3B chip, the latest MAPS chip designed, will be explained in detail, as well focusing in the matrix digital readout. In chapter 5 the noise measurements and its characterization are presented including a brief summary of detector response to irradiation with soft X-rays, sources and particle beams.

# Acknowledgements

First and foremost, I would like to thank Dr. Carlos Solans and Dr. Alberto Valero Biot who have supported me during these years and always given me advice when needed and gratefully acknowledged for reviewing this thesis, also to Dr. Bruce Mellado for his support and pressure for finishing this research. To my supervisors Walter Snoeys for giving me this opportunity to pursue my PhD. I am grateful to Raúl Esteve Bosch for supervising me at the Polytechnic University of Valéncia during my thesis work. Special thanks also go to Dr. Luciano Musa for trusting my skills and giving me the chance to work in Switzerland at CERN, and Finally, my warmest thanks go to Dr. Richard Teuscher for reviewing this thesis, and for taking the time to be my opponent in the defense of this thesis.

I would like to thank my colleagues in the CERN EP-ESE-ME group for many discussions on microelectronics and tools. Thanks to Wojciech, Xavi, Sandro, Szymon, Pedro, Isaac and Rui.

The work described in this thesis is the result of a big collaboration with many people involved in the ALICE ITS upgrade project. Also special thanks to all the people in the WP5 team: Magnus, Felix, Markus, Jacobus, Hartmut, Petra, Monica and Krzysztof, Hyeonjoong and the rest. I want to thank Thanu, for sharing the office, and always having an open ear for all the ideas that came into my mind throughout the last five years. Also, including the WP3 team: Constanza, Gianluca, Alessandra, Daehyoek, Seingjoo, Ping, Chaosong, Jerome and Herve.

Major thanks go to my family. I know they did not appreciate my absence, but I received a lot of support from you nevertheless. To Karlita my niece, who show me that the life is different and, who has brought so much joy into my life, thank you.

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# Chapter 1

# CERN, the LHC and the ALICE ITS upgrade program

Over the last 60 years, CERN has been a model of international scientific collaboration and one of the most important research centers in the world of particle physics. The name of CERN is derived from the acronym in French *Conseil Européen pour la Recherche Nucléaire* and it is located across the French-Swiss border in the Geneva canton, founded on the $29^{th}$ of September 1954 [1, 2].

CERN's success is not only based on its ability to produce scientific results of great interest, or the study of the particles of which matter is made of, but also because of the development of new technologies. Among them, early in the 1990's the World Wide Web (WWW) began as a CERN project. It was based on the concept of hypertext which was intended to facilitate sharing of information among researchers around the world. A plate is dedicated in one of corridors of the organization to the team who conceived the WWW (see Figure 1.1).

CERN's research infrastructure is primarily an interconnected set of particle accelerators and detectors of which the biggest one is the Large Hadron Collider (LHC), which became operational in 2008. Accelerators boost bunches of particles to high energies before the beams collide with each other or with stationary targets in the centre of the detectors that observe and record the results of these collisions [3].

**Figure 1.1:** Plate in recognition of the invention of the the World Wide Web.

CERN celebrated the discovery of the Higgs boson on the $4^{th}$ of July of 2012 by the ATLAS and CMS experiments. A new Higgs-like particle had been observed with mass of $m_H = 125.09 \pm 0.24$ (0.21 statistical $\pm$ 0.11 systematic) GeV, which was the last missing piece of the Standard Model (SM). Nowadays researchers study the properties of the new boson and search for new physics beyond the SM (supersymmetry and dark matter).

Figure 1.2 shows the candidate Higgs boson events from collisions in the center of the experiments. The top figure in the CMS experiment shows a decay into two photons (dashed yellow lines and green towers). The lower figure in the ATLAS experiment shows a decay into four muons (red tracks).

Between the $28^{th}$ and $29^{th}$ of September of 2013, CERN held two major events for the general public: the CERN Open Days, in which the laboratory was open to the general public and the experiments could be visited, guided by many physicist and engineering collaborators. Figure 1.3 shows a member of the open days crew during a visit to the ALICE experiment cavern.

In 2014 CERN celebrated its $60^{th}$ anniversary with the good performance of the LHC. The United Nations Economic and Social Council (ECOSOC) and CERN celebrated science for peace and development highlighting the values of science and its ability to build bridges between nations. The event was the last in a series of celebrations organized by CERN.
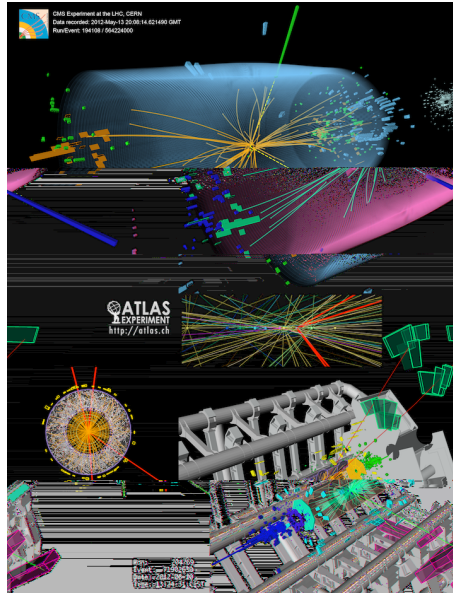
**Figure 1.2:** Candidate Higgs boson events at $\sqrt{s} = 13$ TeV in the CMS (top) and ATLAS(bottom) experiments the LHC[4].



**Figure 1.3:** An offical guide during the CERN open days in 2014.

**Figure 1.4:** Picture of the LHC tunnel [5].

## 1.1 The LHC

The LHC is the world's largest and most powerful particle accelerator. Figure 1.4 shows a section of the LHC tunnel. The LHC machine was built inside the Large Electron Positron (LEP) tunnel, which was a circular collider with a circumference of 27 km straddling the border of Switzerland and France, which operated between 1989 until the end of 2000 and led to the world's most precise measurements of the $Z^0$ boson.

The LHC accelerates and collides protons (p) at a centre-of-mass energy of $\sqrt{s} = 13$ TeV as well as lead (Pb) ions at centre-of-mass energy per nucleon of $\sqrt{s_{NN}} = 2.76$ TeV, and plans are to increase these energies to their design values of 14 TeV and 5.5 TeV, respectively [1] with an instantaneous luminosity exceeding $10^{34}$ cm$^{-2}$ s$^{-1}$.

The LHC beam parameters are detailed in Table 1.1.

Protons are produced by a duoplasmatron source that ionizes hydrogen gas with an electric field. The protons have a kinetic energy of 100 keV after leaving the source. They enter a linear accelerator Linac that uses Radio-frequency (RF) cavities to increase the proton energy
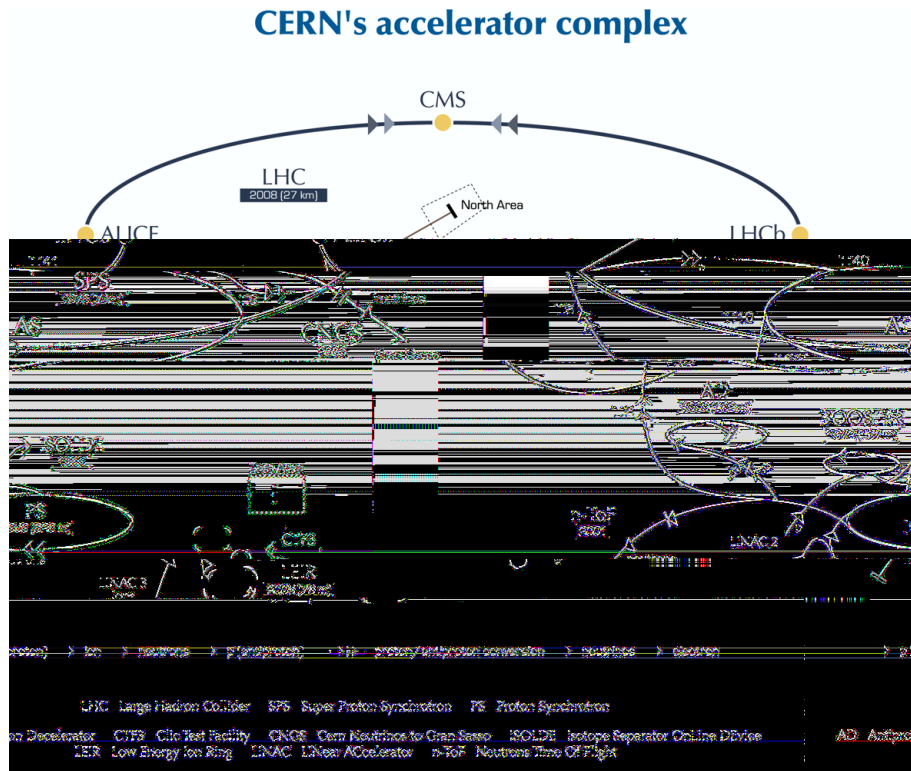
**Figure 1.5:** CERN's accelerators complex [6].

up to 50 MeV. The Proton Synchrotron Booster (PSB) then accelerates the protons up to 1.4 GeV, from where they are injected into the Proton Synchrotron (PS). The PS accelerates the protons to 25 GeV and splits the beam into smaller bunches of 4 ns length with a spacing of 25 or 50 ns as required by the LHC operation. The Super Proton Synchrotron (SPS) increases the proton beam energy to 450 GeV before the beams are finally injected into the LHC for further acceleration, from 450 GeV to 6.5 TeV per beam. Finally, beams cross at the center of the experiments and produce inelastic collisions interesting for the physics program of the LHC. Figure 1.5 summarizes the the accelerators complex and the experiments at CERN.

| | |
|---|---|
| Injection energy per beam | 450 GeV |
| Collision energy per beam | 7000 GeV |
| Nominal number of particles per bunch | $1.15 \times 10^{11}$ |
| Nominal number of bunches per fill | 2808 |
| Nominal luminosity | $10^{34}$ cm$^{-2}$ s$^{-1}$ |
| Inelastic pp cross section | 60 mb |
| Total pp cross section | 100 mb |
| Bunch revolution frequency | 11.245 kHz |
| Bunch frequency | 40.08 MHz |
| Circumference length | 26.66 km |
| Radius | 4.24 km |
| Number of dipole magnets | 1232 |
| Number of quadrupole magnets | 392 |
| Nominal magnetic field strength | 8.33 T |

**Table 1.1:** LHC nominal beam parameters [7] .

The LHC physics program involves upgrades for high luminosity running starting after the Long Shutdown 2 (LS2) scheduled for 2019 and beyond (see Figure 1.6).
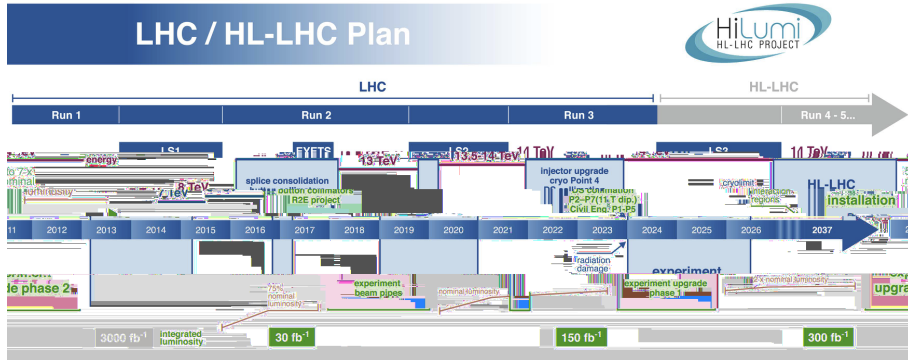


**Figure 1.6:** Time line of the LHC Long Shutdown periods [8].

The four main experiments of the LHC are ATLAS, CMS, LHCb and ALICE.

### 1.1.1 The ATLAS Experiment

The ATLAS experiment [9] is a multi-purpose detector about 45 meters long, more than 25 meters high and an overall weight of approximately 7000 tonnes. The detector is divided into sub-detectors as shown in Figure 1.7. ATLAS is designed to work at high luminosity ($10^{34}$ cm$^{-2}$ s$^{-1}$) with a bunch crossing every 25 ns. Therefore, the detector is built with highly sophisticated technologies and specialized materials. After the successful operation in Run 1 and the electronics consolidation campaign during the LS1, ATLAS is taking data again at $\sqrt{s} = 13$ TeV.
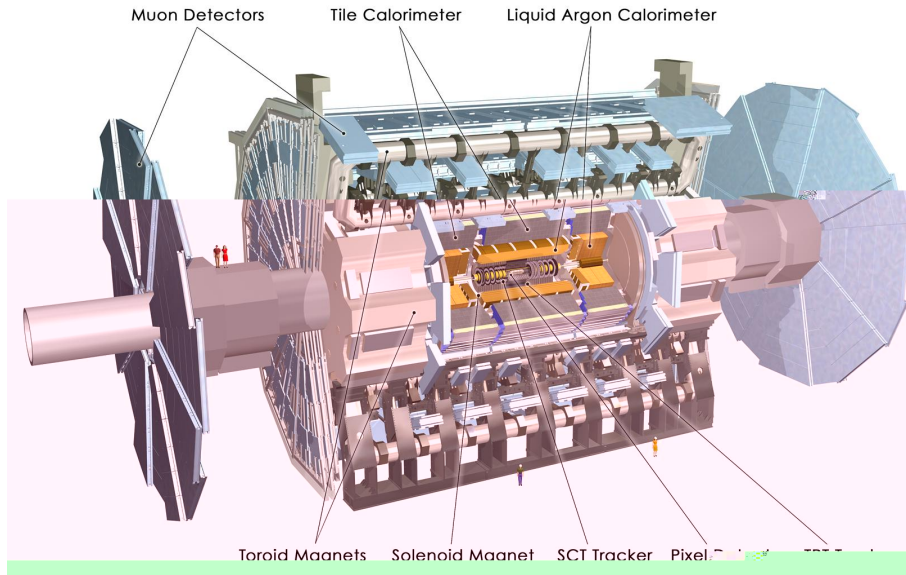


**Figure 1.7:** Artistic view of the ATLAS experiment [10].

The ATLAS inner detector is built around the beam pipe and is designed especially for tracking and vertexing. It is formed by the Pixel, the SCT (SemiConductor Tracker) and the TRT (Transition Radiation Tracker) detectors, that measure the trajectories of charged particles.The inner detector is embedded in a solenoidal magnet which generates a magnetic field of 2 T. The curvature of the trajectories which result from the the magnetic field bending power, is used to calculate the momentum of the particles. Additionally, the TRT pro-

vides electron identification measuring transition radiation photons generated in its radiator material. The electromagnetic and hadronic calorimeters surround the solenoid magnet and are designed to measure the energy of the different kinds of particles. The last layer of the detector is a huge muon spectrometer embedded in a toroidal magnet. The muon tracking system measures the trajectories of charged particles leaving the calorimeters. The trajectories are bent by the magnetic deflection provided by three superconducting air-core toroid magnets, which generate a field of 4 T.

### 1.1.2   The CMS Experiment
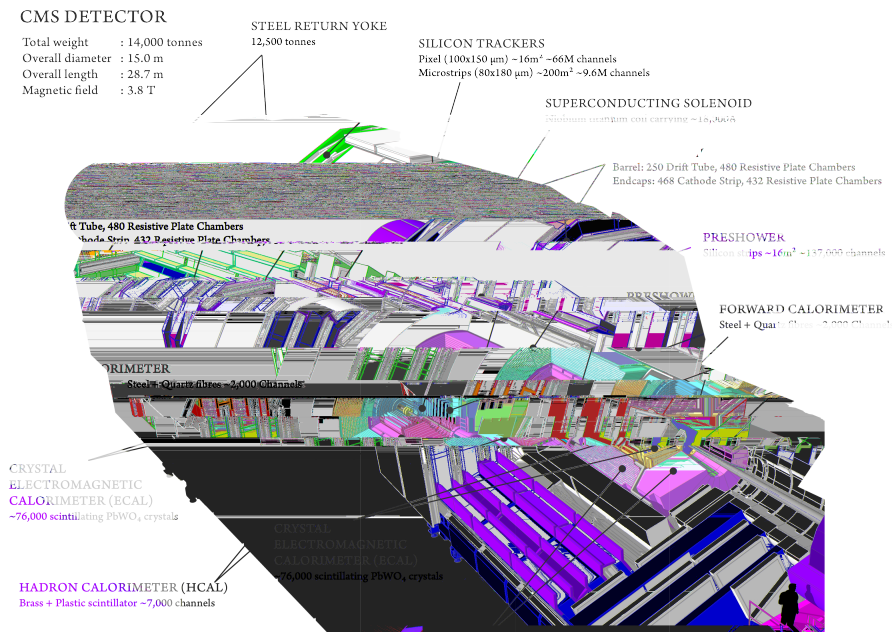


**Figure 1.8:** Artistic view of The CMS experiment [11].

The CMS (Compact Muon Solenoid) experiment [12] was built as a multi-purpose particle detector to study proton-proton, proton-lead, or lead-lead collisions at the TeV scale. It has large dimensions, being 22 m in length and 15 m in diameter, and a weight of 14.000 tonnes (see Figure 1.8). In the CMS detector each layer is specialized in detecting different types of particles. It covers nearly the full solid

angle of $4\pi$ around the nominal interaction point. The distinctive characteristic feature of the CMS apparatus is the superconducting solenoid. Contained within the field volume are a silicon pixel and strip tracker, a crystal Electromagnetic Calorimeter (ECAL) and a brass/scintillator Hadron Calorimeter (HCAL). Muons are measured in gas-ionization detectors embedded in the steel return yoke.

### 1.1.3 The LHCb experiment
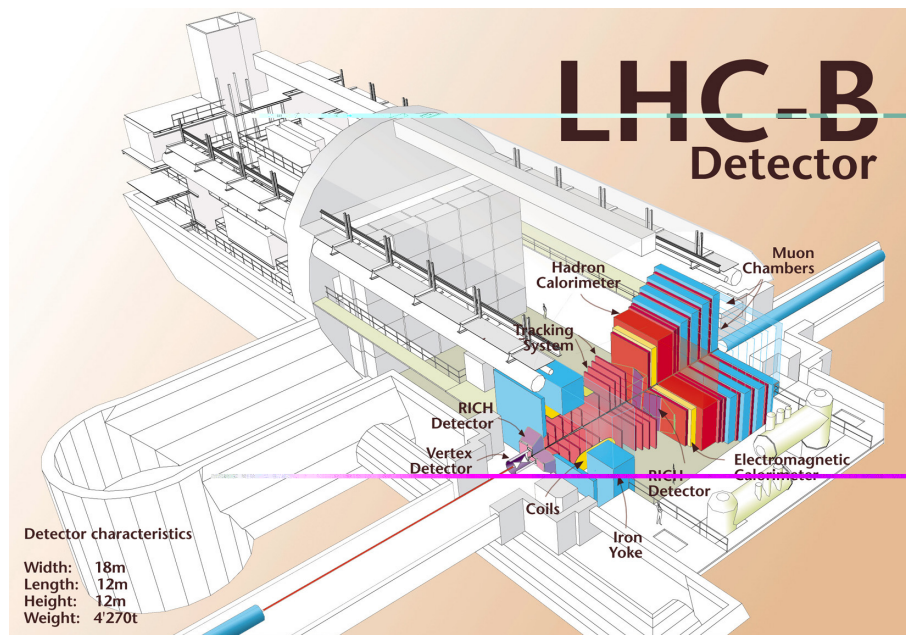


**Figure 1.9:** Artistic view of the LHCb Detector characteristics [13].

The LHCb experiment [14] specializes in investigating the slight differences between matter and antimatter by studying beauty quarks. hence the Large Hadron Collider beauty detector at the LHC. Figure 1.9 shows the LHCb experiment layout.

Instead of surrounding the entire collision point with an enclosed detector as ATLAS and CMS do, the LHCb experiment uses a series of subdetectors to detect mainly particle showers produced forward in the collision. The first subdetector is mounted close to the interaction

point, with the others following one behind the other over a length of 20 meters.

An abundance of different types of quarks are created in the interaction before they decay quickly into other particles. To record the b quarks, LHCb has developed sophisticated movable tracking detectors close to the path of the beams circling in the LHC. Figure 1.9 shows the layout of the LHCb experiment.
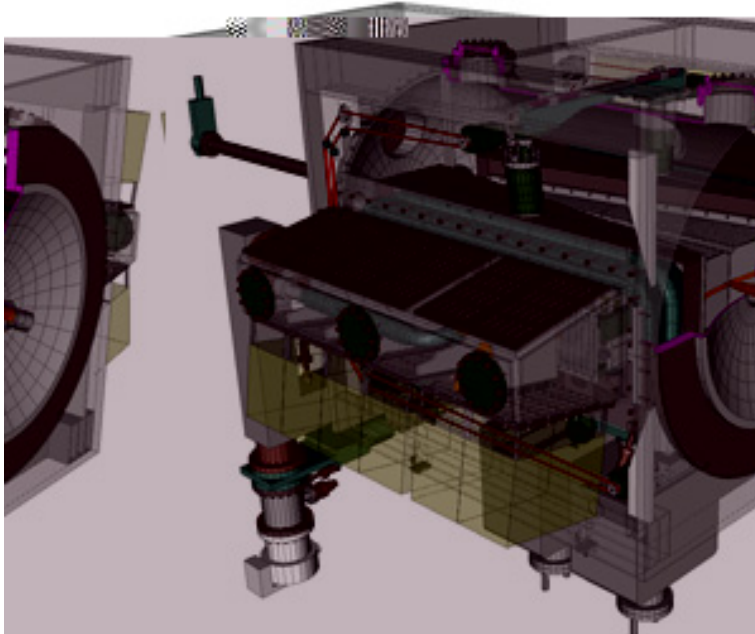


**Figure 1.10:** VELO detector layout of LHCb [15].

The VErtex LOcator "VELO" is the part of the LHCb detector closest to the collisions at the LHC. Its sensitive elements are Si detectors and during operation these are only 8 mm away from the beam. Its proximity to the interactions allows physicists to observe the decays of short lived particles, called B-mesons. The Bs have the property of decaying rapidly, in about one millionth of a millionth of a second. The VELO has been designed to perform an accurate measurement of their decay positions [15]. Figure 1.10 shows the VELO detector layout.

## 1.2 ALICE

ALICE (A Large Ion Collider Experiment) [16] is a general-purpose, heavy-ion detector located at point 2 of the LHC ring [3]. It is designed to study the physics of strongly interacting matter, and in particular the properties of the Quark-Gluon Plasma (QGP), using pp, pPb and PbPb collisions at the LHC. The QGP is the state of matter in which quarks and gluons are deconfined, i.e. where they are not bound into hadrons but may move around freely. It is assumed that this was the state of our universe shortly after it was born with the Big Bang (at the age of 1 ps to 10 $\mu$s) and it is the state that is created in collisions of high-energy heavy ions as they currently happen at the LHC [16].

The ALICE apparatus as seen in Figure 1.11, consists of a central barrel, which measures hadrons, electrons, and photons, and a forward muon spectrometer along with some smaller detectors for trigger and event characterisation. It has dimensions of 26 m in length and 16 m in diameter, and a weight of 10 000 tonnes.
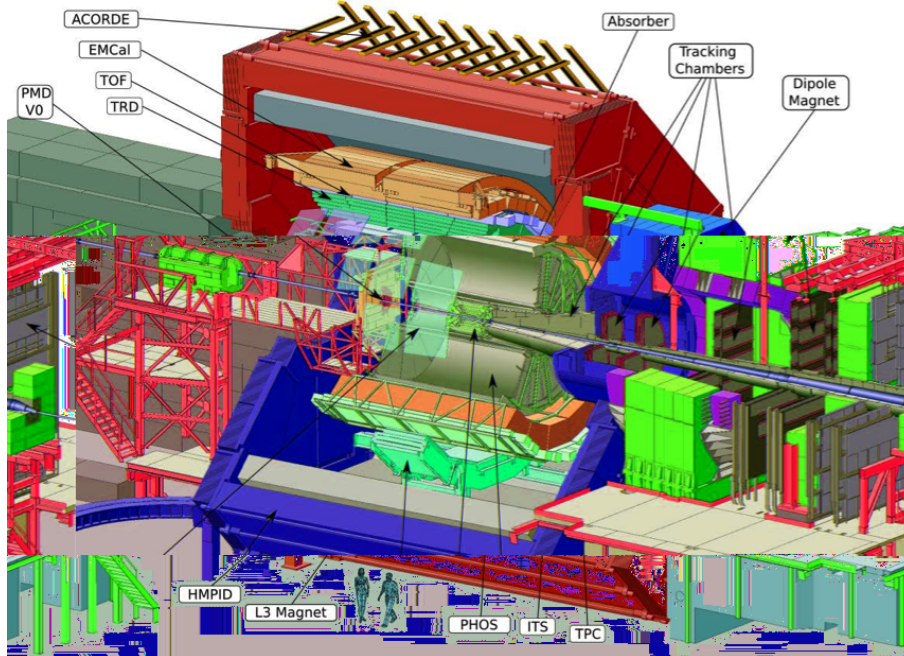


**Figure 1.11:** Layout of ALICE detector set-up, showing its division into subdetectors.

The central barrel is mounted inside a solenoidal magnet which provides a magnetic field of 0.5 T parallel to the beam axis. The detectors in the central barrel are mainly dedicated to vertex reconstruction, tracking, particle identification and momentum measurement. The main tracking detectors in the central barrel are the Time Projection Chamber (TPC) [17] and the Inner Tracking System (ITS)[18]. The ITS performs vertexing and is composed of six layers of silicon detectors: two layers each of Silicon Pixel Detector (SPD), Silicon Drift Detector (SDD) and Silicon Strip Detector (SSD) [19]. The other detectors in the central barrel are the Time Of Flight (TOF) detector [20] for particle identification, High Momentum Particle Identification (HMPID) [21], the Transition Radiation Detector (TRD) [22] counters for electron identification and two electromagnetic calorimeters, the Photon Spectrometer (PHOS) [23] and electromagnetic calorimeter (EMCAL) [24]. There are other smaller detectors for trigger and multiplicity measurement: the Photon Multiplicity Detector (PMD) [25], Forward Multiplicity Detector (FMD), V0 and T0 [26]. There are two sets of hadronic calorimeters which provide the centrality measurements: the Zero Degree Calorimeters (ZDC) [27] located on both sides of ALICE along the beam line at 115 m from the interaction point. In addition, there is an array of scintillators named ACORDE installed on top of the solenoid to trigger on cosmic rays for calibration purposes.

The acceptance in $\eta$ is calculated from the nominal interaction point and is 360° in azimuth, unless noted otherwise. The position is the approximate distance from the interaction point to the face of the detector and corresponds to the radius for barrel detectors (inner and outer radius for the TPC and TRD) or the position along the beam ($z$ coordinate) for the others. The term "Channels" refers to the total number of independent electronic read-out channels, as seen in Table 1.2.

The global coordinate reference system of ALICE is the following: the z axis is on the beam line, with positive z-axis pointing in the direction opposite to the muon spectrometer, the x axis is on the LHC (horizontal) plane, pointing to the center of the accelerator, and the y axis point upwards. In the transverse plane, the cylindrical

coordinates $r$ and $\phi$ localize the radial coordinate of the point with respect to the center of axis and the azimuthal angle measured from x to y respectively. Table 1.2 summarizes the spatial position of the ALICE subdetectors including the number of quantity of channels and the acceptance.

| Detector | Acceptance $(\eta, \phi)$ | Radial Position(mm) | Channels |
|---|---|---|---|
| ITS Layer 1 (SPD) | $\pm 2$ | 39 | 9.8M |
| ITS Layer 2 (SPD) | $\pm 1.4$ | 76 | |
| ITS Layer 3 (SDD) | $\pm 0.9$ | 150 | 133k |
| ITS Layer 4 (SDD) | $\pm 0.9$ | 239 | |
| ITS Layer 5 (SSD) | $\pm 0.97$ | 380 | 2.6M |
| ITS Layer 6 (SSD) | $\pm 0.97$ | 430 | |
| TPC | $\pm 0.9$ at r= 2.8 m | 848 | 557.568k |
| | $\pm 1.5$ at r = 1.4 m | 2,466 | |
| TRD | $\pm 0.84$ | 2,900 | 1.2M |
| | | 3,680 | |
| TOF | $\pm 0.9$ | 3,780 | 157.248k |
| HMPID | $\pm 0.6$, $1.2° < \phi < 58.8°$ | 5,000 | 161.280k |
| PHOS | $\pm 0.12$, $220° < \phi < 320°$ | 4,600 | 17.920k |
| EMCal | $\pm 0.7$, $80° < \phi < 187°$ | 4,360 | 12.672k |
| ACORDE | $\pm 1.3$, $-60° < \phi < 60°$ | 8,500 | 0.12k |

**Table 1.2:** Summary of the ALICE detector subsystems [16].

The forward muon spectrometer is designed to study single muon and di-muon events and consists of a combination of the tracking and trigger chambers, absorbers and a dipole magnet.

### 1.2.1 The ITS

The purpose of the ITS is to localize the primary vertex with a resolution better than 100 $\mu$m, to reconstruct the secondary vertices from the decays of hyperons and D and B mesons, to track and identify particles with momentum below 200 MeV, to improve the momentum and angle resolution for particles reconstructed by the Time-Projection Chamber (TPC) and to reconstruct particles traversing dead regions of the TPC. The ITS therefore contributes to practically all physics topics addressed by the ALICE experiment, as discussed in detail in [29].
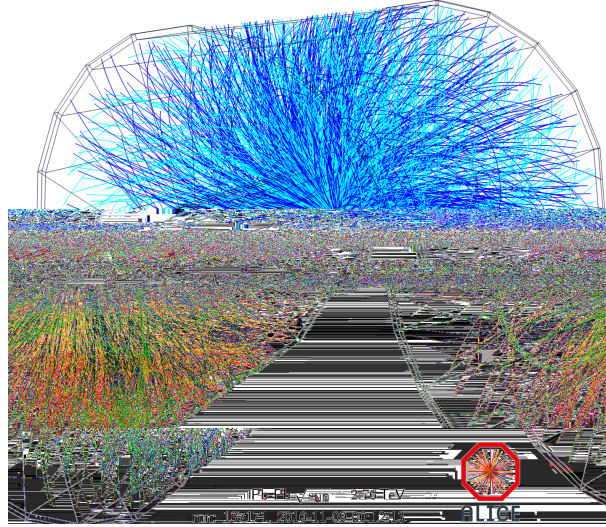
**Figure 1.12:** ALICE event display of a PbPb collision at 2.76A TeV [28].

The ITS consists of six layers of three different types of silicon detectors placed coaxially around the beam pipe with their radii ranging from 3.9 cm to 43 cm, as seen in Table 1.3. They cover a pseudorapidity range of $|\eta| < 0.9$ for vertices located within $z = \pm60$ mm with respect to the interaction point. To sustain a high particle hit density and perform an efficient vertex reconstruction, the first two inner layers are made of SPDs with state-of-the-art hybrid pixel detectors. The two middle layers are made of SDDs followed by two layers of double sided SSDs. The Inner Barrel (IB) consists of the first 2 SPD layers, and the Outer Barrel (OB) is made up of the remaining 2 SDD and SSD layers. The OB layers have analog read-out with Particle Identification PID capabilities through $dE/dx$ measurements in the non-relativistic $(1 \gg \beta^2)$ region.

The first layer has more pseudo-rapidity coverage ($|\eta| < 1.98$) to provide, together with the FMD, continuous coverage for the measurement of charged particle multiplicity. The detectors and front-end electronics are held by lightweight carbon-fibre structures. The geometrical dimensions and the technology used in the various layers of the ITS are summarized in Figure 1.13

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| Layer | Technology | Radial (mm) | Resolution ($\mu$m) r$\phi$ | $z$ |
|-------|-----------|-------------|------------------|-----|
| 1 | pixel | 39 | 12 | 100 |
| 2 | | 76 | | |
| 3 | drift | 150 | 35 | 25 |
| 4 | | 239 | | |
| 5 | strip | 380 | 20 | 830 |
| 6 | | 430 | | |

**Table 1.3:** Properties of the current ITS layers [30].
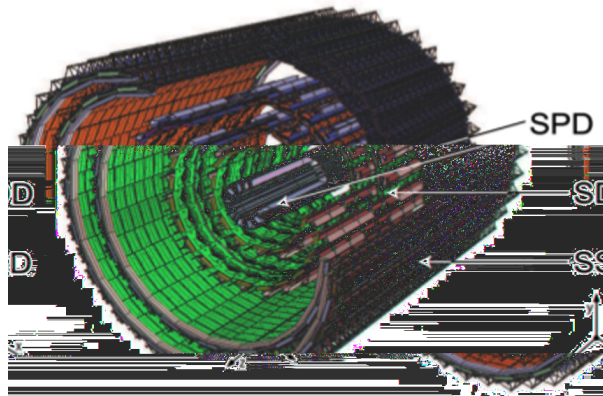


**Figure 1.13:** The ALICE ITS made out of six concentric barrels 2 layers of SPD, 2 layers of SDD, and 2 layers of SSD [30].

One disadvantage of the current ITS is its limited maximum read-out rate of 1 kHz with a high dead time. This is a crucial limitation since it prevents ALICE from exploiting fully the PbPb collision rate of 8 kHz, which the LHC can deliver at the present.

### 1.2.2 The ALICE upgrade strategy

The upgrade strategy for ALICE is formulated on the fact that after the LS2, the LHC will provide PbPb collisions at an interaction rate of up to 50 kHz, corresponding to an instantaneous luminosity, $\mathcal{L} = 6 \times 10^{27} \text{cm}^{-2}\text{s}^{-1}$. To achieve this luminosity and to perform the measurements defined by the upgrade program, detector upgrades are necessary to improve tracking and vertexing capabilities, radiation hardness and allow the read-out of all interactions to accumulate

enough statistics for the upgrade physics program. The objective is to accumulate 10 nb$^{-1}$ of PbPb collisions, recording about $10^{11}$ interactions.

The ALICE upgrade is planned for installation during the LS2. A key element of the ALICE upgrade is the construction of a new, ultra-light, high-resolution ITS. The upgrades include:

- A new beampipe with smaller diameter.

- Inner Tracking System (ITS) [31] covering mid-pseudo-rapidity ($-1.2 < \eta < 1.2$).

- Muon Forward Tracker (MFT) [32] covering forward pseudo-rapidity ($-3.6 < \eta < 2.45$).

- Upgrade of the Time Projection Chamber (TPC), consisting of the replacement of the wire chambers with Gas Electron Multiplier (GEM) detectors and new pipelined read-out electronics.

- Upgrade of the read-out electronics of Transition Radiation Detector (TRD), Time Of Flight detector (TOF), and Muon Spectrometer for high rate operation.

- Upgrade of the forward trigger detectors.

- Upgrade of the online systems and offline reconstruction and analysis framework.

The ALICE collaboration has decided to upgrade the ITS detector in order to improve its performance and address its current weaknesses. The CDR [33] and the TDR [31] of the ITS upgrade were submitted to the LHCC in December 2013, and approved by the CERN Research Board in March 2014 [34].

### 1.2.3 The ITS upgrade

As far as the physics performance in heavy flavour detection is concerned, the current ITS has significant limitations. For example, the study of charm baryons is not feasible with the current detector. The current ITS has an impact parameter resolution larger than the decay length of the $\Lambda_c$ baryon 60 $\mu$m which is the most abundantly produced charm baryon, thus making $\Lambda_c$ inaccessible in PbPb collisions in ALICE.

As we see in the previous sections, the requirements and needs for the new ITS will decrease the material budget and a smaller beam pipe will be designed and placed in the experiment. The ITS resolution will be increased replacing the current ITS for a new set of silicon layers where the first detection layer will be closer to the beam line and the new ITS support structure must design facilities for services and maintenance. The current ITS is inaccessible for maintenance and repair interventions during the yearly LHC shutdowns. This could lead to a significant compromise in maintaining high data quality. So, it is a high priority in the design of the upgraded ITS to have rapid accessibility for maintenance.

For optimal performance, a tracking detector should be as close as possible to the interaction point. In fact, many particles of interest live for a very short time $\tau$ before disintegrating into the daughter particles. For example, the PbPb collisions at the LHC produce $D^0$ mesons that have lifetime $\tau \approx 4 \times 10^{-13}$s, during which they cover a distance of $c\tau \approx 120\mu$m. Then, they decay generating $K^-$ and $\pi^+$. In this case, given that the $D^0$ meson is a neutral particle, the only way to reveal it by using a tracking detector is to trace the trajectories of secondary particles and to localize the decay point.

The impact parameter $b$ depends on the energy of the particle, its lifetime $\tau$ and the angle between its direction of flight and the particles produced in the decay:

$$b = \gamma\beta c\tau \sin\theta \qquad (1.1)$$

For high momentum particles $\sin\theta \approx 1/\gamma\beta$ and therefore b $\approx$ c$\tau$ is equivalent to the distance traveled by the particles before they decay spontaneously. In this case the resolution doesn't depend on the magnitude of the particle's momentum. On the contrary, the resolution only depends on the detector's properties, like resolution and geometry, and the closer the detector is to the interaction point, the better the spatial resolution will be.

The reduction of the beam pipe diameter in the centre of the ALICE detector is one of the main strategies to improve the measurement of the impact parameter resolution and reconstruction of secondary vertices from decaying charm and beauty hadrons. The requirement for an efficient tracking in ITS standalone mode and in combination with the TPC drove the design and geometry of the layers of the upgraded ITS. This translates to a barrel geometry with seven layers and their radii optimized to fit the tracking requirements. Current studies [33] indicate that it should be possible to reach a beam pipe inner radius of 17.2 mm, which can be compared to the present value of 29 mm.

In order to identify the primary vertex, secondary tracks have to be fitted back from the hits in the detector to their point of origin. The spatial resolution for a pixel detector is described in Figure 1.14.

The spatial resolution for the ITS is in the order of 60 $\mu$m [16] and the developments for the ITS upgrade aim to reduce it to 5 $\mu$m (see Table 1.5). The spatial resolution is one of the most important parameters that will affect the resolution of the impact parameter. Spatial resolution is defined as the spatial information recorded by the two dimensional silicon sensors and refers to the size of the smallest possible position that can be detected.

Reducing the material budget is essential for improving the spatial resolution. In general, reducing the overall material budget by small pixel size and thin detectors on light carbon fibre supports will allow the tracking performance and momentum resolution to be significantly improved.

$$\Delta v = \Delta x \bullet \sqrt{\frac{r_2^2 + r_1^2}{\left(r_2 - r_1\right)^2}}$$
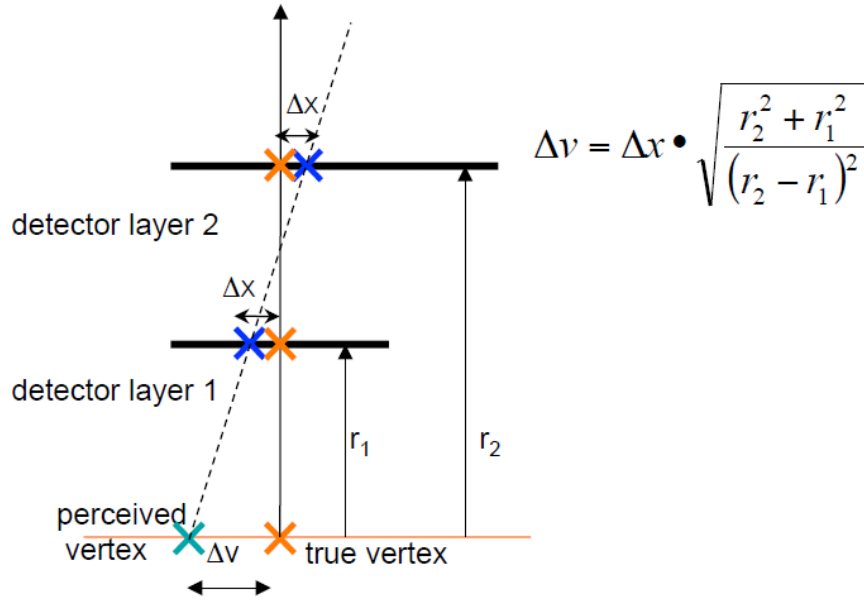
**Figure 1.14:** Relation between impact parameter resolution and spatial resolution for a pixel detector [35].

The IB has three layers, instead of two, and the OB has also 4 layers, as seen in Figure 1.15. This will form a total of seven concentric silicon detector layers as seen in Table 1.4. The CMOS pixel sensor with a small pixel size of $\approx 30 \times 30~\mu\text{m}^2$ is a key feature of the new ITS, which is optimized for high tracking accuracy at low transverse momenta. It allows for a very low mass of the three innermost layers, which feature a material thickness of 0.3% $X_0$ per layer.

Figure 1.15 shows the new beam pipe covered by the IB. A narrower beam pipe enables the installation of the first layer closer to the primary vertex, which in turn improves the impact parameter resolution by a factor 3. This, coupled with the higher interaction rate would require the sensor to be sufficiently radiation hard which was a requirement for the choice of the sensor technology. The sensor should also have faster read-out rates to be able to read out all the interactions.

| Layer | Lenght (mm) | Radius (mm) | Nominal z coverage (mm) | $\eta$ coverage | (Half-) staves[a] # | Chips (#) |
|-------|-------------|-------------|-------------------------|-----------------|---------------------|-----------|
| 0 | 271 | 23 | $\pm112$ | $\pm2.5$ | 12 | 108 |
| 1 | 271 | 31 | $\pm121$ | $\pm2.3$ | 16 | 144 |
| 2 | 271 | 39 | $\pm134$ | $\pm2.0$ | 20 | 180 |
| 3 | 843 | 194 | $\pm390$ | $\pm1.5$ | 44 | 2464 |
| 4 | 843 | 247 | $\pm418$ | $\pm1.4$ | 56 | 3136 |
| 5 | 1475 | 353 | $\pm712$ | $\pm1.4$ | 80 | 7840 |
| 6 | 1475 | 405 | $\pm743$ | $\pm1.3$ | 92 | 9016 |

[a]staves for the Inner Layers (0-2), Half-staves for Middle and Outer Layers(3-6)

**Table 1.4:** Nominal z-coverage of the ITS layers and z length of modules [31].
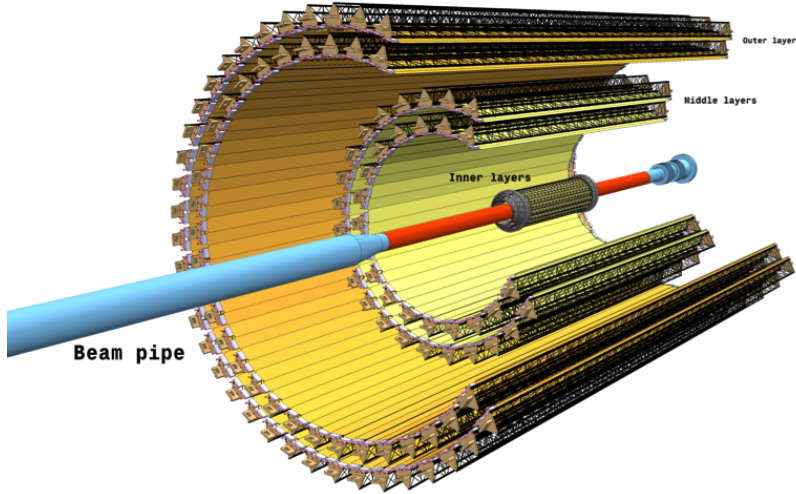


**Figure 1.15:** New ITS conceptual layout with 3 Inner layers and 4 Outer layers [33].

Another requirement for improving the impact parameter resolution is to improve the detector intrinsic resolution. This translates to a requirement of pixels with smaller feature size and low material budget. The selection of the pixel detector technology will be addressed in subsection 2.6.2.

The Table 1.5 summarizes the ITS general requirements in dimension, silicon thickness, radiation damage, fake hit rate and efficiency of the new ITS detector.

| Parameter | Inner Barrel | Outer Barrel |
|---|---|---|
| Chip dimension | $15 \times 30 \,\mathrm{mm}^2$ ($r\phi \times z$) | |
| Max. silicon thickness | $50 \,\mathrm{\mu m}$ | |
| Spatial resolution | $\leq 5 \,\mu\mathrm{m}$ | $\leq 10 \,\mu\mathrm{m}$ |
| Max. power density | $300 \,\mathrm{mW/cm}^2$ | $100 \,\mathrm{mW/cm}^2$ |
| TID radiation hardness[a] | $0.7 \,\mathrm{Mrad}$ | $10 \,\mathrm{krad}$ |
| NIEL radiation hardness[a] | $10^{13} \,1\,\mathrm{MeV}\,\mathrm{n_{eq}/cm}^2$ | $3 \times 10^{10} \,1\,\mathrm{MeV}\,\mathrm{n_{eq}/cm}^2$ |
| Operation temperature | $20\,^\circ\mathrm{C}$ to $30\,^\circ\mathrm{C}$ | |
| Max. integration time | $30 \,\mathrm{\mu s}$ | |
| Max. relative dead time | $10\,\%$ at $50\,\mathrm{kHz}$ PbPb | |
| Min. detection efficiency | $99\,\%$ | |
| Max. fake hit rate | $10^{-5}$/event/pixel | |
| Spatial resolution | $5 \,\mathrm{\mu m}$ | $30 \,\mathrm{\mu m}$ |

[a]This includes a safety factor of ten.

**Table 1.5:** General specifications of the ITS pixel chip [31].

## 1.3   ITS design and chip assembly constraints

In the azimuthal direction, each layer is segmented in staves, which extend over the whole length of the respective layer, and are the basic building blocks of the detector. The stave contains all structural and functional components, thus making it the smallest operable part of the detector. The three IB Layers are built with identical staves, while the staves of the OB Layers have a different layout due to their longer length. Layers 3 and 4 have same layout as 5 and 6 although they are half in size. The conceptual design as seen in Figure 1.16 [33] of both IB and OB staves is based on the following elements :

- **Space Frame:** a carbon fibre M55J-6K (540GPa) support structure providing the mechanical support and the necessary stiffness.

- **Cold Plate:** a sheet of high-thermal conductivity carbon fibre with embedded polyimide cooling pipes, which is either integrated within the Space Frame (for the IB staves) or attached to the Space Frame (for the OB staves), the Cold Plate is in thermal contact with the Pixel Chips or with the Module carbon plate to remove the generated heat.

- **Flexible PCB:** an assembly of a polyimide Flexible Printed Circuit (FPC) on which a number of Pixel Chips, namely 9 and 14
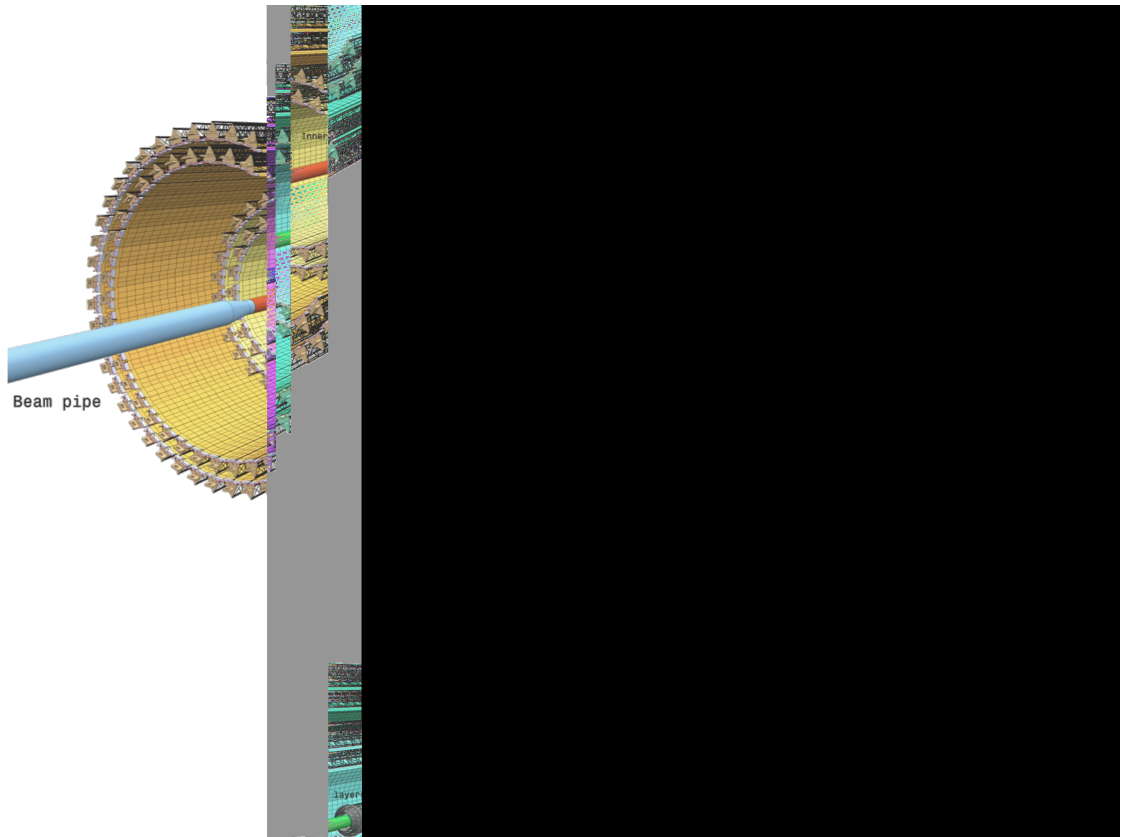
**Figure 1.16:** Schematic view of new ITS staves [31].

for the IB and OB staves respectively, and some passive components, are bonded;

- **Half-stave:** the OB staves are further segmented in azimuth in two halves, called Half- staves. Each Half-stave, extending over the full length of the stave, consists of a Cold Plate on which a number of Modules are glued, namely four and seven for Middle Layers and Outer Layers, respectively.

The chips will be soldered to the flexible PCB in the new stave layout as seen in Figure 1.16. The technique used for this is laser soldering, an industrial technique which can be used to connect the chip pad with the corresponding metal coated hole in the FPC, using a solder

ball which is melted locally by a laser beam, as schematically shown in Figure 1.17. Study to achieve required 99.5% yield in soldering quality (100% for signal connections) could not be completed in the available time. The ITS upgrade program had decided to use wire bonding technique [36]. Laser soldering still needs R&D work, but is a promising option.
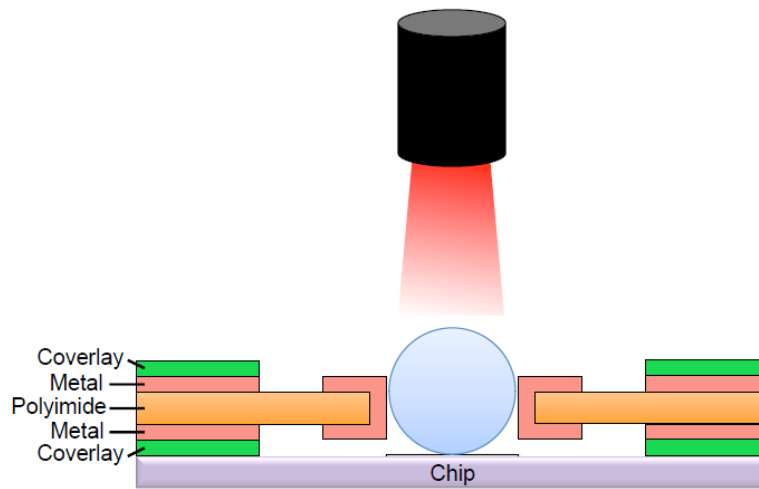


**Figure 1.17:** Schematic view of the laser soldering [31].

## 1.4   Conclusions and overview

One of the goals of the ITS upgrade is to increase the read-out of PbPb interactions rates higher several $10^5$ Hz, currently limited at 1 kHz with full ITS.

The ITS upgrade will improve the tracking efficiency and $p_T$ resolution at low $p_T$ by increasing the granularity from 6 layers to 7 layers, unifying the technology from strips and drift detectors to pixels detector. Furthermore, the spatial resolution will be improve by a factor 3, as a result of (i) placing the new ITS closer to the IP, whereby the first IB layer will move from radial distance of 39 mm to 23 mm, (ii) by a reduction of the material budget $x/X_0$ per layer from 1.14% to

0.3%, and (ii) a reduced pixel size from 50 $\mu$m x 425 $\mu$m to 30 $\times$ 30 $\mu$m$^2$ with a thickness of 50 $\mu$m.

The ALICE ITS upgrade is planned for the LS2 of the LHC. All requirements the Table 1.5 and the chip assembly constraints have had a significant impact on the ITS upgrade program. For the LS2 LHC upgrade scenario, the ALICE ITS detector is considered for a larger area coverage around 10 m$^2$ with $\approx$ 12 Gigapixel camera for pixels of $\approx$ 30 $\mu$m. Upgrade requirements are driven by the demands on high resolution (i.e. small size), low material budget, low power density and high speeds. The present hybrid technology with one-to-one coverage of the area with the sensor, front-end chips and module interconnect layer would contribute to a significant material budget issue. Cost would also be a factor for pixel detectors at larger radii. As result, the design, deployment, and exploration of new interconnection technologies, building new procedures for the cavern placement and the possibility to replace non functioning detector modules during yearly shut-downs are one of the big challenges.

Further improvement of these detection systems can be done in terms of higher granularity and reduced material budget if, for example, the sensor and the front-end read-out are implemented on a single silicon substrate. This approach led to the development of CMOS Monolithic Active Pixel Sensors (MAPS).

In the following chapters we are going to describe the usage of pixel detectors in HEP and the alternatives for pixel detector technologies for the ITS upgrade. The new developments for pixel detectors and experimental results when exposed to particle beams are presented.

# Chapter 2

# Silicon Pixel Detectors in High Energy Physics

In the previous Chapter, we briefly introduced CERN, the LHC and its experiments and we also presented a brief overview of the ALICE experiment and ALICE ITS upgrade.

This chapter gives an overview of pixel sensors and pixel read-out implemented in HEP experiments. Special attention is given to the radiation effects like Single Events Upset and radiation damage and mitigation techniques highly important in HEP.

The chapter starts with a brief review of the mechanism of interaction of radiation with matter and the working principle and detection principle of a pn junction, i.e the sensor key structure. We will review the physics principles that make up pixel detectors, with a description of the main radiation-induced effects which degrade their performance and their implications for in HEP experiments.

The principle of operation of a standard MAPS detector is described and the explanation of the main motivations behind the adoption on the TowerJazz 180 nm CMOS imaging sensor as a baseline for the ALICE ITS upgrade is explained. These MAPS sensors, they have many interesting features for a tracking detector, have some important constraints from the read-out point of view.

## 2.1 Interaction of particles with matter

Electromagnetic radiation interacts in semiconductor detectors in the form of three main processes: the photoelectric effect, the Compton effect and pair production. In these interactions, the incident radiation is either completely absorbed in the sensor material as in the photoelectric effect and pair production or is scattered (Compton effect). Thus, a monochromatic photon beam traversing the sensor material is attenuated in intensity:

$$I(x) = I_0 e^{-x/\mu} \tag{2.1}$$

where $I_0$ and $I(x)$ are the initial and final beam intensity after traversing a material of thickness $x$. The attenuation length, $\mu$, is a property of the medium and of the photon energy. At low energies (below 100 keV for silicon), the photoelectric effect is the dominant process. At higher energies, the scattering process becomes dominant. Silicon is used for photon detection up to energies of about 100 keV. A detailed description of these processes can be found in the literature [37].

### 2.1.1 Interaction with charged particles

The charged particles traversing the sensor undergo scattering processes with the electrons of the interacting medium. These processes are dominant for particles heavier than electrons and can be characterized by the average energy loss suffered by the particle, expressed by the Bethe-Bloch formula, which defines the requirement on the minimal detectable charge, typically releasing some 60 electrons per 1 $\mu$m path length in thin silicon layers:

$$-\frac{dE}{dx} = \kappa z^2 \cdot \frac{Z}{A} \frac{1}{\beta^2} \left[ \frac{1}{2} \ln \frac{2m_e c^2 \beta^2 \gamma^2 T_{max}}{I^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2} \right] \tag{2.2}$$

which is valid for $0, 1 \leq (\beta\gamma) \leq 1000$.

The factor $\kappa$ is given by $4\pi N r_e^2 m_e c^2$ with the classical electron radius $r_e = \frac{e^2}{4\pi\epsilon_0} \frac{1}{m_e c^2}$. The parameters are the charge z of the propagating particle in units of elementary charge, the atomic number Z of the absorber, the atomic mass of the absorber in g/mol, the mean excitation energy I in eV, the maximum loss of kinetic energy Tmax and the density-effect correction $\delta(\beta\ \gamma)$. The Bethe equation with corrections for lower and higher energies is illustrated in Figure 2.1 for positive charged muons in copper.

with,

$$\kappa = 4\pi N r_e^2 m_e c^2 \quad = 0.307075 MeV cm^2 g^{-1}$$

where,

$N$ = Avogadro's number,
$z$ = charge of the traversing particle in units of the electron charge,
$r_e$ = the classical electron radius,
$m_e c^2$ = electron rest mass energy,
$Z$ = atomic number of the sensor material,
$A$ = atomic mass of the sensor material,
$I$ = mean excitation energy,
$\beta$ = velocity of the traversing particle in units of the speed of light,
$\gamma$ = Lorentz factor $\left(\frac{1}{\sqrt{1-\beta^2}}\right)$.

There are additional correction terms, like the density correction for high particle energies and the shell correction for lower energies [38].

A charged particle propagating through matter is mostly interacting with the atomic electrons and thereby ionizing it, creating electron-ion pairs or exciting the atom. The maximum energy deposit $T_{max}$ of a particle in a single collision is given by:

$$T_{max} = \frac{2m_e c^2 \beta^2 \gamma^2}{1 + 2\gamma m_e/M + (m_e/M)^2} \tag{2.3}$$
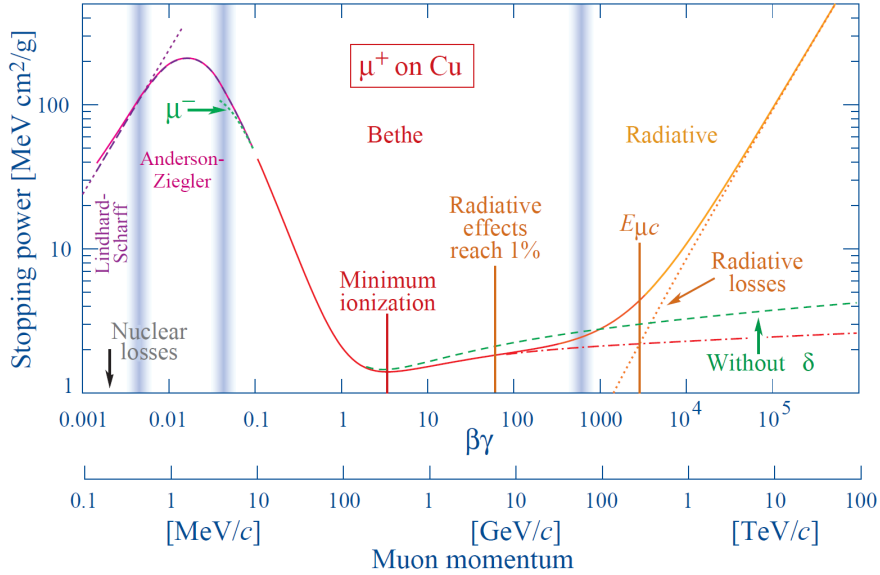
**Figure 2.1:** Stopping power in matter of muons in copper [39].

with the electron mass $m_e$, the speed of light c, the ratio between velocity and speed of light $\beta = v/\mathrm{c}$, the Lorentz factor $\beta$ and the particle mass M. This is valid for all particles but can be simplified to:

$$T_{max} = 2m_e c^2 \beta^2 \gamma^2 \tag{2.4}$$

If electrons are excluded, i.e. $m_e/\mathrm{M} \ll 1$, and assuming $2\gamma\, m_e/\mathrm{M} \ll 1$ is also valid. The mean energy loss of charged particles propagating through matter is given by the Bethe-Bloch formula Equation 2.2.

The number of charge carriers (electron and holes) generated in the semiconductor by the traversing particle is determined by dividing the deposited energy by the mean energy required for ionization (3.6 eV for silicon).

The ionization process during the passage of a charged particle through matter is subject to statistical fluctuation resulting in fluctuations of the energy loss in the medium. The equation 2.3 gives the average

energy loss per unit path length. The probability distribution of the energy loss depends on the thickness of the absorber.

For thick absorbers, the energy loss distribution has a Gaussian shape. In thin absorbers, the fluctuation is higher and the distribution is asymmetric. For silicon sensors, the energy loss distribution was calculated by Landau [40] and Vavilov [41]. Further corrections were incorporated later by Blunck and Leisegang [42], Shulek [43] and Bichsel [44].
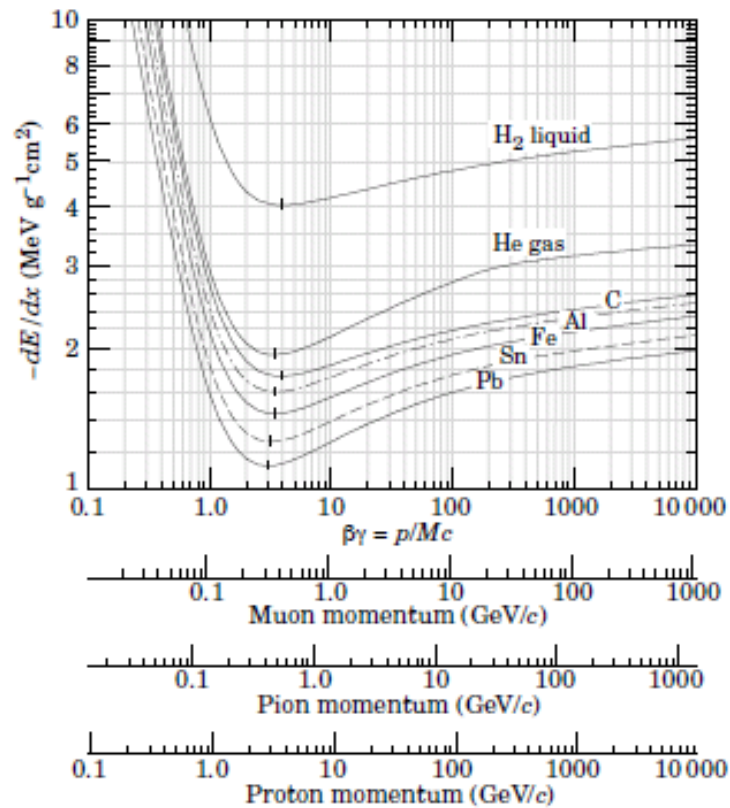


**Figure 2.2:** Simulated stopping power for muon, pion and electrons momemtun [39].

The stopping power for positive muons in copper is shown in Figure 2.2, as a function of $\beta\gamma = (p/m_\mu c)$ over nine orders of magnitude in momentum (12 orders of magnitude in kinetic energy).

The solid curves indicate the total stopping power and the vertical bands indicate boundaries between different approximations. The short dotted lines labeled $\mu^-$ illustrate the "Barkas effect", the dependence of stopping power on projectile charge at very low energies.

Figure 2.2 shows the simulation results for energy loss as a function of the particle momentum for different particle species.

Apart from energy loss, charged particles traversing a detector suffer from Multiple Coulomb Scattering, which can cause a deviation of the tracks and corrupt the measurement; this theme will be addressed in the next section.

### 2.1.2   Multiple scattering

The particles traversing a detector are subject to multiple Coulomb scattering. This results in small deviations of the tracks due to successive small angle defections symmetrically distributed around the incident direction. The scattering angle follows roughly a Gaussian distribution in rms.

Multiple scattering of a charged particle through matter contributes to the width of the energy deposits in a pixel detector. The effect of multiple scattering was studied by Moliére [39], leading to what we know as the Moliére radius in which the 90% of the energy of the shower is contained.

## 2.2   Silicon PN junction as a sensor

Silicon can be made n-type by doping with donors atoms or p-type by doping with acceptors. A PN junction can be created and this allows the creation of semiconductor devices of great variety and versatility, including diodes, thyristors, transistors, solar cells, LEDs, and more.

The resistivity of silicon doped with a $n_p$ density of acceptors and $n_n$ of donors is given by:

$$\rho = \frac{1}{q(\mu_n n_n + \mu_p n_p)} \tag{2.5}$$

The value of $\rho$ can be varied adjusting the density of the dopants. For example, by setting $n_p \ggg n_n$ the majority charge carriers in the material are the holes so the silicon resistivity is $\rho \approx 1/(q\mu_p n_p)$. The doping levels are typically $10^{14}$ to $10^{19}$ atoms/cm$^3$.

When two regions of a semiconductor are doped with complementary impurities, such as p-type and n-type regions, a PN junction is formed. Because of the gradient of concentrations of holes as well as electrons between the two regions in the material, thermal diffusion will drive the majority charge carriers across the junction, leaving in the p-type region an excess of negative ions and in the n-type an excess of positive ions. Therefore, a region of non-mobile space charge is formed. The potential barrier $V_{bi}$ is generated between the two space charge densities. This potential prevents electrons and holes from diffusing further. In other words, between the space charge densities the electrical field $\vec{E}$ is established and it accelerates particles of opposite charges in opposite direction.

No mobile charge carrier is present in the central zone of the junction which, for this reason, is named the depletion zone: its spatial extent $W$ depends on the doping levels with donors $N_D$ for the n region or acceptors $N_A$ for the p region:

$$W = \sqrt{\frac{2\epsilon_s V_{bi}}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)} \qquad (2.6)$$

where $\epsilon_s$ is the silicon dielectric constant and $q$ is the electrical charge. Since the density of the dopants is not symmetrical, $W$ is wider in the region in which the doping level is lower. For example, if we consider $N_D \gg N_A$, where the junction is asymmetrical with a very strong doping level of the n region (p − n$^+$), the depletion zone is more extended in the p region than in the n region.

Figure 2.3 shows the case of no current flow, has no bias. Called equilibrium when a PN junction is zero biased, that is has no bias, it just stays. The depletion region is free of majority carriers, electrons in the n-type material and holes in the p-type material, but under equilibrium conditions electron-hole pairs are generated continually

everywhere within the volume of the crystal. In the absence of an electric field the created carriers recombine. When an ionizing particle hits the PN junction and traverses the depletion zone, it deposits a fraction of their energy; the mean value of the energy loss per unit path length is simply described by the Bethe Bloch Equation 2.2. If however an electric field is present in the semiconductor, the pairs are separated and have little chance to recombine. Electrons and holes drift under the influence of the electric field giving rise to a current.
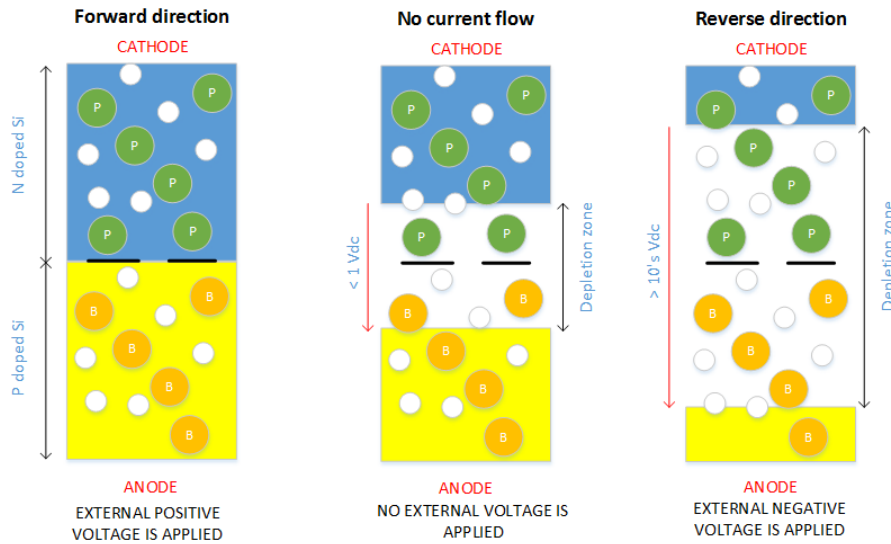


**Figure 2.3:** PN junction current flow scenarios.

Now, if the diode is reverse biased, i.e. then the positive terminal of the source is connected to the n-type end, and the negative terminal of the source is connected to the p-type end of the diode as we can see in Figure 2.3. In reverse current flow direction, there will be no current through the diode except reverse saturation current. This is because at the reverse biased condition the depletion layer of the junction becomes wider with increasing reverse biased voltage. However, there is a small current flowing from n-type end to p-type end in the diode due to minority carriers. This small current is called the reverse saturation current. Minority carriers are mainly thermally generated electrons and holes in the p-type and n-type semiconductor respectively. Now if a reverse applied voltage across the diode is con-

tinuously increased, then after a certain applied voltage the depletion layer will be destroyed which will cause a huge reverse current to flow through the diode. If this current is not externally limited and it exceeds the junction breakdown value, the diode may be permanently destroyed, as we can see in Figure 2.4 for the reverse direction.

Thermally generated carriers in the depletion region are swept up by the electric field, generating a leakage current. The leakage current depends on the intrinsic carrier concentration $n_i$ of the silicon ($n_i = 1.45 \times 10^{10} \text{cm}^{-3}$), the diffusion constant $D_{p,n}$ of both holes and electrons, the diffusion length $L_{p,n}$ of the charge carriers and on the diode. In a reverse bias the p node can provide more margin on the width of the depletion region allows a larger chance to collect charges by drift i.e when the ionizing charged particles traverses the depletion region.

$$I_s = -q[\frac{D_n}{L_n N_A} + \frac{D_p}{L_p N_D}]n_i^2 A \qquad (2.7)$$

Since the concentration of minority carriers is typically lower than that of the majority carriers, the current $I_s$ is very low, about a nA in silicon.

In a PN junction when the forward voltage is applied, i.e. the positive terminal of a source is connected to the p-type side, and the negative terminal of the source is connected to the n-type side, the diode is said to be in a forward biased condition. We know that there is a potential barrier across the junction. This potential barrier is directed in the opposite of the forward applied voltage. So a diode can only allow current to flow in the forward direction when the forward applied voltage is more than the barrier potential of the junction. This voltage is called the forward biased voltage. For a silicon diode, it is 0.7 volts. For a germanium diode, it is 0.3 volts but in our example is 1 volt, as we can see in Figure 2.3. The ideal I-V characteristics of the diode are then:

$$I = I_s(e^{\frac{qV}{K_B T}} - 1) \qquad (2.8)$$

where V is the tension applied (forward or reverse bias); this characteristics is shown in Figure 2.4 in current - voltage characteristics.
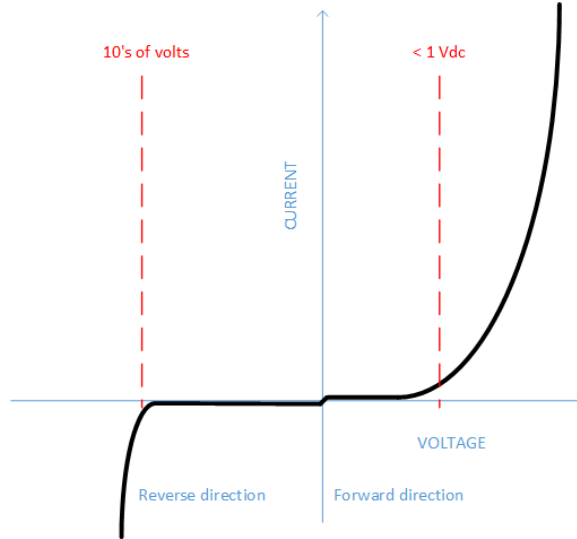


**Figure 2.4:** Current - voltage characteristic curve of a PN junction.

There is a capacitance associated with the depletion layer $C_j = \epsilon_s A/W$ (a dielectric with a conductive terminal in each side). It depends on the doping levels of the n and p regions [37]. The value of $C_j$ is important for the charge conversion efficiency (from current signal to voltage signal) as well as for its influence on the thermal noise of the front-end electronics. However, $C_j$ does not affect the shot noise which is given by $i_n = \sqrt{2qI_g\Delta f}$, where Ig is the electric current generated by particles that traverses the device and $\Delta$f is the bandwidth.

### 2.2.1 Silicon particle detector

A silicon particle detector is a device through which one detects a charged or electrically neutral particle and measures its properties. Although there are many different types of detectors (semiconductor detectors, scintillators, ionization chambers etc...), it should be noted that the principle of operation is always the same: the conversion of the energy released by the particles in the sensitive volume of the

sensor into an electrical signal that is possible to handle by means of electronic circuits.

Complex systems combining different detectors are necessary to identify a particle and to measure its physical properties like energy, momentum, electrical charge and mass.

The sensor electrode forms a PN junction creating a "pin diode" that is reversely biased to deplete as much as possible the sensitive volume (depletion zone) of the sensor. In doing so, the charge signal produced by a traversing particle is maximized. The average number of electron-hole pairs generated by a particle in the active volume can be calculated by dividing the energy loss $E$ by the average energy necessary to produce the charge carriers $E_i$:

$$Q_s = \frac{E}{E_i} \tag{2.9}$$

For example, a MIP (Minimum Ionizing Particles) traversing a silicon detector gives on average about 80 electron-hole pairs per $\mu$m [45].

Because of the reverse bias, in the depletion zone an electric field $\vec{E}$ is established that accelerates the carriers of opposite sign in opposite directions. The drift velocity of carriers depends on the magnitude and the direction of the electric field.

The general method to calculate induced charge on electrodes due to the motion of charge carriers in a detector makes use of Ramo's theorem [46]. He devised a method of computing the signal induced by charge between two conductors with an electric field between them. In 1939 Simon Ramo presented the following simple equation for the contribution of a moving electron in vacuum to the current in the lead of an electrode A: This is also valid in the case of more than 2 electrodes.

$$i_A = e\vec{E_u}.\vec{u} \tag{2.10}$$

Here $i_A$ is the instantaneous current in the lead or wire with positive direction towards the electrode in question, e is the elementary charge, $\vec{u}$ is the velocity of the electron, and $\vec{E}_u$ represents the local electric-field vector at the position of the electron produced by a 1 V "test" or "weighting" potential at the electrode, with all other electrodes grounded.

Ramo's theorem can be applied to predict the amplitude of the charge induced on one of the pixel electrodes and with a reverse bias applied on the substrate. For example, consider the case of creating electron-hole pairs from an ionizing event close to the cathode surface and along an axis that is perpendicular to the center of the pixel. The holes will travel only a short distance to the cathode and will not make any or very little contribution, but the the induced current observed at the pixel electrode is entirely due to the motion of the electrons into the volume of the sensor. Then, the geometry of the electrodes and their pitch segmentation affect the resolution of the particle's position.

### 2.2.2   Silicon tracker detector

The amplitude of the signal read out by the circuitry is proportional to the charge collected by the pixel; this process is illustrated in Figure 2.5. The sensor converts the energy deposited/induced by a particle ionizing charge (or photon) to an electrical signal (see Figure 2.5). The signal charge can be quite small; therefore it must be amplified. Usually, the pre-amplifier is configured as an integrator, which converts the narrow current pulse from the sensor into a step impulse with a long decay time. In HEP detectors the primary function of the pulse shaper is to improve the signal to noise ratio. However, the pulse shape should be compatible with the digitizer or device for interconnection. Analog to digital conversion translates a continuously varying amplitude to discrete steps, which correspond to a unique output bit pattern. Finally, the digital information is ready for subsequent storage and analysis. There are different kinds of detectors, but many of them have some similarities in their basic functions [37].

A semiconductor sensor is suitable for high-rate environments because signal charge can be rapidly collected from it. A sensor chip can be
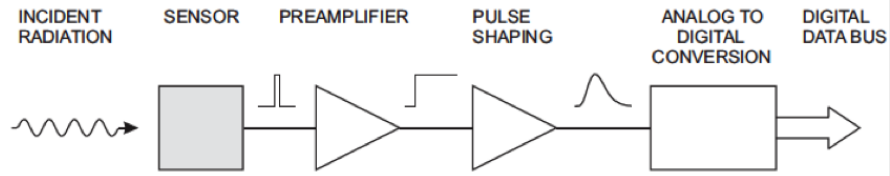
**Figure 2.5:** Basic detector functions.

modelled and simulated with the read-out electronics by a detector capacitance which is added to the input capacitance of the front-end amplifier [45].

A tracking detector is used to determine the trajectories of charged particles that are deflected in a magnetic field and to measure their momenta. In addition, it allows to reconstruct the the primary interaction vertex of interaction and to localize the secondary vertex due to the decays of the particles produced in the interaction. The silicon tracker detector are made of an array of pixels.

Three key requirements of tracking detectors are:

- Speed, in order to allow to study as many events as possible.

- Spatial resolution, to allow precise tracking and momentum measurement.

- Radiation hardness, since in many experiments the sensors are exposed to significant amounts of both ionizing and not ionizing radiation.

Semiconductor detectors are widely used as they satisfy all the above requirements. In particular, silicon tracker detectors provide a superior spatial resolution combined with good energy resolution. In addition, it is possible to design very thin silicon tracker detectors to minimize multiple scattering. Due to their radiation hardness, they can be located close to the interaction point with the main consequences of improving the impact parameter resolution and the separation of multiple tracks.

A Cluster is the number of pixels hit or fired by an ionizing particle crossing the detector. It depends on the pitch of the pixel cell. If the detector pixels are small, the charge of a particle will spread over a number of neighbouring pixels. But even if the pixels are relatively large, there will always be cases to spread to two neighbouring pixels.

Assuming the pixel has a square shape, the single point resolution of a purely binary matrix without any multiple clusters is the pixel pitch divided by the square root of twelve.

This means the smaller the pixel pitch is, the better the intrinsic spatial resolution is. The charge sharing degrades the performance of the sensor to precisely localize the impact point; on the other hand it improves the resolution of the position since the shared fractional charge is determined by a superimposed Gaussian distribution [37]. The integral of the superimposition tends quickly to zero for deviations beyond several standard deviations: the technique to calculate the exact position of the particles is the centroid method.

## 2.3 CMOS technology and circuits

The CMOS (Complementary Metal-Oxide-Semiconductor) is a technological approach allowing the realization of integrated circuits containing two polarities of Metal Oxide Transistors MOS, patterned on the same chip. The sandwich of metal, silicon oxide, and semiconductor, called MOS structure, is the basic building block of the MOS Field Effect Transistors (MOSFETs) [37, 47, 48] which are widely used in microelectronics.

The fabrication of both transistor polarities onto a single chip was a fundamental stimulus in electronics, leading to the VLSI (Very Large Scale Integration) circuit concept. An example of a fundamental block realized in the CMOS technology is the simple inverter based on N and P channel type MOS transistors. Typically one uses a p-type substrate for nMOS transistors, which requires a n-well for the body of the pMOS transistors. The transistor MOS is a four-terminal semiconductor device, patterned in the substrate, where the driving electrodes are the gate G and substrate (Bulk - B), and the output electrodes

are the drain D and the source S. A n-type transistor is sketched in Figure 2.6.
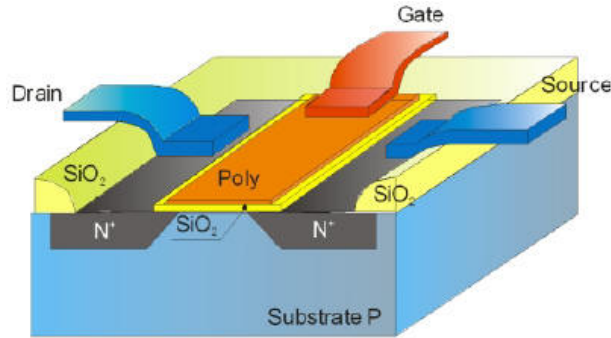


**Figure 2.6:** Simple N-channel type transistor MOS with the substrate (bulk), drain, gate and source electrodes and thin insulating $SiO_2$ barrier [49].

In pixel detectors, which are directly coupled to the read-out electronics, understanding MOS structures is also important to deal with the surface regions between the pixels and with the consequences of radiation-induced surface damage.

### 2.3.1 MOSFET

The Field-Effect Transistor (FET) is a transistor that uses an electric field to control the shape and hence the electrical conductivity of a channel of one type of charge carrier in a semiconductor material on the central terminal. While the conductivity of a bipolar transistor is regulated by the input current (the emitter to base current) and so has a low input impedance, a FET's conductivity is regulated by a voltage applied to a terminal (the gate) which is insulated from the device and therefore always has a high input impedance. The applied gate voltage generates an electric field within the device, which in turn attracts or repels charge carriers to or from the region between a source terminal and a drain terminal. The density of charge carriers in turn influences the conductivity between the source and drain.

FETs can be majority-charge-carrier devices, i.e. the Junction gate Field-Effect Transistor (JFET), in which the current is carried predominantly by majority carriers, or minority-charge-carrier devices,

in which the current is mainly due to a flow of minority carriers. The device consists of an active channel through which charge carriers, electrons or holes, flow from the source to the drain. Source and drain terminal conductors are connected to the semiconductor through ohmic contacts. The conductivity of the channel is a function of the potential applied across the gate and source terminals.
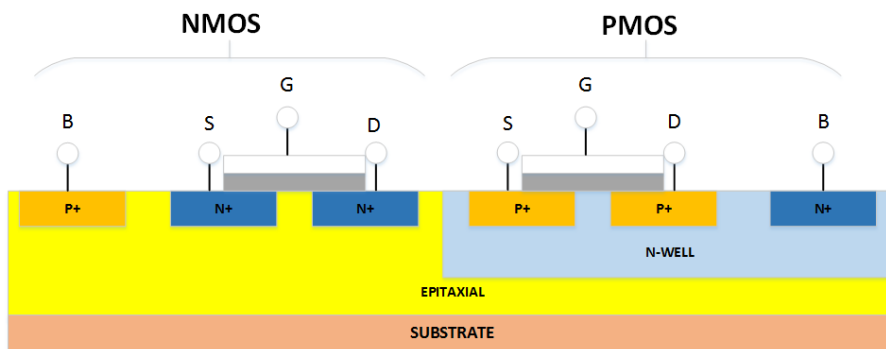


**Figure 2.7:** Typical MOS transistors cross section[50], Usually the MAPS process includes an epitaxial layer.

The most basic element in the design of a large scale integrated circuit is the transistor, which can be built by joining an n-type and p-type material. The type of transistor available is the MOSFET (see Figure 2.7). These transistors are formed as a sandwich consisting of a semiconductor layer, usually a slice, or wafer, from a single crystal of silicon; , together with a layer of silicon dioxide (the oxide) and a layer of metal. These layers are patterned in a manner which permits transistors to be formed in the semiconductor material substrate (see Figure 2.6).

Figure 2.8 shows the $I_D$ - $V_{GS}$ characteristics of an NMOS device in the long-channel process. In order for the drain current to exist there must be carriers present in the area between the gate and and the source, which are referred to as the conducting channel. The figure also illustrates the tolerance due to radiation; this will be discussed later.

The FETs fourth terminal is called a bulk, or substrate. This fourth terminal serves to bias the transistor into operation. In most cases,
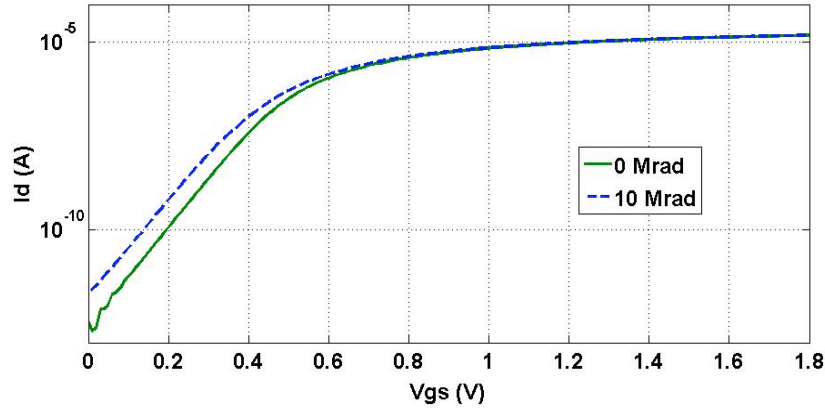
**Figure 2.8:** TowerJazz 180 nm transistor, drain current Id versus gate voltage Vgs for a minimum size NMOS transistor before and after irradiation with 10 Mrad of 10keV X-ray photons.

especially in digital cells, the substrate and the source of an nMOS are connected to the ground potential.

The components of a transistor are the following:

- Substrate: It is the lowest layer made of highly doped (p-type), crystalline silicon with low resistivity. It provides mechanical stability and hosts all other structures. Sometimes substrate contains epitaxial layer.

- Epitaxial layer: The epitaxial layer is grown on top of the substrate. This layer is lightly doped (p-type) and forms the active volume of the detector where charge carriers are generated by the incident particles. The active devices are embedded in this layer.

- Well implantations: They serve as a bulk for the Field Effect Transistors. N-well and p-well implantations are used to integrate pMOS and nMOS transistors respectively.

- Diffusion implantations: They form the source and drain of the transistors. They have higher doping than the wells in which they are embedded. P-type and n-type implantations are used for pMOS and nMOS respectively.

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- Metal lines: They connect the different silicon structures. They are generally made of aluminium or copper and are embedded into silicon oxide, which serves as an insulator.

### 2.3.2 Simple circuits

Complementary MOS circuits use both nMOS and pMOS transistors, and CMOS has been widely used for digital circuits including inverters, NAND, AND and memory cells. It allows for very simple circuit designs such as amplifiers, comparators, etc. Take for instance, the following digital gate: an inverter circuit built using two transistors, one pMOS and one nMOS.
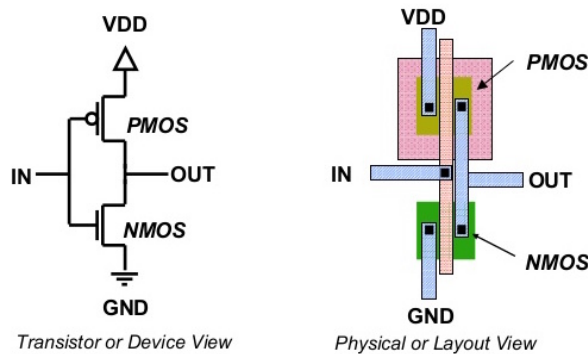


**Figure 2.9:** Physical layout and schematic of an inverter gate. The device and its interconnections are made of polygons that represent different layers of material.

Figure 2.9 shows an inverter gate; the upper transistor is a pMOS. When the channel (substrate) is made more positive than the gate (gate negative in reference to the substrate), the channel is enhanced and current is allowed between source and drain. So, in the above illustration, the top transistor is turned on.

The lower transistor nMOS, having zero voltage between gate and substrate (source), is in its normal mode: off. Thus, the action of these two transistors is such that the output terminal of the gate circuit has a solid connection to Vdd and a very high resistance connection to ground. This makes the output "high" (1) for the "low" (0) state of the input, as is sketched in Figure 2.10.
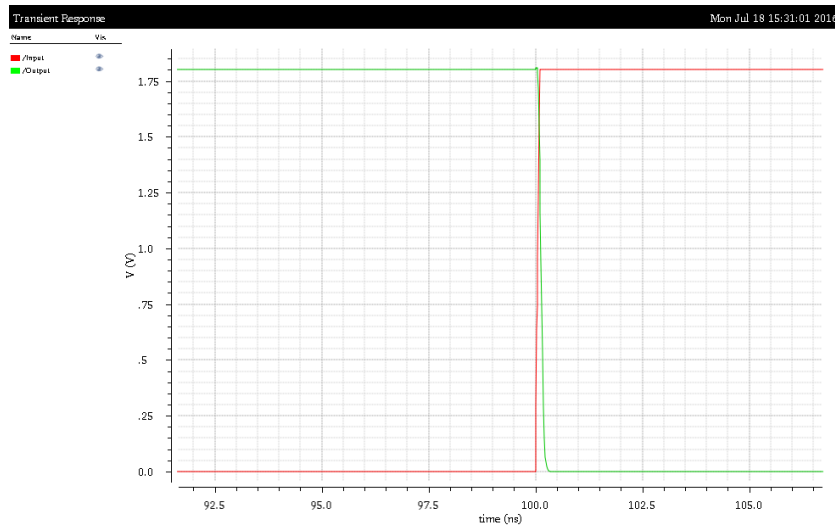
**Figure 2.10:** Transient simulation of the inverter.

Now the nMOS transistor is saturated because it has sufficient voltage of the correct polarity applied between gate and substrate (channel) to turn it on (positive on gate, negative on the channel). The upper transistor, having zero voltage applied between its gate and substrate, is in its normal mode: off. Thus, the output of this gate circuit is now "low" (0). Clearly, this circuit exhibits the behavior of an inverter, or NOT gate, as is sketched in Figure 2.10.

### 2.3.3   The CMOS process

The CMOS process refers to the family of processes used to implement that circuitry on integrated circuits. CMOS circuits use a combination of pMOS and nMOS to implement logic gates and other digital/analog circuits.

The devices are built into a common p-type substrate called a "wafer". This wafer is doped with donor atoms for an n-type substrate or acceptor atoms for a p-type substrate. The nMOS transistors are fabricated directly in the p-type wafer, while pMOS transistors are fabricated in a n-well. The Shallow Trench Isolation (STI) provides electrical isolation between devices, as shown the Figure 2.11 [47]. Metals and
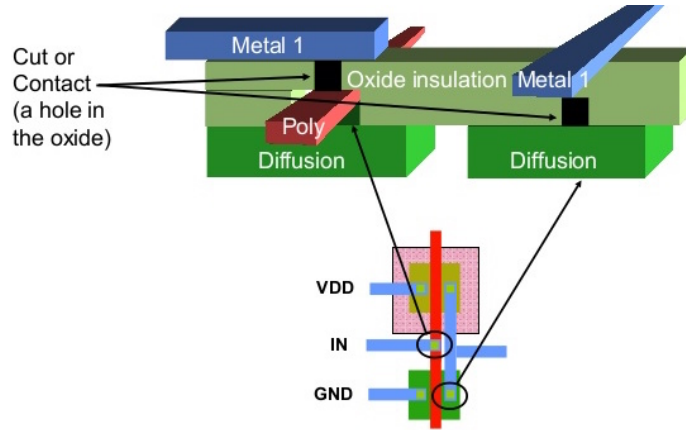
**Figure 2.11:** Example of an inverter interconnected in a CMOS technology [49].

contacts provide access to the device terminal Source, Drain or Gate. The devices are connected together with poly-silicon or metal interconnects; in some cases the interconnect can add unwanted or parasitic capacitance, resistance, diode and inductance effects.
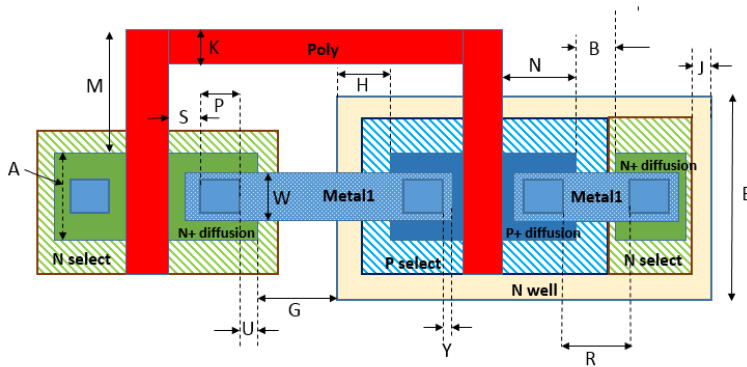


**Figure 2.12:** Layout design rules.

The devices are fabricated on a silicon substrate wafer by layering different materials in specific locations and shapes on top of each other. Each of many process masks defines the shape and location of a specific layer of material (diffusion, poly-silicon, metal, contact, etc.). Mask shapes, derived from the layout view, are transformed to silicon via photo-lithographic and chemical processes. Figure 2.9 (right) shows

the representation of layout polygons. Figure 2.11 shows, how the transistors are interconnected by the poly-silicon via contact and by metal 1. Multiple levels of metal lines are routed to interconnect devices, creating a circuit on a chip.

Design Rules Checking (DRC) are a series of parameters provided by semiconductor manufacturers that enable the designer to verify the correctness of a mask set. Design rules are specific to a particular semiconductor manufacturing process. A design rule set specifies certain geometric and connectivity restrictions to ensure sufficient margins to account for variability in semiconductor manufacturing processes, so as to ensure that the parts can be fabricated correctly.

The most basic design rules are shown in Figure 2.12. The few single-width rule specifies the minimum width of any shape in the design and minimum distance rule between the shapes. A minimum area rule is just drawn between the N+ diffusion and the contact for example. There are many other rule types not addressed here. Antenna rules are complex rules that check ratios of areas of every layer of a net for configurations that can result in problems when intermediate layers are etched. Many other such rules exist and are explained in detail in the documentation provided by the semiconductor manufacturer.

## 2.4   Radiation Effects

Radiation effects in electronics are usually divided into damage by ionizing radiation called Total Ionizing Dose (TID), affecting transistors, especially nMOS, Non Ionizing Energy Loss (NIEL), that affects pixel charge collection, and Single Event Effects (SEE) [51, 52] affecting the registers and state machines in the digital domain. These radiation effects will be described in the next sections.

### 2.4.1  Total Ionizing Dose in transistors

Radiation will induce damage both in the front-end electronics and in the sensors. TID is an accumulating effect which becomes worse the longer a device is exposed to ionizing radiation. The leakage current of the device increases due to charges trapped inside the STI oxide. The critical material is silicon dioxide ($SiO_2$) which is used for the gate oxide, for device isolation, and for separating the routing metals as can be seen in Figure 2.11. In the oxide, charged particles and sufficiently energetic photons produce [electron-hole] pairs. Electrons and holes in $SiO_2$ have very different mobility; hence if an electric field is applied, the two are quickly separated. In absence of electrons, the holes can not recombine and are trapped in the oxide, where they can originate two types of defects. In the oxide itself, the trapped holes generate as positive charges. At the interface between the oxide and the crystalline silicon they can generate the so-called interface states. The build-up of interface states is slower than the direct hole trapping; therefore the device characteristics still evolve after the irradiation has stopped. Interface States are amphoteric, so they can behave as donors or acceptors. This will change the threshold voltage of both normal and parasitic devices and can give rise to leakage currents between drain and source of nMOS transistors and in between neighbouring transistors. A reduction of the TID sensitivity has been observed when moving to smaller technology nodes. This improvement is mostly attributed to the thinner gate oxides. [51, 52, 53].

In the ASICs now in use in the LHC, which are implemented in a 250 nm CMOS process, a very high level of radiation tolerance was achieved through the systematic use of Enclosed Layout Transistors (ELT) and guard-rings. Measurements in 130 nm CMOS technologies [54] suggest that ELT transistors, it must depend on the technology, they may still be needed.

Ionization damage in CMOS transistors causes threshold shifts. Figure 2.13 shows the creation/trapping of charge (by radiation) and its passivation/de-trapping (by thermal excitation). These phenomena are dose rate and temperature dependent [54].
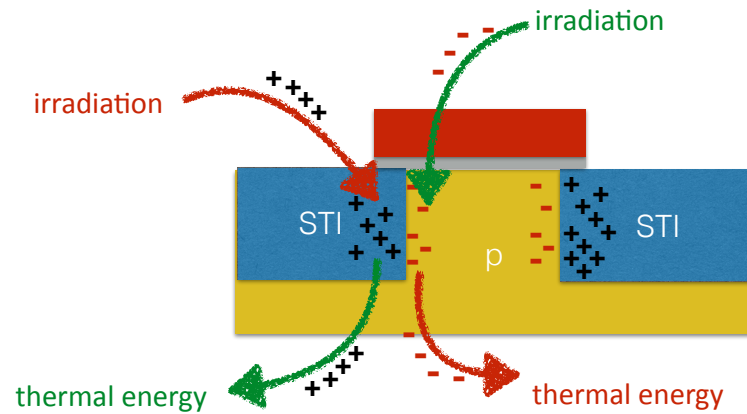
**Figure 2.13:** The leakage current on nMOS under ionizing radiation.

With respect to the current ALICE ITS detector, the innermost pixel layer will move about 17 mm closer to the interaction point. The yearly radiation levels are summarized for the first layer in Table 1.5 is lower than other experiments at CERN.

### 2.4.2   Non Ionizing Energy Loss in sensors

The Non Ionizing Energy Loss (NIEL) is a quantity that describes the rate of energy loss due to atomic displacements as a particle traverses a material. It generates bulk damage in the silicon lattice that in turn can degrade the sensor performance in terms of charge collection efficiency and signal-over-noise ratio and also results in increased leakage current. NIEL damage causes a n-type CMOS transistor to become less n-type until the substrate undergoes type inversion and becomes p-type [55].

Many studies have successfully demonstrated that the degradation of semiconductor devices or optical sensors in a radiation field can be linearly correlated to the displacement damage energy [56], and subsequently to the NIEL deposited in the semiconductor devices or optical sensors. However, NIEL is still a valuable tool, and can be used to scale damages produced by different particles and in different environments, even though this is not understood at the microscopic level.

In general the radiation induced damage to the silicon lattice will lead to a macroscopic degradation of the sensor characteristics. This manifests itself as an increase in leakage current, a change in depletion voltage in case of a depleted operation and in trapping of the signal charge [53]. The leakage current will increase proportionally to the 1 MeV neutron equivalent fluence.

### 2.4.3 Single Event Effects

Ionizing radiation in digital structures can induce Single Event Effects (SEE) is the result of an instantaneous impact of radiation affecting the state of the electronics, and can occur either as a Single Event Transient (SET) or a single-event upset (SEU). The former causes a transient change of voltage in one of the capacitive nodes of a logic gate or a memory cell. The likelihood of an SET decreases with increasing node capacitance. If this change is captured by a memory device, it becomes a persistent effect. In general, this is a threshold phenomenon that depends on the Linear Energy Transfer (LET) of the impinging particle, because the deposited charge must be sufficient to change the status of a circuit node. If a bit-flip happens in a state register of a Finite State Machine (FSM) or in a configuration register, a full system reset or reconfiguration may be needed to restore the system into a properly functioning state [57]. In the next section we describe one technique to mitigate SEU which is widely used in HEP. The Ionization can also cause single event latchup (SEL), a type of short circuit that triggers parasitic structures which can disrupt proper functioning of the element, or possibly can even lead to its destruction.
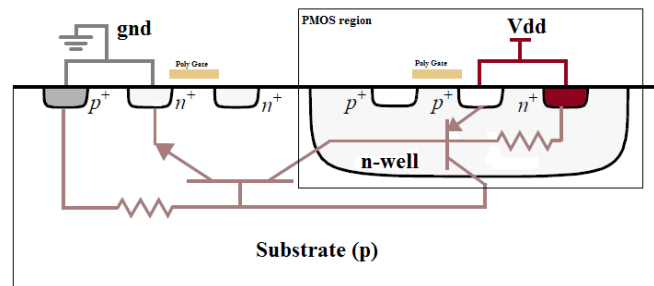


**Figure 2.14:** Parasitic thyristor in a CMOS technology cross section [58].

The ionization charge can cause SEL such that parasitic thyristor (see Figure 2.14) which normally is in the off state is turned on by the ionization and draws a large current. This current can be detrimental to the circuit, and even if it is not, the power to the circuit needs to be taken away to deactivate the thyristor. During a SEL, the device current exceeds the maximum specified for the device. Unless power is removed, the device will eventually be destroyed by thermal effect.

One possible solution to avoid SEL is to place the bulk contact of the nMOS and pMOS transistor close to the source/drain and increasing this bulk contact to generate a good contact. In general, increasing resistance in the contacts reduces the probability of SEL.

### 2.4.3.1 Single Event Upset mitigation implementing Triple Mode Redundancy

Design techniques such as triple modular redundancy (TMR) [59] and Error Correction Coding (ECC) can be used to make circuits very tolerant to SEUs. TMR is based on triplicated logic in which the correct result is a vote of the three outputs. If only one device has been upset, the output of the voting is still correct. ECC such as Hamming coding [59] can also be used to correct single-event upsets or even detect multiple bit upsets. These techniques, however, introduce area, power and timing penalties.
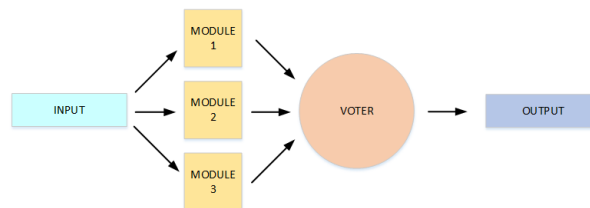


**Figure 2.15:** TMR interconection diagram.

One simple SEU mitigation technique but expensive at a gate-level area is to triplicate all logic that is crucial to the correct functionality of the system. The outputs of all three identical design modules are then connected to a majority voting gate. The majority voting gate simply takes three inputs and outputs 0 if at least two inputs are 0,

and outputs 1 if at least two inputs are 1. This system will function correctly even if one of the three modules fails, but a second failing module may cause the whole system to fail (see Figure 2.15).

Several design techniques for applying TMR to digital design are described in [59, 60, 61]. If an output of a majority voter is fed back to redundant logic modules and their values refreshed every clock cycle when no new data are available, the logic will be immune to SEU as long as only a single module is upset during the same clock cycle. The error will then remain in the system for one clock cycle but will be corrected during the next clock cycle. This is the technique that has been used in all FSMs and other important digital logic such as FIFO pointers implemented in the read-out circuits, as is sketched in Figure 2.16.
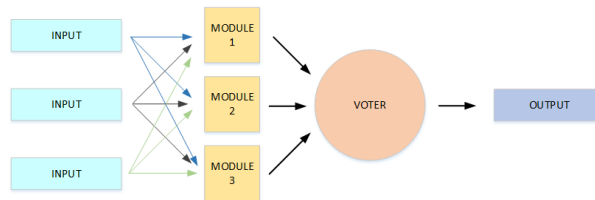


**Figure 2.16:** TMR full interconection driagram.

## 2.5  Technology Options for Pixel Detectors

A number of technologies, each representing a different level of maturity, could potentially fulfil the requirements of the inner ITS layers. The options can be divided into two groups: monolithic and Hybrid silicon Pixel Detectors (HPD) [62]. A layout cross section view of both concepts is shown in Figure 2.17. The pixel detectors will be described in the following sections
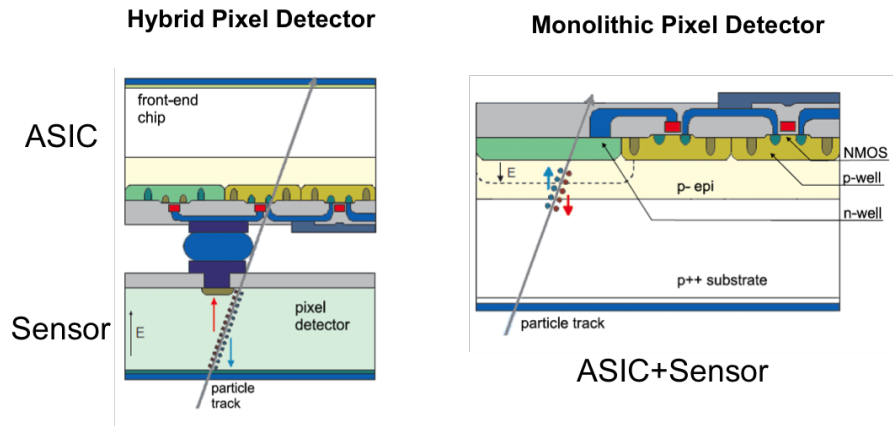
**Figure 2.17:** Charge collection in hybrid pixels and MAPS [62].

### 2.5.1 Hybrid pixels detectors

In Hybrid pixel detectors the sensor and the front-end electronics are implemented in two separate silicon chips see Figure 2.17. On the left of the figure, the sensor chip does not contain any active electronics and is used to produce a signal when a particle passes through it and generates a change signal. The read-out chip is usually an ASIC that contains the electronics used to digitize the analog signals and provides a single bit hit information from the sensor chip, but sometime also analog signal charge information is provided. The sensor chip is manufactured independently from the read-out ASIC, and both are bonded together using different techniques like bump bonding or wire bonding.

HPDs are expensive, and often their cost is dominated by the bonding step. In order to overcome these limitations to build the new generation of radiation hard silicon detectors with higher granularity and less material budget, we require the development of new technology. One way to overcome this is to merge both sensor and read-out electronics into a single detection device.

Hybrid pixel detectors have been the choice for the current LHC experiments because they provide clean, time-stamped, unambiguous 3-dimensional hit information and they are radiation tolerant. In the

hybrid approach the front-end chip and the sensor are produced on two different wafers and then connected using bump bonds. Present bump bonding techniques are limited to pitches of 30-50 $\mu$m. However, the recently introduced Cu-pillar technology may reduce substantially this limit in the near future. Currently, bump bonding represents one of the main cost factors for the production of hybrid pixel detectors and prevents their application to larger surfaces.

### 2.5.2 Monolithic active pixel sensors

The Monolithic active pixel sensors are fabricated in a standard CMOS process but with some modification on the process. MAPS are peculiar because they embed into the same CMOS ASIC both the sensor and the front-end electronics as was commented earlier. Moreover, due to this configuration, MAPS are typically thinner than hybrid pixel sensors so that they are highly suitable for applications where the material budget must be kept low, and they also present a cost advantage.

### 2.5.2.1 MAPS process

Initially, all prototypes of MAPS are fabricated using a standard CMOS process version providing an epitaxial type of substrate as shown in Figure 2.7. The substrate layer is a very low resistivity substrate, typically in the range of a few tens of m$\Omega$cm$^{-1}$, over which a p-doped epitaxial layer is grown. This layer, whose thickness is typically up to 20 $\mu$m with a resistivity of the order of 10 $\Omega$cm$^{-1}$, represents the sensing volume. The electronics are built in the last micron or so of this layer, with nMOS (pMOS) transistors occupying heavily doped p-wells (n-wells) as shown in Figure 2.17 (right). As a detecting element, the most commonly used structure is the one formed by an N-doped well created in the epitaxial layer, for example the n-well diode.

### 2.5.2.2 MAPS Principle Operation

In the MAPS implementation, this epitaxial layer is used as a detector radiation sensitive volume, with a diode n-well/p-epi working as a charge collecting element. The detector is only partially depleted in the vicinity of the n-well/p-epi junction, so the charge is collected mainly through a thermal diffusion mechanism. However, due to the particular doping profile (p++substrate/p-epi/p+well), there is a potential minimum in the middle of the epitaxial layer, limiting the volume spread of diffusing electrons created by the absorption of radiation.

The electrons generated are deflected by the substrate due to a potential barrier formed between the lightly doped p-type epitaxial layer and the heavily doped p-type substrate. The substrate - epi creates a potential barrier preventing the signal charge from diffusing into the substrate.

Similarly, a potential barrier exists between the lightly doped epitaxial layer and the heavily doped p-wells of the nMOS transistors. This results in the containment of the majority of the electrons within the epitaxial layer, which diffuse randomly in the epitaxial layer and are guided towards the n-well of the collection diode.

These electrons may move only along the plane parallel to the surface and are rapidly collected when passing close to the collecting pn diode junction, with a typical collection time of the order of 100 ns. The detector active volume is limited in depth to the epitaxial layer only, because of the small lifetime of charge carriers inside a p++ substrate. Therefore, the total amount of available charge created by an impinging minimum ionizing particle amounts to a few hundreds electrons only, for a typical epitaxial thickness of the order of 10 $\mu$m.

As far as the charge collection mechanism in MAPS is concerned, the presence of the n-well of the pMOS transistor in a standard CMOS process poses a significant problem in Figure 2.18, (left). This n-well which is at a positive potential, could also collect the diffusing electrons and thus compete with the collection diode. This would
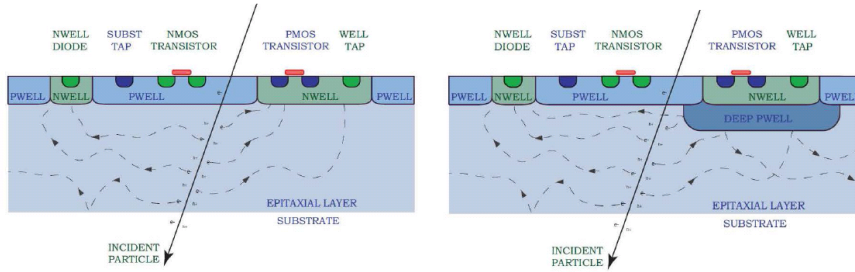
**Figure 2.18:** MAPS cross section [31].

result in the reduction of signal charge collected and hence contribute to a reduction of the charge collection efficiency.
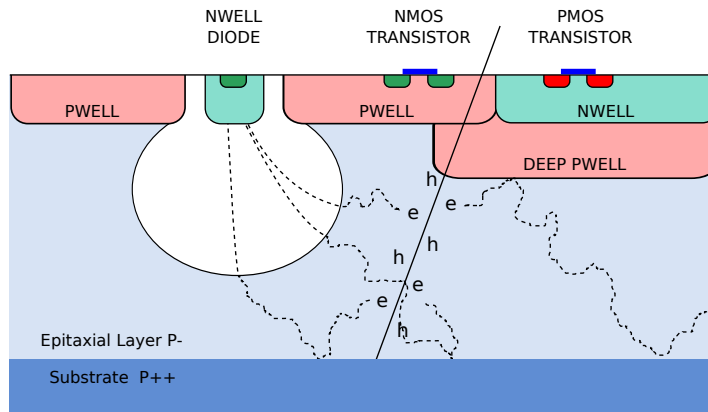


**Figure 2.19:** TowerJazz 180 nm MAPS cross section [31].

One way of solving competition between the charge collection between n-wells is to use a deep p-well under the n-well where the pMOS transistors are placed, (is shown in Figure 2.18 right), using the handle wafer as the detection medium and adding vias through the buried oxide to connect the handle wafer to the CMOS electronics. Figure 2.19 shows that charged particles can traverse the metal layers and any other material, generating a thin trail of electron-hole pairs in the silicon. Provided that there is only one pn junction in the pixel, the entire amount of radiation-generated electrons will be collected, thus making the sensor able to detect particles regardless of where they hit the sensor [59].

### 2.5.2.3 Detector Technology selection

Hybrid pixel detectors fabricated in CMOS 130 nm technology have become a standard for the design of front-end electronics. Complex ASICs like more recently, complex ASICs such as the FEI4 [63] for the ATLAS pixel upgrade and MediPix [64] have been implemented in 65 nm CMOS technology. This process is used by the RD53 collaboration, which develops read-out integrated circuits for the phase 2 pixel detector upgrades of ATLAS and CMS, as well as long term developments. The 130 and 65 nm CMOS processes offer several advantages with respect to the 250 nm CMOS technology widely used in the LHC experiments which are currently taking data. Firstly, the technology is inherently more radiation hard. Secondly, the smaller capacitance of the digital gates and the lower power supply voltage reduce the digital power consumption. Thirdly, the technology is equipped with several options (triple well, transistors, deep moats, etc...) which allow for an effective reduction of the interference of the digital blocks to the analogue ones. However, the 130 nm CMOS process presently used in the hybrid pixel developments does not offer a sufficiently thick epitaxial layer as required by the design of monolithic pixel detectors.

The ITS upgrade has chosen a 180 nm CMOS imaging sensor technology, called TowerJazz. This technology has been selected for the implementation of the ITS upgrade for all layers of the new ITS. The following are the main features that make this technology suitable, and in some respects unique, for the implementation of the ITS upgrade :

- Due to the transistor feature size of 0.18 $\mu$m and a gate oxide thickness below 4 nm, it is expected that the CMOS process is substantially more robust to the TID than other technologies employed up to now as the baseline for the production of CMOS sensors in particle physics applications.

  The nMOS and pMOS transistor structures have been irradiated with X-rays up to a dose of 10 Mrad. The most affected structures are those with a minimum feature size for TowerJazz 180 nm transistors that show a shift in threshold voltage of a few 10 mV at most and an almost complete recovery after 24 h of annealing. The impact of TID on sensor prototypes has been measured

in various test beam campaigns at CERN and at DESY, showing only a very marginal degradation of the charge collection properties after TID irradiation of 3 Mrad. The gate oxide thickness of this technology is 3 nm, making it robust to TID, as demonstrated in the experimental results in [53].

- The feature size and the number of metal layers available (up to six) are adequate to implement high density and low power digital circuits. This is essential, since a large part of the digital circuitry (e.g. memories) will be located at the periphery of the pixel matrix and its area must be minimised in order to reduce the insensitive area as much as possible.

- In addition, applying a moderate negative voltage to the substrate can be used to increase the depletion zone around the collection diode and in this way improve both the charge collection and the signal-to-noise ratio by decreasing the pixel capacitance [65].

  MAPS can significantly improve the spatial resolution, the signal over noise ratio (S/N) and reduce the material budget and cost simultaneously, but often the radiation tolerance of MAPS is not so good. However, the main challenge with MAPS is its low tolerance to non-ionizing radiation in excess of $10^{15}$ $n_{eq}$cm$^{-2}$, because the signal charge is collected by drift. In MAPS charge is often collected by diffusion, causing the signal charge to be trapped more easily, resulting in a moderate radiation tolerance because of displacement damage. However, the radiation requirements for ALICE are moderate compared to other LHC experiments, so MAPS are a viable solution.

- It is possible to produce the chips on wafers with an epitaxial layer of up to 40 $\mu$m thickness and with a resistivity between 1 k$\Omega$cm$^{-1}$ and 6 k$\Omega$cm$^{-1}$. With such a resistivity, a sizeable part of the epitaxial layer can be depleted. This increases the signal-to-noise ratio and may improve the resistance to non-ionizing irradiation effects.

- The access to a stitching technology allows the production of sensors with dimensions exceeding those of a reticle, and enables the manufacturing of die sizes up to a single die per 200 mm wafer diameter. As a result, insensitive gaps between neighbouring chips disappear and the alignment of sensors on a poly-carbonate support. This option has not yet been exploited by the prototypes, but is foreseen as an option for future large-scale chips.

- Higher granularity and lower material thickness, key features of the MAPS process, combined with the resulting small pixel size around $28 \times 28 \ \mu\text{m}^2$, allow one to significantly improve pointing resolution and tracking efficiency. The design goal of the ITS upgrade is to have pixels with the same granularity for all layers, corresponding to an intrinsic resolution of 5 $\mu$m.

- A quadruple well is available, which offers a deep p-well in order to shield the n-well of pMOS transistors from competition with the collection diode, as shown in Figure 2.19. This makes the use of full CMOS circuitry in the pixel area possible without the drawback of parasitic charge collection by the n-wells layer on a p-substrate. The deep p-well option allows the production of pixel structures with significantly enhanced functionality, thus making more complex in-pixel signal processing possible.

## 2.6   Read-out architectures

The traditional read-out in hybrid pixel detectors is the data-driven mechanism that uses a token-ring structure, in which a look-ahead technique is used to decrease the signal ripple down to the chip periphery [60, 66, 67]. This read-out is used by the ATLAS experiment. The traditional read-out in monolithic pixel detectors is the rolling-shutter [68] with a zero suppression logic in the chip periphery which will be explained in the next section. Another zero suppression technique is called OrthoPix [69]. It uses a multiple projection scheme combined with an encoding architecture for the read-out. New read-out architectures that satisfy the ITS upgrade requirements in power and integration time will be explored, studied, designed and character-

ized in terms of small prototypes, thus forming the research objectives of this thesis.

### 2.6.1 State of the art for MAPS : Rolling shutter

MIMOSA sensors have been developed at IPHC since the late nineties and within a partnership with IRFU since early 2000. The development of a new sensor with a rolling-shutter architecture is advancing, using as a reference the MIMOSA26 sensor [70] developed at IPHC and the ULTIMATE sensor [71] developed for STAR. The rolling-shutter architecture allows the continuous and periodic reading, row-by-row, of the charge collected inside the pixels. This architecture results in a low power consumption, since only one row is being read out and powered at a time. In the present MIMOSA sensors, the power consumption corresponds to 150-250 mWcm$^{-2}$ depending on the number of columns per surface unit and on their length. In order to guarantee a small pixel size, the logic inside each pixel is kept to a minimum. A pixel cell contains the sensing element, a pre-amplifier, a clamping node and the row selector.

The first element after the collecting diode is the pre-amplifier. Its feed-back loop also provides the bias voltage of the pixel, with the advantage of a continuous leakage current compensation. A row selector activates one row at a time, and connects the pixels to the discriminators placed at the end of the column.

A sparsification algorithm is implemented in the digitized data, which identifies and encodes a pattern of hits on one row of pixels, retaining only the information of the column address of the first pixel hit and the number of contiguous hits. By processing the matrix row-by-row, the sparsification and zero suppression algorithm will generate output states at a Poisson-distributed rate, going from zero states to a maximum number that depends on the chip occupancy. To equalize the output data rate and limit the data bandwidth, a buffer will be implemented in the form of memory blocks. For the existing MIMOSA26 sensors [70], two memories are implemented and they are alternatively selected: when one memory is being written, the other is read, and vice-versa.

The MIMOSA [72, 73] family has a trigger-less architecture, meaning that once the read-out of the pixel matrix is started, the frames are sent out continuously at a fixed frequency, independent of the LHC collisions. Studies are ongoing on a micro-circuit that will be implemented inside the MISTRAL sensor to select only those frames that correspond to a collision that has activated the ALICE L0 trigger. This will reduce the chips power consumption on the read-out and the output bandwidth, as not all the frames will be sent out. The MISTRAL sensor will be briefly introduced in subsubsection 2.6.2.1.

### 2.6.1.1 The ULTIMATE ASIC

The ULTIMATE sensor developed by the IPHC PICSEL group in AMS 0.35 $\mu$m technology (see Figure 2.20). It can meet the majority of the requirements of the ALICE ITS upgrade. There are limitations, such as its limited radiation tolerance and moderate read-out time. It is, however, a very promising technology for heavy-ion experiments such as ALICE. It is also in such experiments, where measurements at low transverse momentum are crucial, that the advantages of MAPS technology are readily seen. The first large scale application of MAPS technology in a collider experiment is the STAR PXL detector [71], currently installed and operating as an upgrade to the STAR detector.

ULTIMATE is the sensor chip for the STAR PXL detector. Its architecture integrates the main functions of MIMOSA26 [74, 75]. It is a MAPS with fast binary read-out that includes zero suppression
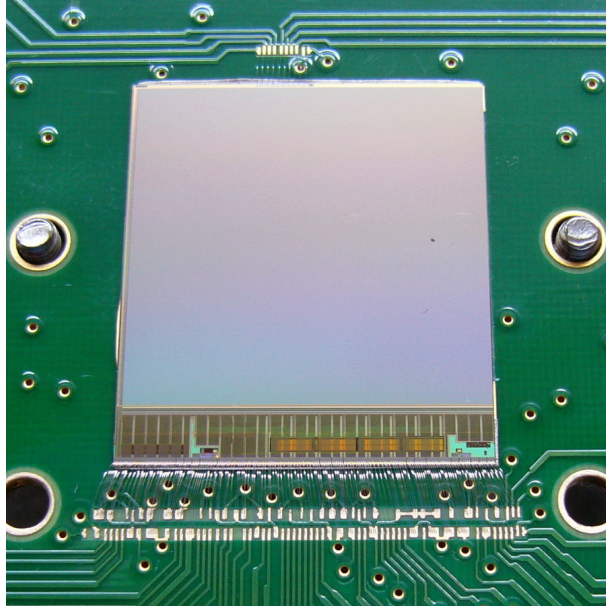
**Figure 2.20:** ULTIMATE sensor designed on AMS 0.35 $\mu$m technology [74] .

Unfortunately, the technology used for the ULTIMATE did not meet the specifications for the ALICE ITS upgrade, particularly in terms of integration time [31], and no deep p-well is available in this AMS CMOS imaging sensor process.

### 2.6.2 Improved rolling shutter

Having a deep p-well [76] available in TowerJazz allowed improved rolling-shutter architectures such as Mistral and Astral based on MI-MOSA that will be briefly introduced in the next sections.

### 2.6.2.1 MISTRAL

MISTRAL will be built on the experience of the ULTIMATE (MI-MOSA-32) chip [72, 77, 78]. A single MISTRAL chip has a surface 1.5 cm $\times$ 3.0 cm containing 375 rows and 1300 columns. The sensor is built from three independent Building Blocks. The target pixel size is about 36 $\mu$m $\times$ 65 $\mu$m, providing a single point resolution of

about 10 $\mu$m [79, 80]. These values result from the necessary balance between the required spatial resolution, which favours small pixels, and read-out speed, which tends to minimize the number of rows. Moreover, the columns need to be wide enough to allow implementing two discriminators at each column end, a configuration imposed by the simultaneous read-out of two rows.

MISTRAL will be equipped with column level discriminators allowing simultaneous two-row read-out in rolling-shutter mode to achieve the full matrix read-out in about $30\mu$s. This architecture is intrinsically nearly dead time free, since all the pixels remain sensitive during the read-out period and all the hits are registered. In case the integration time is larger than the mean time between collisions, event pile-up can occur. The rolling-shutter architecture leads to high power consumption, since only two rows are read out and powered at a time. The power consumption of the MISTRAL architecture is expected to be about 100 mWcm$^{-2}$. The first prototypes built in the TowerJazz [72, 77] technology were MIMOSA- 32 and MIMOSA-32ter, fabricated and tested in 2012; their characterization is presented in the ITS CDR [33].

The discriminator outputs will be processed through an integrated zero suppression logic: SUZE-02, that will provide the downstream part of both MISTRAL and ASTRAL. The data are stored in a memory of four SRAM blocks ($32 \times 512$ bits), capable of holding about 600 clusters per frame on average and allowing either continuous or triggered read-out. The data are serialized onto a high speed serial link, with a maximum SUZE-02 output rate of 640 Mbits. The MISTRAL is a variant of ASTRAL having end-of-column discriminators, resulting in a simpler in-pixel circuitry but a higher power density.

Unfortunately, the MISTRAL does not satisfy the needs of ALICE ITS in terms of both integration time and electronics dead time. However, this solution must be re-designed to be compatible with the ITS polycarbonate support and cable connection.

### 2.6.2.2 ASTRAL

The second chip under development at IPHC, called ASTRAL (accelerated read-out MIMOSA sensor for the inner tracker of ALICE) is an alternative design to the MISTRAL [77] development, based on a concept intrinsically faster and less power consuming.

Two variants of the sensor are considered, one (ASTRAL-IN) optimized for the ITS Inner Layers upgrade which privileges spatial resolution and one (ASTRAL-OUT) best suited to the Outer Layers, where the relaxed requirement on the spatial resolution is used to further suppress power consumption.

The design of ASTRAL-IN is based on 22 $\mu$m $\times$ 33 $\mu$m pixels providing a single point resolution of about 5 $\mu$m [79, 80] and comprising a sensitive area of 1248 columns and 416 rows. The expected frame read-out time is approximately 30 $\mu$s (assuming simultaneous double-row read-out) with a power density of 300 mWcm$^{-2}$. A still lower power density of 100 mWcm$^{-2}$ is obtained with ASTRAL-OUT by enlarging the pixels to 36 $\mu$m $\times$ 31 $\mu$m, which reduces the number of columns to 832 and the number of sparse data units from three to two.

Unfortunately, the outlook of the ALICE ITS upgrade is to have one pixel detector, as was proposed by the ASTRAL team. The ASTRAL Outer Barrel (OB) solution would be selected as a backup solution to be implemented in the ALICE ITS upgrade. Moreover, this solution must be re-implemented to be compatible with the ITS stave pads connection.

### 2.6.3 New architecture ALPIDE

The ALPIDE architecture is based on an approach with more complexity inside the pixel or the matrix. Each ALPIDE pixel contains its own ampliffer and shaper, followed by a comparator and multiple hit buffers. The zero-suppression is performed within the matrix. In order to do this, the Priority-Address-Encoder and Priority-Reset-Decoder (PADRE) circuit is employed. Furthermore, it was implemented without distributing a read-out clock to the pixel matrix. Is a

matrix sparsified read-out architecture follows an approach where its column matrix is subdivided into a set of hierarchies of 4 inputs. In each hierarchy each pixel cell is connected to a priority address encoder which registers the addresses of the hits in every read-out clock cycle.

This circuit takes care of propagating the addresses of hit pixels to the End-Of-Column (EoC) logic and resetting the corresponding in-pixel hit buffers. As a consequence of this approach, the EoC logic is reduced to buffering and interface. This architecture allows to read all pixels in a global-shutter mode. This shutter can either be controlled by an external trigger signal combined with short shutter windows, or operated in continuous acquisition mode, only being closed in between frames to move to the next hit-buffer.

## 2.7   Conclusions and overview

This chapter gives an overview of the principle of operation of Monolithic Active Pixel Sensors (MAPS) and the motivation behind the technology adopted for ALICE ITS upgrade.

We have reviewed the TID and NIEL radiation effects. The Radiation induced effects have a major impact on the electrical behaviour of semiconductor devices and deeply affect their properties. There is no general model able to support a comprehensive interpretation of irradiated characteristics; the generation of complex defects is certainly among the fundamental mechanisms for the degradation of the silicon properties. On one hand the increase of the leakage current on TID must be studied and analyzed for TowerJazz and design prototypes to analyze and study the related concept of displacement damage dose, charge collection and noise. TMR techniques must be implemented in the prototypes to avoid and prevent SEE.

The differences between Hybrid Pixel Detectors (HPD) and Monolithic Active Pixel Sensors (MAPS) have been explained. HPD is the simplest pixel design where the front-end is separated from the read-out logic. MAPS is more complex due to the fact that the collection electrode and the read-out are in the same nWELL and the pixel will

have to be a small nWELL diode (2-3 $\mu$m diameter). The charges are collected by diffusion when is applied a moderate reverse bias voltage to substrate, and it can be used to increase depletion zone around the nWELL of the collection diode.

TowerJazz quadruple-well process offers a deep pWELL layer, this layer shields the nWELL of pMOS transistors over and allows the full CMOS circuitry (nMOS and pMOS transistors) within the matrix active area. The thickness of p-type epitaxial layer is of the order of 20 $\mu$m to 40 $\mu$m thick on p-type substrate and epitaxial layer resistivity higher of 1 k$\Omega$. It will have a big impact on the impact parameter and the charge collection. The technology allows for 6 metal lines. The technology provides access to a stitching technology allowing the production of sensors with dimensions exceeding those of a reticle and enables the manufacturing of die sizes up to a single die per 200 mm diameter wafer. As a result, insensitive gaps between neighbouring chips could be removed.

The ULTIMATE sensor [71] developed for the STAR Heavy Flavor Tracker (HFT) at RHIC was the first application of MAPS in a heavy-ion experiment. However, this sensor developed with AMS 0.35 $\mu$m technology does not satisfy the requirements of ALICE ITS upgrade, especially in terms of radiation hardness and read-out time. These limitations could be overcome by the 180 nm technology provided by TowerJazz.

The new read-out architecture for ALPIDE, based on a priority encoder is one method to allow the implementation of a data-driven read-out. The advantage of this technique is that it does not require hard-wire encoding of the address of each pixel and avoids the clock propagation in the matrix in the acquisition mode.

# Chapter 3

# Monolithic Active Pixel Sensor development for the ALICE ITS Upgrade

In the previous chapter the principles of semiconductor detectors and MAPS, and the read-out scheme for the ALICE ITS upgrade were briefly introduced. In this chapter different concepts of read-out architectures for MAPS are described. The author made his contribution on the design of pixel read-out of the small prototypes including its physical implementation and the validation of the TowerJazz 180 nm CMOS technology. The author designed the digital part of the read-out of all chips described in this chapter. These chips allowed the validation of the TowerJazz 180 nm quadruple well technology for the ALICE ITS upgrade.

In order to characterize the radiation hardness, different prototypes were submitted in a Multi Project Wafer (MPW). The implementation of all designs are based on top-down flow implemented for TowerJazz 180 nm CMOS technology. The top-down flow includes place and route, and sign off via simulation, functional verification and timing analysis. Some of these prototypes are :

- The Explorer0, It was designed to study and optimize charge generation, charge collection and diode layout as well as to study the

effect of back-biasing of the substrate and evaluate the susceptibility to radiation damage.

- The Explorer1: It was designed to analyze and study the charge collection and cluster size before and after irradiation. It was fabricated on seven different substrates with different resistivities and epitaxial layer heights [31].

  - Characterization: The NIEL irradiation of the Explorer1 was done at the TRIGA MarkII Reactor at JSI in Ljubljana using neutrons with a fluence of $0.25{\times}10^{13}$ 1 MeV $n_{eq}$cm$^{-2}$, $1{\times}10^{13}$ 1 MeV $n_{eq}$cm$^{-2}$ and $3{\times}10^{13}$ 1 MeV $n_{eq}$cm$^{-2}$ with the EUDAQ telecope [81, 82]. The SEU cross sections were measured by exposing the digital test structures to proton beams at NPI in Prague with energies of the order of (32.2 MeV and 24.8 MeV) and at PSI in Switzerland with energies of the order of (29.5 MeV, 60 MeV, 100 MeV, 150 MeV and 230 MeV) at fluences between $1.1{\times}10^{7}$cm$^{-2}$s$^{-1}$ and $1.1{\times}10^{8}$ cm$^{-2}$ s$^{-1}$.

- The pALPIDEss sensor is a prototype designed to investigate and explore a new low power front-end and pixel read-out named PADRE. The front-end and its read-out circuit were designed to study the radiation hardness of the TowerJazz 180 nm process and to analyze the charge collection efficiency and the noise performance before and after irradiation [83]; the results of this characterization are available in chapter 5. This chip was characterized before and after irradiation to verify the read-out principle and performance in terms of detection efficiency and noise performance; the results are summarized in subsection 3.2.4.

  - Characterization: The test-beam measurements of the pALPIDEss chip were carried out at the DESY test beam facility in Hamburg. At DESY a 3.2 GeV e$^+$ beam and 6 GeV $\pi^-$ beam were used. For these momenta, the particles are slightly more ionizing than MIPs and the multiple scattering is small enough to allow a position-resolution measurement.

- The ORTHOPIX prototype implements a special read-out architecture based on 4 projections [69] and this chip was also characterized with various back biases.

- The Investigator was motivated by the observation of the pixel performance. This performance is influenced by several parameters such as pixel collection, electrode size, distance to the surroundings, pixel pitch, different ways of reset (Diode or pMOS), deep pWELL size and transistor location space (inside or outside the pixel collection electrode). It contains a set of mini matrices, of which the pixel outputs are brought out in parallel if a particular mini matrix is selected. These outputs are fast compared to other MAPS ($\approx$ 10 ns of rise time), and allow to study charge collection and signal formation in detail for different pixel geometries, pixel pitch, collection electrode geometry etc. A special follower circuit was also implemented to measure pixel capacitance [84].

- The SEU_TJ180 prototype is a test chip design to evaluate the SEE sensitivity during and after irradiation of different types of memory cells of TowerJazz 180 nm technology as FFs and RAM memories to be implemented in the final prototype [53].

The Explorer family, the SEU_TJ180 chip, pALPIDEss chip and the Investigator chip have been studied and characterized by the ITS upgrade characterization team.

## 3.1 The Explorer Family

The Explorer0 chip was the first MAPS prototype designed at CERN. It was designed in the TowerJazz 180 nm CMOS Imaging Sensor (CIS) process and was submitted to foundry submitted in July 2012. [85, 86, 83, 87, 88]. The Explorer1 chip, the second chip of the Explorer family, and was submitted to the foundry in April 2013. The digital read-out and the logic control were implemented in the digital flow as described earlier. The read-out is based on a shift register with control logic using standard cells of TowerJazz 180 nm. The chip is segmented in nine different electrode geometries, which exist in two pitches (20 $\mu$m $\times$ 20 $\mu$m and 30 $\mu$m $\times$ 30 $\mu$m) each. Figure 3.1 shows the different pixel geometries on the Explorer0 sensor and Explorer1 sensor.

| Explorer-0 | | | | Explorer-1 | | | |
|---|---|---|---|---|---|---|---|
| Sector | Shape | Diameter [μm] | Spacing [μm] | Sector | Shape | Diameter [μm] | Spacing [μm] |
| 1 | | 2 | 0 | 1 | | 1.13 | 3.035 |
| 2 | | 3 | 0 | 2 | | 2 | 2.6 |
| 3 | | 4 | 0 | 3 | | 3 | 2.1 |
| 4 | | 3 | 0 | 4 | | 1.13 | 3.035 |
| 5 | | 3 | 0.6 | 5 | | 2 | 2.6 |
| 6 | | 3 | 1.04 | 6 | | 3 | 2.1 |
| 7 | | 2 | 1.54 | 7 | | 1.13 | 0.635 (top) |
| 8 | | 3 | 0 | 8 | | 1.13 | 0.635 (top) |
| 9 | | 3 | 1.04 | 9 | | 2 | 2.6 |

**Figure 3.1:** Comparison of the collection diode geometries of the nine sectors of the Explorer0 sensor and Explorer1 sensor. The geometries are equivalent for the two pixel pitches [88].

In order to increase the flexibility in the characterisation of the pixel's sensing diode, each pixel was designed with two independent analog memories (see Figure 3.2). These memories store the voltage level at the output of the sensing diode. At the periphery a sequencing circuit is used to read-out the memories of all pixels in a serial manner. The pixel circuit operates from the functional point of view: the voltage signal at the output of the sensing diode is first set to a nominal value by turning on the pMOS sensor connecting the collection electrode to Vreset, resetting the collection electrode to a well-defined voltage level. Immediately after the reset operation the signal at the output of the sensing diode is stored in the first memory cell. After some time (integration time) the signal at the output of the sensing diode
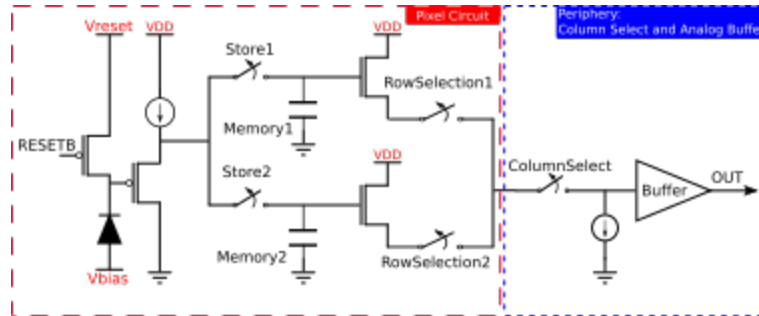
**Figure 3.2:** Conceptual schematic of the Explorer1 ASIC.

is stored in the second memory cell. This allows for measuring the difference in the charge collected by the sensor. The two voltage levels stored in the analog memory cells are read-out sequentially and shipped off-chip where digitisation and the Correlated Double Sampling (CDS) calculation take place. CDS is based on a comparison of two samplings following the reset phase and therefore is independent of the noise introduced by the reset operation. The Explorer1 sensor employs the same circuit but, in order to lower the front-end input capacitance from 3.6 fF to 1.4 fF, it has a different routing and input transistor geometry; this allows for a better measurement of very low-level detector signals.

### 3.1.1 Read-out implementation

The Explorer chip read-out was implemented in the TowerJazz 180 nm CMOS process on 4 metal layers by the author. The read-out circuit dimensions are $3679.2 \times 33.34$ $\mu$m$^2$. The netlist was designed using System Verilog Hardware Description Language (HDL). The architecture of the sequential read-out is based on a shift register.

The shift register is used to sequentially activate the read-out of different pixels in the matrix. Only one analog memory value per clock cycle is stored in the output OUT, as seen in Figure 3.2. Two analog values, corresponding to the independent analog memories, are sequentially read out per pixel. The difference between these two values corresponds to the signal collected by the pixel during this time, called integration time. This difference is calculated off-chip.
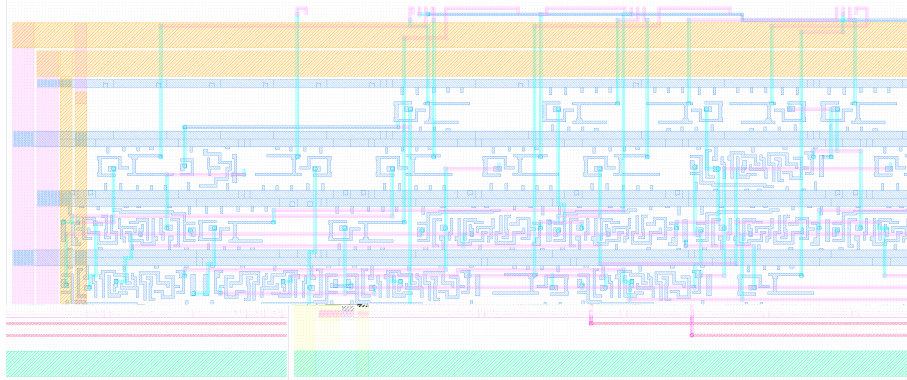
**Figure 3.3:** Part of the Explorer sensor read-out layout implemented by the author. Metal M1, M3 are for horizontal routing in blue and magenta and M2 vertical is shown in green

From the layout point of view, the control output buffers are placed close to the output on top of the circuit. The RC factor was taken in account to select the driving capabilities of the buffers. The buffers were dimensioned to be able to drive the net; in fact the largest buffer strength in the library had to be selected.

The Explorer sensor read-out was designed in 4 metal layers layers, where metal 3 and metal 4 were selected for the power stripes. Metal 1, metal 2 and some metal 3 were used for cell interconnections. The FF of the three shift registers were placed manually using a placement script. Each FF was placed as close as possible to the next one, except in some cases where a gap was required for the automatic placement of buffers for the clock tree or for the FF's reset net tree.

### 3.1.2 Read-out control

The pixel analog storage is controlled by three signals: RESETB, STORE1 and STORE2. These external signals are buffered on the read-out before being sent to every pixel in the matrix.

An initialization phase is required to charge the storage capacitors in the pixel to the correct operating point and initialization with a specific value. The initialization is done by activating the following three

nets at the same time: RESETB, STORE1 and STORE2. Figure 3.4
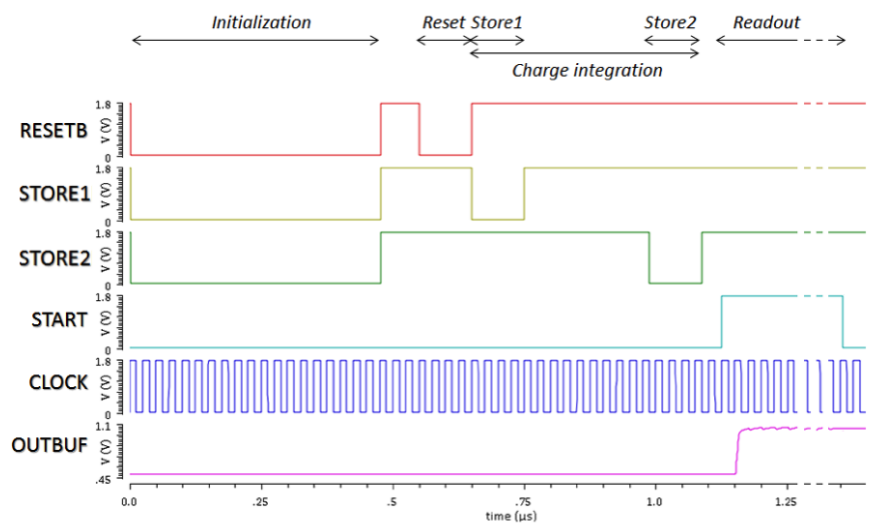


**Figure 3.4:** Read-out control signals designed by the author. The Pixel reset signal RESETB, the selection of the first memory STORE1, selection of the second memory STORE2, read-out start signal START, the general clock signal CLOCK and the serial output signal OUTBUF.

shows the control and the output signals during the initialization, reset, charge integration and read-out phases. Each acquisition cycle requires a reset phase where RESETB pulse resets all the pixel input nodes. Once the RESETB signal is released, the STORE1 signal has to be activated to store the analog reference value on Memory1. Later, the STORE2 signal has to be activated to store the analog information in Memory2. In this example both signals last four clock cycles. STORE1 and STORE2 therefore define the integration time window corresponding to the data acquisition. After the charge integration phase, it is possible to run a serial read-out by activating the digital control logic with the START signal. The digital control circuit operates the internal switches in order to make available the value stored on the analog memories on the OUTBUF output. The sequence of read-out is row after row from the top of the matrix down in one column, and then column after column from left to right. For each pixel, firstly, the Memory1 value is presented to the output and then the Memory2 value. The transition to new data is initiated on every

clock. The sampling of the value therefore happens on the rising edge of the clock just before the data changes. Once the read-out phase is done, the START signal has to be released and it is possible to run a new integration cycle starting from the reset phase.
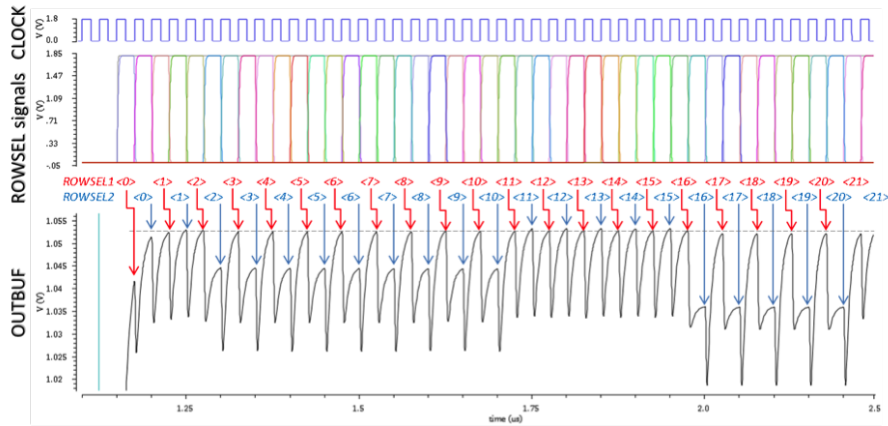


**Figure 3.5:** Detail of the OUTBUF signal.

The Test Pulse is applied at the same time to all pixels of these rows; the rest of pixels should be inactive (see Figure 3.5). A Test Pulse can be applied to the following rows: 28, 29, 58, 59, 60, 61 on matrix1 and 18, 19, 38, 39, 40, 41 on matrix2. The test pulse procedure can be executed as a normal read-out where the test pulse is sent to the pixels cells as a controllable voltage step. Figure 3.5 shows the ROWSEL signals and the OUTBUF output during the read-out of the first 22 pixels of the first column (COLSEL<0> active). For each clock cycle only the ROWSEL signal reported in the line below is active.

### 3.1.3 Experimental results

The sensor performance has been characterized before and after neutron irradiation using a $^{55}$Fe source. In silicon, 5.9 keV X-ray photons from a $^{55}$Fe source generate on average about 1640 electrons in a small volume, allowing to study the effect of radiation as a function of the position of the X-ray conversion. Electrons generated in the depleted volume underneath the collection diode immediately drift to the col-
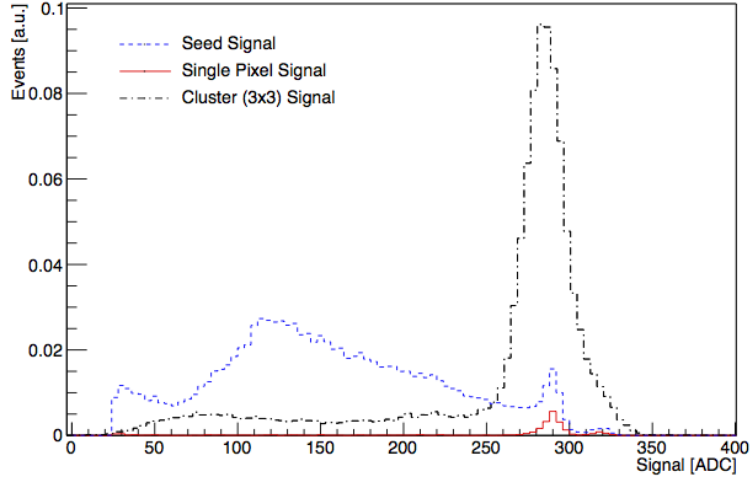
**Figure 3.6:** Seed signal, single pixel cluster signal and $3 \times 3$-cluster signal distribution for an Explorer1 sensor.
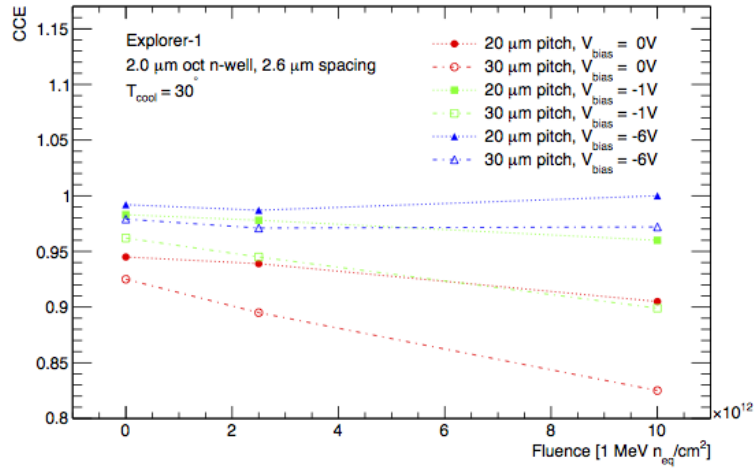


**Figure 3.7:** Effect of NIEL and Cluster CCE measured with Explorer1 sensor for various collection diode designs and different $V_{BB}$.

lection diode, whereas most electrons generated outside the depleted volume first diffuse across the epitaxial layer before entering a depleted volume and being collected. In the majority of the cases the generated charge is spread around several pixels forming a cluster. The

pixel with the highest charge in a cluster is defined as be the seed pixel. A typical seed pixel spectrum is shown in Figure 3.6.
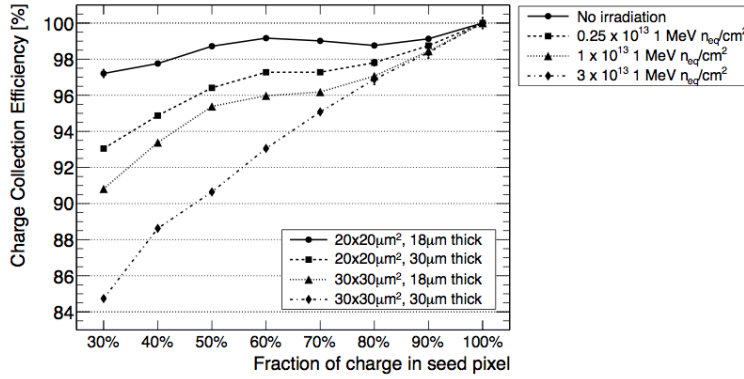


**Figure 3.8:** Cluster CCE measured for Explorer1 sensor for different sensor volumes and a back bias voltage of -6 Vdc before and after irradiation.

The shape of the spectrum depends on the geometry and the operational parameters of the sensor. In order to quantify the behaviour of the spectrum before and after irradiation, the mean value has been calculated for all signal entries in the interval between the signal value of the peak at the right of the spectrum and 50% of that signal value. The charge collection by drift is much faster and therefore significantly reduces the probability for signal charge to be captured by traps, and therefore is much less sensitive to NIEL (Figure 3.7).

The Figure 3.8 shows the seed and the cluster CCE measured for Explorer1 chips of two different pitches and reverse bias voltages before and after irradiation with neutrons. The CCE is defined as the ratio of the detected charge and the charge produced by an impinging particle. The cluster CCE is calculated using the ratio of of the MPV (Most Probable Value) of an incident particle cluster-signal distribution and the MPV of the single-pixel cluster signal distribution. As the cluster signal, the cluster CCE depends on the choice of thresholds for the assignment of the pixels to a cluster. Since the probability of NIEL induced charge trapping is essentially proportional to the path length of such electrons before being collected at the collection diode, one would expect the seed pixel spectrum, and consequently the seed CCE, to be only marginally affected by neutron irradiation due to the low
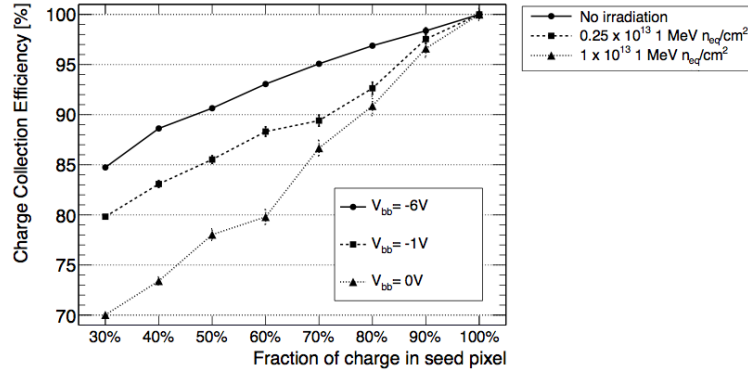
**Figure 3.9:** Cluster CCE measured for a Explorer1 sensor with a 30×30 $\mu$m$^2$ pitch before and after irradiation for different back bias voltage.

trapping probability. This is shown in Figure 3.9, where the seed CCE remains almost unchanged after irradiation with neutrons. The CCE is more affected for charges generated between two adjacent pixels.

The CCE effect also depends on the pixel cell volume which is proportional to the pitch size and epitaxial layer thickness. Figure 3.8 shows the cluster CCE measured for Explorer1 chips of two different pitches and epitaxial layer thickness as a function of the cluster signal fraction collection by the seed pixel after neutron irradiation with $1\times10^{13}$ 1 MeV $n_{eq}$cm$^{-2}$. As expected, it is more pronounced for pixels with larger sensor volumes. Figure 3.9 shows the CCE measured for an Explorer1 chip with a pitch of $30 \times 30$ $\mu$m$^2$ before and after neutron irradiation with $1\times10^{13}$ 1 MeV $n_{eq}$cm$^{-2}$ for various back bias settings. Increased reverse substrate bias extends depletion around the collection electrode and favours collection by drift and therefore significantly reduces the impact of NIEL.

## 3.2 The PADRE circuit in the pALPIDEss

The pALPIDEss chip implements a non-continuous zero suppression architecture based on PADRE for matrix pixel read-out. The matrix is made of pixels of 22 $\mu$m x 22 $\mu$m, arranged in 64 columns of 512 pixels in a single column for a total of 32678 pixels [86, 89]. A screen-
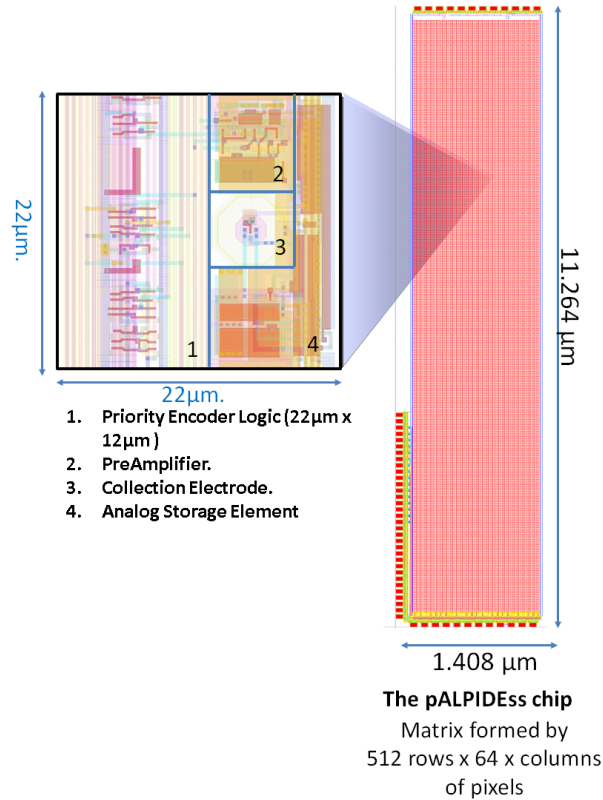
**Figure 3.10:** pALPIDEss chip layout and pixel layout. The pixel is $22 \times 22 \ \mu m^2$.

short of its layout as submitted in 2013 is shown in Figure 3.10. Each pixel is organized into an analog section (containing the sensor, the amplifier, the discriminator, and a capacitor as a dynamic memory buffer) and a digital section, which hosts the read-out logic. The PADRE is one encoding schema to allow the implementation of a data driven read-out. The advantage of this technique is that it does not require hard-wire encoding of the address of each pixel. Furthermore, it can be implemented without distributing a read-out clock to the pixel matrix, favouring low power consumption and low noise.

The pALPIDEss read-out is implemented in two levels designed by the author, one within the column and one at the bottom to define the priority for the different columns. First of all, there is a PADRE circuit
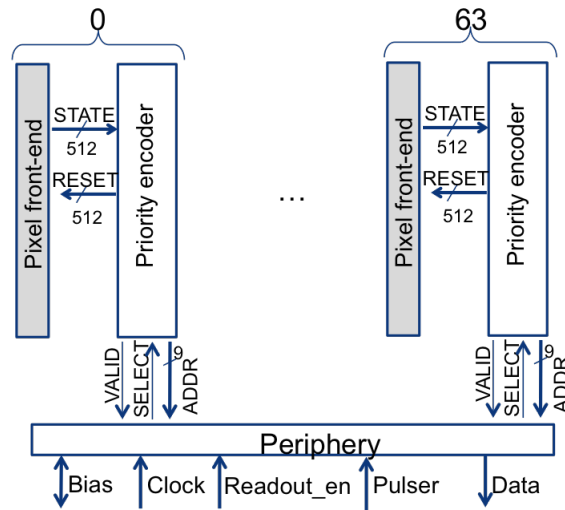
**Figure 3.11:** pALPIDEss chip block diagram.

of 512 pixels organized in a single column, named the priority encoder. Secondly, there is an EoC that is the read-out of 64 priority encoders, having 5 hierarchy levels of PADRE basic blocks. The pALPIDEss sensor generates a VALID assertion every clock cycle and an address of the first hit pixel. According to a certain priority hierarchy tree, at the end of the clock cycle that particular pixel is reset and the circuit logic will select the next hit pixel. The encoded address has 15 bits, where the highest 6 bits are the fired column and the remaining 9 bits are for the position of the fired pixel in the column.

The EoC read-out is operated and controlled by 2 signals at the periphery level. The input read-out_ena signal is the enable signal for the EoC read-out and the input clock signal is managed clock signal to reset the pixel memory buffer to an initial state. These two signals are back forward to all PADRE for each EoC hierarchical layer (Figure 3.11). The maximum read-out speed of this circuit is 50 Mhz.

### 3.2.1 Encoding process

The pALPIDEss priority encoder provides the read-out from the pixel to the periphery. The main process is the encoding of the Address of the first triggered pixel in the input STATE vector. It also forwards a RESET signal from the Periphery to the selected or encoded pixel buffer to be reset. This read-out cycle is repeated for each fired pixel and it is is controlled by the periphery (Figure 3.12).
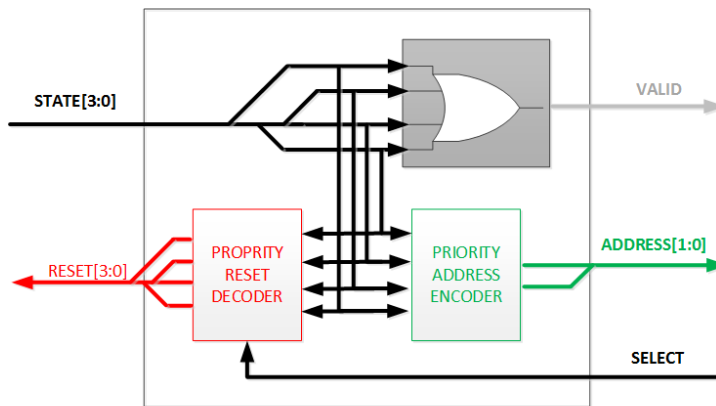


**Figure 3.12:** PADRE basic cell implemented by the author.

The PADRE basic CELL implementation is based on a FAST-OR, a priority address encoder and an one-hot reset decoder.

The PADRE basic cell encodes the address and decodes the fired pixel to be RESET in the next falling edge clock cycle, when one pixel is fired in the whole column, as can be seen in Figure 3.14. As sketched in the diagram of Figure 3.13, the PADRE cell works in the following way: It can generate a valid signal only if at least one pixel has a valid hit. The circuit is organized as a tree with 4 levels of hierarchy. Each cell has 4 child cells that can be pixels or other basic cells. The basic Cell forward up the hierarchy the logic OR of the STATES. It also encodes the address of the first active child cell, sending it to the next level.

At the same time, the RESET signal is routed down-wards to the first active child cell. This routes the RESET signal from the periphery
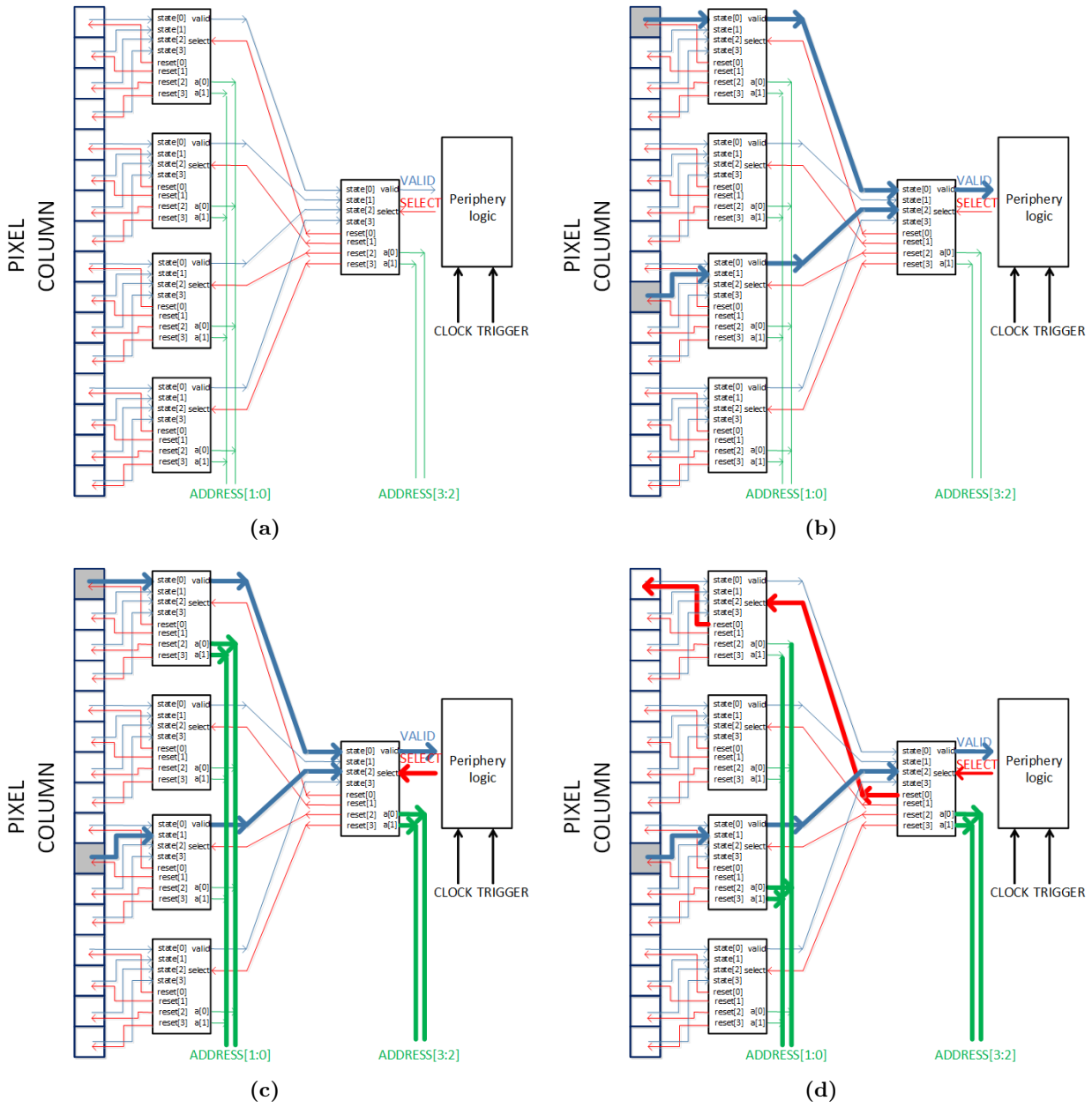
**Figure 3.13:** Read-out of 2 fired pixels.
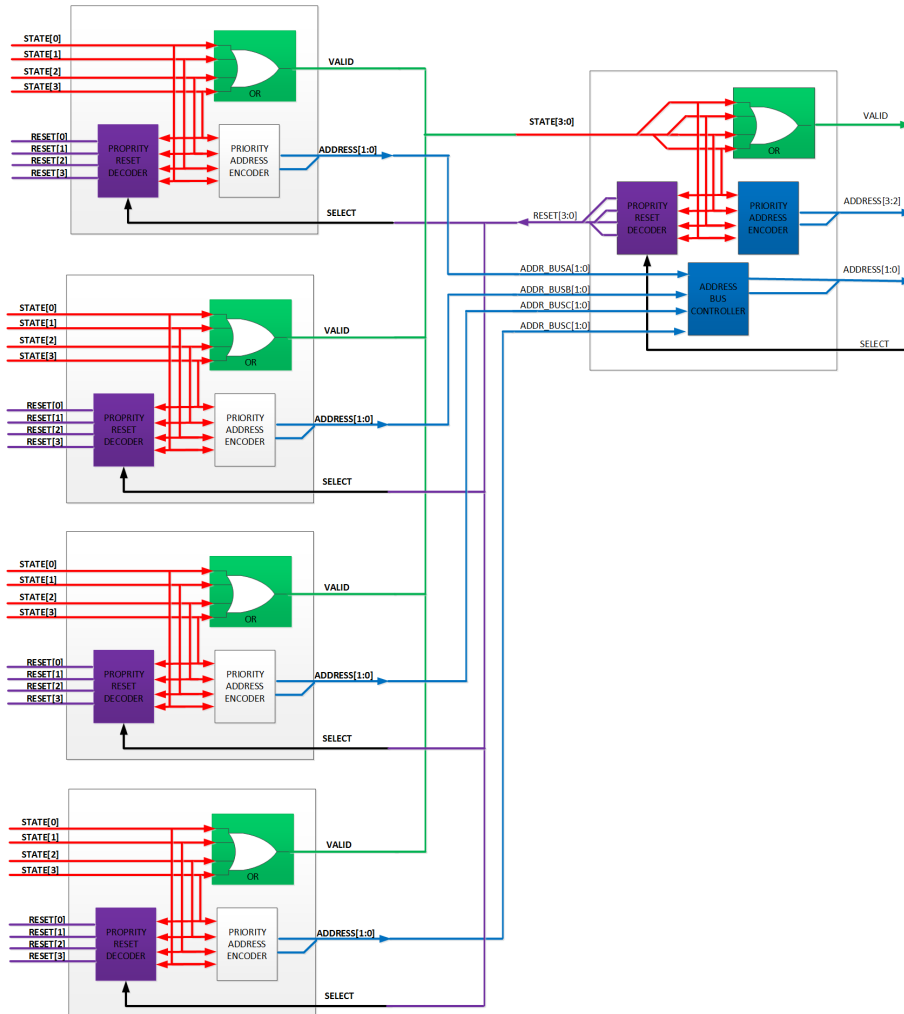
**Figure 3.14:** Simplified ALPIDEss PADRE tree interconection diagram with 2 levels of hierarchy.

through the hierarchy to the active pixel. The address produced by the active child cell is selected and buffered into the next higher level. This read-out cycle is repeated for each fired pixel until the VALID signal is de-asserted.

The number of layers in a priority encoding scheme depends on the number of inputs that a basic block can handle. For instance, in our

encoding process it has a unit block with four inputs. In this case, the output address line will be a two-bit bus and only two levels of hierarchy will be needed. In general, it can be proven that if N is the total number of pixels to be read-out and b is the number of inputs of the basic block ($N_{layer}$), then the number of layers and the total number of blocks ($N_{block}$) are given respectively by:

$$N_{layer} = log_b(N) \tag{3.1}$$

$$N_{block} = \frac{N-1}{b-1} \tag{3.2}$$

### 3.2.2   Physical Implementation
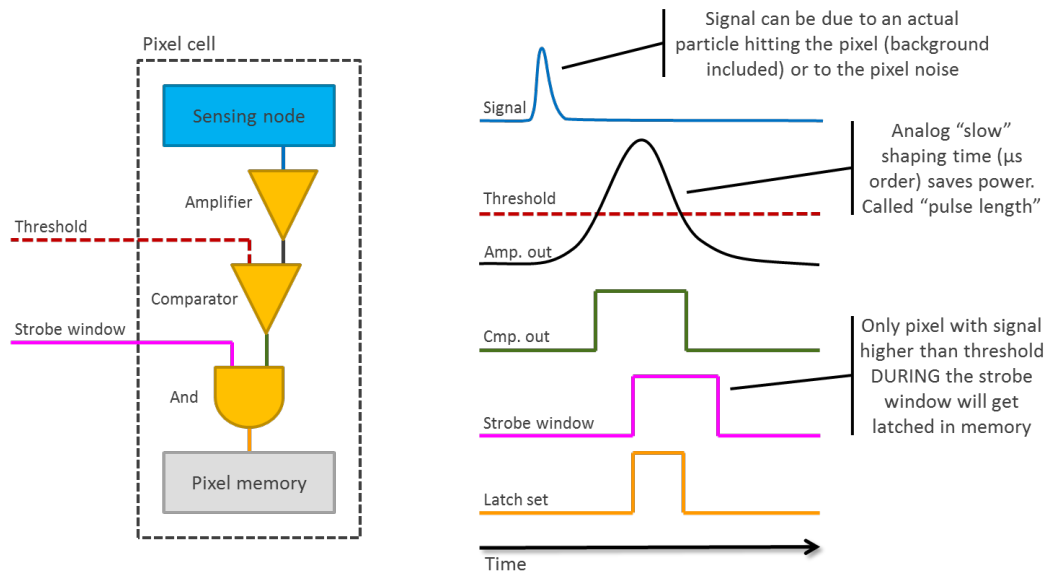


**Figure 3.15:** pALPIDE front-end block diagram.

The use of in-pixel discriminators also offers the opportunity for a data driven read-out, in which only the pixels above a given threshold transfer their data to the chip periphery. In this scheme, the detecting diode are biased by a diode which is linked to a reference voltage and provides the leakage current drawn by the detecting diode. The node

connecting, detecting and biasing diode is linked to the amplifier input. The open loop amplifier amplifies the signal and also includes filtering to shape the signal and optimize the signal-to-noise performance. The amplifier output is connected to a comparator for which the threshold can be adjusted. A hit detected by the comparator is stored in a capacitor (a named memory buffer) which retains the hit information even after the comparator output returns to zero, and interfaces with the priority encoder for the read-out. A block diagram of the circuit is shown in Figure 3.15. Figure 3.16 depicts the pALPIDEss sensor pixel register which is a Dynamic Memory Cell based on a capacitor of 80 fF which is used as an in-pixel hit buffer. During reset, this capacitor is charged. This memory buffer was digitally modelled as a latch with a falling-edge reset signal. In the analog section of each pixel, the sensing diode (IN) is connected to a discriminator and one bit memory cell; when the charge collected by the sensing diode exceeds a certain threshold, the pixel memory (if enabled) is asserted.
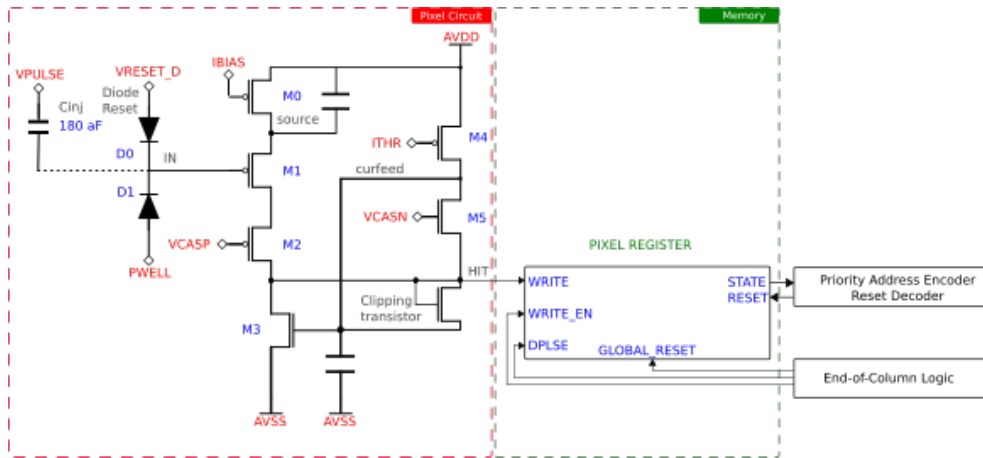


**Figure 3.16:** Schematic drawing of the pALPIDEss sensor circuitry.

The IN signal from the front-end controls the discharging of the capacitor via a transistor. The length of the IN pulse hence needs to be long and high enough to discharge the capacitor below a threshold based on the settings of $I_{THR}$ and $V_{CASN}$. The read-out logic performing the priority address encoding and reset decoder is able to read and/or reset the pixel register cells of the 512 pixels.

The EoC circuit receives as input the logic signals from the 64 columns and sends the chip output pads the addresses of the pixel memories cells which are fired, according to their priority scheme. The EoC read-out is based on the same architecture, a Priority Address Encoder and Priority Reset Decoder. The implementation was designed on combinatorial logic; no FFs or memories were placed in the EoC to avoid SEE effects. Also, the EoC forward-up the global signals to enable the correct functionality of the pixel register.

### 3.2.3 PADRE implementation

As described earlier, the physical implementation of the pALPIDEss priority encoder is based on a top-down flow, where the circuit was placed and routed (PnR) horizontally, thereby improving the routing connection and bringing the power on lower metal connection to the top metal where the power matrix is located. The PADRE basic cell and priority encoder were implemented on customized TowerJazz 180 nm CMOS Standard Cells. The modification was the removal of the nMOS bulk contact on all standard cells. This modification, is to enable the back-bias on the pixel where a PWELL potential will be applied and the Towerjazz standar cell, the nMOS bulk is comnected to digital groud. The placement and routing was followed the top-down flow for Encounter a CADENCE software for digital implementations [90].

The customized standard cells were imported into Virtuoso Open Access views and generated the layout, schematic and abstract view. Thereafter, the top-down flow was executed to generates the layout file, the simulation files and physical verification, testing the DRC and LVS (layout versus schematic) checks and generates the timing propagation and the arcs timing delays for simulation and verification.

Figure 3.17 shows a segment of the pALPIDEss priority encoder circuit where the orientation is rotated. The column axis is horizontal in this illustration. The circuit includes 1 ROW of standard CELLS for the full height of the Column plus additional routing space on the left and right. The total width of the circuit is 10.2 $\mu$m.
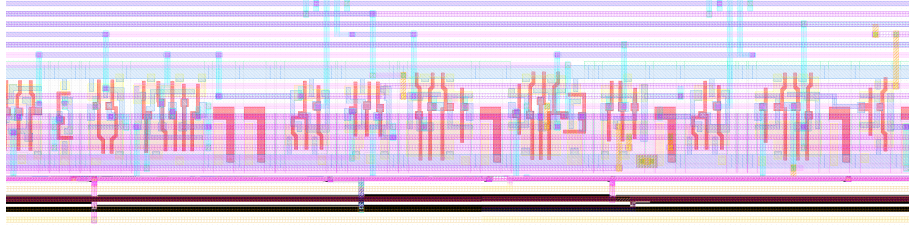
**Figure 3.17:** pALPIDEss priority encoder implementation based on customized standard cells, modified by the author; this circuit is placed and routed using the Encounter CAE tool.

The matrix is built with the placement of the 64 front-end column of priority encoder and with their priority encoders; these columns are then adjacent (see Figure 3.18).

### 3.2.3.1 Considerations about power consumption

The total power consumption of the sensor has three main contributions: the power consumption of the front-end circuits, PADRE circuits and the digital periphery. The front-end power contribution is independent of the hit density and is mainly due to the $I_{BIAS}$ current (20 nA). Since the supply voltage is 1.8Vdc, the power consumption of the 524288 front-end circuits is about 18.9 mW.

The power consumption of the priority encoder circuit depends on the average hit density, on the cluster multiplicity and on the trigger rate. Assuming the previous values for the hit density and cluster multiplicity and considering a trigger rate of 100 kHz, the total power consumption of the read-out of the matrix is about 8.26 $\mu$W. This value was calculated assuming that the total energy consumed by a priority encoder reading-out the address of a hit pixel is 70 pJ (from analog simulations and Encounter power analysis generated by the author):

$$P = [hitdensity] \times [area] \times [clustersize] \times [evrate] \times 70pJ \quad (3.3)$$
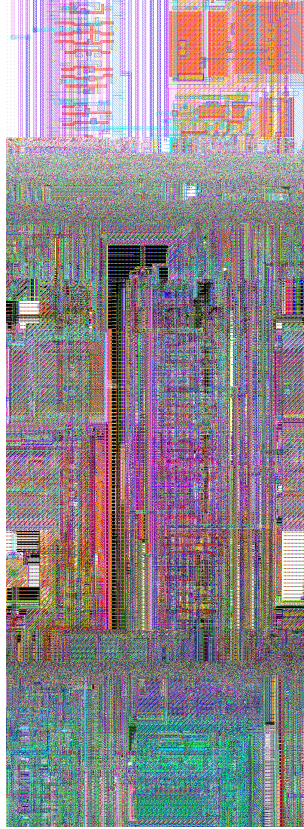
**Figure 3.18:** Priority encoder circuit interfaced with a column of front-end electronics merged with the Virtuoso CAE tool.

### 3.2.4 Experimental results

The pALPIDEss-0 chip is the first version of the ALPIDE architecture. In order to minimise the front-end capacitance, the pMOS input transistor was placed in the collection n-well to reduce its capacitance. During the initial tests of the pALPIDEss-0 chip at default settings, the chip did not reliably respond to pulsing via the injection capacitors. This problem was solved by exposing the chip to visible light. In order to study this behaviour, an array of white LEDs was built to shine a well-defined amount of light onto the chip. The problem was the leakage current on the parasitic diode of the pMOS transistor, the collection electrode diode and the reset diode. The light increases the

leakage current on the collection electrode diode, changing the operation point of the collection diode to a highest leakage current than the parasitic diode enabling the leakage current of the reset diode. For the next iteration of the family this issue was solved.

The characterisation of the pALPIDEss prototypes was carried out and the full laboratory software framework for the ALPIDE developed. In addition, a full custom readout system was designed by INFN Padua and RD51 collaboration [91, 92] based on Xilinx Virtex-5 FPGA 16 and ADC card of 16 differential analog inputs which are digitised by two 12 bit 8 channel ADCs running at 40 MSample/s. Furthermore, the pALPIDEss sensor was integrated into the EUDAQ [81, 82]; this a a test-beam data acquisition system based on the EUTelescope [93, 94] was adapted for the use with the pALPIDEss sensor., which was adapted for use with the pALPIDEss.

The read-out principle of the pALPIDEss sensor was validated in simulations and the functionality was correlated in the lab using a radioactive source and an irradiation campaign. This priority encoder circuit read-out is faster and exhibits lower power consumption than the other MAPS read-out but it has a problem: the routing of the priority encoder circuit is hard-wired. Table 4.4 summarizes the power consumption and integration time of read-out chips in the development of the ITS upgrade. The ALICE ITS characterization team detected a problem. That problem which is systematically observed in a few positions of the columns. The pixel has a higher gain in charge collection. After a visual inspection of the layout of the circuit, the problem was discovered to arise when fractions of propagation nets on metal 4 are close to the interface with the front-end. These nets generate digital noise to the front-end in read-out mode. The solution to this issue was to shield the interface between the front-end and the digital read-out with a pWELL contact, and it was tested in the pALPIDEfs.

### 3.2.4.1 Lab measurement

Figure 3.19 shows the hit-map of the chip under $^{55}$Fe irradiation source exposure with a epitaxial layer thickness of 18 $\mu$m. The idea behind this type of test is to stress the collection electrode as a detector influenced by the radiation source and to test the front-end and read-out chain at the same time. This plot shows that the prototype is fully operational but an implementation problem was spotted: an extra charge is collected on the rows 125 , shown as a green stripe. The author did a study trying to identify this issue. The conclusion: the extra charge was induced by the digital noise coupled with the collection electrode and the automatic routing of the priority encoder circuit read-out. To solve this issue, the digital routing nets must be shielded to avoid charge coupling between the digital domain and the analog domain.
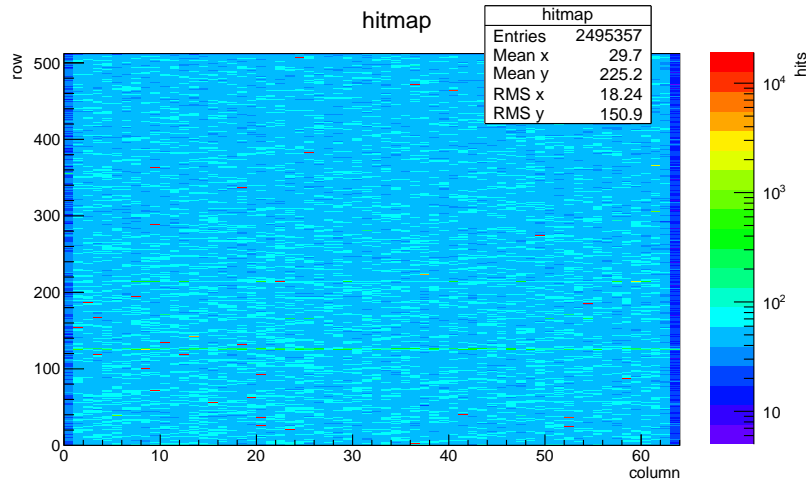


**Figure 3.19:** pALPIDEss sensor hit-map under $^{55}$Fe irradiation source exposure with an epitaxial layer thickness of 18 $\mu$m.

#### 3.2.4.2   Test beam measurement

The test beam measurement was performed at the CERN PS using a 6 GeV $\pi^-$ beam and at the CERN SPS with a 120 GeV $\pi^-$ beam. Figure 3.20 shows the efficiency for different bias settings of $V_{CAN}$ with different $I_{THR}$ settings and back bias applied to the substrate. The plot shows that the efficiency is bellow 100% for a $I_{THR}$ higher than 1.5 $\mu$A. This plot shows the dependence of the biasing and the benefit of the back bias increasing the charge collection.
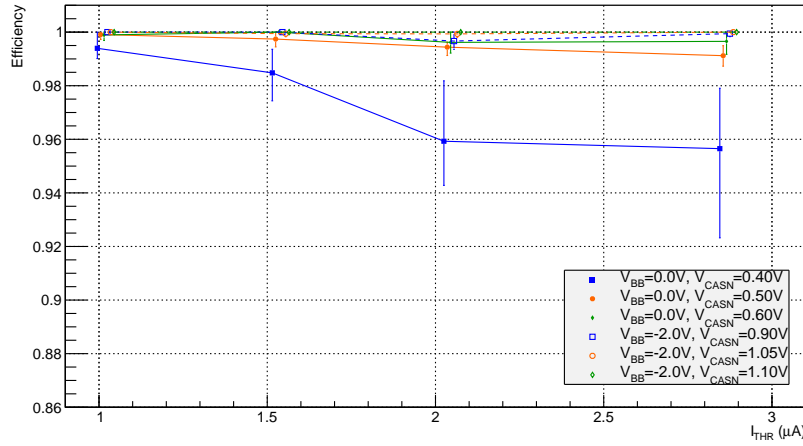


**Figure 3.20:** pALPIDEss sensor test beam at CERN. The plot show the Charge Collection efficiency (CCE) vs different settings of $I_{THR}$ with different $V_{CASN}$ and $V_{BB}$ settings.

The detection efficiency represents the probability of a sensor to detect traversing charged particles. It is determined by two effects: firstly, the charge collected in the seed pixel (and the related distribution) and hence by the sensor geometry, the reverse substrate bias and the particle type and energy, and secondly, the charge threshold. Consequently, lowering the threshold is beneficial for the detection efficiency, which is, however, limited by the increase of the fake-hit rate, as discussed in the previous section. Hence, a trade-off has to be found.

Figure 3.21 shows the fake hit rate of $10^{-5}$ for a $I_{THR}$ higher 1.5 $mu$A and $V_{CASN}$ higher 0.5 Vdc and back bias higher than -2 Vdc. The first results close to the requirements on fake hit for the ITS upgrade are summarized in Table 1.5.
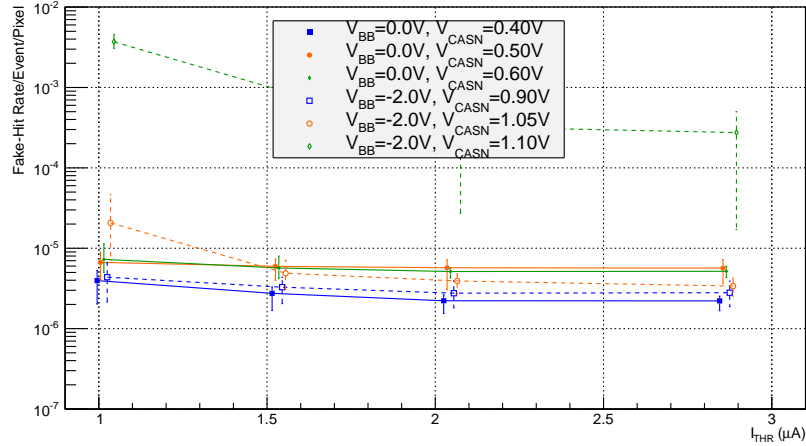
**Figure 3.21:** pALPIDEss sensor test beam at CERN. The plot shows the hit fake rate vs different settings of $I_{THR}$ with differetn $V_{CASN}$ and $V_{BB}$ settings.

The main parameters for influencing the threshold and noise were found to be $V_{CASN}$ and $I_{THR}$. If the $I_{THR}$ current increase the $V_{CASN}$ decrease affecting the default parameters of the front-end. Figure 3.22 shows how an increase of $V_{CASN}$ reverse substrate bias of -2 Vdc leads to a lower threshold, as it corresponds to a higher baseline value of the output pulse at the IN signal node (see Figure 3.16). A decrease in $I_{THR}$ leads to a lower input charge threshold, as expected from the slower reaction of the feedback mechanism discharging the IN signal. However, it has to be adjusted depending on the back bias. This can be explained by the nMOS transistor being embedded in a pWELL, which is set to $V_{BB}$. $V_{CASN}$ also influences the fake hit rate when its threshold is adjusted.

## 3.3 ORTHOPIX

The ORTHOPIX chip is a MAPS prototype designed at CERN (Figure 3.23) and submitted in a MPW in 2013. The idea was to try to test and to demonstrate the feasibility of the ORTHOPIX architecture [69]. This architecture is designed for compressing data in arrays where only a few elements contain useful information, as described in [95, 96].
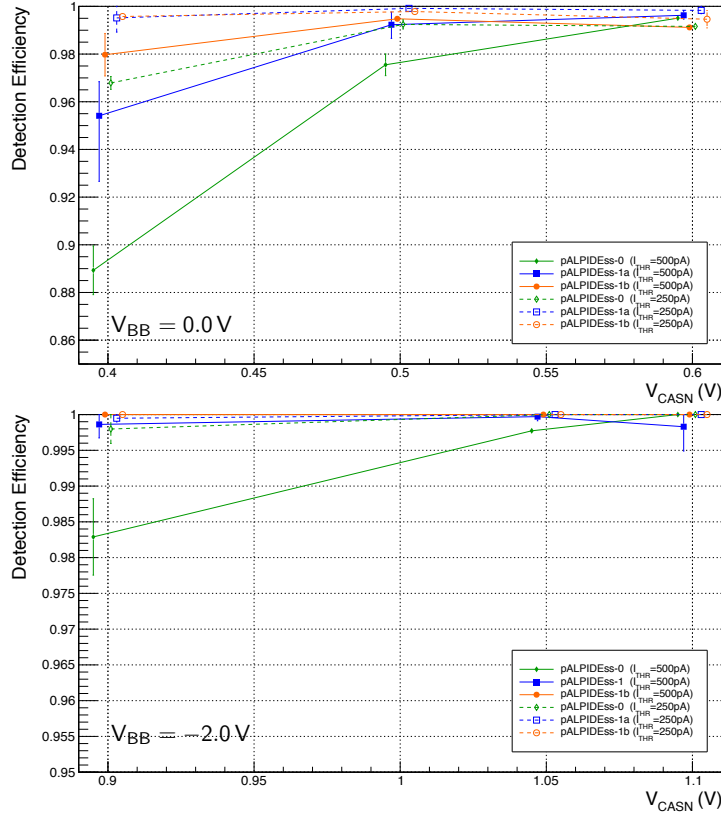
**Figure 3.22:** Detection efficiency as function of $V_{CASN}$ and $I_{THR}$ settings for different pALPIDEss prototypes. Top: without reverse substrate bias $V_{BB} = 0$ Vdc. Bottom: for $V_{BB} = -2$ Vdc.

The ORTHOPIX architecture reads the pixel matrix using a multiple projection scheme (Figure 3.24). In this prototype each pixel has four static connections to the periphery, each of them corresponding to one of four projections: X, Y, U and V. X and Y correspond to the classical row and column projections, while U and V are carefully chosen to minimize ambiguity in the case of multiple hits. In fact these projections satisfy a particular orthogonality condition, hence the name of OrthoPix. All projections are stored in flip-flops to be read-out by the control logic. The prototype matrix contains 255×255 pixels of size 10 $\mu$m×10 $\mu$m each; the orthogonality condition is satisfied only for
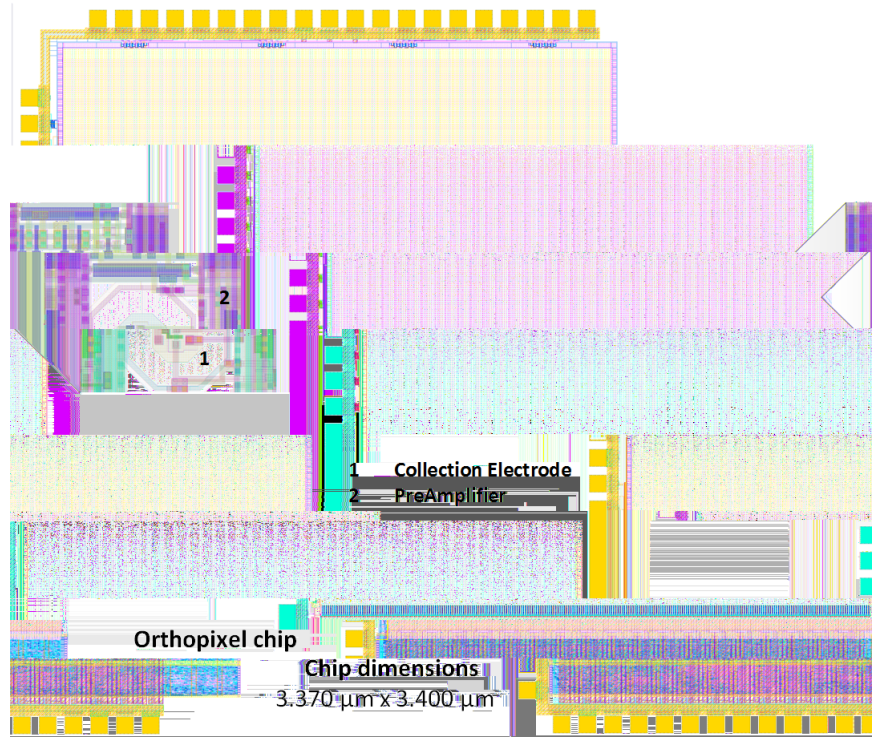
**Figure 3.23:** Orthopix chip layout and pixel floorplan.

an odd number of pixels in the projection. Each projection maps the full matrix into 255 signals, and each signal corresponds to a distinct group of 255 pixels. The projections used in the ORTHOPIX architecture scheme allow to reduce in the number of signals to be treated, in this example from $255 \times 255$ to $4 \times 255$ (or 1020), corresponding to a reduction factor of about 64. At the matrix periphery these 1020 signals are presented to 1020 comparators which write into a register if the signal at the comparator input exceeds a threshold. Two ways of reading out these registers are implemented and are described in the next section.

Concerning the horizontal and vertical connections, assuming 'x' is the number of pixel in the matrix, starting from 1 as the top left pixel and finishing with $255 \times 255 = 65025$ as the bottom right pixel, then
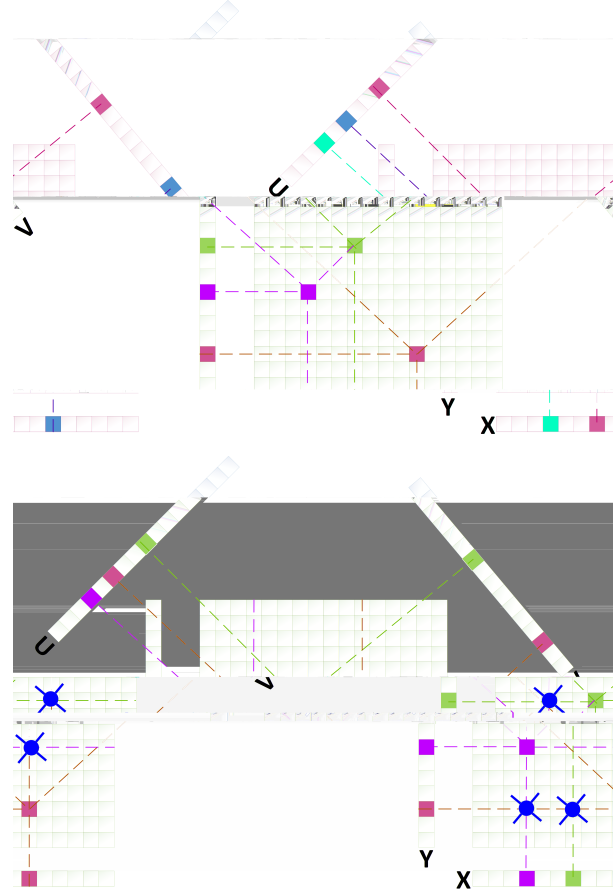
**Figure 3.24:** OrthoPix architecture projections scheme.

the index of the 1020 comparators can be associated to the pixel index with the following formula:

$$OUT_1 < x >= OUTcomp < [(x-1) \times 4 + 1] \; mod \; 1020 > \qquad (3.4)$$
$$OUT_4 < x >= OUTcomp < (int(x/255) - 1) \times 4 + 4 > \qquad (3.5)$$

Concerning the diagonal, the first step is to associate a pixel 'x' to the corresponding diagonal 'd', keeping in mind that the first primary diagonal OUT2<1> contains the pixels located on the primary di-

agonal of the matrix (1, 257, 513, 679, ...) and the first secondary diagonal OUT3<1> contains the pixels (2, 256, 1020, 2039, ....). For the diagonals the assignment is as follows:

$$OUT2 < d >= OUTcomp < (n-1) \times 4 + 2 > \qquad (3.6)$$
$$OUT3 < d >= OUTcomp < (n-1) \times 4 + 3 > \qquad (3.7)$$

Two read-out systems were implemented to read the 1020 bits memory, which contains the data frame designed and implemented by the author. The first one is based on a Circular Shift Register with a serial output, similar to a rolling-shutter, where the memory is read-out sequentially. It is mostly intended for testing and debugging purposes. The second circuit is based on an asynchronous priority encoding sparsification scheme, which performs further data reduction with very low power consumption. This implementation of a read-out is different from the approach adopted by traditional hybrid pixel detectors in HEP. The priority encoder has a tree structure in order to reduce the steps necessary to scan through all the memory elements from n to $\log_n(n)$. The goal of this read-out is to investigate a different implementation of such a read-out.

### 3.3.1 Implementation

The Priority Address Encoder was designed and implemented on the digital flow set up and implemented for TowerJazz 180 nm CMOS standard cells [90]. The read-out circuit dimensions are 2657.59 $\times$ 295.68 $\mu$m$^2$. The routing was implemented in six metal layers, where the metal TOP_M, metal M5 and metal M4 are used for power stripes, the metal M1 and M3 are for horizontal routing and metal M2 for vertical (Figure 3.25).

The placement of the flip-flops for the hit storage were placed according to the pin placement of the 1020 projected lines. For the shift register, the placement of the flip-flops was made close to one another, in order to minimize the interconnection routing, giving small gaps for
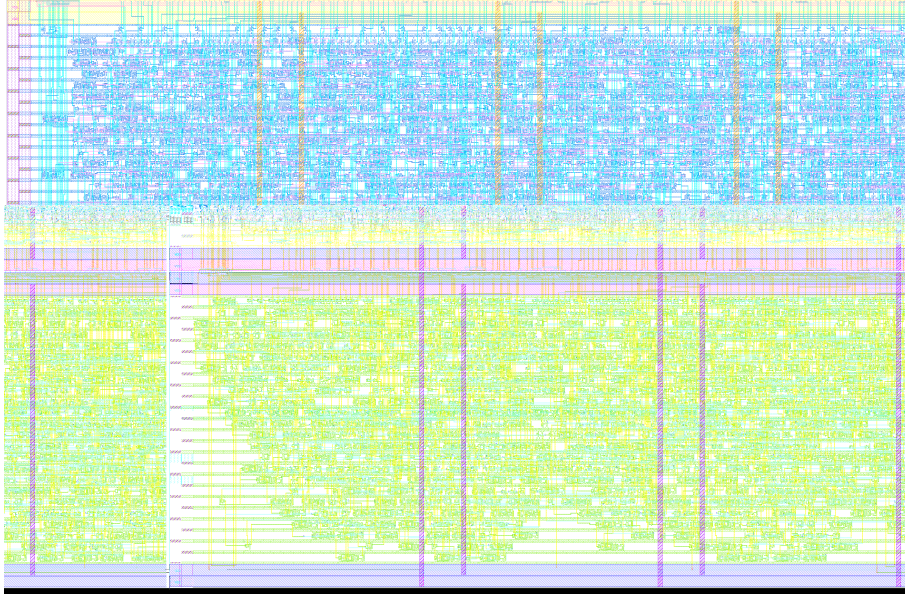
**Figure 3.25:** Part of the read-out layout implemented by the author; on top we can see the shift register and on bottom the Priority Address Encoder.

the clock tree, reset tree and enable tree. The same idea was used in the priority address encoder implementation.

The free channels in M4 were used to shield the sensitive area from the digital switching noise. M5 was routed over the M4 shielding channels for the pixel biasing nets, as can be seen in the bottom side of Figure 3.23 in the bottom side. The power estimation and voltage drop were calculated using the power analysis tool of Encounter; as result, the power stripes widths and power distribution was correct with a voltage drop within of 10% on the supply voltage.

### 3.3.2 Priority Address Encoder

Priority Address encoder is based on the PADRE scheme previously explained in subsection 3.2.1. The read-out phase, as shown in Figure 3.26, occurs when the signal READOUT_EN is asserted and the circuit is enabled. In order to avoid storing new information in the comparator memory during this phase, MEMWREN has to be dis-

abled. During the read-out, while VALID is active, at each falling edge of the CLOCK signal, the address of the pixel with the highest priority in the matrix is available on OUT[9:0]. That comparator memory will internally reset, thus allowing to send out the address of another pixel following the priority scheme. Once all the comparator memories are read-out, the signal VALID is released. This circuit has been simulated with a clock frequency of 100 MHz.
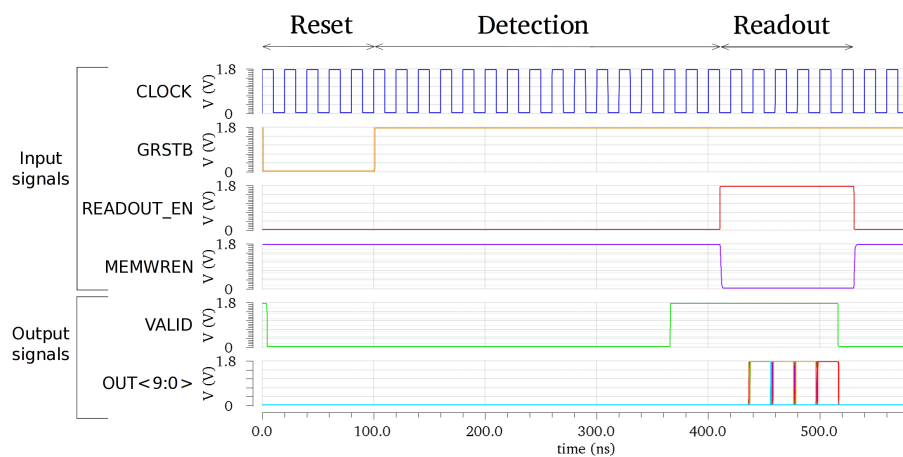


**Figure 3.26:** ORTHOPIX chip read-out by a Priority Address Encoder read-out control and output signals designed by the author. The global clock signal CLK, the active low global reset signal GSTB, the read-out enable signal READOUT_EN the active low memory write enable signal MEMWREN, the propagated or signal named VALID and the column address bus OUT are shown.

### 3.3.3 Shift Register

A Circular Shift Register (CSHR) is a backup read-out circuit. The CSHR is a cascade of flip flops, sharing the same clock, in which the output of each flip-flop is connected to the data input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the bit array stored in it, thereby shifting the data present at its input and shifting out the last bit in the array at each transition of the input clock.

The operations starts as shown in Figure 3.27; when the START signal is asserted the CSHR is off, disabling the input clock net reducing the
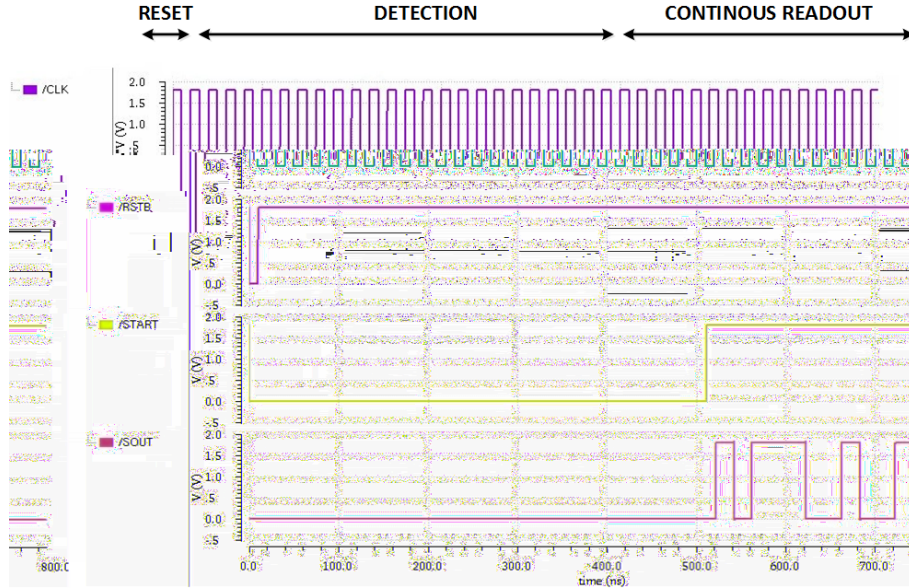
**Figure 3.27:** ORTHOPIX chip read-out by a Priority Address Encoder read-out control and output signals designed by the author. The clock signal CLK, the active low reset signal RSTB, the start enable signal START and the shift register serial output SOUT are shown.

switching power. The CHSR starts when it is enabled on the first rising clock edge. The CSHR starts flipping the pattern, enabling only one pixel of the 1020 projections. It starts the read-out sending on the serial output SOUT the 1020 bits of the comparator memories (one per clock cycle). When all of the bits are sent out, the SR_TEST output is asserted for one clock cycle to indicate the end of the data streaming on SOUT. This circuit has been simulated and tested with a operational CLOCK frequency of 160 MHz.

### 3.3.4 Experimental results

The ORTHOPIX chip was tested in the Padua laser facility attached to the National Institute for Nuclear Physics (INFN) Italy. The chip was tested with a scanning micro-focused laser and a $^{55}$Fe gamma source. It was possible to reconstruct hit pixel position from the compressed data stream as shown in Figure 3.28.

The first step was to verify the pixel mapping scheme by checking how many and which pixel comparators fired at each $^{55}$Fe irradiation souce hit, and if they were correlated as expected. While the observed behavior agrees to that expected, we noticed that for many events all of the four comparators connected to the pixel fired. It was found that threshold settings is one critical parameter of the design, and very low thresholds are necessary to have all four comparators firing for nearly all the pixels. As already stated, the necessity of providing a constant bias current through illumination to make the front-end working renders it difficult to quantitatively evaluate this threshold uniformity; this is the same effect observed in pALPIDEss prototypes [95].
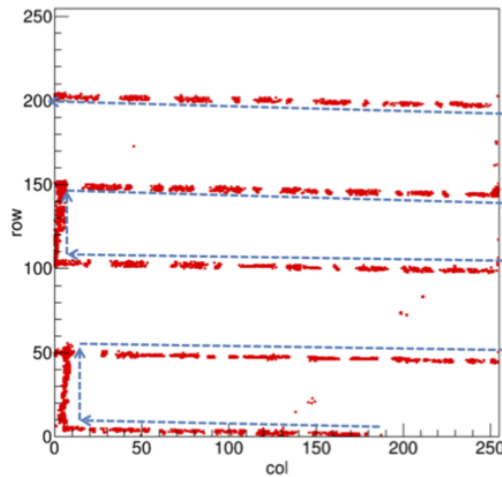


**Figure 3.28:** Laser spot pattern through the ORTHOPIX sensor matrix and reconstructed pattern trace.

A second set of tests was conducted to reconstruct a laser spot position, and to follow it all over the matrix surface. For this laser scanning a 910 nm laser focused onto a 30 $\mu$m spot was used. The relative spot diameter, when compared to the pixel pitch of 10 $\mu$m ensures more than one pixel fires for a given position, therefore approximating a cluster from an ionizing particle.

As a result, it was possible to reconstruct the laser spot position and size all over the matrix. The average measured spot size corresponds

to 3.5 pixels. It is evident, as shown in Figure 3.28, the requirement to lower the thresholds to have all comparators connected to a pixel firing lead to pick-up on some noisy pixels, which clearly appear completely out of the laser track.

## 3.4 Investigator
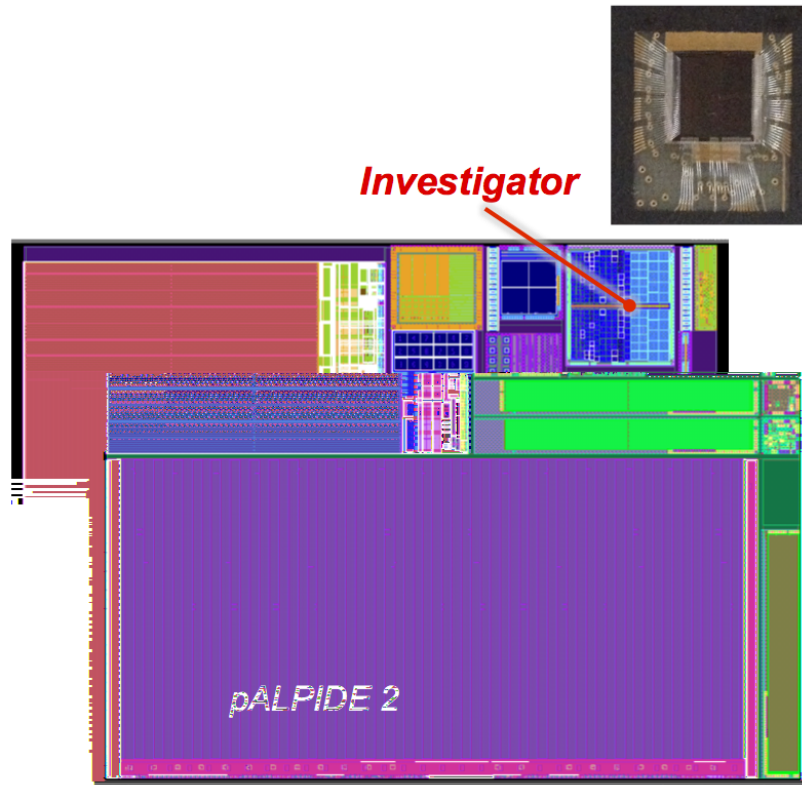


**Figure 3.29:** Mask set Screen-shot of Engineering Run named ITS3. The Investigator is located at the top, and one picture of one wire-bonded Investigator chip to the carrier board is shown in the top.

The Investigator ptototype contains two sets of 134 mini-matrices of 10 x 10 pixels in an array, of which only the central $8 \times 8$ pixels are surrounded by 1 row or column of dummy pixels as is shown in Figure 3.30. On one set it is possible to inject a charge in the pixel

using a pulsing circuit. Each of these mini-matrices can be selected and connected to a set of 64 output buffers. Analog signals can therefore be monitored with sufficient time resolution to study in detail the charge collection in the pixels, (see Figure 3.31), the mini-matrices location and identification.
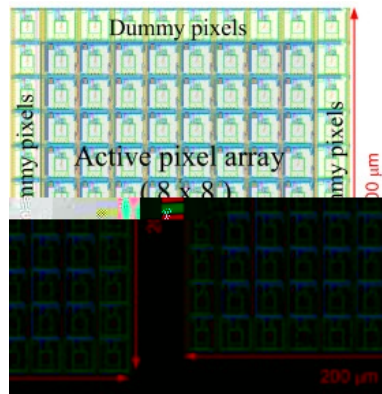


**Figure 3.30:** 8×8 small prototype pixel matrix surrounded by dummy pixels.

The current source follower are widely used for MAPS read-out: they increase charge conversion gain $(1/C_{eff})$ or decrease the effective sensing node capacitance $C_{eff}$ because the follower compensates part of the input capacitance. Charge conversion gain is critical for analog power consumption and, therefore, for material budget in tracking applications, and it also has a direct system impact. For the ITS upgrade, low material budget is a primary requirement. The Source-Drain Follower (SDF) circuit was studied as part of the effort to optimize the effective capacitance of the sensing node [84]. The reverse sensor bias reduces the collection electrode capacitance. The test chip, manufactured in the TowerJazz 180 nm CMOS Image Sensor process, implements a small prototype pixel. In addition, the main point of the Investigator sensor is that the chip provides fast outputs of the pixels in parallel, allowing for a detailed study of charge collection and signal formation, as shown in Figure 3.29.

Therefore, the Investigator sensor contains pixels with a variation of these geometric parameters to allow for more detailed study, as shown in in Table 3.1.
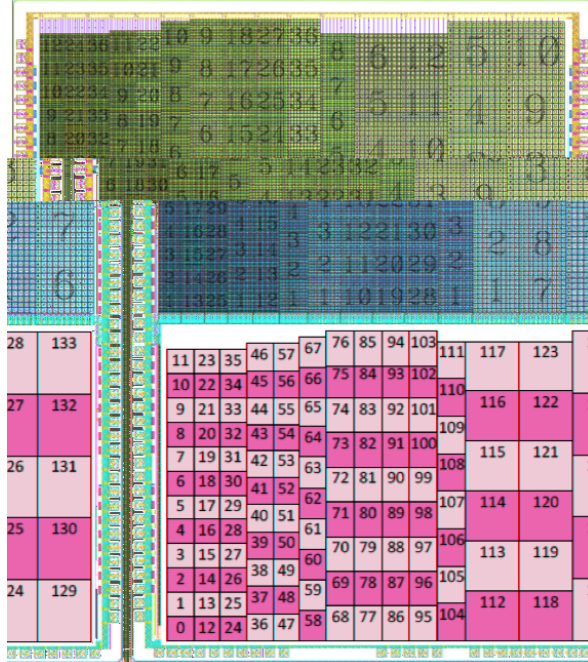
**Figure 3.31:** Investigator Chip Mini-matrices location

| Mini-Matrix id | Pixel size | Number of Mini-matrix |
|:---:|:---:|:---:|
| $0 \rightarrow 35$ | $20 \times 20\ \mu\text{m}^2$ | 36 |
| $36 \rightarrow 57$ | $22 \times 22\ \mu\text{m}^2$ | 22 |
| $58 \rightarrow 67$ | $25 \times 25\ \mu\text{m}^2$ | 10 |
| $68 \rightarrow 103$ | $28 \times 28\ \mu\text{m}^2$ | 36 |
| $104 \rightarrow 111$ | $30 \times 30\ \mu\text{m}^2$ | 8 |
| $112 \rightarrow 123$ | $40 \times 40\ \mu\text{m}^2$ | 12 |
| $124 \rightarrow 133$ | $50 \times 50\ \mu\text{m}^2$ | 10 |

**Table 3.1:** Mini-matrix pixel size

The read-out is based on a 9 bits Encoder designed and implemented by the author. It was designed and implemented for the TowerJazz 180 nm CMOS standard cells [90]. The read-out circuit dimensions are $4464.45 \times 65.50\ \mu\text{m}^2$.

The routing was implemented in six metal layers, where the metal TOP_M, metal M5 and metal M4 are used for power stripes, the

metal M1 and M3 are for horizontal routing and metal M2 for vertical routing, as shown in cyan color in (Figure 3.32).
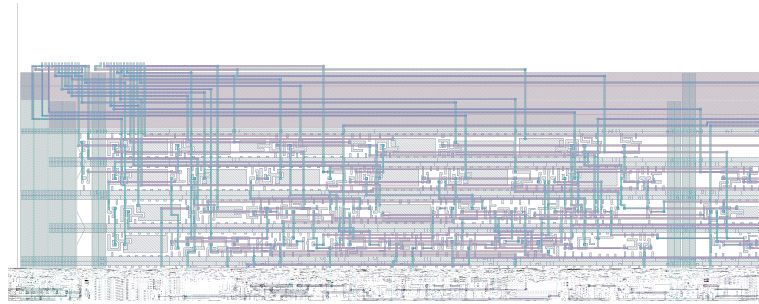


**Figure 3.32:** Part of the layout of the Investigator sensor read-out implemented by the author.

To select one of the 268 mini-matrix, the circuit needs to enable the pixels in the mini-matrix correctly; when the address of the mini-matrix is set, the output buffers present their analog information to the analog output.

### 3.4.1 Experimental results

Measurements have been done at CERN with 5.9 keV X-rays emitted by a $^{55}$Fe source, which generates around 1640 electron-hole pairs. The sensing node voltage signal amplitude is $Q/C_{eff}$, which is collected charge to the sensing node capacitance ratio. This signal is extracted by measuring the output pad signal and applying gain correction with the measured DC voltage transfer function. The signal peak value is extracted with Gaussian function fit on the measured signal spectra.

In case the ionization charge is fully collected by a single pixel, it is possible to estimate the sensing node capacitance from the signal amplitude. If the charge is collected by more than one pixel, the
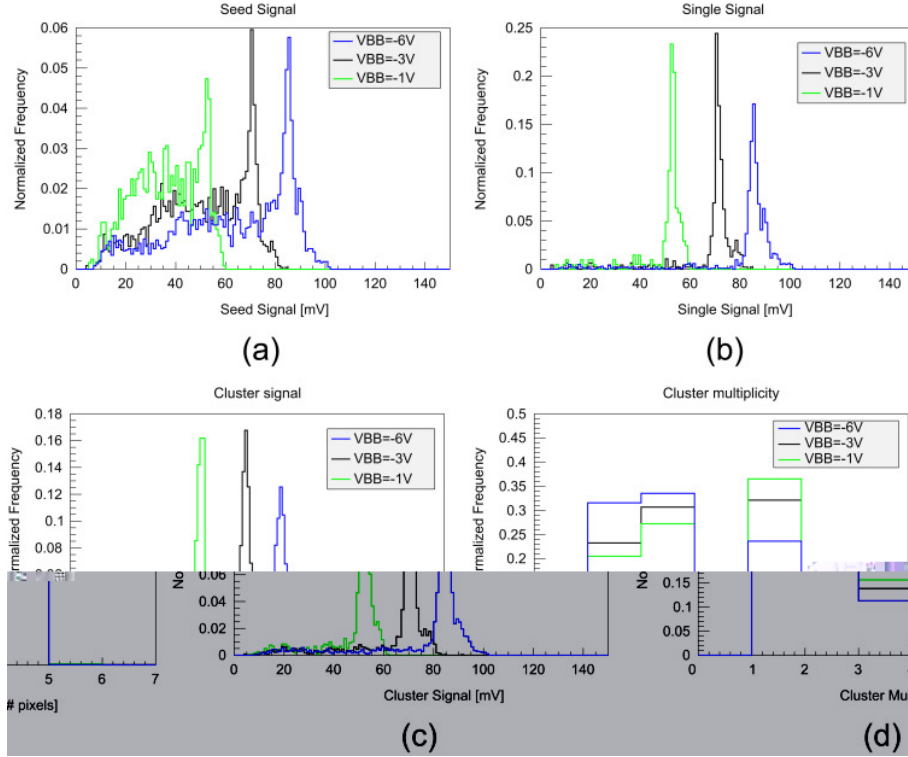
**Figure 3.33:** Source follower signals vary with the substrate back bias voltage $V_{BB}$=-6, $V_{BB}$=-3 and $V_{BB}$=-1: (a) seed signal, (b) single signal, (c) cluster signal and (d) cluster multiplicity.

total signal (cluster signal) is the same as the one of the single pixel signal, but the noise is higher because of uncorrelated noise adding in quadrature. The seed signal is defined as the signal of the pixel with the highest signal in a cluster.

Figure 3.33 shows the source follower circuit signals for different substrate Back Bias Voltage ($V_{BB}$) values; by decreasing $V_{BB}$ from -1 Vdc to -6 Vdc the depletion volume increases, thereby reducing the sensing node capacitance. Using the peak to calibrate, the input capacitance has been estimated as 4.94 fF at -1 Vdc $V_{BB}$ baseline and is reduced by 38% to 3.04 fF at -6 Vdc $V_{BB}$. The noise was measured at about 65 electrons equivalent noise charge (ENC) at baseline and

as a consequence the ENC decreases by 22 % to 51 electrons at -6 Vdc $V_{BB}$.
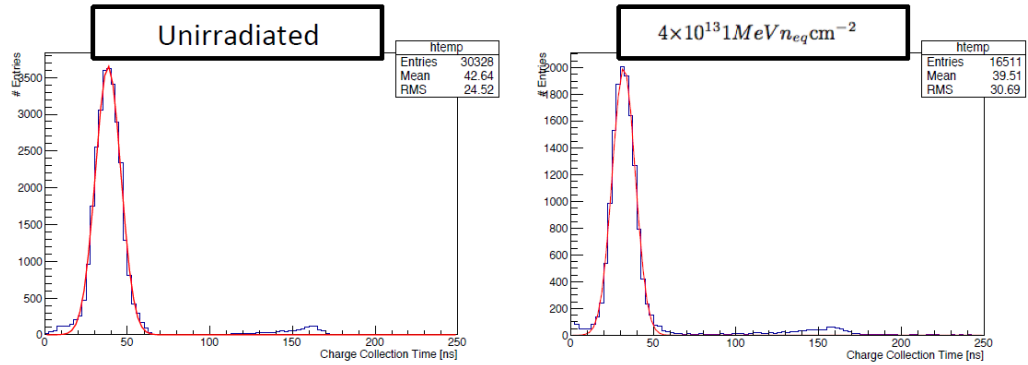


**Figure 3.34:** Before and after neutron irradiation at the TRIGA MarkII Reactor at JSI in Ljubljana using $^{90}$Sr source using a fluence of $4\times10^{13}1MeVn_{eq}$cm$^{-2}$ for 18 $\mu$m epitaxial, 50×50 $\mu$m$^2$ pixel, with $V_{BB}$ -6 Vdc.

The cluster multiplicity decreases by increasing the substrate back bias voltage because of the increase of the drift component in the charge collection.
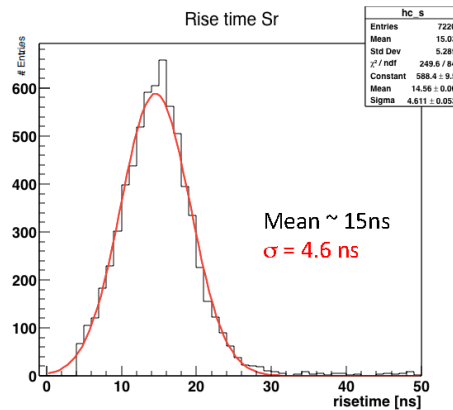


**Figure 3.35:** Signal rise time after neutron irradiation at the TRIGA MarkII Reactor at JSI in Ljubljana using a neutrons $^{90}$Sr source with a fluence of $1\times10^{14}1MeVn_{eq}$cm$^{-2}$ for 25 $\mu$m epitaxial, 50×50 $\mu$m$^2$ pixel, with $V_{BB}$ -6 Vdc.

Figure 3.34 and Figure 3.35 show that the front-end is still working after these radiation doses. The MPV Amplitude in mV reduces slightly

at the same bias voltage. The rise times slightly increase but nevertheless clear signals are observed already -1 Vdc $V_{BB}$ after irradiation from test beam facilities as provided at CERN with energies between 5 - 7 GeV $\pi$.

## 3.5   SEU_TJ180
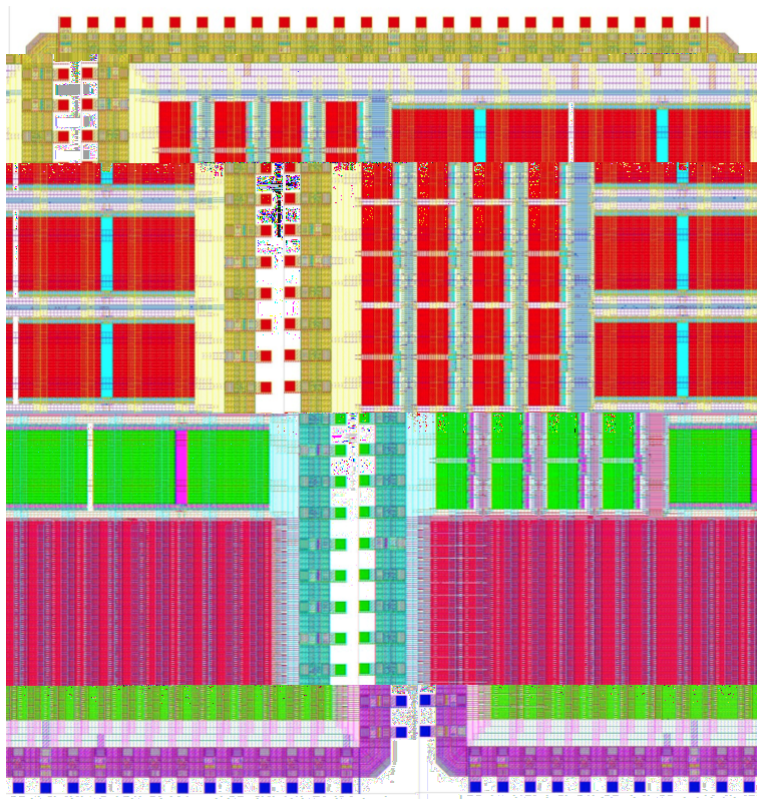


**Figure 3.36:** SEU_TJ180 chip layout and floorplan implemented by the author, at the top left a single port sram, at the top right a dual port ram and bottom sea of flip-flips connected in s-shape creating a shift register.

A Single Event Upset (SEU) is a change of state in memory cells or registers in microelectronic devices caused by ionizing particles. The state change is the result of a charge deposit generated by ionization onto a sensitive node of the circuit. The SEU is a non-destructive effect which does not damage the physical layers of the circuit but

affects the functionality. To analyze this effect a test chip was far-bicated and named SEU_TJ180, designed and implemented by the author. in Figure 3.36 shows the layout in which the components can be identified. :

- SP_RAM block containing an array of 16 single port RAM memories (SPRAM) 1024@16 bits. In Figure 3.36 (top left), we see the placement of a sixteen single-port RAM (SPRAM) and were rotated 90°

- DP_RAM block containing an array of 8 dual port RAM memories (DPRAM) 2048@16 bits, (Figure 3.36) at the top right, the eight DPRAM are visualized.

- 16 bit 2048 stage Shift Register. The 32k FF's are placed in a snake shape, generating a chain per data bit, see Figure 3.36 (bottom).

The SEU_TJ180 chip is interfaced through a digital bus composed of 16 bits input data lines, 15 bits addressing lines, 16 bits output data lines and 7 bits of control lines. The single port memory (SP_RAM) and the dual port memory (DP_RAM) blocks share the same control lines. The SP_RAM, the DP_RAM and the shift register share the input data lines and clock signal.

A digital input bus of 16 bits is shared between the three blocks. The ADDRESS signals for the SP_RAM and DP_RAM memories are common, as well. An 5 bit encoding scheme was used to select each memory. The selection of the memories is based on a multiplexer managed by two bits (see Table 3.2) which is addressed to select the block to be multiplexed to the data output bus among the SP_RAM, the DP_RAM, the shift register and test shift register.

The memories are read out in three different modes **Write Mode**, **Read Data** and **Broadcast Mode** to write all memories at the same time.

A shift register is a chain of D-Enabled, Active-Low flip-flops with Clear and sharing the same clock, in which the output of each flip-flop is connected to the data input of the next flip-flop in the chain. This

| Muxsel | | Output |
|---|---|---|
| b1 | b0 | |
| 0 | 0 | SP_RAM |
| 0 | 1 | DP_RAM |
| 1 | 0 | SR |
| 1 | 1 | SR_TEST |

**Table 3.2:** Blocks data selection output of the SEU_TJ180 chip
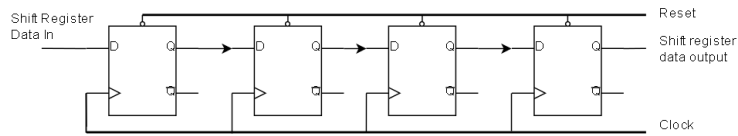


**Figure 3.37:** Basic diagram of the Shift register interconnection

results in a circuit that shifts by one position the bit array stored in it, shifting data in the data present at its input and shifting out the last bit in the array, at each transition of the clock input as is sketched in Figure 3.37.

The Shift Register block has 2048 stages of 16 bits, for a total of 32K bits of memory. From the layout point of view, the flip-flops are connected in an S shape: the output Q of each flip-flop is connected to the input D of the following flip-flop. Given this shape, the Shift Register has a total of 249 columns×144 rows.

To verify the shift register, a test signal SR_TEST is generated. The generation of the test signal happens when MUXSEL is equal to "11". The SR_TEST connects together the 16 bits output once every 128 flip-flops, resulting in a shorted shift register of 16 stages. The idea is to have a fast shifting of the data, for a fast indication of the correct connection of the flip-flops.

### 3.5.1 Single Event Upset measurements

The SEU sensitivity of the TowerJazz technology has been measured in proton beams between 24 and 230 MeV at NPI Prague and PSI and the bit flips were monitored as a function of exposure time and particle flux in Table 3.3 and in Table 3.4 [97].

| TowerJazz cells | Cross Section $\rho_{CS}$ [cm$^2$bit$^{-1}$] | Remark |
|:---:|:---|:---|
| SPRAM | $4\times10^{-14}$cm$^2$ to $8\times10^{-14}$cm$^2$ | Measured |
| DPRAM | $5\times10^{-14}$cm$^2$ to $12\times10^{-14}$cm$^2$ | Measured |
| Shift Register | $3\times10^{-14}$cm$^2$ to $5\times10^{-14}$cm$^2$ | Smallest flip-flop |

**Table 3.3:** TowerJazz SEU cross section measured at NPI and PSI.

| new ITS Layer | TID [MRAD] | 1MeV n$_{eq}$cm$^{-2}$ | # HEH$^a$ ($\gg$ 20 MeV) @ 50 KHz Pb-Pb[$10^3$Hz cm$^{-2}$] |
|:---:|:---:|:---:|:---:|
| L0 | 2.7 | $1.7\times10^{13}$ | $\Phi_I$=770 |
| L3 | 0.1 | $1.0\times10^{12}$ | $\Phi_O$=14 |

$^a$High Energy Hadrons.

**Table 3.4:** SEU Cross Sections and Flux.

The chips were operated in static mode, in which the memories are programmed using 0s, 1s or a checkerboard pattern (alternating 0 and 1) before irradiation starts [57, 61, 98]. The number of accumulated bit flips was monitored every 60 seconds as a function of the proton flux over a total time of 300 seconds. Figure 3.38 shows the SEU cross section as a function of the proton beam energy.

For all type of memories one clearly observes a maximum of the cross section in a proton beam energy region of about 30 MeV to 60 MeV. The SEU cross section for dual port RAMs is about 30% higher than the cross section for single port RAMs and scales roughly with the number of transistors necessary to implement a memory cell (dual port RAM: 8 transistors, single port RAM: 6 transistors).

The SEU cross section for shift registers has been measured at two low proton energies and results in about half the SEU sensitivity of the dual and single port RAM. The SEU cross sections presented here have been used to provide an estimate for the mean error probability
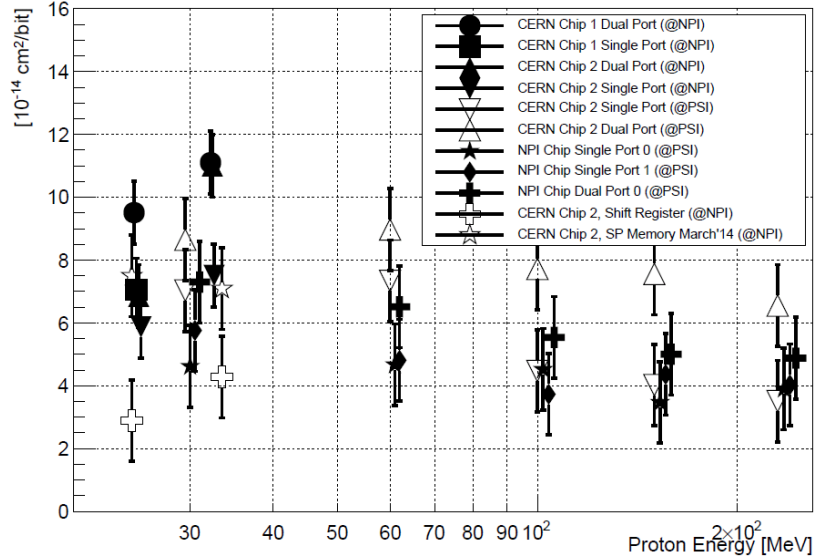
**Figure 3.38:** SEU cross sections as a function of proton beam energy measured for two SEU ASICs in single and dual port mode. For better readability, the values have been slightly displaced horizontally.

per bit of the central sensors that will be most exposed to radiation in the upgraded ITS. With a typical memory depth of N = 2 Mbit and a throughput of $\mu$ = 300 Mbit s$^{-1}$ as well as a total hit density of $\rho$ = 1.6×10$^6$cm$^{-2}$s$^{-1}$ and a SEU cross section of $\sigma$ = 10$^{-13}$cm$^2$bit$^{-1}$, one obtains a mean error probability per bit, $\lambda$, of:

$$BER(95\%CL) = \frac{N}{\mu} \times \rho \times \sigma \approx 1.1 \times 10^{-9} bit^{-1} \qquad (3.8)$$

which is a tolerable induced data corruption rate (BER = Bit Error Rate), under the operational conditions of the ALICE ITS Upgrade. In contrast to errors in the data stream, any error in the configuration logic is persistent until the configuration is updated. SEUs in the control logic of the chip can lead to electrical errors on the bus and even physical damage. Even though the SEU error probability for the configuration logic is relatively small, these parts of the chip will be protected by a redundant, radiation-hardened design.

$$\rho_{CS} = \sigma \ \times \ \Phi_I$$
$$\rho_{CS} = 3 \ \times \ 10^{-14} cm^2 bit^{-1} \ \times \ 7.70 \times 10^5 \ s^{-1} \ cm^{-2} \qquad (3.9)$$
$$\rho_{CS} = 2.31 \times 10^{-6} \ s^{-1} \ bit^{-1}$$

With a SEU cross section of about $\sigma = 3{\times}10^{-14}$cm$^2$bit$^{-1}$, a number of shift registers per chip of about r = 1200 and a maximal total hit density of $\rho_{CS} = 2.31{\times}10^{-6}$s$^{-1}$bit$^{-1}$ one would expect a mean time interval between two SEU events per chip of:

$$\triangle t = \frac{1}{r \times \rho_{CS} \times \sigma} \approx 10000s \approx 2.8 hours \qquad (3.10)$$

Bonacini et. al. in reference [98] have studied SEUs in 65 nm and 90 nm CMOS technologies. It has been concluded that the probability of a SEU in a single device decreases as transistor size is decreased. Although smaller devices have lower capacitance, the probability of hitting a sensitive node in the device is also smaller. On the other hand, the number of devices on a single chip also increases, so the probability of the SEUs across the whole system does not decrease or increase significantly due to CMOS scaling. Since the data logic stored in the shift registers is updated regularly every few clock cycles, SEU effects are thus expected to be negligible. But the results in Equation 3.10 shows that almost in 10k seconds a SEU will be present in the logic of TowerJazz memories. Design techniques such as triple modular redundancy (TMR) and error correction coding (ECC) can be implemented to make circuits more tolerant to SEU. As described earlier, TMR is based on triplicated logic in which the correct result is determined based on a vote of the three outputs. ECC such as Hamming coding can also be used to correct single event upsets or even to detect multiple bit upsets. In conclusion, TRM techniques including ECC should be implemented in sensitive registers and especially in state machines, making the circuit more robust.

### 3.5.1.1 Single Event Latch-up measurements

A Single Event Latch-up (SEL) is a type of short-circuit which can occur in CMOS circuits and is typically caused by heavy ions or protons from cosmic rays or solar flares. It results in the creation of a low impedance path between the power supply rails of these circuits, triggering a parasitic structure which disrupts proper functioning of the component, possibly even leading to its destruction due to overcurrent [58]. The parasitic structure is usually equivalent to a thyristor, a PNPN structure which acts as a PNP and an NPN transistor stacked next to each other. During a latch-up when one of the transistors is conducting, the other one begins conducting too. They both keep each other in conduction for as long as the structure is forward-biased and some current flows through it which usually means until a power-down.

| Ion | Energy [MeV] | Range[$\mu$m(Si)] | LET[MeVcm$^{-2}$mg$^{-1}$] |
|---|---|---|---|
| $^{13}$C$^{4+}$ | 131 | 269.3 | 1.3 |
| $^{14}$N$^{4+}$ | 122 | 170.8 | 1.9 |
| $^{22}$Ne$^{7+}$ | 238 | 202 | 3.3 |
| $^{40}$Ar$^{12+}$ | 379 | 120.5 | 10 |
| $^{58}$Ni$^{18+}$ | 582 | 100.5 | 20.4 |
| $^{84}$Kr$^{25+}$ | 769 | 94.2 | 32.4 |
| $^{124}$Xe$^{25+}$ | 995 | 73.1 | 62.5 |
| $^{15}$N$^{3+}$ | 62 | 60.4 | 3.2 |
| $^{20}$Ne$^{4+}$ | 80.5 | 46.3 | 6.1 |
| $^{40}$Ar$^{4+}$ | 155 | 41.1 | 15.1 |
| $^{84}$Kr$^{17+}$ | 324 | 41.1 | 40 |
| $^{124}$Xe$^{25+}$ | 461 | 38.5 | 69.2 |

**Table 3.5:** Available particles inside the cocktail at CyClotron of LOuvain la NEuve (CYCLONE2) [99].

A separate read-out system was used to study the sensitivity of the SEU_TJ180 chip with regard to SEL. The currents of the four different power domains of the SEU_TJ180 chip were monitored with regard to adjustable thresholds. With a current consumption of the SEU_TJ180 chip of about 25 mA, the occurrence of SEL was signaled when a current exceeded a threshold of 50 mA. SEL cross sections were measured using heavy ions from CyClotron of LOuvain la NEuve (CYCLONE2) in Belgium, a multi-particle and variable energy cyclotron providing two ion "cocktails" of various range domains, as is shown

in Table 3.5. Ions are provided with a variable flux of between a few particles cm$^{-2}$s up to about $10^4$ cm$^{-2}$s with energies up to 75 MeV. The beam flux can be modified from the user station; this is done with injection grids (for a constant attenuation factor) or by inflector bias on a variations (for intermediate values). The Homogeneity is $\pm$ 10% on 25 mm diameter. The test setup was installed in a vacuum vessel.

The SEL measurements were started with the highest flux and LET in order to maximize the occurrence of latch-up. The latch-up currents for the test device were measured to be of the order of a few tens of mA. After each SEL detection, the chip was switched off within 1 ms in order to avoid the destruction of the chip by high currents. After 1 s the chip was switched on again.
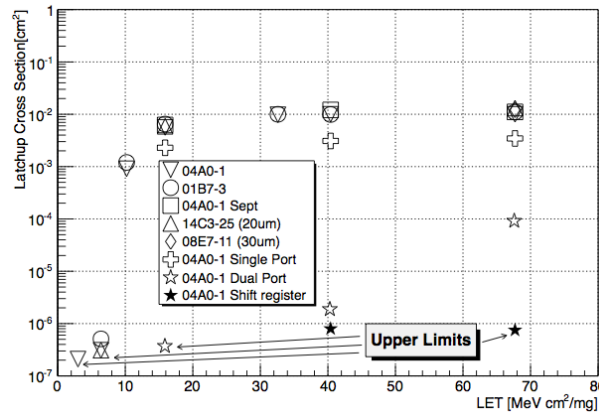


**Figure 3.39:** Latchup cross section as a function of the LET measured for various SEU_TJ180 chips and various memory types. Some markers are upper limit values as no latchup occurred over the measurement period.

Figure 3.39 summarizes the result of measurements carried throughout the summer of 2014. To assess the overall SEL sensitivity of the memory structures used in the TowerJazz 180 nm CMOS imaging sensor process, the latch-up cross section was measured as a function of the ion LET for two SEU_TJ180 chips of different epitaxial layer thickness and resistivity (18 $\mu$m and 12 $\mu$m and 1 k$\Omega$cm$^{-1}$ and 30 k$\Omega$cm$^{-1}$ respectively). Latch-up events were observed as from a LET of 6.4 MeV cm$^{-2}$mg$^{-1}$. Both types of SEU_TJ180 chips show identical cross sections, saturating for LET values above 32.6 MeVcm$^{-2}$mg$^{-1}$.

The latch-up sensitivity has also been measured separately for the various memory types used in the SEU_TJ180 chips by using small collimator in order to irradiate selected memory regions only. Figure 3.39 shows the latch-up cross section for an irradiated area of about one third of the single port memory surface (04A0-1 Single Port), resulting in about a third of the total cross section for the entire chip. On the other hand, the latch-up cross sections measured for dual port memory and shift registers, shown in Figure 3.39 as 04A0-1 Dual Port and 04A0-1 Shift Register respectively, exhibit at least three orders of magnitude smaller SEL sensitivity for high LET values. In particular for LET values below the maximum LET value of 15 MeV $cm^{-2}mg^{-1}$ expected for the LHC, no latch-up events were observed over the duration of the measurement and the indicated cross sections are thus upper limits. The results consequently indicate that in the SEU_TJ180 chip only the single port memory is latch-up sensitive and the flipflops and dual port memory aren't latch-up sensitive.

## 3.6 Conclusions and overview

The new ALICE Inner Tracking System, to be installed in 2018-2019, will be entirely based on monolithic pixel detectors to be able to record PbPb collisions at 50 kHz and proton-proton up to 1 MHz collision rates with improved vertexing capabilities. Several prototypes have been already fabricated with the TowerJazz 180 nm CMOS technology.

Chips of the Explorer family, fabricated in different variants and implemented on different substrates, have been tested in terms of charge collection efficiency, noise and charge detection efficiency, both with radioactive source and beams of charged particles. The results obtained fully support the chosen approach, and an efficient layout of the collecting diode has been identified.

Another prototype, the pALPIDEss, has also been fabricated with a matrix of pixels read with a sparsified read-out based on a priority address encoding scheme for the pixel address that also acts as a reset forward circuitry for the selected pixel to be read-out. Measurements on this prototype have studied applying a digital pulse to some of the

pixels inside the matrix, and the encoding circuitry for the address has been validated.

A small prototype of the ORTHOPIX chip has been designed and manufactured in the TowerJazz 180 nm CMOS technology. This solution is an alternative read-out architecture compared to the traditional rolling-shutter or token-ring architectures in particle detectors, which performs real-time data compression at greatly reduced power consumption and with a minimal layout footprint. This prototype isn't fully characterized, and it demonstrates how this architecture could offer an effective solution for applications, like tracking and very low occupancy imaging, where small pixel pitch, extremely fast frame rate and low material budget are required.

The Investigator chip provides the opportunity to study and characterize TowerJazz 180 nm technology beyond the ALICE requirements. Currently the ATLAS pixel community has started to analyze the circuit up to levels of $10^{16}$ 1 MeV $n_{eq}$cm$^{-2}$ and the results of these new studies will determine the route-map of the MAPS for a vertex sensor.

The characterization of the SEU of the TJ_180 gave the opportunity to identify how tolerant this technology is to be implemented in a radiation environment, in particular for the memories and flip-flops.

The result of this characterization showed that mitigation of SEU effects is necessary, in particular, in the configuration registers. This can be done using triple modular redundancy (TMR) with error correction coding (ECC), resulting in some penalty in power and area.

The author was responsible for the design of the digital part of all these circuits, including simulation, layout implementation, and post-layout verification.

Furthermore, the author's research is concentrated on the PADRE circuit. All these circuits contributed to early phases of the upgrade project to define and characterize key aspects of the technology and the design blocks critical for the implementation of a full scale sensor chip for the ITS upgrade in the TowerJazz 180 nm technology, further described in the next chapter.

All small prototypes presented in this chapter made the author understand how to design a monolithic ASIC, from the conceptual design, implementation and integration of analog and digital circuits, to the finalization with the fabrication and production phase.

# Chapter 4

# New full scale developments for the ALICE PIXEL DETECTOR

This thesis is focused on the design of the novel digital pixel read-out architecture for Monolithic Active Pixel Sensor for the new ALICE Inner Tracking System based on TowerJazz 180 nm technology described earlier.

In this chapter the ALPIDE architecture is described. It is based on the PADRE circuit described in the previous chapter. The pixel read-out for the pALPIDE3 prototype and its twin the pALPIDE3B prototype are presented, along with a description of its full scale predecessors, the pALPIDEfs and the pALPIDE2 prototypes. The pALPIDE3 chip is a Pixel Detector Chip developed by a collaboration formed by CCNU (Central China Normal University in Wuhan, China), CERN, INFN (L'Istituto Nazionale di Fisica Nucleare branch Cagliari and Torino in Italy), Yonsei (South Korea), CEA/IRFU (Centre d'etude de Saclay Gif-sur-Yvette in France), MIND (France), IPHC Institut Pluridisciplinaire Hubert CURIEN (France) and NIKHEF (The Netherlands). The pALPIDE3 chip is a particle detector based on Monolithic Active Pixels Sensor and the sensor is implemented in TowerJazz 180 nm CMOS technology. Several prototypes have already been designed, submitted for fabrication, and some of them have been tested with X-ray, $^{55}$Fe and $^{90}$Sr sources and charged particle beams.

The ALPIDE development is an alternative to a rolling-shutter architecture, and aims to reduce power consumption and integration time by an order of magnitude below the ITS upgrade specifications [31] summarized in Table 1.5.

This would be quite beneficial in terms of material budget and background. The approach is based on a binary analog front-end combined with a hit-driven architecture.

The hierarchy sparsified read-out architecture is a double column with 1024 pixels and hence a 10 bit address bus. This architecture follows an approach where the chip matrix is subdivided into a set of small hierarchies. In each hierarchy, a priority is implemented which allows to read-out the address of the fired pixel and then subsequently reset it. The processing in each hierarchy is carried out in parallel. All priority encoders of the full matrix are connected to the end-of-column electronics. This architecture allows to a real sparsified read-out in every hierarchy, which features a read-out time that scales with the track multiplicity.

An important constraint for the design of the circuitry in the matrix, so both for analog front-end and digital circuitry, is that pads to connect the chip to a flex circuit need to be implemented over the matrix. These require 2 level of metals, limiting the circuitry under the pads to only 4 metal layers, hence severely constrain routing capability for the digital circuitry.

Another constraint on the digital part is the requirement to be robust against single event effects (but this is not required for the data in the matrix itself).

## 4.1 The ALPIDE family

The chip is surrounded by a $p^+$ seal ring to limit leakage and to prevent breakdown effects at the boundary. To shield the sensitive area from the rest of the circuitry, a $n^+$ ring was designed all around the matrix detector, which allows for the collection of the charge that diffuses or leaves the sensitive area (see Figure 4.1).
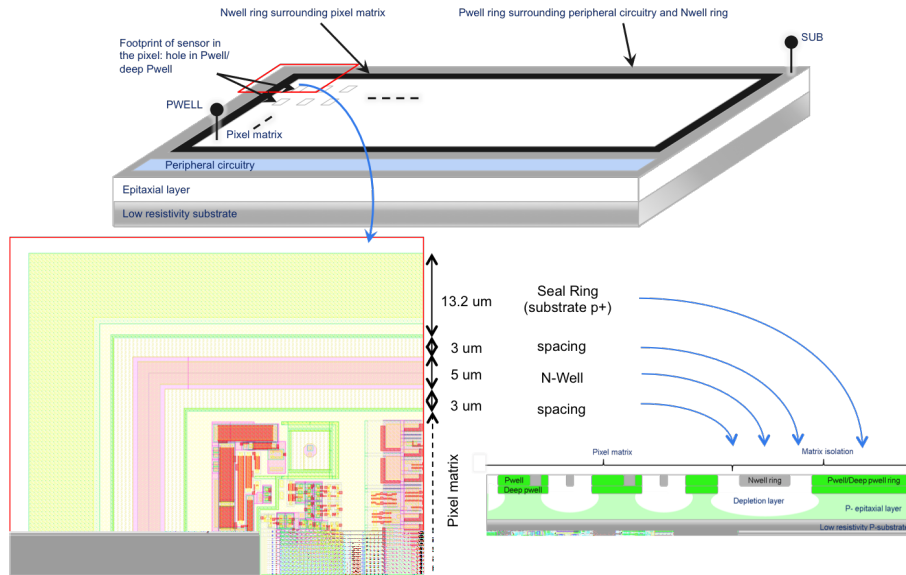
**Figure 4.1:** Schematic illustration of the $p^+$ seal ring isolation around the matrix active area and the application of the reverse substrate bias in the ALPIDE design.

The deep-pWELL is implanted everywhere in the sensitive area but below the collection diodes (not only beneath pMOS nWELLs). The design exploits all the 6 metal layers provided by the technology, but to provide proper power distribution, the last two metal layers are mainly used for power routing mesh. At the same time several Pads Over Logic (POL) are placed over the sensitive area of the chip. To reduce coupling between the analog and the digital circuitry of the chip, which coexist up to the pixel level due to the architecture, the analog and digital power domains are kept separate. A third domain is used to power the 20 CMOS compatible pads at the edge of the sensor. All the three power domains operate at the same supply voltage (1.8 V). Eleven 256-step DACs (full analog block) that can be configured through the digital periphery, provide bias (6 voltage levels and 6 current levels) to the active area. The reference voltage to the DACs is generated externally and provided through a dedicated pad (VREF, 1.8 Vdc) positioned at the edge of the sensor (no bandgap reference) [100].

The ALPIDE family contains a novel low-power in-pixel discriminator circuit [101, 102] that drives an in-matrix asynchronous address encoder circuit, read-out by an end of column lossless data compression and de-randomizing circuit. The digitization of the signal in-column address encoder (zero suppression data driven architecture) within the pixel eliminates the need for an analogue column driver, reduces the power consumption significantly and allows for fast read-out, only the hit pixels are read-out, because only the fired pixels are read-out. The front end generates a logic 1 when it receives a particle hit which deposits a signal charge above threshold.
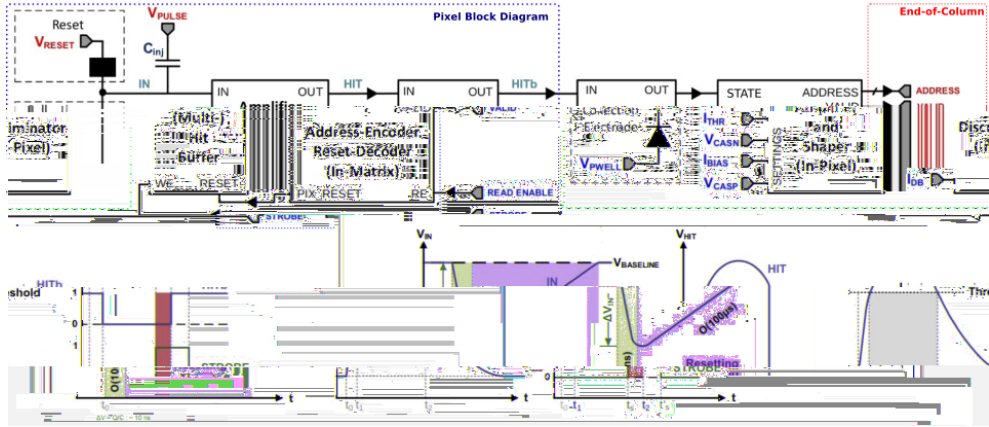


**Figure 4.2:** pALPIDE3 sensor front-end principle of operation.

Figure 4.2 at top shows the principle of operation of the front-end and interface to the front-end read-out. The charge signal is integrated at the input node IN with a typical collection time of approximatly 10 ns. The IN voltage signal amplitude is equal to the ratio of the collected charge $Q_{IN}$ to the total input capacitance $C_{IN}$. The bottom part shows the operation principle when a charge particle hit the pixels. The reset circuit restores the input baseline voltage level within a time around 1 ms. It also provides compensation for the sensor leakage current which is expected to be below 2 pA. The signal is amplified by the front-end, which acts as a delay line with a peaking time of around 2 $\mu$s. The discriminated output HITb is put in coincidence with the STROBE signal, allowing the latching of the hit information in the

multi event buffer memory. The data are read out by a hit-driven architecture that has activity only when there are stored hits [102].
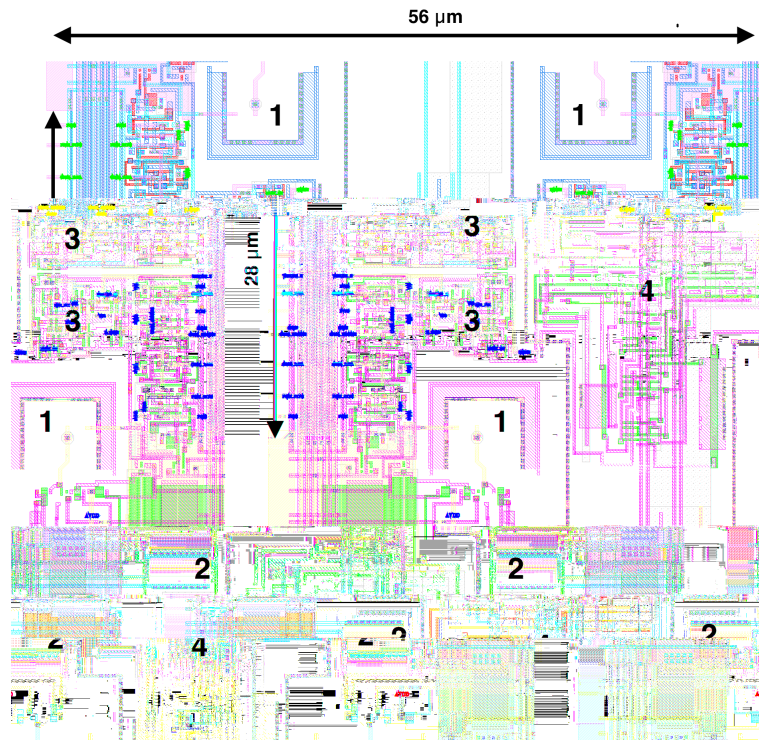


**Figure 4.3:** pALPIDEfs sensor and pALPIDE2 sensor with four front-end and one full custom front-end read-out layout. The pixel layout components are: 1. collection electrode, 2. preAmplifier & discriminator, 3. digital custom storage element, 4. AERD full custom logic Front-end read-out.

The pALPIDEfs chip represents the first full-scale prototype within the ALPIDE development. It contains the novel low-power front-end and the sparsified read-out architecture characteristic for the ALPIDE design [73, 89, 101].

The change of pixel size compared to the pALPIDEss prototypes is driven by the need for more space for in-pixel circuitry. For testing purposes a masking register per pixel was added to disable noisy pixels, together with a single in-pixel hit buffer instead of a capacitor. The pALPIDE2 chip is the second full-scale prototype with all of the

pALPIDEfs chip features and more. It will be briefly explained in this section. Figure 4.3 shows the front-end interconnection to its full custom read-out for the pALPIDEfs sensor and the pALPIDE2 sensor.

The pALPIDEfs and the pALPIDE2 prototypes [104, 105, 106] consist of 524288 pixels, of size 28 $\mu$m × 28 $\mu$m and arranged in 512 rows times 1024 columns, for a total active area of 28.7 mm × 14.3 mm. The total die size is 30 mm × 15.3 mm$^2$, and the height of the periphery, positioned at the edge of the die, is 1 mm. The height of this prototype slightly exceeds the requirements in given Table 1.5 where the height is set to 1.53 cm. The power pads were oriented according to the ITS upgrade assembly working package. Due to layout constraints, each pair of pixel columns (double column) is connected to an array in-matrix full custom digital circuit, called AERD [104, 106] (Address- Encoder Reset-Decoder). A low-speed data and control pads were designed for the CHIP read-out. On other hand, the pALPIDE2 chip had the same size and front-end read-out of its predecessor the pALPIDEfs. 7 pads for the Chip identification (CHIPID) were added for addressing schema and identification of the chip according to the 2 scenarios IB and OB. Furthermore, a low speed DDR data port for communications was implemented due to the fact that the high speed serializer was not finished on time. The power pads were reoriented according to the ITS upgrade assembly working package and the CHIPID pads in the stave module assembly; these pads will be soldered to a flexcable.

The AERD circuit is full custom design based on the PADRE circuit encoding scheme. The difference lies in the address bus propagation; in the case of PADRE this is based on a chain of OR logic between hierarchy levels, but for the AERD this is based on a tri-state buffer chain.

The pALPIDEfs chip had a failure in the power managementdue to an error in the memory control; they were not deactivated when not in used resulting in a waste of 200 mW (314 mW instead of 114 mW).

The dynamic power analysis is part of the behaviour of the chip. Figure 4.4 shows the pALPIDE2 tested in different configuration modes according to the quantity of pixels pulsed to be read-out. The plot

shows the transient current when some regions are fired. In the case of fired regions, the current peak at 1000 $\mu$s is proportional to the quantity of fired pixels. The second current peak at 4000 $\mu$s is not fully understood.

One possible explanation is due to unbuffered global signals with a high RC factor. The second peak could be the result if the tri-state buffer switching activity on the AERD circuit.The second peak is due to some lines being driven by tri-state buffers which draw extra current and result in higher power consumption in the readout logic.
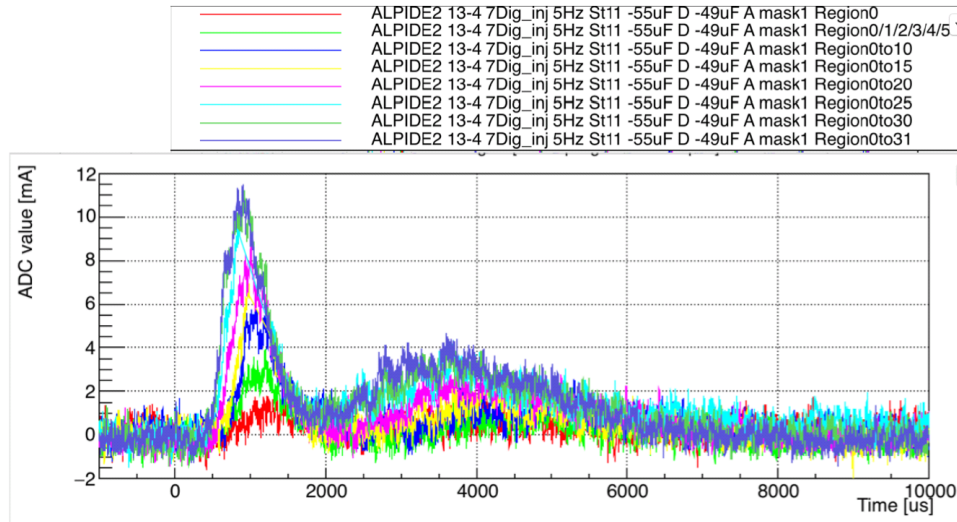


**Figure 4.4:** pALPIDE2 chip dynamic power analysis.

Figure 4.5 shows the concordance between the quantity of fired pixels and the current consumption. This confirms the hypothesis that the tri-state buffers inside the AERD circuit cause the extra power consumption. In this case a few sectors and priority encoders were triggered; the colour yellow represents 191 priority encoders in 30 regions and the colour red represents 93 priority encoders with 7 regions. The second peak at $\approx$ 4000 $\mu$s and the low transient are due to the RC factor when the signals of tri-state buffers are not driving current and and return to a metastable state. To reduce this extra power consumption, the tri-state data bus transmission in the matrix read-out

must be replaced and different ways of low power data transition from the fired pixel to the periphery.



| Priority Encoders | | Regions | |
|---|---|---|---|
| Yellow 191 | | Pink 30 | |
| Pink 189 | | Blue 30 | |
| Blue 167 | | Red 29 | |
| Green 105 | | Yellow 15 | |
| Red 93 | | Green 7 | |
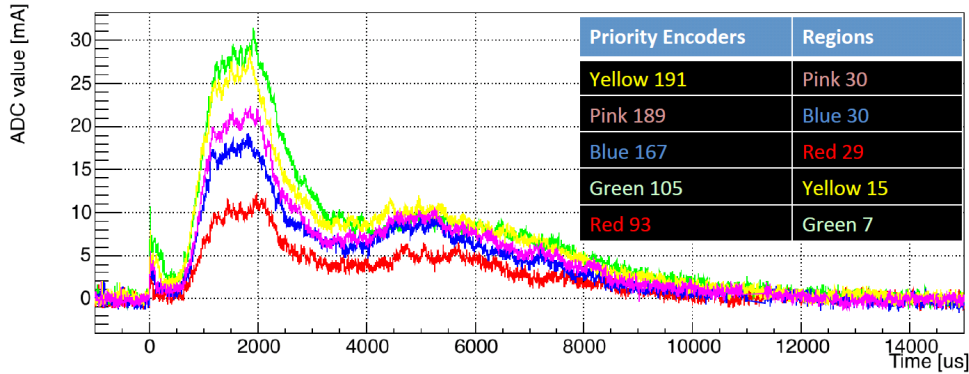
**Figure 4.5:** pALPIDE2 chip dynamic power analysis pulsing different regions.

A shared data bus is a commonly used architecture for transferring data. The tri-state bus is not the best solution for the pALPIDE2 prototype. One possible solution is the implementation of the pALPIDEss prototype that relies on a multiplexer-based and AND-OR-based bus. Each bus has a number of hierarchies who initiate bus transactions and slaves which respond to these transactions. In pixel read-out chips the buses are typically routed from the top of the columns to the bottom [66, 67, 107, 108, 109]. In MAPS the read-out buses are implemented next to the front-end underlying the pixel; these buses cover almost the full distance of the chip. On the other hand, these buses are uni-directional, having multiple repeaters to decrease the RC and the propagation delay up to the end of column.

## 4.2 pALPIDE3

The pALPIDE3 prototype (see Figure 4.6) is one of several chips implemented in the context of the microelectronics R&D process, towards the design of a final ALPIDE chip that will target all the requirements of the ALICE ITS Upgrade. The pALPIDE3 chip is a third step on a path intended to address the system aspects related to the integration of a large scale ($3 \times 1.5$ cm$^2$) MAPS chip and to the physical and electrical interconnection of such a chip on flex printed circuits.
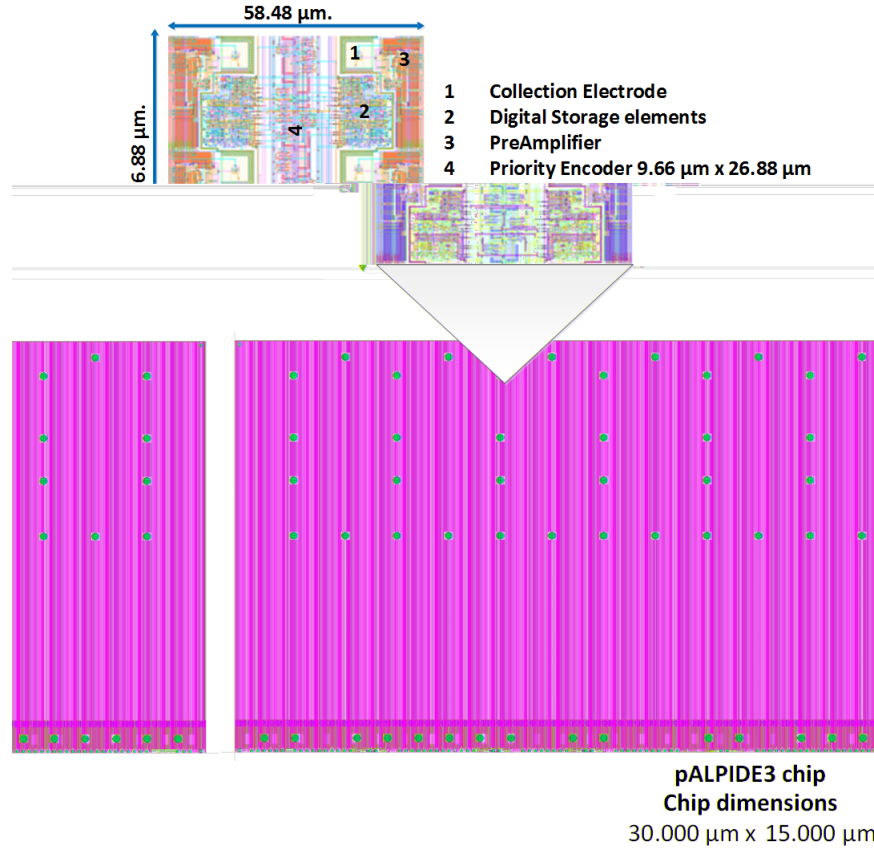
**Figure 4.6:** ALPIDE3 chip layout assembled by the author using Encounter CAE tool. The shows the pALPIDE3 pixel layout components: 1. the collection electrode, 2. the digital storage element, 3. the preAmplifier & discriminator, 4. the Priority Encoder.

With respect to its immediate predecessors (the pALPIDEfs chip and the pALPIDE2 chip), the pALPIDE3 prototype meets most of the requirements of the ALICE ITS Upgrade. The pALPIDE3 chip sensitive matrix is composed of eight variants of pixels, for continuing optimization of the pixel analog circuits.

The chip's feature size is 15 mm (Y) by 30 mm (X) and contains a matrix of $512 \times 1024$ sensitive pixels. The pixels are $29.24 \ \mu m \times 26.88 \ \mu m$ (X×Y). A periphery circuit region of $1.2 \times 30 \ mm^2$ including the readout and control functionalities is present. It is assumed that the chip

is observed from the circuits side and oriented such that the periphery is on the bottom. The pixel columns are numbered from 0 to 1023, going from left to right. Pixel rows are numbered from 0 to 511, going from the matrix top side to the bottom one.

Figure 4.7 shows at the top the front-end of the pALPIDE3 sensor, and at the bottom the simulation of the front-end to different input charges at nominal bias: the voltage at the HIT node is presented as a function of time after a charge injection (at t = 1 $\mu$s) at the sensing node. The response is non-linear, with a decreasing peaking time with increasing signal amplitude. The minimal detectable charge has been measured to be about 130 electrons, at nominal bias and threshold setting.
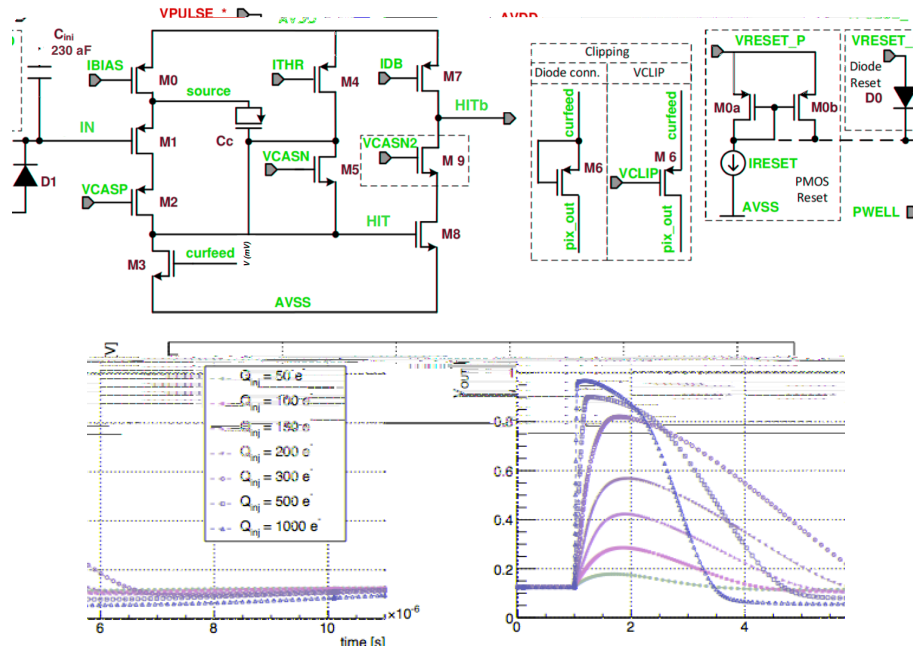


**Figure 4.7:** At top pALPIDE3 pixel schematic and at bottom the front-end simulation of response to different input charges.

There are eight sub-matrices of 512×128 pixels; each one is composed of identical pixels and the same read-out functionally. They differ for specific parameters of the charge collection diode and of the analog front-end circuits. Each pixel variant features an ultra-low power,

non-linear front-end with shaping and discriminated output. The pixel sensor and front-end are always active. The front-end acts as a delay line: upon a particle hit, it generates a pulse with a duration of a few microseconds. A threshold is applied to form a binary pulse. A hit is latched into one of the three in-pixel memory cells if one of the three STROBE and MEMSEL signals are applied to the corresponding cell while the aforementioned binary pulse is asserted. The assertion of STROBE signals to the pixels during the response interval following an event of charge release in the sensing diode causes the latching of the discriminated output into one of three storage cells in the digital section of the pixel. The pixels feature a built-in test pulse injection circuit trigger-able on command based on an XY access scheme. A digital-only test pulse mode is also available, forcing the writing of a logic one in the selected in-pixel memory cell. The STROBE and MEMSEL signals are generated at the periphery and applied simultaneously to all pixels. The logic generating the STROBE signal is configurable according to different operating modes, and the duration of the STROBE signals is also programmable. The generation of STROBE signals is typically triggered by an externally applied trigger command.
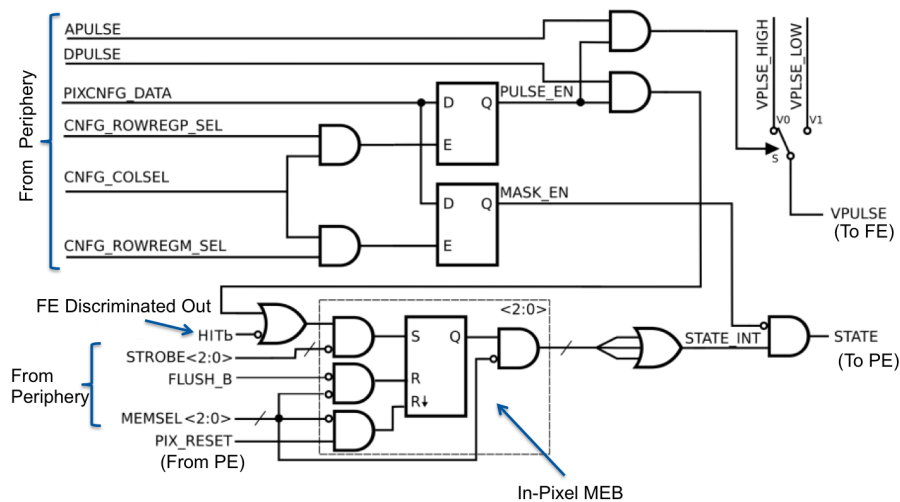


**Figure 4.8:** pALPIDE3 IN pixel register.

The hits stored in the three pALPIDE3 IN pixels multi-event buffers are read out by means of Priority Encoder circuits, as shown in Figure 4.8. These provide the address of a pixel with a stored hit based on a hard-wired topological priority. During one hit transfer cycle a pixel of one of the three multi-event buffers with a hit is selected, its address generated and transmitted to the periphery and, finally, the in-pixel memory element is reset. This cycle is repeated until all hits at the inputs of the Priority Encoder are read out. The read-out of the sensitive matrix to the periphery is therefore zero-suppressed and hit-driven. Processing time and energy are consumed proportionally to the number of hits at the inputs of the Priority Encoder.

The read-out of the matrix is organized in 32 regions (512×32 pixels), each of them with 16 double columns being read-out by 16 Priority Encoder circuits, as is the case for the predecessors, the pALPIDEfs chip and the pALPIDE2 chip. The hits inside one region are read-out sequentially in consecutive read-out cycles.

The process of read-out of the 32 regions is executed in parallel. This is driven by state machines in the Region Read-out Unit blocks. The Region Read-out Units also contain multi-event storage memories and data compression functionality based on clustering by adjacency. The data from the 32 Region Read-out Blocks are assembled and formatted by a chip level Top Read-out Unit.

Hit data can be transmitted on two different data interfaces according to one of three alternative operating modes envisaged for the Upgraded ALICE ITS: *Inner Barrel Module chip*, *Outer Barrel Module Master*,*Outer Barrel Module Slave*. A 1.2 Gb/s serial port *HSDATA* with differential signalling is intended to be the primary data read-out interface for the Inner Barrel Module chips [110]. The same interface is intended to be used for the transmission of data off-detector by the Outer Barrel Module Master chips. These also collect the data of a set of neighbouring Outer Barrel Module Slave chips and forward their data off-detector on a common differential link.

A parallel output data port using CMOS signalling is also present. It enables the implementation of the data exchange between the Outer Barrel Module Slave chips and the corresponding Master. All the

functionalities related to the Outer Barrel Module bus arbitration, data encoding and data transmission are implemented by a dedicated Data Management Unit.

### 4.2.1   Read-out design and implementation
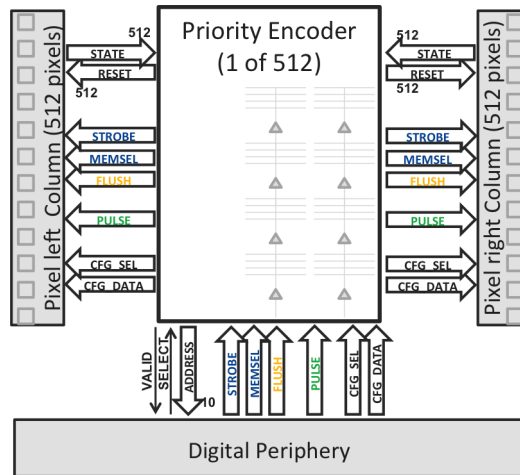


**Figure 4.9:** The pALPIDE3 priority encoder is interfaced to 2 columns of 512 pixels and one End-Of-Column.

The pALPIDE3 priority encoder circuit provides the read-out from the pixel to the periphery (see Figure 4.9). The main process was described in section 3.2. Inside of the pALPIDE3 priority encoder the global signals are buffered. The signals that configure a write into pixel registers are also routed through the pALPIDE3 priority encoder circuit, which also buffers the pixel configuration signals.

The encoding process is based on the pALPIDEss PADRE circuit described in subsection 3.2.1, the pALPIDE3 padre circuit is organized as a tree with 5 levels of hierarchy.

The pALPIDE3 priority encoder implementation is based on the pALPIDEss PADRE circuit cited in subsection 3.2.3. The pALPIDE3 priority encoder circuit includes 2 ROWS of STD CELLS and four metal layers. For the full height of the column plus additional routing space on left and right, a total width of 19.6 $\mu$m is required, as seen in Figure 4.10.
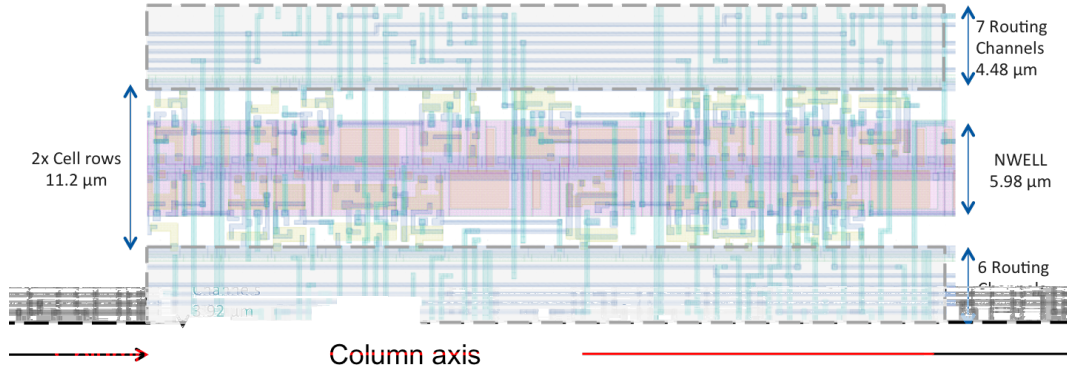
**Figure 4.10:** The pALPIDE3 priority encoder implementation by the author using the Encounder CAE tool.
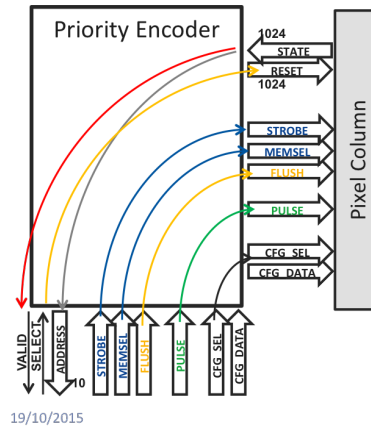


**Figure 4.11:** Propagation of representative timing arcs in the Priority Encoder.

The pALPIDE3 priority encoder circuit is fully simulated at block level with back annotation delays( see Figure 3.26). The timing diagram shows the example of 5 cycles of address encoding and pixel resetting. First the STROBE is applied to the pixel and the MEMORY bank is selected. At this moment the input STATE vector changes, and the PE encodes the address of the first pixel. The Periphery samples the address and toggles the SELECT that is propagated to the first pixel as RESET. The pixel state is reset and the PE encodes the next fired pixel. The read-out cycle is repeated until there are no more hits and the VALID signal is deasserted.
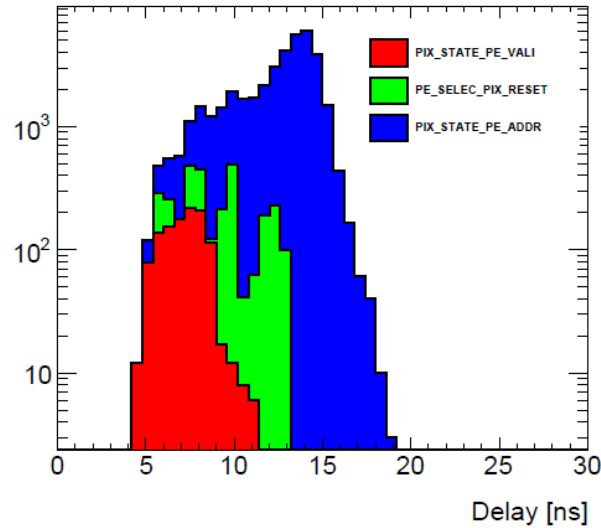
**Figure 4.12:** Propagation delays of representative timing arcs extracted by the author.

The circuit has been fully characterized for timing arcs by the author. A timing arc defines the propagation of signals through logic gates/nets. This timing information is used to define the timing propagation at the periphery level. The major timing arcs are illustrated in Figure 4.11, where the propagation delays are given for the worst case: for the lowest power supply voltage (1.62 Vdc) and the highest expected temperature (125°C). For the read-out, the crucial timing paths are from STATE to ADDRESS and from SELECT to the RE-SET of the pixel, as can be seen in Figure 4.12. The sum of this two delays defines the minimum duration of a hit transfer cycle, that is one clock cycles of 25 ns. In conclusion, the read-out circuit can operate within 25 ns for the worst corner of operating parameters. This worst corner condition is out of scope in the ITS upgrade program but it is needed for the top-down flow timing propagation constraints.

### 4.2.2 Chip assembly

The Chip assembly is made by the author with a top-down flow as described earlier. The Matrix sensitive area is made by the placement of the 512 Double Columns and their corresponding PEs next to them the connections between PEs and Double Columns are by abutting (see Figure 4.13). The Pads over logic and alignment markers are placed. After the placement the power meshes and the pixel configuration control wires are routed.
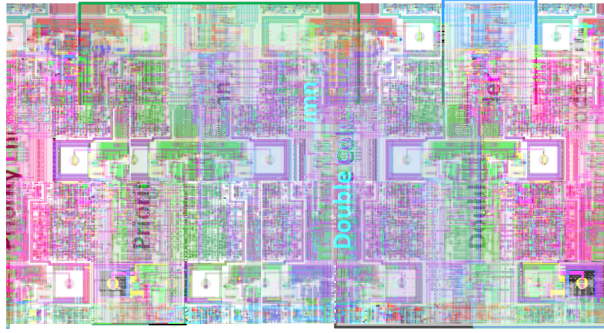


**Figure 4.13:** Matrix block implemented by the author with digital flow.

The pALPIDE3 priority encoder presents at the periphery level the address of the fired pixels, but the pixel are arranged in a special way according to the pins placement. The mapping is illustrated in Figure 4.14. On the top of the figure we see the column number and the quantity of priority encoders per double column and on the left we see the rows. However, the schema for the pixel positions between the double column is encoded internally.

The PADs over the Matrix TowerJazz 180 nm CMOS process are referred to as PADS over LOGIC (POL) (they are normally not used over a pixel matrix). It is advised to use two metal layers for the pad for mechanical robustness. The Pads Over the Matrix needed for Power connections take the top two metal layers, M5 and TOP_M. The power meshes are also implemented by the author on the two top metals, as can be see in Figure 4.15. The power mesh contacts directly the power pads stripes with the power mesh on Metal M3.
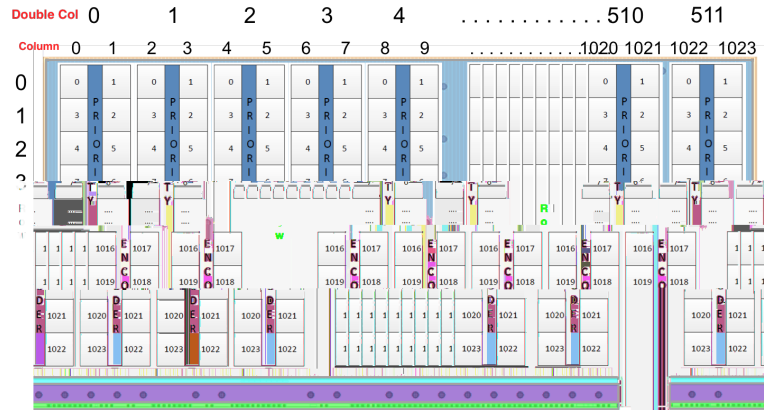
**Figure 4.14:** Priority encoder and Matrix mapping pixel and matrix position.

The power grid is also implemented on M4 and below and therefore the power grid is continuous under the pads over the matrix.
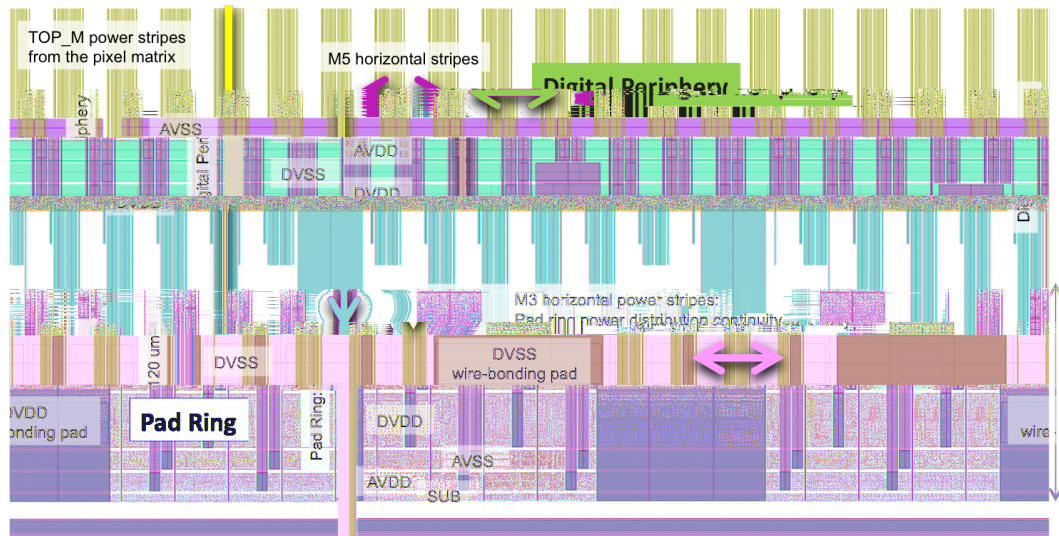


**Figure 4.15:** Power routing mesh and integration of some digital power pads layout; the power routing and pads placement are implemented by the author. The metal top layer consists of TOP_M vertical stripes, metal M5 horizontal stripes and metal M3 horizontal stripes.

The vertical power stripes are made on metal TOP from the Matrix top to the pad ring (see Figure 4.15). The Pad ring is made with

horizontal stripes in metal 3, where all structures had a pattern to continue the power projections. The idea is to continue the stripes in every structure placed in the pad ring. The pads placed in this row are functional pads; in the case of the power these pads include custom Electro Static Discharge (ESD) protection. Decoupling cells placed close to the switching digital and power pads are included in this row as well by the author.

### 4.2.2.1 pALPIDE3 Chip layout and physical implementation

The floorplan of the pALPIDE3 chip, where the Blocks: matrix, DACs, digital periphery, pad ring with custom block are placed by the author (see Figure 4.16). All blocks were verified at block level. This procedure gives access to a verilog netlist for the full chip, which can be used for the integration and the verification simulations, where the block models can be simplified to a behavioural model.
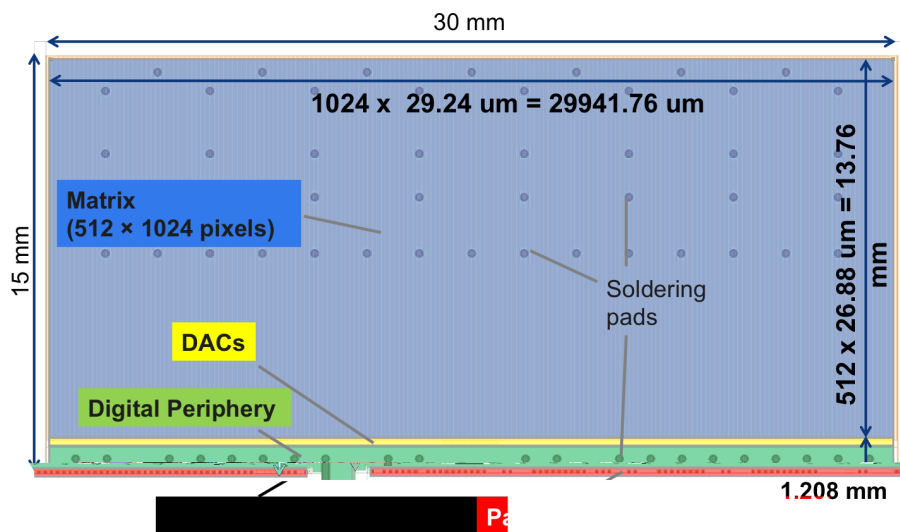


**Figure 4.16:** pALPIDE3 chip floorplan, placement and routing by the author with identification of some structures' spatial position.

At this level all circuits are placed following the integration constraints for minimum pitch in the case of the pads over circuits, alignment markers and functional pads.

#### 4.2.2.2 Digital signal routing over DACs block

Just below the matrix an analog biasing circuit is implemented: it contains the digital to analog converters (DACs) necessary for the biasing of the analog circuitry in the matrix and also for the temperature sensor. The reference for the DAC is derived from the analog power supply. In the final ALPIDE a design monitoring ADC is implemented with a bandgap as independent reference.

The Full Analog circuit is made of a 8 bits static DAC for thirteen bias values: 12 for pixels and one extra for the temperature sensor. It can be configured through the digital periphery providing bias (6 voltage levels and 7 current levels) to the active area. The reference voltage to the DACs is generated externally and provided through a wire connection to the AVDD 1.8 Vdc.
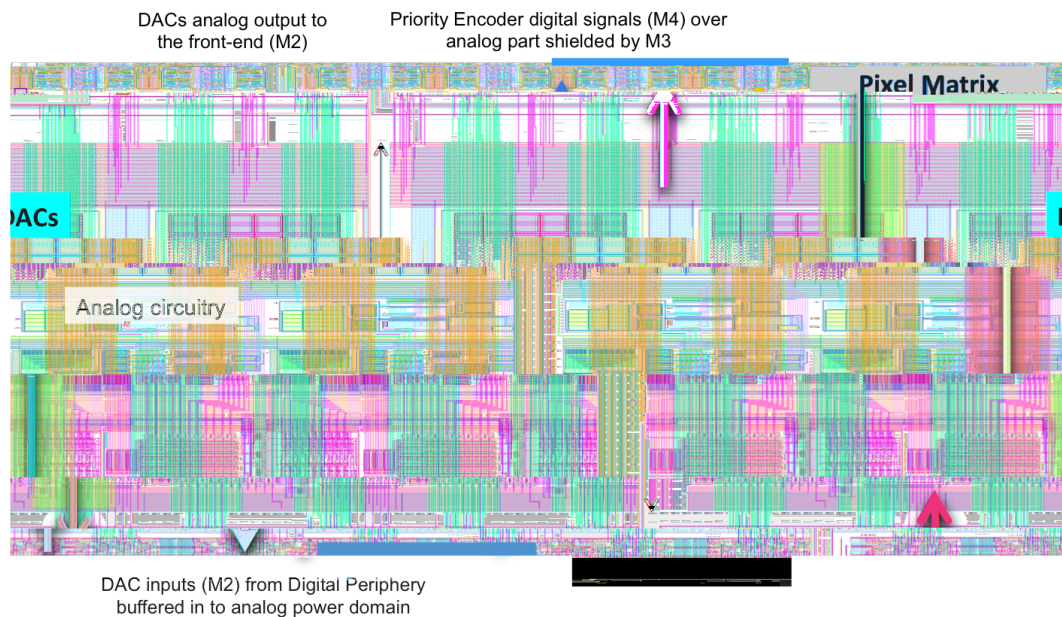


**Figure 4.17:** Routing control signal and data though DAC block implemented by the author.

After the Matrix and Matrix ring placement, the DAC biasing block is placed; the interconnection between the DAC biasing is made with automatic routing to the pixel column biasing nets by the author. The

priority encoder's inputs and outputs(IOs) is routed in metal 4 on the Full Analog circuit to the digital periphery by the author. It implements free channels on metal 4 over some sectors (see Figure 4.17) and it is isolated with metal 3 for noise coupling from the digital switching. The configuration of the the 256 inputs of the DACs is controlled from the digital periphery is connected with automatic customized routing.

### 4.2.3  Matrix power mesh analysis

The power mesh was implemented on the last two metal layers by the author (see Figure 4.18), where the digital power stripes are placed over the PE circuit and the Analog power stripes are placed over the front-end but not covering the collection electrodes. These are only covered by the metal of the pads over the circuit and in the alignment marks (see Figure 4.13).

The power mesh resistance in the horizontal (M5) and the vertical (TOP_M) directions have been calculated based on sheet resistances and geometry. The power mesh resistance (VDD & VSS) per grid unit cell based on the information on Table 4.1 is:

$$TOP\_MstripeL = 26.88\mu m \times 2 = 53.76\mu m \rightarrow \qquad (4.1)$$

$$R_{TOP\_M} = \rho_s L/W = 0.4\Omega \qquad (4.2)$$

$$M5stripeL = 29.24\mu m \times 2 = 58.48\mu m \rightarrow \qquad (4.3)$$

$$R_{M5} = \rho_s L/W = 0.9\Omega \qquad (4.4)$$

The Matrix power mesh comprises $512 \times 256$ grid unit cells, or a total mesh resistance $< 1\ \Omega$

This informations has been used to model the voltage drops in the supply lines, which will be discussed in the next section.

| Width | TOP_M | M5 |
| --- | --- | --- |
| $\mu$m | Vertical | Horizontal |
| AVDD | 5.6 | 5.04 |
| AVSS | 5.6 | 5.04 |
| DVDD | 5.6 | 5.04 |
| DVSS | 5.6 | 5.04 |
| PWELL | 1.12 | 0.56 |
| SUB | 0.56 | 0.44 |
| Space | 1.2 | 1.0 |

**Table 4.1:** Matrix metal layer widths.
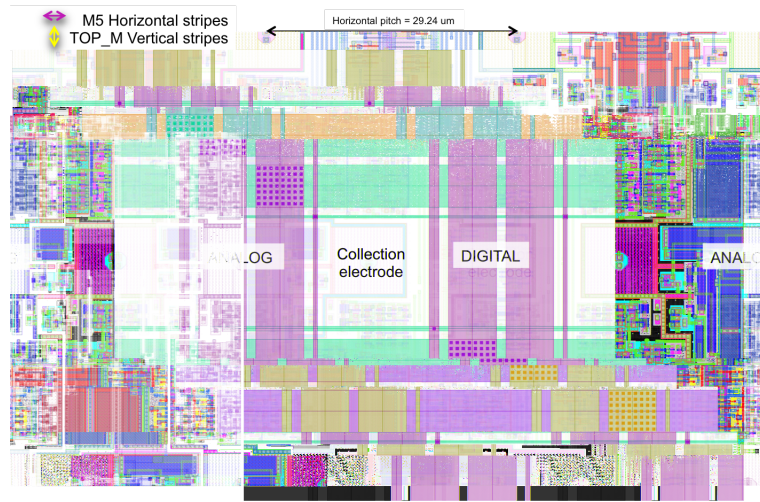


**Figure 4.18:** Matrix power mesh routed by the author.

#### 4.2.3.1 Analog Voltage drop

The voltage drop calculation is based on the following assumptions:

- The Power PAD is on the matrix edge

- Given the matrix geometry and the PAD position, the analog current flows mainly through TOP_M. First, the current primarily flows vertically.

- The Analog current per pixel $Ipix \approx 20.5$ nA, distributed uniformly over the column length. Second, the current primarily flows horizontally.

- The total analog voltage drop therefore equals: $IDAC = 2$ mA which flows to the periphery

$$\sum_{i=0}^{n-1}\sum_{k=0}^{m-1}(IDAC/m + (n-i)kIPIX)R_{TOP\_M} \approx (k/2IPIX(n+1) + IDAC/m)nR_{TOP\_M} \approx 1.5mVdc \tag{4.5}$$

Where n = 256 and m = 512 are the number of grid unit cells in a column and in a row respectively, k = 4 in the number of pixels powered by a grid unit cell, and $R_{TOP\_M} = 0.4$ Ω.

### 4.2.3.2 Digital Voltage drop

The voltage drop calculation is based on the following assumptions:

- Matrix power mesh: the current flows on metal top (TOP_M) to the periphery.

- Digital top circuit

  - Decoupling cells ≈ 2.5 nF

  - symbiotic capacitance ≈ 4nF

    * assuming 20% activity, gate area 15% of $3.5 \times 10^6$ $\mu$m$^2$

  - pWELL-nWELL junction capacitance ≈ 4nF

    * assuming $4 \times 10^6$ $\mu$m junction area 1 fF/$\mu$m$^2$

- Total decoupling capacitance > 10 nF

  - Close to the digital circuits

- DVDD/DVSS average current $I_D$ ≈ 75 mA

- Power mesh resistivity from DVDD/DVSS pads to periphery R ≈ 0.3 Ω

- $\triangle V_{drop}$ ≈ 22.5 mVdc

- Power rail RC time constant: $> 3$ ns

The Power consumption and voltage drop of a system cannot be solely determined from high- level models, but the models can be used as tools to estimate the power consumption of the full architecture; this is treated in the next section.

### 4.2.3.3 Power estimation
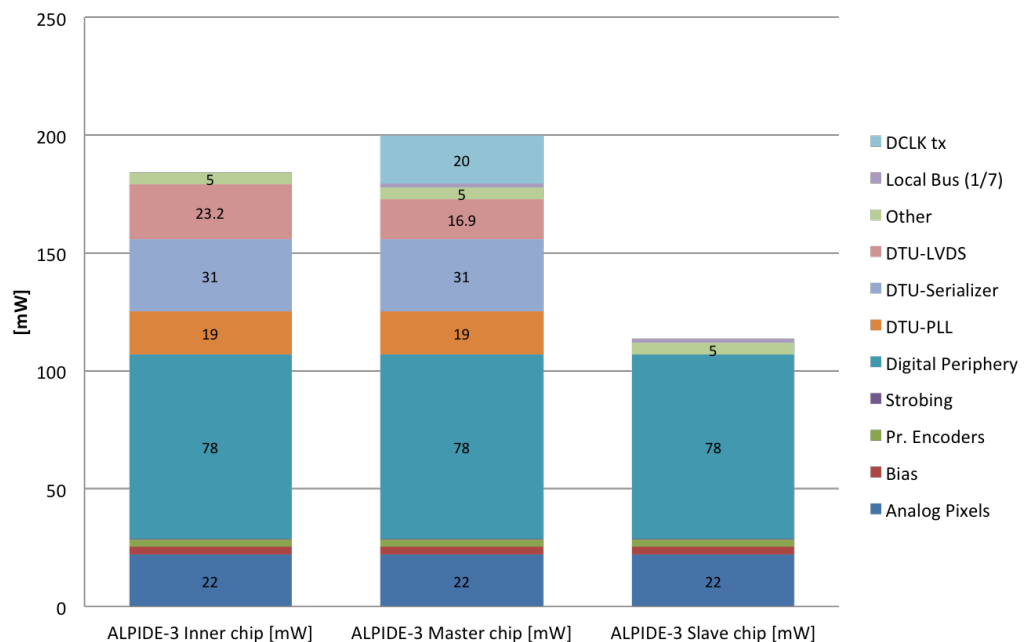


**Figure 4.19:** pALPIDE3 chip power estimates by Encounter.

Once an architecture with sufficient performance in terms of efficiency and latency has been found, a super pixel or even a pixel block can be designed at at RTL (Resistor Transistor Logic) level. . This block can then be synthesized and a prototype of the physical design completed. A back-annotated netlist of this prototype can be used in simulation to obtain toggling rates for all nets in the design in the form of Value Change Dump (VCD) information. Again back-annotating this information into a physical design tool, an accurate estimate for power

consumption of this block is obtained. The block can be characterized with different activity factors, for example idle 90% of the time and active 10% of the time. Using the power estimation from a single block and the activity map from the full architecture, an estimation for the power consumption can be obtained. Thus by taking advantage of the homogeneous structure of the pixel matrix and even the EoC blocks and the high-level models, characterizing only a few blocks can give an accurate estimate of the total power consumption. Because recording VCD files during a back-annotated simulation adds to the run-time overhead of simulation, a longer power profile for a system can be obtained by combining the activity-based power information and the high-level simulation (see Figure 4.19). The power consumption in the inner and outer barrel are different, for the first the stave configuration all chips are configured as a master, such that every chip will transmit up to 1.2 Gbps. For the outer barrel, only the master will transmit; the rest are configured as slaves and they will communicate by sending their date to the master..

| Group | Total Power mW |
|---|---|
| Sequential | 33.56 |
| Macro | 7.986 |
| Combinational | 16.73 |
| Clock | 24.34 |
| Total | 82.61 |

**Table 4.2:** Read-out Scenario Summary.

For the pALPIDE3 chip, the power of the clock tree and gates might be reduced substantially. The clock gating for the present figure without gating is: $\approx$102 mW, 35 mW for the clock tree and 67 mW for statistical estimation, the major contribution on the power consumption is the high speed serializer.

- Inner Barrel Module 184 mW / 4.5 cm$^2$ $\approx$ 41 mW/cm$^2$

- Outer Barrel Module (200+ 6*112) mW / (7*4.5 cm$^2$) $\approx$ 28 mW/cm$^2$

  Read-out conditions for study with some conservative assumptions and simulated over 40 events with 2GB VCD file.

| Group | Total Power mW |
|---|---|
| Internal | 50.29 |
| Switching | 32.29 |
| Leakage | 0.035 |
| Total | 82.61 |

**Table 4.3:** Read-out scenario summary(cont).

- Events generated by a Poisson process with a frequency of 100 kHz. A trigger is sent for every event provided that BUSY is not asserted and that the event separation is at least 800 ns.

- $85 <$ Number of clusters per event $\leq 90$. This corresponds to 18.89 /cm$^2 <$ total occupancy $< 20$ /cm$^2$. Note: Absolute maximum is reported as $19.01/$cm$^2$ and average as 15.33 /cm$^2$.

- Average cluster size is taken as 4 pixels

- $5 <$ noisy pixels / frame $< 8$. This corresponds to $10^{-5} \leq$ noisy pixel probability $\leq 1.5 \times 10^{-5}$.

#### 4.2.3.4 Measured power analysis

The dynamic power analysis on the Figure 4.20 shows a different behaviour of the pALPIDE2 chip. The bunches are the configuration of the fired pixels on the chip.

Figure 4.21 shows that the PADRE readout does not exhibit any current peaks as a function of the readout phase. Such peaks could be easily identified from the pixel readout phase. In this plot, the 32 regions with one PE fired per column gives a total of 192 pixels pulsed seven times. The red signal, the decoupling capacitors placed on the PCB were removed and the green signal, the decoupling capacitors were not removed on the PCB. The plot shows the change in current as a function of the fired pixels, and how the power supply is affected
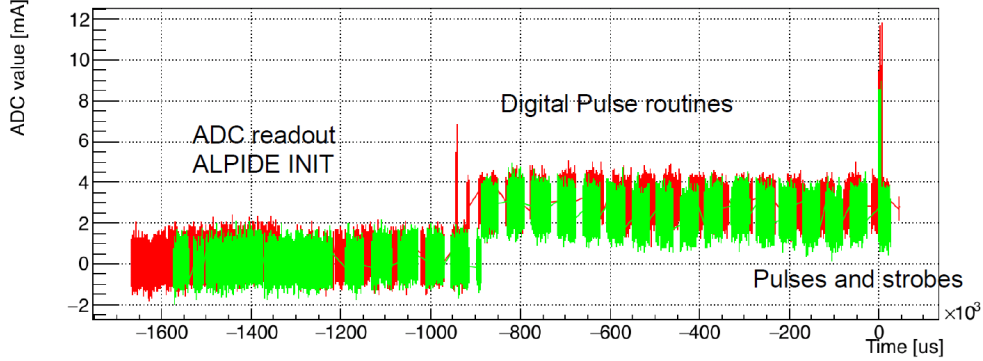
**Figure 4.20:** The pALPIDE3, pulsing 1 pix_PE per column and 6 PE_region per region having in total = 192 fired Pixels on 32 regions; in Red no decoupling capacitor and Green: RO v3 nominal board(no modifications).

with a high current consumption from the digital activity and the read-out time per bunch.
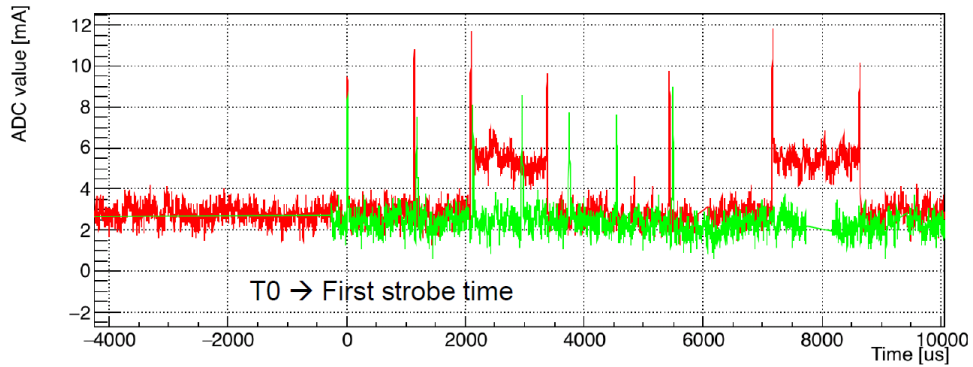


**Figure 4.21:** The pALPIDE3, pulsing 1 pix_PE per column and 6 PE_region per region having in total = 192 fired Pixels on 32 regions; in Red no decoupling capacitor and Green: RO v3 nominal board(no modifications).

Figure 4.22 shows the current profile of the read-out phase when the *STROBE* signal is applied. The peak shows the duration of the read-out that is under 20 $\mu$s and meets the ITS upgrade specifications in Table 1.5.
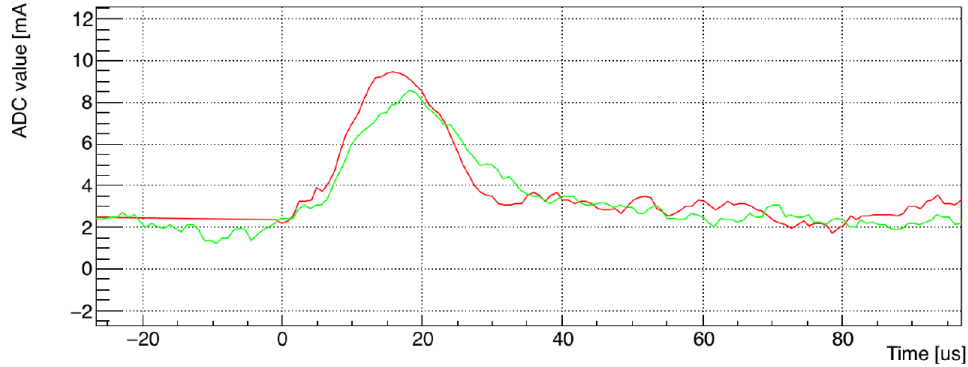
**Figure 4.22:** The pALPIDE3, pulsing 1 pix_PE per column and 6 PE_region per region having in total = 192 fired Pixels on 32 regions; in Red no decoupling capacitor and Green: RO v3 nominal board(no modifications).

## 4.3 Conclusions

The ALICE ITS upgrade has adopted MAPS for its read-out implementation. The ALPIDE development aims to reduce the power consumption and the integration time by an order of magnitude below the specifications, using a low power binary front-end (40 nW) and a data-driven read-out. As an alternative to the traditional rolling shutter read-out architecture, the Address Encoder and Reset Decoder data-driven read-out architecture has been implemented and tested, and shows significant advantages both in terms of read-out time and power consumption. This allows the pALPIDE2 chip development to reduce integration time and power consumption well below the specifications for the ALICE ITS upgrade. The test results from the fabricated prototypes show that it meets the ALICE ITS requirements.

The goal of this thesis is the design of a pixel read-out implemented in this MAPS technology, where all circuits designed are working satisfying the pixel size, read-out time and power consumption.

The thesis has discussed and presented a data-driven architecture in the matrix read-out chips of the pALPIDE families taking into account area and power limitations presented in this chapter. In Particular, read-out architectures for vertexing were presented. The presented techniques for chip assembly, which are especially adapted for area

| Architecture | Pitch | Integration time | Power consumption |
|---|---|---|---|
| (discriminator, read-out) | $(r\phi \times z)(\mu m^2)$ | ( $\mu$s) | $(mWcm^{-2})$. |
| MISTRAL[79, 80] | 36×65 | 30 | 100 |
| (endofcolumn, rolling-shutter) | | | |
| ASTRAL[79, 80] | 22×33 | 30 | 300 |
| (in-pixel, rolling-shutter) | 36×31 | | 100 |
| pALPIDE_ss chip | 20×20 | <2 | < 20 |
| pALPIDE_fs chip /pALPIDE2 chip | 28×28 | 4 | < 80 |
| pALPIDE3 chip /pALPIDE3B chip | 29.24×27.64 | 2 | < 50 |
| (in-pixel, in-matrix sparsification) | | | |

**Table 4.4:** Overview of the read-out chips in the development of the ITS upgrade.

and implementation of mixed-signal pixel read-out ASICs, can be used to improve the read-out efficiency of read-out architectures. The techniques presented here are also compatible with modern digital ASIC design techniques and standard cell design flow, making it possible to quickly port them into new CMOS technologies.

The average particle occupancy per event foreseen in the inner layer of the ITS is 150 hits per cm$^{-2}$ [31]. The read-out time for such a number of hits is lower than 2 $\mu$s. Including the previous values for the hit density and cluster multiplicity and considering a trigger rate of 100 kHz, the total power consumption of the 512 PADRE circuit of the matrix is about 8.26 $\mu$W.

Looking in the summary Table 4.4 and confronting the requirements in Table 1.5, the ALPIDE family meets the ALICE ITS upgrade requirements.The radiation hardness, charge collection and efficiency will be addressed in the next chapter.

# Chapter 5

# Full scale experimental results

This chapter focuses on the experimental results and characterization obtained for the ALPIDE full scale chips, and reports on their performance with ionization particles. The sensors are irradiated with neutrons and the effects of Non Ionizing Energy Loss (NIEL) are studied. A custom read-out system for the ALPIDE full scale samples was designed.

All circuits designed under the ALPIDE family have been studied and characterized by the characterization team. It is formed by a collaboration of INFN Bari, Cagliari and Catania from Italy, Pusan and Inha from Korea and the ALICE ITS team. The circuits were tested in a radiation campaign starting in 2012 in the following facilities DESY in Germany, Frascati in Italy and PS & SPS at CERN.

## 5.1   Read-out System

During 2014 a read-out system based on a FPGA was developed in Cagliari to characterise the pALPIDEs prototype. It consists of a single DAQ card (size 12 cm × 10 cm) that interfaces directly to the pALPIDE carrier board (Figure 5.1) through a PCI Express connector.

The system exploits the USB 3.0 protocol to communicate with an external PC for configuration and for raw data transmission. The
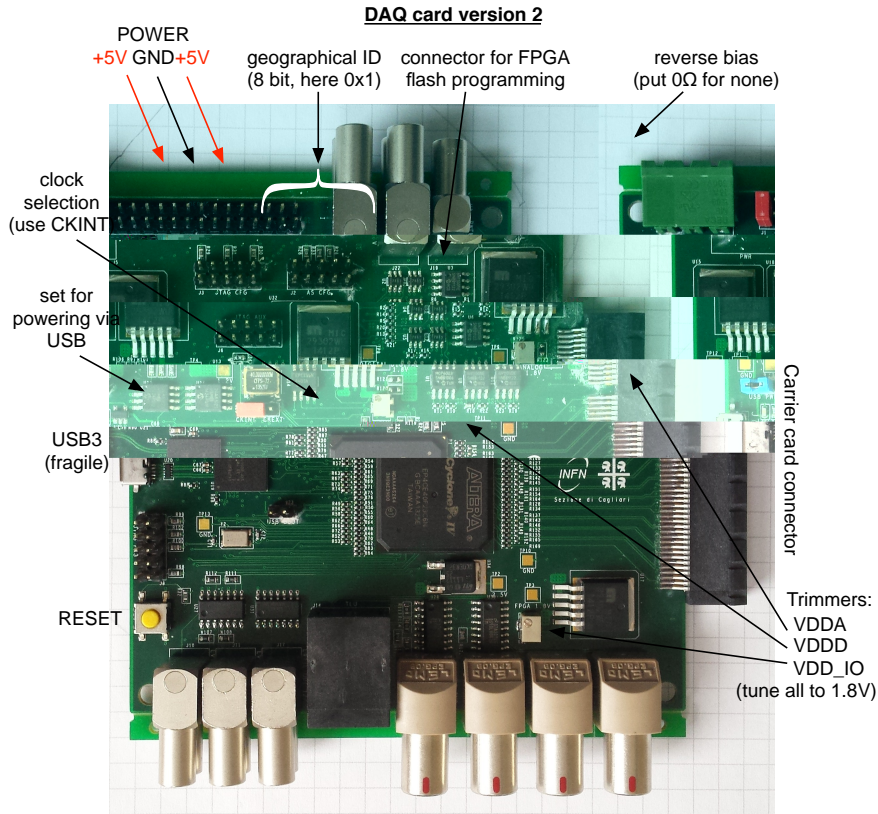
**Figure 5.1:** Read-out DAQ board.

USB connector is also used to power the card. However, an additional 5V power connector was placed on it to provide additional current strength in order to ensure proper electrical stability.

## 5.2 ALPIDE family experimental results

In the following subsections, the author will bring a brief explanation on the results obtained from the ITS upgrade characterization team. Each of the following measurements in the lab was performed covering the sensor to shield it from the sunlight and any kind of light. The conversion factor that gives the correspondence between DAC units

and electrons is not obtained with a calibration of the system, but by exploiting the pulse mechanism observed by the sensor. Since the pulsing capacitor is 160 aF, the charge injected into the pixel when a voltage step $\Delta V$ is applied to that capacitor is given by:

$$
\begin{aligned}
Q_{inj}[e^-] &= C_{inj}\Delta V \\
&= \frac{1}{1.6 \, 10^{-19}} 160 \; 10^{-18} F \frac{1.8}{256} N[DAC] \\
&\approx 7.03 N[DAC]
\end{aligned}
\tag{5.1}
$$

which gives the conversion factor 1 DAC $\approx$ 7 e$^-$.

The detector response to an irradiation (hit-map) is tested with soft X-rays (E < 10 keV) or radioactive sources, which for these tests are $^{55}$Fe and $^{90}$Sr. The $^{55}$Fe radioactive source emits photons with energy between 5.9 and 6.5 keV and the $^{90}$Sr radioactive source $\approx$ 550 keV. The energy is deposited in the epitaxial layer (via the photoelectric effect) is comparable to the energy deposited by a minimum ionizing particle of 1060 / 146 electrons in the nWELL diode around the center of the impact point of the radioactive source.

The pALPIDE2 chip has been successfully characterized in a test beam before and after the exposure to non-ionizing radiation of $1 \times 10^{13}$ 1 MeV n$_{eq}$cm$^{-2}$. Figure 5.11 shows the detection efficiency, fake-hit rate, spatial resolution and cluster size as a function of the I$_{THR}$ bias, which is proportional to the charge threshold. The results are presented for an epitaxial layer thickness of 25 $\mu$m, an nWELL-pWELL spacing of 2 $\mu$m and a substrate voltage of -6 Vdc. At nominal threshold setting (I$_{THR}$ = 500 pA), the detection efficiency is close to 100% with a fake hit rate below $10^{-8}$ hits/pixel/event. At the spatial resolution of 5 $\mu$m is achieved with an average cluster size of 2 pixels. These results show that the pALPIDE2 satisfies the ALICE ITS requirements summarized in Table 1.5.

All ALPIDE family circuits which were tested and were studied using a telescope based on an arrangement of bi-dimensional reference planes. The DUT (Device Under Test) is placed close to the reference device to track the particles which are typically focused on the center of the

telescope. As result the DUT was analyzed with the results of the reference device and the differences were compared. The tracks were recorded per read-out event.

The pALPIDE3 and pALPDIE3B sensors were fully tested, including the characterization and qualification of their functionality. The circuit is functional (see Figure 5.12), where the Front-end read-out was implemented by the author and its read-out frequency is a 20 Mhz clock. The results on the qualification on pALPIDE3B sensor and the selection of the pixel collection electrode size and reset mechanism were selected on March 2016 by the ALICE ITS coordination. The functionality of the new customized Front-end for the ALICE ITS was thoroughly tested on radiation test campaign.

### 5.2.1 Charge Threshold Setting

The correct bias settings will have a major impact on the functionality, charge collection and fake-hit rate. The main parameters for influencing the threshold and noise were found to be $V_{CASN}$ and $I_{THR}$ (see Figure 4.7), as expected from the circuit design. An increase of $V_{CASN}$ leads to a lower threshold, as it corresponds to a higher baseline value of the output pulse at the HIT node. A decrease in $I_{THR}$ leads to a lower threshold as expected from the slower reaction of the feedback mechanism discharging HIT. $V_{CASN}$, however, has to be adjusted depending on $V_{BB}$. This can be explained by the nMOS transistor being embedded in a pWELL, which is set to $V_{BB}$. $V_{CASN}$ in fluences not only threshold but also has a stronger influence on the fake-hit rate than $I_{THR}$ with and without Reverse Substrate Bias $V_{BB}$. The$V_{BB}$ applied bias range was from 0 Vdc to -6 Vdc.

### 5.2.2 Noise occupancy as a function of bias

The estimation of the noise occupancy, i.e. the rate at which noise produces a response of the pixel front-end which exceeds the selected threshold (fake hit), is of great importance as it strongly affects the tracking capabilities of a layered detector. If the noise occupancy is significant, track fitting algorithms lose efficiency and/or resolution in

the estimation of the impact parameter. For the ALPIDE family, the rate of fake hits was obtained according to the following procedure:

- First, the front-end bias is set to a fixed value of $V_{CASN}$ and then a voltage scan is performed on $I_{THR}$ and the rest bias to the defaults

- A given number of triggers, N, is sent to the sensor in absence of any radioactive source and the circuit is brought to acquisition mode by applying a STROBE signal, in this case for a few ns in this case.

- The total number of hits due to the noise is counted in each of the four sectors of the sensor *($N_i$ $^{fh}i$, $i = 1,..,4$)*, depending to the ALPIDE family

The fake hit rate in a sector is obtained with the following:

$$F_i = \frac{N_i^{fh}}{NN_{pix}} \tag{5.2}$$

where $N_{pix}$ is the number of pixels of that sector. Since this measurement depends on the threshold it is typically performed for various $V_{CASN}$ and $I_{THR}$ combinations, to see how the bias of the front-end affects the noise occupancy.

## 5.3  pALPIDEfs

Each pALPIDEfs collection diode is obtained by implanting a n-well in the lightly p-doped epitaxial layer. The shape of the nWELL (octagonal) are chosen so that the couplings between the two are minimized and hence the Q/C ratio is maximized.

Two reset mechanisms are used: diode and pMOS reset, as seen in Figure 5.2 and Figure 5.3 . In both cases the collection diode is continuously reset, but in the former case the time constant associated to the reset mechanism can be varied by setting the gate potential of the reset transistor.
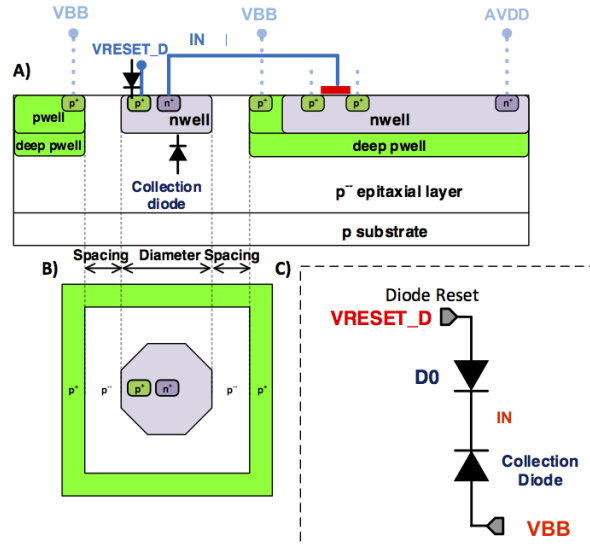
**Figure 5.2:** Collection electrode and pixel circuit including diode reset mechanism. a) Cross section, b) top projections, c) circuit schematic.
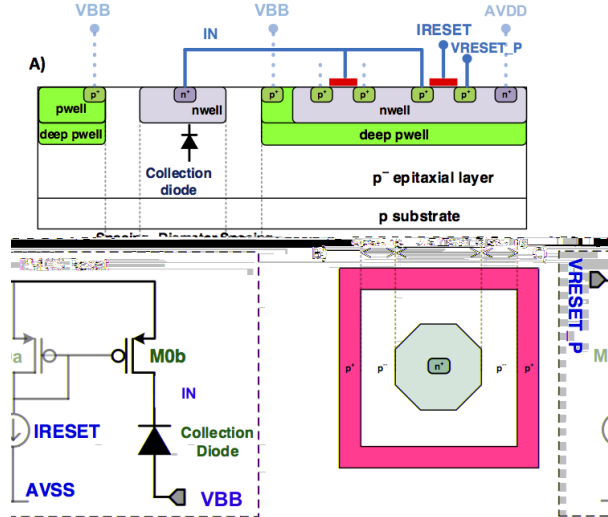


**Figure 5.3:** Collection electrode and pixel circuit including pMOS reset mechanism. a) Cross section.b) top projections, c) circuit schematic.

The pALPIDEfs matrix contains four types of collection diodes placed in four sectors, each containing 256 double columns of 512 pixels. The

| Sector | Columns | nWELL diameter $\mu$m | Spacing $\mu$m | Reset |
|--------|---------|-----------------------|----------------|-------|
| 0 | 0 to 255 | 2 | 1 | pMOS |
| 1 | 256 to 511 | 2 | 2 | pMOS |
| 2 | 512 to 767 | 2 | 2 | Diode |
| 3 | 768 to 1023 | 2 | 4 | pMOS |

**Table 5.1:** Geometrical parameters and reset mechanisms of pALPIDEfs sensing elements in the four chip sectors.

pixels of a given sector differ from the pixels of the other sectors in the nWELL diameter, nWELL/deep-pWELL spacing and reset mechanism. Table 5.1 shows the geometrical parameters of the collection diodes of the four pixel types designed for pALPIDEfs. The corresponding reset mechanisms are also listed.
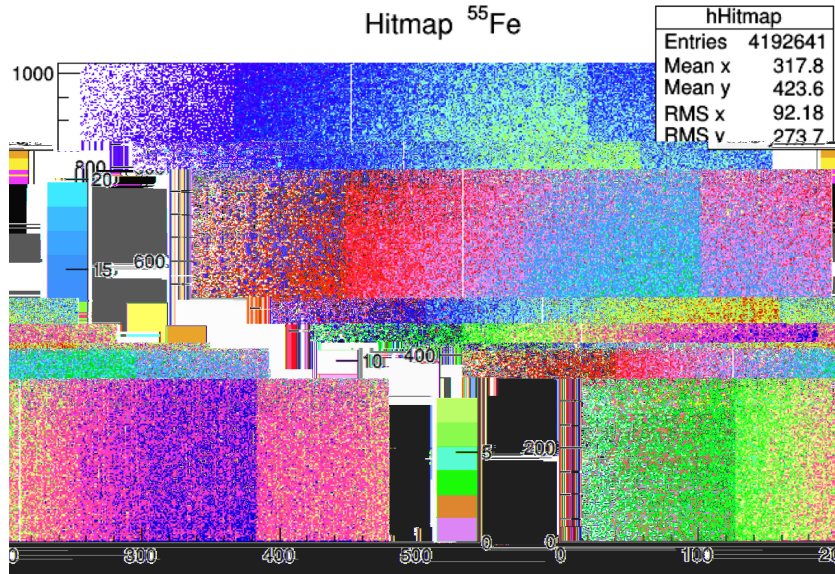


**Figure 5.4:** pALPIDEfs hit-map under $^{55}$Fe exposure. The source was placed over the colummn 0 and row 350, and easily are identify the different sensing elements throug all rows.

Figure 5.4 shows the hit-map of the chip under $^{55}$Fe source exposure and the figure clearly indicates the location of the source and also illustrates the different sectors on the chip and and how it is opera-

tional as a pixel detector. As we see the circuit is fully operational and the front-end read-out works correctly. Additionally, we can identify the difference between a few pixels of the pALPIDEfs. Further characterization on charge collection, efficiency and fake hit rate will be implemented in the characterization on the pALPIDE2. The collection electrodes of the 4 sectors are easily identified.

### 5.3.1 Source scan

The threshold has an important effect on most of the performance parameters of the sensor: a lower threshold will increase the detection efficiency, but also increase the fake-hit rate. Furthermore, an increased threshold results in a decreased cluster multiplicity, with a direct consequence on the position resolution.



(a) Threshold.                    (b) Temporal noise.
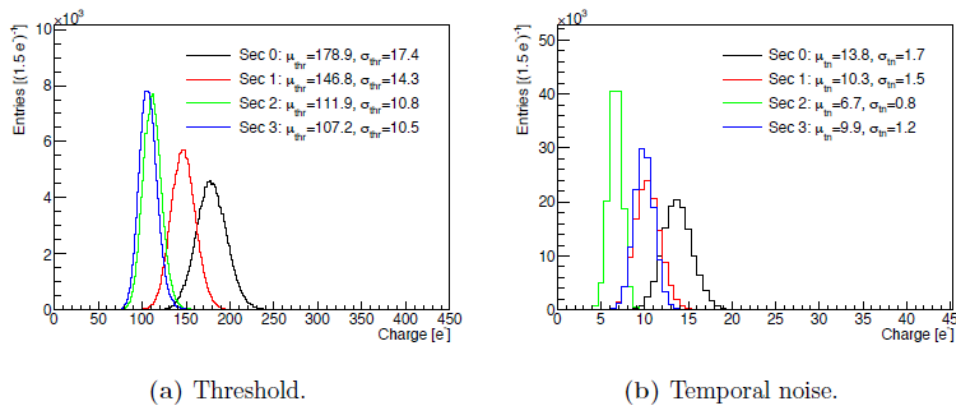
**Figure 5.5:** Threshold and temperoal noise distributions (including all pixels) for pALPIDEfs chipat $V_{BB}$= -3 Vdc, $I_{THR}$= 20 DAC counts, and nominal $V_{CASN}$.

Example of a threshold scan on a single pALPIDEfs chip. The Figure 5.5 shows the distributions of the measured thresholds for the four sectors of the chip. The scan was done without back bias at nominal settings ($V_{CASN}$ 57, $I_{THR}$ 51). The mean value of the threshold is 136 e$^-$.

### 5.3.2 Test beam measurement

Test beam mMeasurement at PS at the CERN facility with energies between 5 - 7 GeV $\pi$ beam. The pALPIDEfs chips were irradiated neutrons with fluxes of $0.25 \times 10^{13}$ 1 MeV $n_{eq}$cm$^{-2}$. This flux is 10 $\times$ higher than expected in the lifetime of the ALICE upgraded detector. The ALICE upgrade is planned to be in operation after Long Shutdown 2 (LS2) and has a programme that will extend into the HL-LHC era after Long Shutdown 3 (LS3)[31].
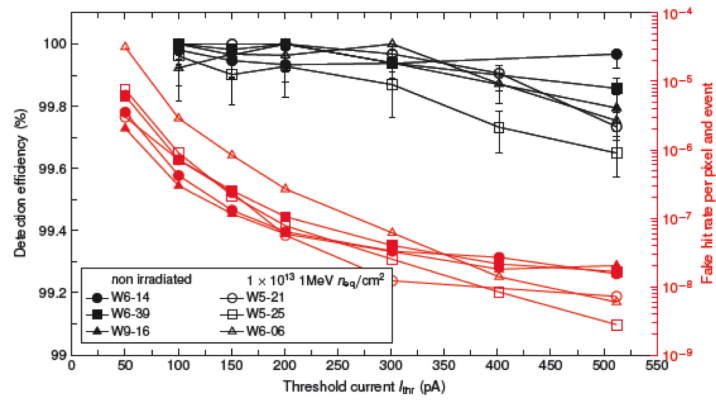


**Figure 5.6:** pALPIDEfs efficiency and fake hit rate.

Figure 5.6 shows the efficiency and fake-hit rate for the best biasing settings before and after neutron irradiation. This plot should be divided in two parts; the left part with black dots shows the detection efficiency scale after and before irradiation. We can identify in some cases that the detection efficiency is around 100% but it is strongly influenced by $I_{THR}$. The dependence of the detection efficiency on the charge threshold can clearly be recognized, as it decreases for all curves with the increment of $I_{THR}$. The same behaviour is evident for the fake-hit rate, shown by red dots.

## 5.4 The pALPIDE2

The pALPIDE2 sensor matrix contains four types of collection diodes placed in four sectors, each containing 256 double columns of 512 pixels as its predecessor pALPIDEfs. Figure 5.9 shows the geometrical parameters of the collection diodes of the four pixel types designed for pALPIDE2. The corresponding reset mechanisms are also listed.

| Sector | Columns | nWELL diameter $\mu$m | Spacing $\mu$m | Reset |
|--------|---------|---------------|---------|-------|
| 0 | 0 to 255 | 2 | 2 | pMOS |
| 1 | 256 to 511 | 2 | 2 | pMOS |
| 2 | 512 to 767 | 2 | 4 | pMOS |
| 3 | 768 to 1023 | 2 | 4 | Diode |

**Table 5.2:** Geometrical parameters and reset mechanisms of pALPIDE2 sensing elements in the four chip sectors.

pALPIDE2 sensor has implemented the same reset mechanism implemented in pALPIDEfs seen in (Figure 5.2) and (Figure 5.3) where the collection diode is continuously reset, but in the former case the time constant associated to the reset mechanism can be varied by setting the gate potential of the reset transistor.

The characterization of pALPIDE2 was at DESY with energies from 1 to 6 GeV with fluxes of $1.7 \times 10^{13}$ 1MeV $n_{eq}$cm$^{-2}$ electron beam. For the pALPIDE2, the detection efficiency and position resolution and their dependence on the epitaxial-layer thickness and front-end settings were studied.

### 5.4.1 Source scan

Figure 5.7 is a plot with default settings, where no back bias was applied. The plot shows the threshold in electrons for all pixels of the chip. The scan was done without back bias at nominal settings ($V_{CASN}$ 57, $I_{THR}$ 51). The four different sectors of the chip are clearly visible, as well as (parts of) the pads over the matrix. And we can easily identify the best sector according to the charge collection. The sector 3 was placed in the right of the chip in red colour.
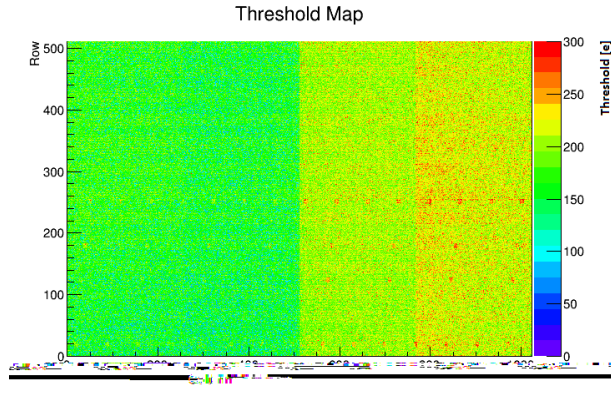
**Figure 5.7:** pALPIDE2 Threshold Map nominal settings.

Figure 5.8 shows the impact of the back bias on the threshold improving the charge collection. For thresholds between 100 and 200 e$^-$, there is a clear difference between different sectors and with some increase of the threshold in regions with pads over matrix.
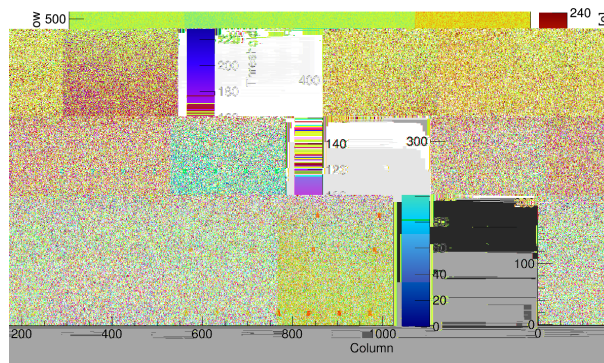


**Figure 5.8:** pALPIDE2 Threshold Map V$_{BB}$= -3 Vdc.

Figure 5.9 shows, an example of a threshold scan on a single pALPIDE2 chip and this plot shows the threshold in electrons for all pixels of the chip. The scan was done with -3 Vdc back bias at settings (V$_{CASN}$ 135, I$_{THR}$ 51). The four different sectors of the chip are clearly visible, as well as the pads over the matrix in the sector 3. The back bias voltage in this sector improves the charge collection.

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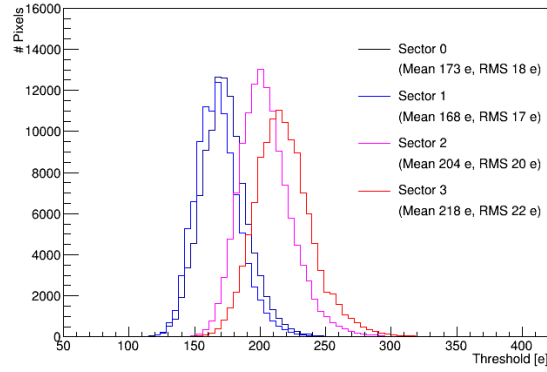
**Figure 5.9:** pALPIDE2 Threshold Full chip nominal settings.

Figure 5.10 shows, the mean threshold values for the four sectors of the pALPIDE2 chip as a function of $I_{THR}$ with -3 Vdc back bias. All values have been averaged over 1% of the pixels of 4 different chips. The scans were done with a $V_{CASN}$ setting of 135; the nominal setting for $I_{THR}$ is 51.
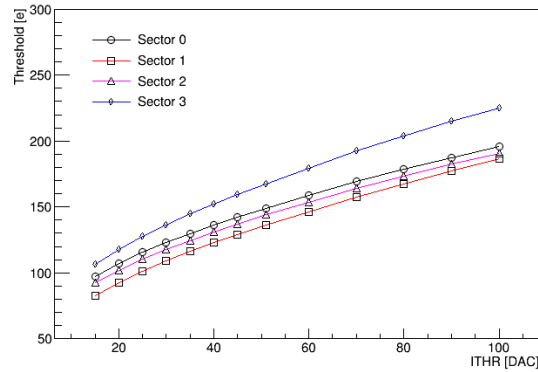


**Figure 5.10:** pALPIDE2 Threshold Map on full chip, $V_{BB}$= -3 Vdc.

### 5.4.2 Test beam measurement
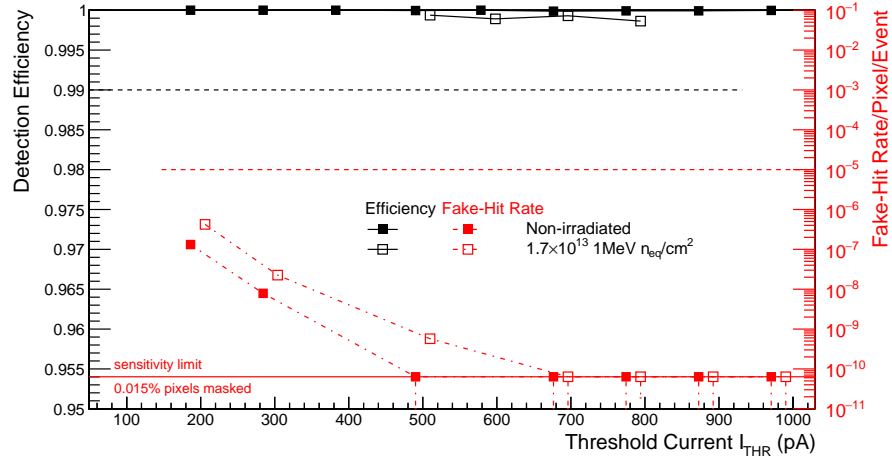


**Figure 5.11:** pALPIDE2 $4\mu$m spacing, 25 $\mu$m epi, -6V back-bias pMOS reset.

Figure 5.11 shows the efficiency and fake-hit rate for the best settings before and after neutron irradiation. This plot must be divided in two parts; in the left part, the black shows the detection efficiency scale after and before irradiation. The black points shows the lower detection efficiency which is acceptable for the ITS upgrade program summarized in Table 1.5. The second part shows the fake hit rate scale in red. The red points show the higher limit on the fake hit rate summarized in Table 1.5. This plot shows an efficiency higher than 99.5% with a fake hit rate lower than $10^{-6}$. This means that the pixel behaves as expected when the $I_{THR}$ is higher than 500 pA.

The influence of $I_{THR}$ and $V_{CASN}$ settings and the dependency of the detection efficiency on the charge threshold can clearly be recognized, as it decreases for all curves with increasing $I_{THR}$ and increases with increasing $V_{CASN}$. Since the front-end bias settings have no influence on the charge collection process, similar values of detection efficiency can be observed for different combinations of $I_{THR}$ and $V_{CASN}$. Similar trends can be noticed for the average cluster multiplicity. The influence of reverse substrate bias voltage influences the extension of the depletion zone, with a direct effect on the junction capacitance and the characteristics of the charge collection process. The effect can

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be clearly observed, where for all pixel types (sectors) and front-end bias combinations the detection efficiency is significantly larger when increasing $V_{BB}$ from 0 Vdc to -3 Vdc or -6 Vdc.

## 5.5   The pALPIDE3 and pALPIDE3B

The pALPIDE3 sensor matrix contains eight types of collection diodes placed in eight sectors each containing 128 double columns of 512 pixels width 3.75 mm/sector. Table 5.3 shows the geometrical parameters of the collection diodes of the eight pixel types designed for pALPIDE3 front-end (see Figure 4.7). The corresponding reset mechanisms are also listed including the type of clipping and $V_{CASN2}$ and M1 transistor bulk connection.

| Sector | Columns | nWELL diameter $\mu$m | Spacing $\mu$m | Reset | $V_{CASN2}$ transistor | Clipping M6 | M1 bulk |
|--------|---------|-----------------------|----------------|-------|------------------------|-------------|---------|
| 0 | 0 to 127 | 2 | 2 | Diode | Yes | Diode | AVDD |
| 1 | 127 to 255 | 2 | 2 | Diode | No | Diode | AVDD |
| 2 | 256 to 383 | 2 | 2 | Diode | No | Diode | AVDD |
| 3 | 384 to 511 | 2 | 2 | Diode | Yes | VCLIP | AVDD |
| 4 | 512 to 639 | 2 | 2 | Diode | Yes | VCLIP | Source |
| 5 | 640 to 767 | 2 | 3 | Diode | Yes | VCLIP | Source |
| 6 | 768 to 895 | 2 | 2 | pMOS | No | Diode | AVDD |
| 7 | 896 to 1023 | 2 | 2 | pMOS | Yes | VCLIP | AVDD |

**Table 5.3:** *Geometrical parameters and reset mechanisms of pALPIDE3 sensing elements in the eight chip sectors.*

As described earlier, the same reset mechanism for the pALPIDEfs sensor and the pALPIDE2 sensor was implemented in the pALPIDE3 sensor. Two reset mechanisms are sketched in Figure 4.7 and their layout is seen in Figure 5.2 and Figure 5.3 showing a reset via a pMOS transistor and reset via diode, respectively. In both cases the collection diode is continuously reset, but in the former case the time constant associated to the reset mechanism can be varied by setting the gate potential of the reset transistor

The pALPIDE3 arrived the $20^{th}$ of October 2015. The ITS characterization team started the studies and functional verification of chip. The
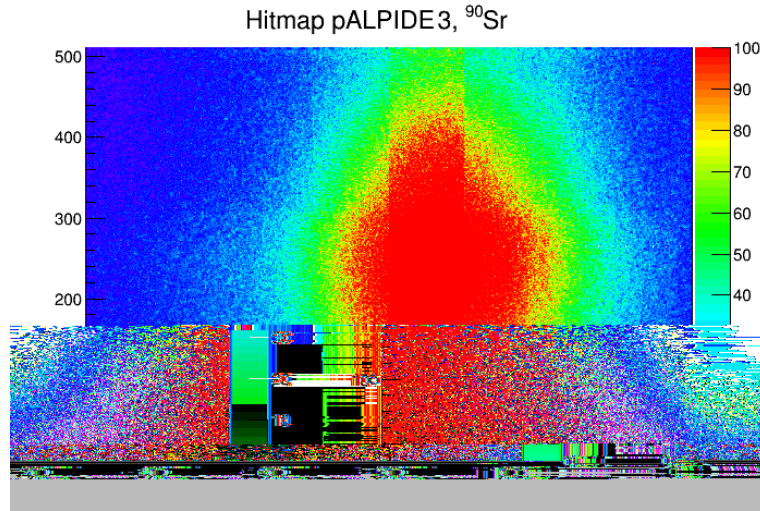
**Figure 5.12:** pALPIDE3 hit-map with a $^{90}$Sr radiation source.

chips are tested with a $^{90}$Sr gamma source, as seen in Figure 5.12. The figure shows that the chip is operational as a pixel detector, testing all structures starting from the front-end to the transmission line. The figure clearly indicates the location of the source and also illustrates the different sectors on the chip.

The first results were as follows:

- Yield seems to be higher than for pALPIDE2 sensor (based on the first 9 chips).

- General threshold and noise behaviour are similar to pALPIDE2 sensor, with two differences:

  - Thresholds at same setting are lower in general.

  - Thresholds in sectors 4 and 5 are much lower than in pALPIDE2, apparently without penalty in the noise occupancy.

- The characterization team found some problems with the masking masking schema. Due to the routing of the masking nets under the pads over logic, and when the pad over the matrix is wire-bonding; it generate a short circuits between the TOP_M

layer and the masking net in M5 layer; first tests seem to confirm this. This problem was solved by adding a structure to connect the masking and selection nets under the pad thereby avoiding the routing through the free channels on metal M5.

### 5.5.1 Test beam measurement
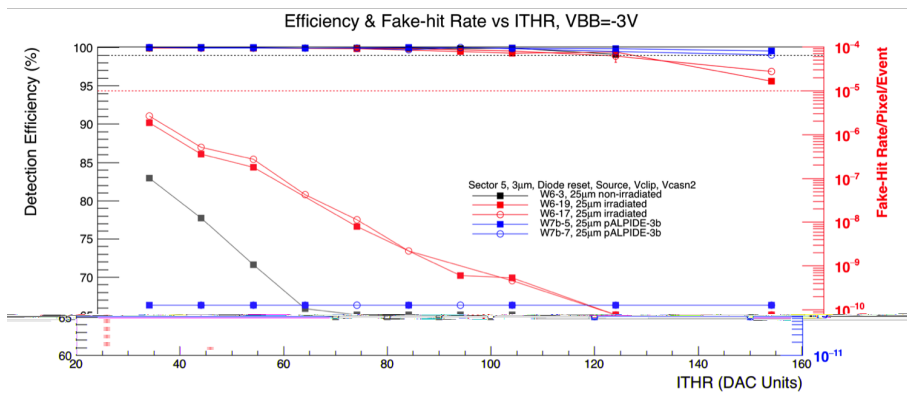


**Figure 5.13:** The pALPIDE3B with $3\mu$m spacing, 25 $\mu$m epi, -3 Vdc back-bias Diode reset, VCLIP and $V_{CASN2}$ in nominal settings.
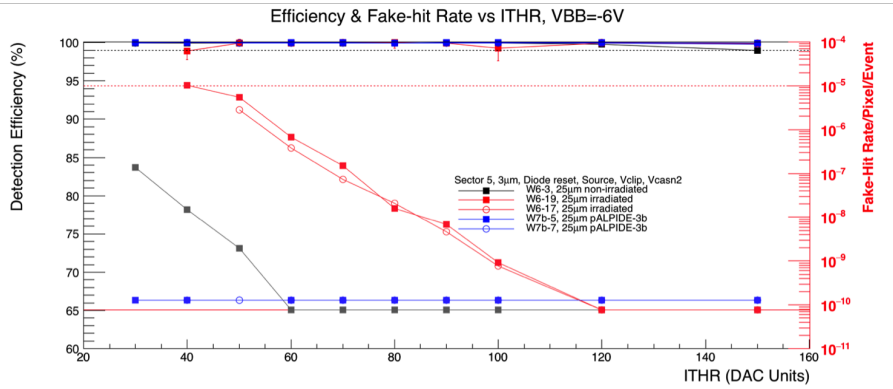


**Figure 5.14:** The pALPIDE3B with $3\mu$m spacing, 25 $\mu$m epi, -6 Vdc back-bias Diode reset, VCLIP and $V_{CASN2}$ in nominal settings.

The pALPIDE3B was tested in the Frascati Synchrotron facility in Rome with fluxes of $1.7\times10^{13}$ 1MeVn$_{eq}$cm$^{-2}$ at 28 °C with an electron beam of 450 MeV. The pALPIDE3B was tested in a pixel telescope implemented by the ALICE ITS characterization team using the

pALPIDE2 chips. It is composed with 7 planes of 6 layers of tracking plane and 1 DUT (Device Under Test) plane. For each run, we obtained 30000 events with 20 tracks / event and having dead beam-time. The dead beam-time is due to changing input particles (e$^-$ ⇔ e$^+$).

Figure 5.13 and Figure 5.14 show the efficiency and fake-hit rate for the best settings with -3 Vdc and -6 Vdc back bias respectively. These plots must be divided in two parts. In the left part, the black shows the detection efficiency scale after and before irradiation. The black dots show the lower detection efficiency acceptable for the ITS upgrade program summarized in Table 1.5. The minimum allowable detection efficiency is 99% and it is indicated in the plot by the black dotted line. The second part shows the fake hit hate scale in red. The minimum detection efficiency is $10^{-5}$ and it is indicated in the plot by the red dotted line. The red dots show the higher limit on the fake hit rate summarized in Table 1.5. This plot shows an efficiency higher than 99.5% with a fake hit rate lower than $10^{-9}$. This demonstrates that the pixel behaves as expected when the $I_{THR}$ is between 30 DAC counts and 100 DAC counts before and after irradiation for the Chip identified as **W7b-5**.

Figure 5.13 and Figure 5.14 show that the pALPIDE3 sensor is essentially 100% efficient with a sufficiently low fake-hit rate over a large of parameters.
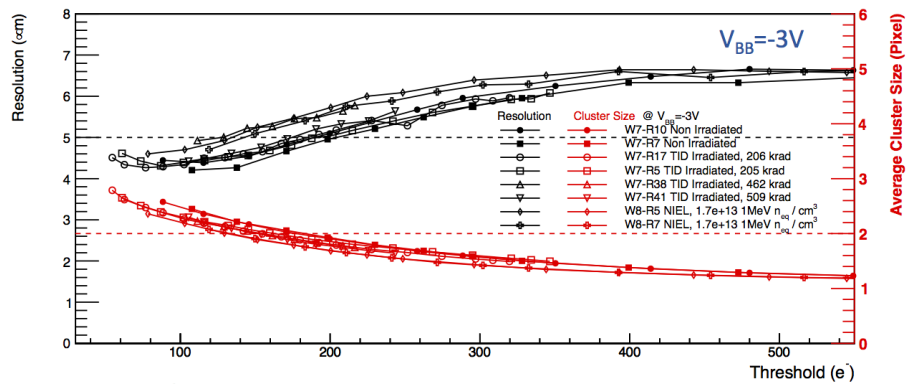


**Figure 5.15:** pALPIDE3B 3$\mu$m spacing, 25 $\mu$m epi, -3 Vdc back-bias Diode reset, VCLIP and in nominal settings.

Figure 5.15 shows the resolution and the cluster size for the best settings with -3 Vdc back bias. These plots must be divided in two parts; in the left part, the black shows the resolution before and after irradiation. The minimum allowable resolution is $5\mu$m and it is indicated in the plot by the black dotted line. The spread of the black lines shows the resolution of the tracker. The second part shows the average cluster size in red. The minimum allowable cluster size is 2 and it is indicated in the plot by the red dotted line. The red dots show the higher limit on the fake hit rate summarized in Table 1.5. The non-irradiated and TID/NIEL chips show a similar performance. The resolution is about 6 $\mu$m with a threshold of 300 electrons. The plot shows sufficient operational margin even after the ten times expected lifetime NIEL dose.

## 5.6 Conclusion

As described in section 4.3, a different fast and low power architecture has been implemented and tested, resulting in significant advantages, both in terms of read-out time and power consumption. This allows the pALPIDE family development to reduce integration time and power consumption well below the specifications for the ALICE ITS upgrade. The test results from the fabricated prototypes show that the front-end read-out circuit exceeds specifications on the integration time.

The beam test illustrates very good position resolution and detection efficiency. Reverse substrate bias provides more operation margin. Irradiated devices are currently being tested; from previous test, we expect to satisfy the ALICE requirement of $1.7\times10^{13}$ 1MeV $n_{eq}$cm$^{-2}$.

The ITS upgrade characterization team recommends unanimously to use sector 5 of pALPIDE-3b on a 25 $\mu$m-thick epitaxial layer for ALPIDE. This decision is based on the demonstrated performance in terms of detection efficiency, fake hit rate, time response. This decision was discussed in the ITS upgrade characterization team and TC meetings in march 2016. The decision was based on the large operational margin and additional configurations that this sector offers. It has larger operational margins in terms of chip settings that fulfil

all ITS requirements. It can also be used with 18 $\mu$m-thick epitaxial layers without back-bias, as can be seen in Figure 5.14. We selected sector 5, and that was the end of the optimization to go to the Alice Pixel Detector (ALPIDE) chip.

# Chapter 6

# Conclusions and future work

The upgrade of the ITS aims to have a high granularity to improve the standalone tracking efficiency at low $p_T$ , a reduction of the power consumption to decrease the material budget, a reduction of the integration time to decrease the pile-up probabilities and a fast read-out. This will offer the possibility to perform high precision measurements which are needed in order to characterize QGP.

The ITS upgrade has chosen MAPS for its implementation. The ALPIDE architecture has been chosen after it demonstrated to be the best option to satisfy the requirements, offering very low power through a 40nW binary front end and a special sparsification read-out architecture. It is implemented in a technology with a deep-pWELL allowing full CMOS circuitry in the pixel. The author designed the digital read-out of the pixel matrix, but also significantly contributed to the chip assembly and to the many small-scale prototypes which were used for testing in the early phases of the project.

Intensive R&D has been carried out over the past four years on MAPS in the framework of the ALICE ITS upgrade. Various small-scale demonstrators have been developed and successfully tested with X-ray, irradiation sources and beams of particles. The radiation tolerance of ALICE ITS is moderate with a TID radiation hardness of 700 krad and a NIEL radiation hardness of $10^{13}$ 1 MeV $n_{eq}cm^{-2}$. Thus MAPS are a viable option for the ITS upgrade.

The original contribution of this thesis is to implement a novel digital pixel read-out architecture for MAPS. This thesis presents an asynchronous In-column address encoder (Zero Suppression data-driven architecture and a bus-based architecture), named PADRE for the ALPIDE architecture, but the author also contributed significantly to the assembly and verification of the chips. PADRE is the main research of the author. It is based on a hierarchical priority encoder circuit of four inputs and it is an alternative to the rolling-shutter read-out. The characterization of full custom designs were made by the author using analog simulations and the generation of digital models for the simulation chain needed for the functional verification process. All of this research presented in this document made the author understand how to design an ASIC from the conceptual design, production and fabrication phase.

The major challenge faced during this work using MAPS was the development of a read-out within the pixel. As a result, the PADRE read-out concept was implemented and verified in a small-scale prototype named pALPIDEss and the functionality as a pixel detector. This was verified in the laboratory with sources and beam test, being the first full operational MAPS sensor designed at CERN. Finally, the full-scale prototypes were designed implementing this read-out.

The PADRE read-out provides a fast-or signal, priority-encoded address, priority reset decoder and address bus propagation at the same time, providing the address of the fired pixel every clock cycle. The PADRE read-out generates fulfils the time requirement and data propagation below a clock period signal of 25 ns being faster and lower power than other MAPS read-out.

Besides small-scale prototypes, full-scale (15 mm & 30 mm) demonstrators have also been developed employing a novel hit driven read-out based on a custom version of PADRE circuit. A first full-scale prototype (pALPIDEfs) was developed in 2013 that was characterised by a very low integration time (few $\approx$ s due to its AC sensitive front-end), a very low matrix read-out time ($\approx \mu$s at the average hit density of the inner-layers after LS2 due to the hit driven architecture) and a very low power consumption, less than 80 mW cm$^{-2}$.

The pALPIDE2 sensor has demonstrated to be a very attractive option for deployment in the new ITS detector as its performance cannot be reached by prototypes based on the more traditional rolling shutter read-out designed in the same technology. It has now become the baseline option for the upgrade, with further development culminating in the final ALPIDE circuit. For this reason R&D on ALPIDE prototypes has continued with the aim to further optimise the sensor performance, especially in terms of dead time and to study solutions to other system integration aspects.

The bottlenecks in this architecture have also been identified. Generally, the bottleneck is either found from the pixel-to-End of column "EoC" data transport or at the output of the chip. Using different techniques, the bottleneck can be easily eliminated. However, in future applications, to avoid pile-up three storage elements were placed in the pixel circuitry with this architecture. When facing higher hit rates, it may not be feasible to transmit this data on-chip, even if the internal architecture could sustain the rates. More intelligent and more efficient data reduction techniques are thus, required.

The thesis has discussed and presented a hit-driven in-matrix zero suppression circuit named priority named the encoder. In particular, the thesis presents a solution for the ITS application requiring a pixel pitch of 29.24 $\mu$m and height of 26.88 $\mu$m were presented. The techniques presented, which are especially adapted for area and power limitations of mixed-signal pixel read-out ASICs, can be used to improve the efficiency of read-out architectures. The techniques presented here are also compatible with modern digital ASIC design techniques and standard cell design now making it possible to quickly port them into new CMOS technologies. As on-chip wire delays do not scale down similarly as gate delays when moving to newer CMOS technologies, the architectural techniques presented here have also addressed this problem by adding timing constraints in the integration phase.

Based on the simulations and experimental results, the latest ALPIDE circuit, the pALPDIE3B sensor, consumes less than 50 mW cm$^{-2}$ with throughput of 1.2 Gbps and an efficiency higher than 99.95% meeting the ALICE ITS specifications. The characterization of this chip validated working points for which the detection efficiency, position

resolution and fake hit rate are in line with, or even surpassing. This includes a sufficient operating margin after irradiation with an equivalent fluence of $1\times10^{13}$ 1 MeV $n_{eq}$ cm$^{-2}$. Moreover, this validate the time resolution of about 2 $\mu$s, fake-hit rate and position resolution. Table 4.4 summarized the ALPIDE designs specifications on integration time and power.

Another contribution of this thesis was the integration of circuits for the full-scale prototypes based in a top-down flow for TowerJazz 180 nm. Moreover, this circuit has a low Noise, charge coupled reduction between power domains. The front end is quite sensitive and it had been carefully shielded from digital activity. And finally, it generates the netlist files for full chip verification.

The ALPIDE is the first full-scale monolithic sensor with a sparsifying architecture similar to hybrid detectors, and it provides very low power consumption.

The optimization phase and prototype circuits designs are finished and the start of the mass production of the final pixel chip is planned for 2017. The full detector will be commissioned on the surface throughout 2019 and will be installed during the LS2 in 2020 in the ALICE cavern.

The pALPIDEss and full-scale prototypes were extensively tested and functional, hence proving the full functionality of the architecture, and that the ALPIDE is now in production and it will be installed during the LS2 in the ALICE cavern.

Table 6.1 summarizes, the chips deployed under the ITS upgrade program showing the type of solution applied per chip.

## 6.1   Future work

The pALPIDE4 chip will address and solve all problems in the characterization and qualification of the pALPIDE3B sensor. The dynamic power analysis of the pALPIDE3 sensor and measurements of the switching noise impose requirements on the data transmission unit. One technique to avoid the noise induction on digital power rail to

| Chip name | Solution applied |
|---|---|
| The pALPIDE_ss chip | Removed the leakage current in the parasitic diode. |
| | Suppressed the Extra charge collected by the pixel. |
| | Designed the first fully digital prototype with in-pixel discrimination and buffering, |
| | Sparsified read-out with zero suppression within the matrix. |
| The pALPIDE_fs chip | Disabling memories to reduce the power consumption. |
| | Optimized of sensitive layer and charge collection electrode. |
| | Reduced of the capacitance in the collection diode. |
| | Optimized the diode reset mechanism. |
| | Added Bonding pads over the matrix. |
| | Generated a Slow control interface for chip configuration. |
| The pALPIDE2 chip | Optimized of sensitive layer and charge collection electrode. |
| | Optimization of periphery read-out and digital circuit blocks. |
| | Optimized the diode or the pMOS reset mechanism. |
| | Optimized the shaping time. |
| | No high-speed output link: Added a 40 Mbit/s DDR instead of the final 1.2Gbit/s. |
| | Changed the PADS over logic and constructed of ITS module prototypes. |
| The pALPIDE3 chip | New Chip size. |
| | Reduced of the of the dynamic power due to the read-out. |
| | Designed a new front-end read-out. |
| | Duplicated of the CHIPID PADS. |
| | Generated a new front-end. |
| | Reduced of the capacitance in the collection diode. |
| | Optimized the pixel reset mechanism. |
| | Reduced of the Dead-time. |
| | Added Triple memory per pixel. |
| | Added High speed serializer. |
| | Optimized of sensitive layer and charge collection electrode. |
| | TMR was implemented in the core state machine and some sensitive logic. |
| | Implemented Clock gating. |
| | IB and OB read-out scenarios were implemented. |
| | Added an analog current and voltage bias monitoring. |
| | Added a Band-gap and temperature sensor. |
| The pALPIDE3B chip | Reduced the digital power shift for the high speed serializer. |
| | Added New power domain for the serializer |
| | Optimized the M5 layer routing under the PADS over the Matrix |
| | Optimized of sensitive layer and charge collection electrode |
| | Final interface, allowed construction of ITS module prototypes. |

**Table 6.1:** Overview all pALPIDE chips deployed for the ITS upgrade.

the transition unit, is to create a new power domain, where it must be propagated from the power pads position in this application in the Matrix to the transmission unit position. Also, this switching noise is coming from the activation/commutation of the global nets propagated inside of the PE. The use of these global nets must be switched with a skew of a clock cycle. Moreover, the full parallel read-out of all the regions generates a current peak affecting power distribution and induces noise in the digital power rail. One solution would be the skew of the regions read-out or only select a few to be read out. The triplication of the reset logic and applying of TMR to all sequential logic to avoid SEUs and SELs, that affects the correct operation and the functionality of the full circuit. All of these modifications will be implemented in the pALPIDE4 chip, the final prototype to be submitted and fabricated to be the candidate to be implemented in the ALICE ITS upgrade.

The performance requirements for MAPS chips are constantly increasing. This read-out chips leads to more complex and better performing read-out chips are required. The stitching technology to obtain a large CMOS sensors exists today. In ALICE it could be used for the inner layers, where it would give a factor 2 of improvement in impact parameter resolution. Furthermore, the OrthoPixel architecture or moreover a mixed architecture based on a token ring and priority encoder would be feasible to be implemented in a large area with a high interaction rate, suitable for the ALICE ITS. Even though the architectural read-out optimization offers some possibilities for improving the performance, eventually one clearly feasible approach is to adapt the ALPIDE priority encoder, and use peripheral circuitry. The approach with peripheral circuitry only on one side is more elegant, but requires more development by making a read-out chip more programmable.

The ATLAS experiment has started a R&D program with new state-of-the-art technologies for its new vertex detector named the Inner Tracker detector (ITK) and for future precision tracking detectors. One of the possible technologies to be included in this research is the TowerJazz 180 nm CMOS process and the architecture ALPIDE Matrix read-out implemented for ALICE ITS upgrade. The results of

these R&D programs could drive the future of vertexing detectors and the suitable CMOS technologies that could be implemented in HEP.

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