Study and design of the front-end and readout electronics for the tracking plane in the NEXT experiment

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Abstract

The NEXT experiment is one of the most innovative ones looking for the neutrinoless double beta decay, which finding will answer one of the most important questions in the last years physics: is the neutrino its own antiparticle? Or in other words, is it a Majorana particle?

With that purpose NEXT uses a TPC (Time Projection Chamber) filled with enriched xenon gas at high pressure, and two photosensors planes, one on each end. The first plane contains PMTs (PhotoMultiplier Tube), that collect the light emitted by the xenon when an event happens and precisely measures its energy. The second plane is a SiPM (Silicon PhotoMultiplier) matrix that allows to 3D-reconstruct the event track. Both planes together allows NEXT to have a great background rejection, which makes a difference with the other experiments aiming for the neutrinoless double beta decay. In addition, SiPMs are a new technology which nowadays is evolving to, in the future, displace the classical PMTs. For that reason the study of these sensors starts from zero, as there were not previous uses as pixel-tracking, and lead a new path in the physics detectors, for both high and low energy.

This thesis is focused on the study and design of the electronics involving the tracking plane, which includes some technical solutions related also with mechanical issues. From the sensors placed inside the detector, the SiPMs, to the front-end electronic boards, there are few elements on the chain; as the support boards for the SiPMs which must satisfy severe outgassing and radiopurity levels. Also the inner and outer cabling has been designed, focusing on obtaining the best signal-noise ratio; and also the feedthrough for the tracking plane, which

solved at low cost the huge problem of taking out about 4000 lines from the pressurized xenon to the outside.

Finally, one of the most important elements on this chain and the one that this thesis is focused on, is the front-end board. Starting with the experience acquired with the first prototype, NEXT-DEMO, the electronics have been improved, able to condition, integrate and digitize the signals from all the tracking plane SiPMs; allowing the further acquisition and processing through an ATCA-based system (Advanced Telecommunications Computing Architecture).

All the elements designed have been produced and assembled on the NEW detector, a large-scale prototype of the final detector, placed at the *Laboratorio Subterráneo de Canfranc*, an underground laboratory at the aragonese Pyrenee.

Resumen

El experimento NEXT es uno de los más innovadores en la búsqueda de la desintegración doble beta sin neutrinos, cuyo hallazgo daría con la respuesta a una de las cuestiones más importantes de la física en los últimos años: ¿es el neutrino su propia antipartícula? O dicho de otro modo, ¿es una partícula de Majorana?

Para ello NEXT hace uso de una TPC (Time Projection Chamber) llena de gas xenón enriquecido a alta presión, y con dos planos de fotosensores, uno en cada extremo. El primero de ellos está formado por PMTs (Photo Multiplier Tube), que recogen la luz generada por el xenón cuando ocurre un evento, y miden la energía de éste. El segundo consiste en una matriz de SiPMs (Silicon PhotoMultipliers) que permiten reconstruir tridimensionalmente la traza de dicho evento. El conjunto de ambos planos de fotosensores otorga al experimento NEXT un gran rechazo a eventos de fondo, lo que marca la diferencia con otros experimentos en busca de la desintegración doble beta sin neutrinos. Además, los SiPMs son una tecnología de reciente aparición que en la actualidad está evolucionando a grandes pasos para, en un futuro, desplazar a los fotomultiplicadores clásicos. Por ello el estudio de estos fotosensores parte prácticamente desde cero, ya que no existen aplicaciones previas de su uso como pixel-tracking, y ha permitido abrir un nuevo camino en los detectores de física, tanto de alta como baja energía.

Esta tesis doctoral tiene como objetivo el estudio y diseño de la electrónica involucrada en el plano de reconstrucción de trazas, y que involucran en menor medida dar solución a problemas técnicos de aspecto mecánico. Partiendo

de los sensores ubicados dentro del detector, los SiPMs, hasta las tarjetas de front-end, se incluyen varios elementos de la cadena; como son las tarjetas empleadas como soporte para los SiPM en el interior de la cámara, las cuáles deben cumplir rigurosas medidas de radiopureza y degasificación. También se ha diseñado el cableado tanto interno como externo, haciendo énfasis en conseguir la mayor relación posible señal-ruido; y el pasamuros específico para el plano de reconstrucción de trazas, el cual ha resuelto a bajo coste el problema de extraer casi 4000 líneas desde la zona de xenón a alta presión hasta el exterior.

Por último, uno de los elementos más importantes de esta cadena y en el cuál se centra principalmente esta tesis, es la tarjeta de front-end. Partiendo de la experiencia adquirida del primer prototipo del experimento, NEXT-DEMO, se ha perfeccionado una electrónica capaz de tratar, integrar y adquirir las señales de todos los SiPM del plano de reconstrucción de trazas, permitiendo su posterior adquisición y procesado mediante un sistema basado en la estructura ATCA (Advanced Telecommunications Computing Architecture).

Todos los elementos diseñados han sido ensamblados y puestos en marcha en el detector NEW, un prototipo a gran escala del detector final, que está ubicado en el Laboratorio Subterráneo de Canfranc, en el Pirineo Aragonés.

Resum

L'experiment NEXT és un dels més innovadors en la recerca de la desintegració doble beta sense neutrins, i aquesta troballa donaria amb la resposta a una de les qüestions més importants de la física en els últims anys: és el neutrí la seua pròpia antipartícula? O dit d'una altra manera, és una partícula de Majorana?

Per açò NEXT fa ús d'una TPC (Time Projection Chamber) plena de gas xenó enriquit a alta presió, i amb dos plànols de fotosensors, un a cada extrem. El primer d'ells està format per PMTs (Photo Multiplier Tube), que arrepleguen la llum generada pel xenó quan ocorre un esdeveniment, i mesuren l'energía d'aquest. El segon consisteix en una matriu de SiPMs (Silicon PhotoMultipliers) que permeten reconstruir tridimensionalment la traça d'aquest esdeveniment. El conjunt de tots dos plànols de fotosensors atorga a l'experiment NEXT un gran rebuig a esdeveniments de fons, la qual cosa marca la diferència amb altres experiments a la recerca de la desintegració doble beta sense neutrins. A més, els SiPMs són una tecnología de recent aparició que en l'actualitat està evolucionant a grans passos per a, en un futur, desplaçar als fotomultiplicadors clàssics. Per això l'estudi d'aquests fotosensors part pràcticament des de zero, ja que no hi ha aplicacions prèvies del seu ús com a pixel-tracking, i ha permés obrir un nou camí en els detectors de física, tant d'alta com de baixa energia.

Aquesta tesi doctoral té com a objectiu l'estudi i diseny de l'electrònica involucrada en el plànol de reconstrucció de traces, i que involucra en menor mesura donar solució a problemes tècnics d'aspecte mecànic. Partint dels sensors situats dins del detector, els SiPMs, fins a les targetes de front-end, s'inclouen diversos elements de la cadena; com són les targetes emprades com a

suport per als SiPMs a l'interior de la càmera, les quals han de complir rigoroses mesures de radioactivitat i degasificació. També s'ha disenyat el cablejat tant intern com extern, fent èmfasi en aconseguir la major relació possible senyal-soroll; i el passamurs específic per al plànol de reconstrucció de traces, el qual ha resolt a baix cost el problema d'extraure quasi 4000 línies des de la zona de xenó a alta presió fins a l'exterior.

Finalment, un dels elements més importants d'aquesta cadena i en el qual es centra principalment aquesta tesi, és la targeta de front-end. Partint de l'experiència adquirida del primer prototip de l'experiment, NEXT-DEMO, s'ha perfeccionat una electrònica capaç de tractar, integrar i adquirir les senyals de tots els SiPM del plànol de reconstrucció de traces, permetent la seua posterior adquisició i processament mitjançant un sistema basat en l'estructura ATCA (Advanced Telecommunications Computing Architecture).

Tots els elements disenyats han sigut muntats i engegats en el detector NEW, un prototip a gran escala del detector final, que està situat en el *Laboratorio Subterráneo de Canfranc*, al Pirineu Aragonès.

Agradecimientos

Es difícil dar las gracias adecuadamente, y puede que ese sea precísamente el motivo por el cual no lo hacemos tan a menudo como deberíamos. Dar las gracias con motivo de esta tesis no es únicamente cuestión de agradecer a esas personas que han estado ahí durante la redacción de la misma, sino a todas aquellas personas que, de un modo u otro, han influido en mi vida encaminándola hacia donde estoy ahora. A todas esas personas con las que me he cruzado a lo largo de mi vida y han hecho de mí la persona que soy. No voy a dar nombres, pues la lista sería interminable. Dejo a decisión de cada uno darse o no por aludido:

A aquellos que han creído en mí, por darme la confianza necesaria para seguir adelante; y también a aquellos que no lo hicieron, por darme motivos para superarme. A quienes me han educado, y también a quienes me han enseñado. A los que me han dado la oportunidad de demostrar de qué soy capaz; pero también a los que no, pues me enseñaron que las oportunidades hay que ganárselas. A las personas que me han hecho pasar buenos momentos y han dado sentido a mi vida; y a las que me enseñaron que los malos momentos te hacen valorar más lo que tienes. A quienes me han dado lo que tengo; y no menos a quienes me han hecho ganármelo y aprender el valor de las cosas. A aquellos que me han ayudado a estar dónde estoy, y a aquellos que todavía me ayudan. A los que me han acompañado durante gran parte del camino y siguen ahí; y a los que me acompañaron en su día, y jamás olvidaré.

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Contents

Introduction

The Neutrino Experiment with a Xenon TPC (NEXT) started in 2008, as the first experiment with tracking reconstruction in the neutrinoless double-beta decay search race. Some time and prototyping later, the SiPM (Silicon PhotoMultipliers) were chosen as the photosensors for the pixel tracking. This decision implied a lot of hard work and studies which the NEXT collaboration carried out, as the SiPM were still (and are) a novel technology.

The student stepped in the collaboration in summer 2010, and since then has been working on the experiment's electronics group. This implies knowledge in all the areas developed almost since the beginning, and a lot of experience acquired during the first prototype assembly, NEXT-DEMO. Then, as responsible of the electronics group, started to work on the next step of the tracking plane: the NEW detector, a mid-scale prototype. All the experience gained in NEXT-DEMO helped to evolve and improve all the elements of the detector, but also the size of this new tracking plane implied new challenges that must be solved for further scaling in the future and final detector: NEXT-100.

This thesis describes the studies and work done in the tracking plane, focused in the NEW detector, which rough scheme can be seen on figure 1. From the beginning the whole system needed to be redesigned, as the detector must be radiopure to have enough background rejection, and its size implies almost 1800 photosensors in the tracking plane, compared to the $\sim$ 250 working on NEXT-DEMO.

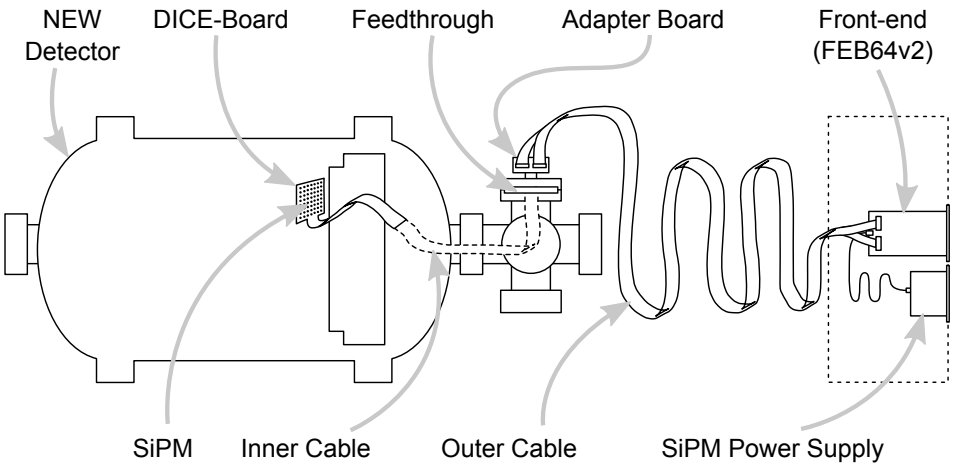

Figure 1: *NEW Detector tracking plane scheme. The full signal chain from the silicon photomultipliers to the front-end electronics is shown.*

The proposed objectives for this thesis were:

- Study of the silicon photomultipliers properties for different models and manufacturers, like gain dependence with bias voltage and temperature, dark count and noise.
- Design and production of a SiPM bias supply scalable for NEXT-100.
- Design and production of a front-end for the NEXT experiment silicon photomultipliers, fitting all the performance required.
- Design, production and installation of the SiPM carrier boards.
- Study of the NEXT experiment ground system.

Chapter 1 summarizes the NEXT experiment target, evolution, status and future. An introduction to neutrinoless double beta decay physics helps to understand the concept of the experiment and the implication on the physic research areas. Also the silicon photomultipliers are described in detail; its structure, working principle and performance.

Chapter 2 focuses on the NEXT-DEMO tracking plane, the first SiPM pixel tracking system. It describes the whole chain of electronics, the different stages of the prototype and the first front-end electronics boards. The design requirements are also described, together with the status of the art in SiPM electronics. This acts as a base for further designs, like NEW.

Then, on Chapter 3, firsts front-end prototypes are shown and explained. This involved several studies and simulations, trying to understand the optimal performance for the new requirements on the tracking plane. This development lead into a differential scheme for the SiPM readout, which entail a full redesign of the cabling and support boards for the photodetectors.

After the conclusions on Chapter 3, Chapter 4 describes the final design for the front-end electronic boards. These ones are able to provide the bias voltage, read, integrate and digitize 64 SiPMs. Compared to the previous front-ends in NEXT-DEMO, this one allows the readout of 4 times more SiPMs in half the board area. Also, as described in the chapter, some performance improvements were achieved; like noise reduction, less power consumption per channel and less cost per channel.

Chapter 5 shows the design of the support board for the SiPMs: the DICE-Boards. Two designs were made during the tracking plane development, for single-ended signals and for differential ones, as both schemes were considered for the front-end electronics.

On Chapter 6 is described all the cabling done specifically for the SiPM tracking plane, both internal and external. This includes simulations and numerical studies, due to the difficulty of carrying the small current signals produced by the SiPMs along five meters of cable, in a noisy environment. A custom feedthrough was also designed, to solve the problem of supply the bias voltage and take out the signal of almost 1800 SiPMs. The solution came on a combination of electronics and mechanics, using a thick printed circuit board (PCB) as barrier between the pressurized xenon and the atmospheric air.

Chapter 7 describes the custom power supply unit designed by the collaboration, which allows to provide the bias voltage to the SiPMs and also stabilize the gain

of the whole tracking plane in a constant value, by compensating actively the bias as a function of temperature in the DICE-Boards.

Finally, Chapters 8 and 9 show the results and conclusions of the work described in this thesis. As said before, all the electronics and elements described here have been produced and installed in the NEW detector at the LSC (Laboratorio Subterráneo de Canfranc). By now, NEW has been successfully running for several weeks, and a huge amount of calibration data has been acquired.

Proudly, the tracking plane is fully functional; and hopefully it will be running for a long time.

"The scientific man does not aim at an immediate result. He does not expect that his advanced ideas will be readily taken up. His work is like that of the planter - for the future. His duty is to lay the foundation for those who are to come, and point the way."

– Nikola Tesla

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The NEXT Experiment

The Neutrino Experiment with a Xenon TPC (NEXT), will search for the neutrinoless double beta decay of ^{136}Xe using a radiopure high-pressure xenon gas Time Projection Chamber (TPC) filled with 100 *kg* of Xe enriched in its ^{136}Xe isotope. The experiment will be located at *Laboratorio Subterráneo de Canfranc*, which is carved into the rock at 850 meters deep below the Tobazo Mountain, on the Spanish side of the Pyrenees. NEXT will be the first large high-pressure gas TPC to use electroluminescence readout with SOFT (Separated, Optimized Functions TPC) technology. The following sections outline the most relevant aspects of the experiment, summarizing the neutrinoless double beta decay.

1.1 Neutrinoless Double Beta Decay ($\beta\beta0\nu$)

The Standard Model (SM) of Particle Physics is a theory concerning the electromagnetic, weak, and strong nuclear interactions, which describes fundamental properties of subatomic particles. This model works well in general, but there are still some missing pieces, many of them related to neutrinos. These particles are unique in many ways; in particular, their lack of color or electromagnetic charge means that, of the three fundamental forces described by the SM, they only feel the weak force. The Standard Model requires massless neutrinos in its basic formulation, but recent experiments on neutrino oscillations have demonstrated that they are massive particles, opening a new field of physics beyond the Standard Model.

Neutrinos might be the only particles having a Majorana mass term, forbidden to the other fermions, explaining the different mass scale of neutrinos compared with other fundamental particles. Experimental evidence of this phenomenon would have deep implications in physics and cosmology, since Majorana particles would be their own antiparticles as described by Majorana [Majorana 1937].

If neutrinos are Majorana particles, neutrinoless double beta decay ($\beta\beta0\nu$) could be observable and a mean to prove this hypothesis. The simple existence of $\beta\beta0\nu$ decay would prove that neutrinos are Majorana particles and that lepton number is not always conserved, while the decay rate would measure the Majorana neutrino mass.

Double beta decay ($\beta\beta$) is a very rare nuclear transition in which a nucleus with Z protons decays into a nucleus with $Z+2$ protons and same mass number A. It can only be observed in those isotopes where the β decay mode is forbidden due to the energy of the daughter nuclei being higher than the energy of the parent nuclei, or highly suppressed. If this condition is fulfilled, two simultaneous β decays are possible.

Two $\beta\beta$ decay modes are normally considered. The standard two neutrino double beta decay mode ($\beta\beta2\nu$) was proposed by Goeppert-Mayer in 1935

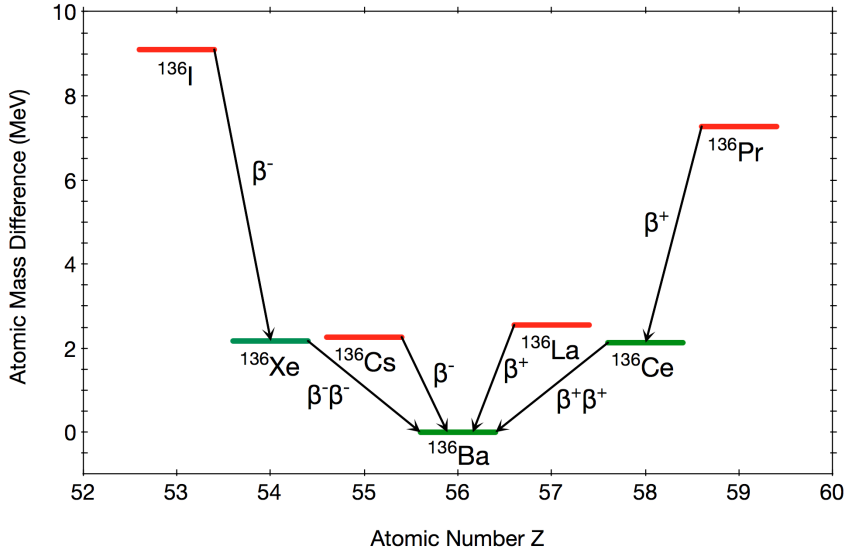


Figure 1.1: *Atomic masses of isotopes with $A = 136$ given as differences with respect to the most bound isotope, ^{136}Ba. The red levels indicate odd-odd nuclides, whereas the green indicate even-even ones. The arrows show the type of nuclear transition connecting the levels. Double beta (either plus or minus) transitions are possible because the intermediate state ($\Delta Z = \pm 1$) is less bound, forbidding the beta decay [Justo Martín-Albo 2015].*

[Goeppert-Mayer 1935] and has been observed in several nuclei, where an anti-neutrino associated to each electron is emitted. This process has typical lifetimes on the order of $10^{18} - 10^{21}$ years.

In the neutrinoless double beta decay mode ($\beta\beta0\nu$) the electrons carry essentially all the energy released in the decay. This process, which was postulated by Furry in 1939 [Furry 1939] and has not been observed yet, is forbidden in the Standard Model of Particle Physics. The Feynman diagrams for both possible decays are represented on figure 1.2.

Only if neutrinos are massive Majorana particles, and therefore their own antiparticles, $\beta\beta0\nu$ can take place. The anti-neutrino created in a vertex from one β decay virtually propagates to the other vertex, where it acts as a neutrino producing an electron via inverse beta decay. As the neutrino acts in a vertex as a neutrino and in the other as an anti-neutrino, this process is only possible

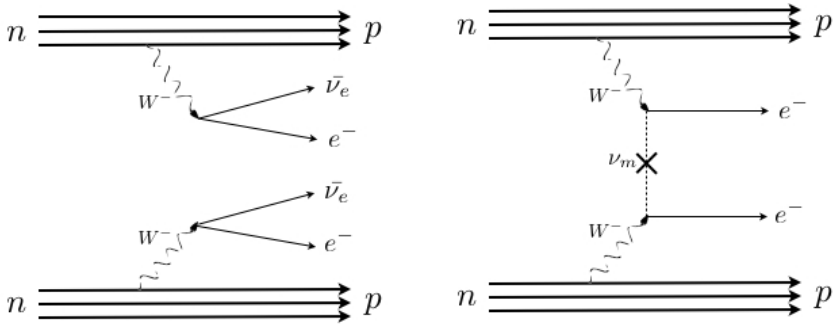


Figure 1.2: *Feynman diagram for the $\beta\beta 2\nu$ (left) and the $\beta\beta 0\nu$ (right).*

if both particles are the same. Additionally, the observation would demonstrate that total lepton number is violated in physical phenomena, an observation that could be linked to the cosmic asymmetry between matter and antimatter through the process known as leptogenesis.

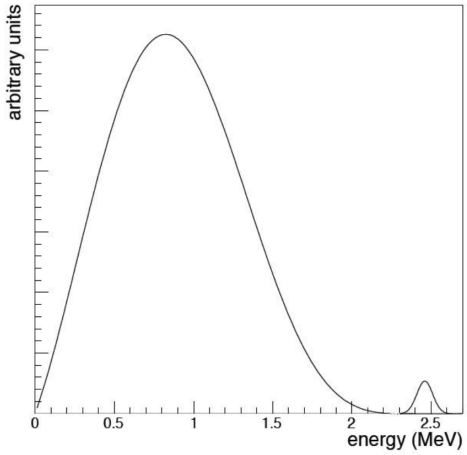


Figure 1.3: *Energy spectrum of the electrons emitted in the $\beta\beta$ decay of ^{136}Xe, as seen with a 1% FWHM energy resolution at $Q_{\beta\beta}$. The left peak corresponds to the $\beta\beta 2\nu$ decay, while the right peak, centered at $Q_{\beta\beta} = 2458\ keV$, corresponds to the $\beta\beta 0\nu$. The normalization scale between the two peaks is arbitrary.*

In the case of $\beta\beta0\nu$, the sum of the kinetic energies of the two released electrons is always the same, and corresponds to the mass difference between the parent and the daughter nuclei: $Q_{\beta\beta} \equiv M(Z,A) - M(Z+2,A)$. However, due to the finite energy resolution of any detector, $\beta\beta0\nu$ events are reconstructed within a non-zero energy range centered around $Q_{\beta\beta}$, typically following a gaussian distribution, as shown in figure 1.3. Other processes occurring in the detector can fall in that region of energies, thus becoming a background and compromising drastically the experiment's expected sensitivity to the effective Majorana neutrino mass ($m_{\beta\beta}$).

$\beta\beta$ *Experiments*

The main goal of basically all double beta decay experiments is to measure the total energy of the radiation emitted by a $\beta\beta$ source. In a neutrinoless double beta decay, the sum of the energies of the two emitted electrons is constant and equal to the mass difference between the parent and the daughter atoms ($Q_{\beta\beta}$). Any experiment hoping to measure the $\beta\beta0\nu$ half-life must be able to count the number of events at this energy due to $\beta\beta0\nu$. However, the measurement is limited by the experimental sensitivity of the detector employed.

Natural fluctuations and detector effects combine to smear the energy response and backgrounds from naturally occurring radioisotopes can pollute the energy region. For that reason, the materials with which the detector is built must be selected carefully to reduce the natural radioactivity present in all materials. In addition, double beta decay experiments must be placed at underground facilities, in order to reduce the background levels from atmospheric radiation. Finally, the intrinsic background from the standard two neutrino double beta decay mode, which has a continuous energy spectrum, can be problematic if the energy resolution is not very good.

Three experiments of the present generation are taking data already. On the one hand, the GERDA experiment [Lehnert 2014] looks for the neutrinoless double beta decay of ^{76}Ge at *Laboratori Nazionale del Gran Sasso*. In GERDA, high purity germanium detectors (HPGe) are arranged in strings and mounted in special low-mass holders made of ultra-pure copper and PTFE. The strings are

suspended inside a vacuum-insulated stainless steel cryostat of 4.2 m diameter and 8.9 m height filled with 64 m^3 of liquid argon. A copper lining 6 cm thick covers the inner cylindrical shell of the cryostat. The cryostat is placed in a 590 m^3 water tank instrumented with PMTs which serves as a Cherenkov muon veto as well as a gamma and neutron shield. The GERDA Collaboration has published a measurement of the $\beta\beta2\nu$ half-life of $T^{2\nu}_{1/2}(^{76}Ge) = (1.926 \pm 0.095) \times 10^{21}$ years [Agostini et al. 2015] and a limit on the $\beta\beta0\nu$ half-life, $T^{0\nu}_{1/2}(^{76}Ge) > 5.3 \times 10^{25}$ years (90% C.L.) [The GERDA Collaboration 2017].

On the other hand, there are xenon-based detectors like KamLAND-Zen [Gando et al. 2013], a transparent nylon-based balloon with 3.08 m diameter, containing 13 tons of liquid scintillator loaded with 320 kg of xenon (enriched to 91% in ^{136}Xe). The balloon is suspended by film straps at the center of a stainless steel spherical vessel with 1879 photomultiplier tubes mounted on the inner surface, which record the scintillation light generated by $\beta\beta$ events occurring in the detector. With this configuration it has achieved an extrapolated energy resolution of 9.9% FWHM at the $Q_{\beta\beta}$ value of ^{136}Xe, publishing recently a limit on the half-life of $\beta\beta0\nu$ of $T^{0\nu}_{1/2}(^{136}Xe) > 1.07 \times 10^{26}$ years.

In parallel, the EXO Collaboration has published a limit on the half- life of $\beta\beta0\nu$ of $T^{0\nu}_{1/2}(^{136}Xe) > 1.1 \times 10^{25}$ years [The EXO-200 Collaboration 2014] using the EXO-200 detector, a symmetric TPC filled with 110 kg of liquid xenon (enriched to 80.6% in ^{136}Xe). In EXO-200, ionization charges in the xenon created by charged particles drift towards the two anodes of the TPC due to the presence of an electric field. Events in the chamber are reconstructed by a pair of crossed wire planes which measure their amplitude and transverse coordinates, and an array of avalanche photodiodes (APDs), which detect the 178 nm xenon scintillation light. The sides of the chamber are covered with teflon sheets that act as VUV reflectors, improving the light collection. The EXO-200 detector has achieved an energy resolution of 4% FWHM at the $Q_{\beta\beta}$ value of ^{136}Xe.

In the following section, a new neutrinoless double beta decay experiment is introduced: the NEXT experiment, which will search for neutrinoless double beta decay of ^{136}Xe at *Laboratorio Subterráneo de Canfranc* with the NEXT-100 detector. Such a detector, containing 100 kg of ^{136}Xe, thanks to its excellent

and demonstrated energy resolution, together with a high efficiency background rejection, will be one of the leading experiment in the field, exploring the region of neutrino mass lower than 100 meV.

1.2 NEXT Concept

The NEXT detector uses the Separated, Optimized Functions TPC (SOFT) concept (figure 1.4), which consists in the idea that tracking and energy measurements are performed separately [Nygren 2009]. Using this concept, both energy resolution and tracking described in the previous sections can be achieved. When a charged particle interacts with the high pressure xenon, ionizes and excites its atoms. The excitation energy results is the prompt emission of VUV ($\sim$ 172 nm) scintillation light (S1) which is detected by a plane of PMTs located behind a transparent cathode in one side of the TPC and giving the start-of-event (t_0).

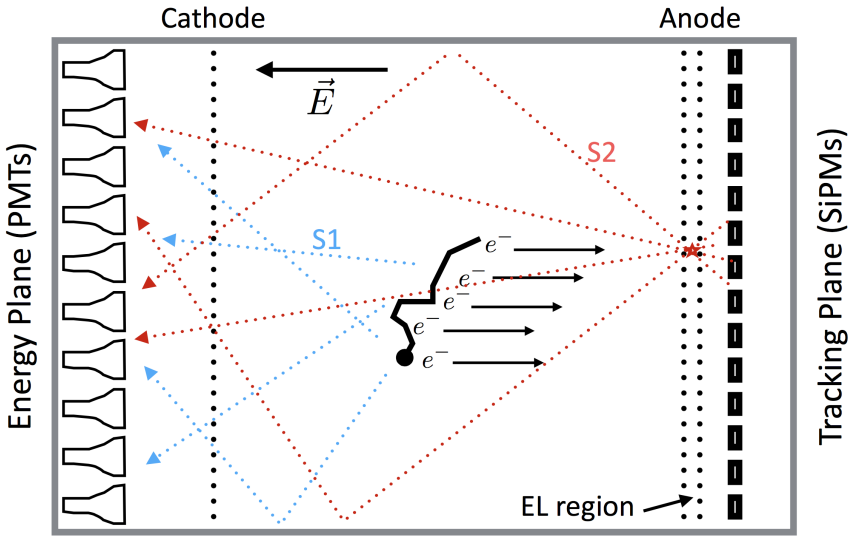


Figure 1.4: *The Separated, Optimized Functions TPC (SOFT) concept. EL (Electroluminescence) light generated at the anode is recorded in the photosensor plane right behind it and used for tracking. It is also recorded in the photosensor plane behind the transparent cathode and used for a precise energy measurement.*

The ionization electrons left by the passage of the charged particle are prevented from recombining by an electric field which causes them to drift towards the TPC anode where they enter a region of more intense electric field between two meshes. In this region they are accelerated and induce the production of secondary excitation of xenon atoms without secondary ionization, by electroluminescence (EL) amplification. The EL light (S2) is generated a few millimeters away from an array of Silicon Photomultipliers (SiPMs), which form the tracking plane, providing the track of the event. As EL light is emitted isotropically, roughly half will reach the PMT plane, since now energy plane, giving a precise energy measurement. The advantage of the separate functions for the two measurements is the decoupling of the operational configuration between the two planes of sensors, which gives more freedom to modify the operational parameters of each set, optimizing the performance of the whole detector.

1.3 NEXT-DEMO

NEXT-DEMO [Álvarez et al. 2013a], shown in figure 1.5, is a high-pressure xenon electroluminescent TPC implementing the NEXT detector concept described above. Its active volume is 30 *cm* long and 30 *cm* diameter. A tube of hexagonal cross section made of PTFE is inserted into the active volume to improve the light collection. The TPC is housed in a stainless-steel pressure vessel that can withstand up to 15 *bar*. Natural xenon circulates in a closed loop through the vessel and a system of purifying filters. The detector is not radiopure and is not shielded against natural radioactivity. It is installed in a semi-clean room (see figure 1.6) at the *Instituto de Física Corpuscular* (IFIC), in Valencia, Spain.

The main objective of NEXT-DEMO was the validation of the NEXT-100 design. More specifically, the goals of the prototype were the following: (a) to demonstrate good energy resolution in a large active volume; (b) to reconstruct the topological signature of electrons in high-pressure xenon gas (HPXe); (c) to test long drift lengths and high voltages; (d) to understand gas recirculation and purification in a large volume, including operation stability and robustness

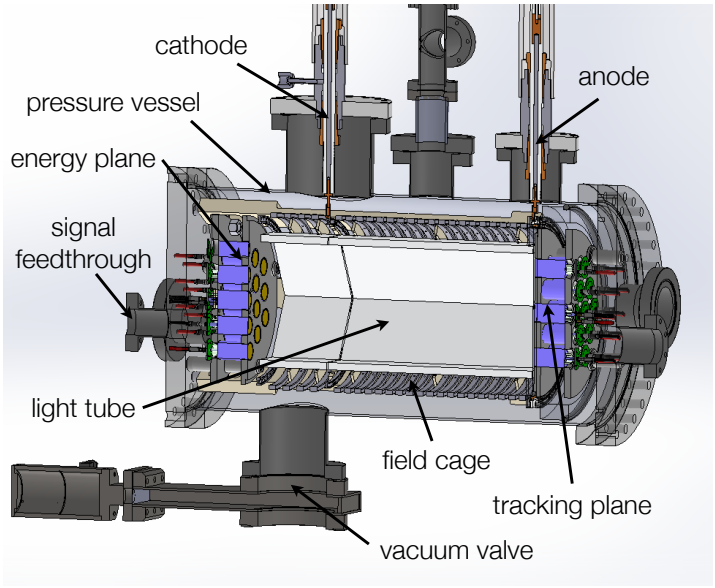


Figure 1.5: *Cross-section drawing of the NEXT-DEMO detector with all major parts labelled.*

against leaks; and (e) to understand the collection of light and the use of wavelength shifters (WLS).

The initial operation of NEXT-DEMO had a tracking plane implemented using 19 pressure-resistant photomultipliers, identical to those used in the energy plane but operated at a lower gain. Instrumenting the tracking plane with PMTs — unlike NEW and NEXT-100, which will use SiPMs — during the first period simplified the initial commissioning, debugging and operation of the detector due to the smaller number of readout channels (19 PMTs in contrast to the 248 SiPMs projected for the second phase of NEXT-DEMO) and their intrinsic sensitivity to the UV light emitted by xenon. Later the tracking plane was updated, and the PMTs were replaced by SiPMs as will be detailed on Chapter 2.

The detector response was studied under two different conditions: an ultraviolet configuration (UVC) in which the PTFE light tube had no coating; and a blue configuration (BC) in which the panels were coated with tetraphenyl butadiene

Figure 1.6: *The NEXT-DEMO detector and ancillary systems (gas system, front-end electronics and DAQ) in their location at a semi-clean room at IFIC.*

(TPB), a wavelength shifter, in order to study the possible improvement in light collection.

Gas system

The functions of the gas system of NEXT-DEMO are the evacuation of the detector, its pressurization and depressurization with xenon (and argon), and the recirculation of the gas through purification filters. A schematic of the system is shown on figure 1.7.

The standard procedure during normal operation of the detector starts with the evacuation of the vessel to vacuum levels around 10^{-5} *mbar*, followed by an argon purge. A second vacuum step exhausts the argon from the system. The detector is then filled with xenon gas to pressures up to 15 *bar*. The xenon can be cryogenically recovered to a stainless-steel bottle connected to the gas system

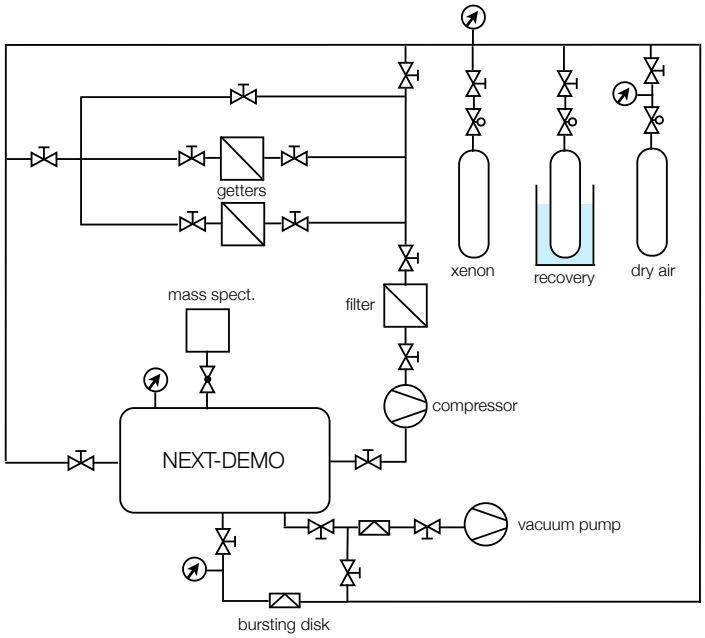


Figure 1.7: *Simplified schematic of the gas system of NEXT-DEMO.*

by simply immersing this in a dewar filled with liquid nitrogen. The pressure regulator of the bottle is fully opened to allow the xenon gas to flow inside it (due to the temperature difference) and freeze.

The vacuum pumping system consists of a roughing pump (*Edwards XDS5* scroll vacuum pump) and a turbo molecular pump (*Pfeiffer HiPace 300*). Vacuum pressures better than 10^{-7} *mbar* have been obtained after pumping out the detector for several days. The recirculation loop is powered by an oil-less, single-diaphragm compressor (*KNF PJ24999-2400*) with a nominal flow of 100 standard liters per minute. This translates to an approximate flow of 10 liters per minute at 10 *bar*, thus recirculating the full volume of NEXT-DEMO ($\sim$ 45 *L*) in about 5 minutes. The gas system is equipped with both room-temperature (*SAES MC50*) and heated *getters* (*SAES PS4-MT15*) that remove electronegative impurities (O_2, H_2O, etc.) from the xenon. All the gas piping, save for the inlet gas hoses

and getter fittings, are 1/2 inch diameter with VCR[1] fittings. A set of pressure relief valves (with different settings for the various parts of the system) and a bursting disk in the vacuum system protect the equipment and personnel from overpressure hazards.

The operation of the gas system has been, in general, very stable. The detector has run without interruption for long periods of up to 6 weeks with no leaks and continuous purification of the gas.

Pressure vessel

NEXT-DEMO pressure vessel is a stainless-steel (grade 304L) cylindrical shell, 3 *mm* thick, 30 *cm* diameter and 60 *cm* length, welded to CF[2] flanges on both ends. The two end-caps are 3 *cm* thick plates with standard CF knife-edge flanges. Flat copper gaskets are used as sealing. The vessel was certified to 15 *bar* operational pressure. It was designed at IFIC and built by *Trinos Vacuum Systems*, a local manufacturer. Additional improvements — including the support structure and a rail system to open and move the end-caps — have been made using the mechanical workshop at IFIC.

The side of the chamber includes 8 CF40 half-nipples. One set of 4 is located in the horizontal plane while the other is displaced towards the underside with respect to the first set by 60°. These contain radioactive source ports used for calibration of the TPC. The ports are made by welding a 0.5 *mm* blank at the end of a 12 *mm* liquid feedthrough. On top of the vessel and along the vertical plane there are three additional half-nipples (CF130, CF67 and CF80) used for high-voltage feeding and connection to a mass spectrometer (through a leak valve). On the opposite side, at the bottom, a CF100 port connects the pressure vessel to the vacuum pumping system. A guillotine valve closes this connection when the vessel is under pressure. The end-caps include several CF ports for the connections to the gas recirculation loop and for the feedthroughs (power and signal) of the PMT planes.

[1] VCR are metal gasket face seal fittings commonly used in pressurized gas systems which require good tightness levels.

[2] CF flanges use a copper gasket and knife-edge flange to achieve an ultrahigh vacuum seal. A number following this designation indicates the tube inner diameter in millimeters.

Time projection chamber

Three metallic wire grids — referred to as *cathode*, *gate* and *anode* — define the two active regions of the chamber (see figure 1.8): the 30 *cm* long *drift region*, between cathode and gate; and the 0.5 *cm* long *EL region*, between gate and anode. Gate and anode were built using stainless-steel meshes with 88% open area (30 μm diameter wires, 50 wires/inch) clamped in a tongue-and-groove circular frame with a tensioning ring that is torqued with set screws to achieve the optimum tension. The cathode was built in a similar fashion by clamping parallel wires 1 *cm* apart into another circular frame.

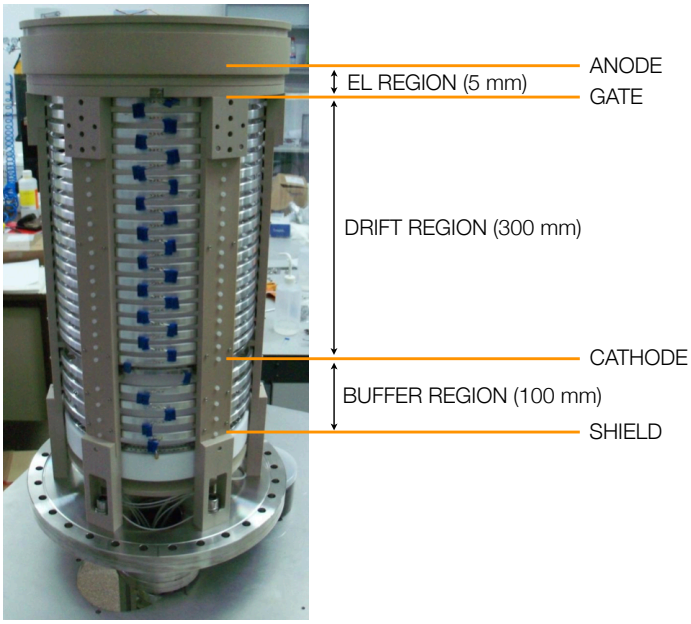


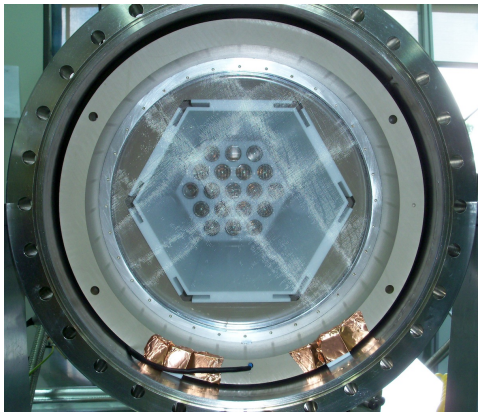
Figure 1.8: *External view of the time projection chamber mounted on one end-cap. The approximate positions of the different regions of the TPC are indicated.*

The electric field in the TPC is created by supplying a large negative voltage to the cathode and then degrading it across the drift region using a series of metallic rings of 30 *cm* diameter spaced 5 *mm* apart and connected via 0.5 $G\Omega$ resistors. The rings were manufactured by cutting and machining aluminum pipe. The gate is at negative voltage so that a moderate electric field — up to

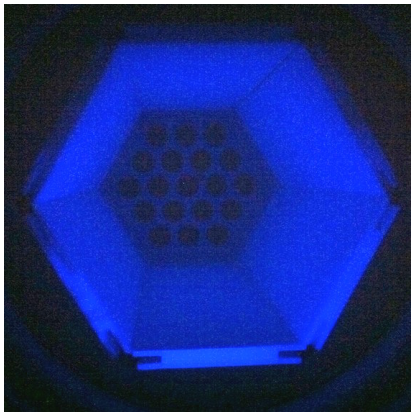
1 kV/cm — is created towards the cathode; and a high electric field — typically of 2.5 to 3 kV cm^{-1} bar^{-1} — is created between the gate and the anode, which is at ground. A *buffer region* of 10 cm between the cathode and the energy plane protects this from the high-voltage by degrading it safely to ground potential.

The high voltage is supplied to the cathode and the gate through custom-made high-voltage feed-throughs (HVFT) built pressing a stainless-steel rod into a Tefzel (a plastic with high dielectric strength) tube, which is then clamped using plastic ferrules to a CF flange. They have been tested to high vacuum and 100 kV without leaking or sparking.

A set of six panels made of PTFE (Teflon) are mounted inside the electric-field cage forming a *light tube* of hexagonal cross section (see figure 1.9) with and apothem length of 8 cm. PTFE is known to be an excellent reflector in a wide range of wavelengths [Silva et al. 2009], thus improving the light collection efficiency of the detector. In a second stage, the panels were vacuum-evaporated with TPB — which shifts the UV light emitted by xenon to blue ($\sim$ 430 nm) — in order to study the improvement in reflectivity and light detection. Figure 1.9b shows the light tube illuminated with a UV lamp after the coating.



(a) *The meshes of the EL region can be seen in the foreground, and in the background, at the end of the light tube, the PMTs of the energy plane are visible.*



(b) *The light tube of NEXT-DEMO illuminated with a UV lamp after being coated with TPB.*

Figure 1.9: *View of the light tube from the position of the tracking plane.*

Six bars manufactured from PEEK, a low outgassing plastic, hold the electric-field cage and the energy plane together. The whole structure is attached to one of the end-caps using screws, and introduced inside the vessel with the help of a rail system. All the TPC structures and the HVFT were designed and built by *Texas A&M*.

Detection planes

In NEXT-DEMO, the energy plane (see figure 1.10, left panel) is equipped with 19 *Hamamatsu R7378A* photomultiplier tubes. These are 1 *inch*, pressure-resistant (up to 20 *bar*) PMTs with acceptable quantum efficiency ($\sim$ 15%) in the VUV region. The resulting photocathode coverage of the energy plane is about 39%. The PMTs are inserted into a PTFE holder following an hexagonal pattern. A grid, known as *shield* and similar to the cathode but with the wires spaced 0.5 *cm* apart, is screwed on top of the holder and set to electrical ground. As explained above, this protects the PMTs from the high-voltage set in the cathode, and ensures that the electric field in the 10 *cm* buffer region is below the EL threshold.

As mentioned already, the first tracking plane of NEXT-DEMO detector also uses 19 *Hamamatsu R7378A* PMTs, as shown on figure 1.10 (right), but operated at lower gain. They are also held by a PTFE honeycomb, mirroring the energy plane. The PMT windows are located 2 *mm* away from the anode mesh. Position reconstruction is based on energy sharing between the PMTs, being therefore much better than the distance between PMTs (35 *mm* from center to center).

The PMTs are connected to custom-made electronic bases that are used as voltage dividers, and also allow the extraction of the signal induced in the PMTs. This requires a total of 38 cables (on each side, as both planes have PMTs) inside the pressure vessel connected via feedthroughs.

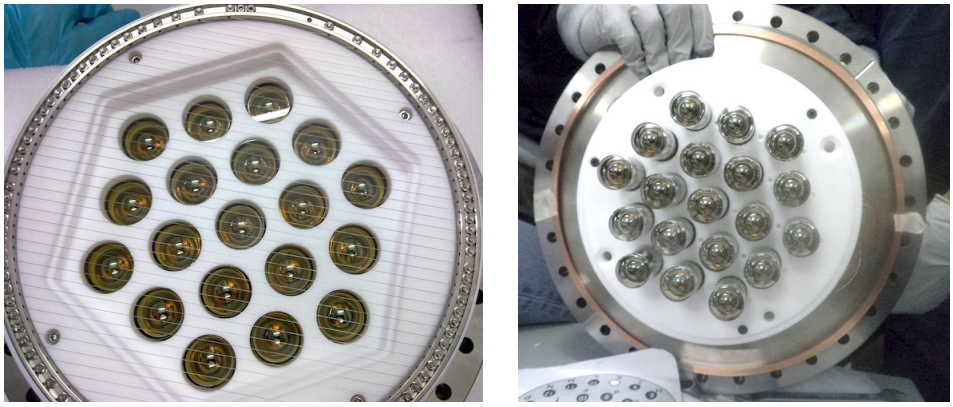


Figure 1.10: *The energy (left) and tracking (right) planes of NEXT-DEMO, each one equipped with 19 Hamamatsu R7378A PMTs.*

Electronics and DAQ

The two optical primary signals in the NEXT-DEMO detector are in very different scales, and the photomultipliers and their front-end electronics must be ready to handle both. Primary scintillation results in weak (a few photoelectrons per photomultiplier) and fast (the bulk of the signal comes in about 20 *ns*) signals, whereas the secondary scintillation — that is, the EL-amplified ionization — is intense (hundreds to thousands of photoelectrons per PMT) and slow (several microseconds long).

The gain of the PMTs in NEXT-DEMO was adjusted to around 5×10^6 for the energy plane to place the mean amplitude of a single photoelectron pulse well above electronic system noise, and approximately half that for the tracking plane since they record the direct secondary-scintillation light produced in the EL region and, as such, would have a higher probability of saturation at the same gain as those of the cathode.

The PMTs produce fast signals (less than 5 *ns* wide) making necessary the shaping and filtering of the detector output so that they match the sampling rate of the digitizer. This process also performs the important function of eliminating high frequency noise. A first low pass filter is implemented by

adding a capacitor and a resistor to the PMT base output. The charge integration capacitor shunting the anode stretches the pulse and reduces the primary signal peak voltage accordingly. The design uses a single amplification stage based on a fully differential amplifier *THS4511*, which features low noise (2 $nV/\sqrt{Hz}$) and provides enough gain to compensate for the attenuation in the following stage. Amplification is followed by a passive CRC filter with a cut-off frequency of 800 kHz. This filtering produces enough signal stretching to allow the acquisition of many samples per single photo-electron at 40 MHz. The front-end circuit for NEXT-DEMO was implemented in 7 channel boards and connected via HDMI cables to 12-bit 40 MHz digitizer cards. These digitizers are read out by the FPGA-based DAQ modules (FEC cards) that buffer, format and send event fragments to the DAQ PCs. As for the FEC card, the 16-channel digitizer add-in card was designed in a joint effort between CERN and the NEXT Collaboration within the RD-51 program [Martoiu et al. 2011]. These two cards are edge mounted to form a standard *6U* 220 *mm* Eurocard. An additional FEC module with a different plug-in card is used as trigger module. Besides forwarding a common clock and commands to all the DAQ modules, it receives trigger candidates from the DAQ modules, runs a trigger algorithm in the FPGA and distributes a trigger signal. The trigger electronics also accepts external triggers for detector calibration purposes.

As said before, the first tracking plane was implemented using the same PMTs than the energy plane, but the real tracking plane (TP) was intended to be with silicon photomultipliers (SiPMs) as NEXT-100 will be. As this thesis focuses on the SiPM TP, the NEXT-DEMO tracking plane with SiPMs is detailed on Chapter 2, and the electronics developed for it are explained on sections 2.3 and 3.1.

1.4 NEW

NEXT-DEMO was the prove of concept for the NEXT experiment, and still is a bench for tests that may extend our knowledge and understanding. And the so called NEXT-100 detector will be a radiopure detector that will start operation in *Laboratorio Subterráneo de Canfranc* (LSC) in the following years.

Between them we find the NEW (NExt-White) detector, which really is the first stage of the NEXT experiment (figure 1.11). The primary goal of NEW is to provide an intermediate step in the construction of the NEXT-100 detector that would allow the validation of the technological solutions proposed in the TDR [Álvarez et al. 2012c]. In addition, NEW would permit a measurement of the energy resolution at high energy, and the characterization of the 2-electron topological signature, by measuring the $\beta\beta 2\nu$ mode. Finally, NEW will permit a realistic assessment of the NEXT background model before the construction of the NEXT-100 detector.

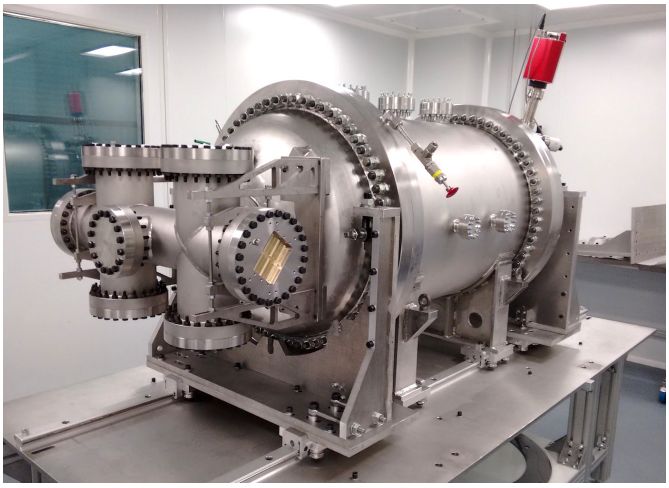


Figure 1.11: *NEW detector pressure vessel.*

Gas system

The gas system used for the NEW detector is almost the same than the one for NEXT-100, because both detectors have the same gas requirements except, of course, for the volume. Thereby, once the NEXT-100 detector is ready, the only parts that we will need to change are the vessel and the recovery tanks.

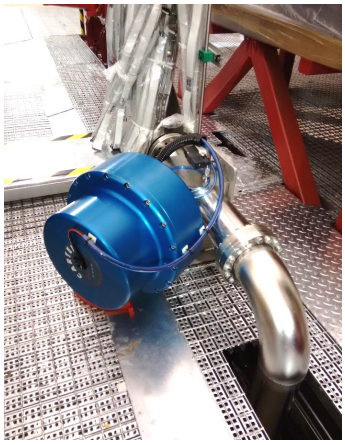
The functions of the gas system are the same described for NEXT-DEMO: pressurize and depressurize the system, recirculate and clean the gas, and evacuate the detector. However, the reliability that we have to acquire for NEW

and NEXT-100 is enormous due to the xenon cost, so the gas system has become a huge subsystem. So only some parts will be described.

This reliability level can not be achieved just with passive components, because there are some decisions that require a minimum of "intelligence". For this reason the gas system has been fully automated, using a *Compact RIO*; a FPGA-based PLC (Programmable Logic Controller) from *National Instruments*. The *Compact RIO* runs a real time *LabVIEW* variant, and has connections for monitoring the whole system (pressure gauges, vacuum gauges, valves, compressor, chiller...) and acts properly opening and closing the valves that control the gas flow. The *Compact RIO* is also connected to the Slow Control net, so all the parameters can be used to generate the proper reports, alarms and interact with the other elements connected to this net, explained later.

For the gas evacuation, the standard procedure allows to liquefy the gas stored in the whole system using a custom cryo-recovery bottle. This bottle is cooled carefully with liquid nitrogen, so the gas is recovered slowly by the depressurization created. Then, a vacuum pump is used to recover the residual gas in the vessel and the rest of the pipes.

(a) *Cryo-recovery bottle.*



(b) *Carten valve connected to the tracking plane side for evacuation.*

(c) *NEXT-100 vessel used as emergency recovery tank.*

Figure 1.12: *Different parts of the NEW gas system involved in gas recovery.*

But this method is too slow in case of emergency due to, for instance, a leak in the system. For that reason we needed the emergency recovery tank. This tank is kept at a moderate vacuum and its volume is calculated to hold the whole gas in the experiment at ~ 1 *bar*. Then, during normal operation, if an anomaly is detected and the gas on the experiment is compromised, a big *Carten* valve (figure 1.12b) is automatically opened and the gas flows quickly from the vessel to the tank through a 4" pipe. Once there, the gas can be redirected to the cryo-recovery bottle to safely store the gas. As shown on figure 1.12c, during the NEW phase the NEXT-100 vessel is used as recovery tank, as it has the desired volume for this function and allows the collaboration to save money.

The compressor for the gas recirculation (figure 1.13b) was built by the *SERA* company, according our specific requirements for pressure, reliability and leak rate. As the compressor has to be running continuously during the data taking periods, it needs to be cooled to guarantee the performance. For this reason it is connected to a chiller device, which is automatically controlled by the *Compact RIO* each time the compressor is running.

(a) *Gas system frame with the main components.*

(b) *Compressor.*

(c) *Compact RIO cabinet.*

Figure 1.13: *Different parts of the NEW gas system involved in gas recirculation.*

On figure 1.13a the gas system frame is shown. Here are placed most of the manual valves, which are the ones that are too critical to rely on an automated system, lot of pipes to redirect the gas flow and the getters. This getters are

used, same as in NEXT-DEMO, to clean the gas from impurities that deteriorate the energy measurement in the detector. Two types of getters are used: the cold getters, which clean the gas from O_2, H_2O, CO, H_2, volatile acids, organics, refractory compounds and volatile bases; and the hot getter, which outlet impurity levels for O_2, H_2O, CO, CO_2, H_2, N_2 and CH_4 are reduced to low parts per billion (ppb) levels or below.

Also for gas cleanliness purpose, several vacuum pumps are distributed and connected at some points of the gas system. This allows to have the whole gas system at vacuum, which is desirable to clean all the pipes, valves and volumes before the clean gas is introduced; and also allows to find leaks on the system. An additional vacuum pump is connected also to the energy plane volume because, as will be explained, this entire cavity needs a good vacuum for the PMTs to operate safely and for easier leak detection.

Pressure vessel

The NEW pressure vessel has been manufactured with the same 316Ti steel alloy selected for the NEXT-100 detector, from *Nironit* [Maneschg et al. 2008] [Aprile et al. 2011]. The fabrication of the vessel was made possible thanks to a *CEDETI* grant. Figure 1.11 shows the pressure vessel before placing it in the operation platform, where will be surrounded by the lead castle; and figure 1.14 shows the cross-section of the vessel, with its inner parts.

With an internal diameter of 64 *cm* and a length of 950 *cm*, the dimensions of NEW are intermediate between NEXT-DEMO and NEXT-100. By design the pressure vessel can hold up to 50 *bar*, and it is CE certified to 20 *bar*.

For shielding purposes inside the vessel there are 6 *cm* thick copper bars, covering all the cylinder. The bars are designed with a stepped profile, so each one matches the adjacent bars. This way there are no straight paths for outer particles to getting into the active volume. Also, as can be seen on figure 1.14, both detection planes have big copper plates with 12 *cm* thickness. This ensures that all the active volume is properly shielded form any direction. However,

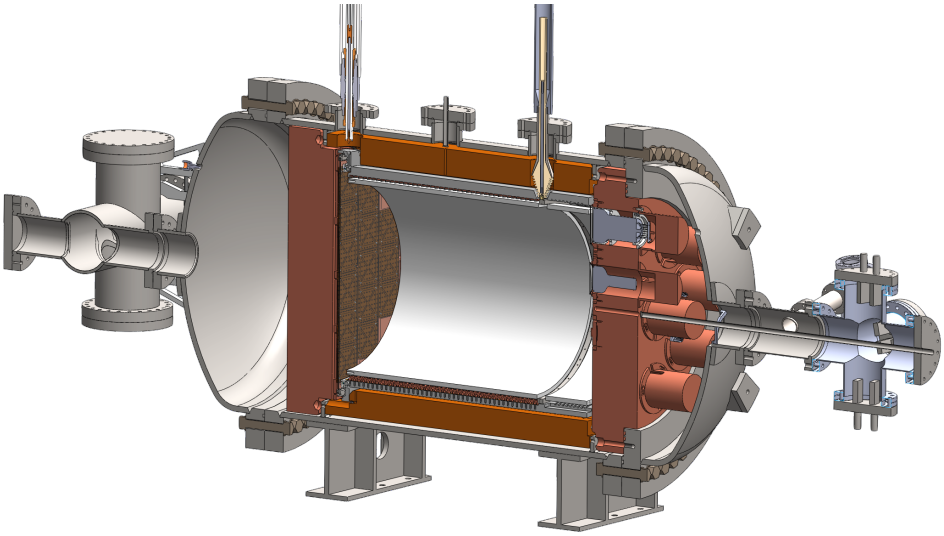


Figure 1.14: *Cross-section view of the NEW detector. The tracking plane (on the left) holds* 28 *DICE-Boards for the tracking reconstruction, and the energy plane (right) has* 12 *PMTs for the precise energy measurement.*

there are some openings in the copper, placed to allow the detector calibration using radioactive sources outside the vessel.

Time Projection Chamber (TPC)

Simulation

The electric field of the field cage has been simulated with finite elements algorithms using *COMSOL Multiphysics*. All the geometry was imported and the electric field was computed for the whole field cage (figure 1.15). In order to see the variations of the electric field across the field cage a detailed study of the critical regions of the field cage has been performed.

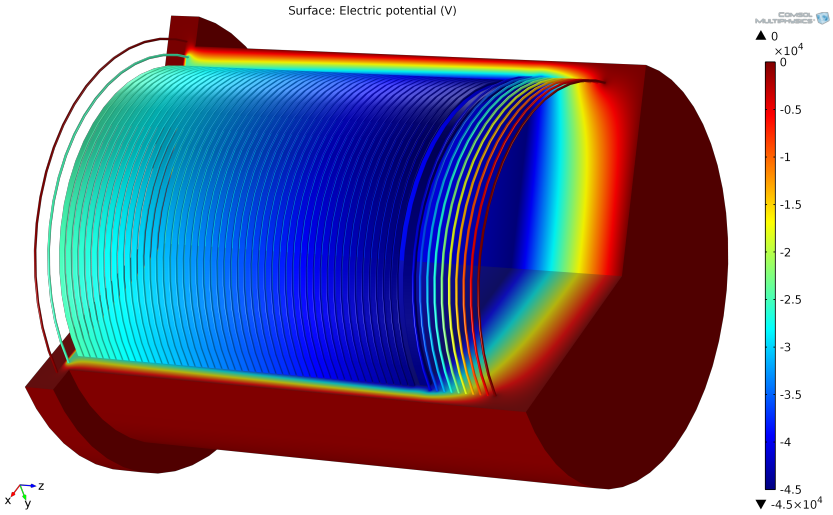


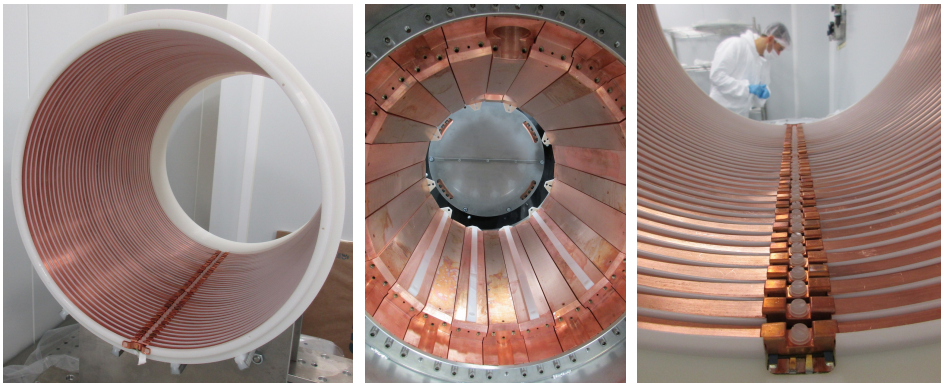
Figure 1.15: *The NEW field cage electric field was simulated using finite elements software (COMSOL Multiphysics).*

Field Cage

The NEW field cage design is based on a high density polyethylene (HDPE) cylindrical shell, 25 mm thick, which isolates the copper shield from the voltage in the copper rings and the cathode. The rings are placed inside grooves and connected by copper clamps to a resistor chain. The field cage has an outer diameter of 500 mm and a length of 500 mm. Thus, both the longitudinal and radial dimensions are roughly half of those of NEXT-100.

The drift region in high pressure xenon needs of a moderate electric field ($300 - 600\ V/cm$), thus a maximum voltage of 30 kV (for a drift of 500 mm) is foreseen in the cathode. This electric field is enough to avoid electron recombination in gas and drift the charges towards the anode. On the other hand, the field in the drift region should be highly uniform and homogeneous trying to avoid any radial component of the field. Those field characteristics are mandatory to ensure no charge losses in the walls during the drifting process.

The rings in the drift region are made out of electrolytic copper which section is a rounded rectangle of $10 \times 3mm$ and $0.5mm$ radius on the edges. The rings are



(a) *Field cage before being installed.* **(b)** *HDPE supports to keep the field cage in place.* **(c)** *Detail of the copper rings attached to the resistor chain.*

Figure 1.16: *NEW field cage details during assembly.*

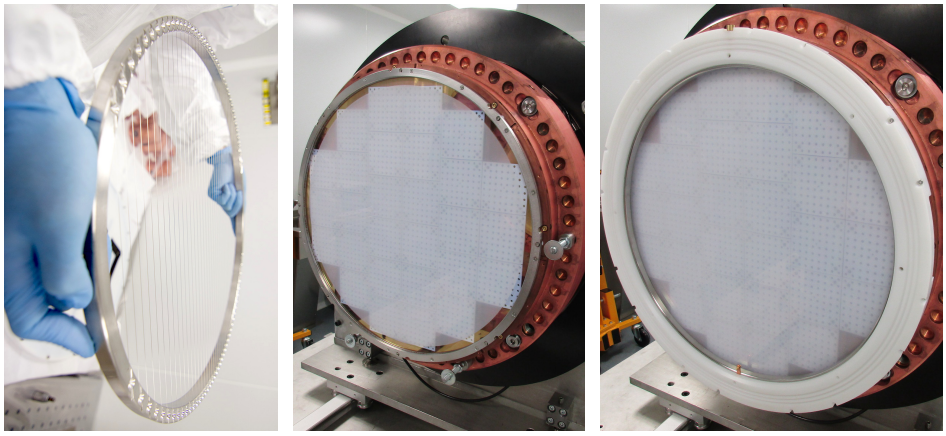
inserted in grooves inside the high density polyethylene body of the field cage. These grooves are 4 *mm* in depth, allowing some space between the surface of the ring and the wall of the field cage that is necessary to support the light tube inside the field cage.

Cathode

In the energy plane side (where the PMTs are) the field cage is terminated by a transparent cathode grid (figure 1.17a), placed at 100 *mm* from the PMTs. The cathode is the section with the highest voltage, which produces the electric field towards the gate, but also towards the PMTs along what we have called "the buffer".

The buffer zone is necessary to degrade the electric potential from the cathode to near zero volts at the PMT window surface. In that region of the TPC we do not demand the electric field to be highly uniform and then different degrading options are possible. The current design degrades the voltage without using rings, trying to avoid electric fields regions near the breakdown. In order to protect the PMTs against the electric field, their windows are coated with ITO (Indium-Tin Oxide), a transparent conductive molecule. The polyethylene in the

buffer region is slightly thinner (15 *mm*) than in the drift region to give enough space to introduce the cathode inside the field cage.



(a) *Cathode grid.* **(b)** *Fused silica anode.* **(c)** *Gate grid mounted over the anode.*

Figure 1.17: *NEW field cage cathode, anode and gate, during the installation on June 2016.*

Gate & EL region

The solution for the EL region is to use a mixture between a mesh for the gate (figure 1.17c) and a solid quartz (fused silica) plate coated with Indium-Tin Oxide (ITO) as anode (figure 1.17b). This coating results in a $\sim$ 90% transparency conductive layer that allows to fix a voltage in the surface of the quartz plate and then creates an homogeneous field in the EL region. The quartz plate has to be coated with TPB to shift the VUV light of the Xenon electroluminescence to blue, to be detected by the tracking plane SiPMs.

The quartz plate solution has multiple advantages. First, it protects the SiPMs from sparking and then there is no need to coat the SIPMs. Second, it removes the necessity for tension and strength at one side of the mesh, only a small ring surrounding the edge of the ITO coating is needed to prevent sharp edges of the conductive layer. Last, the production of the quartz plate is simpler and cheaper than the mesh.

Both anode and gate are assembled in the tracking plane copper plate, so the distance between the anode and the SiPMs can be precisely adjusted. Then a spring contact in the gate connects it electrically to the field cage.

Resistor Chain

The resistor chain has two purposes: to hold together the two sides of the different rings, and to connect the rings by resistors. Thereby a voltage divider is created and the potential is uniformly degraded.

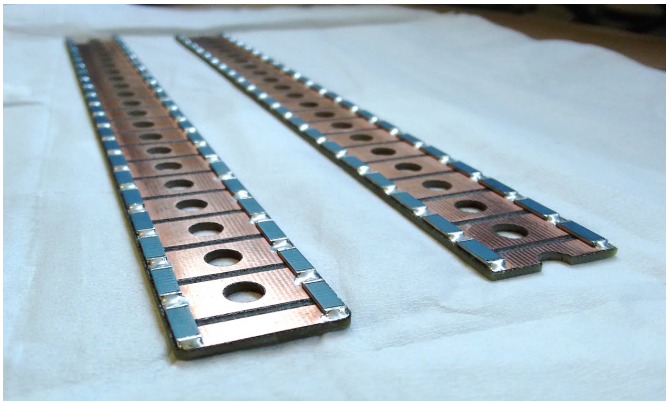


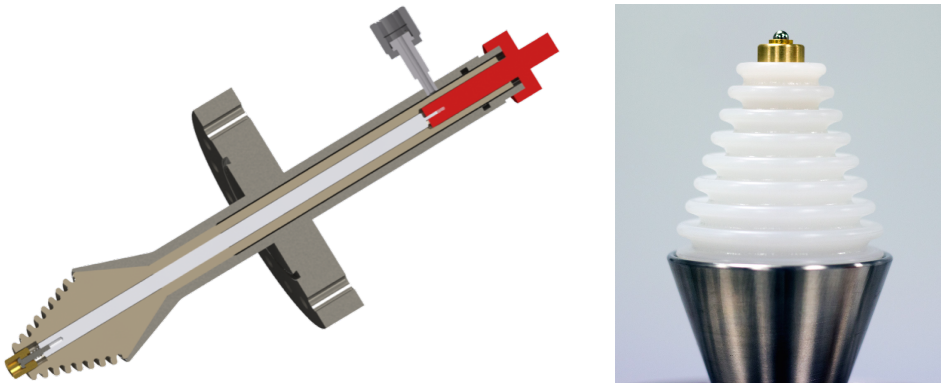
Figure 1.18: *NEW resistor chain in two pieces before the assembly on the field cage. The chain shown is the first FR4 prototype, made to test the field cage performance before the final one is produced.*

The NEW resistor chain (figure 1.18) will be mounted on a *CuFlon* board connecting every ring to the next one and also the cathode and the gate to their closest rings. The resistors need to hold high voltage and their tolerance needs to be minimum to guarantee homogeneity in the electric field. Instead of using just one resistor between rings we have mounted two parallel 10 $G\Omega$ resistors, to safeguard a possible resistor failure. These values may be soon decreased by one order of magnitude, as the high voltage modules can provide enough current and the power dissipation will be performed by the copper rings according to the calculations. This change will have the benefits of making it easier to

find radiopure resistors and reducing the effect of parasitic conductance and capacitance.

High Voltage Feedthroughs

The voltages needed for NEW operation are similar to the NEXT-DEMO requirements. The design has been slightly modified for a better connection with the cathode and gate in the NEW detector.



(a) *HV feedthrough design cross section.* **(b)** *HV feedthrough tip detail.*

Figure 1.19: *High voltage feedthroughs designed for NEW.*

The feedthroughs have been completely redesigned to ensure that they hold easily the 50 kV considered as the maximum requirement for normal operation. The design is based on an original idea by H. Wang presented in the "*High Voltage in Noble Liquids for High Energy Physics*" workshop held at *Fermilab* [Rebel et al. 2014].

Light Tube

The light tube (figure 1.20) consists of a hollow PTFE cylinder, placed inside the field cage. It is the most internal part of the detector, where the events of interest are produced. For the same reasons explained before for the NEXT-DEMO detector, the inner side of the light tube has been coated with TPB. Due

to the big size of the pieces, the coating was made at the facilities of the *Laboratori Nazionali del Gran Sasso* (LNGS) by the members of the NEXT collaboration.

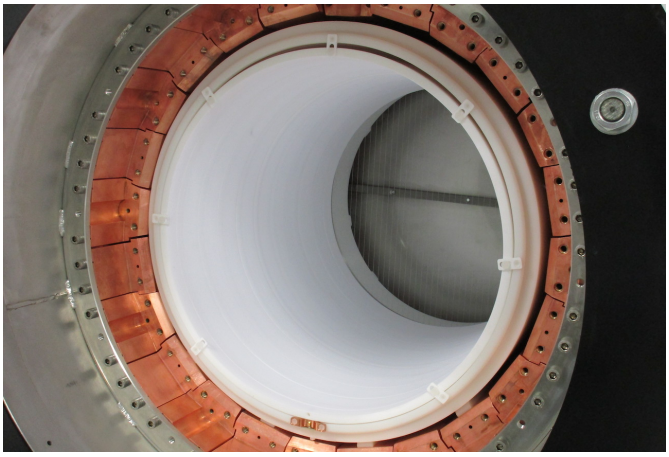


Figure 1.20: *NEW light tube, made of PTFE.*

The light tube has a inner diameter of 416 mm, and a wall of just 10 mm. Due to the tricky design parameters, the one showed in the picture is made by several rings attached together; but a new one will be produced in just one piece and will be installed in the next detector upgrade.

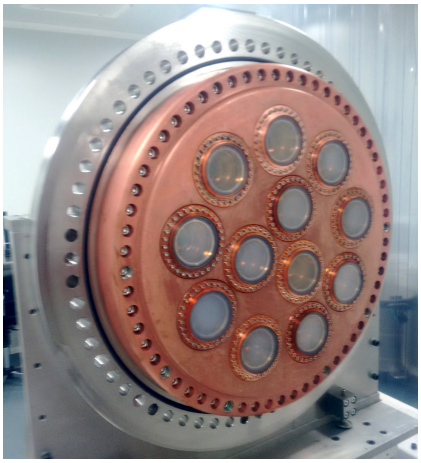
Near the cathode there is a small support that prevents it from touching the cathode wires. The light tube does not need any fixing to the field cage, it is supported by friction to it.

Energy Plane

The design of the energy plane (shown on figure 1.21) consists of a 12 cm thick copper support plate with 12 copper window surrounds with brazed sapphire windows fixed to the front of the plate and covering the 12 apertures through which the PMTs will be fed. The set-up as a whole seals the pressure vessel from the torispherical head which will be held at vacuum levels of $\sim 10^{-4}$ $mbar$.

Additional copper shielding (see figure 1.21a) will be fixed to the vacuum side of the apertures to guard against gammas traversing the PMTs and entering in

(a) *Back side of the energy plane being installed. The PMTs are placed inside the holes, and covered with a 12 cm copper "hat".*



(b) *Front side of the energy plane. The sapphire windows isolate the vacuum from the pressure.*

Figure 1.21: *NEW energy plane during installation on July 2015.*

the detector volume. The 12 *Hamamatsu R11410-10* PMTs are optically coupled to the sapphire window using *NyoGel OCK-451* and held in place by a HDPE brace and spring.

In order to improve the light recollection, the sapphire windows were coated with TPB. And to protect the PMTs from TPC the electric field, the windows were also coated with a conductive layer of ITO, the same used for the fused silica plate on the field cage.

The PMTs are supplied with high voltage and have their signal extracted via a shielded twisted pair cable connected to a custom feedthrough in the torispherical head. The distribution of signal and supply at each individual PMT is controlled via *Kapton* circuit board (base) which has the resistor divider to properly fed the PMT dynodes. Then the base is covered with a copper cap filled with epoxy which is connected by a braid to the support plate, to allow generated heat to be dissipated in the vacuum conditions.

(a) *One of the Hamamatsu R11410-10 PMTs.* **(b)** *Kapton base potted with thermal epoxy.*

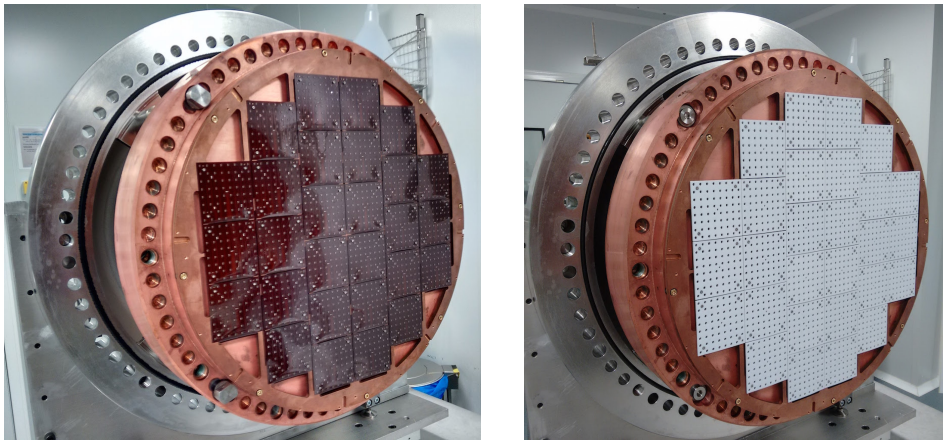
Figure 1.22: *PMT and its polarization base used in NEW.*

Tracking Plane

The NEW tracking plane is made of 28 *Kapton* DICE-Boards (KDB). Each KDB has an 8×8 SiPM array placed with 1 *cm* pitch, a NTC temperature sensor and four LEDs for calibration. The KDBs over-cover the fiducial region with ~ 1800 SiPMs, ensuring that there are no dead regions. The connector is located at the end of a long tail, and is screened from the gas, in the fiducial volume, by a 120 *mm* thick copper plate shield.

The DICE-Boards (DBs) for NEXT-DEMO were made of multi-layer *CuFlon*, and their radioactivity budget was moderately high, due to the adhesive needed to glue the layers. Two additional problems with the DBs were the need to solder SiPMs by hand (since *CuFlon* does not tolerate the temperatures of an oven) and the need to use connectors (all of which are known to be non radiopure).

The new KDBs for NEW solve all the above issues. The material is *Kapton*, and the measured radioactivity budget (only upper limits) is one order of magnitude less than in the old DBs. In addition, TPB was coated directly on top of the DEMO DBs. Instead, the design of the electroluminescent region with a quartz plate allows for a direct coating of the plate instead of the individual DICE-Boards.



(a) *Tracking plane installation on November 2015.*

(b) *Tracking plane upgrade with PTFE masks on April 2016.*

Figure 1.23: *NEW tracking plane.*

To improve the reflectivity of the tracking plane and be able to collect more light on the energy plane the DICE-Boards were covered by PTFE masks, as shown on figure 1.23b, some months after the initial installation.

As this thesis is focused on the NEW tracking plane, more technical details can be found on further chapters.

Electronics and DAQ

From the beginning of the NEXT Experiment, the electronics were thought to be easily scalable and compatible with all the detector stages. So almost all the electronics are evolved versions from the early stages of NEXT-DEMO.

In case of the energy plane front-end, the main specifications and components remain the same (see section 1.3), but upgraded to the new differential cable scheme intended to reduce the coupled noise due to the long cables. Also, as the new PMTs are biased with positive voltage, a coupling capacitor is needed in order to isolate the high voltage from the input analog stage, but allowing the smalls signals to pass through. This produce a known effect that distort the

signal, so a further offline signal reconstruction is needed to keep the energy resolution. Once the analog signal has been amplified and shaped it is sent also in differential mode to the ADC cards via HDMI cable. There the signals are digitized, and then processed as explained later.

Figure 1.24: *The NEW electronics cabinets. From the left, the computers and servers, the energy plane, and the tracking plane cabinet. At each side of the cabinets there is a big UPS, capable of supply the whole system up to 40 minutes in case of power failure.*

The tracking plane front-end electronics will be widely explained on chapters 3 and 4. Concerning the digital stage, each front-end board has a *Virtex-6 XC6VLX130T* FPGA which reads out data from up to sixty-four 1 *MHz* ADCs, formats data, time-stamps and stores them in a reconfigurable-length dual-event circular buffer to avoid dead time. When a trigger is received, zero-suppressed data is read out and sent to the upper stage. The circular buffer is implemented with the internal resources of the FPGA and is able to store two complete events in raw mode, whose maximum size corresponds to approximately twice the maximum detector drift time (up to 3.2 *ms*).

Baseline adjustment and zero-suppression parameters (baseline reference, value over the baseline, pre- and post-samples, minimum number of samples to consider a pulse) are configurable through a set of commands. In zero-

suppression mode, the system triggers when the signal exceeds the value over the baseline fixed during at least the minimum number of samples to consider a pulse. Then, this signal is sent with its pre- and post-samples. Raw data mode of operation, where no zero suppression occurs, is also supported for testing purposes.

Both tracking plane and energy plane front-end cards interface the Scalable Readout System's (SRS) DAQ interface modules [Toledo et al. 2011] (tested on both FECv3 and the new FECv6) through the SRS' DTCC (Data, Trigger, Clock and Control) link specification over copper [Tarazona et al. 2014]. In this link, data, trigger, clock and slow controls flow on the same RJ-45 or HDMI connector over 4 LVDS pairs. *ALICE's DATE* is used as DAQ software environment. As a result, the front-end electronics are fully compatible with CERN RD-51 SRS electronics. The DTCC configuration used is the basic one. The link has been fully tested up to 250 *Mbps* over the two data pairs using 1 *meter* SFTP 6A copper cables.

Slow Control

Obviously, an experiment with such complexity as the NEW detector will need an advanced control system. That is what we have called the Slow Control (SC).

With the slow control we have created an internal network which connects all the subsystems and devices involved in the experiment, and adds an intelligence that keeps the system safe and acts to prevent and solve problems immediately. On figure 1.25 the control displays are shown.

Without going into greater detail, there are 6 different programs connected to the experiment and between them:

- **High Voltage:** Monitors and controls the voltage on the field cage cathode and gate. Detects the sparks and recovers or shuts down the system according to the parameters set.
- **Gas System:** Monitors all the parameters involving the gas system: valves, pressure, vacuum, compressor, chiller, vacuum pumps, RGA... As the gas

Figure 1.25: *The NEXT Slow Control.*

system was defined as critical, almost all intervention is forbidden because the system is autonomous. Nevertheless, an emergency stop can be done through the SC.

- **Power Supplies:** Monitors and controls all the power supplies that power the electronics in the experiment, including the SiPM custom bias sources.
- **PMT High Voltage:** Monitors and controls the PMTs power supply, detects overcurrents and controls also the vacuum pump connected to the energy plane volume.
- **Sensors:** Monitors the temperatures and other important parameters of the electronics and DAQ computers. Controls also the contactors that power almost all the equipment and electronics.
- **Main:** This slow control receives the main parameters and warnings from the other ones, so the shifter knows if everything is working properly just looking at this one. It also has an emergency button, that stops everything to prevent damage, and can remotely switch on the other slow control computers.

Each one of the slow controls also generates reports, including all the events registered for each subsystem and the main parameters measured. Also emails

are sent to the shifter, with warnings or alarms produced, so he can act as soon as possible.

Lead Castle

To shield NEW (and NEXT-100 in the future) from the external flux of high-energy gamma rays, a relatively simple lead castle (figure 1.26) has been chosen, mostly due to its simplicity and cost-effectiveness. The lead wall has a thickness of 20 *cm* and is made of layers of staggered lead bricks held with a steel structure.

Figure 1.26: *The NEXT Experiment lead castle. The NEW detector stands previously to the piping and cabling installation.*

The lead bricks have standard dimensions ($200 \times 100 \times 50$ mm^3), and, by requirement, an activity in uranium and thorium lower than 0.4 mBq/kg. The lead castle is made of two halves mounted on a system of wheels that move on rails with the help of electric engines. The movable castle has an open and a closed position. The former is used for the installation and service of the pressure vessel; the latter position is used in normal operation. A lock system

fixes the castle to the floor in any of the two configurations to avoid accidental displacements.

In both castle sides, where the two halves seal, there are moving "doors". This "doors" are also made of lead bricks, and can be moved to allow working space (on the open position) and to shield the joint between the two castle halves (on the closed position).

Due to the mild seismic activity of the part of the Pyrenees where the LSC is located, the lead castle is mounted on a seismic structure in order to isolate it from possible ground vibrations. Thereby the lead castle is not mechanically attached to the working platform, and all the electrical and gas connections are flexible between these separate structures.

1.5 NEXT-100 and Beyond

The NEXT experiment was formally proposed to the Laboratorio Subterráneo de Canfranc (LSC) in 2009 in a Letter of Intent [Granena et al. 2009]. The detector design was narrowed down in a Conceptual Design Report [Álvarez et al. 2011] published in 2011, and fixed a year later in a Technical Design Report (TDR) [Álvarez et al. 2012c]. Consequently, the Collaboration favored the configuration that had been tested with the NEXT-DEMO and NEXT-DBDM prototypes.

As explained before, NEW is a reduced version of NEXT-100 with the same technologies. So there is no need of a detailed explanation of every NEXT-100 component. However, the main differences are the following:

- **Pressure vessel:** The pressure vessel of NEXT-100, shown on figure 1.27, consists of a cylindrical central section of 160 cm length, 136 *cm* inner diameter and 1 *cm* wall thickness, and two identical torispherical heads of 35 *cm* height, 136 *cm* inner diameter and 1 *cm* wall thickness. It has been fabricated with stainless steel type 316Ti due to its low levels of natural radioactive contaminants.

- **Field cage:** The main body of the field cage is an open-ended high-density polyethylene (HDPE) cylinder of 148 *cm* length, 107.5 *cm* inner diameter

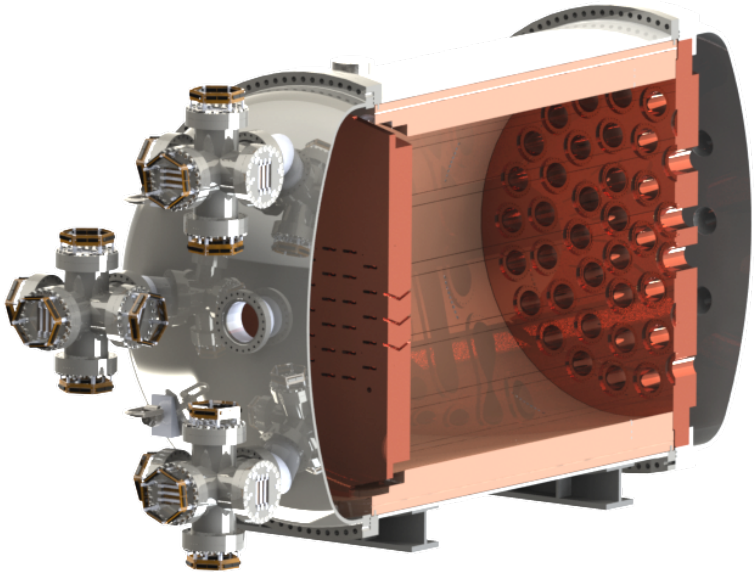


Figure 1.27: *Cross-section view of the NEXT-100 detector. The active volume is shielded from external radiation by at least 12 cm of copper in all directions.*

and 2.5 *cm* wall thickness that provides structural stiffness and electric insulation. A series of copper rings for electric field shaping are fixed to the inner surface of the cylinder, soldered to a resistor chain that fixes the voltage of each ring. The rings are covered by PTFE tiles coated with TPB to shift the xenon VUV light to blue and improve the light collection efficiency. One of the ends of the HDPE cylinder is closed by a fused-silica window 1 *cm* thick. The inner surface of the window functions as the TPC anode thanks to a transparent, conductive, wavelength-shifting coating of Indium-Tin Oxide (ITO) and TPB. The two other electrodes of the TPC, EL gate and cathode, are positioned 0.5 *cm* and 106.5 *cm* away from the anode, respectively, and are built with highly-transparent stainless steel wire mesh stretched over circular frames.

- **Energy plane:** The energy plane of NEXT-100 will be composed of 60 *Hamamatsu R11410-10* PMTs located behind the cathode of the TPC and covering approximately 30% of its area. The copper plate and mechanical

elements of the energy plane have the same structure as NEW, adapted to the bigger size of the detector.

- **Tracking plane:** The tracking plane will have the same structure as NEW, but the number of DICE-Boards is increased to 112, which gives a total of 7168 SiPM matrix. As consequence of the larger number of SiPMs, the feedthrough is being improved and optimized, to allow higher connector density. Also the front-ends used will be the future revision of the board, the FEB64v3.

- **Electronics:** As the electronics designed for the NEXT experiment are fully scalable, there are no big changes on this subsystem. It will need a larger number of electronic boards ($\sim$ 5 times more front-end cards) and the DAQ system will be scaled accordingly.

- **Gas system:** The gas volume in NEXT-100 is bigger, but the main components used for NEW are the ones planned for NEXT-100. The main difference is the emergency recovery tank, which is 10 times bigger than the one used for NEW, due to the gas volume needed.

1.6 Seeing the invisible: Silicon PhotoMultipliers (SiPM)

As explained on previous sections, the use of silicon photomultipliers as pixel tracking is a novelty, and since the beginning NEXT had to develop new technologies that made it possible. This sections act as introduction to semiconductor devices and describes the operating principle of the SiPMs [Lorca 2015].

1.6.1 Semiconductor devices

Silicon, as a semiconductor material, presents an electronic bands structure, illustrated in figure 1.28. This structure consists of a valence band, a "forbidden" energy gap and a conduction band. The energy bands are regions of many discrete levels which are so closely spaced that they may be considered a continuum, while the "forbidden" energy gap is a region in which there are

no available energy levels at all. The highest energy band is the conduction band. Electrons in this region are detached from their parent atoms and are free to move around the material. The electrons in the valence band levels, however, are more tightly bound and remain associated to their respective lattice atoms.

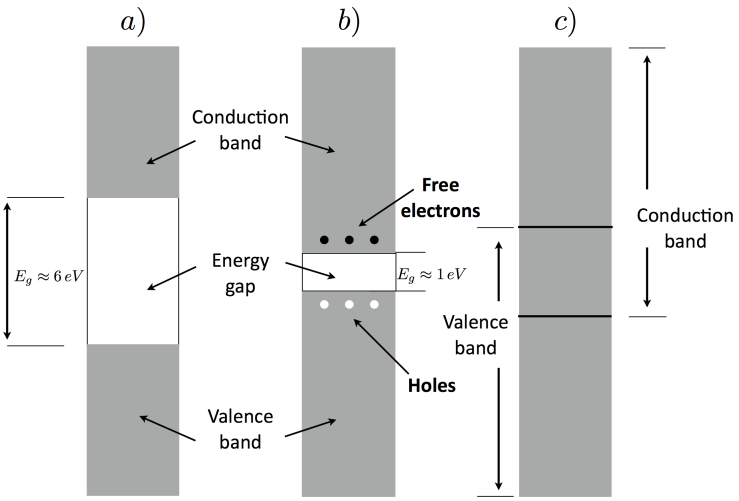


Figure 1.28: *Scheme of the energy-band structure of (a) an insulator, (b) a semiconductor, and (c) a conductor.*

In a semiconductor, the width of the energy gap is relatively small, around 1 eV [Leo 2012], so a few electrons can be thermally excited and jump into the conduction band. In insulators, the energy gap is larger, and their electrons are normally all in the valence band. In conductors, however, the gap is nonexistent and electrons are free to jump into the conduction band and, if an electric field is applied, a current is generated.

Silicon is a tetravalent atom, that is, it has four valence electrons to create four covalent bonds and stabilize the joint, forming an atomic crystal. In this configuration, if a valence electron is thermally excited, it moves into the conduction band leaving a hole in the valence band. This hole is rapidly filled by a neighboring valence electron, leaving a new hole which will be filled by another valence electron. The repetition of the process along the structure of

the crystal results in the apparent movement of a positive charge (the hole), and thus a positive current is generated. In silicon, contrary to what happens with metals where the current is generated only by electrons in the conduction band, the electric current arises from two sources, the movement of the free electrons in the conduction band and the movement of the holes in the valence band.

If the silicon is "pure", the number of holes is equal to the number of electrons in the conduction band. However, a small amount of impurities can be added to the crystal, modifying its lattice. This process is called doping. If the dopant is pentavalent, which means that it has five electrons in the valence band, four covalent bonds will be formed leaving one free electron. This free electron will reside in a discrete energy level created in the energy gap by the presence of the impurity atom, which will be extremely close to the conduction band being separated by only 0.05 eV [Leo 2012]. In this configuration, electrons are the majority charge carriers and silicon called n-type (figure 1.29 left). On the other hand, if the impurity is trivalent, it contains three electrons in the valence band and three covalent bonds will be formed, generating an excess of holes in the crystal. The trivalent impurities also perturb the band structure by creating a new state in the energy gap, but this time close to the valence band. In this case, holes become the majority charge carriers and silicon is called p-type (figure 1.29 right). The impurities typically used are arsenic or phosphorus to create n-type, and gallium or boron for p-type. The level of impurities present in the crystal is usually small compared to its density (10^{22} atoms/cm^3), typically of the order of 10^{13} atoms/cm^3 [Leo 2012].

Silicon photomultiplier technology uses as its base the silicon diode. Such devices are made by diffusing n-type and p-type dopants into adjacent regions on a silicon substrate to create pn junctions, as shown on figure 1.30. Along the border between majority p-type and majority n-type regions the difference in electron and hole concentrations causes diffusion between the regions. As more electrons diffuse into the p-type region and holes move in the opposite direction an electric field is created which opposes further movement. The region in which this field acts is called the depletion region and, generally, has a width of order 0.5 μm and potential difference of $V_0 = 0.7\ V$.

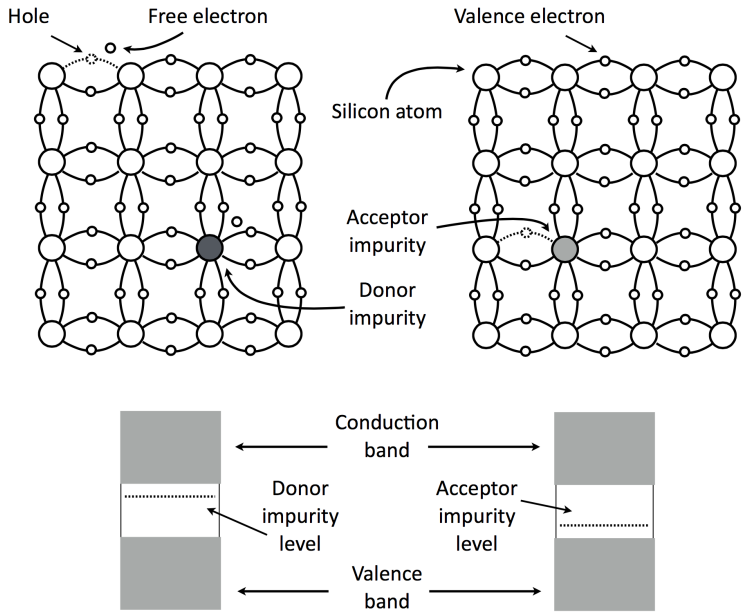


Figure 1.29: *Covalent bonding of silicon. Left: Addition of pentavalent impurity (donor) forming n-type silicon. Right: Addition of tetravalent impurities (acceptor) forming p-type silicon.*

If a bias voltage is applied to the pn junction in such a configuration that the p-type is connected with the positive terminal and the n-type is connected with the negative terminal, free electrons present in the n-region are pushed by the electrons from the negative terminal to the pn junction, at the same time that the positive terminal attracts the valence electrons in the p-region, or, in other words, holes are pushed toward the pn junction. In any case, the depletion zone will be reduced according to the applied bias voltage and the external applied voltage reduces the potential barrier for electrons and holes, and current easily crosses the junction. This is the forward bias configuration.

On the other hand, if the bias voltage is applied in the reverse bias configuration, where the p-type region is connected to the negative terminal and the n-type region is connected to the positive terminal, the opposite effect occurs. Valence electrons present in the n-type region are attracted by the positive terminal at

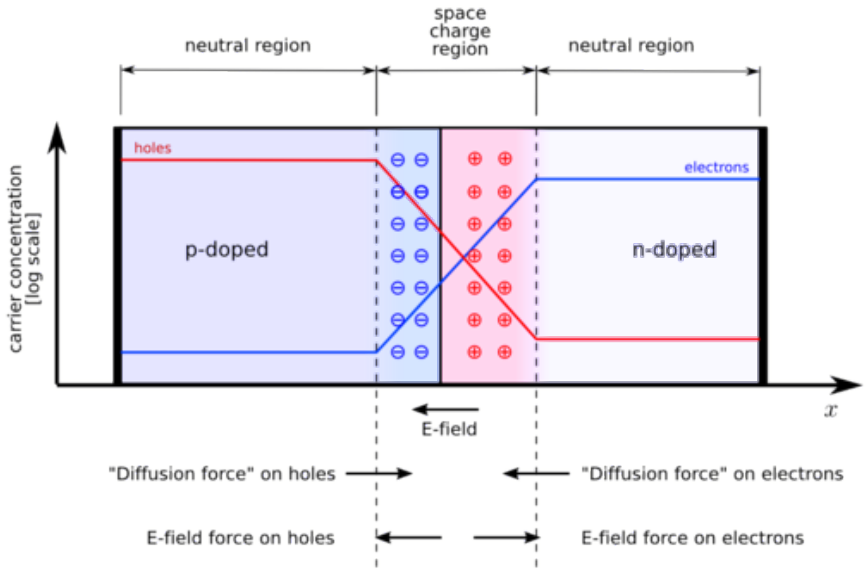


Figure 1.30: *Scheme of pn junction model.*

the same time as the negative terminal provides electrons to the holes present in the p-type region. This process is repeated until the depletion zone acquires the same potential as the supplied as well as an electric field proportional to the generated by the bias voltage. The net effect is an enlargement of the depletion zone, which is limited by the resistance of the semiconductor, until width values of around 1 mm. If the applied bias voltage keep rising the the pn junction will breakdown and begin conducting. Under these conditions, the depletion zone acquires the spatial property of being devoid of all mobile charged particle. The average energy for electron-hole pair creation in silicon at $25^{\circ}C$ is 3.62 eV [Leo 2012]. Ionizing radiation entering in this zone will create electron-hole pairs which will be swept out by the present electric field, and a current signal generated. The intensity of this signal depends of the bias voltage applied. If this voltage does not exceed a threshold, charges recombine, so no current signal will be generated. As bias voltage increases, the electric field causes that each original electron leads to an avalanche which is basically independent of

all other avalanches formed from other electrons associated with the original ionizing event. The collected charge remains proportional to the number of original electrons. This is the proportional mode. With a higher electric field, the depletion zone operates in Geiger mode, in which one avalanche can itself trigger a second avalanche at a different position. The difference between both modes is due to the holes: in Geiger mode they trigger avalanches, whereas in proportional mode, due to their ionization coefficient being much lower than that of electrons, they do not have enough energy to do so.

Real APD devices are more complex than a *pn* junction, as can be seen on figure 1.31, because in this photosensors the p-type silicon commonly has three different stages.

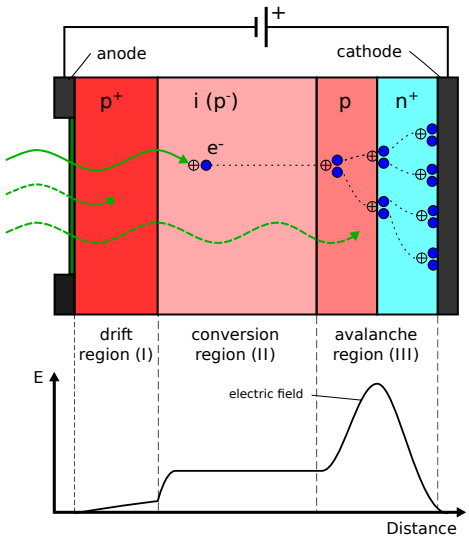


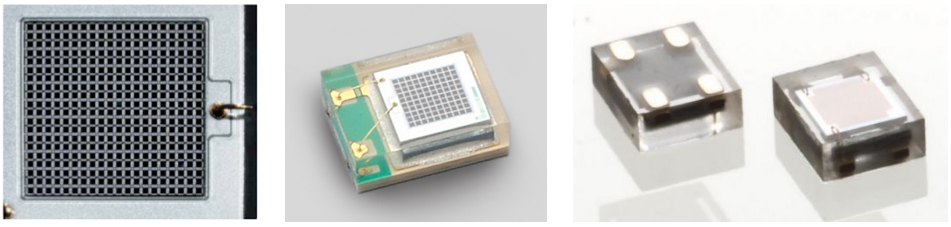
Figure 1.31: *Scheme of an APD (Avalanche PhotoDiode) junction model. The substrate configuration and geometry depends on the wavelength range where the manufacturer wants to maximize the detection efficiency.*

First a thin p^+ layer acts as anode needed for the drift. The conversion region, which is the weakly p-doped or intrinsic part, is where the most incoming photons produce photoelectrons which are then drifted towards the avalanche

region. There, the high electric field created by the $p - n^+$ junction allows the characteristic avalanche of this kind of sensors.

1.6.2 Silicon PhotoMultipliers

A Silicon PhotoMultiplier (SiPM) consists of a matrix of photodiodes, like the ones described in previous section, operating in Geiger mode. These photodiodes are connected in parallel with each one acting as a pixel of the SiPM. A single SiPM cell or pixel can only detect one photon at a time while the avalanche is produced. So the array configuration of hundreds (or thousands) of very small pixels allows the SiPM to "see" several simultaneous photons detected on different cells, while the statistical probability of two photons arriving to the same pixel at the same time is reduced (considering a low intensity light source). A detailed picture of this structure is shown on figure 1.32. The pixels are connected using aluminum strips to read out the combined signals. The pixels are electrically decoupled by polysilicon resistive stripes between the pixels. These sensors are known by a huge range of names such a G-APD, SiPM, MRS APD, AMPD, or Multi Pixel Photon Counter (MPPC).



(a) *Detail of the pixel array.* **(b)** *Hamamatsu SiPM.* **(c)** *SiPM from SensL.*

Figure 1.32: *Silicon photomultipliers.*

Two sensors are candidates to provide the tracking function in the NEXT experiment, the *Hamamatsu S10362-11-050P* model and the *SensL MicroFC-10035-SMT-GP* model. Both sensors have been chosen because of their many attractive features (see table 1.1), such as low cost (about 20 € to 50 € per unit in large quantities), low operating voltage (usually smaller than $100V$), high gain, insensitivity to magnetic fields, and compact dimensions. Drawbacks arise from

the high thermal noise rate (typically from 100 kHz up to a few MHz at a half photoelectron threshold) and the occurrence of after-pulses and crosstalk.

Parameter	S10362-11-050P	MicroFC-10035-SMT-GP
Effective active area	1×1 mm	1×1 mm
Number of Pixels	400	576
Pixel size	50x50 μm	35x35 μm
Operating Temperature	0 to 40 °C	-40°C to 85 °C
Fill factor	61.5 %	64 %
Spectral response range	320 to 900 nm	300 to 800 nm
Peak Sensitivity wavelength	440 nm	420 nm
Operating Voltage Range	70±10 V	24.65±0.25 V
Dark Count	400 kcps	70 kcps
Terminal Capacitance	35 pF	100 pF
Time resolution (FHWM)	200 to 300 ps	1500 ps
Gain	$7.5 \cdot 10^5$	$3 \cdot 10^6$
Temperature dependence	56 mV/°C	23 mV/°C

Table 1.1: *Hamamatsu S10362-11-050P* [Hamamatsu 2015] and *SensL MicroFC-10035-SMT-GP* [SensL 2015] SiPMs basic parameters

Electrical Model

The most simple electrical model of a SiPM is shown in figure 1.33. The depletion zone of the silicon introduces a capacitance to the pixel as it is basically a parallel plate capacitor. The pixel can be regarded as a parallel circuit of a reverse biased diode and a capacitor with the pixel capacitance C_d. When the pixel is fired, the resulting avalanche makes the diode conducting so the capacitor is shorted and discharges.

The breakdown of the diode has to be quenched. Most of the time this is done passively with a quenching resistor. After the discharge of the pixel capacitance, the current starts flowing over the quenching resistor, which reduces the bias voltage V_{bias} at the diode below the breakdown voltage V_{bd}. This stops the breakdown and the diode blocks the current again. The quenching resistor is made of polysilicon and has a quenching resistance (R_q) in the order of hundreds of $k\Omega$. The quenching increases the pulse amplitude of the SiPM by introducing a spike component, since it is discharged during the breakdown of the pixel.

When a free electron is produced in one pixel, it initiates an avalanche of charge which produces a current. The currents of the pixels add up, so the output charge signal is proportional to the number of pixels fired.

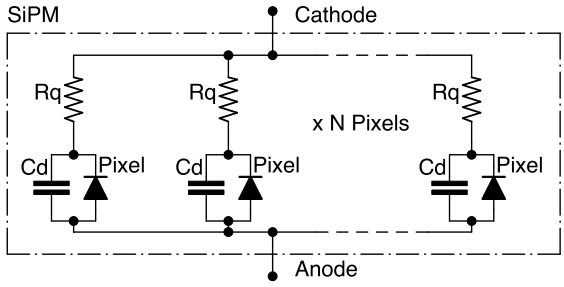


Figure 1.33: *SiPM electrical model.*

For detailed simulation purposes, a more sophisticated model is required [Corsi et al. 2009]. The model shown in figure 1.34 contains the main parasitic elements that affect the SiPM performance.

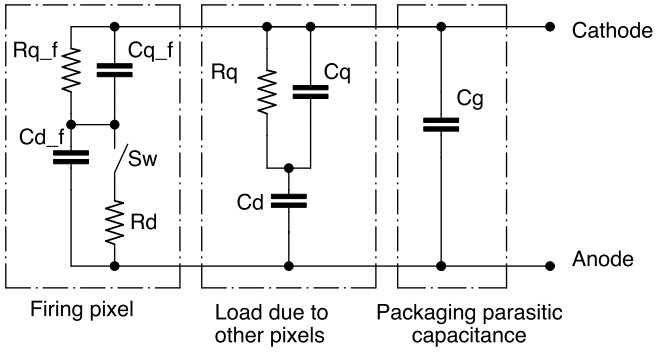


Figure 1.34: *SiPM simulation model.*

In addition to the previous model, this one includes a parasitic capacitance (C_{q_f}) in parallel with the quenching resistor (R_{q_f}), which works as a fast path for the charge delivered during the avalanche. A large metal routing, which spans all over the detector surface, is used to connect in parallel the micro-cells, thus

a further parasitic capacitance (C_g) between the terminals of the whole device must be introduced in the model. And as the SiPM is a pixel array, also the parasitic effects of the remaining cells should be taken into account (R_q, C_q and C_d). Finally, the switch with the series resistor (R_d) act as the pixel firing, which discharges the pixel capacitance through the anode.

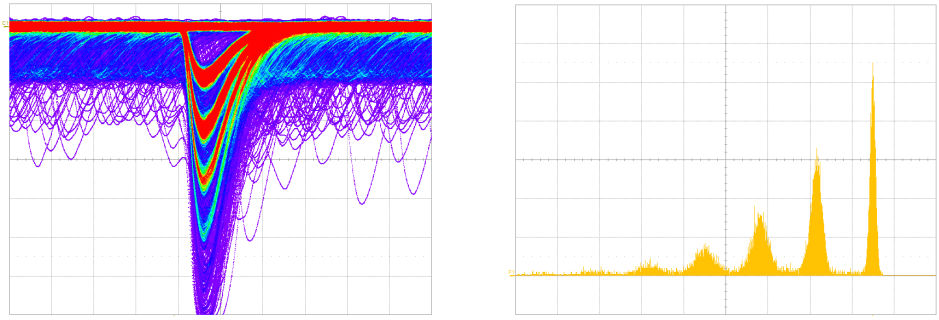
Of course, each SiPM variant of each manufacturer has different performance due to the mechanical differences; so the value of the elements in the simulation model are different for each one. In our case, we used the measured parameters for the *Hamamatsu S10362-11-050P* SiPM, as they were the ones used in NEXT-DEMO and the initial candidates for the NEW detector. This parameters were obtained by a thorough characterization done by our collaborators at *Fermilab*.

SiPM Gain

For most of the SiPM applications, it is very important not just to detect light, but quantify it. That is the reason why to know the SiPM gain is so important, because it is the parameter that relates the signal provided by this device and the amount of photons detected.

The signal provided by a SiPM is the addition of every pixel fired, each one discharging its internal capacitance. The result is, at the output of the device, a narrow current pulse whose charge is proportional to the number of pixels fired, in principle by photons. This performance can be easily seen in figure 1.35a, where hundreds of waveforms are overlapped. In red, the different pulses heights correspond to the number of pixels fired; so the baseline has no charge (no pixels fired), the smallest pulse is the result of on pixel being fired, the second one occurs when two pixels are fired, etc.

Then, the area of each pulse is proportional to the pulse charge. So plotting the histogram of the pulses areas we can obtain the characteristic shape showed in figure 1.35b. There, the peak on the right corresponds to zero area (no charge, no pixels fired). The second peak from the right are the events of one pixel fired, the third for two photons, etc. In this spectrum , the x-axis is the charge, so we



(a) *Persistance displayed waveforms of a SiPM.*

(b) *SiPM pulse area histogram (also known as "single photon spectrum").*

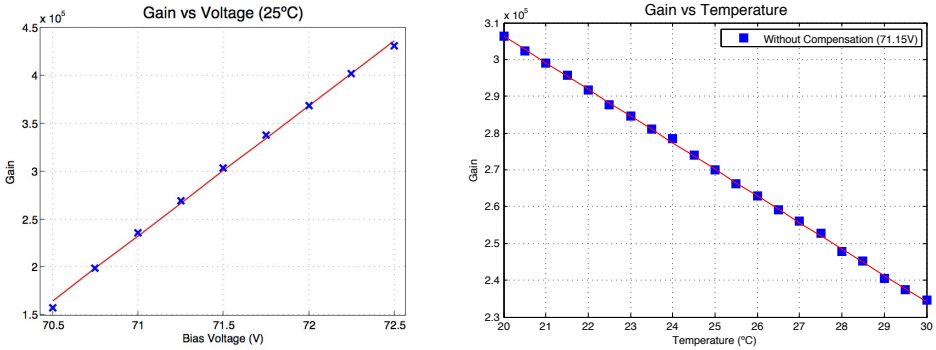
Figure 1.35: *Silicon photomultiplier waveform and single photon spectrum.*

can obtain the gain as the distance between peaks, usually measured in e^- / ph (electrons per photon detected).

The gain of a SiPM is determined from the manufacturing process. However, there are two main conditioning factors: bias voltage and temperature.

As explained previously, a larger bias voltage produces a larger depletion zone and a higher electric field, which means that the SiPM acquires a higher gain. In the other hand, an increase in the device temperature produces a decrease in the gain. This effect is generated because higher the temperatures the more vibration of molecules in the crystal structure, so free electrons in the avalanche process are more likely to collide and stop its movement; so the avalanche is smaller as well as the charge emitted by the SiPM. Both effects can be seen on figure 1.36.

So in order to obtain reliable measurements with a SiPM, or thousands of them as in NEXT, both bias voltage and temperature must be precisely measured and controlled. As will be detailed in Chapter 7, the solution implemented in NEXT uses a programmable power supply with temperature feedback from the SiPMs inside the detector. This way the bias voltage is adjusted continuously as a function of temperature in order to keep a constant and homogeneous gain in the whole tracking plane.



(a) *Gain as a function of bias voltage.* **(b)** *Gain as a function of temperature.*

Figure 1.36: *Silicon photomultiplier gain dependence with bias voltage and temperature. Measurements for the* Hamamatsu S10362-11-025P *device.*

SiPM Dark Count

In some cases, the signal generated by a SiPM does not correspond with an incident photon or afterpulsing effects (seen later). In these cases, the signal is produced by free charge carriers, mainly due to thermal generation or tunneling effect, which triggers the Geiger discharge spontaneously, generating an identical avalanche. Such events occur even when the SiPM is operated in the dark; for that reason this effect is known as dark current or dark counts. The dark count rate (DCR) is a limiting factor for low intensity photon detection, as they can be confused with the arrival of real photons. At higher temperatures ($T > 25°C$), the major contribution to dark count rate is the thermal generation of free charge carriers in the depletion zone. Direct transition of an electron from the valence to conduction band is very rare due to the width of the band gap in silicon.

On the other hand, at lower temperatures it is the tunneling effect which becomes dominant in the DCR because thermal generation of charge carriers is highly suppressed [Nabet 2015]. And the probability for an electron to penetrate the band gap is proportional to the bias voltage, so the tunneling effect becomes significant for induced electric fields above $10^6\ V/cm$, increasing non linearly with field.

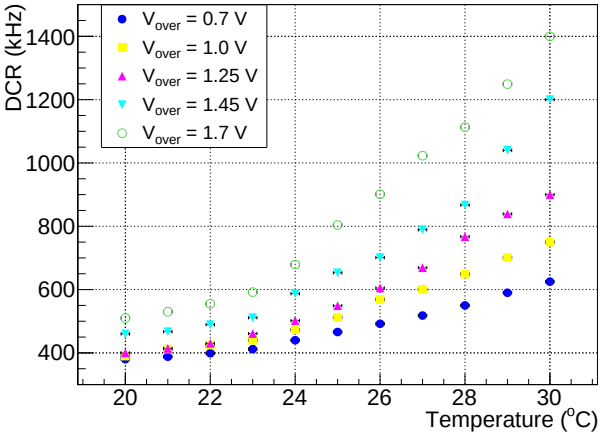


Figure 1.37: *Dark Count Rate of the S10362-11-050C versus temperature at different overvoltages.*

Figure 1.37 shows the DCR at different overvoltage and temperature conditions, as a result of the SiPM characterization process for NEXT-DEMO [Lorca 2015]. Since the DCR is a limiting factor at low light intensities and has a dependency both on temperature and overvoltage, these parameters must be closely monitored and controlled during data taking.

SiPM Afterpulsing

Impurities introduced in the lattice at the time of doping can produce regions with different band structures, traps, where avalanche electrons can be held and released after a characteristic time. If this characteristic time is longer than the recovery time, the released electron will produce a new avalanche within the pixel. This process is called afterpulsing and its probability strongly depends on the density of impurities in the silicon.

In the case that the electron is released before the bias voltage is completely restored, which occurs typically after three times the recovery time, the new avalanche will contain less charge than the pixel capacitance, and will also

reduce the photon counting capability of the SiPM since this charge introduces an additional background to the response spectrum.

SiPM Optical Crosstalk

During the breakdown of one pixel, every electron of the avalanche emits optical photons at wavelengths less than 1000 nm. Considering a gain about 10^6, around 20 photons are generated per fired pixel. These photons can easily reach neighboring pixels, triggering new avalanches which are unrelated to the original one. If this occurs, both signals are integrated as a whole, limiting the photon counting capability of the SiPM, and making it impossible to determine the exact number of original photons detected. This effect is know as optical crosstalk, and increases exponentially with overvoltage due to the number of electrons during breakdown increasing. This effect can be easily reduced by the introduction of opaque trenches between the pixels of the SiPM, which block the arrival of these photons to the neighboring pixels, reducing significantly the optical crosstalk for the overvoltage values where these sensors will be operated [Eckert et al. 2010].

1.6.3 SiPMs and MPPCs in Physics Experiments

Silicon photomultipliers have been gaining popularity along the years, especially in the high energy physics and medical physics fields. For both applications the SiPMs allow to increase the granularity respect PMT detectors, and the simpler electronics needed makes easier the scaling-up of the experiments.

For instance, T2K detectors use about 56000 MPPCs [Kudenko 2009], only achievable with cheap and robust sensors. And CALICE [Jeans and CALICE collaboration 2009], a prototype ILC (International Linear Collider) scintillator-Tungsten electromagnetic calorimeter, was constructed with active layers consisting of scintillator strips, individually read out by MPPC devices. For each calorimeter module the analog signals from the SiPMs are read out by four 36-channel ASICs, the SPIROC chip. Also ILC HCAL (Hadronic Calorimeter) was equipped also thousands of SiPMs [Bouchel et al. 2011], using also scintillator

strips. Another application of SiPMs can be found on the Mu3e experiment [Bravar 2015], which aims to study a lepton flavour violating decay using scintillating fibers for tracking and time of flight measurements. And as last example the CMS Outer Hadron Calorimeter (HO), the first large scale hadron collider detector to use SiPMs [Lobanov and CMS Collaboration 2015].

The need of reading such quantity of channels implied that the front-end electronics designed by some of these experiments, as will be seen in section 2.5, lead to the design of different ASICs (Application Specific Integrated Circuit) as a compact electronic solution.

Almost all the experiments using silicon multipliers are intended for calorimetry applications in high energy physics. The NEXT experiment appeared as the first one using SiPMs as single pixels in a tracking plane, so the electronics' requirements were not fulfilled by the existing solutions developed by previous experiments.

"Oh, si, el pasado puede doler. Pero según lo veo puedes o huir de él, o... aprender."

"Oh yes, the past can hurt. But from the way I see it, you can either run from it, or... learn from it."

– El Rey León / The Lion King

2

The NEXT-DEMO Tracking Plane

The NEXT Experiment made a difference from the beginning: the tracking reconstruction. But being the pathfinder has a great disadvantage, because no one has made something like this before.

Also the SiPMs were a novel technology when the experiment started, and just a few things related to SiPMs could be found on the market. But none of them could be useful for NEXT. So the collaboration had to start from scratch and design everything: support boards, cabling, electronics and even a custom power supply.

Here is where everything started.

2.1 Design Requirements

A $\beta\beta0\nu$ event will deposit 2458 keV ($Q_{\beta\beta}$ for ^{136}Xe) in the xenon gas and will produce a track of about 30 cm long at 10 bar pressure. This track has a distinctive energy deposition pattern in gaseous xenon: a long and tortuous cord due to multiple scattering, ended by two-blobs, corresponding to the ranging-out of the two beta particles (see figure 2.1 left). The average energy deposition in the track is about 70 keV/cm, except in the blobs at both track ends, where about 200 keV/cm are deposited [Álvarez et al. 2011]. The ability to record the topological signature of the $\beta\beta0\nu$ events provides a powerful background rejection factor for the $\beta\beta$ experiment [Álvarez et al. 2012c].

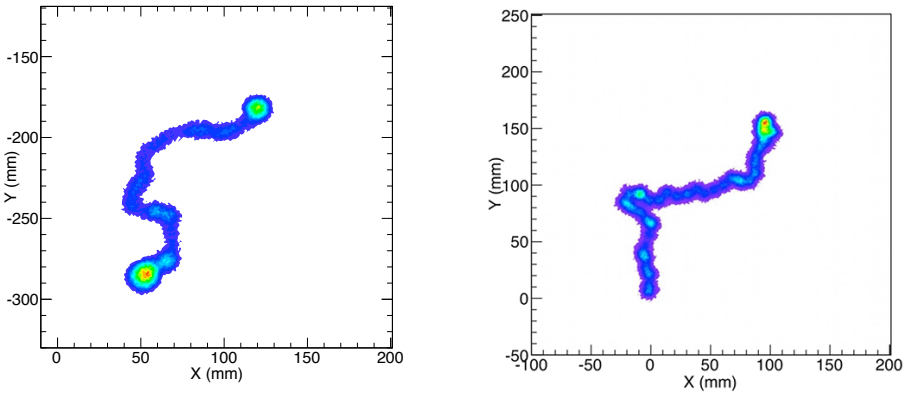


Figure 2.1: *Geant4 simulation of the x-y topological signature of a ββ event (left), corresponding to two ranging-out electrons [Álvarez et al. 2012c] and of one-electron event (right), produced by photoelectric effect from the interaction of a ^{214}Bi gamma-ray (2447 keV) in the xenon gas at 10 bar pressure [Nadia Yahlali et al. 2010].*

The ionization electrons which drift to the TPC anode (at a typical velocity of 1 $mm/\mu s$) generate EL light when crossing the region of intense field ($E/p \sim 2.5\ kV\ cm^{-1}bar^{-1}$) between the highly transparent EL meshes. Thus, setting up a plane with pixel photosensors, located right behind this EL region, enables the measurement of the transverse (x, y) coordinates of the tracks. The

longitudinal coordinate (z) is drawn from the time delay t-t_0 between the time t at which the EL signals are recorded and the reference time t_0.

In addition to the position information, the tracking photosensors have to provide a rough measurement of the energy for the reconstruction of the tracks topology. Indeed, the measurement of the energy per unit of length of the tracks is required for the pattern recognition. To be able to perform tracking using EL, the detection pixels of a few mm^2 area should have a limited field of view more-or-less straight towards the parallel EL meshes. If the tracking plane is a few mm away from the EL region, the tracking pixels mounted on this plane will produce a signal only while the EL is generated within their field of view.

The spatial resolution in the tracking plane is naturally limited by the transverse diffusion of the ionization electrons during the drift time. In pure xenon at 10 bar pressure and at a typical drift field of 1 kV/cm, the maximum transverse diffusion in NEXT-100 is of the order of 10 mm, as drawn from [Biagi 1999]. This suggests a minimum spacing of 10 mm of the detection pixels in the tracking plane, leading to about 10^4 channels per m^2.

In a $\beta\beta0\nu$ event, the average number of primary electrons released by ionization of the gas along the track is about 300 electrons per mm (assuming an energy deposition of 70 keV/cm and a mean energy to produce an electron-ion pair in xenon gas of 21.7 eV [Dias et al. 1997]). For an incident drift velocity of 1 $mm/\mu s$, about 300 ionization electrons from a track directed along the drift direction will enter the EL region every microsecond. Each electron produces EL light for a time interval given by the gap size between the meshes divided by the drift velocity in the EL region. This is several microseconds for 5 mm gap and a reduced EL field of $E/p \sim 2.5\ kV\ cm^{-1}\ bar^{-1}$. For this typical EL field value actually used in NEXT-DEMO prototype, the optical gain is about 1100 [Monteiro et al. 2007], thus the total number of EL photons produced is on average 3.3×10^5 per microsecond. The tracks less parallel to the drift axis contribute with a higher number of electrons per unit time within the EL gap and the number of EL photons produced can be much higher.

A detection element of 1 mm^2 located at 5 mm distance from the EL region, in the direct view of a track parallel to the drift axis, will subtend a mean solid angle

fraction of 0.0016. Hence, about 460 $photons/\mu s$ will impinge on that detection area, assuming 88% transparency of the EL meshes. And is because that low light production we can use SiPMs, as explained on section 1.6.2. If we consider a SiPM of 1 mm^2 active area as a detection element, with 50% maximum photon detection efficiency (PDE), coated with TPB, the effective detection efficiency of the EL photons is about 22%, assuming 90% conversion efficiency of the coating and 50% reemission onto the SiPM surface. This estimation is compatible with the recent measurements of the effective PDE of a TPB-coated SiPM reported in [N. Yahlali et al. 2013]. Hence, a signal level of about 100 photoelectrons (pe) per μs is expected from SiPMs of 1 mm^2 active area and 50% maximum PDE, instrumenting a tracking plane located 5 mm behind the EL meshes. Then, as design requirement the dynamic range for the SiPMs were set to 250 $photons/\mu s$, leaving enough margin below the saturation level.

In this simple estimate, multiple scattering and diffusion of the drifting electrons are neglected. The imaging resolution of the tracking system depends on the distance between the meshes and the tracking plane. The smaller this distance the better is the imaging resolution, provided the illumination level on the SiPMs is below their saturation limit and within the dynamic range of the readout electronics. In the NEXT-DEMO prototype this distance is set to 10 mm, which is the maximum available space for positioning the tracking plane behind the EL grids in the TPC. The information of the 3D coordinates of the tracks provided by the tracking pixels should be completely registered for the analysis of the event topology. This requires that the events are recorded for the entire drift time in the TPC, typically 300 μs in NEXT-DEMO.

2.2 From Mother and Daughter Boards to CuFlon DICE-Boards

As explained on section 1.3, the first commissioning of NEXT-DEMO used a PMT tracking plane, because it was a technology more developed in the field and simplified the understanding of the whole detector on its beginnings.

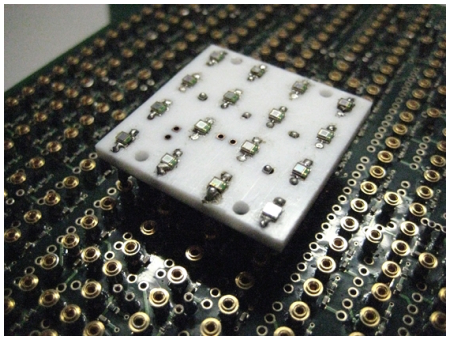
In the second phase towards the development of the NEXT tracking system, 248 SiPMs of 1 mm^2 active area were used for instrumenting the tracking plane. Two MPPC types from *Hamamatsu*, *S10362-11-025P* and *S10362-11-050P* [Hamamatsu 2015], were considered.

The outstanding features of the MPPC *S10362-11-025P* are pixel size of 25 $\mu m \times$ 25 μm, gain of 2.75×10^5 at the nominal voltage of $\sim$ 71 V (typical over-voltage of 1.5 V) and at 25°C, typical photon detection efficiency (PDE) indicated by Hamamatsu of 25% at 440 nm, and a wide linearity range due to its high number of pixels (1600). The recovery time of the APD pixels of this MPPC indicated by the manufacturer is typically 20 ns. The second MPPC considered, *S10362-11-050P*, has larger pixel size of 50 $\mu m \times 50$ μm, higher gain of 7.5×10^5 at a similar nominal voltage, and higher PDE of typically 50% at 440 nm indicated by Hamamatsu, which enable a substantial increase of the photoelectron (pe) resolution in the readout electronics. However, this MPPC has a higher dark noise level and lower linearity range, due to its lower number of pixels (400). The recovery time of the APD pixels in this case is typically 50 ns. The typical PDE values indicated by Hamamatsu are measured using the photocurrent method in which the contribution of optical crosstalk and after-pulses cannot be subtracted [N. Yahlali et al. 2013] [Vacheret et al. 2013]. The true PDE values of the considered MPPCs free of after-pulsing and crosstalk contributions reported in references [Eckert et al. 2010] [Vacheret et al. 2013] are about 30% lower than those indicated by the manufacturer.

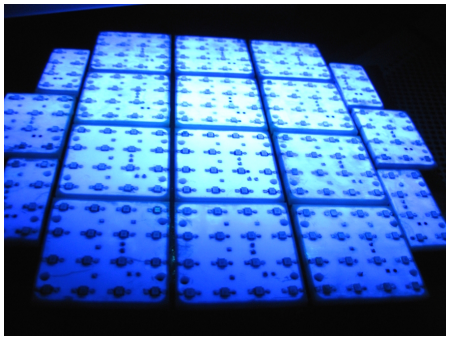
The after-pulsing probability we may expect from the MPPCs considered has been measured and reported in [Eckert et al. 2010]. It is about 2% for the MPPC *S10362-11-025P* operated at a typical over-voltage of 1.5 V, and about 7% for the MPPCs *S10362-11-050P* operated at a typical over-voltage of 1 V. The after-pulsing rate may deteriorate the photon-counting resolution of the MPPCs and thus their absolute charge information. However, the determination of the absolute charge truly induced by the EL photons is not required for tracking. The useful tracking information is provided by the relative charge measurement of the SiPMs array.

SiPMs of both types were arranged to cover a circular plane of 16 *cm* diameter with 1 *cm* spacing between the photosensors. Two different arrangements and biasing configurations of the SiPMs were developed for the tracking plane, to be tested in NEXT-DEMO with the aim of assessing the development of the NEXT-100 tracking system.

The first SiPM arrangement used the MPPCs of type *S10362-11-025P*. These were soldered onto 18 daughter-boards (DB) of 38×38 mm^2 maximum size (see figure 2.2a) made of CuFlon, which is a compound of PTFE of 3.18 *mm* thickness and electroplated with 35 μm of oxygen-free hard copper. CuFlon has the advantage of high light reflectivity and low degassing, while its composition (PTFE and copper) is very radiopure. The DBs are plugged onto a mother-board (MB) as shown on figure 2.2a, which provides the mechanical support and the electronic circuits for biasing the photosensors. Different DB geometries containing up to 16 SiPMs were built to fit the area of the tracking plane as shown in figure 2.2b. The DBs were coated with vacuum-evaporated TPB, following the protocol described in [Álvarez et al. 2012d].



(a) *Picture of a CuFlon daughter-board with 16 SiPMs, plugged onto the mother board.*

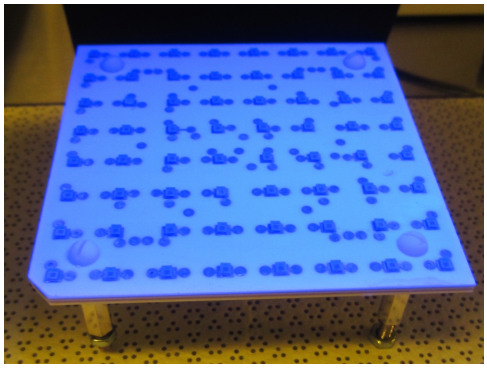


(b) *Picture of the 18 SiPM daughter-boards of NEXT-DEMO tracking plane, coated with TPB and illuminated with a UV lamp, emitting at 254 nm.*

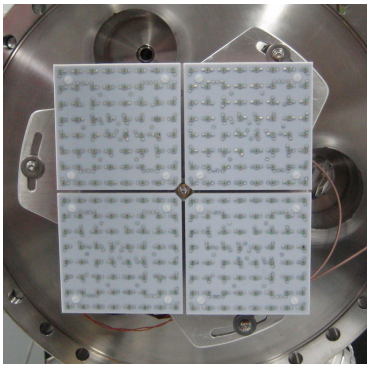
Figure 2.2: *CuFlon boards on the first NEXT-DEMO SiPM tracking plane. Different DB configurations, containing* 4×4, 2×4 *or* 3×4 *SiPMs, are arranged on the mother-board to cover the tracking plane.*

The second SiPM arrangement used the MPPCs of type *S10362-11-050P* to populate a different version of the CuFlon SiPM board of 79×79 mm^2 area,

so-called DICE-Board, shown in figure 2.3a. The DICE-Boards comprise 64 SiPMs and the electronic circuits and components for their biasing. These were selected with the requirement of radiopurity, mainly replacing the small ceramic capacitors used for individual SiPMs in the mother-board by large and less radioactive tantalum capacitors used for groups of 16 SiPMs. Four of these dice-boards units are used to cover the area of the tracking plane in NEXT-DEMO, as shown on figure 2.3b.



(a) *Picture of a DICE-Board with 64 SiPMs, coated with TPB and illuminated with 254 nm photons. The converted light from the TPB layer is blue (430 nm). The DICE-Board contains the electronic circuits and components for biasing the SiPMs.*



(b) *CuFlon DICE-Boards arranged to cover the NEXT-DEMO tracking plane. Notice the UV LED on the geometrical center for calibration purposes.*

Figure 2.3: *CuFlon boards on the second NEXT-DEMO SiPM tracking plane.*

The SiPMs in each board were biased using one common operating voltage, taken as the average nominal voltage of all the SiPMs in the board. This biasing option is driven by the necessity of reducing the number of voltage channels and the overall cost of the tracking system due to the high number ($\sim$ 7000) of SiPMs in NEXT-100. The common bias introduces, however, a gain dispersion within the SiPM boards, that can be minimized by an adequate selection of the SiPMs. Choosing them properly using the parameters provided by the manufacturer, the maximum gain dispersion achieved on a single daughter-board was 3.6% [Álvarez et al. 2012a].

Also, the SiPM gain is very sensitive to temperature variations. For a given value of the reverse bias, the gain is shown to decrease by a factor of 2 for a temperature increase of $10°C$ [Marrocchesi 2009]. The thermal agitation in the SiPM dissipates the energy of the charge carriers, which inhibits their collection and decreases the gain at a fixed reverse voltage. This temperature dependence of the gain can seriously impair the photon counting capability of the photosensors and have a negative impact on the charge measurements in the NEXT tracking detector. For this reason the collaboration designed its own bias supply, which performs active bias regulation as a function of temperature, as is detailed on Chapter 7.

2.3 Front-end and Readout Electronics

The typical drift velocity of the electrons along the longitudinal axis (z) of the NEXT-DEMO TPC is 1 $mm/\mu s$ [Álvarez et al. 2012b]. Thus sampling the EL signals at a rate of 1 MHz with an ADC provides a resolution of 1 mm in the z coordinate. The processing of the SiPM signals is performed by a 16-channel front-end (FE) board (figure 2.4) including 16 analog paths and a digital section. Each analog path consists of three stages. The first stage is a transimpedance amplifier which converts the SiPM current into a voltage signal providing a gain of 1.5 V/mA and baseline adjustment. The second stage is a gated integrator with 22 ns RC constant and a nominal integration time of 1 μs, which acts also as low pass filter and BLR (BaseLine Restorer). An offset control at the first stage enables the optimization of the integrator dynamic range. The third stage is an inverter with a gain of 1.2 required to produce a positive signal at the ADC input. An offset correction is included at this stage since the integrator introduces an output deviation. The first two stages were manufactured using the *OPA659* operational amplifier, and the last one with the *OPA842*, both from *Texas Instruments*.

The signals obtained in the outputs of the analog paths are digitized at a rate of 1 MHz using 12-bit ADCs. In the digital section, a configurable FPGA (*Xilinx Virtex-5 LX50T*) is used to read the ADCs, control the switches in the gated integrators (*ADG719* in figure 2.5), build a frame with the digitized data

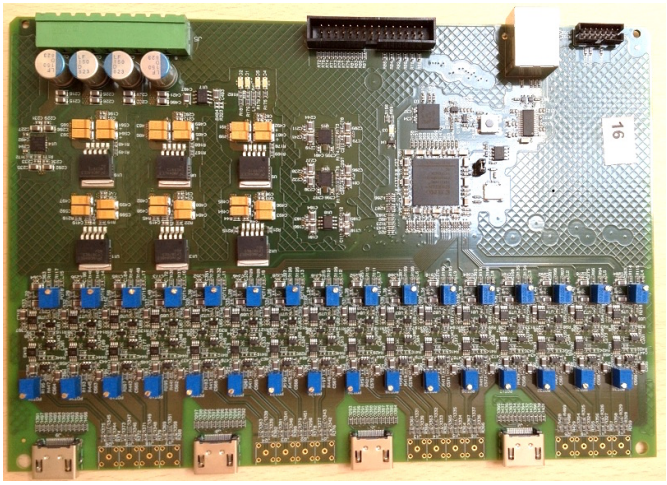


Figure 2.4: Picture of the SiPM front-end card.

and communicate with the upstream readout stage through a standard RJ-45 connector and cable. Careful PCB layout techniques ensure that the digital section introduces very little noise in the analog stages.

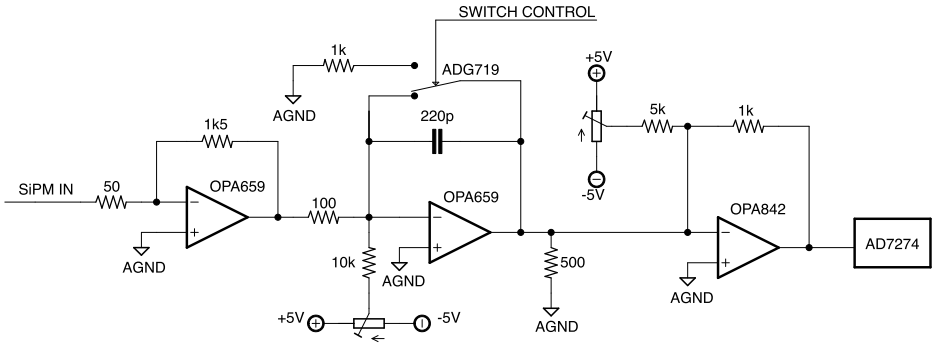


Figure 2.5: Schematic of the front-end analog stage (simplified).

The gains in the three stages of the analog sections have been set to obtain an output level which can resolve single photoelectrons. For the system to have this

resolution the output voltage obtained from a single photoelectron (pe) should be higher than the equivalent output noise of the circuitry which has a typical standard deviation of 2 mV. The gain values at the different stages are set to obtain a voltage level of 17 mV/pe for signals from SiPMs type *S10362-11-50P* and about 5.6 mV/pe for signals from SiPMs *type S10362-11-25P*.

The front-end cards are readout by the Front-End Concentrator (FEC) card, designed within a joint collaboration between CERN-PH-AID and NEXT in the framework of the RD-51 Collaboration [Toledo et al. 2011] [Chefdeville 2011]. Up to 16 front-end cards can be connected to the FEC module, resulting in 256 channels, which is enough for the NEXT-DEMO prototype. This readout system can be scaled up for NEXT-100 by simple addition of FEC cards. The data is sent to the data acquisition PC via gigabit Ethernet links.

The front end electronics in NEXT-DEMO are placed outside the chamber for reasons of space inside the TPC and accessibility of the front end cards for development studies and maintenance. These cards are placed close to the detector in order to minimize signal losses through cables.

2.4 Results

A few years after commissioning, the results and knowledge acquired with the NEXT-DEMO prototype show that the collaboration understands the technology and now is ready to work on the next step: the NEW prototype. Some of the results obtained related with the tracking capabilities with the NEXT-DEMO tracking plane are the following [Lorca 2015] [Álvarez et al. 2013b]:

Calibration

The first challenge of the tracking plane was to be able to be calibrated, as the rest of the analysis depends on this feature. The absolute gain of the SiPMs was calculated prior to their introduction in the TPC using their single photon response to illumination with a 400 nm LED, achieving a gain spread between 2% and 3.6% at their nominal voltages. However, due to the posterior addition

of a wavelength shifter coating (TPB) over the SiPMs, to make them sensitive to the xenon scintillation light, together with the addition of the electronic read-out chain, an independent calibration is required to give a true representation of the relation between photoelectrons (pes) and ADC counts.

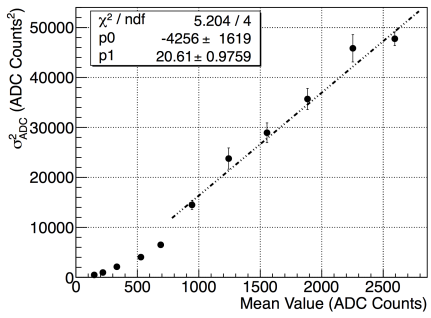
A measurement of the dark current of the SiPM channels would provide directly the conversion factor. However, once the tracking plane was introduced inside the detector, an increase in the noise levels was observed, represented by the fluctuations in the baseline of one electronic channel. The origin of this noise was identified as the electrical facility of IFIC where all electronics were connected, and bursts of about 3 kHz with a few MHz noise were identified on the mains power supply. This noise is transferred by capacitive coupling to the readout distorting the baseline.

For this reason, three independent techniques are introduced here to perform the calibration or equalization of the SiPMs: the response of the SiPMs to X-ray depositions present in data, the photon transfer curve technique using a blue (400 nm) LED and the common noise filtering.

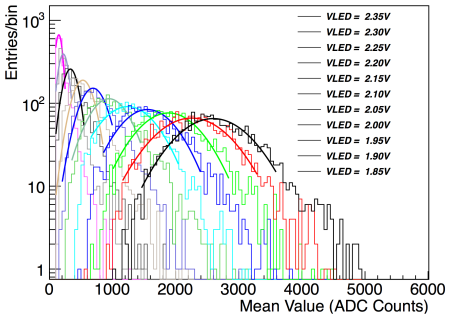
X-ray energy depositions have been identified as a useful resource for the homogenization of the SiPMs response. Such events are produced by the 30 keV electrons extracted by gamma rays coming from external sources. These events are very abundant during data taking, providing thousands of depositions distributed all around the active volume of the detector. The range of those e^- at 10 bar is $\sim$ 0.6 mm, which by multiple scattering deposits all its energy where are produced. The blob of charge produced drifts toward the anode due to the electric field present in the chamber, where produces EL light. Since the SiPMs that form the tracking plane are located just a few millimeters away from the EL generation region, the forward photons tend to be concentrated in few channels. Considering as estimator of the energy released in each recorded event only the channel with maximum charge, a low energy spectrum is reconstructed for each channel, which exhibits a peak corresponding to the X-ray energy. The 30 keV peak is fitted, and its mean value used to characterize the response to X-rays. The position of the X-ray peak is different for each channel. These differences are used to homogenize the response of the SiPMs, slightly modifying the original

gain of the sensors. Once gains are modified, the correlation between both planes changes, achieving a linear response between the two planes.

As an additional method of absolute determination of the gain in the absence of the dark current method, the Photon Transfer Curve (PTC) method using a blue LED is proposed. A random noise can be associated to the read-out channel and its processing electronics, and represents the baseline noise in total darkness. Illuminating the SiPM, as the input light level increases in amplitude, the noise at the system output rises out of the baseline noise and becomes dominated by shot noise. The Photon Transfer Curve is shown in figure 2.6a for an individual read-out channel, and illustrates the various noise regions. During the PTC measurements, the SiPM was exposed to a blue LED located at the TPC cathode producing an uniform illumination, and pulsated at different voltage amplitude values. The digital SiPM response (S_{ADC}) at different intensities is represented on figure 2.6b.



(a) *Photon Transfer Curve of a SiPM and linear fit in the shot noise region obtaining the absolute gain of the system.*



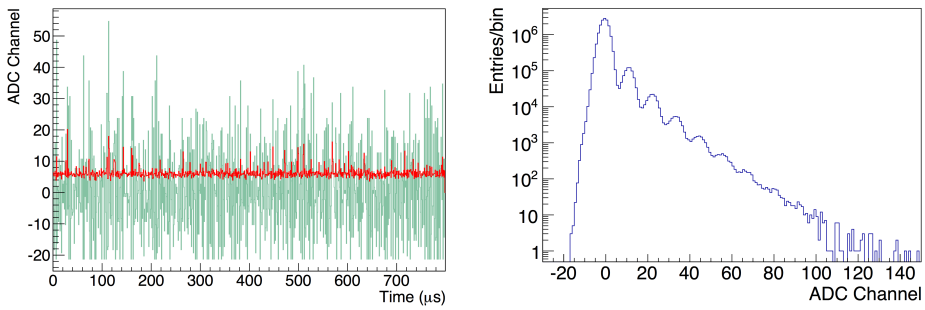
(b) *Average response of the SiPM at different illumination levels of the LED and gaussian fit to the mean value.*

Figure 2.6: *Gain calibration with the PTC method.*

The gain values obtained with the PTC method match perfectly with the values calculated during the external calibration using dark count events, making of this method useful for further monitoring of the gain during the data taking.

The last technique used is the Common Noise Filtering (CNF) method, based on the idea that the noise induced in the electronics has a common pattern since

the source of the noise is common to all channels even if their response is not the same. The main idea of this method is to identify the common noise in a group of channels (typically 4 or 8 channels of the same row, which share the same cables all the way) and subtract it. First the baseline offset of each channel is subtracted, the distribution is fitted to a Gaussian curve, and then the channels are normalized. The signal recorded by electronics is actually the sum of the signal generated by SiPMs plus the pickup noise in the system. The fact that dark count events are produced randomly following Poisson statistics, makes these events uncorrelated with the pickup noise, and this the latter can be subtracted leaving only the relevant information of the SiPMs. This is shown in figures 2.7a and 2.7b, where a waveform of a biased SiPM is represented before and after the CNF model is applied. Once subtracted, dark count events are clearly visible, allowing the construction of the Single Photon Spectrum (SPS) with peak identification and therefore, the sensor calibration.



(a) *Waveform of a biased SiPM with dark count events before (green) and after (red) CNF is applied.*

(b) *Single Photon Spectrum obtained with DK events after CNF.*

Figure 2.7: *Gain calibration with the CNF method.*

The correlation within the absolute constants obtained by applying the CNF method is similar to the one obtained with the other methods, ensuring the reliability of the three methods described in this section.

Tracking reconstruction

Using the event timing and the barycenter calculated using the total integrated signal in each SiPM, it is possible to obtain an estimation of the position of the energy deposit associated to the interaction of a particle. This definition is a good approximation when the particle behaviour is point-like, as is the case for x-rays. However, the electrons produced by the interactions of the 511 keV photons emanating from the ^{22}Na calibration source are not necessarily point-like. They have finite probability to travel several centimeters in the gas. For instance, the majority of the charge in ^{22}Na events tends to be concentrated within 4 μs either side of the time sample (μs width slice) with maximum charge. Defining this region as the "blob" and calculating the position of this deposit compared to that calculated from the full integrated charge of the event, the global position is still a good estimator of the position of the energy deposit.

A more involved reconstruction is required to understand the actual topology of individual events. A first approximation of the event topology can be made by subdividing, to a minimum width of 1 time sample, the charge in time. This allows for a deeper understanding of an event's z structure and is the starting point for track reconstruction.

For the analysis presented here, slices of 4 μs width were used, on the grounds that this width is comparable to the width of the blob, as defined above, and the time an electron needs to cross the EL region ($\sim$ 3 μs). In addition, the charge collected in a 4 μs width window is sufficient to achieve a reliable xy reconstruction. Each time slice, while having a single z coordinate, can be comprised of multiple x, y points. In this analysis a single xy point is reconstructed per slice and those events exhibiting slices with more than one isolated charge deposit in the tracking plane are excluded from analysis until a more sophisticated clustering algorithm is developed.

The xy position of a slice is reconstructed using its barycenter. This position then has the energy recorded in the cathode for the same time interval associated with it so that the event dE/dz can be studied. The energy and position information

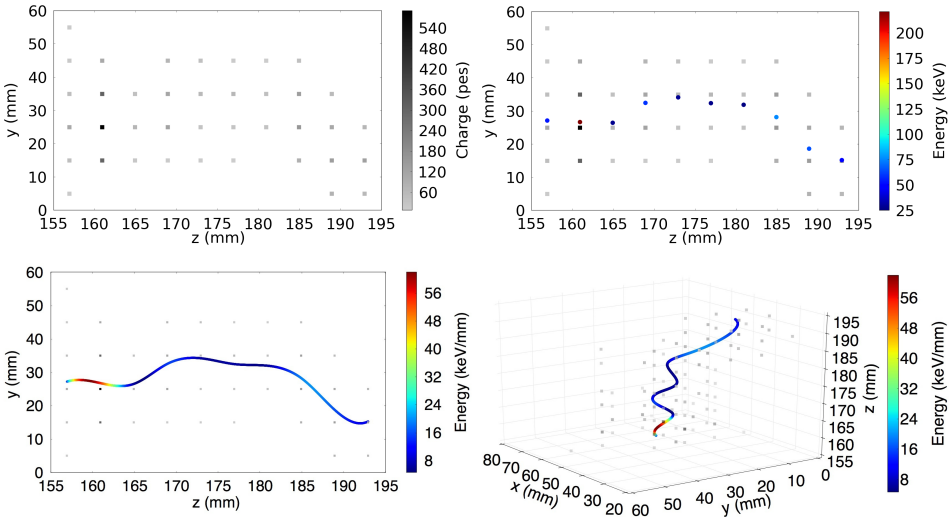


Figure 2.8: Example of the reconstruction of a ^{137}Cs track: The charge of the different SiPMs is split into slices of 4 *mm* width in z (top left). One point is calculated for each slice using the barycenter method and the energy of the points is then associated with the measurement made in the cathode (top right). A cubic spline is used to interconnect the different points. The result is shown in the bottom line: yz projection (bottom left) and 3D image (bottom right) of the reconstructed track [Álvarez et al. 2013b]

are then used to calculate a cubic spline between the individual points in order to obtain a finer description of the path.

Figure 2.8 illustrates the method applied to the reconstruction of a ^{137}Cs photoelectric event. The reconstructed electron trajectory presents all the features found in the Monte Carlo: a tortuous path due to multiple scattering, a "wire" region of MIP (Minimum Ionizing Particle) deposition and a blob of high energy deposit towards its end.

2.5 State of the art in SiPM Front-end Electronics

When the NEXT experiment started SiPMs were a novel technology and their use was not as expanded as today, used mainly for optic fiber applications and strip-based trackers.

This kind of applications do not need high accuracy on the charge provided by the SiPMs, as they just need short time response and roughly the signal size. Almost all experiments preceding NEXT used an ASIC (Application-Specific Integrated Circuit), because they provide a very compact and low power solution that fits the requirements (some of them introduced on section 1.6.3). Of course we explored the current solutions, back in 2011, hoping that one of the already produced ASICs could fit our main specifications: high channel density, gated integrator scheme, low power and in-chip digitization.

The available readout techniques can be divided in two different methods: sampling and time-based readout. While the first method may achieve best energy resolution it also adds extra complexity. On the other hand, the time-based readout allow better time resolution but makes difficult to manage waveforms with unknown shape. As explained before NEXT does not need a very precise time resolution, but a reliable energy resolution is desirable. Both requirements lead to choose the sampling method, but combined with an integrator stage in order to reduce the sampling frequency needed.

Some ASICs as the "ROC" family (MAROC, SPIROC) were focused on the trigger detection, not in the charge resolution. Other options intended for PET (Positron Emission Tomography) applications used the "time over threshold" technique to estimate the input charge, which is not useful for us if we are managing signals with different shapes and lengths.

After a thorough search of available ASICs we decided to design our own discrete front-end electronics, as there were no electronics available that fit all our specific characteristics. And, as far as we know, we were the first to do it for a SiPM tracking plane. We though also about producing our own ASIC, but

ASIC	Application	Channels	Dynamic Range
FLC_ SiPM	ILC analog HCAL	18	-
MAROC2	ATLAS	64	80 pC
SPIROC	ILC HCAL	36	2000 pe
NINO	ALICE ToF	8	2000 pe
PETA	PET	40	-
BASIC	PET	32	70 pC
SPIDER	SPIDER RICH	64	12 pC
RAPSODI	SNOOPER	2	100 pC

Table 2.1: *Some of the available SiPM dedicated readout chips by 2011 [Kucewicz 2011].*

we were still learning the prototype performance and a long term production seemed too risky.

"Give me six hours to chop down a tree and I will spend the first four sharpening the axe."

– Abraham Lincoln

3

From the Beginning: Front-end Prototype

This chapter focuses on the analog stages of the silicon photomultiplier front-end, from the input to the ADC. The design starts based on the previous front-end developed for NEXT-DEMO, but conditioned by new requirements and improvements for NEW and NEXT-100; such less board size, larger channel density, less power consumption and cheaper components. Finally, due to the needs of noise reduction explained on Chapter 6, the system became differential and the front-end analog stage evolved to read this kind of signals.

3.1 First Scheme

The first design for the SiPM reading was intended to operate with the NEXT-DEMO detector, and validate the gated integrator method. According to the design requirements explained on Chapter 2, the front-end electronics for NEXT-DEMO were developed, and two versions of the board were produced. The last one, which improves the performance of the first version, was able to read the signals from 16 SiPMs, integrating the signals and digitizing them at 1 MHz.

As detailed on section 2.3, the front-end board has 16 analog blocks as the one showed on figure 3.1. The switch and the ADC are controlled by the *Xilinx Virtex-5 LX50T* FPGA, which also pack the data and send it to the FEC card (Front-End Concentrator).

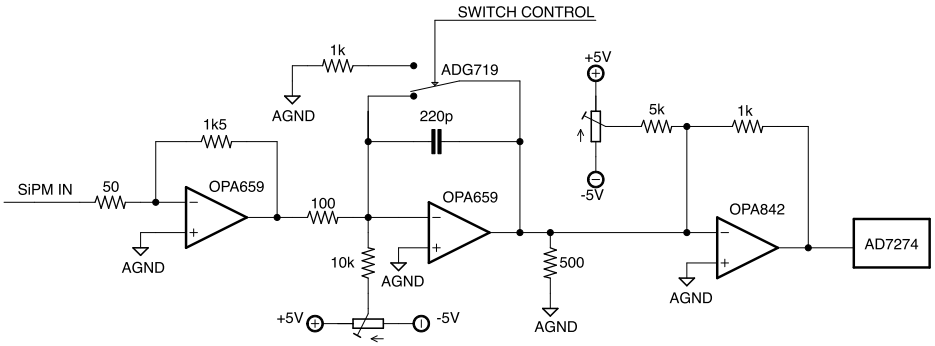


Figure 3.1: *NEXT-DEMO SiPM front-end board analog channel (simplified).*

On this front-end, the operational amplifiers (OPA) used were the *OPA659* and *OPA842* from *Texas Instruments*. These OPAs guaranteed a very good performance on bandwidth and low noise for this stage of the experiment, but its power consumption made non-viable to use them while the detector scales up.

Nevertheless, it validated the gated integrator scheme and the data acquisition system, and lead the way for the upcoming electronics on NEW and NEXT-100.

3.2 Single ended Scheme

For the new SiPM front-end electronics the main idea is to simplify the design, reducing the cost and the physical size of each channel; so more channels can be included on each board. If possible, another objective is to reduce the noise of the electronics, improving the chain resolution; and reduce the power consumption as much as possible, without losing performance. The goal is to produce a 64 channel front-end board with the same power consumption than the old one (which has only 16 channels), and better performance.

3.2.1 Circuit

The starting point of the new analog electronics was a simplification of the scheme, while keeping the features. As we learned that the gated integrator worked as expected, we removed the last amplification stage and compensated the total gain in the two remaining stages. Also, as the manual baseline adjustment is non-viable for thousands of channels, we introduced a DAC (Digital to Analog Converter) at the gated integrator input for automatic baseline adjustment, as shown on next picture:

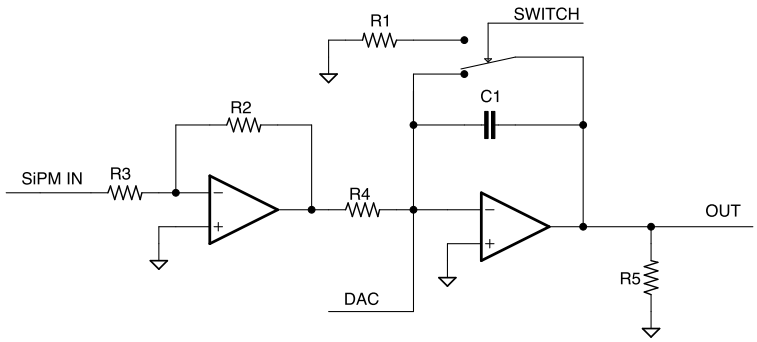


Figure 3.2: *SiPM front-end channel single ended scheme proposal (simplified).*

The first stage is a transimpedance amplifier, which allows to convert the SiPM current signal into a voltage signal. The resistor R_3 is used to attenuate signal

reflection, and the resistor R_2 fixes the gain of the transimpedance amplification stage.

Then the resistor R_4 converts the voltage signal back to a current signal before the second stage.

$$I_C = \frac{V_{OUT1}}{R_4} = \frac{-I_{SiPM} \cdot R_2}{R_4} \tag{3.1}$$

Where I_C is the current through the capacitor $C1$ on figure 3.2. The second stage is a gated integrator controlled by the switch, which allows the charge and discharge of the integrating capacitor C_1. During the integration time the switch is connected to the resistor R_1, so the capacitor is charged by the current signal from the first stage:

$$I_C = C\frac{dV_C}{dt} \quad \longrightarrow \quad V_C = \int \frac{I_C}{C} dt \quad \longrightarrow \quad V_{OUT} = -V_C = \int \frac{I_{SiPM} \cdot R_2}{C \cdot R_4} dt \tag{3.2}$$

At this point of the project we were evaluating two SiPM models, the model *S10362-11-050P* from *Hamamatsu* and the model *MicroFC-10035-SMT-GP* from *SensL*, as explained on section 1.6.2. From the point of view of the front-end electronics the only parameter that makes a difference between the two models is the gain, which is four times bigger on the *SensL* SiPMs; while the dynamic performance of both models is very similar. However, by this time we were more experienced with the SiPMs from *Hamamatsu* and we had some devices available for tests, so the front-end gain was calculated for the *S10362-11-050P* series. This will give us also a true comparison between the electronics developed for NEXT-DEMO and the new front-end, and changing the chain gain for other devices is not difficult.

This SiPMs have a nominal gain of $7.5 \cdot 10^5$ at $25°C$. This means that one single photon seen by a pixel produces $7.5 \cdot 10^5$ electrons, ergo produces a pulse with a charge of $7.5 \cdot 10^5\ e^- = 120\ fC$. As we want an output signal of $10 - 20$

ADC counts per photon detected (to keep the same dynamic range than NEXT-DEMO), we have calculated the best component values which result in this performance. So the final single photon response output for the analog chain is:

$$V_{OUT} = \int \frac{I_{SiPM} \cdot R_2}{C \cdot R_4} dt = Q \frac{R_2}{C \cdot R_4} = 120\ fC \frac{2.7\ k\Omega}{330\ pF \cdot 100\ \Omega} \approx 10\ mV \qquad (3.3)$$

The ADC dynamic range is the same than its supply voltage, so as we will show later we have 12 bits for 3.3 V. So the 10 mV integrated voltage will be seen as a $12 - 13$ ADC counts pulse by the readout electronics.

Every microsecond the capacitor is discharged; otherwise it would saturate the ADC input after few light events. For the discharge the switch connects both terminals of the integrating capacitor just 20 nanoseconds, in order to minimize the dead time of the system (only 2%[1] for this reset time). Just before the discharge, the ADC reads the output voltage and sends it to the FPGA via SPI communication.

As the operational amplifiers have some voltage offset error, the second stage has an offset adjustment branch controlled by a DAC. Adjusting the output voltage of this DAC we can add some current to the integrating capacitor and correct the system offset error. This process is made automatically by the FPGA, which reads the signal baseline and adjusts the DAC voltage systematically and achieves the final value after a few iterations (less than five seconds). The algorithm calculates the baseline value, given by the mean value of the channel along several microseconds. Then the DAC output is increased or decreased on each iteration, getting closer to the desired value. When the difference between the actual value and the desired one is higher than the first threshold, the steps added or subtracted are several ADC counts. Then, when the difference is smaller the steps are more precise, just one or two ADC counts, until the

[1]This value for the dead time assumes the ideal performance of the switch. However, as the behavior during connection and disconnection times are uncertain, the real dead time is between 14 *ns* and 24 *ns* (1.4% *to* 2.4%).

second threshold is reached. The algorithm adjusts the 64 channels (8 DACs of 8 channels each) one by one, moving the baseline within a small range close to the desired value. All the parameters can be easily tuned from the java interface, as will be detailed on section 4.7.

Switch

The chosen switch is the *ADG719*, which has very good characteristics. The fast switching times, only 10 *ns* for connection and 4 *ns* for disconnection, allows the fast capacitor discharge with minimum integration dead time. It has also high bandwidth and low resistance when connected, about 0.75 Ω typically, so the fast signals from the first amplification stage are not modified. The input is TTL CMOS compatible, which is directly compatible with the FPGA used. As it was mentioned before, most of the time the switch is disconnected, so the second stage integrates the input signal. Then, just after the ADC has acquired the integrated value of one microsecond, the switch turns on and discharges the capacitor.

On next figure the main signals of the designed circuit are shown:

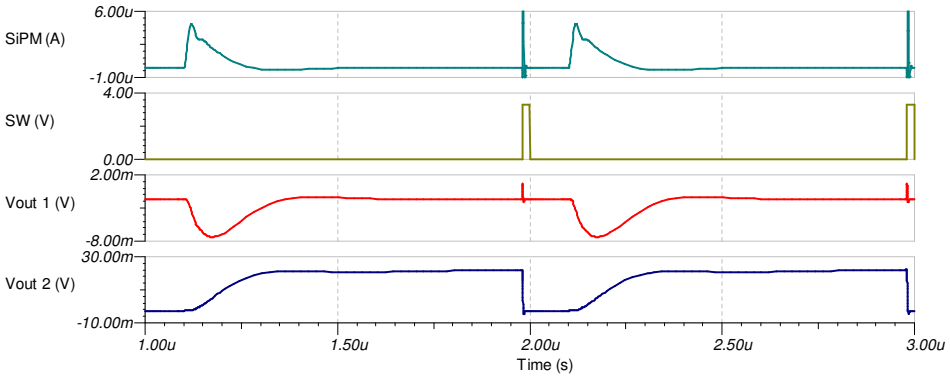


Figure 3.3: *Simulation of the front-end electronics analog conditioning.*

The first plot is the input current signal from the SiPM, produced by one pixel which has seen light, measured in the front-end input. V_{OUT1} is the output

voltage of the first stage, inverted as explained previously. And V_{OUT2} is the integrated signal after the second stage. The second one (SW) is the switch control signal, which discharges the integrating capacitor every microsecond, connecting both terminals during 20 ns. This signal produces small pulses on the input and output of the first stage, as can be seen in the first and third plots, but has no significant effect on them. As shown, the analog chain is working properly on the simulation, and the integrated signal is reseted to zero each cycle.

DAC

But as explained before, the operational amplifiers have some offset error, different for each device. So each channel needs a different offset correction. On the previous design each channel had a potentiometer which allows this, adding a little DC current to the integrating stage input. But for the final detector is not desirable to have $\sim$ 7000 potentiometers that must be hand adjusted. For this reason we have replaced the offset adjustment potentiometer by a DAC connected to the FPGA by an *I2C* port. The selected model is the *DAC7678* from *Texas Instruments*, which is a low power low error device, with 8 output channels and 12 bits resolution.

However, in the prototype developed we have kept the potentiometer adjustment as an option for test purposes, so the offset can be also modified when the DAC control is not enabled, just soldering one resistor or the other.

The values of the resistor divider, shown on the next picture, are calculated to provide a fine offset adjustment in an approximated range of $\pm 0.5V$.

So in the case that R_{19} is not soldered the offset correction is controlled by the DAC, giving a current through the R_{11} resistor to the integrating capacitor. The output current of the branch can be calculated as:

$$I_{offset} = \left(\frac{V_{DAC}}{R_{13}} - \frac{5}{R_{12}} \right) \cdot \left(\frac{1}{1 + R_{11} \left(\frac{1}{R_{13}} + \frac{1}{R_{12}} \right)} \right) \tag{3.4}$$

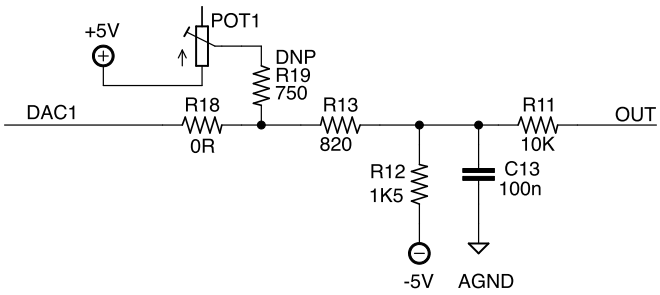


Figure 3.4: *Offset adjustment branch.*

As the DAC output can be adjusted from 0 to 5 volts, the output current of this branch can be set in the range from $-176.7\ \mu A$ to $146.6\ \mu A$ in steps of $79\ nA$. This current modifies the signal baseline slope, which is a voltage offset on the ADC data. According to the equations shown before, each step produces a voltage modification of:

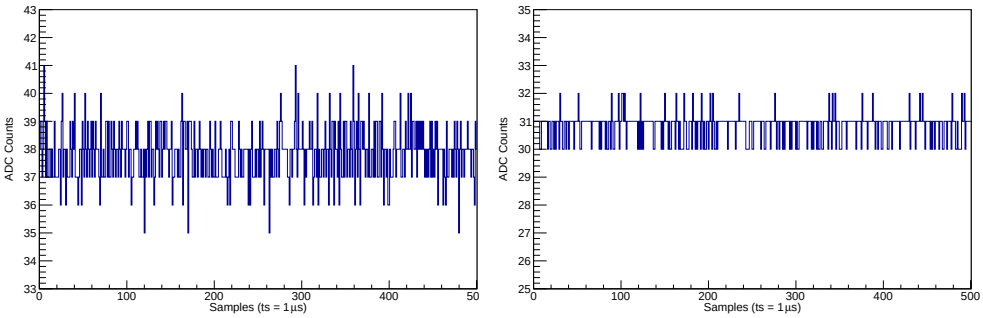
$$V_{offset} = \int \frac{I_C}{C} dt = I_{offset}\ t_{int}\ \frac{1}{C} = 79\ nA \cdot 980\ ns \cdot \frac{1}{330\ pF} = 235\ \mu V \qquad (3.5)$$

Where the integration time is $980\ ns$. This means that the offset can be adjusted from $-525\ mV$ to $435\ mV$ in $235\ \mu V$ steps, which is less than 3 times smaller than one ADC count, and allows a very precise adjustment.

For the automatic offset correction, the FPGA obtain the mean value of the signal baseline, without connecting the SiPMs bias supply. Then at each iteration adds or subtracts a number of DAC counts, given by the parameter called `Step H`. When the difference between the desired baseline and the actual one is smaller than this parameter, the value that is added or subtracted is given by the parameter `Step L`. The process is stopped when the measured baseline is the desired, or in the range of acceptance.

ADC

About the ADCs, on the previous design we used the *AD7274*, which is a low power 12 bit analog to digital converter. But for the new design a second ADC was included in the prototype, with a smaller footprint, less power, less error and lower price; the *ADS7883*. The idea is to compare both ADCs, and check if the new one is suitable for the new front-end electronics.



(a) *AD7274 without input signal.* **(b)** *ADS7883 without input signal.*

Figure 3.5: *ADC comparison.*

With the same analog chain, both ADCs had the same performance (maybe the new one has a little less noise, but the final result depends on the full chain overall performance, studied later). So as the *ADS7883* has some advantages we decided to use it for the new design.

Operational Amplifiers

For the operational amplifiers selection, the main characteristics needed for the new front-end boards are low noise, low power and low cost. Some of the devices selected are the ones shown on the next table:

OPA	Power (mA)	Noise ($nV/\sqrt{Hz}$)	Cost/u (>1000 u)
ADA4895	3	1	2.69 €
LMH6654	4.5	4.5	0.84 €
LMH6624	12	0.92	1.71 €
OPA659	32	8.9	2.95 €
AD8055	5	6	0.86 €
LM7121	5.3	17	1.42 €
LMH6702	12.5	1.83	1.44 €
OPA656	16.2	7	5.81 €
THS3201	19	1.65	3.11 €

For the first design the best option seems to be the *ADA4895*, due to its low noise and very low power consumption. But simulations reveal that this device does not support the integrator scheme of the second stage due to the capacitive load, and the output oscillates. Keeping the *ADA4895* on the first stage and replacing the second stage by the *LMH6654* simulations were successful. So we proceed to mount them on the real circuit prototype; but the second stage oscillated again, probably because this type of fast low noise amplifiers are very sensitive to the board layout, and any parasitic capacitance on the input or output pins can make the output oscillate (even though the manufacturer recommendations were applied).

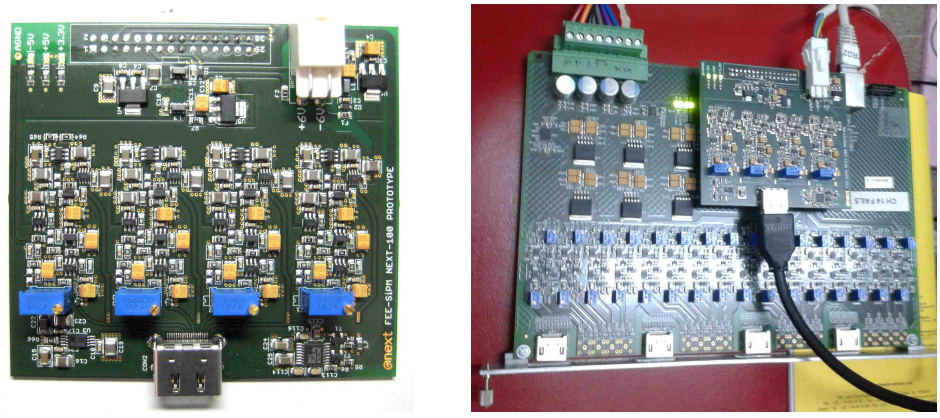
Unfortunately, the SPICE models for simulation are not perfect, and they can not predict the parasitic effects due to the board layout. This may cause, as in our case, that a configuration which works properly on simulation oscillate when mounted on a PCB.

Other operational amplifiers were tested, and some of them also oscillated. The *OPA659* worked properly, and allowed us to verify that the circuit worked and we could take some data. But this device has a high power consumption, which is not desirable for our application. For this reason more operational amplifiers were tested, and finally we found one that works properly, with a very good combination of low power, low noise and low cost: the *AD8055*. The results with this amplifier were very promising, both on the simulations and on the real circuit board. As this device can be also bought in a dual amplifier package,

the first stage was also replaced by this one, which shown a lower output noise. Although the *ADA4895* has, theoretically, a lower noise and consumption, the dual amplifier package of the *AD8055* allows us to reduce the board layout size, is also a cheaper option and seems to have less noise once we tested it with real signals.

3.2.2 Results

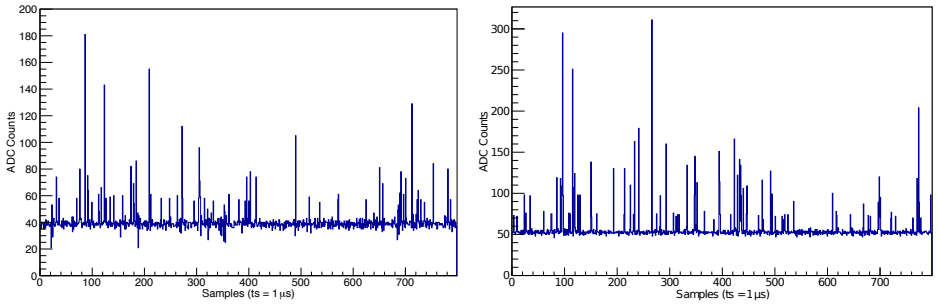
Once the prototype was finished it was connected to the system. The prototype was designed to be plugged in the expansion port of the old front-end board, so the control lines of the first four channels can be redirected to the expansion port. This allows us to make work the four prototype channels and acquire its signals. For the tests we used a temperature controlled black box, with four SiPMs inside. All the measurements were taken at $20°C$.



(a) *Front-end 4 channel prototype.* **(b)** *Prototype plugged on the old front-end board.*

Figure 3.6: *Front-end prototype.*

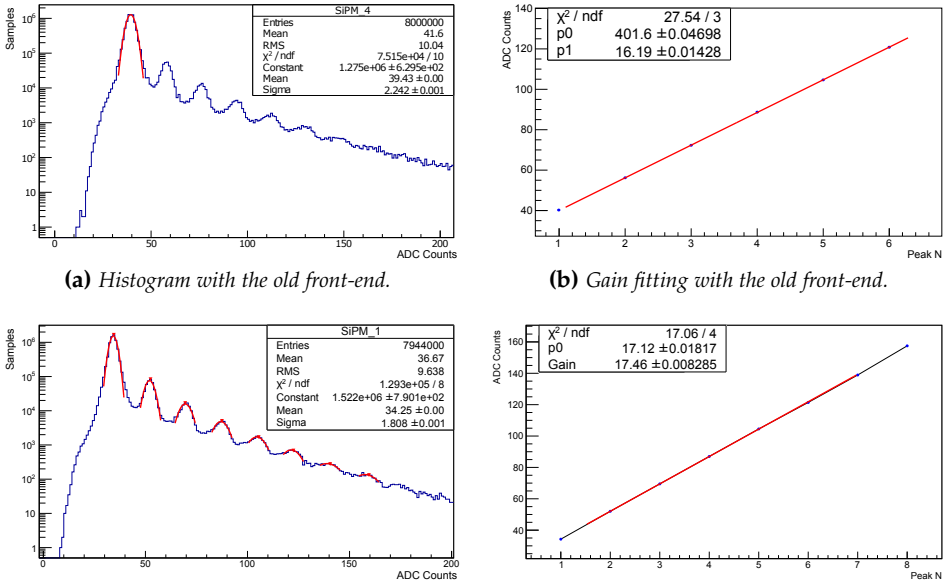
As shown on figure 3.7, the waveform with the new front-end prototype seems to have less noise than the old one. This is because the new operational amplifiers are less noisy, the new ADC has better performance, and there are two stages instead of three.



(a) *Waveform with the old front-end.* **(b)** *Waveform with the new front-end (*AD8055*).*

Figure 3.7: *SiPM front-end waveform comparison.*

With this data we can plot the photoelectron spectrum of each SiPM, which allows us to obtain the gain of the device and the analog chain (figure 3.8).



(a) *Histogram with the old front-end.* **(b)** *Gain fitting with the old front-end.*

(c) *Histogram with the new front-end.* **(d)** *Gain fitting with the new front-end.*

Figure 3.8: *Resolution and gain comparison for the old and new electronics.*

To compare the resolution and/or the noise of the system, we look at the sigma parameter of the baseline fitting. Then, the gain can be calculated from the slope

of the line defined by the Gaussian fitting for each histogram peak, as explained on section 1.6.2. For the old front-end the sigma obtained is about 2.2, while with the new one is 1.8. The gain is more or less the same for both electronics, and can be easily adjusted without affecting the sigma of the histograms.

3.2.3 Conclusions

As described in previous section, the chain resolution has been improved with the new electronics. So as we want at least the same performance, this is a very good result.

About the power consumption of the analog chain:

- The old front-end has two OPA659 and one OPA842 $\longrightarrow$ 86 mA
- The new front-end uses two AD8055 $\longrightarrow$ 10 mA

This means a power reduction by a factor 8.6.

About the price per channel the tables below summarize the cost of each front-end, showing also a great cost reduction.

Old Front-end	
Device	Price
OPA659	2×2.95 €
OPA842	1.60 €
AD7274	6.58 €
ADG719	0.75 €
TOTAL	**14.80 €**

New Front-end	
Device	Price
AD8055	2×0.86 €
ADS7883	2.25 €
ADG719	0.75 €
TOTAL	**4.72 €**

So it has been demonstrated that the new front-end electronics scheme has a lot of advantages compared with the old one, like the resolution, power consumption, price and layout size. But this prototype was tested in a small and controlled setup, where the conditions are almost ideal. Later, when we tested the front-end prototype inside the clean room together with all the NEXT-DEMO electronics and computers, we figured out that this scheme is very susceptible

to the environmental radiated noise, same way that it was for the NEXT-DEMO SiPM front-end (section 2.4). For this reason, we had to move the design to a differential transmission readout, as explained on the following section.

3.3 Moving to a Differential input Scheme

The main problem in NEXT-DEMO SiPM front-end electronics was the huge noise coupled to the SiPM signals, which made difficult the calibration of the photosensors and the data processing; as explained on section 2.4. Using advanced methods, as the Common Noise Filtering, X-ray deposition or the Photon Transfer Curve, we were able to understand the tracking plane and successfully took data. But for the upcoming detectors NEW and NEXT-100 the amount of SiPMs increases a lot, so it does also the complexity of the system. As the new detectors will be inside the lead castle, the length of the cables increases a lot, $\sim 6\ m$ from the SiPM to the front-end.

For this reason we were forced to improve the scheme and achieve a more robust design, which brought us to the differential scheme.

As can be seen, the differential scheme shown on figure 3.9 is almost the same than the single ended scheme previously explained. The main difference consists in the input, even before the first amplification stage.

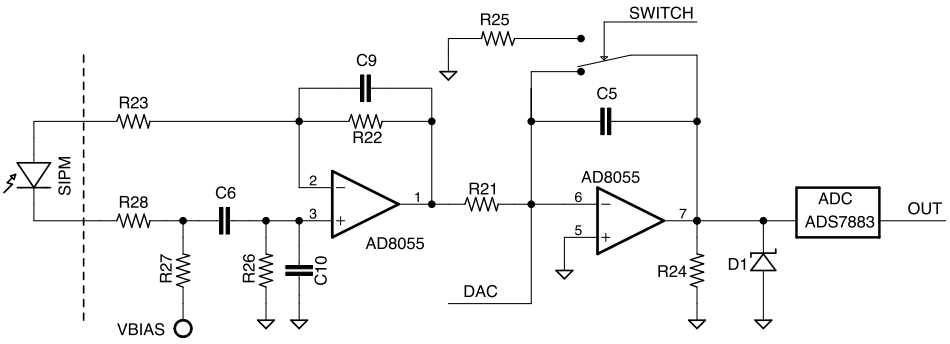


Figure 3.9: *Differential SiPM front-end channel (simplified).*

The circuit now has two inputs, connected directly to the SiPM anode and cathode. So the effect is that now we have doubled the signal, because the same current flows in both terminals, but in the opposite direction.

For the values calculation, the scheme concept can be simplified a lot. R_{26} and C_{10} must be the same values than R_{22} and C_9 in order to balance the input, and these resistors define the first stage gain; which now can be calculated as:

$$I_C = \frac{-I_{SiPM} \cdot (R_{26} + R_{22})}{R_{21}} \quad \longrightarrow \quad V_{OUT} = \int \frac{I_{SiPM} \cdot (R_{26} + R_{22})}{C \cdot R_{21}} dt \tag{3.6}$$

Where I_C is the current through the capacitor C5 on figure 3.9. Both R_{22} and R_{26} were set at half the value of the previous scheme, so the final gain remains the same.

R_{23} and R_{28} are both 100 Ω to attenuate signal reflection. The function of C_6 is to decouple the SiPM bias voltage (now provided through the front-end due to the differential signaling requirement) from the signal. As the SiPM pulses are fast, they are almost unaffected. The final value, checked with simulations as can be seen later, was set to 100 nF.

And finally R_{27}, fixed at a high value, provides the current limit to the bias line while does not affect the signal; because provides a very high impedance path for the signal current compared to the first stage input. Assuming a maximum bias voltage of 80 V (worst case for a *Hamamamtsu* SiPM), a resistor of 33 $k\Omega$ will limit the current in case of short circuit at 2.4 mA; far enough from the 5 mA limit of the bias power supply.

A zener diode (D_1) protects the ADC form overvoltages, as the operational amplifiers are fed at ± 5 V and the maximum rating for the ADC input is 3.3 V. More information about the zener performance can be found on next chapter, section 4.5.

As the DAC offset adjustment is placed at the second stage input, and that stage stays identical, the performance and calculations of the remaining circuit are the

same than the single ended scheme explained in the previous section. For the details see the page 80.

As shown on figure 3.10, the performance of the differential circuit is almost identical to the single ended scheme.

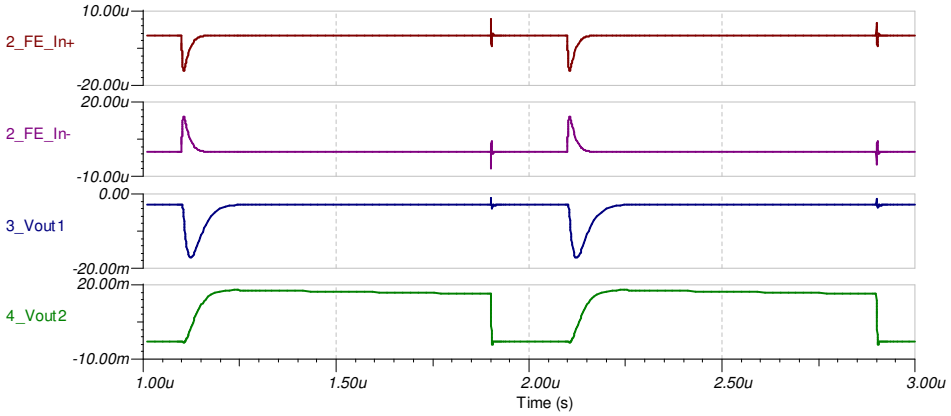


Figure 3.10: *Simulation of the differential front-end electronics analog conditioning.*

The first two plots are the inputs of the new circuit, which correspond to the SiPM anode and cathode. As foreseen, both have identical shape but opposite polarity. Third plot corresponds to first stage output, which amplifies and slightly shapes the pulse. And finally, the last plot shows the integrated signal previous to the ADC, which again is identical to the single ended scheme; although it needed a slightly offset adjustment.

With the differential input we had, theoretically, improved the endurance of the signal chain against coupled noise without affecting the performance and the main electronic design; so we kept the power consumption and the cost previously calculated. But the real test was when the electronics were tested with the full setup, including all the internal and external cables that the NEW detector has (chapter 6).

3.4 Noise Analysis

An important issue that must be also analyzed is the noise due to the circuit itself, which may be not negligible for some configurations. As we have already checked the circuit performance, this analysis does not intend to predict the output noise, but give knowledge about the elements that cause the noise we have already seen. There are known many noise sources, but for our case we decided to check just the ones we considered more relevant: the OPAs, and the resistors thermal noise. As the switching integrator reduces a lot the system bandwidth, high frequency noise like the flicker noise has less repercussion on the output. Also the shot noise become irrelevant compared with the previous ones, as it is proportional to the DC current on the circuit which, in our case, is negligible.

For this analysis the final values of the components are needed, so it was performed once the design process was completed to check the viability of the circuit. On figure 3.11 the final components values are shown.

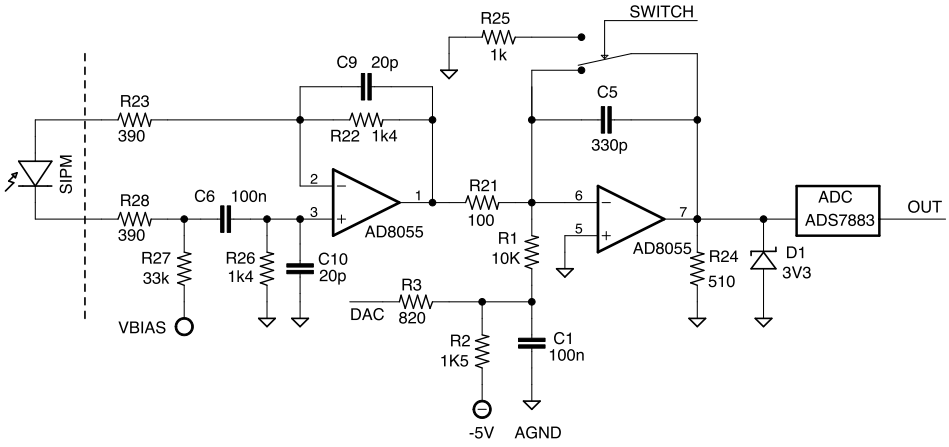


Figure 3.11: *Differential SiPM front-end channel with final components' values.*

The output noise is the result of all the noise contribution from each component in the circuit. Each noise contribution in the output can be related to an equivalent input current, as we are working with current signals:

$$\overline{v_{out}{}^2} = \Bbbk \cdot \overline{i_{in}{}^2} \tag{3.7}$$

where $\Bbbk$ is a constant that includes also the effect of the system bandwidth. This method simplifies the calculation of each noise contribution, as avoids to deal with the integrator effect for each component because its effect is also included in the constant factor.

In order to calculate this factor we need to know the transfer function of the analog chain, so we can predict the output for each noise input. The transfer function in the time domain of the analog chain can be obtained as the convolution of each stage:

$$H(s) = H_1(s) \cdot H_2(s) \tag{3.8}$$

To solve this equation we need to move it from the time domain to the frequency domain, which can be done using the Parseval theorem:

$$\int_{-t}^{t} |H(t)|^2 dt \simeq \int_{0}^{BW} |H(j\omega)|^2 d\omega \tag{3.9}$$

So in the s domain, the gain of the two analog stages can be described as[2]:

[2]For the first stage transfer function only one branch of the circuit has been considered. Remember that we are looking for a tool that simplifies the noise contribution estimation, virtually placing the noise at the input. So we can not assume that noise as fully differential neither common mode. Assuming half the noise on each input branch, the result will be the same than having all the noise on the upper branch, as considered.

$$H_1(s) = -R_{22} \tag{3.10}$$

$$H_2(s) = \frac{1}{R_{21}C_5} \tag{3.11}$$

Which leads us to the constant value that relates the output noise as a function of the input current:

$$\mathbb{k} = \int_0^{BW} |H(j\omega)|^2 d\omega = {A_T}^2 \cdot T_s = \left(-R_{22} \, \frac{1}{R_{21} \, C_5} \right)^2 \cdot T_s = 1.8 \cdot 10^{15} \tag{3.12}$$

where T_s is the integration time, 1 μs in our case.

Once the procedure has been defined, as explained, each noise contribution is obtained as an input current, thereby the effect in the output can be easily calculated. For the operational amplifiers the manufacturer specifies a noise density of $\overline{v_o} = 6 \, \frac{nV}{\sqrt{Hz}}$, which produces an input current of:

$$\overline{{i_{in_{OPA1}}}^2} = \frac{\overline{{v_{o_{OPA1}}}^2}}{{R_{23}}^2} \tag{3.13}$$

$$\overline{{i_{in_{OPA2}}}^2} = \overline{{v_{o_{OPA2}}}^2} \left[\frac{R_{21}}{(R_1 + (R_2 \parallel R_3)) \, R_{22}} \right]^2 \tag{3.14}$$

And for the resistors, their contribution is:

$$\overline{{i_{in_{R_1}}}^2} = \overline{{v_{o_{R_1}}}^2} \left[\frac{R_{21}}{(R_1 + (R_2 \parallel R_3)) \, R_{22}} \right]^2 \tag{3.15}$$

$$\overline{{i_{in_{R_2}}}^2} = \overline{{v_{o_{R_2}}}^2} \left[\frac{R_{21}}{(R_2 + (R_1 \parallel R_3)) \, R_{22}} \right]^2 \tag{3.16}$$

$$\overline{i_{in_{R_3}}{}^2} = \overline{v_{o_{R_3}}{}^2} \left[\frac{R_{21}}{(R_3 + (R_1 \parallel R_2))\, R_{22}} \right]^2 \tag{3.17}$$

$$\overline{i_{in_{R_{21}}}{}^2} = \frac{\overline{v_{o_{R_{21}}}{}^2}}{R_{22}{}^2} \qquad \overline{i_{in_{R_{22}}}{}^2} = \frac{\overline{v_{o_{R_{22}}}{}^2}}{R_{22}{}^2} \tag{3.18}$$

$$\overline{i_{in_{R_{23}}}{}^2} = \frac{\overline{v_{o_{R_{23}}}{}^2}}{R_{23}{}^2} \qquad \overline{v_{o_{R_{24}}}{}^2} = \overline{v_{R_{24}}{}^2} \tag{3.19}$$

$$\overline{i_{in_{R_{26}}}{}^2} = \frac{\overline{v_{o_{R_{26}}}{}^2}}{R_{23}{}^2} \qquad \overline{i_{in_{R_{27}}}{}^2} = \frac{\overline{v_{o_{R_{27}}}{}^2}}{R_{23}{}^2} \tag{3.20}$$

$$\overline{i_{in_{R_{28}}}{}^2} = \frac{\overline{v_{o_{R_{28}}}{}^2}}{R_{23}{}^2} \tag{3.21}$$

Where each resistor noise density corresponds to the thermal or Johnson-Nyquist noise, is given by:

$$\overline{v_{o_R}{}^2} = 4k_B TR \tag{3.22}$$

Note that for the resistor R_{24} the contribution is directly the output, due to its position.

This way, each noise contribution is obtained as an input current which can be translated to an RMS output voltage noise:

$$V_{oRMS} = \sqrt{\int_0^{BW} |v_o|^2 df} = \sqrt{|v_o|^2} \tag{3.23}$$

Finally the main noise contributions can be found on the table 3.1.

	$\overline{i_{in}{}^2}\ \left(\frac{A^2}{Hz}\right)$	$\overline{v_{out}{}^2}\ \left(\frac{V^2}{Hz}\right)$	$V_{oRMS}\ (V)$
OPA 1	$2.37 \cdot 10^{-22}$	$4.26 \cdot 10^{-7}$	$6.53 \cdot 10^{-4}$
OPA 2	$1.66 \cdot 10^{-27}$	$2.98 \cdot 10^{-12}$	$1.73 \cdot 10^{-6}$
R_1	$7.95 \cdot 10^{-27}$	$1.43 \cdot 10^{-11}$	$3.78 \cdot 10^{-6}$
R_2	$2.59 \cdot 10^{-26}$	$4.66 \cdot 10^{-11}$	$6.83 \cdot 10^{-6}$
R_3	$1.60 \cdot 10^{-26}$	$2.88 \cdot 10^{-11}$	$5.37 \cdot 10^{-6}$
R_{21}	$8.82 \cdot 10^{-25}$	$1.59 \cdot 10^{-9}$	$3.98 \cdot 10^{-5}$
R_{22}	$1.23 \cdot 10^{-23}$	$2.22 \cdot 10^{-8}$	$1.49 \cdot 10^{-4}$
R_{23}	$4.43 \cdot 10^{-23}$	$7.97 \cdot 10^{-8}$	$2.82 \cdot 10^{-4}$
R_{24}			$8.81 \cdot 10^{-18}$
R_{26}	$1.59 \cdot 10^{-22}$	$2.86 \cdot 10^{-7}$	$5.35 \cdot 10^{-4}$
R_{27}	$3.75 \cdot 10^{-21}$	$6.75 \cdot 10^{-6}$	$2.60 \cdot 10^{-3}$
R_{28}	$4.43 \cdot 10^{-23}$	$7.97 \cdot 10^{-8}$	$2.82 \cdot 10^{-4}$

Table 3.1: *OPA and resistors thermal noise contribution.*

Note that the biggest noise contribution is given by the resistor R_{27}, which is the one that limits the SiPM bias current. Due to its placement the resistor noise is filtered by the RC configuration in the input, composed by R_{27} and C_{10}, which results in a $\sim 250\ kHz$ corner frequency. So, as this frequency is a quarter of the gated integrator, the noise contribution can be scaled down by a factor 4 to have a more realistic approach. This means that, on the output, the noise is close to 1.3 mV_{RMS}.

Still that resistor is, theoretically, the major contributor for the output noise. Taking into account that the single photon has, by design, an amplitude between $10 \sim 15\ mV$, the noise level seems reasonable. And compared with the system resolution this noise is less than 2 LSBs ($\sim 800\ \mu V$ per LSB).

The remaining elements introduce almost negligible noise in the system and, as will be shown on further chapters, the main noise source became from the

radiated one; not surprisingly as we have several meters of cable from the SiPMs to the front-ends.

"Para un condensador su misión en la vida es cascar."

– J.F. Toledo Alarcón

4

Front-end Electronics: The FEB64

Once the prototype was validated, the challenge was to export this electronic design to a professional board which contains 64 readout channels and a FPGA, with all the required circuits for the supply and communication.

The goal to achieve is a 3U size board capable of conditioning and reading the 64 SiPMs of a whole DICE-Board, which has enough low noise to properly obtain the single photon spectrum for the tracking plane calibration. The resulting board is what we called the FEB64 (Front-End Board 64-channels) [Rodríguez et al. 2015].

4.1 Power Supply Requirements

Even though the board size is very compact, it contains a powerful FPGA and 64 analog conditioning channels with individual ADCs. So the power design must be done carefully, not just for consumption but also for noise coupling between the digital and analog supplies. The board input voltages are separated for digital and analog components, and have been reduced in number for simplicity. Thereby the only power inputs are $+6\ V$ for digital devices (with its own digital ground) and $\pm 6\ V$ for the analog stages, each one with a dedicated analog ground connection.

For the analog stages the supply has been split in two halves, due to the power consumption. So the channels are powered in groups of 32 using low-noise high-PSRR linear voltage regulators, which provides the $\pm 5\ V$ required for the operational amplifiers; and also for the DACs and the offset adjustment branch. These voltage regulators are enabled or disabled by the FPGA, so the analog stages are only connected while the data acquisition is running, and allows us to save power consumption.

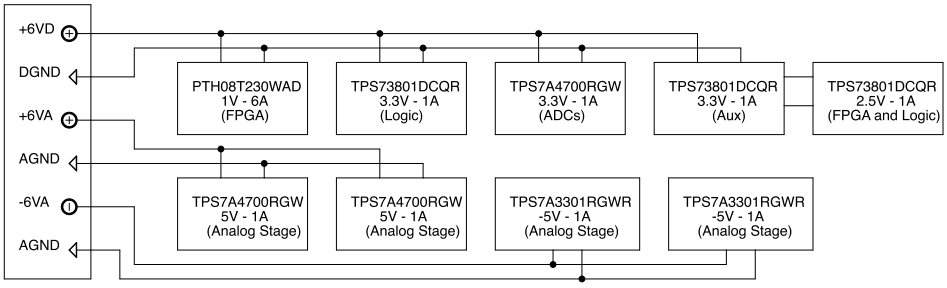


Figure 4.1: *Scheme of the voltage regulators used in the FEB64.*

Then, to supply the digital devices the dedicated 6 V line is used. The FPGA selected is the *Virtex-6 XC6VLX130T* from *Xilinx*, which main supply is 1 V with an estimated consumption of $3 \sim 4\ A$. For that purpose we chose a 6 A rated DC/DC converter module, the *PTH08T230WAD*. Other voltages are required for some devices like the ADCs, DACs, flash memory, and auxiliary parts like the

jitter cleaner, the LVDS level converter; so a total of three 3.3 V and one 2.5 V regulators are used. One of the 3.3 V voltage regulator has been selected also for low noise and high PSRR, to be used for the ADC and the switch on every integrator branch. Even if these are digital devices they are connected to the analog stage, so they should be managed carefully in order to avoid noise on the treated signal.

For the correct power up of the FPGA and the other devices we use a power supply sequencer, the *LM3881* from *Texas Instruments* which controls the power-up and power-down via the enable inputs of the voltage regulators. This integrated circuit has been configured to power-up when the input voltage has reached at least 4.5 V, and to enable the regulators sequentially every 30 ms. Same way, the power-down sequence is activated if the input voltage decrease under 4.5 V; thereby there are not dangerous voltage transients on the FPGA.

The last supply requirement is the one for the SiPMs themselves, as the bias voltage is given through the same signal cables via the front-end. A discussion was opened here, because an on-board SiPM power supply will simplify the installation on the detector; but at the same time will complicate the FEB64. Finally the SiPM power supply was not included on the FEB64, as it will need processing hardware dedicated for the gain stabilization and the FPGA will be fully dedicated to the SiPM signal acquisition. Thereby the front-end acts as a bias voltage bypass and is fully decoupled from the SiPM power supply.

4.2 From Prototyping to Full Design

The final board design was a great challenge, as the channel density has been increased in a factor 4, while the size is half the previous front-end board (FEB) for NEXT-DEMO. The prototype validated the analog stage and allowed us to take data using the expansion port of the old FEB, but the whole design include a huge number of devices that makes the board intelligent and powerful.

As mentioned before each one of the 64 analog channels has its own ADC, 12-bit at 1 MHz sampling frequency; so the FPGA has to be capable of reading and processing such flow of data, manage the data buffer, synchronize with the front-

end concentrator boards (FEC) and send the packaged data. For that reason we chose the *Virtex-6* family, as its specifications are powerful enough for our needs.

For the FPGA correct performance some extra circuitry is needed. Two 128 *Mb* flash memories are used to store the FPGA program, one for normal operation and one for the safe boot. The FPGA is programmed by a JTAG port as usual, but our design allows also remote programming via ethernet, which makes it a lot easier to work in an underground laboratory with access restrictions.

To communicate with the DAQ and send the acquired data two different options were included; RJ-45 for the old FEC version compatibility, and HDMI as the new DAQ version has moved to this connector interface. Also, in order to improve the communication and reduce the data errors, a jitter cleaner was added to the data transmission lines.

About the analog stages some changes or additions were also made. In the FEB64 each DAC controls the offset of 8 channels, as that is the outputs number it has; which reduces the number of devices to be controlled.

Then some safety elements were added, to prevent damage to electronics in case of overvoltages. This is very important as we are dealing with the SiPM bias voltage (up to 80 V for some models) and with the field cage high voltage (a few kV). To limit the bias voltage current we added a limiting resistor, as was explained, but this resistor has to be able to hold the power dissipation in case of bias short circuit; so we chose an overrated value for the resistor power. Also a diode was included in the SiPM anode wire, which corresponds with the positive signal, as a short in the SiPM will produce the bias voltage to reach the OPA input. Thereby any voltage over 0.7 V will be clamped. In addition an ESD diode was added at each differential input, to prevent damage not only due to ESD, but also due to sparks from the field cage to the tracking plane.

As all the elements on the DICE-Board are directly connected to the FEB64, some actions must be done. The bias voltage, as was explained, is provided by an external power supply described on chapter 7; so both bias voltage and NTC sensor must be connected to it in order to perform the gain stabilization. For that purpose we use a 4-pin LEMO connector, which simplifies the job in

a very reduced space while matches the shielding and voltage requirements. And also the LEDs on the DICE-Board should be driven. This time, as the firmware required for this task is very simple, we decided to drive them directly via the FPGA through NMOS transistors. This way the calibration LEDs can be illuminated with different pulse widths, and can be internally synchronized with the data acquisition, which makes easier the procedure.

The last detail we added was a connector for five LEDs which will be placed on the front panel. These LEDs are directly driven by the FPGA, so they can be programmed for any function we need. Nowadays we are using three of them in order to indicate the FPGA firmware load, the synchronization with the FEC and the enabled status of the analog section.

4.3 Board Layout Distribution: a Matter of Size

In order to fit all the required electronics in a 3U board, as it seemed to be the most adequate size for a compact design, the components distribution has to be done very carefully. As can be seen on figure 4.2 the board is divided into four different areas: digital, analog, digital power and analog power.

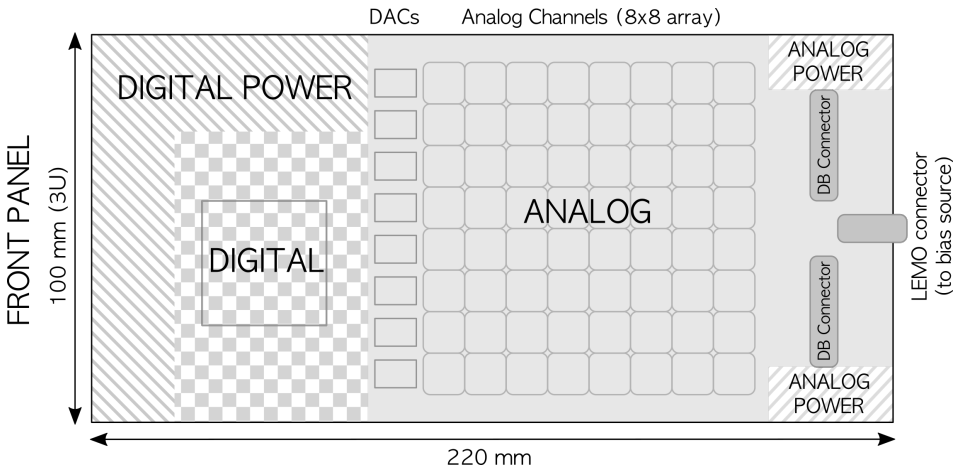


Figure 4.2: *Components distribution on FEB64.*

By separating digital and analog elements and grounds, the noise coupled to the analog signals due to digital devices is reduced. Only the ADC and the switch located in the analog stage are the devices that carefully join both analog and digital sections. This is a very important matter, specially relating the switched voltage regulators. For this reason the board has been distributed as a logical path, where the analog signals coming from the SiPMs enter the board through the opposite side of the digital devices (right side on the figure 4.2); then after the conditioning, signals are digitized and sent to the left side where the FPGA reads them.

Regarding board size, the 64 discrete analog channels were reduced to a 11×11 *mm* cell each, in order to fit them all just taking half of the total board surface.

To accomplish both size and proper distribution requirements, the printed circuit board had to be designed in a 12 copper layer configuration to allow the high density of channels and signals, as shown on figure 4.3.

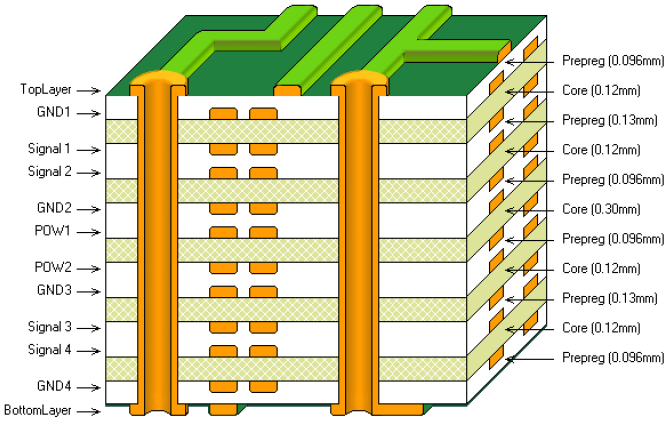


Figure 4.3: *Layer stackup distribution on the FEB64v2.*

The use of each one of the copper layers is the following one:

- **Top and bottom:** Placement of components and small routing between close devices.

- **GND1, GND2, GND3 and GND4:** Separate distribution for digital and analog ground. The "comb" shape allows the ADC and switch have a proper digital ground connection, while the operational amplifiers are close to the analog one.
- **Signal 1, Signal 2, Signal 3 and Signal 4:** Right where the analog ground plane is placed in the adjacent layer, the signals coming from the SiPMs are routed. In the other hand, the digital traces are routed in the areas where the digital ground plane is.
- **POW1**: Used to distribute some power lines. The "comb" shape is used to supply the 3.3 V to the ADC and switch, and the $+5$ V to the OPAs.
- **POW2**: Used also to distribute some power lines. This time the "comb" shape corresponds to the -5 V line for the analog stages.

4.4 A Functional Design: FEB64v2

Once the design was completed, a small batch was produced for testing. The boards were connected to a small setup with a DICE-Board and a controlled LED in a black box, and several tests were performed for noise, data transmission errors, single photon resolution capability and long term stability. This allowed us to test the full tracking plane chain for the first time, and we found some small issues to correct before the final production, so we did a design revision for minor changes.

This revision included the change and addition of some filtering capacitors for the supply, enable the data transmission via the HDMI connector instead the RJ-45 (as explained on section 4.7 we moved the DAQ from the old FECs to the ATCA-SRS system), small mechanical changes, and improve the routing and filtering of the DC/DC converter that supplies the FPGA as it was coupling switching noise to some analog channels.

Later, the full batch of electronic boards was produced, known as FEB64v2 (figure 4.4).

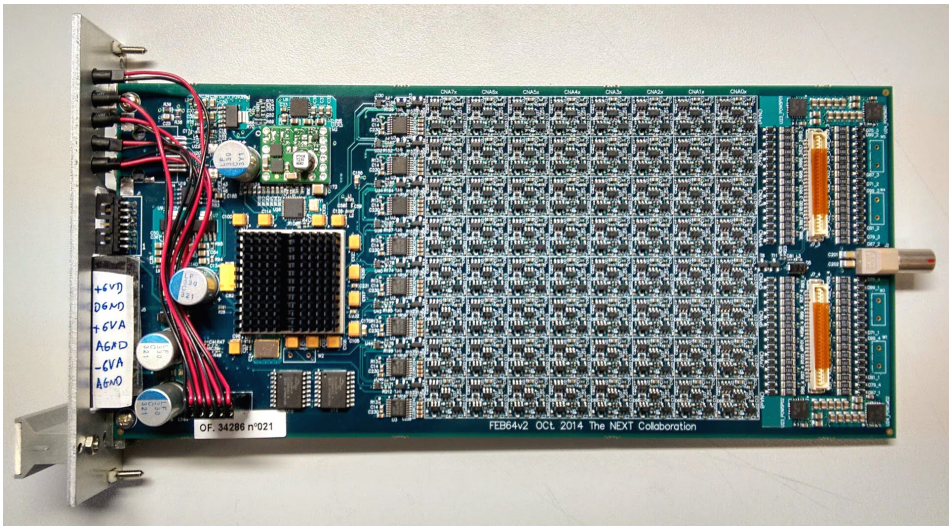


Figure 4.4: *First FEB64v2 fully assembled and functional.*

On figure 4.5 a full rack of front ends is shown. It has 12 front-ends and one SiPM bias supply (detailed on chapter 7). The front side, as can be seen, accommodates the connections for the HDMI data transmission, the JTAG for the FPGA programming and the power supply lines.

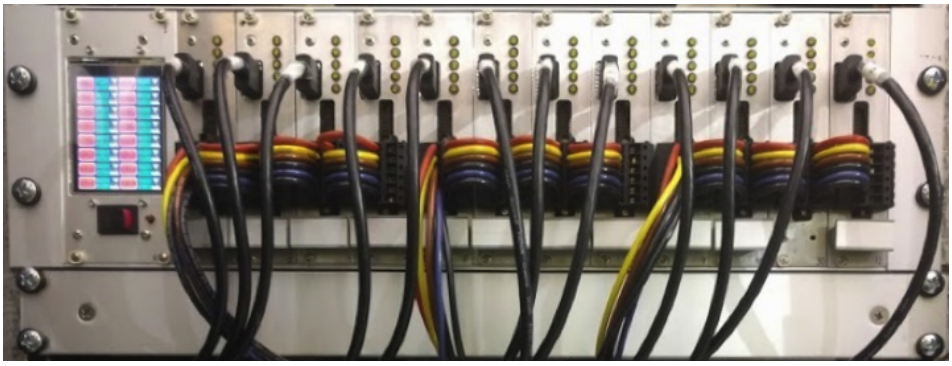


Figure 4.5: *19" 3U crate with one power supply providing the required bias to 12 front-ends, a total of 768 SiPMs. A 1U fan tray is placed below the crate for the required electronics cooling.*

Due to the power consumption, the boards are supplied in groups of four units, in a daisy-chain connection. The cables coming from the tracking plane connect to the rear side of the boards, as well as the SiPM bias supply.

A total of 34 boards were assembled. Two of them were damaged from production or assembly, and another two were used for tests and the setup at the lab. The remaining 30 boards were sent to the LSC (*Laboratorio Subterráneo de Canfranc*), and 28 were installed on the NEW detector and have been successfully working for several months... until a small issue was found...

4.5 The zener issue

The NEW tracking plane was fully installed on November 2015, and allowed the proper calibration of the ∼1800 silicon photomultipliers using both dark counts and pulsed LEDs.

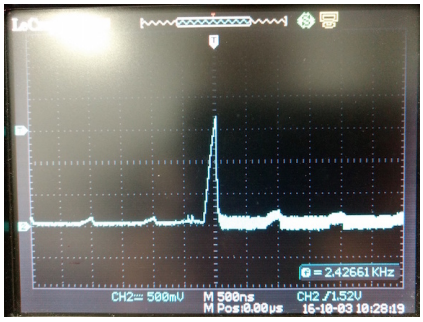
On September 2016 the field cage and the high voltage feedthroughs were installed, the NEW detector was finally ready for operation, and every subsystem was connected at LSC. When the first light events were detected inside the vessel, some of the tracking plane front-ends increased their current consumption far beyond the nominal value. And also the waveforms produced were visibly affected.

At that point the acquisition with the tracking plane was stopped until the problem was identified and corrected.

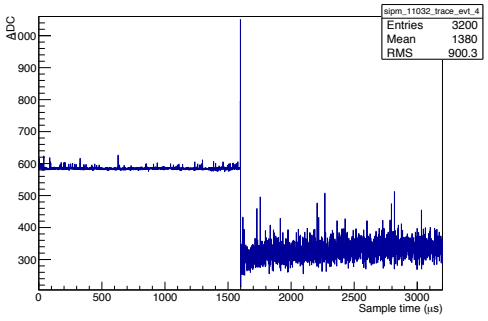
4.5.1 Malfunction detection

A small setup was assembled at IFIC, and the malfunction was successfully replicated using a pulsed LED. As seen at LSC, after a big light event the front-end consumption increases a lot, and as shown on figure 4.6a the output signal has an oscillation that was not there before.

After some tests with the scope and simulation, we decided to look for the overcurrent using a thermal camera. Figure 4.7 shows a picture taken just after



(a) *Scope waveform during a malfunction transition. As can be seen, after the big light pulse the waveform has some oscillation.*



(b) *Acquisition data from NEW where the malfunction is detected.*

Figure 4.6: *Comparison between scope and acquisition for a failure-causing event.*

a light pulse, where the channels that started to oscillate are perfectly identified as hot spots on the front-end.

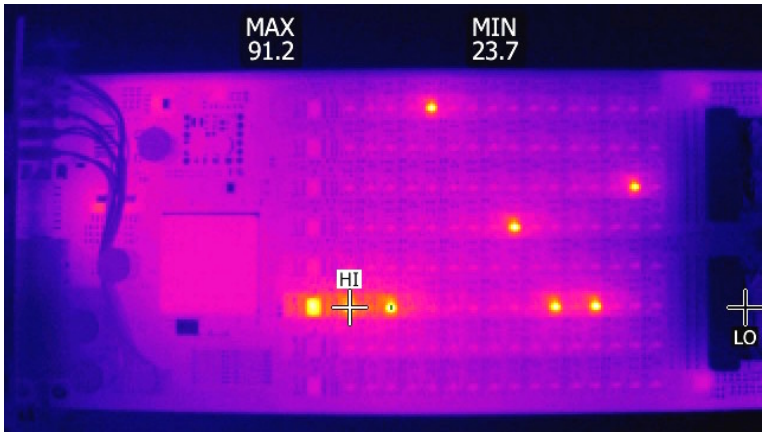
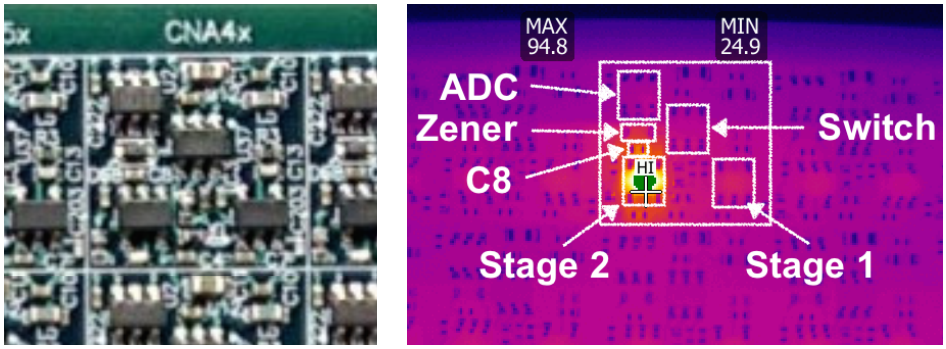


Figure 4.7: *FEB64 view with the thermal camera. The channels not working properly appear as very high temperature dots.*

Taking a closer look to one of that hot spots we could identify that the operational amplifier on the second stage, the one with the gated integrator, was extremely hot (figure 4.8).



(a) *One analog channel cell.* **(b)** *Thermal view of the analog cell.*

Figure 4.8: *Detail of the analog channel cell, where the malfunction was detected using a thermal camera.*

Once the issue was located some tests were done focusing on the second stage amplifier. Finally we found that the zener diode was the guilty device, as its parasitic capacitance makes the amplifier output unstable after a threshold voltage is reached.

4.5.2 Solution

After the problem was detected, two different solutions were implemented.

First, a new FPGA firmware version was developed and extensively tested in the front-ends. This firmware included a malfunction detection algorithm, based on the baseline deviation, and is able to detect a malfunction and shutdown the analog power in a few milliseconds.This stops the oscillation. Then the FPGA powers up again the analog front-end area and keeps working.

On the other hand a hardware solution has been found, as we identified the zener diode as the problem source. Once the zener is removed, the front-end works as expected, without any issue even for huge events that saturate the ADC for several milliseconds.

That diode was placed between the second stage integrator and the ADC input to limit the signal amplitude to 3.3 V (see circuit on figure 3.9, page 88), but fortunately it is a redundant protection. The *AD8055* operational amplifier has an output limit of ± 3.1 V when powered at ± 5 V, and the *ADS7883* ADC has internal protection diodes.

So, carefully removing the zener diodes (by hand) solved the problem, and the NEW detector was able to start taking data with the largest fully functional tracking plane ever built.

4.6 Planned design modifications: Future FEB64v3

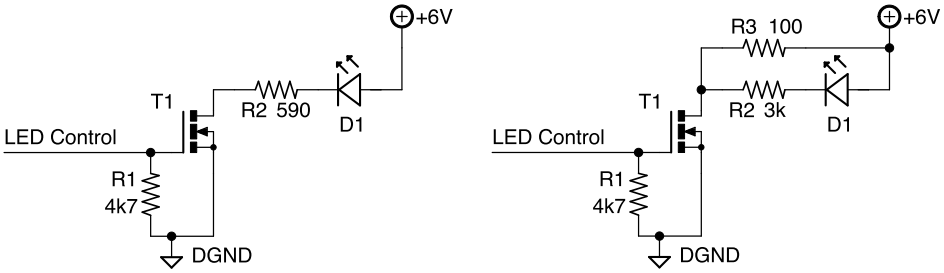
As all designs, the FEB64v2 has room for improvement. During the months that the system has been working we have learn a lot about the performance of the electronics, and some possible improvements showed up. This is a list of the planned modifications that will be included on the FEB64v3 design, once we have fully tested the FEB64v2 for every possible signal and condition.

Zener removal

As detailed on section 4.5, the protection zener diode placed at the ADC input caused a huge malfunction triggered by large events. All the zener diodes were removed from all the FEB64v2 manufactured in order to have a fully working tracking plane in the NEW detector. Of course, these diodes will not be included in the new design.

LED Driving circuit

As mentioned before, each DICE-Board has room for four LEDs meant to perform geometrical calibration of the energy plane. Due to the high sensitivity of the photodetectors used, the driving pulses for the LED should be extremely small, just for the LED to emit a few photons. This LEDs are pulsed via the front-end, controlling the parameters using the *Java* application. With this purpose in mind, the driving circuit was designed as shown in figure 4.9a.



(a) *LED driving original circuit.* **(b)** *Modified circuit for smaller and sharper pulses.*

Figure 4.9: *Detail of the LED driving circuit modification to improve the performance on SPE calibration.*

Even for the smallest possible pulse that the FPGA could generate, the amount of light emitted was excessive. Several tests and simulations later, we realized that the reflecting walls of the light tube made the PMTs collect too many photons. For this reason, we had to modify the LED driving circuit as shown on figure 4.9b. The current limiting resistor (R_2) was increased to reduce the amount of light emitted, and also a pull-up resistor (R_3) was added to sharpen the pulses. This modification has been made just in two front-end boards, as it is not an easy intervention, and the calibration in this phase of the experiment does not need all the LED to be operating.

Routing improvement

Some small modifications on the signal traces routing may be done, to improve the signal integrity and reduce the noise. For instance, the HDMI traces routing may be modified to reduce data errors during transmission.

Improved spark protection

Even though several protections were placed to prevent circuit damage in case of sparks, some malfunctions have been detected. The study of the "after-spark" effects is still undergoing, but we already know that sometimes the data acquisition stops, and the SiPM bias sources lose their internal DAC calibration.

Once we collect enough information about these effects, we will introduce the required protection on the new FEB64v3 design.

4.7 SRS-ATCA & Java Interface

NEXT (via the UPV team) has co-developed together with IFINHH (Bucharest) and CERN a new readout and DAQ concept named SRS [Muller 2011] for the international RD51 Collaboration at CERN. NEXT front-end modules are connected via copper links to the SRS DAQ interface modules. ALICE's DATE environment is used as DAQ software [ALICE Collaboration 2010]. This brings a number of advantages, like counting on a large base of users and developers, reducing production costs and profiting from other groups' developments. SRS has been successfully used in NEXT-DEMO (PMT and SiPM readout, DAQ interface and trigger modules) [Toledo et al. 2011].

The Scalable Readout System (SRS) was defined by the CERN RD51 Collaboration as a multi-channel, scalable readout platform for a wide range of front ends. In 2014, SRS was ported to the ATCA (Advanced Telecommunications Computing Architecture) standard. After the evaluation of the SRS ATCA from the noise point of view in NEXT-DEMO, a final decision was taken in February 2015 leading to the use of SRS ATCA in NEW.

This is, to our knowledge, the first experiment operating entirely on SRS-ATCA [Esteve, Toledo, Rodríguez, et al. 2016].

4.7.1 ATCA

In 2014, SRS was ported to the ATCA (Advanced Telecommunications Computing Architecture) standard upon agreement with the German company *EicSys*. The use of certified crates with built-in and redundant cooling, power and shelf management makes it a more robust mechanical and electrical solution for prolonged operation in experiments than the original SRS flavour based on light Eurocard crates. Higher data bandwidth is achieved by replacing the DTCC

link cables with multi-gigabit channels across a full-mesh backplane, enabling 10 Gb/s I/O through the RTM and using faster FPGA and memory.

The ATCA-FEC carrier has two *Xilinx Virtex-6* FPGAs and a DDR3 SO-DIMM memory module for each FPGA. The two FPGAs are interconnected via high-speed links. A third FPGA, a *Spartan-6*, is used for board management purposes. Two on-board custom mezzanine connectors provide I/O flexibility for a wide range of front ends. Two mezzanine models exist with 24 ADC channels (12 bit, up to 60 MSa/s) and 12 DTCC links on HDMI connectors to interface digital front ends. In-design mezzanines include multi-gigabit optical transceivers with FPGAs. The ATCA-FEC is functionally equivalent to 2 "classic" FEC modules. SRS-ATCA includes rear transition modules (RTM) for multiple GbE, 10 GbE and other I/O connectivity. ATCA backplanes exist with full mesh and star topologies, using 10 Gb/s channels. This backplanes are currently not being used by NEXT, but are available for further upgrades.

4.7.2 DAQ Architecture

Reading out the 28 SiPM front-end boards in the tracking plane partition requires one and a half ATCA-FECs and a total of three digital interface mezzanines (each one having 12 DTCC interfaces over HDMI). Front-end boards work in free-running mode, storing data continuously in a circular buffer. Data is only sent to the ATCA-FEC modules when a timestamped trigger is received.

The energy plane (12 PMTs) is read out with a single 24-channel ADC mezzanine plugged onto half ATCA-FEC module, which sends trigger candidates based on early energy estimations to another half ATCA-FEC (used as trigger module). As a result, three ATCA-FECs are needed to read out the detector's energy and tracking planes and implement the trigger algorithm. Each ATCA-FEC interfaces a DAQ PC via 4 Gigabit Ethernet optical links, as can be seen on figure 4.10.

ALICE's DATE environment is used as DAQ software. The DAQ PC farm comprises three Local Data Concentrator PCs (LDC), each one connected to an ATCA- FEC via 4 Gigabit Ethernet optical links; two Global Data Concentrator

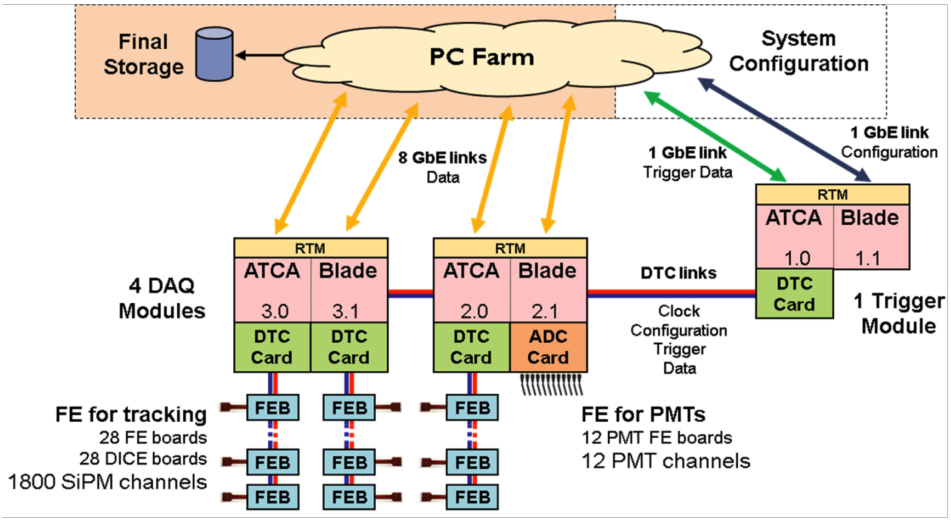


Figure 4.10: *NEW DAQ and trigger system architecture.*

PCs (GDC), for event building; and a storage PC (equipping a number of hard disks). A Gigabit Ethernet switch interconnects these six PCs.

The array of 1792 SiPMs in the tracking plane uses 28 front-end boards that integrate and digitize (12 bit, 1 MSa/s) 64 channels each. For 28 front-end boards, 1 ms events and a 10 Hz trigger rate, the SiPM tracking partition generates 35 $MByte/s$ in raw data mode. For the energy plane, the array of 12 PMTs uses ADC cards to digitize the signal at 40 MSa/s, 12 bit. Once digitized and framed, this produces approximately 10 $MByte/s$ at a 10 Hz rate.

The complete system described has been already successfully installed and validated in laboratory at LSC, as shown previously on figure 1.24.

4.7.3 DAQ Features

Dead time must be minimized, suggesting the use of double buffers. These are implemented in the SiPM front-end boards for the tracking plane partition, and in the ATCA-FEC's DDR3 memory in the case of the energy plane partition. Events are configurable in length up to 3.2 *ms*, with a nominal value of 1.2 *ms* which corresponds to double the length of the NEW drift region. NEW is expected to operate at a 10 *Hz* trigger rate produced by background events.

Three different DAQ modes are supported, depending of the data analysis wanted:

- **Test mode:** The system works in raw data mode. The double buffer scheme (explained on section 1.4) is used for every type of event. The trigger is limited to a maximum frequency of 10 *Hz*.
- **Normal Mode 1**: The system works in zero-suppressed data mode for "normal" events, and raw data mode for "interesting" events. The double buffer is used for all events. The use of a trigger frequency limitation is possible.
- **Normal Mode 2:** Very similar to *Normal Mode 1*, but the double buffer is only used for "interesting" events.

Zero suppression is configurable for both PMTs and SiPMs via the *Java* application, which parameters define the threshold level, pre and post-samples and filt-samples. This method saves a lot of unnecessary data and processing time.

The trigger algorithm [Esteve, Toledo, Monrabal, et al. 2012] must combine information from the first scintillation light as well as from the early total event energy estimation. A trigger is generated if (1) a defined number of PMTs have detected at least a certain number of scintillation photons within a defined time window, and (2) some time after the scintillation, the estimated total integrated energy in a defined time window is within certain upper and lower bounds. The trigger algorithm is implemented on FPGA to achieve the minimum response time.

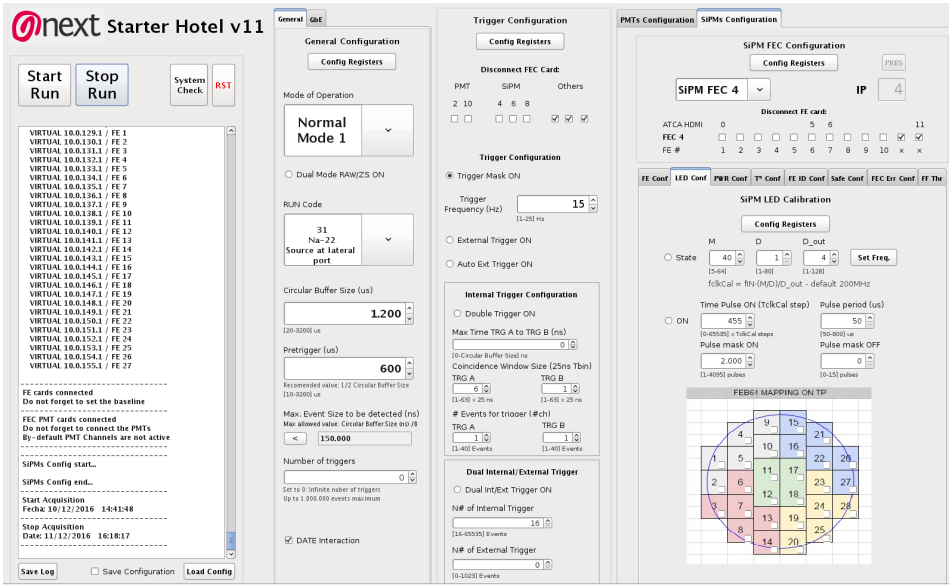


Figure 4.11: *DAQ configuration application based on Java.*

All thresholds and levels are configurable via the *Java* application, shown on figure 4.11; likewise all the parameters that define the data acquisition, cards synchronization and data sending. Other features which are also controlled via the *Java* interface are:

- Run the system for a fix number of events.
- Selectable Run Code.
- Different trigger types configuration (internal: simple and double, external, auto-trigger).
- Zero Suppression configuration for both PMTs and SiPMs.
- For PMT channels:
  - Baseline restoration.
  - Trigger candidates configuration.
- For SiPM:
  - Auto baseline adjustment.
  - LED control.

"Caminando en línea recta no puede uno llegar muy lejos..."

"Droit devant soi on ne peut pas aller bien loin..."

– El Principito / Le Petit Prince

5

New SiPM array: The Kapton DICE-Board

Due to the drawbacks of the *CuFlon*® DICE-Boards, we needed an alternative with better radiopurity and robustness, and also simplify the cabling for NEW.

As new substrate for SiPM arrays, we have chosen *Kapton*®, which is a polyimide laminate with very good characteristics like flexibility, low radioactivity, stable dielectric constant and high dielectric strength. It also allows us to move the connector, which is not radiopure enough, from the back side of the board and extend the board as a cable, what we have called pigtail, with the connector at the end. This way we can place the capacitors (if needed) on the end of the pigtail close to the connector, which will be placed behind the inner copper shielding, as is shown on figure 5.1.

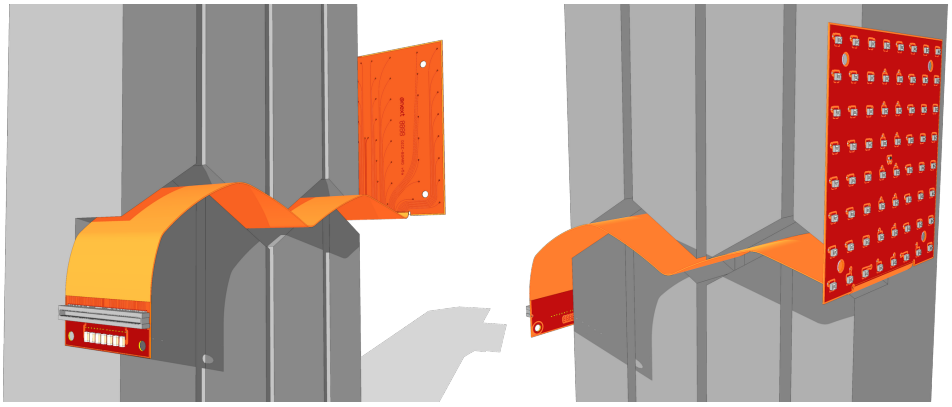


Figure 5.1: *DICE-Board with the pigtail through the inner copper shielding (represented in grey).*

In the first conceptual design, the one shown on figure 5.1, the copper shielding was made by four copper plates with diagonal flat holes to pass the pigtails. Some iterations later, done in parallel with the DICE-Boards and electronics design, the copper shielding became a combination of a 12 *cm* thick copper plate and a thin copper structure to hold the DICE-Boards; which will be detailed later.

Another important research before starting the design was finding a proper connector for the DICE-Boards and, consequently, for the inner cables. Each board will contain 64 SiPMs, and at least one temperature sensor and one LED. And the connector had to be small and flat, to reduce the hole needed to pass them through the copper shielding. Therefore, looking at the available options in the market, we decide to narrow the options and fix some parameters: use a board-to-board connector, to achieve a flat and robust connection; 2 row, 140 to 160 pin, 0.5 *mm* pitch connectors; which is a standard, fits the expected size, will allow that each SiPM has its own current return and still leaves free extra lines.

In order to reduce the radioactivity background on the detector, we have tried to minimize the adhesive mass used on the board manufacturing. For this reason the chosen option was a two-layer adhesiveless base substrate, with polyimide coverlay on both sides, which only requires a little amount of adhesive.

The adhesiveless base can be selected in different thicknesses, but as we want to reduce the crosstalk as much as possible, and also minimize the noise coupling, we have chosen the thinnest option, which is 1 *mil* (25.4 μm). For the coverlay, which is the external polyimide cover layer, we want also a thin layer, because the pigtail should be flexible enough to pass through the copper shielding; but it should be also thick enough to avoid signal coupling between parallel cables. Finally we compromised a solution with 5 *mil* (127 μm) coverlay (as can be seen on figures 5.3 and 5.11).

5.1 Embedded microstrip

With this scheme we tried to keep the same electronic design than the one used on NEXT-DEMO, but to be used with the upgraded single ended electronics explained on section 3.2. Later, the electronics changed to a differential scheme in order to made the system more robust, and also did the DICE-Board as will be explained.

For the first design we tried to keep the scheme from NEXT-DEMO: one common bias voltage for all the SiPMs and some bypass capacitors to provide enough charge. But this time the capacitors were placed on the end of the pigtail, because by this way they will be behind the inner copper shielding which will attenuate the radioactivity on the active volume.

A microstrip is a type of electrical transmission line consisting of a conducting strip separated from a conductive plane by a dielectric layer known as the substrate. Then, an embedded microstrip is a microstrip which strips are also covered by a dielectric, typically used in multilayer PCBs or, as in our case, to gently protect the copper traces (as shown on figure 5.3). The initial design we made for the DICE-Board was an embedded microstrip scheme, with a copper plane for the bias voltage on one layer, and another layer for the SiPM signals traces and other lines. The main difference with the NEXT-DEMO scheme is that the copper plane now is connected to bias voltage instead of ground. This is because as the bypass capacitors are placed on the end of the pigtail, the current return along the DICE-Board goes via the bias. Then, from the capacitors to the

front-end the current return remains on the ground, so the cables should have an additional ground plane. This scheme is shown on the figure 5.6.

This approach was considered because with thin traces close to the bias plane (which will have the current returns) we avoid the noise coupling; and also the plane acts as shielding.

In order to optimize the design performance, we have taken into account two important issues when working with microstrips: crosstalk between neighbor lines and signal integrity; both detailed on the following sections.

5.1.1 Crosstalk

As a DICE-Board has 64 SiPMs providing very fast signals along 40 *cm* parallel traces and the copper plane is shared by all of them, a high crosstalk level can be found if the design is not properly done.

To have a crosstalk estimation on a microstrip line, we assume that the current density distribution on the copper plane as a function of the distance to the center is [Ott 2011]:

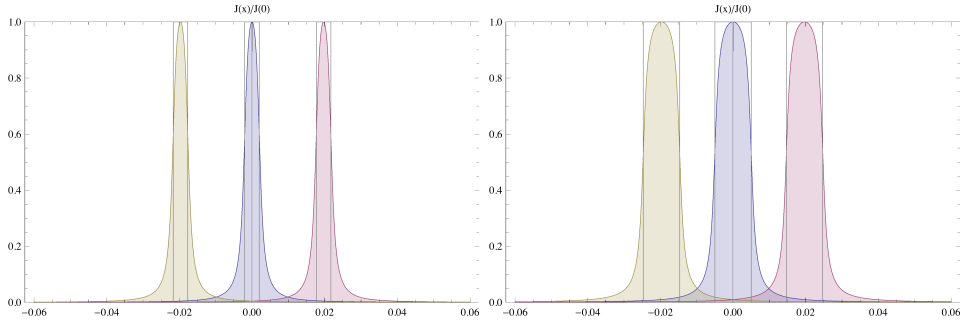
$$J(x) = \frac{I}{w\pi}\left[tan^{-1}\left(\frac{2x-w}{2h}\right) - tan^{-1}\left(\frac{2x+w}{2h}\right)\right] \tag{5.1}$$

Where "w" is the trace width, and "h" is the trace height above the copper plane. As said before, the chosen substrate base is the thinnest available to ensure the minimum crosstalk, which fixes the parameter "h" to 1 *mil*. Another fixed parameter is the trace pitch because, as was explained on the chapter beginning, the chosen connector will have 0.5 *mm* pitch. Still, these parameters could be changed if the expected performance in not good enough for the application.

In order to reduce the crosstalk to the minimum, and taking into account the connector pitch, the chosen trace width is 100 μm (3.94 *mils*). Several calculations were made with different traces widths and plane distances, two of them shown on the figure 5.2, where the current distribution on 3 consecutive traces can be

seen. As can be also seen, a thinner trace means less current overlap, but there are some manufacturing limitations for traces thinner than 100 μm, and this affects also to the trace impedance which will be studied later.

Also it was checked that a thinner core ("h") reduces the crosstalk, and more separated traces improve this parameter too. But we had to compromise a solution between design capabilities and performance.



(a) 100 μm *width, 1 mil heigh.* **(b)** 300 μm *width, 1 mil heigh.*

Figure 5.2: *Current density distribution for 3 traces comparison for different configurations, obtained as* $\frac{J(x)}{J(0)}$ *from the equation 5.1.*

For a long transmission line — considering long that it contains the effective length[1] of the generated signal rise time — the maximum theoretical crosstalk contribution can be estimated by the amount of current overlapped by two traces (in our case 500 μm pitch, or 19.68 $mils$), which can be calculated as:

$$\mathbb{k} = 100\,\frac{Overlapped\ Current}{Total\ Current} = 100\,\frac{\int_{pitch/2}^{\inf}\frac{J(x)}{J(0)}\,dx}{\int_{-\inf}^{\inf}\frac{J(x)}{J(0)}\,dx} \tag{5.2}$$

[1]The effective length of an electrical signal (or feature, like the rising edge) depends on the time duration of the feature and its propagation delay, which can be associated to a physical length that "contains" the feature [Johnson and Graham 1993]

For 1 *mil* (25.4 μm) polyimide thickness and 100 μm (3.94 *mils*) trace width, the maximum estimated crosstalk due to a neighbor signal is 3.27%; so the worst case (two neighbors) is 6.53%.

An important observation is that crosstalk does not depend on trace or plane copper thickness, so we had freedom choosing this parameter.

5.1.2 Stackup

For the embedded microstrip scheme, after some conversations with the manufacturer, the chosen stackup is the following:

- 127 μm (5 *mils*) polyimide coverlay
- 25.4 μm (1 *mil*) adhesive
- 25.4 μm (1 *mil*) gold plating
- 18 μm ($1/2$ *oz*) copper plane
- 25.4 μm (1 *mil*) polyimide base
- 18 μm ($1/2$ *oz*) copper traces
- 25.4 μm (1 *mil*) gold plating
- 25.4 μm (1 *mil*) adhesive
- 127 μm (5 *mils*) polyimide coverlay

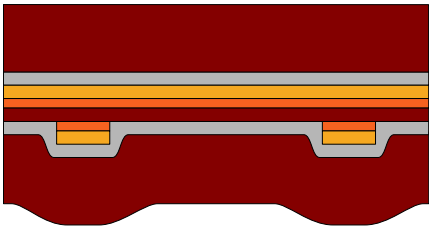


Figure 5.3: *DICE-Board section for embedded microstrip stackup.*

As mentioned before, the *Kapton* coverlay thickness was a compromise between mechanical and signaling performance, following the manufacturer advice. The pigtail passes through flat holes in the inner copper shielding, so it is the coverlay which sets the distance between the traces and the copper. Obviously a thick coverlay is desirable in this case, in order to avoid noise coupling or added crosstalk due to the copper shielding being too close; so we choose the thickest coverlay that still guaranteed the flexibility we need.

5.1.3 Transmission Line Parameters

The resultant stackup is an embedded microstrip with 100 μm traces, which main parameters were calculated using a 2D field solver [*MDTLC* n.d.]. For the polyimide dielectric constant the standard value of $Er_{polyimide} = 3.5$ is assumed, as this material is hard to characterize at high frequencies and we are working on a low frequency bandwidth [Oliver 2014].

DICE-Board line parameters:

- $R_{DC} = 94.07\ m\Omega/in$
- $C = 5.82\ pF/in$
- $L = 4.24\ nH/in$
- $Z_0 = 27\ \Omega$
- $T_d = 157.7\ ps/in$

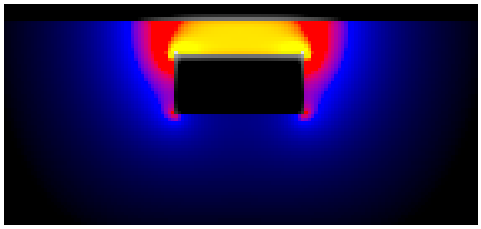


Figure 5.4: *Electric field simulation for the embedded microstrip stackup.*

On figure 5.4 the zero electric field is represented in black, so the trace is easily recognizable as the black rectangle in the middle and the copper plane is on the top of the plot. As can be seen the electric field is mostly confined between the trace and the plane, so barely can affect the adjacent traces or other stacked cables. No scale is shown as the plot is represented in arbitrary units and it is just representative.

In addition to the signal integrity, it is very important to know the voltage drop in the SiPM bias due to the signals they provide. Each event that produces signal discharges the SiPM to the front-end, and at the same time the SiPM takes current from the bias line to restore the internal charge and be ready for the next event. So the current that flows from the bias source (the decoupling capacitors or the power supply) will cause a drop in the bias line at the SiPM side due to the cable resistance and inductance; and a drop in the voltage, as explained in chapter 1, means gain reduction in the SiPMs.

In order to calculate this effect it is necessary to have the R_{AC} of the traces, because the SiPM signal is a short and fast pulse with high frequency

components. Even if the high frequency is not an issue for the electronics, as we are integrating the pulses, it will affect on how the signal is propagated along the cables. According to the manufacturers' specifications the rise time for a single photo electron — considering the fastest SiPM of the possible candidates — is about 2 ns, when the maximum signal amplitude is reached. From this value we can extract the highest frequency component of the signal as $T_R = \frac{0.35}{BW}$; so $BW = 160\ MHz$. As market devices are constantly being upgraded and new SiPM models are released every year, as security factor we took 500 MHz for the AC performance estimation; so this is the frequency the AC resistance is calculated for:

$$R_{AC} = \frac{\rho}{A} = \frac{\rho}{w\delta(f)} = \frac{\rho}{w\sqrt{\frac{\rho}{\pi f \mu_0}}} = 58.04\ \Omega/m = 1.474\Omega/in \tag{5.3}$$

Where $\rho = 17.094 \cdot 10^{-9}\ \Omega/m$ is the copper resistivity, $\mu_0 = 4\pi 10^{-7}\ TmA^{-1}$ is the vacuum permeability, w is again the trace width, and $\delta(f)$ is the current penetration depth as a function of frequency due to the skin effect. As it is known, the actual section of a conductor where a current is flowing becomes reduced as the frequency increases, which is called skin effect. In a microstrip transmission line the current tends to focus on the side of the strip close to the conductor plane, so the strip section actually used is $w \times \delta(f)$.

For the DICE-Board the maximum trace length is 40 cm ($\sim$ 16 in), so from the parameters obtained before we can extract:

$$R_{AC} = 23.58\Omega \quad R_{DC} = 1.505\ \Omega \quad C = 93.12\ pF \quad L = 67.84\ nH \tag{5.4}$$

On the other hand, we need also the bias plane parameters. The capacitance is the one of the signal trace, and for the AC resistance we can assume that the 80% of the current is contained in a distance $\pm 3\ h$ from the conductor center.

Assuming also a penetration of 1 skin depth, the plane AC resistance can be approximated to [Ott 2011]:

$$R_g(\Omega/in) = \frac{\rho}{6h\delta(f)} \tag{5.5}$$

So for a frequency $f = 500\ MHz$; and $h = 1\ mil \longrightarrow Rg = 0.968\Omega/in$.

About the inductive reactance of the copper plane [Ott 2011]:

$$X_{Lg} = 2\pi f L_g = 4.59 \cdot 10^{-10} \cdot f \cdot 10^{15.62h} \tag{5.6}$$

$$L_g = \frac{4.59 \cdot 10^{-10} \cdot 10^{15.62h}}{2\pi} = 75.7\ pH/in \tag{5.7}$$

So for the 16" DICE-Board pigtail, the bias plane parameters are:

$$R_{ACplane} = 15.49\Omega \qquad L_{plane} = 1.21\ nH \tag{5.8}$$

Notice that the $R_{DCplane}$ is not taken into account, because due to the geometrical size of the copper plane the value is just a few milliohms, negligible compared with the $R_{ACplane}$.

5.1.4 Bypass Capacitors

As the SiPMs provide quick current pulses, *Hamamatsu* recommends placing a capacitor close to each SiPM. For that reason we have simulated a bunch of capacitors of different values, in order to cover all the possible frequencies.

This capacitors, if needed, will be placed on the end of the pigtail behind the inner copper shielding; because one of the most important detector requirements is the low radioactive background and the capacitors are not radiopure enough.

The chosen capacitors are from *Kemet* low inductance commercial series, and as is shown on figure 5.5, with the selected capacitors we achieve a very low ESR (Equivalent Series Resistance), below $\sim$ 100 $m\Omega$, in the range from 10 kHz to 500 MHz. This allows a very quick current pulses from the capacitors to the SiPMs.

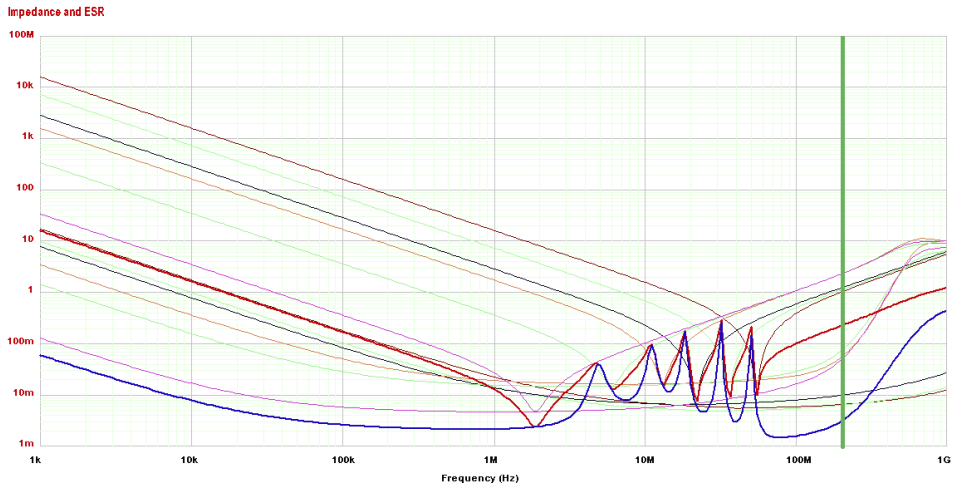


Figure 5.5: *Frequency performance simulation of the 7 chosen capacitors in parallel, done with the software provided by Kemet. The thick blue line represents the combined ESR, and the thick red line the combined impedance.*

Then, the models of all the capacitors with their parasitic components (ESR and inductance) were added to the signal simulation.

In the simulation there is an extra inductance connected from the capacitors to the bias plane, which represents the plated through vias of the DICE-Board design. The equation for the via inductance calculation was taken from [Johnson and Graham 1993]. For measures in inches, the result is in nH:

$$L_{via} = 5.08h\left(ln\left[\frac{4h}{d}\right] + 1\right) \tag{5.9}$$

So for a via with $h = 4.4\ mils$ (1 mil polyimide $+2 \times 0.7\ mils$ copper layers $+2 \times 1\ mil$ plating) and $d = 15.7\ mils$, the inductance is $L_{via} = 24.9\ pH$.

If we have 14 parallel vias connecting the capacitors with the bias plane, the total inductance is 1/14 the inductance of one via: 1.78 pH. Notice that this inductance is negligible compared with the capacitors parasitic inductances, due mostly to their package, which are in the order of $\sim 1\ nH$; but is still used as some simulations without capacitors are also performed.

5.1.5 Simulation

The most important thing to achieve with the design is to keep a good SiPM signal, and have the minimum bias voltage drop after the SiPM recovery time. If the bias drop is too high, the SiPM gain will be reduced, which reduces the resolution.

The main fact that keeps the bias voltage stable is the capacitance seen from the SiPM terminal, which is composed by the bypass capacitors and the parasitic capacitance. At this point, we started to wonder what is the minimum capacitance required for our purpose, because due to the DICE-Board cross section geometry there is a non negligible capacitance already in the pigtail. It will be a great improvement in the radioactive budget if we could remove all the capacitors from the design, and for that reason we focused the simulations also in this option.

The first simulation was just to check the performance of the DICE-Board, using the SPICE software *Tina-TI* from *Texas Instruments*. The scheme includes the 16" microstrip traces, the SiPM electrical model described in chapter 1, the bunch of capacitors previously selected with their parasitic components, and the vias inductance. A simplified version of the scheme is shown on figure 5.6, while the simulation circuit can be found on figure 5.7.

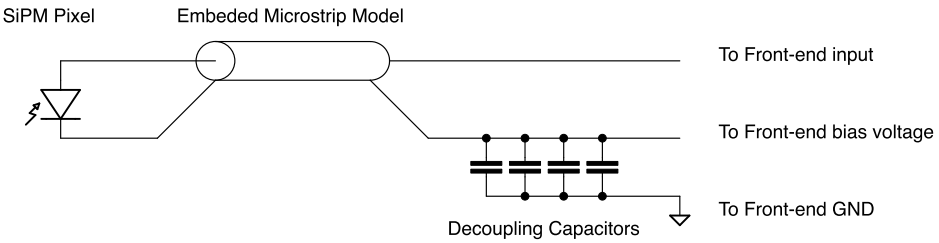


Figure 5.6: *Simplified scheme for the embedded microstrip approach.*

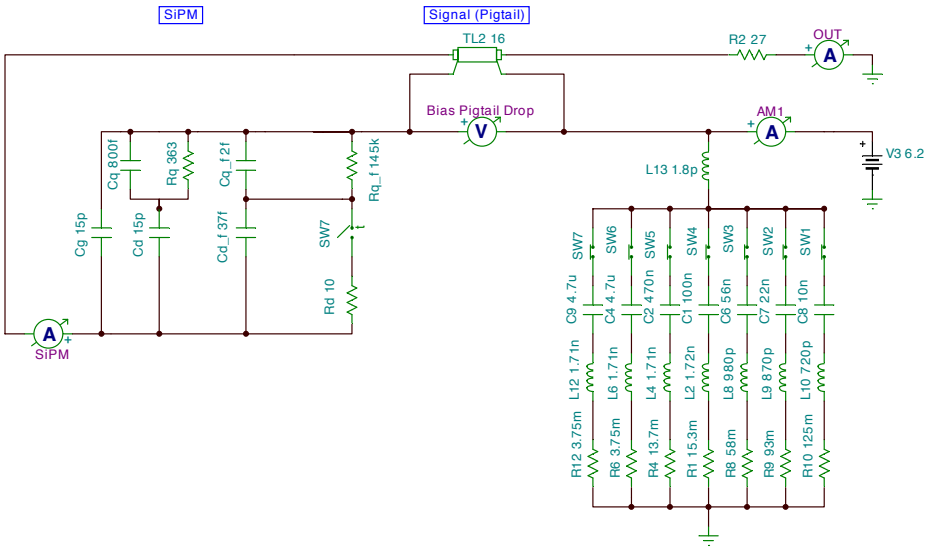


Figure 5.7: *Simulation circuit for the embedded microstrip approach.*

The performed simulation (figure 5.8) showed a fantastic result for the signal integrity, which is almost identical to the SiPM output but slightly delayed. The middle plot shows the DICE-Board output while the lower is the SiPM signal, both measured as current. The upper plot represents the bias voltage drop along the DICE-Board pigtail, which has the same shape than the SiPM signal. As can be seen the drop has a maximum of 1 mV and a duration of $\sim$ 20 ns, which will be analyzed later on this section.

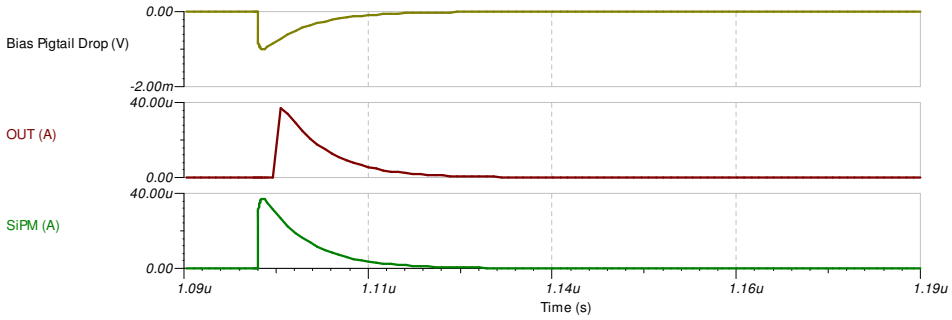


Figure 5.8: *DICE-Board simulation results. From top to bottom: Bias Voltage Drop, DICE-Board Output and SiPM signal.*

Then the capacitors were disconnected from the simulation, and surprisingly the result was identical. Still we kept them in the first design as we were skeptical to this result, and were still simulated later in the full chain model to be sure of the overall performance.

The DICE-Board pigtail will be connected to a long cable, then to the feedthrough and another long cable that goes to the front end electronics. This cables were simulated just as a 4 m cable because the mechanical design of the detector was not finished at this stage, but still would give us an idea of the foreseen performance. The long cable was modeled with the same stackup of the DICE-Board, as that was the initial idea in order to keep a stable transmission line. On figure 5.10 the simulation of a DICE-Board with a 4 m cable is shown, with a very promising result.

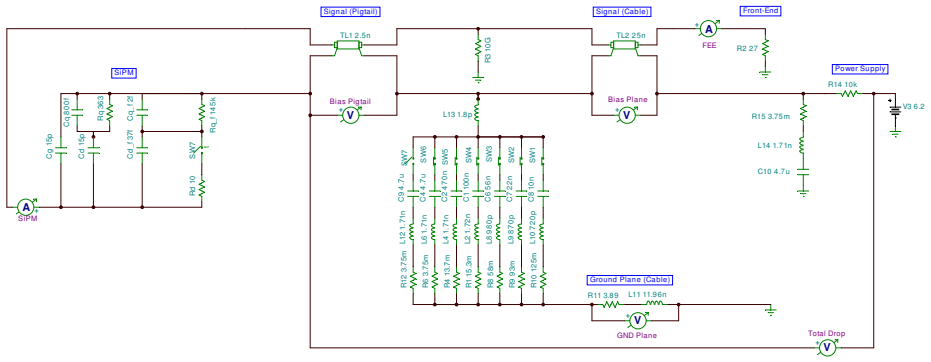


Figure 5.9: *DICE-Board and cable simulation circuit.*

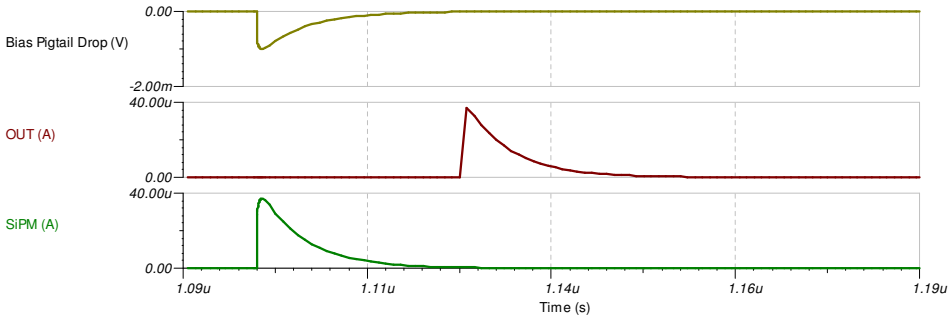


Figure 5.10: *DICE-Board and cable simulation. From top to bottom: Bias Voltage Drop, DICE-Board Output and SiPM signal.*

As shown, the signal shape has no changed and neither did the bias voltage drop. Of course this is still an ideal result with a perfect transmission line termination, and that will change once we simulate the full chain with the front-end electronics.

Again the simulations were done with and without the bypass capacitors and, fortunately, there were no difference between both of them. Assuming that capacitors are not needed, we can avoid the ground for the cable design and the current return will be along the bias plane, as in the DICE-Board. If that

is the case, the cable will have exactly the same stackup than the DICE-Board pigtail, but 4 m long. So for a 4 m cable (160 *inches*) the parameters of the traces and the bias plane can be obtained from the previous equations, or just scaling up the ones from the DICE-Board:

$$R_{AC} = 235.84\ \Omega \quad R_{DC} = 15.05\ \Omega \quad C = 931.2\ pF \quad L = 678.4\ nH$$
$$R_{ACplane} = 154.88\ \Omega \quad L_{plane} = 12.1\ nH$$

Regarding the voltage drop in the SiPM bias, we can assume that the recovery current for a SiPM pixel is the same than the signal current (seen in simulations), and all the current flows along the bias copper plane that compose the microstrip design. Then, the voltage drop in the bias has the same shape than the signal current, proportional to the resistance seen by the SiPM. As seen in the simulation showed on figure 5.10, the signal has a smaller effective length than the cable length, so as the signal is contained in the cable the impedance seen by it is the one of the transmission line: 27 Ω.

In round numbers, we have a current peak of $\sim 40\ \mu A$ that produces a drop of $\sim 1\ mV/pe$ during $\sim 20\ ns$.

The dynamic range designed is 250 $pe/\mu s$. Each DICE-Board has 64 SiPMs, so assuming 16 SiPMs fully illuminated we have 4000 $pe/\mu s$.

With an expected homogeneous distribution of light we have 80 $pe/20\ ns$, which gives us a maximum drop of 80 mV. For the *Hamamatsu* SiPMs, that have the highest gain/voltage dependence, the variation is $0.05\%/mV$. So that results in a maximum gain variation of 4% in the worst case scenario. That is below the 5% design requirement but still slightly high. Fortunately, from this point of view, the change in the electronics lead us to modify also the DICE-Board design to a new one that solved this problem.

Finally and previously to the design change we produce several units of the DICE-Board with the microstrip stackup, and we successfully tested the performance. One DICE-Board with some *Hamamatsu* SiPMs was placed inside

a black box with a pulsed LED, and then connected to the front-end electronics prototype (the one detailed on section 3.2).

This allowed us to made the first real mechanical test of a *Kapton* DICE-Board with a flexible pigtail, and also several electronic tests that ensure we were on the right track. We could check that definitively the bypass capacitors were not needed, which made very happy the people working in the radiopurity and background simulations. Some crosstalk tests were also performed and the results showed that, for the DICE-Board length, there was no measurable crosstalk.

5.2 Broadside Coupled Traces

As explained on section 3.3, the coupled noise we had in NEXT-DEMO made more complicated the data analysis and lead us to adopt methods to reduce system noise. After some discussions with experts in this field, we decided to make a little effort and upgrade the electronics as a differential scheme.

Of course that affected the DICE-Board design, which now had to hold the double number of traces. Some brainstorming later we discarded the "ribbon" scheme which will have all the traces side to side, because the current loop will expose to much area and the noise pick up will be dangerous. Alternatively, we decided to keep the same stack up configuration changing the copper plane to individual traces. So the broadside coupled traces DICE-Board concept was born. Well thought the idea is very simple: just two long wires connecting the SiPM anode and cathode to the differential front-end input; and its tight geometry avoids the noise pick up while adds enough parasitic capacitance to keep the bias voltage stable.

As we already had chosen very dense 2-row connectors, this change allowed us to reuse almost all the previous design. So it was just a matter of checking the design by simulation prior to manufacturing the new DICE-Boards.

In fact the crosstalk simulation would not be needed for the DICE-Board because now the SiPM do not share bias plane, so there is no current overlap as seen

for the microstrip scheme. So, for sure, the crosstalk between channels will be smaller than the one estimated for the microstrip DICE-Board, which was already good enough theoretically and measured negligible for the DICE-Board length. Still the capacitive crosstalk should be taken into account, but due to the geometrical design (see figure 5.11) it is expected also to be negligible compared with the external cables, as will be detailed on next chapter.

5.2.1 Stackup

For the new DICE-Board stackup we preserved the same configuration than the last time because it worked perfectly from the mechanical point of view, has the thinnest core tho keep the two differential lines as close as possible and the measured radioactivity was inside the range of acceptance for the experiment.

The new DICE-Board cross section is shown on figure 5.11.

- 127 μm (5 *mils*) polyimide coverlay
- 25.4 μm (1 *mil*) adhesive
- 25.4 μm (1 *mil*) gold plating
- 18 μm ($1/2$ *oz*) copper traces
- 25.4 μm (1 *mil*) polyimide base
- 18 μm ($1/2$ *oz*) copper traces
- 25.4 μm (1 *mil*) gold plating
- 25.4 μm (1 *mil*) adhesive
- 127 μm (5 *mils*) polyimide coverlay

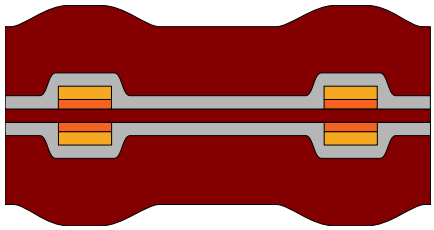


Figure 5.11: *DICE-Board section for broadside coupled traces stackup.*

5.2.2 Line Parameters

The line parameters for the broadside coupled traces were obtained again using a 2D field solver [*MDTLC* n.d.]. This time, as the configuration is a differential transmission line the software gives the results for the differential and common mode, corresponding to the odd and even electric field respectively.

Thinking about it we came to the conclusion that the transmission line can be modeled just as a differential one, discarding the common mode. As mentioned before the SiPM is connected in a closed loop, so the current signal on the

trace connected to the anode is the same as the one on the trace connected to the cathode, but opposite polarity. This approach assumes that, for our operation range (V/I), the SiPM acts as a symmetrical source. This kind of performance was checked first by simulation, and later with the differential front-end prototype showed on section 3.3.

As we use the line as differential, only the differential or odd parameters are useful for us. However the common or even parameters are also shown as representative example.

DICE-Board line parameters for odd (differential) mode:

- $R_{DC} = 94.07\ m\Omega/in$
- $C = 9.33\ pF/in$
- $L = 2.66\ nH/in$
- $Z_0 = 33.8\ \Omega$
- $T_d = 157.7\ ps/in$

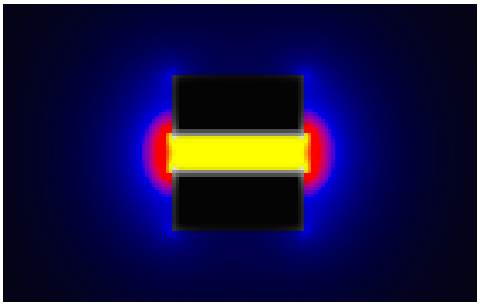


Figure 5.12: *Odd mode electric field simulation for the broadside coupled traces stackup.*

Same than last time, on figure 5.12 the absence of electric field is represented in black. The two traces can be easily recognizable as the black rectangles in the center. As can be seen the odd electric field is confined to the area between the two traces, even more than for the microstrip approach. So, as explained, the channel to channel crosstalk should not be a problem, both for adjacent lines or stacked cables.

About the line parameters obtained they are quite similar to the previous ones, so no surprises about the signal integrity are expected. The most significative change is the increase of the capacitance as opposed to the inductance reduction. The capacitance expected effect is a more shaped signal on the output, but that also will help to keep the bias voltage stable. Note also that the simulation

assumes a fully differential signal, so by definition the impedance seen by the signal is double the impedance expected for a conductor for that inductance and capacitance parameters [Johnson and Graham 2003].

To obtain the R_{AC} resistance we can use the result from the equation (5.3), as the geometry of the trace is the same than the microstrip. In fact that applies to both traces, signal and bias, as the design is symmetric. With all the values in hand the line parameters for the DICE-Board (40 cm or 16") are:

$$R_{AC} = 23.58\Omega \quad R_{DC} = 1.505\ \Omega \quad C = 149.3\ pF \quad L = 42.6\ nH \tag{5.10}$$

For the long cable, again as a representative result because they were not chosen yet, we assumed the same DICE-Board stackup for a 4 m (16") length; so the values are just a factor 10 over the DICE-Board ones.

Finally, as said just to keep in mind the effect, the DICE-Board line parameters for even (common) mode are:

- $R_{DC} = 94.07\ m\Omega/in$
- $C = 0.649\ pF/in$
- $L = 25.6\ nH/in$
- $Z_0 = 99.3\ \Omega$
- $T_d = 128.9\ ps/in$

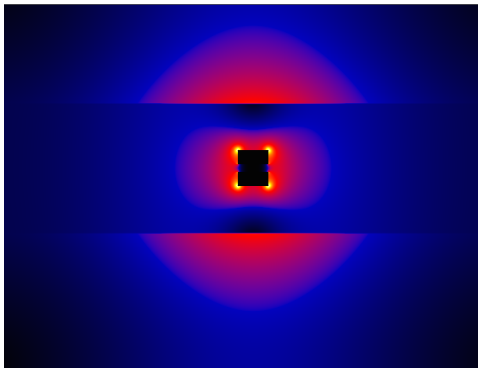


Figure 5.13: *Even mode electric field simulation for the broad side coupled traces stackup.*

The even mode or common mode electric field is shown on figure 5.13. Note the zoom out needed to cover the area where the electric field is spread. Again, the traces are represented as the black rectangles in the center, and the cable

coverlay limit can be identified as the horizontal pattern for the electric field transition over and below the traces. This helps to understand that this type of configuration used for common mode signals will have a huge crosstalk effect in all directions, so some shielding or other solutions will be need to make this work. Fortunately is not our case.

Note that, on the contrary than the odd mode case scenario, the even mode transmission over a differential line causes the line impedance to be half the expected, as technically the conductor is almost equivalent to one with double the section [Johnson and Graham 2003].

5.2.3 Simulation

Following the same procedure, we performed several simulations with the new line parameters in order to discard design problems. As before the simulations worked as expected for both signal integrity and bias voltage drop. The simulation circuit for the DICE-Board and cable is shown o figure 5.14, and the results can be found on figure 5.15; again, with ideal conditions for the line termination.

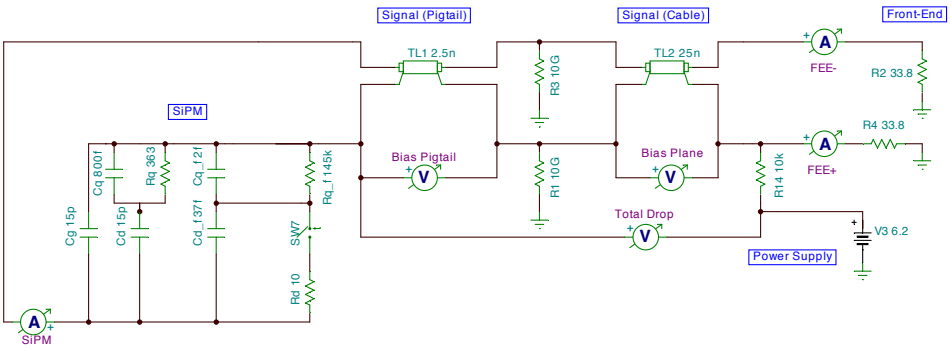


Figure 5.14: *DICE-Board and cable simulation circuit.*

As can be seen, the current signals provided by the SiPM anode and cathode have identical shape, but opposite polarity. Also the output signals are a bit

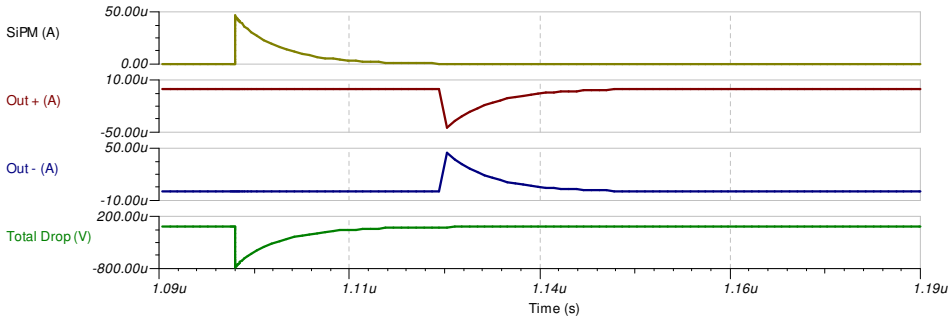


Figure 5.15: *DICE-Board and cable simulation. From top to bottom: SiPM signal at anode, positive and negative outputs at the front-end side, and bias voltage drop measured at the SiPM cathode.*

slower then the input, not important as long as the total charge is preserved and the signal length does not exceed the integration time (1 μs).

About the bias voltage drop now is $\sim$ 800 μV during $\sim$ 20 ns, a bit smaller in amplitude than the measured for the microstrip scheme. Anyway, doing the same calculations for the gain variation, even considering 1 mV for the bias drop, the impact on the performance has been reduced due to the new scheme. The dynamic range designed is 250 $pe/\mu s$. But now each SiPM has its own bias trace, so they do not interact with other SiPMs on the same DICE-Board, so the maximum expected light for a single SiPM is 250 $pe/\mu s$. With an expected homogeneous distribution of light we have 5 $pe/20$ ns, which gives us a maximum drop of 5 mV. With a gain/voltage dependence of 0.05%/mV results in a maximum gain variation of 0.25% in the worst case scenario. That is far below the 5% design requirement, so this will not be an issue even for high luminescence signals.

5.3 Finishing the DICE-Board

After the theoretical design of the DICE-Board and prior the production some details must be considered, like the mechanical design and some useful additions to the board. Also, to satisfy the experiment requirements, the radiopurity measurements must be taken into account before the final product validation.

5.3.1 Mechanical Design

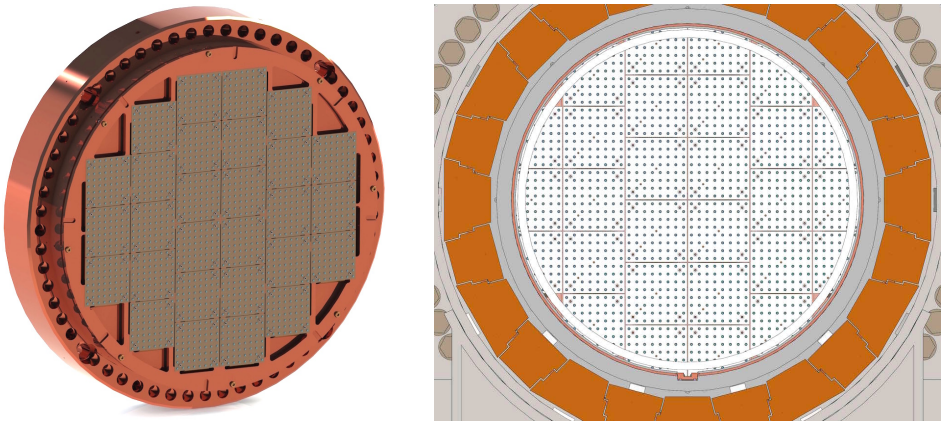
In order to achieve the best design for the NEW tracking plane the electronic and mechanical engineers have been working very close, thereby design iterations can be done quickly. From the physics point of view there are some important design requirements: 10 *mm* pitch for the SiPM array, precise distance between the SiPMs and the field cage anode, maximum coverage area, and radiopurity.

The pitch requirement and the total number of SiPMs lead to the design of the DICE-Board array, an 8×8 array as compromise between number of boards and their size. To have 64 channels per board is also desirable, as is a number commonly used for ASIC and front-end designs.

For the maximum coverage area, we did a misaligned distribution of the DICE-Boards fitting the inner diameter of the pressure vessel and trying to cover all the inner light tube area. As can be seen on figure 5.16b almost the 100% of the surface is covered.

The radiopurity requirements were accomplished with a combination of material selection and the proper shielding of the most radioactive components. As described on chapter 1 the tracking plane main structure is a 12 *cm* copper plate with flat "v" shaped holes for the DICE-Board pigtail to pass through them. This way the connectors (known as radioactive) are placed behind the copper, which acts as shielding, and the "v" shape avoids straight paths for the gammas to reach the fiducial volume.

For a precise alignment to the field cage anode and the vessel, a thin copper plate is mounted over the thick copper shielding using springs. Thereby when



(a) *Computer generated picture of the NEW tracking plane.*

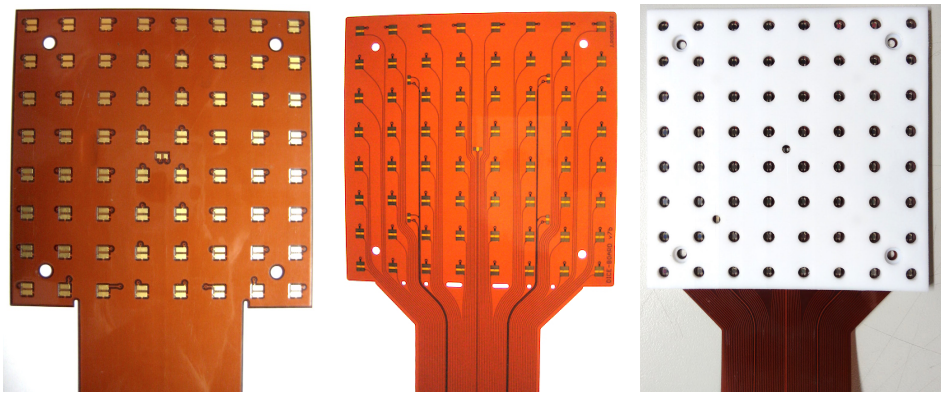
(b) *Front view of the NEW tracking plane from the inside of the detector.*

Figure 5.16: *NEW tracking plane design details.*

the endcap is closed the thin plate is auto-aligned to the field cage and the light tube, and a spring loaded contact ensures the electrical connection. As shown on figure 5.16a the DICE-Boards are mounted on the thin plate, and as explained on chapter 1 the field cage gate and anode are also mounted over it. This way all the parts can be precisely aligned.

Another issue we had was the folding point between the squared area of the DICE-Board (what we called "head", where the SiPM array is placed) and the pigtail. Lot of DB designs were made, to adapt the characteristics to the requirement changes; and a total of 3 batches were manufactured. Figure 5.17 shows the heads and folding areas for the three DICE-Boards produced.

The first produced design was the microstrip DICE-Board (figure 5.17a). As this one has a copper plane it is stiffer, and for that reason the design had two small grooves on the pigtail sides; this way we increase the available folding radius. For the first broadside coupled traces DICE-Board (figure 5.17b) the available routing area was reduced because the copper plane disappeared. So the transition from the pigtail to the head became wider and we did not have space for the grooves. Instead we made some holes along the folding line, which



(a) *DB v5a version.* **(b)** *DB v7b version.* **(c)** *DB SLKv2 version.*

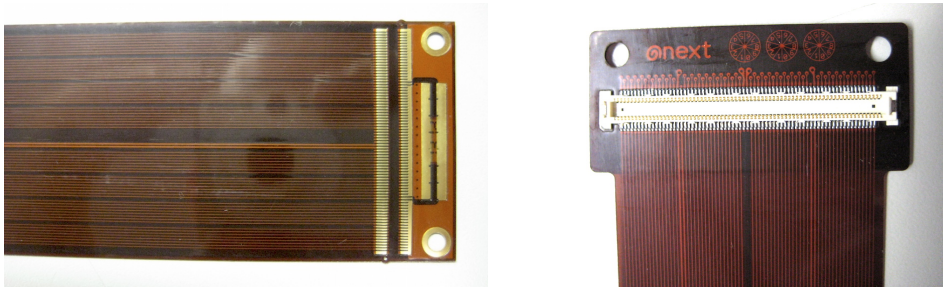
Figure 5.17: *Different designs for the DICE-Board pigtail folding.*

we thought will help to fold the board. But we were wrong: the new stackup was softer and this holes made the folding more delicate, and without enough care the joint could crack and break the traces. Last design, shown on figure 5.17c, had the same concept than previous one but adapted to the *SensL* SiPM footprint. On this iteration we removed the holes, as the stackup without copper plane could be easier bent. The picture shows also the PTFE mask added to the tracking plane to increase the light collection.

Another design detail we were concerned about was the pigtail end, where the connector is placed (both designs produced shown on figure 5.18).

As can be seen on figure 5.18a the first design had room for the bias voltage coupling capacitors, which were later discarded. The connector used was from the *Panasonic P5KS* series, the 160 pin version. The pigtail width was adjusted to the connector length to optimize the space and minimize the hole size needed in the copper shielding.

Later we had to replace the connector, as the *P5KS* series fabrication was discontinued. As replacement we chose the *FX11* series from *Hirose*, a 140 pin connector which is more flat, robust and with longer lifetime. As shown in figure 5.18b we kept the same width for the connector area, but the pigtail itself



(a) *DB v5a version.* **(b)** *DB v7b and SLKv2 version.*

Figure 5.18: *Different designs for the DICE-Board pigtail end, where the connector is located.*

was more narrow to improve the flexibility. Also a 254 μm polyimide stiffener was included on the connector area in order to make it more robust, and some marking numbers were added. This pigtail end design was kept for further designs, as it showed very good performance and stability.

In addition, to make the DICE-Board more useful, the design included a NTC sensor and four LEDs. The NTC is a sensor which resistance depends on the temperature, and was chosen due to the very small package (0603 SMT size) and the low radioactivity due to the absence of any plastic on the package. The device we chose is the *NCP18XH103F03RB* from *Murata*, and it is placed on the geometrical center of the DICE-Board head, on the same side than the SiPMs. This way we ensure that the temperature measured is the same than the SiPMs, and the value can be used to compensate the bias voltage and keep the gain stable (see Chapter 7).

Finally the four blue LEDs are placed on the center of each quadrant of the DB head, thereby the whole tracking plane is a 4×4 cm pitch LED array. They can be driven independently from the front-end electronics, and will help for the geometrical characterization of the detector. The devices selected are the *OSRAM LB Q39E-N1P1-35-1*, which are also 0603 SMT size, 470 nm wavelength and were also checked for radiopurity levels.

5.3.2 Radiopurity issues

There are various potential components of the background spectrum of NEXT in the energy region around $Q_{\beta\beta}$ [J. Martín-Albo et al. 2016]. The relevance of any background source in NEXT depends on its probability to generate a signal-like track in the active volume of the detector with energy around the Q value of ^{136}Xe. In principle, charged particles (muons, betas, etc.) entering the detector can be eliminated with high efficiency ($> 99\%$) by defining a small veto region (of a few centimeters) around the boundaries of the active volume. Electric field inhomogeneities or malfunctioning photosensors could affect negatively this performance, but those effects can be measured with periodic calibrations using, for instance, crossing muons. Confined tracks generated by external neutral particles (such as high-energy gamma rays) or by internal contamination in the xenon gas can be suppressed taking advantage of the distinctive energy-deposition pattern of signal events.

Natural radioactivity in detector materials and surroundings is, as in most other $\beta\beta0\nu$ decay experiments, the main source of background in NEXT. In particular, the hypothetical $\beta\beta0\nu$ peak of ^{136}Xe ($Q_{\beta\beta} = 2458.1 \pm 0.3\ keV$) lies in between the photo-peaks of the high-energy gammas emitted after the β decays of ^{214}Bi and ^{208}Tl, intermediate products of the ^{238}U and ^{232}Th series, respectively.

The NEXT Collaboration is carrying out a thorough campaign of material screening and selection using Ge gamma-ray spectroscopy (with the assistance of the LSC Radiopurity Service) and mass spectrometry techniques (ICPMS and GDMS). Several measurements have been performed since 2011, thereby a database of more than 150 materials used in NEXT have been recorded [Cebrián et al. 2015a] [Cebrián et al. 2015b]. The design of a radiopure tracking plane, in direct contact with the gas detector medium, was specially challenging since the needed components like printed circuit boards, connectors, sensors or capacitors have typically, according to available information in databases and in the literature, activities too large for experiments requiring ultra-low background conditions. Table 5.1 summarizes the activities measured for the main tracking plane elements, some of them discarded or replaced due to its excessive values.

Material	Units	^{208}Tl (^{232}Th Chain)	^{214}Bi (^{238}U Chain)
CuFlon DICE-Board	mBq/pc	< 0.25	0.28 ± 0.08
Adhesive (CuFlon)	mBq/pc	0.04 ± 0.004	0.28 ± 0.02
Kapton DICE-Board v5a	mBq/pc	0.04 ± 0.01	0.03 ± 0.01
Kapton DICE-Board v7b	mBq/pc	0.031 ± 0.004	0.068 ± 0.007
Molex Connector	mBq/pc	2.62 ± 0.18	1.68 ± 0.10
Panasonic P5K Connector	mBq/pc	3.4 ± 0.5	6.0 ± 0.9
Hirose FX11 Connector	mBq/pc	2.3 ± 0.36	4.6 ± 0.7
Hamamatsu $1mm^2$ SiPM	μBq/pc	17 ± 2	33 ± 3
SensL $1mm^2$ SiPM	μBq/pc	< 0.72	< 2.7
LED	μBq/pc	3.3 ± 0.4	2.1 ± 0.3
NTC	μBq/pc	< 0.108	< 0.8
Solder Paste	mBq/kg	< 13	< 6.5
M2 Screws	μBq/pc	< 1.04	< 3.7
M2 Inserts	μBq/pc	< 1.2	< 3.6
PLA Filament	mBq/kg	< 1.5	< 6.6
Adapter Boards	mBq/pc	45.4 ± 2.5	84.4 ± 3.9
Feedthroughs	Bq/kg	6.6 ± 0.3	13.6 ± 0.6

Table 5.1: *Activities measured in relevant tracking plane materials for NEXT in* 2015 *and* 2016. *Reported errors correspond to* 1 σ *uncertainties and upper limits are given at* 95% *C.L.*

Printed circuit boards are commonly made of different materials and a large number of radiopurity measurements can be found. Therefore, several options have been taken into consideration for the substrate of SiPMs arrays. FR4 was disregarded because of both an unacceptable high rate of outgassing and bad radiopurity; glass fiber-reinforced materials at base plates of circuit boards are generally recognized as a source of radioactive contamination. *CuFlon* offers low

activity levels, as shown in the measurement of samples from *Crane Polyflon* by GERDA, using both ICPMS and Ge gamma spectroscopy; and the main activity of this material is focused on the adhesive used to bond the layers, measured also separately. On the other hand, components made of just *Kapton* (like *Cirlex*) and copper offer very good radiopurity. Therefore, new DB produced by *FlexibleCircuit* using only *Kapton*, plated copper and adhesive were analyzed. A two layer adhesiveless base substrate with polyimide coverlay on both sides, which only requires a little amount of adhesive, was chosen for the boards manufacturing. For the radioactivity results, only the exposed area of the DICE-Board has been taken into account.

Different kinds of board-to-cable connectors were measured, in particular FFC/FPC (Flexible Printed Circuit & Flexible Flat Cable) connectors supplied by *Hirose* and similar *P5K* series connectors from *Panasonic* were considered, finding activities of at least a few mBq/pc for isotopes in ^{232}Th and the lower part of ^{238}U chain. Thermoplastic connectors from *Molex* were also screened, giving values slightly smaller but of the same order. Since all these connectors contain Liquid Crystal Polymer (LCP), it seems that the activity measured is related to this material. As the activity of connectors would give an unacceptable high rate in the region of interest a direct bonding of the cables to the *CuFlon* DBs was originally foreseen; however, in the final design using the all-in-one *Kapton* DBs, connectors are placed behind the inner copper shield thanks to the pigtail design.

Concerning SiPMs, although silicon is, as germanium, a very radiopure material with typical intrinsic activities of ^{238}U and ^{232}Th at the level of few $\mu Bq/kg$, materials used in the substrate or package of the chip can be radioactive. That is exactly what happened with the *Hamamatsu S10362-11-050P* SiPMs, which showed a huge activity in the chains of interest making impossible using them for the NEXT experiment. Fortunately, the *SensL MicroFC-10035-SMT-GP* use a different material for the package and the measured activity is small enough for the NEXT requirements.

As the NTC sensors and the LEDs are placed also in the active volume of the detector, their contribution to the background must be well quantified. Both

elements showed a small activity in the chains of interest, specially the NTCs as they are basically silicon oxide. About the LEDs, although their activity is also small, we decided to limit the use to just one unit per DICE-Board.

Other materials were also screened, even though they are placed behind the copper shielding and far away from the active volume. Some of them, like the feedthroughs and the adapter boards, have a relative high activity for the isotopes ^{214}Bi and ^{208}Tl; so the addition of their contribution to the Monte Carlo simulation is very important to obtain a reliable system model.

About the PLA filament, used in several 3D printed pieces explained in chapter 6, we chose the translucent one as it should have less additives and pigments. The low activity measured for this material allowed us to speed up the production of some parts, as the time required from design to prototyping is substantially reduced.

Nowadays the screening campaign keeps on, looking for alternative materials that may improve the background for NEXT-100.

"Neo, sooner or later you're going to realize, just as I did, that there's a difference between knowing the path, and walking the path."

– Morpheus (The Matrix)

6

From the SiPM to Front-end: The Cabling Problem

As was explained on section 1.6, the SiPM provide a very small current signal for each photon captured. So one of the biggest problems is how to transport thousands of these signals from the photodetectors to the front-end electronics, crossing through the pressure vessel, and traveling along several meters of cables, without losing the information.

The front-end electronics are placed as close as possible to the detector, but due to radiopurity requirements they must be outside the lead castle. So, even in the best case, the signal should travel along the DICE-Board pigtail, about one meter cable from it to the inner side of the feedthrough, cross it, and then travel along other cable four meters to the rack where the electronics are placed.

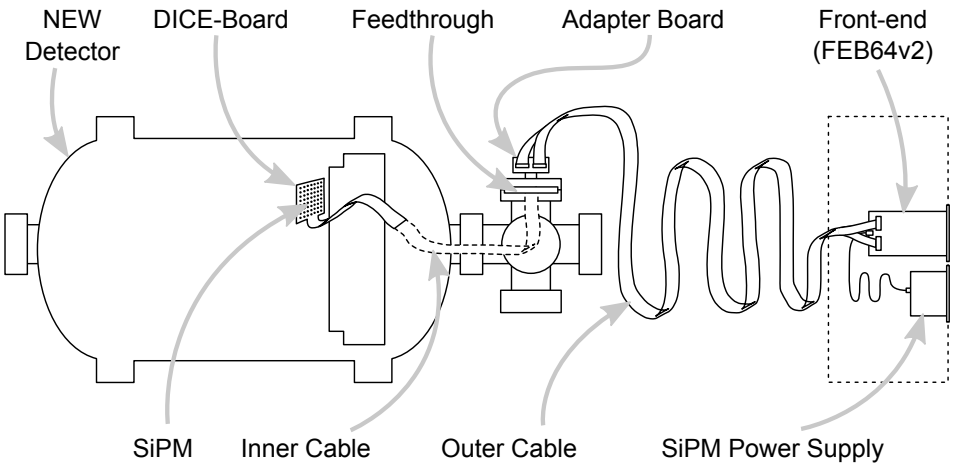


Figure 6.1: *NEW Detector tracking plane scheme. The full signal chain from the silicon photomultipliers to the front-end electronics is shown.*

6.1 Inner Cables

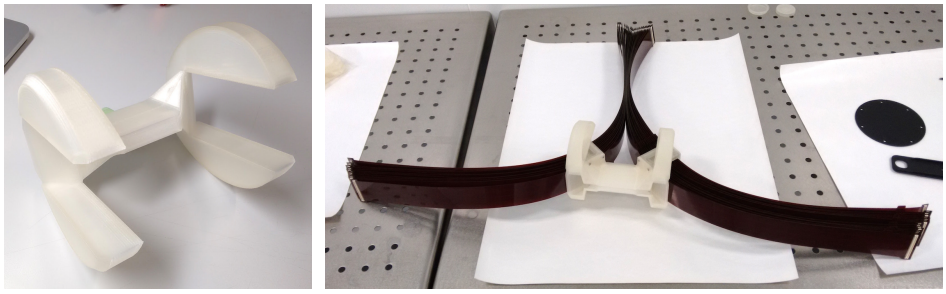
As explained on the previous chapter the ideal scenario will have all the cables identical, so the transmission line has a perfect continuity. But there are several restrictions to do that: the technology used for the DICE-Board is very precise and need very tiny tolerances on the production, so the cost would be excessive for long cables, or lots of short cables should be used. But they are affordable for shorter lengths so we used them for the inner cables, which connects the DICE-Boards to the inner feedthrough side.

These cables have exactly the same stackup than the DICE-Board and the same geometry than the pigtail. For the ends we used also the same connector, header on one side and receptacle on the opposite side; thereby the cables can be connected in series without modifying the pinout, and achieve larger lengths.

As a manufacturing limitation, the company we worked with can only make up to 40 *cm* size boards, still at a reasonable price; so we design the inner cables with that length. As one cable is too short for the purpose, two cables have to be

connected in series in order to connect the pigtail to the feedthrough and leave enough room for the tracking plane copper plate to be opened.

To ensure that two cables were enough a full size mock-up was built in the laboratory, using a 3D printer and PVC pipes. Then we realized that, even though the cables length was enough, the cables tend to disconnect, and were hard to manage inside the tubes that connect to the feedthrough. For this reason we designed clamps to fix the connection between cables and also to the feedthrough; and a structure to hold all the cables inside the tubes and distribute them cleanly. This structure was designed to fit perfectly inside the "space ship" port (described on section 6.3.2), and after some tests we 3D-printed the final design shown on figure 6.2a, which we called the "TIE Fighter".



(a) *3D printed "TIE Fighter" structure.* **(b)** *The 56 inner cables (28 × 2) assembled to the "TIE Fighter".*

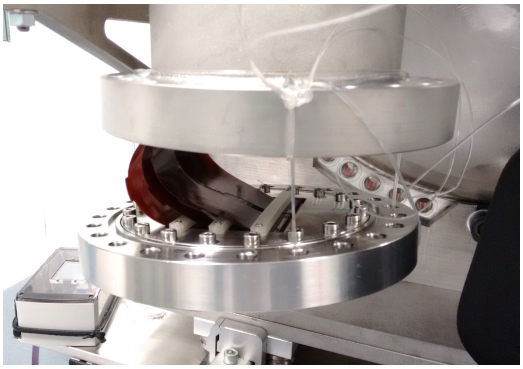
Figure 6.2: *Inner cables attached to the holding structure before installation.*

The use of the 3D printer gave us the possibility to produce our designs on the spot, which shortened a lot the time between the idea and the real test; and producing the final parts in the laboratory saves money and time. The mechanical characteristics of the printed PLA are known to be very good, and the low mass of the pieces means less radioactive contribution. Of course the PLA radiopurity was measured, and we had green light to made the needed pieces.

The clamps were also 3D printed, and after some prototypes we produce a whole set for all the NEW tracking plane cabling. On figure 6.3a is shown

the connection between the DICE-Boards pigtails and the inner cables using the clamps; and figure 6.3b shows the connection to the feedthrough.

(a) *Inner cables connected to the DICE-Board pigtails on the copper shielding back side.*



(b) *Inner cables connected to the feedthrough.*

Figure 6.3: *Inner cables installation on November 2015.*

Regarding the electrical properties of the inner cable, no surprises were expected as the DICE-Board accomplishes all the requirements. Nevertheless, an additional simulation was made considering the DB and the two inner cables. In addition the parasitic effect of the connectors was added to the simulation as a series resistance between cables, which maximum value is given by the manufacturer as $R_{CONMAX} = 60\ m\Omega$. The parasitic inductance can be calculated from the geometrical properties of the contacts, but as the height is $< 2\ mm$ its value is negligible compared with the cable inductance.

The simulation output can be seen on figure 6.5, as result of the circuit shown on figure 6.4. As shown, the signal has lost its perfect shape due to the effect of the parasitic elements in the cables and the connectors. Nevertheless the result is very good, as no reflections are visible, the pulse duration is the same and the gated integrator scheme we are using is not sensitive to the signal shape. Also the bias voltage drop is under 1 mV, so the cable electrical properties can be validated.

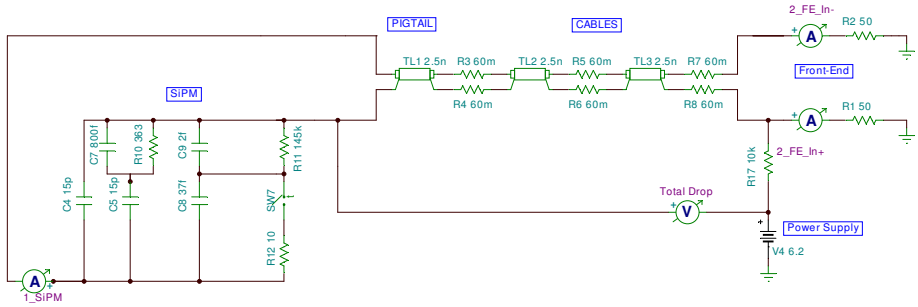


Figure 6.4: *Simulation circuit for the DICE-Board and two inner cables with the connectors contact resistance.*

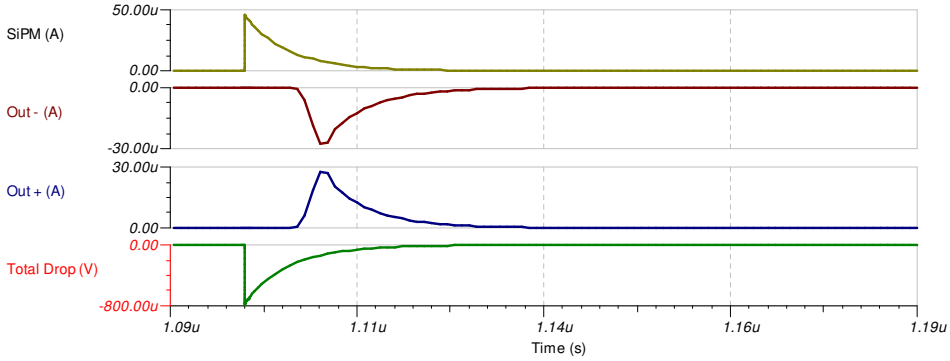


Figure 6.5: *Signal propagation simulation including the DICE-Board, two* 40 *cm inner cables, and the contact resistance of the connectors on all the transitions. From top to bottom the simulation shows: SiPM output, negative and positive cable outputs, and bias voltage drop.*

6.2 Outer Cables

For the outer cables selection, we had to compromise a solution between cost and performance, because we need to carry on almost two thousands signals each one with its own bias voltage along 4 meters.

On one hand, having custom cables with the same stackup than the DICE-Board, which would be perfect, is not an affordable solution due to the high cost. But on the other hand, there are not commercial cables that fit perfectly our specifications.

6.2.1 Cable specifications

Assuming that custom *Kapton* cables are not affordable for the detector scaling, the best option was a commercial cable design manufactured for the length we need. We found a company that produces custom ribbon cables with different connector options and custom length, *Parlex*, and the cable *PS2829AA4000S* seemed to fit mostly our requirements. It is not an expensive cable, and also has a very reasonable specifications that can work for us. According to the vendor, the selected ribbon cable has 51 flat wires with 0.5 *mm* pitch, embedded in flexible polyester substrate. This cables are 4 meters long, with surface mount connectors at the ends (part *DF9B-51S-1V* from *Hirose*). This connectors have low profile mounting, and are robust enough to guarantee the reliability of the connections. We knew that we would have an impedance mismatch between the inner and outer cables, but theoretically as the total pulse charge keeps constant it should not affect after the signal integration. However, we decided to give it a try, because we did not have other any easy alternatives.

We decided to use four cables per DICE-Board because that way we could assign the pinout for two bias wires surrounding the signal one, in order to reduce the noise coupling and the crosstalk between channels. And there were still remaining free wires for the LEDs and the temperature sensor. Later, as will be explained on the section 6.2.3, one of the bias wires will be used as guard, in order to reduce the crosstalk between channels.

On the figure 6.6 is shown the section of the cable for two channels, with three wires each.

As we did for the DICE-Board and the inner cable, we used a $2D$ field simulator in order to obtain the cable properties needed for simulation. The result corresponds to the configuration with one bias trace adjacent to the signal,

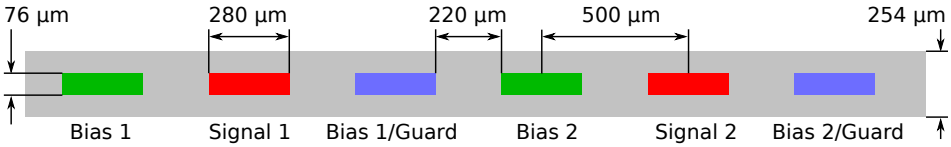


Figure 6.6: *Cross section and pinout of the external cable (two channels shown).*

and one guard trace between channels connected to ground as explained on figure 6.6.

- $R_{DC} = 20.57\ m\Omega/in$
- $C = 2.553\ pF/in$
- $L = 6.456\ nH/in$
- $Z_0 = 100.58\ \Omega$
- $T_d = 128.38\ ps/in$

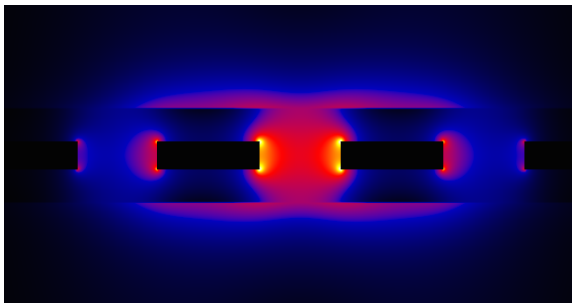


Figure 6.7: *Electric field between signal and bias wires simulation for the external cable.*

As the guard traces are connected to ground just at the front end side, for shielding purposes, the outer cables kept the differential transmission scheme. For this reason the electric field simulation showed on figure 6.7 and the line parameters obtained are the ones for the odd electric field, which corresponds to the differential transmission. As seen on the figure, this time the electric field is more scattered than the broadside coupled traces scheme, due to the geometry of the cable. The simulation shows four traces: the two externals are the guards connected to ground, and the two on the centers are the signal and bias traces. Still, most of the electric field is contained between the differential wires, but some also escapes even outside the cables. So that was a result to keep in mind.

With the parameters obtained the signal transmission simulation model was upgraded to include the outer cable and the remaining parasitic elements.

For the outer cable connectors the manufacturer specifies a maximum contact resistance of $R_{CONMAX} = 50\ m\Omega$, so were also included. Note that the contact resistance assumed for all the connections is the worst case scenario.

A feedthrough is placed between the inner and the outer cable, which due to its geometry (see section 6.3) has a non negligible parasitic inductance. This inductance can be calculated from the equation (5.9) which gives the via inductance as a function of its geometry. For the feedthrough, which has a total thickness of 6 mm and a via diameter of 0.5 mm, the parasitic inductance is $L_{FT} = 5.84\ nH$.

The last element to take into account is the adapter board, described on section 6.3.3. This board is necessary because the feedthrough size would be excessive if it had to hold all the connectors for the outer cables, or we would need a huge number of them. This way the feedthrough size can be moderate, and the adapter boards hold the huge number of connectors. As will be detailed on the proper section, the adapter board stackup is exactly the same than the DICE-Board and the inner cable, and its length is just 15 cm; so in order to simplify the simulation (there is a software limitation for the maximum transmission lines in the model) the parasitic components of the adapter board were added to the ones of the feedthrough, and its length to the inner cable. Thereby the resulting scheme for the complete tracking plane cabling is shown on figure 6.8.

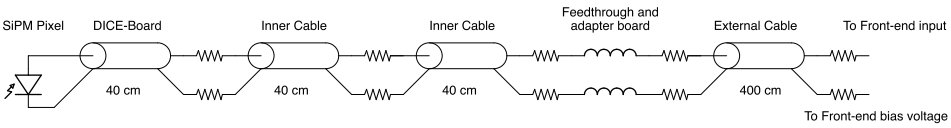


Figure 6.8: *Complete cable scheme with the parasitic effects of the connectors and feedthrough.*

Then the simulation for the cabling was done according to figure 6.9, which results are shown on figure 6.10. As expected, the impedance mismatch between the inner and outer cable produces reflections on the signal, but they did not seem to be terrible.

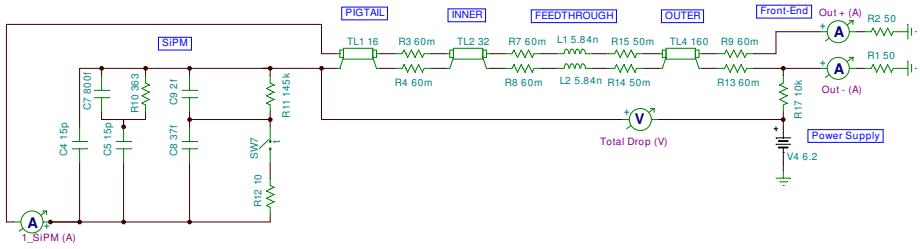


Figure 6.9: *Simulation circuit of the full cabling chain.*

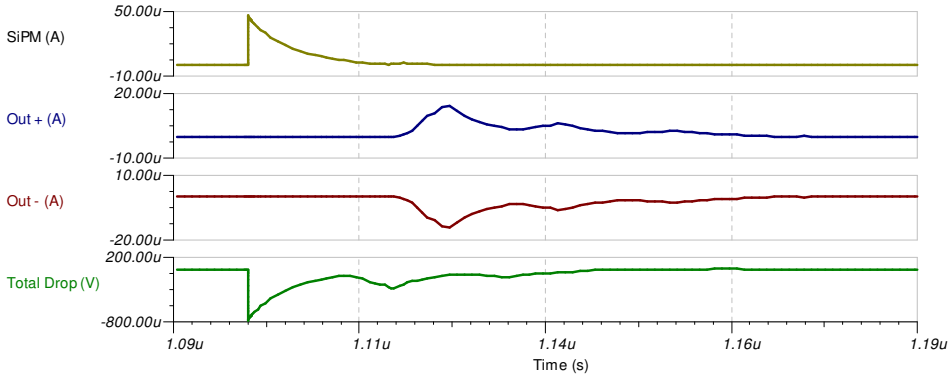


Figure 6.10: *Simulation of the full cabling chain, including the DICE-Board, two inner cables, the 4 m external cable and the parasitic components of the connectors, the feedthrough and the adapter board. From top to bottom the simulation shows: SiPM output, positive and negative cable outputs, and bias voltage drop.*

As can be seen the output signal has been also very stretched to $50 - 60\ ns$, due to all the parasitic elements on the cables and connectors. And finally, we saw that the bias voltage drop has a peak of $800\ \mu V$ and has also the same reflections than the signal.

Taking into account all these results we validated the external cable, at least theoretically, by now. So we decided to buy some units and connect them to the

prototype setup and see what was the real performance of all the elements once together.

6.2.2 Noise

The first test with all the cables connected to the electronics showed us that this setup is very sensitive to noise, because there is no shielding and the cable assignment is not symmetric. So looking directly at the cable ends, we were able to see lot of noise at different frequencies as is shown on figure 6.11:

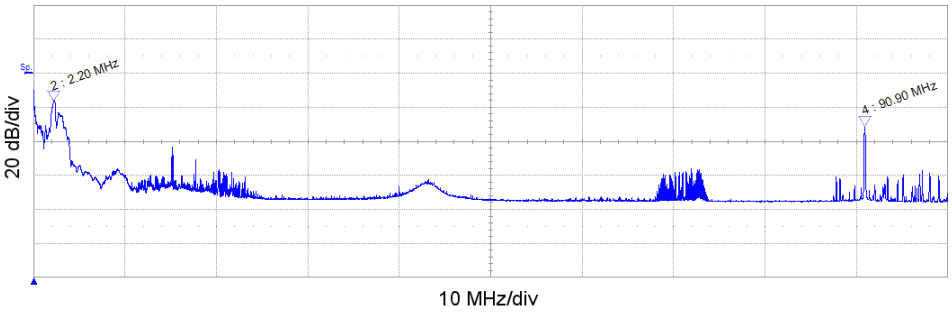


Figure 6.11: *Noise frequency spectrum with the 4 meter external cable at IFIC laboratory. Noise spectrum is slightly different at LSC.*

These frequencies can be classified in three different ranges:

- $2-3\ MHz$: Short bursts of $2-3\ \mu s$ length produced randomly (typically several microseconds between bursts).
- $9-75\ MHz$: Low amplitude noise due to TV, HF and VHF radio emissions.
- $90\ MHz$: A huge peak from the local radio station.

The goal we set for the noise was the capability to obtain the single photon spectrum of the SiPMs, in order to characterize easily the tracking plane. So for continuous noise, as the high frequency ones, its level should be under $1/3$ of the single photon amplitude; and for bursting noise just to be under the SPE height. This way, according to the numbers, the performance of the system would be as desired.

At this point we decided to consider the experimental bandwidth of the system, as the theoretical estimations may differ from the real setup once all the elements and parasitic effects join the game. The experimental bandwidth measured of the first amplifier stage in the front-end was about 20 MHz, therefore the 90 MHz frequency is attenuated and has small amplitude. Also the VHF signals are not important, for the same reason; and they have lower amplitude and the integration reduces them also. But the $2-3$ MHz bursts are a huge source of noise, because they are amplified on the same scale as the signal. Just at the front-end input this kind of noise has a measured amplitude up to 500 mV_{pp} on the initial configuration test, which will become a 8 V_{pp} signal after the first amplification stage. So this made it impossible to distinguish the SiPM signals from the burst noise, and it must be removed from the system.

The first thing to look at was the individual signal of each wire, because as the front-end scheme is differential, all the common noise should be removed. For the first approach on the external cable we used one wire for the anode and the two surrounding wires for the bias/cathode, thinking that way we will shield the signal. But we were wrong. Here we saw that the bias voltage had more noise amplitude, because it had two wires connected while only one was connected to the signal input. So the first change was to disconnect one of the bias wires. Then the noise amplitude became quite similar in both wires, and therefore was also reduced at the front-end output from volts to hundreds of millivolts.

At this point we could not ignore the fact that we needed a proper shielding, because cables that long are good antennas. We chose a 1 mm aperture tube mesh, with its maximum noise attenuation at 1 MHz, quite close to the frequencies we want to avoid. So the cable can be completely inside the shielding and just the connectors at the ends came out. As the main noise source we saw was the capacitive coupled, the best performance of the shield is connecting it to the analog ground just on one of the ends. If the connection were made at both ends of the cable, we would need to connect the vessel ground to the front-end, and this scheme had bad performance in the past, as seen on NEXT-DEMO. Also the connection at both ends would cause ground loops, increasing the noise level on the analog ground and risking the correct front-end behavior. The best analog ground available is the one at the front-end, so we connected just here

the mesh. This shielding decreased the noise under one hundred millivolts at the first stage output. Great improvement.

Still looking at the noise symmetry in the differential pair, we realized that on the first differential front-end scheme first stage had the same impedance in both branches for current signals, but not for voltage signals as R_{28} was not initially placed[1]. So the current noise is removed while the voltage one is not. That means the inductively coupled noise, which produces voltage noise, is not the same at the operational inputs and therefore is not subtracted. Then the next step was to balance the differential input of the front-end adding a series resistor in the bias voltage wire. In the figure 6.12 scheme the added resistor is numbered as R_{28}.

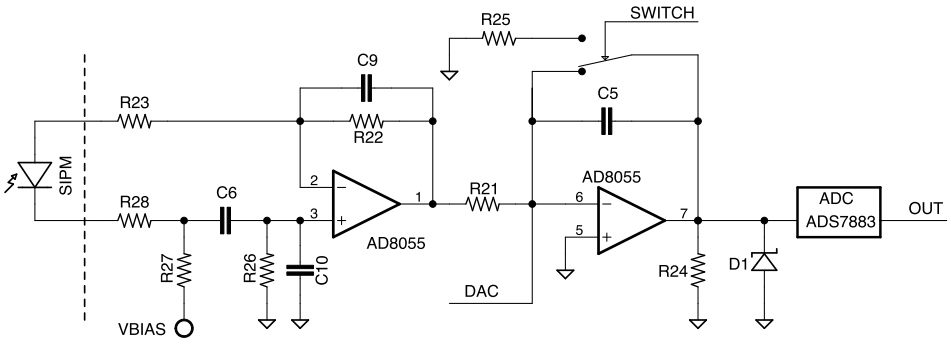


Figure 6.12: *Resistor R_{28} added to balance the voltage noise*

Thereby we reduced the noise to 40 mV at the integrator output.

Still looking at the input, it is easy to see that the gain on the first stage is very different for voltage and for current signals. As explained previously and as can be obtained from the front-end scheme the gain for a differential current signal, which are the ones given by the SiPMs, at the first stage output is:

$$V_{OUT} = -I_{IN}\,(R_{22} + R_{26}) \tag{6.1}$$

[1]On the first design R_{28} was not placed on the circuit, which was a mistake quickly solved. R_{23} was initially placed just for protection purposes, but as soon as we started to measure the noise we realized the importance of both input resistors.

But for differential or common voltage signals, which are produced by the inductively coupled noise, the gain depends also on the two input resistors:

$$Differential \longrightarrow V_{OUT} = -V_{IN}\left[\frac{R_{22}}{R_{23}} + \frac{R_{28}}{R_{26}+R_{28}}\left(1+\frac{R_{22}}{R_{23}}\right)\right] \tag{6.2}$$

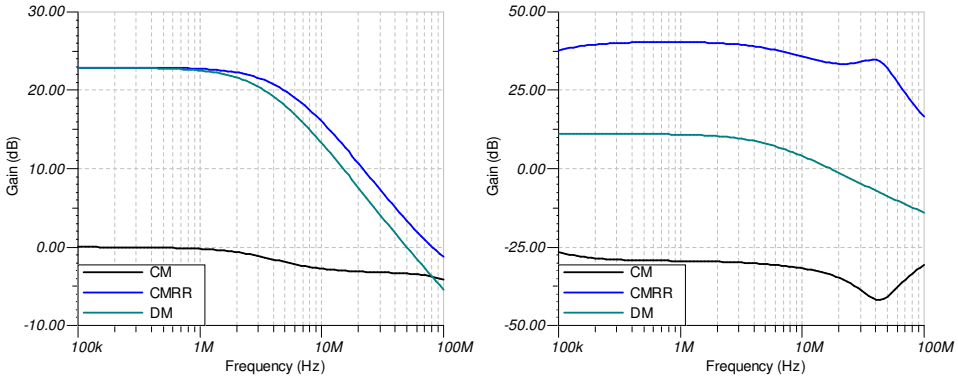
$$Common \longrightarrow V_{OUT} = -V_{IN}\left[\frac{R_{22}}{R_{23}} - \frac{R_{26}}{R_{26}+R_{28}}\left(1+\frac{R_{22}}{R_{23}}\right)\right] \tag{6.3}$$

In both cases, in order to reduce the output voltage the input resistors (R_{23} and R_{28}) must be increased, as they are in the equation denominator. But increasing the input resistors causes also a stretching in the signal, which has been already shaped by the cables capacitance, and adds another impedance mismatching point where the signal would produce reflections.

Over again, we compromised a solution of noise reduction and signal integrity. As the integrating time is 1 μs, we fixed as limit this value for the signal maximum width. This way we are still sure that the signal produced by a SiPM pixel is acquired, in the worst case, in two samples. First by simulations, and checked later with the prototype, we fixed the optimal input resistors of 390 Ω, as showed previously on the noise analysis (section 3.4). This modification reduced the noise to 12 mV, which was already below the single photoelectron level, and keeps the SiPM signal width between $600 - 800$ ns.

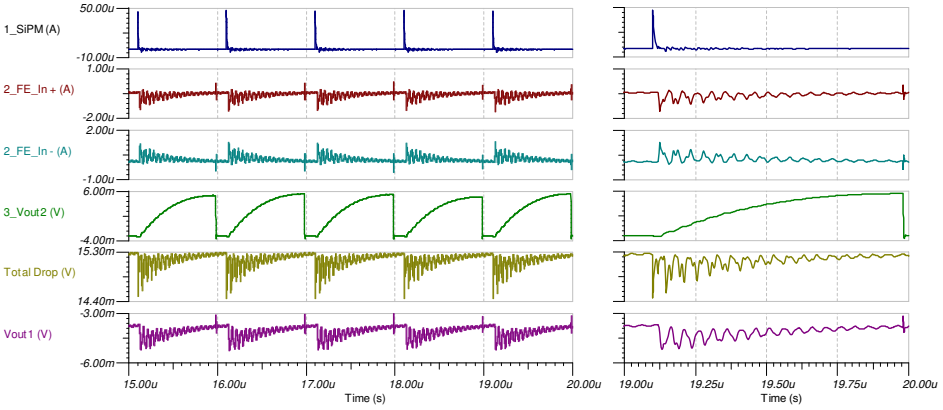
In the figure 6.13 there is a comparison of the first stage CMRR for voltage signals, which is the response affected by this modification. As can be seen, both differential and common gain have decreased. But the difference, which gives us the CMRR coefficient, has increased from 22 to ~ 37 dB; and also the bandwidth of this response has been extended from 2 MHz up to 30 MHz.

The simulation shown on figure 6.14 present the result of the full chain, from the SiPM to the front-end output. It includes also all the parasitic elements seen on figure 6.8, so the result is as similar to the reality as possible, but also the worst case scenario as we used the maximum contact resistance value.



(a) *Before* **(b)** *After*

Figure 6.13: *First stage CMRR comparison before and after the input resistor modification*



(a) *Simulation of* 5 μs *for the full chain.* **(b)** 1 μs *zoom for one cycle detail.*

Figure 6.14: *Full chain simulation from SiPM to front-end. From top to bottom the signals are: SiPM output, negative and positive front-end inputs, stage 2 output (after integration), bias voltage drop, and stage 1 output (before integration).*

As can be seen the signals have been stretched a lot, but still under the 1 μs limit, and they suffer several reflections. Nevertheless after the integration the output is very clean and achieve the proposed goals.

One important thing to take into account at this point is the final gain of the electronics. At this point, prior to the final front-end cards production, the radiopurity measurements showed that the *Hamamatsu* SiPMs had a huge radioactivity that made impossible to use them in the final detector; but fortunately the *SensL* SiPMs were clean enough for NEW (see table 5.1 on page 141). For this reason the electronics gain was adjusted to the *SensL* SiPMs gain, which is four times bigger than the *Hamamatsu* ones. And that's the reason why the simulation output shows an amplitude of $\sim 5\ mV$, because it still used the *Hamamatsu* SiPM model and once we use the new SiPMs the output will be also multiplied by four.

Finally the explained modifications were applied to the electronic prototype, and the performance was successfully checked on the scope and we were able to obtain the single photon spectrum of the silicon photomultiplier.

6.2.3 Crosstalk

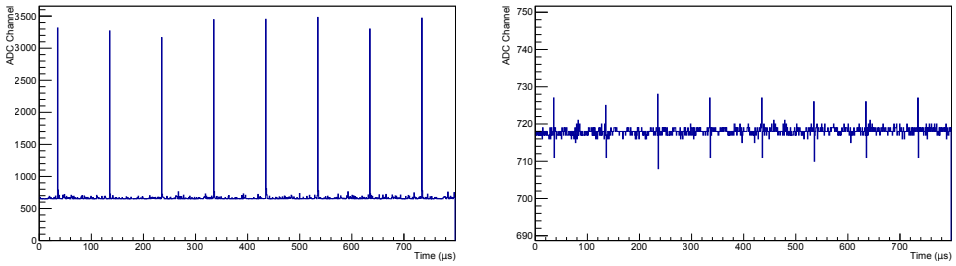
Once the noise problem was solved, we focused on the crosstalk between channels. The first step was to check the crosstalk levels with the current configuration, and then evaluate the possible improvements that can be done.

For this test two adjacent channels were connected to the front-end prototype, and the scope inputs were plugged to the first stage outputs. Only one of this channels has a SiPM, while the other remains unconnected. This way, triggering the SiPM with narrow and intense LED pulses we can evaluate the crosstalk level on the neighbor channel.

The first results showed us that for a signal of 1.5 V on the SiPM channel, a small pulse of 120 mV can be seen on the disconnected one. This means the current crosstalk level is about 8%, and should be reduced.

The main tool that we have for the crosstalk reduction is the unconnected bias wire, which became a guard wire for each channel. Just connecting this wire to the analog ground on the front-end, we allow it to shunt the radiated noise of each channel to ground. This way the measured crosstalk was reduced to 0.9%, which is a very reasonable performance.

In addition, we connected the full front-end prototype to the acquisition system to verify this results, obtaining the data showed on the figure 6.15.



(a) *Channel with SiPM illuminated* **(b)** *Neighbor channel (unconnected)*

Figure 6.15: *External 4 meter cable crosstalk test results.*

As can be seen the crosstalk level is even better, about 0.4% in the worst case; or 0.8% assuming two neighbors surrounding a non-illuminated channel. That means a SiPM channel on saturation causes a signal on the neighbor channel still smaller than a single photoelectron pulse, which can be hardly improved.

As shown before on figure 6.7 (the electric field simulation after connecting the guard to analog ground), the electric field is mainly confined to the gap between the wires, and a bit of it escapes outside the cable. But the guards do not allow it to cross to the neighbor pair.

The performance improvement compared with the previous test is probably due to the scope and the probes used, which adds sensitive points where the signal can be coupled to the adjacent channel. And also the waveform noise seen with the DAQ was quite smaller than the measured previously with the scope.

6.3 Custom Feedthrough

Taking into account that every SiPM has its own bias voltage wire, there are about 3600 electrical connections that must be passed from the inner volume of the pressure vessel to outside. That means we need very high density feedthroughs so we can extract the SiPM signals from the tracking plane, without affecting them significantly.

The main problem is that high density feedthroughs for high pressure are not very common, and the ones that are available do not fit our requirements or are extremely expensive. For that reason we developed our own high-pressure, high-density feedthrough.

6.3.1 FR4 PCB feedthrough prototype

The main idea of this feedthrough is using a multilayer PCB directly as a separation barrier between the pressurized xenon and the external air, taking advantage of the good mechanical characteristics of the FR4 to hold the pressure. The board stackup is designed with 3 copper layers and blind vias (drills) misaligned, so there is not a direct path for a gas leak (figure 6.16). In order to increase the reliability of this design, the vias will be filled with vacuum epoxy.

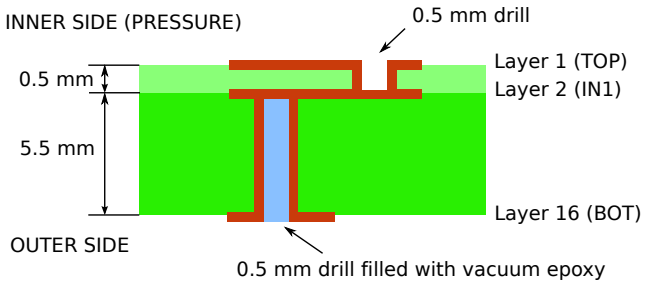


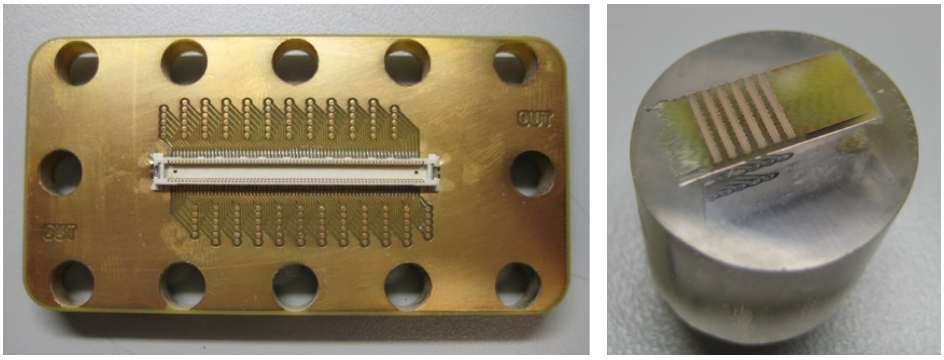
Figure 6.16: *Cross section of the PCB feedthrough stackup.*

We developed a small prototype that has one connector on each side and allows to take the signals of one full DICE-Board. It is designed with the same connector as the inner cables, so it can be directly connected to the DICE-Board pigtail.

The 6 *mm* thickness of the design will hold more than 20 *bar* of pressure, since standard FR4-class PCB materials have very good mechanical characteristics. In case we modify the design for a larger size, some stainless steel reinforcements would be enough. This feedthrough is quite cheap, because the materials and

procedures used are standard on PCB production, while the only complicated parameter is the board thickness.

The small prototype shown in figure 6.17a was produced and tested. Also a cut section can be seen in figure 6.17b, with the detail of the epoxy filled vias.



(a) *Board produced with the connector already assembled.* **(b)** *Cross section of the PCB.*

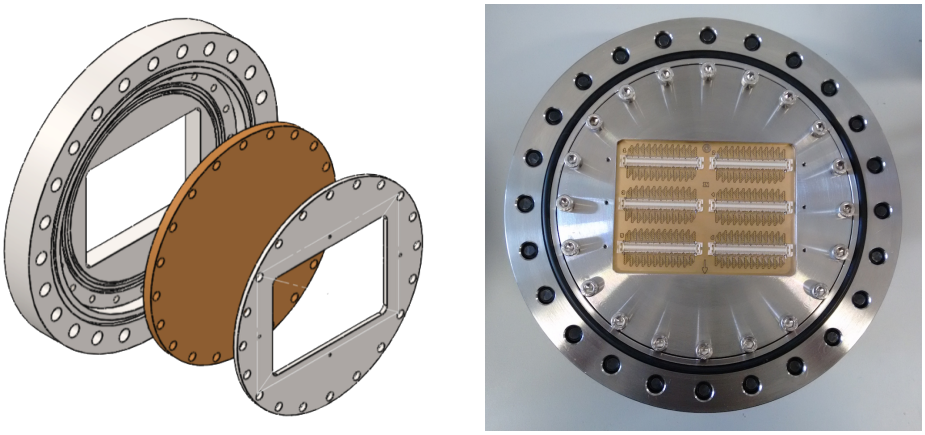
Figure 6.17: *FR4 PCB feedthrough produced prototype.*

The prototype was tested electrically and mechanically. It was connected to the electronics prototype setup, and the data showed no difference between before and after the feedthrough connection. However, as explained on page 152, the parasitic inductance introduced by the feedthrough was taken into account in the full chain simulations, as it may affect the signal integrity in a long transmission line.

Then, using Ar at 20 *bar* pressure we measured a leak rate of $\sim 10^{-2}$ $nmol/s$. The designed leak rate for NEW is < 10 $g/year \longrightarrow 2.3$ $nmol/s$ for Xe; so the feedthrough is two orders of magnitude below the limit. Also, as the Ar molecule is smaller than Xe, the feedthrough leak rate should be even lower for Xe.

6.3.2 NEW FR4 PCB Feedthrough

For NEW the feedthrough design includes 6 connectors for DICE-Boards, with the same PCB stackup than the prototype. To make easier the sealing with the flange and in order to hold more pressure, the new feedthroughs are round shaped and also a stainless steel reinforcement plate is added at the back side, as shown on the figure 6.18a. Thereby now the feedthrough can hold up to 25 *bar* by design, even though this one is much larger.



(a) *Feedthrough design (flange, FR4 PCB, and reinforcement plate).*

(b) *6 DB feedthrough produced.*

Figure 6.18: *FR4 PCB feedthrough design for NEW.*

For the sealing between the flange and the pipe we are using an elastomer gasket, but in the future it will be replaced by a metal gasket. The flange union with the PCB has a double elastomer gasket, which is butyl rubber o-rings. Between the two o-rings there is a small hole connected to a 1/4" port, through which vacuum will be made and monitored via the RGA in order to detect leaks.

As it is shown in figure 6.19 we have designed a multi-port adapter for the vessel. This way we can place the 5 feedthroughs required for NEW, and also replace them if necessary. It has also two additional ports, one for gas emergency evacuation and other one as spare.

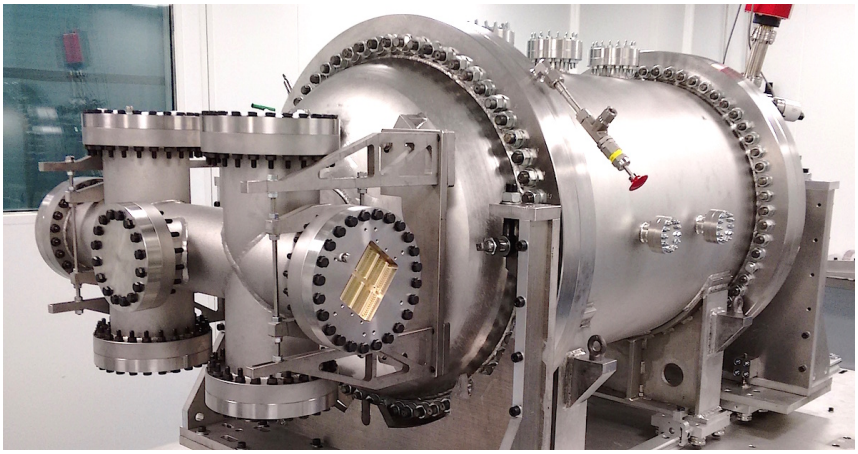


Figure 6.19: *Multi-port adapter for the tracking plane (the "spaceship").*

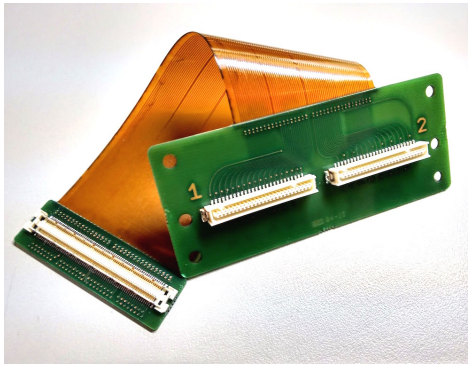
This feedthrough was also tested, same way than the prototype. The electronic test showed no surprises as the electrical connections are identical than last time. About the mechanical tests, it was tested under Ar at 20 *bar* and the measures showed a leak rate of $\sim 2 \times 10^{-3}$ $nmol/s$, five times smaller than the prototype due to the double o-ring. That means the feedthrough leak rate is three orders of magnitude better than the limit for NEW and NEXT-100.

6.3.3 Adapter Boards

As has been commented on previous sections, the tracking plane cabling was a huge challenge with lots of issues to solve. Together with the feedthrough design, we realized that it was not obvious to connect everything with each other. On the inner side we had one 140-pin cable per DICE-Board, and outside there were four 51-pin cables which weight was not despicable. A feedthrough able to hold the external cable connectors will need a larger size, or to be split in more units. This would complicate the system too much, so the smartest solution came with the addition of the adapter boards.

The concept of the adapter board is as easy as it sounds: a board to adapt the feedthrough output connectors to the external cables. A few designs later

working together with the mechanical engineers, and after the feedback of some manufacturing companies we came to the design shown on figure 6.20.



(a) *Adapter board, a combination of kapton and FR4 stackup.*

(b) *Six adapter boards are placed around one feedthrough with hexagonal distribution.*

Figure 6.20: *Adapter boards during installation on November 2015.*

This design was created in parallel with the feedthrough, so the adapter board can be considered as a part of it. As shown, the adapter board is a *Kapton* based PCB with the same stackup than the DICE-Board, and embedded between FR4 where the connectors are located: one 140-pin connector for the feedthrough and four 51-pin connectors for the external cables.

As can be seen on figure 6.20b six adapter boards are placed in hexagonal distribution around each feedthrough, using a plastic structure created with the 3D printer. Thereby we have created a robust structure which protects the feedthrough surface and can hold the external cables without problems.

The adapter board first batch was tested, including it in the whole chain test setup we had at IFIC. As the adapter board stackup is the same than the DICE-Board and the connectors were also tested in the past, we expected good results. This setup, for the first time, included all the elements: the DICE-Board, two inner cables, one feedthrough, the adapter board, four external cables and a front-end card. The data obtained showed an amazing performance of the system, which encouraged us for the final assembly in NEW.

6.4 SiPM & Cabling connection test ("Check System")

As has been explained in previous sections, the NEW tracking plane cabling is quite complex and has a huge number of connections that are potential failure points for the SiPMs signals. In the past, for NEXT-DEMO, the tracking plane installation became very tedious when we had to check every SiPM connection one by one using a multimeter and tons of patience. We wasted a lot of time doing this repetitive work, over and over again. For this reason on an earlier design stage of NEW we decided to create an automated system, which help us to check the continuity of the cables and connections.

The device designed is based on an *Arduino Mega* microcontroller, some modular boards with the required electronics, a battery and a touchscreen; all enclosed in a box as shown in figure 6.21a.

(a) *Check system box. All the connectors are placed on the side for easy connection.*

(b) *Programmable touchscreen to interact with the device. Picture shows a successful DICE-Board test.*

Figure 6.21: *Check system.*

The main board has the proper connectors for the other elements to plug in, distributes the power, and has $4 \times 16 : 1$ analog multiplexers and 8 I2C 40-bit I/O port expansions; which provides the system with a total of 64 analog I/O and 320 digital I/O.

Then the external board connected using PCI-E sockets includes a set of connectors that matches the ones in the DICE-Board, inner cables, feedthroughs and outer cables. That allows to perform several tests depending on the cables connected and the test selected; so it can check the full chain connection, inner or outer cables continuity, feedthrough connections and even the adapter boards.

Depending on the option selected via the touchscreen the system proceeds with the required set of tests, which includes:

- **SiPM detection:** Using the analog I/O the SiPMs are directly polarized, and the voltage drop is measured and compared with the reference values. This way the system knows if a SiPM is present at the end of the line, and if it has been damaged.
- **Short circuit and continuity detection:** An algorithm writes digital signals on some wires ad reads on other ones sequentially, so the continuity of the traces is checked and short circuits are detected.
- **NTC reading:** The system includes a subcircuit for the NTC reading, so if a reasonable value is read the NTC is considered as properly connected.
- **LED test:** The lines of the LEDs are also checked, and they are illuminated sequentially to see if they work.

This system allowed us to save a huge amount of time, because during the tracking plane installation we could check the connections of a whole DICE-Board in a few seconds, and be sure that everything will work as expected.

It was also used during the feedthroughs and adapter boards soldering process, which was made by hand, thereby short circuits or disconnections were easily identified and repaired.

6.5 Protection against ESD

As has been explained on Chapter 4, protective diodes were placed on every front-end input, because dealing with the field cage high voltage may be very dangerous for low voltage electronics. These are TSV (Transient Voltage Suppressor) based ESD protection diode arrays, typically used for consumer electronics where the human body ESD may damage the devices; and were chosen due to the similarity between a field cage spark and an electrostatic discharge: several kilovolts and fast discharges.

But once the detector was fully working we detected some issues on the electronics related with field cage sparks. Sometimes the data acquisition stopped working, a front-end FPGA was not sending data, or even a SiPM bias supply lost its internal DAC calibration. Then we understood that a proper understanding of the safety ground connections was needed, as we knew the sparks were not affecting the signal lines while were affecting the whole electronics system.

Figure 6.22 shows the initial safety ground scheme done by the laboratory personnel, and also the later modifications we did trying to enhance the electronics behavior against sparks.

As can be seen, the initial ground scheme was not suitable from an electronics point of view, because the only connection from the high voltage modules to ground was made by the NEW vessel which is mounted on the platform, and also the electronics cabinets were connected directly to the detector's seismic platform. This caused that a spark event derived to the vessel ground was easily propagated to the electronic ground, which affect some sensitive devices, like the FPGAs, and made the system unstable.

The modifications shown on figure 6.22 forced the electronic's ground to pass through the main NEXT electrical panel; so the safety ground scheme now is "star" topology like, instead of a linear one. Now, in case of spark in the vessel, the discharge has less impact on the electronics.

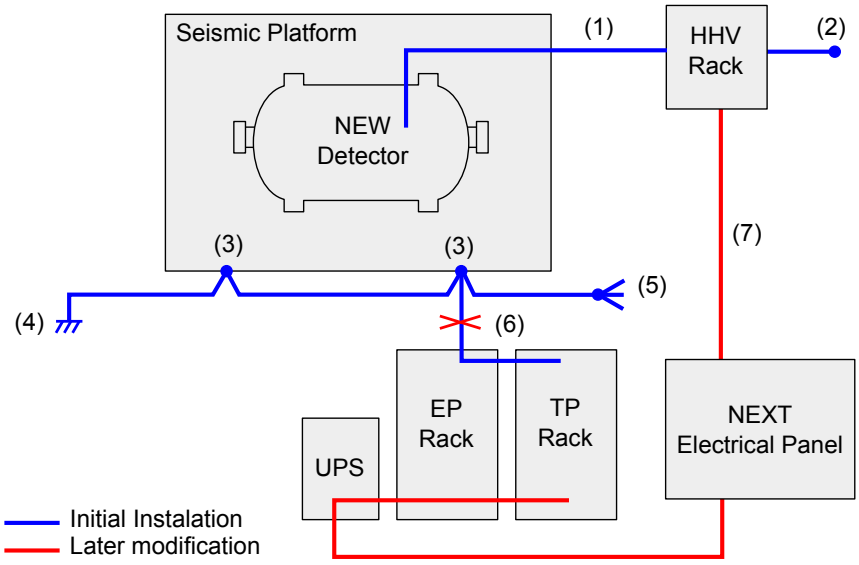


Figure 6.22: *Safety ground connection scheme, original shown in blue and later modifications shown in red. (1) Coaxial shield connects HV ground to vessel. (2) HV rack originally connected to a floating tray. (3) Nut-bolt to the seismic pedestal. (4) Earth connection from LSC (not NEXT electrical panel. (5) GND fanout prepared for compressor. (6) EP and TP racks were connected to the seismic platform. Later this connection was replaced by a new one passing trough the UPS to the main NEXT electrical panel. (7) HV ground redirected to the NEXT electrical panel.*

After this modifications no more problems related with the sparks have been detected in the tracking plane front-ends, but some still occur on the bias supplies. For this reason we thought to introduce ferrite cores on the SiPM external cables, as we expected to attenuate the common mode noise theoretically produced by the sparks. Fortunately this was previously tested on the test setup, using a high voltage "sparker" and three different types of ferrites from different manufacturers. And here we found that this modification was negligible for the spark effects on the signal, so it was not applied to the electronics at LSC.

Right now a close look up of the sparks effects is being done, so all the information collected can be used on the future *FEB64v3* design, and also for the SiPM bias source revision expected for NEXT-100.

"Despair, or folly? It is not despair, for despair is only for those who see the end beyond all doubt. We do not. It is wisdom to recognize necessity, when all other courses have been weighed, though as folly it may appear to those who cling to false hope. Well, let folly be our cloak, a veil before the eyes of the Enemy!"

"¿Desesperación, o locura? No desesperación, pues sólo desesperan aquellos que ven el fin más allá de toda duda. Nosotros no. Es sabiduría reconocer la necesidad, cuando todos los otros cursos ya han sido considerados, aunque pueda parecer locura a aquellos que se atan a falsas esperanzas. Bueno, ¡que la locura sea nuestro manto, un velo en los ojos del Enemigo!"

– Gandalf (The Fellowship of the Ring)

7

Programmable Power Supply with SiPM gain stabilization

Silicon Photomultipliers (SIPMs) are replacing PMTs in a growing number of high-energy, nuclear and medical physics applications where the reduced cost and size, small operating voltage, mechanical robustness and insensitivity to magnetic fields, overcome a number of drawbacks (like higher noise, reduced active area and higher temperature dependence).

One key element in the use of this technology is the power supply. SiPMs from different vendors require bias voltages ranging from 20 V to 90 V and the type of application will imply current demands ranging from microampers to milliampers. Good output load regulation will ensure a uniform response in the dynamic range, while temperature compensation is a must in applications that

require high gain stability or are subject to temperature variations. Temperature compensation, being device specific, usually requires some sort or adjustment or configurability. Multiple-output capability (as well as remote monitoring and control) is desirable in applications with large SiPM arrays, as the ones in the NEXT Experiment detectors.

Due to the lack of alternatives in the market, NEXT has been working in its own bias supply since the beginning. For the NEXT-DEMO prototype a first power supply was designed, to cover the basic needs of the first SiPM tracking plane. This first device was based on an Arduino microcontroller, and was capable of providing bias voltage up to 24 groups of SiPMs (as explained on section 2.2 the first tracking plane had 19 "daughter" boards). Few iterations later and ready for the NEW detector, the result is an autonomous and very versatile device which can provide the required bias voltage and ensure the gain stability to hundreds of SiPMs, while keeps a very moderate size [Querol et al. 2016].

7.1 Requirements for NEW and NEXT-100

In terms of integration, the power supply must be 3U-rackable, as the front end boards are 3U Eurocard form factor. Remote monitoring and control via ethernet is a must, in order to integrate the power supply in the experiment's *LabVIEW*-based Slow Control system. Multiple outputs are required (16 is considered a good factor) to reduce the overall power supplies volume. Due to the already existing low-voltage power supplies' characteristics, the SiPM power supply must accept $\pm 12\ V$ as input voltages.

In terms of bias voltage output, a $0 - 85\ V$ is required to accommodate both *Hamamatsu* and *SensL* devices. Voltage resolution must be better than $5\ mV$ for accurate gain stabilization with temperature, according to the manufacturers data provided. Output current per channel up to only a few μA is required (a result from calibration tests on the 64 SiPMs in a *Kapton* carrier with the expected illumination in the experiments), though the source actually has good load regulation up to $5\ mA$.

As proposed goal, gain stability with temperature in the SiPM must be better than 1% in a 10 $^{\circ}C$ range, even thought the underground laboratory is kept at a constant temperature of $21 - 22$ $^{\circ}C$.

On the NEW detector the bias voltage for the SiPMs is fed through the same cables used for the signals via the front end. Also the two terminals of the temperature sensor placed on each DICE-Board are also available through the front-end, so the bias supply must be able to read it for the desired performance. Three 16-channel external power supply units feed the bias voltages to the 28 front-end boards and read out the temperature sensors using a 4-pin *LEMO* connector.

7.2 Design

Taking into account all the requirements defined, a 5-channel prototype was developed to test the circuit performance, and also to start developing the user interface and the remote communication. Once the prototype was validated, the real challenge started and the 16-channel power supply was designed.

7.2.1 Temperature Compensation

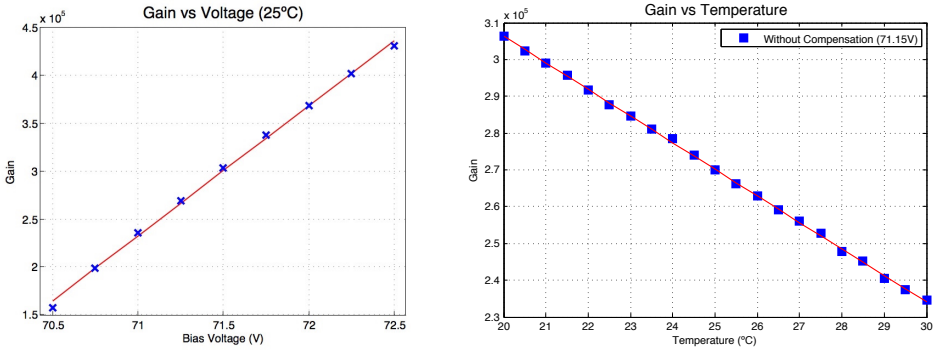
As explained on section 1.6, SiPMs are avalanche photodiodes operated in Geiger mode, reverse biased at a small overvoltage (V_{ov}, typically $1.5 - 3.5$ V for *Hamamatsu* devices [Hamamatsu 2015] and $1 - 5$ V for *SensL* [SensL 2015]) beyond the breakdown voltage (V_{bk}). The gain (G) of the device is a linear function of the bias voltage, $V_{bias} = V_{bk} + V_{ov}$. As V_{bk} has a relatively large variation with temperature (its temperature coefficient is typically $20 - 70$ $mV/^{\circ}C$), the device gain changes $1 - 10\%/^{\circ}C$. Consequently, some sort of compensation (that results in adjusting V_{bias} when temperature changes) is required for most applications. This adjustment allows a real time gain stabilization, which simplifies a lot the data processing as offline correction due to temperature is not needed.

A survey of different temperature compensation techniques is presented in [Shukla et al. 2014]. Some techniques are based on SiPM dark current control, which has a negative exponential relation with temperature at a given gain value. A thermistor (which has a negative exponential response too) is used in the bias circuit to compensate for the gain variation. However, these techniques are limited to low temperature and/or low intensity of light if high accuracy is sought, besides requiring changes in the thermistor circuit if the SiPM model is changed.

A more flexible and accurate family of methods are based on direct bias voltage control. Our group presented in 2011 [Gil et al. 2011] a direct bias voltage control method in which the output of a high-resolution DAC is connected to the control input of a high-voltage module in order to provide a compensated V_{bias}. A temperature sensor and characterization data for the SiPM are used to compute the DAC output in a microcontroller. Other works referenced in [Shukla et al. 2014] implemented later on similar approaches.

The power supply developed for the NEW detector inherits the temperature compensation from our previous work. In order to determine the V_{bias} required for a given temperature (T), two characteristic curves need to be measured and fitted to straight lines: $\partial G/\partial V$ and $\partial G/\partial T$, as illustrated on figure 7.1. The former allows to determine a and β_1 coefficients in the expression $G = a + \beta_1 \cdot V$, while the latter renders coefficients b and β_2 in the expression $G = b - \beta_2 \cdot T$ (showing a negative dependence of gain with T). The relation between a change in temperature ΔT and the required change in V_{bias} (ΔV) can be easily inferred as $\Delta V = -(\beta_2/\beta_1) \cdot \Delta T$. Finally, taking as a reference room temperature (25 $^\circ C$), the applied voltage is $V_{bias} = V_{bias\ 25^\circ C} + \Delta V$.

This way we ensure a stable gain during the data taking. Note that the precision is not as important as the stability, because a correction factor may be easily applied during the data processing. But it will be harder if a different time depending correction is needed for each DICE-Board.



(a) *Gain as a function of bias voltage.* **(b)** *Gain as a function of temperature.*

Figure 7.1: *Silicon photomultiplier gain dependence with bias voltage and temperature. Measurements for the* Hamamatsu S10362-11-025P *device.*

7.2.2 Output channel

Each of the 16 channels are based on the *LT3482* chip, a 90 V boost DC/DC converter with control input and current monitoring aimed at APD applications. It provides a direct current monitor signal (I_{mon} in figure 7.2, with a maximum error of 12 μA) to a low-noise ADC, which also digitizes the output voltage and the temperature sensor. To monitor the output voltage a very precise resistor divider is used, with 0.1% tolerance resistors. A *Raspberry Pi* module uses these data to compute the required correction in the bias voltage output, which is fed to the DC/DC converter's control input via a 16-bit DAC, closing the control loop. Both ADC and DAC are connected to the *Raspberry Pi* via a SPI bus. The resulting closed-loop control allows a precise SiPM gain stabilization, and the *LT3842* module includes a number of convenient features like overcurrent, overvoltage and overheat protection, as well as automatic power off.

For remote SiPM temperature sensing in the NEW detector a *Murata* NTC sensor is used, as described on section 5.3. In order to improve the sensor behavior, a second-grade polynomial is fitted in the range from 15 $°C$ to 35 $°C$. The results obtained with this method show a 0.06 $°C$ (1.32 mV) maximum fit error. With the SiPM *SensL MicroFC-10035-SMT-GP*, currently used in NEW, this corresponds to 0.037% maximum gain compensation error due to this fit. To avoid calibrating

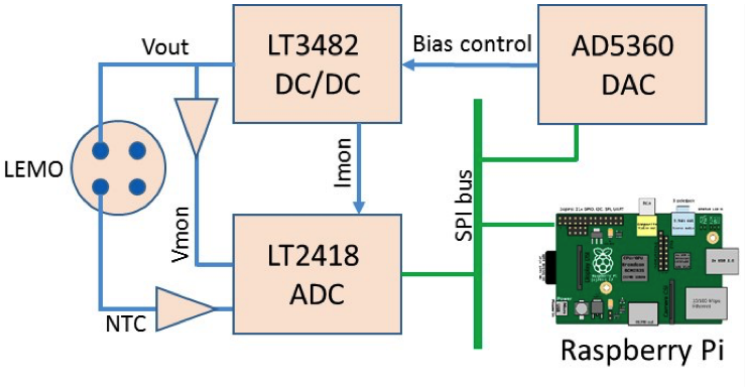


Figure 7.2: *Block diagram of one power supply channel.*

each NTC sensor in the tracking plane, the mean response of 30 NTC sensors was fitted, and the maximum error achieved is 0.259 $^{\circ}C$ (5.7 mV). This produces a 0.16% maximum gain compensation error due to the temperature sensing, quite below the limit sought.

7.2.3 I/O Interfaces

The front panel equips a 2.8" color touch screen (see figure 7.4a) from *4D Systems*, as main user control. A graphical user interface provides in-field monitoring and control of the source parameters, a convenient feature for stand-alone applications or for quick in-field troubleshooting.

A USB memory can be plugged on the rear USB connector (shown on figure 7.4b) to store the diary reports, measurements and channel configuration data; or the internal microSD card can be also used for this purpose. Also on the rear side all the 4-pin *LEMO* connectors are placed, as well as the power cable which provides ± 12 V. An ethernet interface allows remote monitoring control of the power supply using the SSH (Secure SHell) protocol, a cryptographic network protocol for operating network services securely.

A *LabVIEW* VI (Virtual Instrument) has been created as interface to the power supply from LabVIEW using SSH (figure 7.3). It is integrated in the NEXT

Slow Control net, and allows to easily supervise the tracking plane performance. The right side of the image shows the SiPM plane, where voltage, current and temperature for each 64 SiPM group is displayed. All the power supply variables can be monitored, and warnings are also showed and reported here.

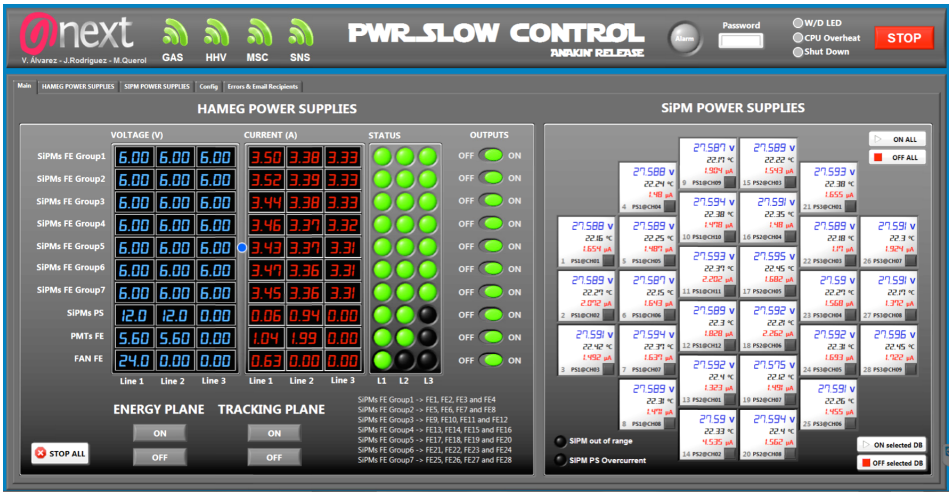


Figure 7.3: *PWR Slow Control designed for the NEW detector, which allows an easy monitoring and control of the power supplies.*

7.2.4 Mechanical Design

The electronics were carefully designed to fit inside a commercial 3U-12hp steel box, as shown on figure 7.4, which acts also as electromagnetic shielding. A total of 3 electronic cards are placed inside; one to provide the required supply and to interconnect the different elements, and two 8-channel boards with the DC/DC converters and the remaining devices. Also the *Raspberry Pi* and the touchscreen are placed inside, so every millimeter is used.

The small size design provides a compact solution fully compatible with the NEW tracking plane readout, which consists of 28 groups of 64 SiPMs (making a total of 1792 SiPMs). A 19" 3U crate accommodates a programmable power supply and 12 front-end boards (see figure 7.5). As a result, the whole tracking plane is read-out with three 3U crates like this one.

(a) *Front view of the bias source, where the touchscreen is placed.*

(b) *Back side of the device. Output connectors are placed here, together with the USB and ethernet interfaces.*

Figure 7.4: *Finished power supply for silicon photomultipliers in a 3U sized case.*

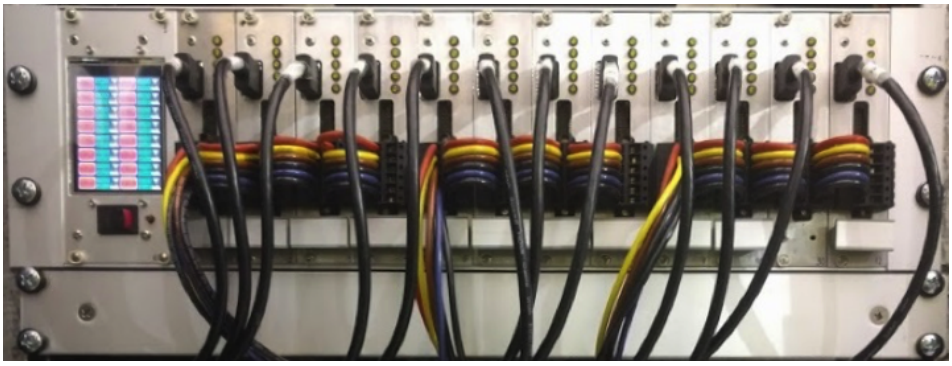


Figure 7.5: *19" 3U crate with one power supply providing the required bias to 12 front-ends, a total of 768 SiPMs. A fan is placed below the crate for the required electronics cooling.*

7.3 Results and Outlook

A *Lecroy WaveRunner HRO 64zi* oscilloscope (12-bit vertical resolution, set to infinite persistence, AC coupling, 1 $M\Omega$ input impedance) has been used to

measure output voltage stability in a 2-hour interval. Stability was measured better than 2 mV_P, measuring difference between desired and actual output voltage. Output voltage resolution, after calibration, is better than 1 mV in the full range. Other relevant specifications are summarized below:

- Maximum output voltage of 85 V
- Power consumption between 5 W (typical) and 29 W (max)
- Controlled rise and fall slopes
- Self-calibration algorithm

In the NEW detector, one power supply channel provides the bias voltage to 64 SiPMs. Sensors for each group have been selected for minimum parameter dispersion, and the temperature compensation feedback was adjusted to the mean of the group. Figure 7.6 shows the first results of the SiPM power supply and the NEW tracking plane on April 2016. As can be seen on the left plot the gain variation with temperature has been reduced just to less than 0.5% in a 10 $^{\circ}C$ range, tested in a temperature controlled black box. Right plot shows that the single photon spectrum is clear enough to perform the SiPM calibration using the dark count events, with data already taken from the NEW detector.

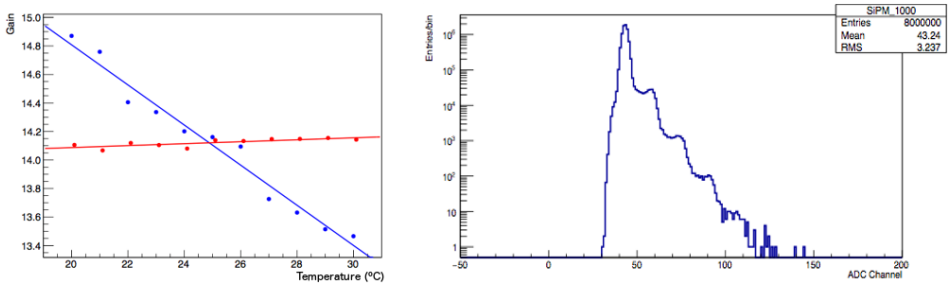


Figure 7.6: *Performance results of the SiPM bias supply designed for NEXT. Left plot shows the gain dependence as a function of temperature before (blue) and after (red) the temperature compensation. Right figure shows a SiPM photon spectrum taken from the NEW detector.*

This is a solution for SiPM bias supply with temperature compensation without introducing additional complexity to the bias circuit, which may be interesting

for applications with high density of SiPM or other applications where there are space or heating constraints and active circuits with operational amplifiers are not desirable. The device produced provides gain stability for the SiPMs in the NEW detector of 0.5% in the operation range, with output voltage stability better than 2 mV_P. Three power supplies are being used in the NEW detector since spring 2016, whose tracking plane is made by $\sim$ 1800 SiPMs, and they allowed a full sensor calibration ready for the data taking. As the design is fully scalable together with the front-end electronics a new batch will be built for the NEXT-100 detector, containing $\sim$ 8000 SiPMs.

"I do not think there is any thrill that can go through the human heart like that felt by the inventor as he sees some creation of the brain unfolding to success... such emotions make a man forget food, sleep, friends, love, everything."

– Nikola Tesla

"The most exciting phrase to hear in science, the one that heralds new discoveries, is not 'Eureka!' but 'That's funny...'"

– Isaac Asimov

8

First Results of NEW Tracking Plane

After some years of hard work and a roller coaster of emotions, the tracking plane was fully functional and working on November 2016. And for the first time NEW was completed with all the elements properly working: gas system, energy and tracking plane, field cage, electronics and acquisition, and slow control. As every detector on development phase, the first thing to do is to calibrate it in order to understand its true potential and capabilities; first the sensors by themselves, and then using radioactive sources.

8.1 NEW Tracking Plane Calibration

As very preliminary result, after "the zener issue" described on section 4.5, the first gain calibration of the tracking plane was performed on November 2016. This measurement has been done using the silicon photomultiplier dark count, and also using one of the pulsed LEDs located at the energy plane, close to each PMT. Figure 8.1 shows an example of the photon spectrum obtained for a single SiPM, with the both methods introduced.

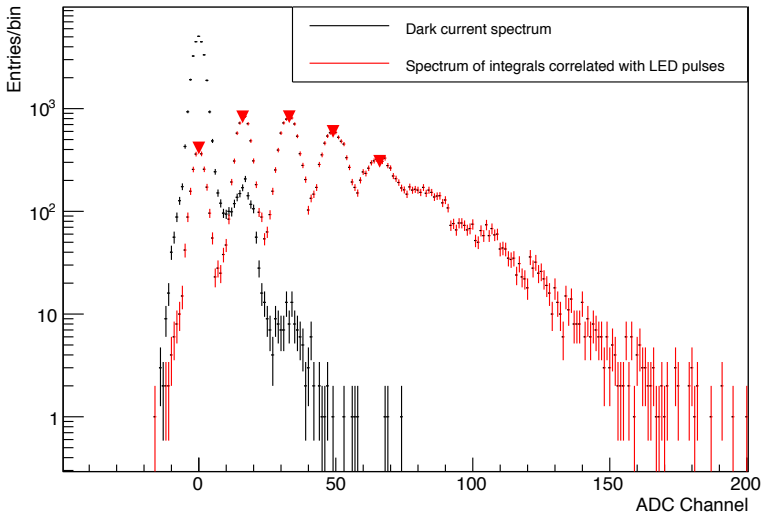


Figure 8.1: *Single Photon Spectrum (SPS) of a single SiPM obtained with dark count (black) and pulsed LED (red).*

As can be seen the calibration using just dark count events is not easy, due to the low dark count rate of the *SensL* silicon photomultipliers (which is something desired, indeed). But adjusting carefully the LED light emission the SPS can be obtained, which allows to accurately calculate the SiPM gain. As explained, the SiPMs are grouped in the DICE-Boards according to their gain to minimize the spread, but also the physical device performance and the electronic components tolerances affect the final value, so this step must be done.

Using this method the single photon gain has been obtained for the whole tracking plane, 1792 silicon photomultipliers, giving as a result the gain distribution showed on figure 8.2.

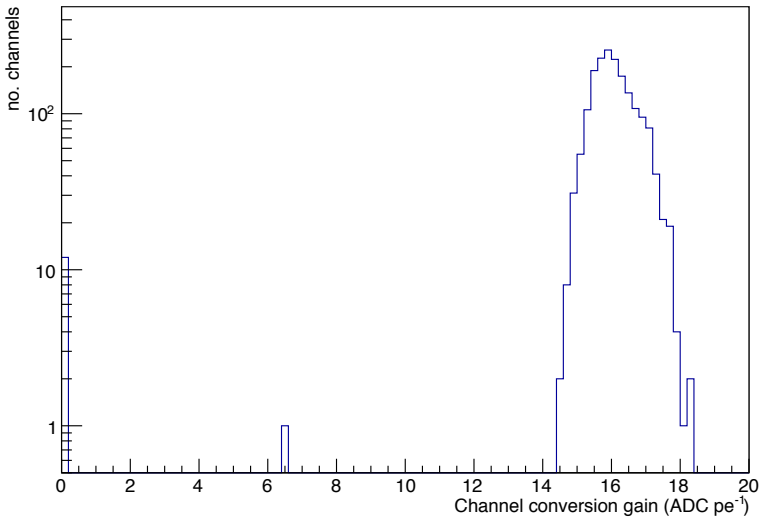


Figure 8.2: *Gain distribution of all the SiPMs placed on the NEW tracking plane.*

As shown the gain spread is very small, and centered in the expected value of $\sim 16\ ADC_{counts}/pe$. But some SiPMs show no gain or a value not expected. This are the so called "dead" channels; most of them identified during production and soldering, and placed out the light tube were they are negligible (as explained on previous chapters, the DICE-boards over cover the light tube, so a few SiPMs are not used for tracking reconstruction).

Just one "dead" SiPM has been identified on the tracking plane center, as shown on figure 8.3. This one and also the group on the upper right area were identified as improper cable connections, and were fixed for later runs.

Using the data taken with the pulsed LED we were also able to know the amount of light seen by each SiPM, to deeply understand the tracking plane homogeneity. Figure 8.4 shows the average light seen by each SiPM, measured in photoelectrons.

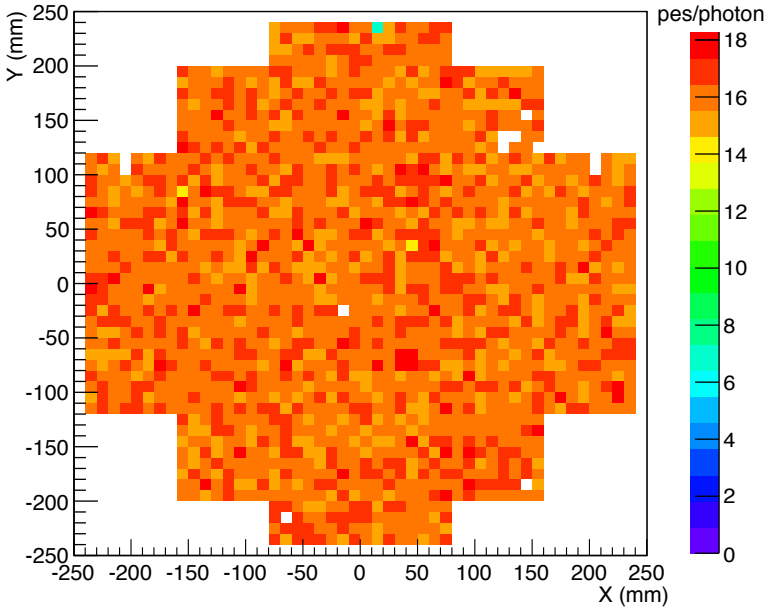


Figure 8.3: *XY gain map of the NEW tracking plane SiPMs.*

As can be seen, the round light tube is clearly recognizable. Even the light attenuation on the borders, as some SiPMs are half covered by the mesh frame. This plot also allowed to verify the SiPM mapping, as a wrong pattern will demonstrate the opposite.

This first calibration was very encouraging. We managed to have a functional pixel tracking plane, working as expected and ready to see whatever happens inside the NEW detector.

8.2 First run with ^{22}Na

For the first run we used a ^{22}Na source, placed on the lateral port of the detector. The radioactive sources are an extended method for calibration, as they allow to understand the response of the detector at a known energy deposition.

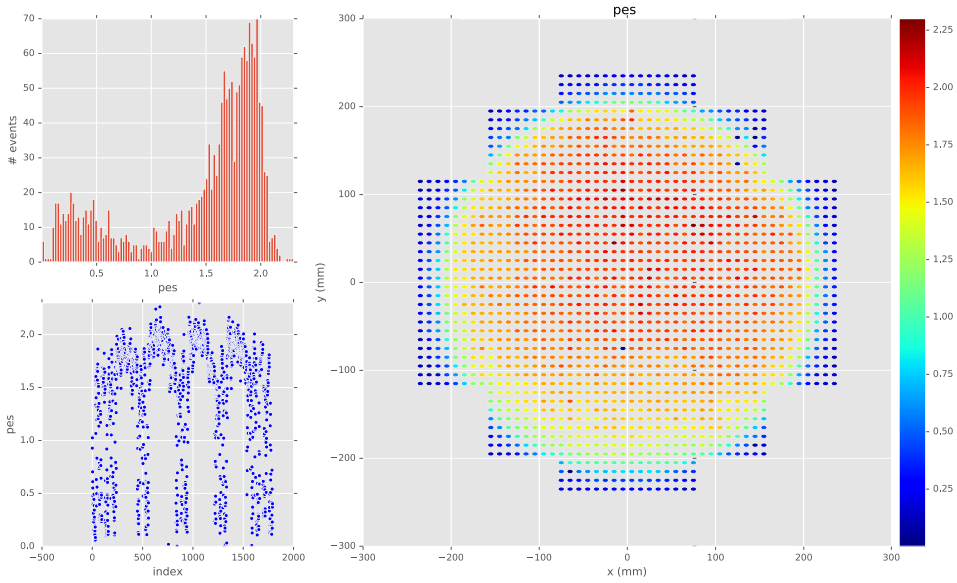
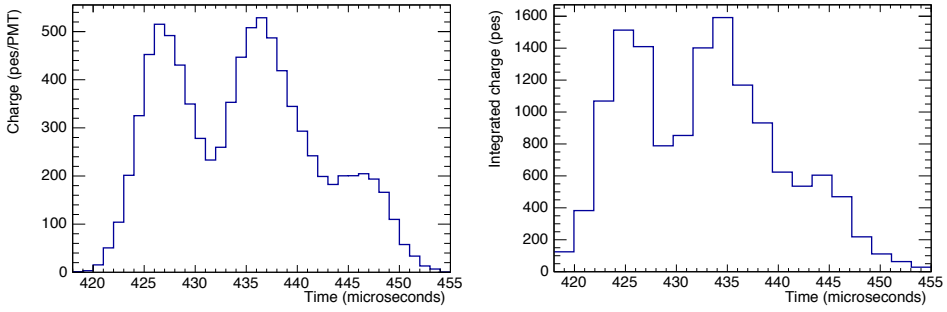


Figure 8.4: *LED calibration data of the tracking plane. Plot shows the average light seen by each SiPM, measured in photoelectrons.*

Figure 8.5 shows the waveform comparison between the energy plane and the tracking plane for the same sodium event. As can be seen, the shape is the same for both detection planes, even though the silicon photomultipliers collect less light than the PMTs due to each sensor active area.



(a) *Waveform seen at energy plane (mean of the 12 PMTs) for a ^{22}Na event.*

(b) *Waveform seen at tracking plane (sum of all SiPMs after the noise cut applied at 99%) for a ^{22}Na event.*

Figure 8.5: *Waveform comparison between energy and tracking plane for the same ^{22}Na event.*

From the same event, figure 8.6 shows a single slice of the signal seen by the tracking plane. As can be seen the light collected is mostly located in a few SiPMs around the coordinates (-100, 0), while the rest just see some photons due to the light dispersion

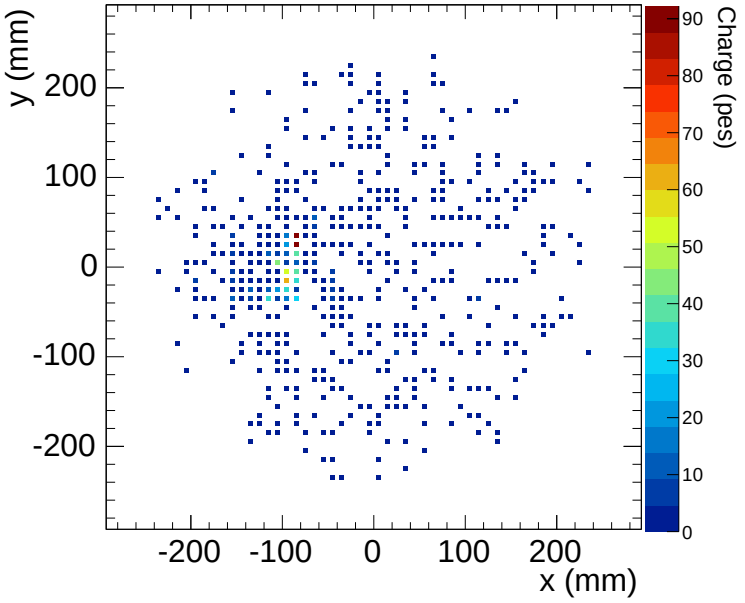


Figure 8.6: *Single X-Y slice (1µs) of a sodium event after the noise cut applied at 99% of noise distribution for each SiPM.*

Figure 8.7 shows the location of several events seen by the tracking plane in the same sodium run, calculated as the charge barycenter of all the SiPMs that see at least the 50% of the light seen by the most illuminated SiPM. The events are more usual on the left side of the detector, as that is the place where the radioactive source is located. In this figure the round section of the light tube is clearly seen, as the SiPMs outside it are not seeing light.

Finally, removing the background noise of the SiPMs not seeing light, we were able to see a sodium track. Figure 8.8 shows the axis projections of the first track reconstructed on NEW, and figure 8.9 is the 3D representation of that track. The

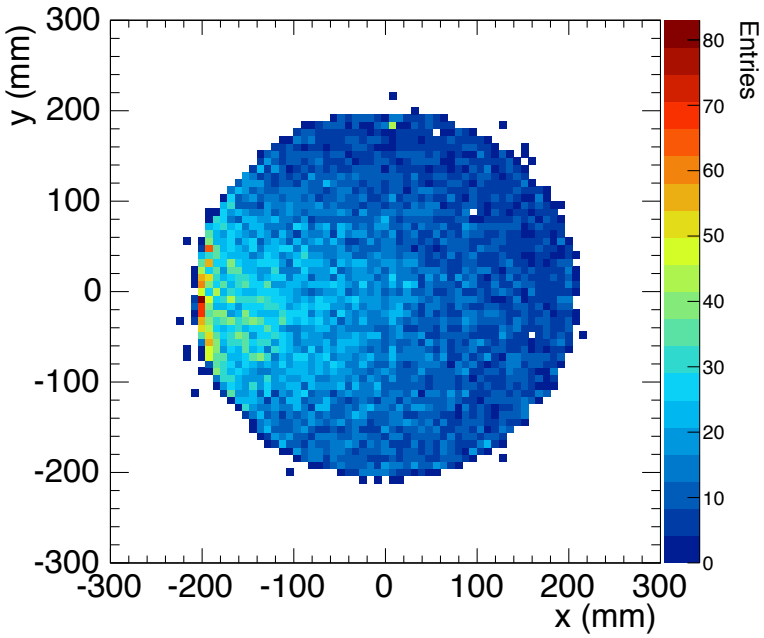


Figure 8.7: *X-Y position reconstruction of several ^{22}Na events, using the charge barycenter. Events are located mainly close to the lateral port where the radioactive source is placed.*

reconstruction clearly shows the electron path, and the high energy deposition blob at the end. This is a very small track, less than 100 *mm*, but demonstrates the truly capabilities of the tracking plane and, even more important, demonstrates that everything is working.

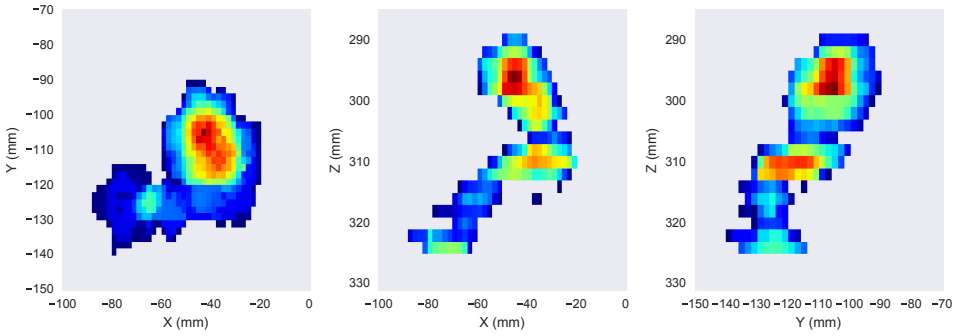


Figure 8.8: *Axis projections of the first ^{22}Na track reconstructed in NEW.*

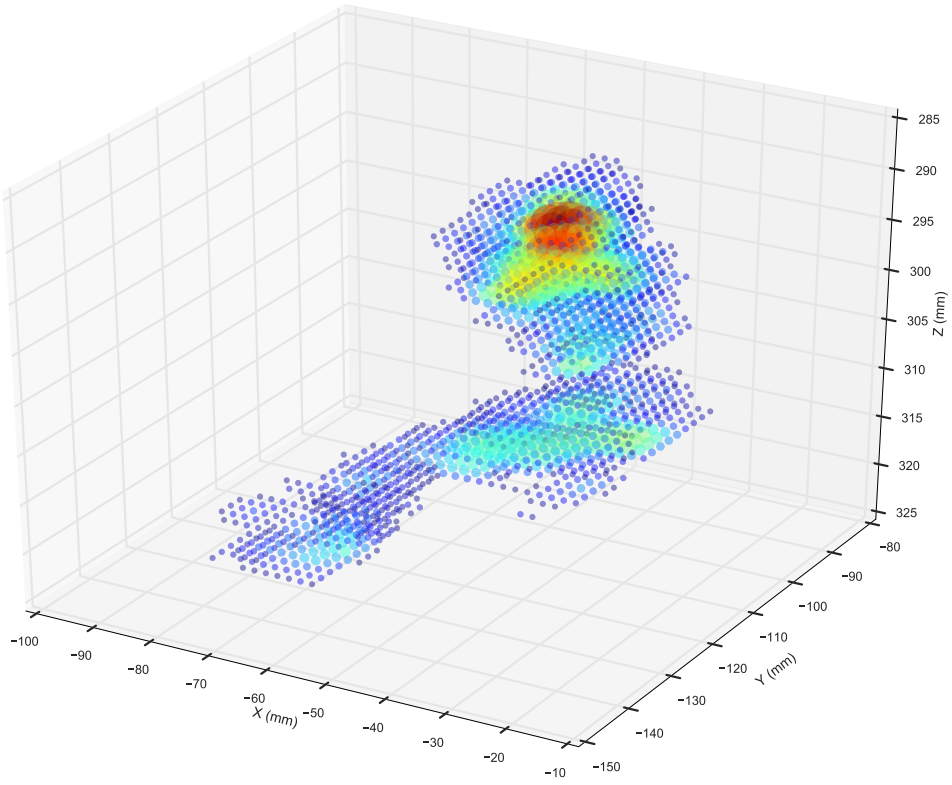


Figure 8.9: *3D reconstruction of the first ^{22}Na track.*

"Creativity is intelligence having fun."

– Albert Einstein

9 Conclusions

The objectives defined for this thesis were focused on the study, design, production and installation of the electronics involved in the NEXT experiment tracking plane. As has been explained, all the studies and developments done during this period have been applied to the NEW detector, and are though to be scalable for the next step: the NEXT-100 detector. Seen on detail, the initial objectives versus the corresponding work developed and results achieved are:

- Study of the SiPM properties for different SiPM models and manufacturers, like gain dependence with bias voltage and temperature, dark count and noise.

  This study was done by the student together with some NEXT collaborators, and the results obtained were used for the selection of the

final devices used and for the better understanding of the electronics needed. For this purpose the student built a small setup, able to precisely control and measure the temperature and bias voltage of the devices, while pulsed with a blue LED. Some of these results appear implicitly along the text, even that finally the decisive factor for the election was the radioactive contribution of the material.

- Design and production of a SiPM bias supply scalable for NEXT-100.

  This is the main topic of Chapter 7. As explained, the SiPM power supply has been a reiterative work line in NEXT. The first SiPM power supply was the result of the student's Master Thesis on Electronic Engineering, and laid the groundwork for further developments. This was the first time this scheme was used to supply photodetectors, based on a 4-device feedback loop (microcontroller - DAC - DC/DC Converter - ADC), and was presented on the IEEE - NSS/MIC (Nuclear Science Symposium and Medical Imaging Conference) on 2011 [Gil et al. 2011]. Some time later this scheme has been also used by other companies, like *Hamamatsu*, which meant that we were on the right path.

  Two years later, the new power supply was designed and produced as a new Master Thesis done by another NEXT collaborator, this time under the academic direction of the student. The resulting power supply provided a compact solution for the SiPM biasing and their gain stabilization, and its integration with the NEXT slow control net made possible to automate them while the safe operation is guaranteed. Still at production date there was no commercially available any device that could achieve that number of channels at that size and cost. This device resulted in an article published on 2016 [Querol et al. 2016], and has been also used by the medical physics group at IFIC.

- Design and production of a front-end for the NEXT experiment silicon photomultipliers, fitting all the performance required.

  A meticulous study of the current solutions for SiPMs readout was performed, focusing on the ASICs used by other physics experiments.

But none of the existing electronics fit our requirements, so a custom solution was needed. Then, as detailed on Chapters 3 and 4, a thorough design has been developed and successfully tested, based on discrete electronic components. The performance of the front-end developed fulfill all the requirements wanted, like single photon resolution, good signal to noise ratio (to allow gain calibration via dark count spectrum) and stable performance. This front-end was the main topic on an article published on 2015 [Rodríguez et al. 2015], and has allowed NEXT to be the first experiment running with a SiPM pixel tracking plane that large. A minor revision is foreseen prior to the NEXT-100 installation; as some characteristics might be improved mainly focused on robustness.

- Design, production and installation of the SiPM carrier boards.

  As described on Chapter 5 this boards, called DICE-Boards, were carefully designed by the student and some versions were produced until the optimum performance was achieved. The requirements of low radioactivity made impossible to place any connector on the detector's active volume, so a specific solution was needed to solve this issue. The solution came as an all-in-one circuit which included both the SiPMs and a cable that passes through the inner copper shielding, where the connectors will not be problem. This boards were manufactured using the most precise technology available — and affordable — at that moment, as the micrometer tolerances in a 40 cm all-flexible board are not easy to achieve. The NEXT Collaboration is very proud of the solution given by this boards, both for radiopurity and electronic performance. The design will be reused for NEXT-100, and the concept will be brought to other experiments using SiPMs, like the PETALO prototype intended for medical physics application.

- Study of the NEXT experiment ground system.

  Unfortunately the tight schedule did not allowed the student to perform this study, which was an important issue to solve once all the electronics and high voltage modules were installed.

But the experiment development lead to other needs not planed or thought to be carried by other people; so some of them were done by the student during the period of this thesis:

- Tracking Plane Feedthrough.

  As described on section 6.3, NEXT developed a custom high-density pressure-tight feedthrough to solve the problem of taking out all the tracking plane signals. There were no commercially available feedthroughs that satisfy our channel density and pressure tightness requirements, so a new approach was needed. The FR4 feedthrough concept was taken from another prototype made by some members of the NEXT collaboration; so the student proposed to adapt it to a custom design, improved for a larger number of contacts and lower leak rate. This design was created by the student with the help of the mechanical engineers, as includes both electronic and mechanical challenges. After several tests it has proved very good performance results for signal transmission and gas tightness, as the leak rate measured is several orders of magnitude below the allowed limit.

- Slow Control.

  The Slow Control was intended to be developed by an external group but, due to the good performance achieved by the early software designed by the NEXT electronics group, the final decision was to keep this path and develop the full system at home. For this reason the student, as part of the electronics group at IFIC, made an important contribution to the software development. Right now the NEXT Slow Control is a self-contained control system able to make decisions based on the data provided by the net of sensors distributed over the full system. Every single device is controlled and monitored via the Slow Control, composed by four computers and a FPGA-based PLC, and just the more sensitive parts related to the gas system are left to be operated by the users.

But nothing is perfect, and some mistakes have been done along the years of work. One of these mistakes can be found on the front-end electronics. Even with the changes made for the second board revision, the noise measured in the

top row of analog channels is higher than the other ones. This is known to be due to the switched mode voltage regulator, as this is the place where the power lines are routed, and it is pending to be solved.

Another issue encountered during the tracking plane installation was the inner cables connector's robustness. These connectors are thought to be used on board-to-board connections, not on "hanging" cables. For this reason on the mockup assembly we realized that some connections were failing, as some connectors were partially disconnected. We designed a 3D printed clamps as emergency solution, which have been working properly on NEW up today, but clearly this is an issue to be solved for NEXT-100.

Right now NEW is proudly taking data and teaching us how to improve the detector. All the experience gained will be used in future design and construction of NEXT-100, which will start immediately. For this bigger detector some subsystems will be easily reused o scaled up, like the gas system or the lead castle. But almost all the remaining subsystems need a proper upgrade to be adapted to the new requirements. For instance the tracking plane, which is the main topic in this thesis, will be about four times larger than the one in NEW. Even if the DICE-Boards used are exactly the same, there are other pending issues: as said, the front-end electronics will suffer a minor revision to fix the small issues found during NEW installation; the inner cabling can not be directly scaled up from NEW, as the performance/length ratio is not linear for the current scheme; and even the feedthroughs may need a revision due to the inner cabling dependence.

So lot of work is still pending before NEXT-100 can replace NEW, but this time the groundwork is more solid than ever thanks to the know-how learned during this period of hard work.

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List of Acronyms

$\beta\beta$	Double beta decay
$\beta\beta0\nu$	Neutrinoless double beta decay
$\beta\beta2\nu$	Two neutrino double beta decay
ADC	Analog to Digital Converter
APD	Avalanche PhotoDiode
ASIC	Application-Specific Integrated Circuit
ATCA	Advanced Telecommunications Computing Architecture
BLR	BaseLine Restorer
CF	ConFlat
CMOS	Complementary Metal-Oxide-Semiconductor
CNF	Common Noise Filtering
DAC	Digital to Analog Converter
DAQ	Data Acquisition
DB	Dice Board
DCR	Dark Count Rate
DTCC	Data, Trigger, Clock and Control

EL	Electroluminescence
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistor
FFC	Flexible Flat Cable
FPC	Flexible Printed Circuit
FEB	Front-End Board
FEB64	Front-End Board 64-channels
FEC	Front-End Concentrator
FPGA	Field Programmable Gate Array
FWHM	Full Width Half Maximum
GDC	Global Data Concentrator
GDMS	Glow Discharge Mass Spectrometry
HDPE	High Density Polyethylene
I2C	Inter-Integrated Circuit
ICPMS	Inductively Coupled Plasma Mass Spectrometry
ITO	Indium-Tin Oxide
I/O	Input/Output
KDB	Kapton Dice Board
LCP	Liquid Crystal Polymer
LDC	Local Data Concentrator
LNGS	Laboratori Nazionali del Gran Sasso
LSC	Laboratorio Subterráneo de Canfranc
LVDS	Low Voltage Differential Signaling

MIP	Minimum Ionizing Particle
NEW	NExt White
NEXT	Neutrino Experiment with a Xenon TPC
NEXT-DBDM	NEXT-Double Beta, Dark Matter
NEXT-DEMO	NEXT-DEMOnstrator
OPA	OPerational Amplifier
PCB	Printed Circuit Board
PE	Photo-Electron
PET	Positron Emission Tomography
PLC	Programmable Logic Controller
PMT	PhotoMultiplier Tube
PTFE	Polytetrafluoroethylene
SC	Slow Control
SFTP	Screened Fully-shielded Twisted Pair
SiPM	Silicon PhotoMultiplier
SM	Standard Model
SMT	Surface-Mount Technology
SOFT	Separated, Optimized Functions TPC
SPI	Serial Peripheral Interface
SPICE	Simulation Program with Integrated Circuit Emphasis
SRS	Scalable Redout System
SSH	Secure SHell
TIE	Twin Ion Engine

TPB	TetraPhenyl Butadiene
TPC	Time Projection Chamber
TSV	Transient Voltage Suppressor
TTL	Transistor-Transistor Logic
UHMWPE	Ultra-High-Molecular-Weight Polyethylene
VUV	Vacuum UltraViolet

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"I tried so hard
and got so far,
but in the end
it doesn't even matter.
I had to fall
to lose it all,
but in the end
it doesn't even matter."