University of BRISTOL

Front-end Low Noise Amplifier

Design and Build

Héctor M. Pellicer Grau

Supervised by Dr. Paul Warr

April 2017

Final year project thesis submitted in support of the degree of

Bachelor of Engineering in Electrical and Electronic Engineering

Department of Electrical & Electronic Engineering

University of Bristol

THIS PAGE INTENTIONALLY LEFT BLANK

DECLARATION AND DISCLAIMER

Unless otherwise acknowledged, the content of this thesis is the original work of the author. None of the work in this thesis has been submitted by the author in support of an application for another degree or qualification at this or any other university or institute of learning.

The views in this document are those of the author and do not in any way represent those of the University.

The author confirms that the printed copy and electronic version of this thesis are identical.

Signed:

Dated:

THIS PAGE INTENTIONALLY LEFT BLANK

Abstract

In this project we will manage to design and build a Low-Noise Amplifier (LNA) in discrete format that will operate around 125MHz. The purpose of a LNA is to amplify a very low-power signal without adding too much noise to the surrounding frequencies, in other words, to avoid degrading its signal-to-noise ratio (SNR). To achieve this, we will use a junction field effect transistor (JFET) as the core device instead of the popular bipolar junction transistor (BJT). In comparison with BJTs, JFETs have a much lower sensitivity to changes in the applied signal, are more temperature stable, are usually smaller and are relatively less noisy because of its internal structure.

For the design process, we will start proposing some schematic drafts based on theoretical concepts, then putting them together into a single schematic and simulating it with the software *LTSpice*. Input and output biasing and matching are an important part of the design. We will carefully select appropriate real components with its spice models, which will later be ordered from our preferred components provider.

Once design and simulation is done, we will proceed to build our system physically into a stripboard dealing with all the unexpected factors that exist in the real world, such as parasitic capacitances and inductances, component tolerances, RF interferences, device limitations and other kind of inconveniences that will pop up during the job. Taking them into account and making some necessary adjustments to the initial design, and with the help of an oscilloscope and a vector network analyser (VNA), we will try to test the system and compare its performance with the previous simulation outputs.

THIS PAGE INTENTIONALLY LEFT BLANK

Table of Contents

1. Introduction

Mobile phones, GPS receivers, hospital instrumentation, satellite communication systems, high fidelity audio players, wireless data transfers… all of them have something in common. All of them can be found everyday dealing with signals, interferences, noise… What makes them so good at fighting against signal obfuscation? They make use of a system which is called Low-Noise Amplifier (LNA). The purpose of a LNA is to amplify a very low-power signal without adding too much noise to the surrounding frequencies, in other words, to avoid degrading its signal-to-noise ratio (SNR).

The aim of this project is the design and build of a Low-Noise Amplifier in discrete format that will operate around 125MHz. It will have a low input impedance and a 50Ω output impedance. Other parameters as gain or noise figure will need to be optimized during the design process in order to get the best performance available. The core of the system will consist of a FET transconductance stage followed by a bipolar current buffer. It is expected to be built physically into a stripboard to be tested and compared with the simulation outputs.

2. Background

2.1. RF Noise

"Without noise, an RF receiver would be able to detect arbitrarily small inputs, allowing the communication across arbitrarily long distances." (Razavi, 2011)

Noise is, in RF terms, any undesired signal contributing to the deterioration of the response at the output of a system. Noise can be originated externally, for example by atmospheric phenomenon, temperature variations or interferences; or internally, by wires, connectors, antennas or active amplifiers; and it is random. By random we mean that its instantaneous value cannot be predicted.

For example, in a resistor connected to a battery and drawing a current, each electron experiences thermal agitation due to ambient temperature, making it follow a random path while, on the average, moving toward the opposite terminal of the battery. As a result, the average current remains constant despite of the instantaneous current shows random values. In this example, thermal noise is produced by thermal agitation. Thermal noise appears on any device presenting a determined resistivity and held at any temperature different from 0K.

2.2. Noise Temperature

"The noise temperature is a means for specifying noise in terms of an equivalent temperature. The equivalent noise temperature T_e is not the physical temperature of the system, but rather a theoretical construct that is an equivalent temperature that produces that amount of noise power." (Carr & Brown, 2001)

Noise Temperature is a way of expressing an amount of noise power introduced by a component or a source. Its spectral density is expressed in terms of the temperature (in Kelvins) that would produce that level of noise as follows:

$$P = k_B T B$$

Eq 1. Noise Power Spectral Density

Where:

- $\boldsymbol{P}$ is the power (in W)
- $\boldsymbol{k_B}$ is the Boltzmann constant ($1.38x10^{-23}$ J/K)
- $\boldsymbol{T}$ is the Noise Temperature (in K)
- $\boldsymbol{B}$ is the bandwidth (in Hz)

2.3. Noise Factor and Noise Figure

"For components such as resistors, the noise factor is the ratio of the noise produced by a real resistor to the simple thermal noise of an ideal resistor." (Carr & Brown, 2001)

The noise factor F_n of a system is the ratio of output noise power P_{no} to input noise power P_{ni}. The noise factor is always measured at the standard temperature (T_0) 290K:

$$F_n = \left.\frac{P_{no}}{P_{ni}}\right|_{T=290K}$$

Eq 2. Noise Factor of a system

The **Noise Figure** is the noise factor expressed in decibels:

$$NF = 10log(F_n)$$

Eq 3. Noise Figure

Where:

- $\boldsymbol{NF}$ is the Noise Figure (in dB)
- $\boldsymbol{F_n}$ is the Noise Factor

2.4. Low Noise Amplifiers

An RF amplifier is an active network that increases the level of low power signals. Unfortunately, amplifiers add distortion and noise to the original signal. The purpose of a Low Noise Amplifier (LNA) is to boost the signal without adding too much noise to the surrounding frequencies, in other words, to avoid degrading its signal-to-noise ratio (SNR). LNAs play a critical role in the overall

performance of a design: by placing a LNA close to the signal source, the noise created by the device itself is injected directly into the received signal, while the signal gain created by the LNA reduces the effect of noise from posterior stages of the receive chain in the system.

"The noise figure is a frequently used measure of an amplifier's goodness. Thus it is a figure of merit." (Carr & Brown, 2001)

A good LNA has a low NF and enough gain to amplify the signal. A typical LNA may supply a power gain between 20 and 30 dB while decreasing the SNR of the signal less than 2-3dB.

3. Description of the project

In this project we will manage to design, build and measure a Low-Noise Amplifier in discrete format that will operate around 125MHz. It will have a low input impedance and a 50Ω output impedance. Other parameters as gain or noise figure will need to be optimized during the design process in order to get the best performance available. The core of the device will consist of a FET transconductance stage followed by a bipolar current buffer. The signal source will have an output impedance of 50Ω and provide a 1-3mV amplitude signal at 125MHz. The AC load will be 50Ω and will provide the power supply for the system as well. Input and output biasing and matching are an important part of the design.

The design will be firstly introduced and simulated into the software *LTSpice*. Once design and simulation is done, we will proceed to build our system physically and make the necessary adjustments to test and measure it properly. Results will be compared with the simulation outputs.

However, the department of Electrical and Electronic Engineering has no useful method of measuring amplifiers of very low-noise figure. Therefore, an experimental method will be designed based on the "hot-cold resistor" technique.

4. Objectives

- Propose some schematic drafts based on theoretical concepts for different parts of the design.
- Select appropriate components and simulate the system with its spice models.
- Physically build the designed system using real components and make the necessary adjustments until it works properly.
- Learn about the experimental noise figure measurement and propose a method to test the designed device.

5. Design

5.1. Transconductance Stage

In a transconductance amplifier, a voltage difference between two inputs creates a current at the output. The FET transistor, unlike the bipolar junction transistor (BJT) in which the current flows through the base creating an output current at the collector, is a voltage-controlled device. This means that the drain current will be a function of the voltage between the gate and the source.

For a FET, transconductance is the ratio of the change in drain current I_D to the change in gate-source voltage V_{GS} over a defined interval on the I_D vs V_{GS} curve:

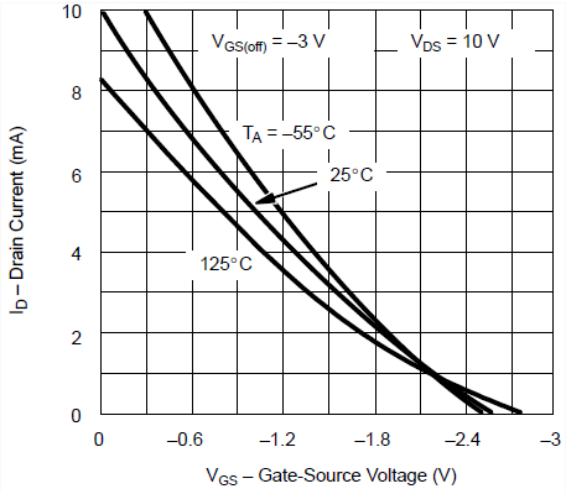


Fig 1. I_D vs V_{GS} curve

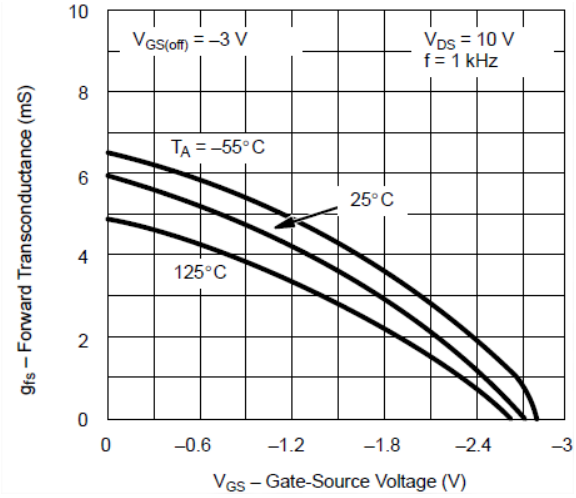


Fig 2. Transconductance vs V_{GS} curve

The figures above correspond to the transfer characteristics curves of a FET device.

In the design of our LNA we will make use of a Junction Field Effect Transistor (JFET). In JFETs the isolation between gate and channel is a reverse biased PN junction instead of using a layer of metal oxide. Because of this, JFETs are depletion only devices, which means that the device is normally ON at zero gate–source voltage. Nevertheless, when V_{GS} reverse-biases the PN junction, the flow between source and drain connections becomes limited. Maximum V_{GS} stops all current through source and drain, thus forcing the JFET into cut-off mode. This explains why the forward transconductance g_{fs} is higher when the gate–source voltage is closer to zero in *Figure 1* and *Figure 2*.

The point for using a JFET is that they are better than any other technology in making low-noise high-impedance amplifiers. “What makes JFETs good for noise at low frequencies is the fact that they are buried devices. The transistor junction that does the work is not up against the surface of the die. This means that the junction is not subject to the impurities, defects, and contamination of the surface.” (Rako, 2010)

One of the most important features of a JFET is its high input impedance, which lays typically from 1MΩ to several hundred megaohms. In comparison with BJT transistors, they have a much lower sensitivity to changes in the applied signal and are more temperature stable. (Boylestad & Nashelsky, 2012, p. 379)

Another important parameter is threshold voltage V_T, which is the gate–source voltage required in order to induce a channel between source and drain; increasing V_{GS} further enhances this channel. There are three distinct regions of operation when using a FET:

- **Linear region**: where $V_{DS} \ll V_{GS} - V_T$
- **Triode region**: where $\sim V_T/10 < V_{DS} < V_{GS} - V_T$
- **Saturation region**: where $V_{DS} > V_{GS} - V_T$

When employed as an analogue amplifier, it is used in the **saturation region**. In this mode, as a first order approximation, I_D is considered independent of V_{DS}.

5.1.1. JFET biasing

The selected device for this project will be the JFET **MMBF4416**, with has an operative range over 1GHz and claims to have a very good Noise Figure of 2dB at100MHz and, at least, 20dB of power gain. For further information about it, please refer to the datasheet attached to the appendices at the end of the document.

The device will operate in **common source configuration**, where the source terminal is tied to ground and the input signal is applied to the gate, thus varying the V_{GS} parameter. As seen before, this causes a change in drain current I_D proportional to the transconductance ratio. In order to make this possible, we need to keep V_{GS} as a negative voltage to reverse-bias the PN junction, so we will place a resistor between source and ground. This is called self-bias configuration.

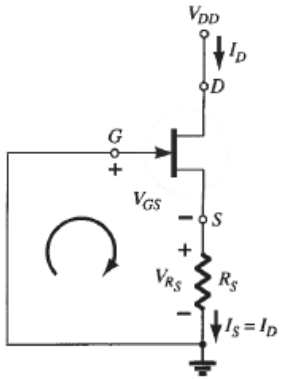


Fig 3. DC analysis of the self-bias configuration

The value of the resistor R_S needs to be as low as possible since we want to keep V_{GS} close to zero in order to provide a better transconductance (see *Figure 2*). There is a reason why we can't just give this resistor a fixed value, and it is because depending on the amplitude of the input signal we need a greater V_{GS}. We have selected a **25Ω variable resistor** so when I_D becomes maximum (about 10mA referring to datasheet), the value of V_{GS} reaches -0.25V, which should be enough.

The source of the JFET needs to be grounded for the signal path, so a capacitor C_S will be tied in parallel to R_S. It will also help us against noise: as explained previously, thermal noise appears on any device presenting a determined resistivity and held at any temperature different from 0K (R_S), which means that the capacitor C_S will also keep that noise from being added to the output signal. Since the value of this component is not critical at all, we will choose, for example, a **100nF** capacitor for this purpose.

Gate terminal also needs to be grounded for biasing, but this will be discussed in the next section: input matching.

5.1.2. Input matching

Our amplifier must provide a low input impedance which lays, by definition, around 1 to 4 Ω. However, since the JFET is a voltage controlled device its gate has a very high input impedance. To solve this, we will place an **L matching network** which is, basically, an LC resonator tuned at the working frequency of the system. This method is widely used in the design of tuned amplifiers since its response resembles that of a band-pass filter, which stops bands on either side of the central frequency.

We also want to keep our gate grounded in DC terms for biasing, so the schematic to be implemented is the high-pass L matching network shown in the figure below:

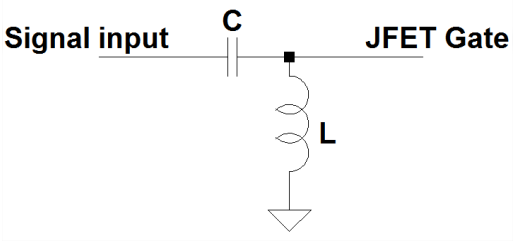


Fig 4. LC resonator for input matching

This allows the input signal to pass through the capacitor C and reach the gate while it remains DC biased to ground with the help of the inductor L.

Let's calculate the input impedance of the proposed matching network, assuming the JFET gate impedance to be very high (open circuit):

$$Z_{IN} = Z_C + Z_L = \frac{1}{j2\pi f_0 C} + j2\pi f_0 L$$

Eq 4. Input impedance of the L network

To get a low input impedance we need to assume $Z_{IN} = 0$. Being f_0 the central frequency of the amplifier, we obtain the following expression which gives us pairs of values for both capacitor and inductor that will be resonant at f_0.

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

Eq 5. Resonant frequency of the L network

Now we need to choose them keeping in mind the availability in our components provider and the frequency range we are working on (*nH* and *pF*). In order to be able to tune our amplifier properly, the inductor will be a fixed value and the capacitor an adjustable one. Selecting the inductance to be **120nH**, we proceed to calculate the capacitance using the previous equation which results as follows:

$$C = \frac{1}{(2\pi\sqrt{120nH} \cdot 125MHz)^2} = 13.51pF$$

So by now the chosen component will be a **22pF** variable capacitor. Later we will need to tune it to the correct frequency while building the system. With this, the input matching is done.

This is what we got so far:

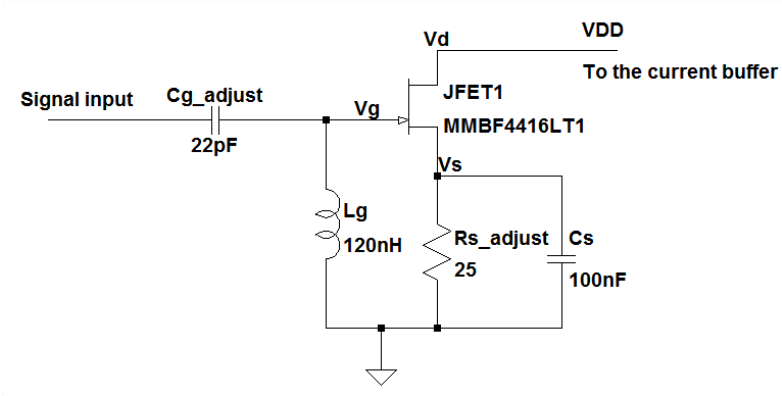


Fig 5. Complete schematic of the transconductance stage

Where the input matching plays three key roles:

- To band-pass the input signal.
- To provide a very low input impedance to the LNA.
- To keep the device biased.

5.2. Current Buffer

This section will cover up the design of the BJT current buffer and its corresponding output matching towards the load. A buffer is a system that provides impedance transformation from one circuit to another, leaving the signal unchanged. This can be modelled as a unity gain amplifier or, in this case, a current follower.

The schematic shown previously in *Figure 5* provides a current I_D which carries the amplified input signal through the JFET drain, so that stage is the one which provides a transconductance gain to the signal. Then it will go through the current buffer, whose purpose is to drive the power to the output load.

We will make use of a bipolar transistor in order to achieve it. The BJT working principle can be summarised into this: when a current I_B is driven into the base terminal, the device allows the current flow between collector and emitter. To be able to draw current through the base terminal, it is necessary to apply a minimum base-emitter voltage V_{BE} which is usually around 0.7V.

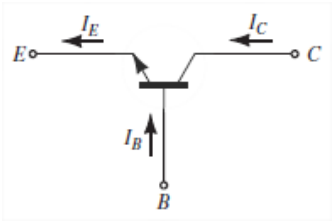


Fig 6. Currents diagram of a BJT

5.2.1. BJT biasing

The chosen device is the BJT **BC547B**, which is designed to operate up to 300MHz. Its datasheet can be found in the appendices at the end of the document.

The device will operate in **common base configuration**. This means that the signal will go through emitter and collector while referenced to the base, which will need to be grounded for the AC path. To ensure the current to flow, we need to constantly keep the device in active mode, so the V_{BE} voltage won't go below 0.7V. We also need to take into account that the voltage at the emitter V_E will be feeding the JFET stage, so it is important to not to drop it too much.

They key here is a resistive voltage divider between collector, base and ground. It will provide the necessary DC references for a correct biasing. It is shown in the figure below:

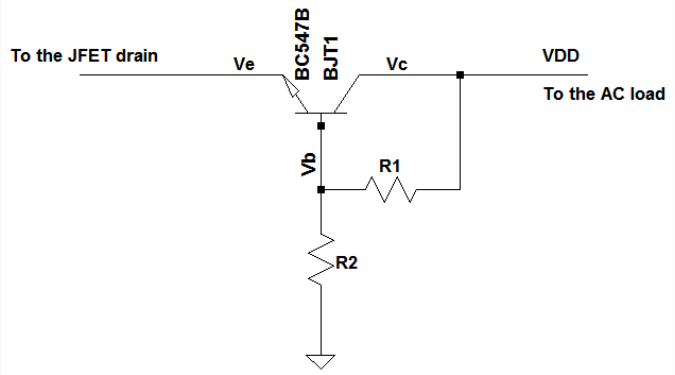


Fig 7. BJT biasing schematic

To choose appropriate values for the resistors R_1 and R_2, we will consider the following statements:

- $V_C = V_{DD}$
- V_{BE} around 0.7V
- V_E as high as possible.

Then if we want $V_E = V_{DD} - 0.7\text{V}$, V_B needs to be close to V_{DD}, so $R_2 >> R_1$.

Here we have an extract from the device datasheet:

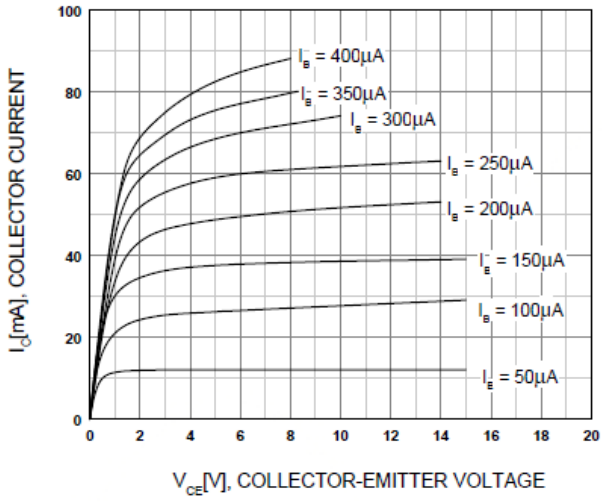


Fig 8. I_B and I_C curve from datasheet

Previously we stated that the maximum amount of current provided by the JFET would be around 10mA. Looking at the *Figure 8* above, for that I_C the base current should be less than 50µA. For efficiency purposes, we don't need to draw much more current through the $R_1 + R_2$ divider, because it will be dissipated anyway. This means than the optimum value of both $R_1 + R_2$ will be around 500KΩ. The selected resistor values are then **10KΩ** for R_1 **470KΩ** for R_2.

Finally, in order to get the BJT base grounded for the signal path and to avoid adding thermal noise to the output signal, we need to bypass R_2 with a capacitor C_b just like we did with R_S in the JFET. Since the value of this component is not critical at all, we will choose the same value as before so it will be a **100nF** capacitor. So far, here it is the complete schematic designed in this section:

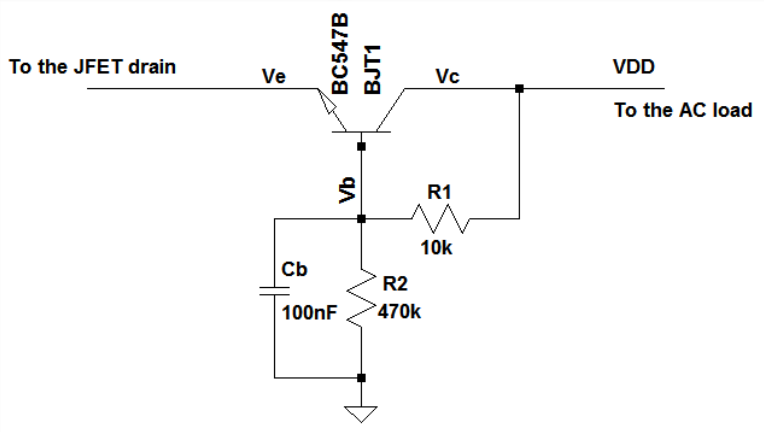


Fig 9. Complete BJT current buffer schematic

5.2.2. Output matching

Impedance matching is the technique of maximising the power transfer between a source and its load, or minimising the signal reflection from the load. To achieve this, we need to "match" both source and load impedances. Consider the example circuit below with a voltage generator, source and load impedances:

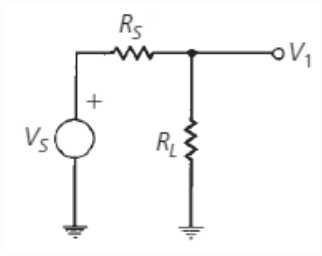


Fig 10. Example circuit

The power transfer expression from the source V_S to the load R_L is:

$$P = V_S \cdot \frac{R_L}{R_S + R_L}$$

Eq 6. Power transfer to R_L

And its graph:

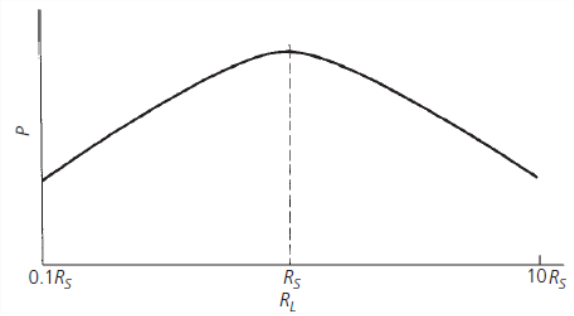


Fig 11. Graph of the power transfer expression

As we can see, the match occurs when both source and load impedances are equal. However, this is slightly different when dealing with AC signals. In that case they need to be the complex conjugate each other, this is, having the same real part but with an opposite reactance. To match complex impedances, we make use of matching circuits (or matching networks) which usually consist of capacitors and inductances.

To start with the matching, we first need to find out what the output impedance of our current buffer is. We will employ the *LTSpice* simulator for this purpose:

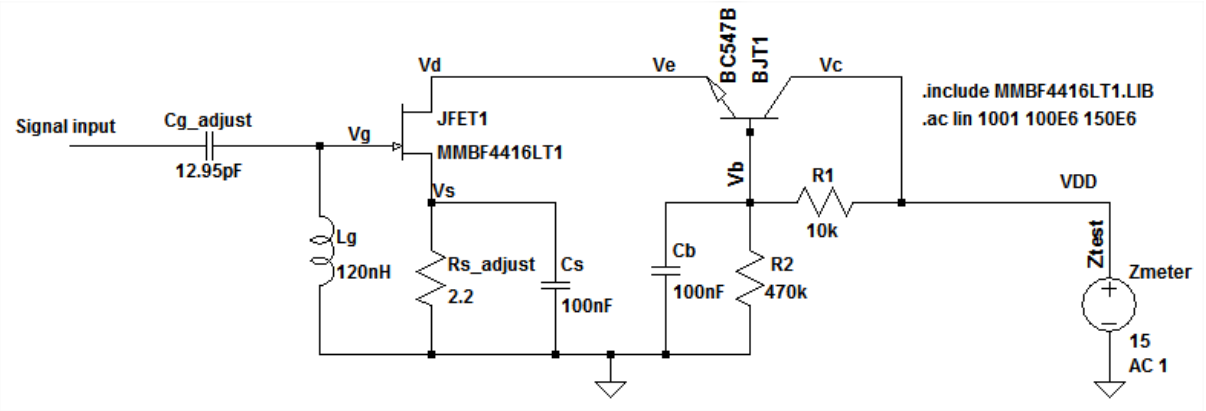


Fig 12. Measuring output impedance. Schematic

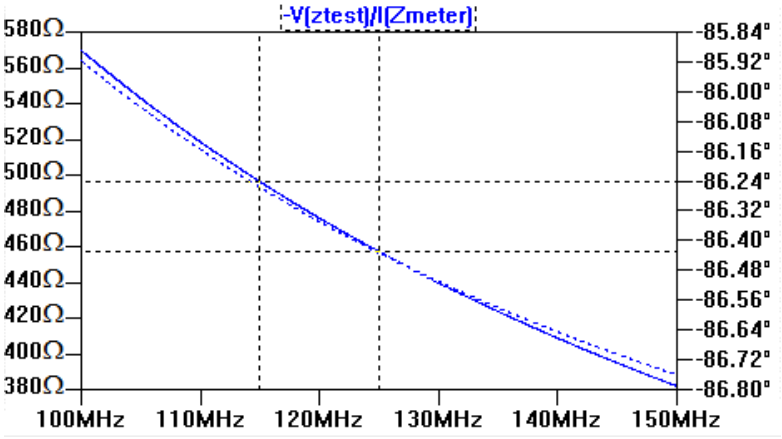


Fig 13. Measuring output impedance. Graph

The software gives us an output impedance of 28.57 – 455.39j Ω at 125MHz.

Now we need to match it with a pure resistive 50Ω AC load. This could have been done by hand either using equations or a Smith Chart, but it is easier to use a tool to calculate it automatically. (EEWeb Pi-Match Online Calculator, 2017)

We select a **PI network** that does not block DC and has a Q factor around 5-10. The application gives us back the following matching network:

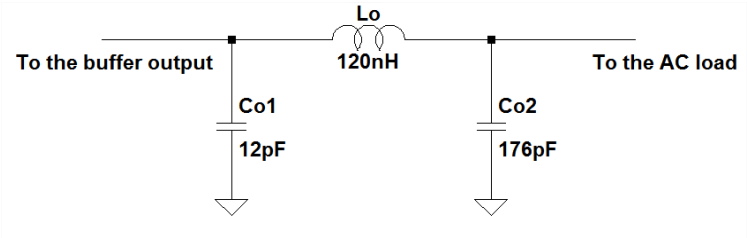


Fig 14. Output PI matching network

The Q factor is 6.9

The values of the capacitors will be: C_{O1} = **12pF** and C_{O2} = **150pF + 60pF** variable capacitor. The inductance L_O will be **120nH**.

We proceed now to check the designed matching network using the *LTSpice* simulator again. The results are:

- Input impedance of the matching network: 28.49 + 454.06j Ω
- Output impedance of the matching network: 48.97 + 3.67j Ω

So we can conclude that the matching network will work properly.

5.3. Signal source and AC load

To facilitate the measurement of the system, we also need to design some complements that will work together with the LNA in the physical build.

Firstly, we need to build a signal source to feed the circuit. Our solution is to use a 125MHz packaged active crystal oscillator (**SG-8003**) followed by an operational amplifier (**TSV622**) with unity gain. Their datasheets are attached to the appendices at the end of the document.

The oscillator itself generates a **400mVpp 125MHz** wave with a DC offset. We will high-pass filter this signal to remove the continuous component and attenuate its amplitude. Then it will be tied to a voltage-follower operational amplifier with 50Ω output impedance:

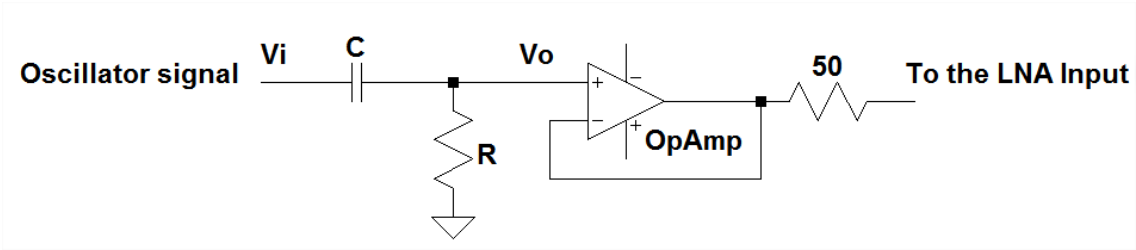


Fig 15. Oscillator, filter and voltage follower placed together

To design the filter, let's have a look at its response:

$$v_o = v_i \frac{R}{R + Z_C}$$

Eq 7. Filter response

We set v_i = 200mVp and v_0 = 1mVp and proceed to calculate RC:

$$RC = \frac{v_o}{(v_i - v_o)2\pi f} = 6.4x10^{-12}$$

So we can select a **5pF** variable capacitor and a **2.2Ω** fixed value resistor. This way we would be able to adjust the signal amplitude just by tuning C.

In order to power both devices, oscillator and operational amplifier, we have placed a 3.3V voltage regulator (UA78M33C) from the 15V power supply.

Secondly, an AC load also need to be designed. In a real application the output transmission line will provide the 50Ω load while powering the amplifier. To model this, we have proposed the schematic shown in the figure below:

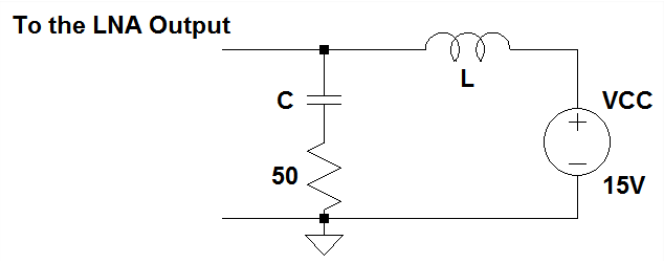


Fig 16. AC Load and Power Supply through the same line

The inductor L blocks the AC signal to pass through the power supply, while the capacitor C blocks the DC component to go through the 50Ω load. These two components will need to be carefully selected to cancel the total reactance of the load at the working frequency. The load impedance in AC terms is:

$$Z_{LOAD} = (Z_C + 50) \,//\, Z_L = \frac{\left(\frac{1}{j2\pi fC} + 50\right) j2\pi fL}{\left(\frac{1}{j2\pi fC} + 50\right) + j2\pi fL} = 50\Omega$$

Eq 8. Impedance of the load in AC terms

By fixing frequency $f = 125MHz$ and choosing the inductor $\boldsymbol{L = 500nH}$, we can calculate the capacitor which results to be $C = 196.7pF$. We will place a **150pF + 60pF** variable capacitor so it can be adjusted later with the help of a VNA.

With this, all the design process is done.

6. Simulation results

In this section we will use the simulation software *LTSpice* to test all the designed schematics.

6.1. Input matching

We adjusted the capacitor in the LC resonator until the input impedance was minimum at 125MHz. This are the results:

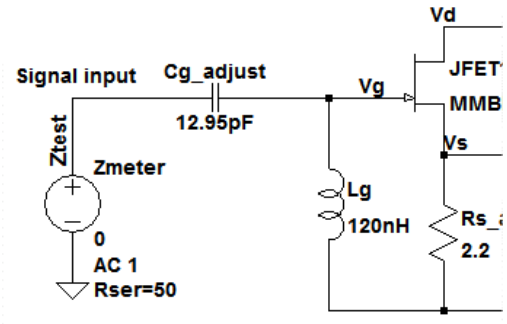


Fig 17. Input matching schematic

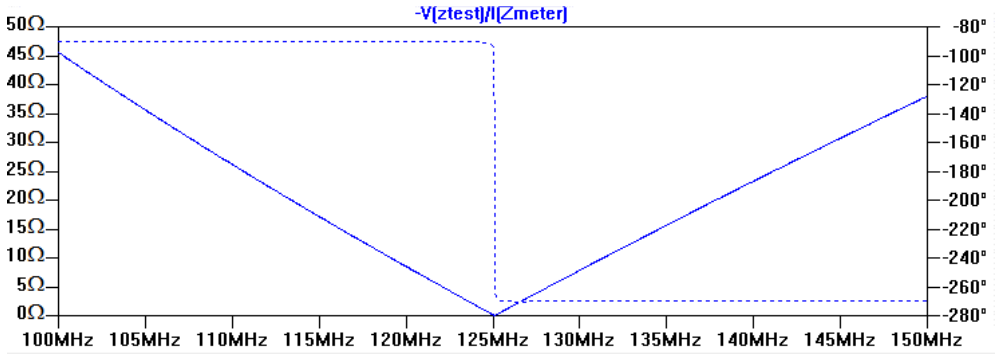


Fig 18. LNA input impedance

As we can see in the *Figure 18* above, the input impedance is minimum at the working frequency.

The input matching is working properly.

6.2. Transconductance stage

We proceed to add a signal source as the input signal. It generates a 1mV 125MHz wave. Then we measure V_{GS} and I_D in the time domain to adjust the R_S resistor at the source of the JFET, which controls the gate-source voltage. We establish that 0.5Ω seems to be a proper value, since it keeps V_{GS} around -6.5mV on average and gives us a drain current I_D of 13.3mA.

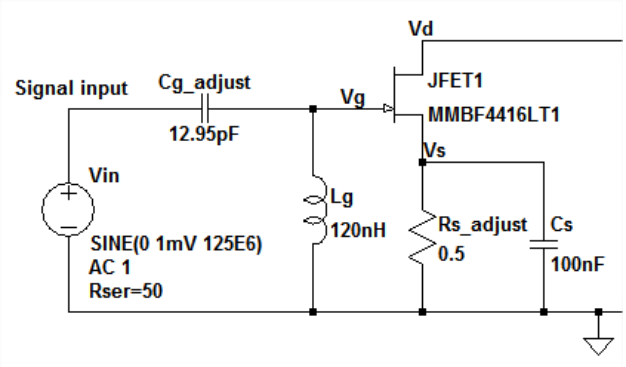


Fig 19. Schematic of the JFET transconductance stage

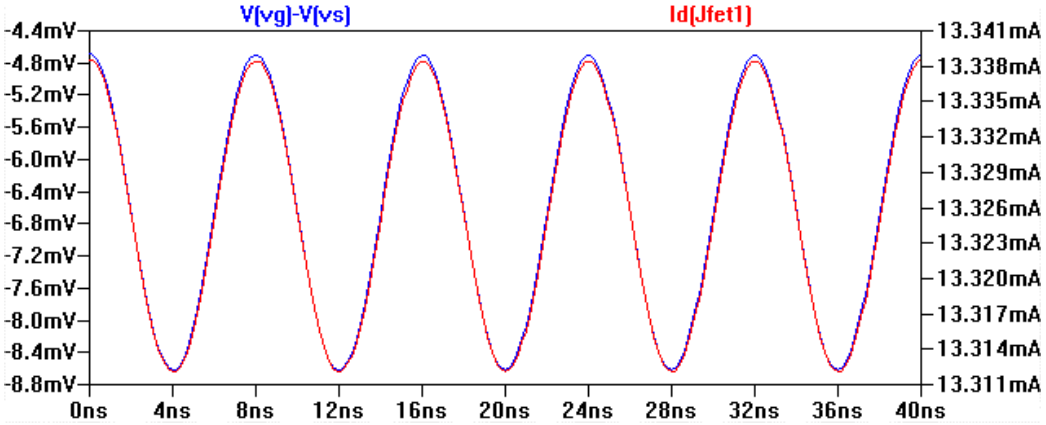


Fig 20. V_{GS} and I_D after adjusting R_S

To check if it is working on normal conditions, it is possible to measure the admittance of the device. To do it, we proceed as follows:

$$Y_{fs} = \frac{1}{g_{fs}} = \frac{(13.338 - 13.312)\ mA}{(8.616 - 4.71)\ mV} = \mathbf{6656\mu mhos}$$

Looking at the datasheet, we can verify that the *Forward Transfer Admittance* $|Y_{fs}|$ range of the device goes from 4500 to 7500 µmhos, which means that the simulation is working fine and the JFET is properly biased.

6.3. Current buffer

Checking the performance of the current buffer will be easier. We will measure both input and output currents to confirm that they are pretty identical:

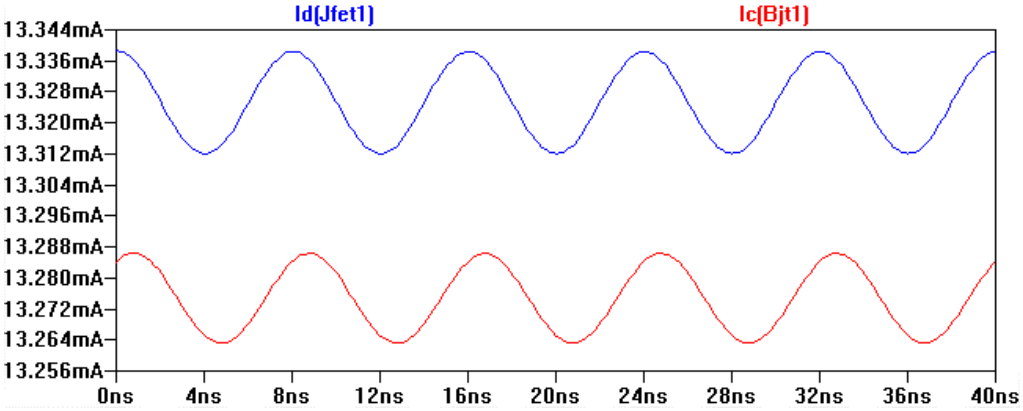


Fig 21. Input (blue) and output (red) currents

Since the emitter current I_E carries both collector I_C and base I_B current, it is slightly greater. The difference is measured to be 50.5µA.

$$I_E = I_C + I_B$$

Eq 9. Current balance on a BJT

To check that the device is working nice, we can get the β (or h_{fe}) parameter of the BJT which is, by definition, the relationship between collector and base currents:

$$\beta = \frac{I_C}{I_B} = \frac{13.275mA}{50.5\mu A} \cong 260$$

According to the device's datasheet, h_{fe} range spans from 200 to 450. We conclude that the biasing is working properly.

6.4. Output matching

This is one of the most important parts of the design. A good matching ensures that the amplifier can deliver all its power to the load. For the simulation, we will place the matching network and the designed AC load just at the output of the current buffer. Then we will perform an AC analysis to check if both, input and output currents, are maximums at the working frequency.

Here it is the complete design to be put under test. Note that a null voltage source has been placed to measure the output current:

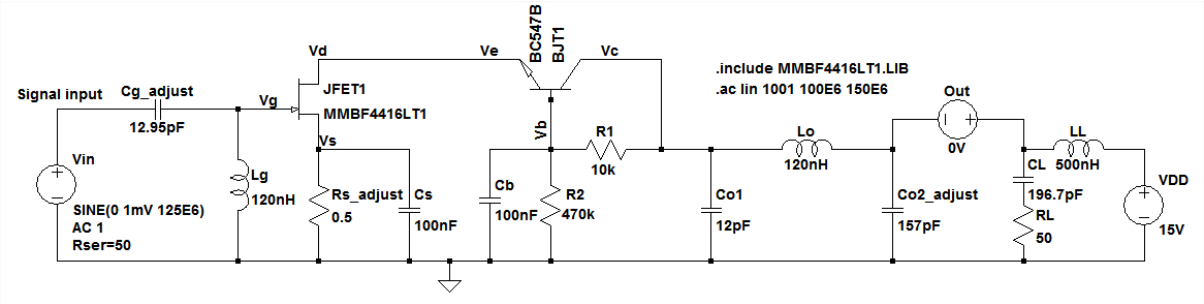


Fig 22. Complete schematic to be tested

And the results:

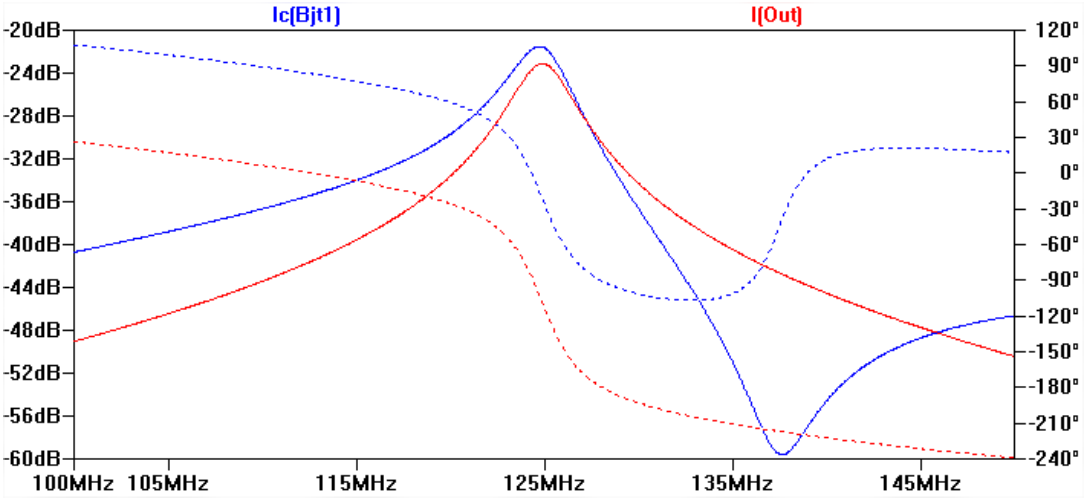


Fig 23. AC analysis of the output matching

After slightly adjusting the capacitor C_{O2}, we were able to tune the PI network to provide maximum power transfer at 125MHz. Despite the fact that there is a current loss of 1.5dB, the output matching proves to be working properly.

Since the whole system is working fine together, we can proceed now with power gain and noise figure analysis.

6.5. Power gain

To estimate the power gain of the system we need to calculate the power level of input and output signals. Firstly, we perform an transient analysis plotting voltage times current for both signals:

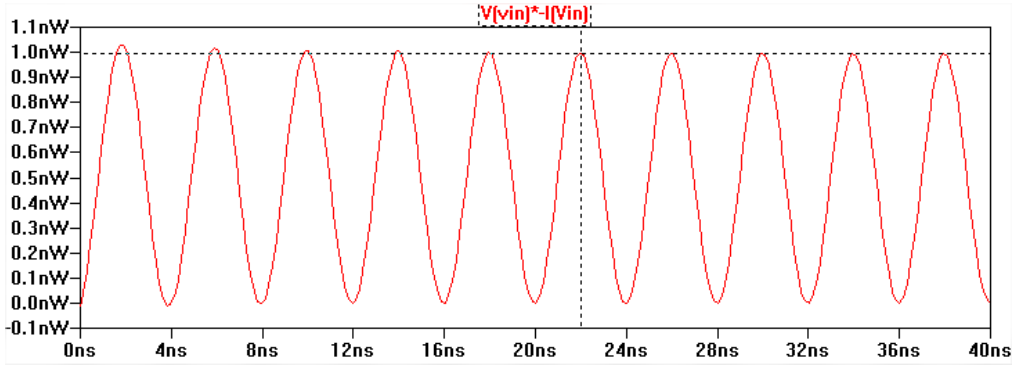


Fig 24. Input signal instantaneous power is 1nW

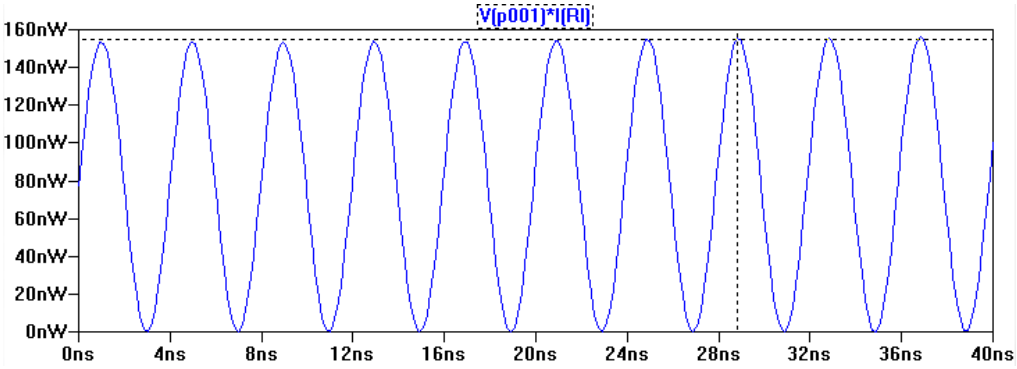


Fig 25. Output signal instantaneous power is 155nW

Now we proceed to calculate the total power gain G_T in decibel notation:

$$G_T = 10 \cdot log\left(\frac{P_{OUT}}{P_{IN}}\right) = 10 \cdot log\left(\frac{155\ nW}{1\ nW}\right) = 21.9\ dB$$

The system introduces a **power gain of 21.9 dB**, which is within the range it was expected to be.

6.6. Noise Figure

The simulator *LTSpice* also allows to perform a noise analysis of the system. We select the input voltage source as the noise reference, and the output voltage node as the point to analyse. The results thrown by the simulator are discussed below:

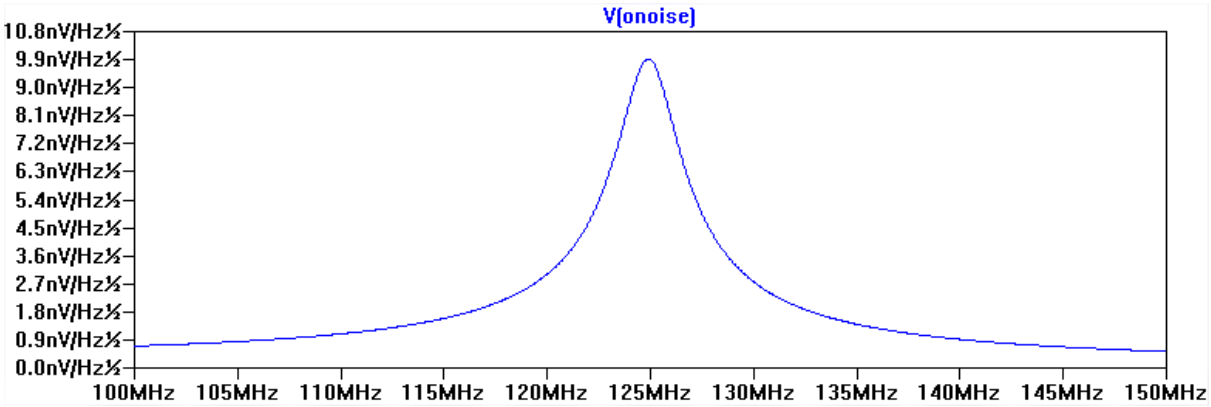


Fig 26. Noise analysis output

The first thing to take into account is the format of the results. They are shown as noise spectral density ($\tilde{v}$). It shows that at 125MHz we got a noise spectral density of 9.9nV/√Hz. To convert this into noise power we need to know the bandwidth of our signal.

For example, MRI applications use a typical bandwidth of 50KHz. We will consider that one for this example. (Graessner, 2013)

$$v_{RMS} = \tilde{v} \cdot \sqrt{B} = 9.9x10^{-9} \cdot \sqrt{50000} = 2.2\mu V_{RMS}$$

The estimated introduced voltage noise level is $\mathbf{2.2\mu V_{RMS}}$.

7. Build

7.1. Choosing the right components

In order to get the components on time, the selected providers have been Farnell and RS. One of the most challenging things when trying to build a RF design out of a simulator, is to fight against every unexpected factor that exist in the real world, such as parasitic capacitances and inductances, component tolerances, interferences, device limitations and other kind of inconveniences that will pop up during the job. In order to save time and avoid some problems we have taken into account some considerations when ordering components:

- **Capacitors**: we will choose the ceramic or plastic film ones. Electrolytic capacitors won't work for us at this frequency range due to its internal structure.
- **Inductors**: air-core coils preferred. Otherwise, we will need to have a look at its datasheet. The main reason is the self-resonance frequency (SRF), which can convert the inductor into a capacitor at higher frequencies.
- **Resistors**: avoid the wire-wound resistors. They can behave in an unusual way when used for RF purposes. If an uncommon resistor value is required (e.g. 50Ω), we can group some standard resistors to create that value (e.g. 2x100Ω in parallel), and what's more, it will reduce the conjunct tolerance.
- **SMD components**: not really practical for prototyping by hand, avoid if possible.
- **Core devices**: purchase several of them, they are the most important components of the project.
- Always have spare components.

With all of this in mind, we can now start to build the LNA.

7.2. Signal generator

This auxiliary circuit has been built and soldered into a stripboard. The most challenging parts to solder have been the SMD components like the oscillator, which has been placed to the back of the board, and the operational amplifier, whose short leads made it tricky.

One of the considerations taken into account while building this circuit has been the 50Ω load, which has been placed into a socket to allow futures manipulations or replacements. It consists of two 100Ω 1% resistors.

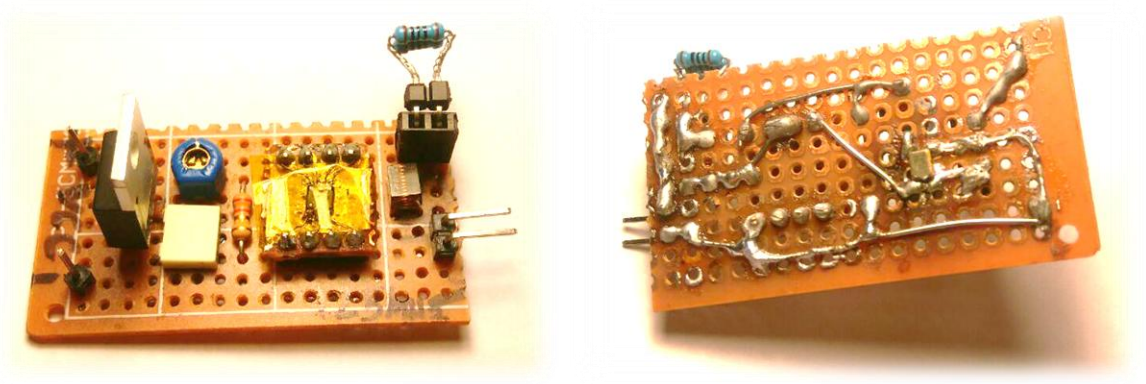


Fig 27. 125MHz signal generator finished

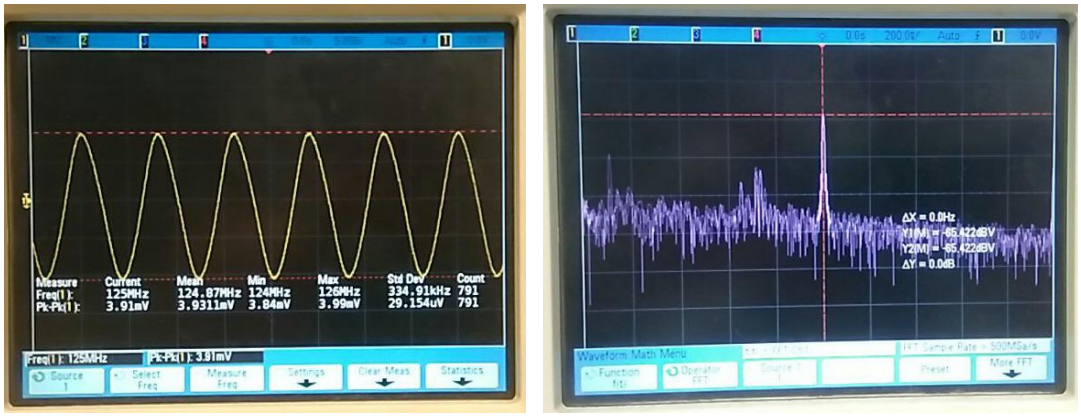


Fig 28. Generated signal

It works and provides a very clean 125MHz signal of 4mVpp amplitude, which can be adjusted with a variable capacitor.

Fig 29. Signal generator output impedance

However, its output impedance is not good enough. It seems that there is some kind of parasitic capacitance which agregates -95jΩ to the original 50Ω.

7.3. AC load

The AC load has been built on a stripboard as well. This are the results:

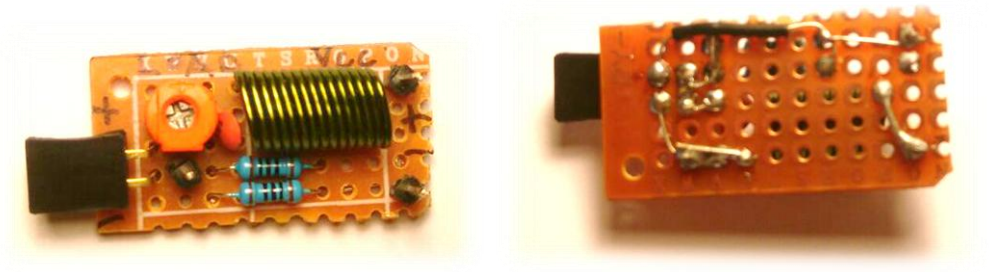


Fig 30. AC load built on a stripboard

Note that: a couple of 100Ω 1% resistors have been used to replace the 50Ω resistor in schematic.

Fig 31. AC load input impedance

We measured its input impedance with the help of a VNA, and the result was quite close:

$$\boldsymbol{Z_L = 51.3 + 4.2j\ \Omega}$$

This measurement will be written down just in case there is any need to modify the output matching of the LNA.

7.4. LNA prototype

Before starting with the build and adjustment process, here is an extra advice: all the connections must be as close as possible each other, avoiding long wire pieces, bridges, big solder joints… specially on the output matching. Otherwise, there might appear parasitic inductors, capacitors or even antennas that will introduce changes to the circuit, ruining all the previous designs and

simulations. A better way to do this would be with the design of a printed circuit board (PCB), but it is not considered to be worth on a first prototype by now.

Here is a general view of the final result:

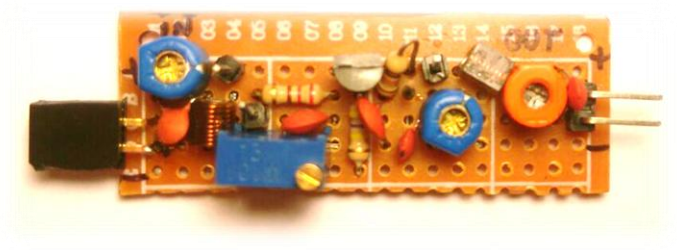


Fig 32. LNA prototype: top

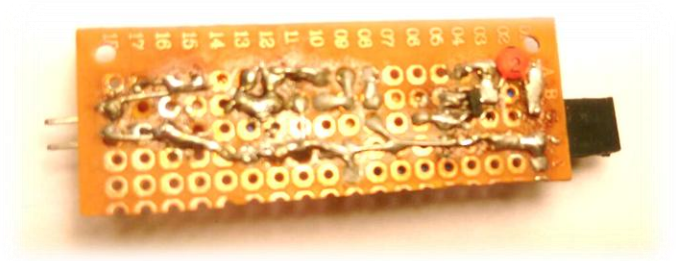


Fig 33. LNA prototype: bottom

As seen in the pictures, the JFET device has been soldered to the back since it uses SMT.

First of all, we need to adjust the input matching resonator. With the help of a VNA the capacitor C_G is tuned until the input impedance becomes minimum at 125MHz. Here is the result once it's done:

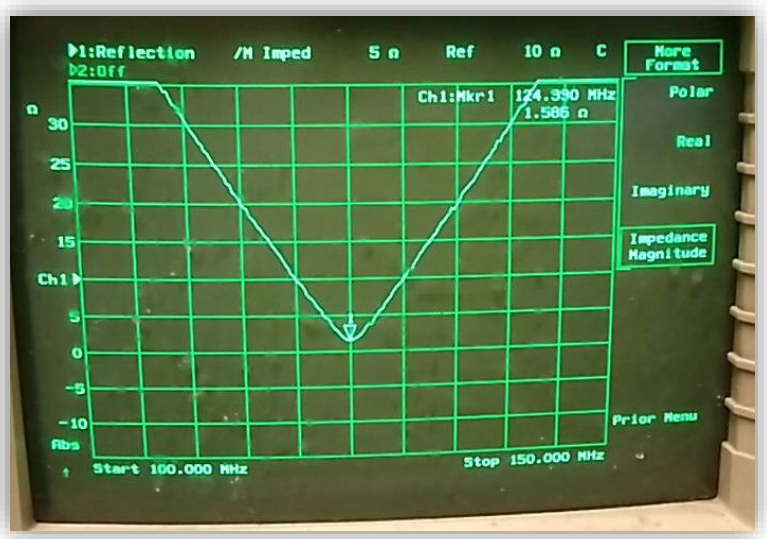


Fig 34. Input impedance magnitude

Fig 35. Input impedance Smith chart

The measured input impedance is **1.6 – 0.1j Ω**. As expected, it is a very low impedance.

The next step will be to adjust the resistor R_S to set the biasing of V_{GS}. It will end up being **-2mV**.

At its maximum, R_S = 25Ω, drops a voltage of 200mV, which means that the current I_D of the JFET is **8mA**. It was expected to be slightly higher, from 10 to 13mA.

Fig 36. Adjusted V_{GS} = -2mV

The next step is to check the current buffer. We find that the DC voltages are right, so it should be working fine.

Before soldering the output matching network, it is a good idea to measure the output impedance of the device, to check that everything is correct. Unfortunately, something has changed:

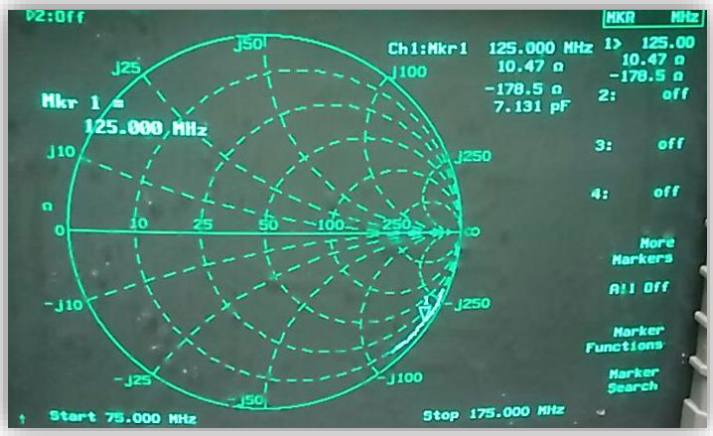


Fig 37. Output impedance of the current buffer

The measured impedance turns out to be **10.5 – 178.5j Ω** instead of the 28.57 – 455.39j Ω calculated by the software simulator. To solve this, we just need to design a new matching network with this new impedance and the one that we wrote down when we built the AC load. We will try to use a lower Q to make it easier to adjust. (EEWeb Pi-Match Online Calculator, 2017)

The new components are:

$$C_{O1} = 8.2pF \qquad L_O = 120nH \qquad C_{O1} = 117pF$$

To make it even easier, both capacitors will be adjustable.

When the new matching network is completely built and adjusted, we proceed to measure the LNA output impedance:

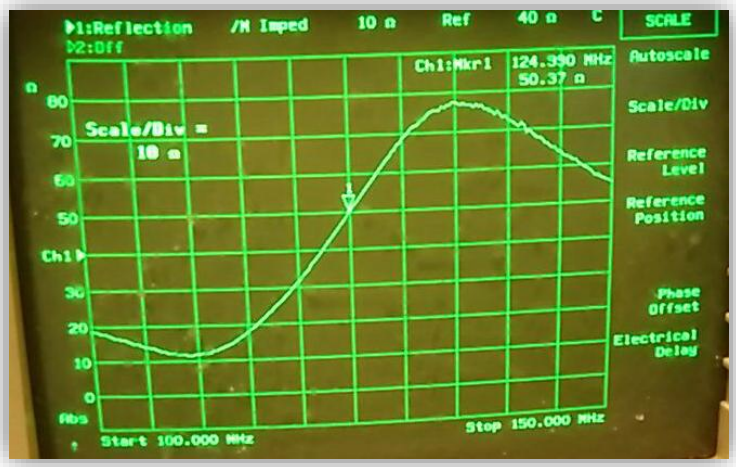


Fig 38. LNA output impedance: magnitude

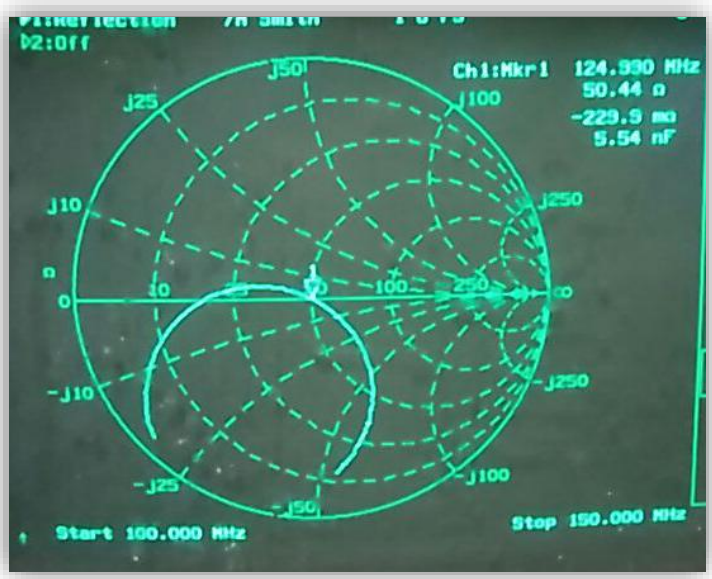


Fig 39. LNA output impedance: Smith chart

The result seems to be positive. The LNA output impedance is **50.4 – 0.2j Ω**

Here is a general overview of the whole design with both, schematics and physical LNA:

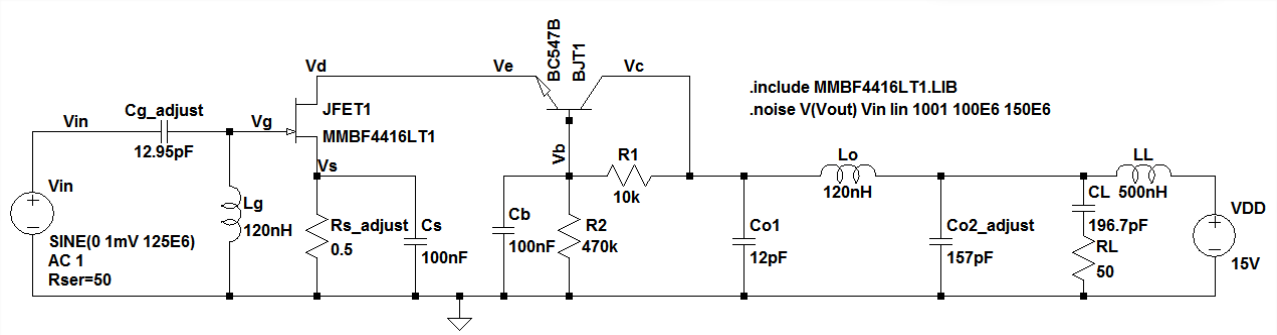


Fig 40. Final complete schematic for the LNA

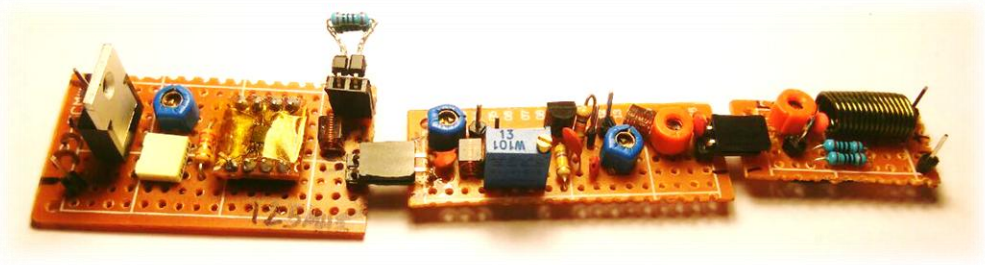


Fig 41. Finished build of the physical project

Unfortunately, despite all the measurements seem to be correct, the built device does not work properly. It refuses to provide any gain further than 2-3dB. But this will be discussed in detail in the next section.

8. Conclusions

Despite the fact that the built system refused to work, even after several modifications, I would qualify the overall results as a complete success based on the limitations that were imposed by this kind of project.

On the one hand, the simulation has shown to be working without any problems according to all the theoretical concepts and calculations. Because of that, the design seems to be valid.

On the other hand, several parts of the physical system have also proved to work accordingly to the simulations, except of the core devices. However, the process of building, testing, failing, walking around the problems, modifying, finding solutions, learning to use new equipment… all these have taught me more than if the project had been a complete success.

Because of that, in the next section I will propose some future work, just in case I have the opportunity of resume this project and take it further.

9. Future work

There will be several aspects of the project that will be marked as a future work. The first of them is to find out why the built system is not working properly. Maybe it is a soldering failure of an impedance mismatch, but it needs to be revised.

Another modification that can be done is to design a printed circuit board to build the prototype. It would avoid the apparition of parasitical components such capacitances or inductances, making it much easier to success, and also easier to measure the performance accurately.

A last future work would be to design and build an experimental method of measuring an amplifier of very low noise figure based on the "hot-cold load" technique. It is not a difficult method but it requires preparation and understanding about the process.

10.References

- Bowick, C. (2007). *RF Circuit Design.* Newnes.
- Boylestad, R. L., & Nashelsky, L. (2012). *Electronic Devices and Circuit Theory.* Prentice Hall PTR.
- Carr, J. J., & Brown, J. M. (2001). Noise factor, noise figure, and noise temperature. In *Introduction to Biomedical Equipment Technology.* Pearson Education.
- EEWeb Pi-Match Online Calculator. (2017). Retrieved from https://www.eeweb.com/toolbox/pi-match
- Farnell. (2017). Retrieved from http://uk.farnell.com/
- Graessner, J. (2013). *Bandwidth in MRI?* MAGNETOM Flash.
- Harter, A. (2003). *LNA Matching Techniques for Optimizing Noise Figures.*
- Ke, Q., & Feldman, M. (1993). *A technique for accurate noise temperature measurements for the superconducting quasiparticle receiver.*
- Rako, P. (2010). *Your friend, the JFET.*
- Razavi, B. (2011). *RF Microelectronics.* Prentice Hall.
- RS Components. (2017). Retrieved from https://uk.rs-online.com/

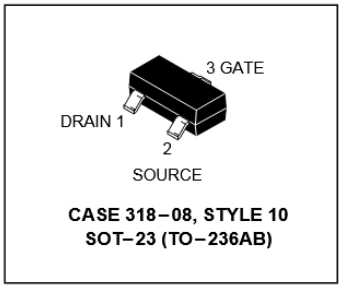
11.Appendices

11.1.Datasheets

11.1.1. JFET: MMBF4416

ABSOLUTE MAXIMUM RATINGS

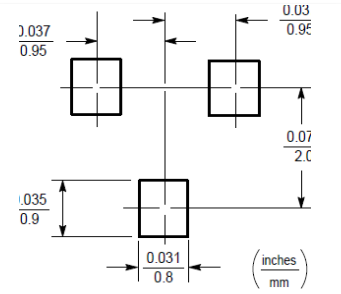
Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DS}	30	Vdc
Drain–Gate Voltage	V_{DG}	30	Vdc
Gate–Source Voltage	V_{GS}	30	Vdc
Gate Current	I_G	10	mAdc



CASE 318–08, STYLE 10
SOT–23 (TO–236AB)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR–5 Board(1) T_A = 25°C Derate above 25°C	P_D	225 1.8	mW mW/°C
Thermal Resistance, Junction to Ambient	R_{JA}	556	°C/W
Junction and Storage Temperature	T_J, T_{stg}	−55 to +150	°C



SOT–23

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

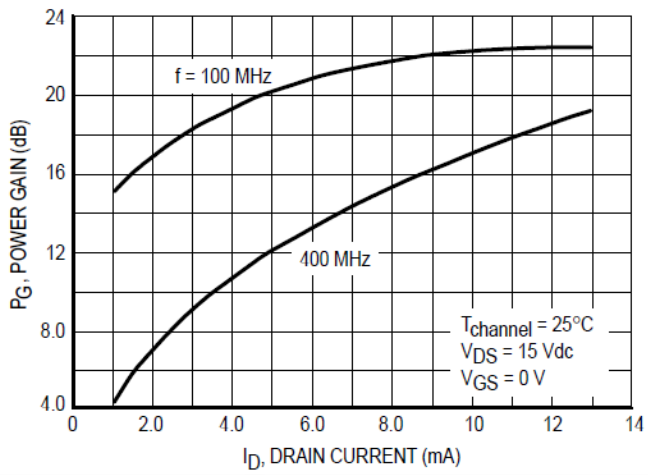
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Gate–Source Breakdown Voltage (I_G = 1.0 μAdc, V_{DS} = 0)	$V_{(BR)GSS}$	30	—	Vdc
Gate Reverse Current (V_{GS} = 20 Vdc, V_{DS} = 0) (V_{GS} = 20 Vdc, V_{DS} = 0, T_A = 150°C)	I_{GSS}	— —	1.0 200	nAdc
Gate Source Cutoff Voltage (I_D = 1.0 nAdc, V_{DS} = 15 Vdc)	$V_{GS(off)}$	—	−6.0	Vdc
Gate Source Voltage (I_D = 0.5 mAdc, V_{DS} = 15 Vdc)	V_{GS}	−1.0	−5.5	Vdc
ON CHARACTERISTICS				
Zero–Gate–Voltage Drain Current (V_{GS} = 15 Vdc, V_{GS} = 0)	I_{DSS}	5.0	15	mAdc
Gate–Source Forward Voltage (I_G = 1.0 mAdc, V_{DS} = 0)	$V_{GS(f)}$	—	1.0	Vdc
SMALL–SIGNAL CHARACTERISTICS				
Forward Transfer Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	$\|Y_{fs}\|$	4500	7500	μmhos
Output Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	$\|y_{os}\|$	—	50	μmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	4.0	pF

Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 10 MHz)	C_{rss}	—	0.8	pF
Output Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	2.0	pF

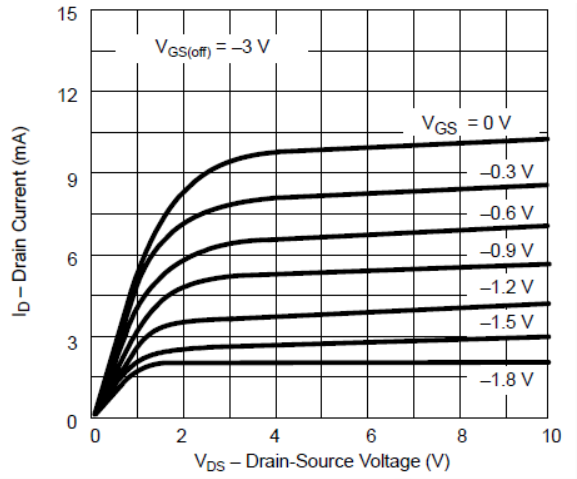
FUNCTIONAL CHARACTERISTICS

Noise Figure (V_{DS} = 15 Vdc, I_D = 5.0 mAdc, $R_g \approx 1000\ \Omega$, f = 100 MHz) (V_{DS} = 15 Vdc, I_D = 5.0 mAdc, $R_g \approx 1000\ \Omega$, f = 400 MHz)	NF	 — —	 2.0 4.0	dB
Common Source Power Gain (V_{DS} = 15 Vdc, I_D = 5.0 mAdc, f = 100 MHz) (V_{DS} = 15 Vdc, I_D = 5.0 mAdc, f = 400 MHz)	G_{ps}	 18 10	 — —	dB

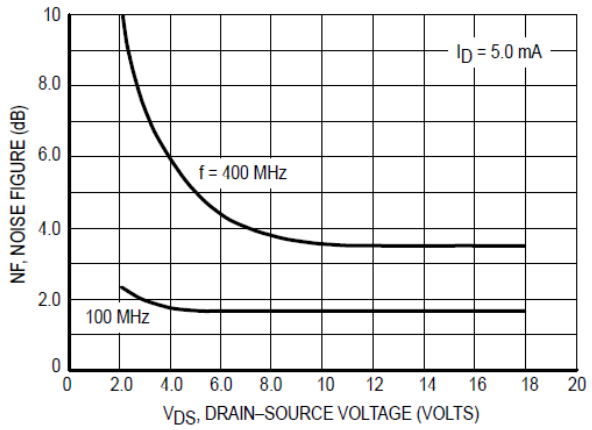
POWER GAIN

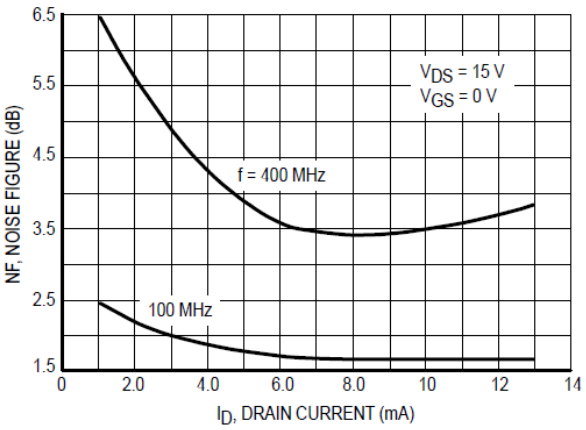


OUTPUT CHARACTERISTICS



NOISE FIGURE
($T_{channel}$ = 25°C)





11.1.2. BJT: BC547B

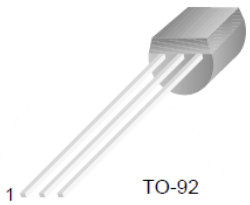
Electrical Characteristics

Values are at T_A = 25°C unless otherwise noted.

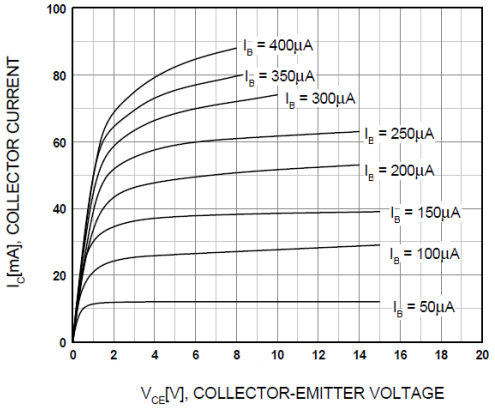
Symbol	Parameter		Conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector Cut-Off Current		V_{CB} = 30 V, I_E = 0			15	nA
h_{FE}	DC Current Gain		V_{CE} = 5 V, I_C = 2 mA	110		800	
$V_{CE}(sat)$	Collector-Emitter Saturation Voltage		I_C = 10 mA, I_B = 0.5 mA		90	250	mV
			I_C = 100 mA, I_B = 5 mA		250	600	
$V_{BE}(sat)$	Base-Emitter Saturation Voltage		I_C = 10 mA, I_B = 0.5 mA		700		mV
			I_C = 100 mA, I_B = 5 mA		900		
$V_{BE}(on)$	Base-Emitter On Voltage		V_{CE} = 5 V, I_C = 2 mA	580	660	700	mV
			V_{CE} = 5 V, I_C = 10 mA			720	
f_T	Current Gain Bandwidth Product		V_{CE} = 5 V, I_C = 10 mA, f = 100 MHz		300		MHz
C_{ob}	Output Capacitance		V_{CB} = 10 V, I_E = 0, f = 1 MHz		3.5	6.0	pF
C_{ib}	Input Capacitance		V_{EB} = 0.5 V, I_C = 0, f = 1 MHz		9		pF
NF	Noise Figure	BC546 / BC547 / BC548	V_{CE} = 5 V, I_C = 200 µA, f = 1 kHz, R_G = 2 kΩ		2.0	10.0	dB
		BC549 / BC550			1.2	4.0	
		BC549	V_{CE} = 5 V, I_C = 200 µA, R_G = 2 kΩ, f = 30 to 15000 MHz		1.4	4.0	
		BC550			1.4	3.0	

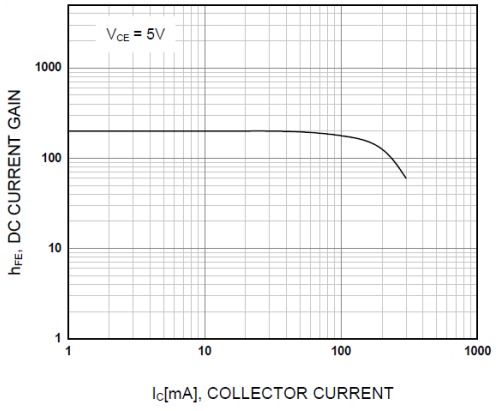
h_{FE} Classification

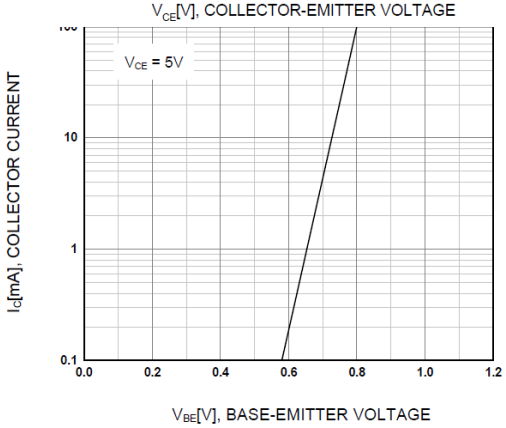
Classification	A	B	C
h_{FE}	110 ~ 220	200 ~ 450	420 ~ 800



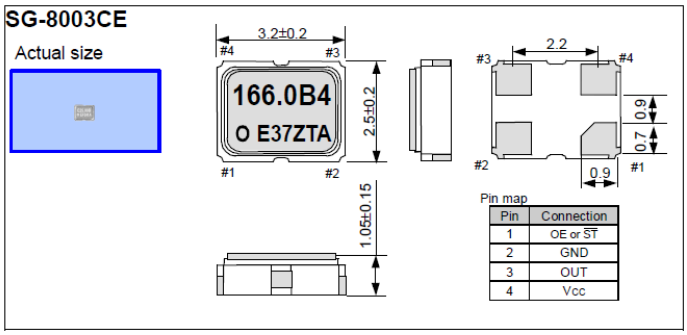
1. Collector 2. Base 3. Emitter

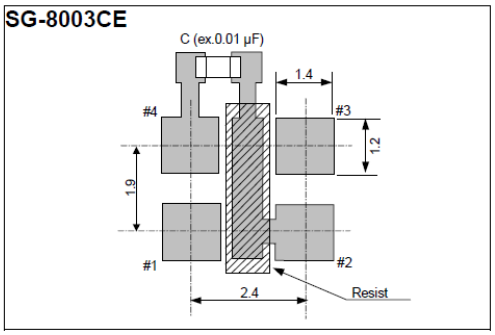






11.1.3. 125MHz Crystal Oscillator: SG-8003CE





Item	Symbol	Specifications		
		PE / SE	PD / SD	PC / SC
Output frequency range	f0	1 MHz to 166 MHz		
Supply voltage	Vcc	1.8 V Typ. 1.6 V to 2.2 V	2.5 V Typ. 2.2 V to 2.8 V	3.3 V Typ. 2.7 V to 3.6 V
Storage temperature	T_stg	-40 °C to +85 ℃		
Operating temperature	T_use	-20 °C to +70 ℃ / -40 °C to +85 ℃		
Frequency tolerance	f_tol	B: ±50 × 10^{-6}, C: ±100 × 10^{-6}		
		L:±50 × 10^{-6}, M: ±100 × 10^{-6}		
Current consumption	Icc	3.5 mA Max.	4.0 mA Max.	
		5.0 mA Max.	6.5 mA Max.	
		6.0 mA Max.	8.5 mA Max.	
		7.0 mA Max.	10.5 mA Max.	
		8.5 mA Max.	12.5 mA Max.	
		10.0 mA Max.	15.0 mA Max.	
Output disable current	I_dis	8 mA Max.		
Stand-by current	I_std	50 µA Max.		
Symmetry	SYM	45 % to 55 %		
Output voltage	VOH	90 % Vcc Min.		Vcc -0.4 V Min.
	VOL	10 % Vcc Max.		0.4 V Max.
Output load condition (CMOS)	L_CMOS	15 pF Max.		
Input voltage	VIH	80 % Vcc Min.		
	VIL	20 % Vcc Max.		
Rise and Fall time	tr/ tf	5.0 ns Max.		
		2.5 ns Max.		
Start-up time	t_str	5 ms Max.		
Frequency aging	f_aging	±3 × 10^{-6} / year Max.		

Product Name (Standard form)

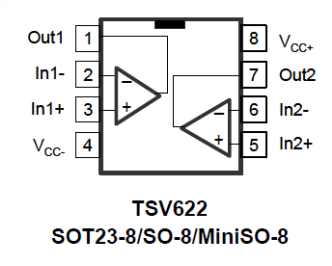
SG-8003 CG 166.000000MHz P E B
① ② ③ ④⑤⑥

①Model ②Package type ③Frequency
④Function (P: Output enable, S:Standby)
⑤Supply voltage ⑥Frequency tolerance

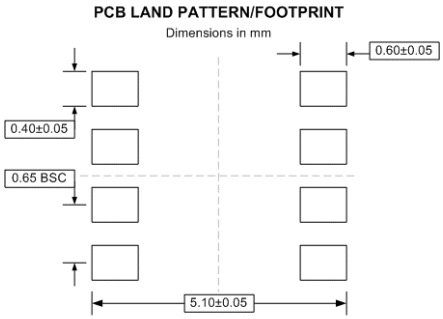
⑤Supply voltage	
C	3.3 V Typ.
D	2.5 V Typ.
E	1.8 V Typ.

⑥Frequency tolerance	
B	±50 × 10^{-6} / -20 to +70℃
C	±100 × 10^{-6} / -20 to +70℃
L	±50 × 10^{-6} / -40 to +85℃
M	±100 × 10^{-6} / -40 to +85℃

11.1.4. Operational Amplifier: TSV622



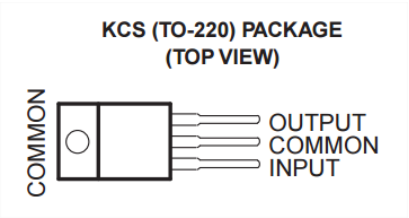
TSV622
SOT23-8/SO-8/MiniSO-8

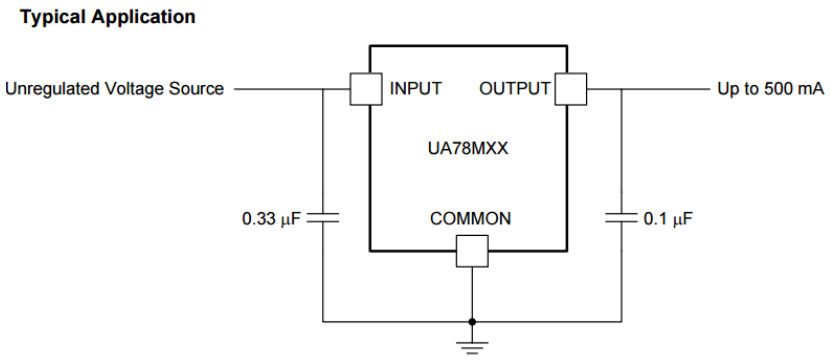


Electrical characteristics at V_{CC+} = +3.3 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25° C, and R_L connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage	TSV62x TSV62xA TSV623AIST - MiniSO10			4 0.8 1	mV
		TSV62x -T_{min} < T_{op} < T_{max} TSV62xA - T_{min} < T_{op} < T_{max} TSV623AIST - T_{min} < T_{op} < T_{max}			6 2 2.2	
$\Delta V_{io}/\Delta T$	Input offset voltage drift			2		µV/°C
I_{io}	Input offset current			1	10(1)	pA
		T_{min} < T_{op} < T_{max}		1	100	
I_{ib}	Input bias current			1	10(1)	
		T_{min} < T_{op} < T_{max}		1	100	
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0 V to 3.3 V, V_{out} = 1.65 V	57	79		dB
		T_{min} < T_{op} < T_{max}	53			
A_{vd}	Large signal voltage gain	R_L=10 kΩ, V_{out} = 0.5 V to 2.8 V	81	98		
		T_{min} < T_{op} < T_{max}	76			
V_{OH}	High level output voltage	R_L = 10 kΩ T_{min} < T_{op} < T_{max}	35 50	5		mV
V_{OL}	Low level output voltage	R_L = 10 kΩ T_{min} < T_{op} < T_{max}		4	35 50	
I_{out}	Isink	V_o = 5 V	23	45		mA
		T_{min} < T_{op} < T_{max}	20			
	Isource	V_o = 0 V	23	38		
		T_{min} < T_{op} < T_{max}	20			
I_{CC}	Supply current (per operator)	No load, V_{out} = 2.5 V		26	33	µA
		T_{min} < T_{op} < T_{max}			35	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF, f = 100 kHz	310	380		kHz
F_u	Unity gain frequency	R_L = 10 kΩ, C_L = 100 pF		310		
ϕm	Phase margin			41		Degrees
G_m	Gain margin			8		dB
SR	Slew rate	R_L = 10 kΩ, C_L = 100 pF, A_V = 1	0.11	0.175		V/µs

11.1.5. 3.3V Voltage Regulator: UA78M33C





Electrical Characteristics — uA78M33C

at specified virtual junction temperature, V_I = 8 V, I_O = 350 mA, T_J = 25°C (unless otherwise noted)

PARAMETER0	TEST CONDITIONS(1)		uA78M33C			UNIT
			MIN	TYP	MAX	
Output voltage(2)	I_O = 5 mA to 350 mA, V_I = 8 V to 20 V		3.2	3.3	3.4	V
		T_J = 0°C to 125°C	3.1	3.3	3.5	
Input voltage regulation	I_O = 200 mA	V_I = 5.3 V to 25 V		9	100	mV
		V_I = 8 V to 25 V		3	50	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz	I_O = 100 mA, T_J = 0°C to 125°C	62			dB
		I_O = 300 mA	62	80		
Output voltage regulation	V_I = 8 V,	I_O = 5 mA to 500 mA		20	100	mV
Temperature coefficient of output voltage	I_O = 5 mA,	T_J = 0°C to 125°C		–1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			40	200	µV
Dropout voltage				2		V
Bias current				4.5	6	mA
Bias current change	I_O = 200 mA, V_I = 8 V to 25 V,	T_J = 0°C to 125°C			0.8	mA
	I_O = 5 mA to 350 mA,	T_J = 0°C to 125°C			0.5	
Short-circuit output current	V_I = 35 V			300		mA
Peak output current				700		mA

(1) All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.
(2) This specification applies only for dc power dissipation permitted by *Absolute Maximum Ratings*.

11.2. Software and hardware used

- *LTSpice* v4.23
- Oscilloscope *Agilent DSO6014A*
- RF Network Analyzer *Hewlett Packard 8714B*