Addressing Fiber-to-Chip Coupling Issues in Silicon Photonics

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Prefacio

Este trabajo trata sobre fotónica de silicio. Trata, pues, de la manipulación de la luz, o fotones. La luz que transporta la información por todo el planeta. La luz de los sistemas de comunicaciones basados en fibra óptica. La fotónica de silicio es la aplicación a estos sistemas fotónicos que usan silicio como medio óptico. La fotónica de silicio estudia la manipulación de la luz en dispositivos a una escala sub-micrométrica (hasta nanométrica) para muchas aplicaciones y, por tanto, también para comunicaciones en particular.

Cuando empecé mi trabajo en el NTC como estudiante de ingeniería en 2005, este Centro estaba casi empezando a investigar en el campo, especialmente en el tema del acoplo fibra-chip. Tuve así pues el placer de continuar investigando en el tema como estudiante de doctorado, bajo la supervisión de Pablo, a quien estoy muy agradecido por ello. En los pasados cinco años, la fotónica de silicio se ha convertido en un campo muy activo en el grupo, con al menos diez personas investigando en diferentes aplicaciones. Con los años, hemos intentado desarrollar una exhaustiva comprensión de la complejidad de la fotónica de silicio. Este es uno de los propósitos de este libro: compartir nuestra visión.

Muchas de las ideas aquí expuestas son resultado de fructíferas discusiones entre compañeros tanto del interior del grupo como de otros grupos de investigación. Con el riesgo de olvidar a alguien, me gustaría mencionar algunas personas por su nombre.

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Gracias, Antoine, por haber sido mi compañero durante este tiempo. Soy consciente de la increíble persona con la que he estado trabajando. Te deseo todo lo mejor con tu tesis, y mucha suerte tanto en lo personal como en lo profesional.

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Este trabajo no habría sido posible sin las manos del equipo de fabricación del NTC, quienes, con el objetivo de poder hacer nuestros experimentos, han procesado tantas obleas como ha sido necesario, y empleado siempre el tiempo que se les ha requierido. Gracias Amadeu, Jose, Juan, Laurent, Paco por vuestro siempre buen trabajo de fabricación, y por vuestras siempre útiles discusiones sobre procesos y métodos de fabricación. Gracias también al equipo de instalaciones Alfredo, Luis, Antonio y Glenn, por hacer posible "construir" nuestra casi nueva sala limpia (recordar, el lugar más limpio de España).

Nuestros compañeros de los proyectos ePIXnet y HELIOS también se merecen las gracias. Mucho de mi trabajo se ha llevado a cabo en el marco de estos proyectos, y sin las colaboraciones, las cosas habrían sido diferentes. Gracias especiales a nuestros amigos Lars y Tolga, a quienes conocí gracias a nuestra colaboración dentro de estos proyectos. Gracias de nuevo, Tolga, por tu generoso alojamiento en Berlin el verano de 2009. Nunca lo olvidaré.

Fuera de mi trabajo, hay algunas personas que siempre me han mantenido con los pies en la tierra en estos años. De algún modo, ellos también han contribuído en mi trabajo. Papá, Mamá, gracias por todo vuestro apoyo (incluído financiero) que me ha ayudado desde el principio hasta el fin en la universidad. Hermana, gracias por ser parte de mi sangre.

Y sobre todo, gracias, Ariana. Siempre has estado ahí para mí, lo estás, y espero que lo estés siempre.

Perdón si no nombro a todo el mundo, pero un gracias general a toda la gente con la que he estado en contacto de cualquier modo durante estos años.

Jose Vicente Galán. Valencia, 28 de Noviembre de 2010

Resumen

Interés de la investigación: Esta tesis trata de resolver el problema de la interconexión (acoplo) entre un circuito integrado fotónico de silicio (chip) y el mundo exterior, es decir una fibra óptica. Se trata de uno de los temas más importantes a los que hoy en día se enfrenta la comunidad científica en óptica integrada de silicio. A pesar de que pueden realizarse circuitos integrados fotónicos de silicio de muy alta calidad utilizando herramientas estándar de fabricación CMOS, la interfaz con la fibra óptica sigue siendo la fuente más importante de pérdidas, debido a la gran diferencia en el tamaño entre los modos de propagación de la fibra y de las guías de los circuitos integrados fotónicos. Abordar el problema es, por lo tanto, muy importante para poder utilizar los circuitos integrados fotónicos de silicio en una aplicación práctica.

Objetivos: El propósito de este trabajo es hacer frente a este problema en la interfaz del acoplamiento fibra-chip, con énfasis en el ensamblado o empaquetado final. Por lo tanto, los objetivos principales son: 1) estudio, modelado y optimización de diseños de diferentes técnicas eficientes de acoplamiento entre fibras ópticas y circuitos integrados fotónicos de silicio, 2) fabricación y demostración experimental de los diseños obtenidos, 3) ensamblado y empaquetado de algunos de los prototipos de acoplamiento fabricados.

Metodología: Este trabajo se desarrolla a lo largo de dos líneas de investigación, en conformidad con las dos principales estrategias de acoplamiento que pueden encontrarse en la literatura, concretamente, estructuras de acoplamiento tipo "*grating*" (la fibra acopla verticalmente sobre la superficie de circuito), y estructuras del tipo "*inverted taper*" (la fibra acopla horizontalmente por el extremo de circuito). El texto comienza con una introducción (capítulo uno), incluyendo la motivación y el contexto de la investigación, la definición del problema de acoplamiento fibra-circuito en fotónica de silicio, así como los objetivos y la organización del trabajo. El estado del arte de las dos estrategias de acoplamiento a investigar se incluye en el capítulo dos. Cada una de las estrategias (acopladores "*grating*" e "*inverted taper*"), se trata ampliamente en capítulos separados (capítulos tres y cuatro, respectivamente), incluyendo tanto el principio de funcionamiento del dispositivo, como el diseño y estrategia de fabricación

seguidos, así como resultados de las pruebas experimentales de diseños fabricados, con el fin de comprobar su validez. En el capítulo cinco, se tratan soluciones de empaquetado para ambas técnicas de acoplamiento fibra-chip desarrolladas, donde también se examina previamente el estado del arte de empaquetado de circuitos fotónicos de silicio. A tales efectos, el objetivo principal es el empaquetado de circuitos integrados fotónicos de silicio multipuerto basado en componentes disponibles comercialmente. En el último capítulo, se incluye un resumen y conclusión de los resultados obtenidos, así como las perspectivas de trabajo futuro.

Resultados: tanto en el caso de estructuras tipo "*grating*" como en el caso de estructuras "*inverted taper*", son importantes los avances conseguidos sobre el estado del arte. En lo que respecta al "*grating*", se ha demostrado dos tipos de estructuras. Por un lado, se ha demostrado "*gratings*" adecuados para acoplo a guías de silicio convencionales. Por otra parte, se ha demostrado por primera vez el funcionamiento de "*gratings*" para guías de silicio tipo "*slot*" horizontal, que son un tipo de guía muy prometedora para aplicaciones de óptica no lineal. En relación con el acoplamiento a través de "*inverted taper*", se ha demostrado una estructura novedosa basada en este tipo de acoplamiento. Con esta estructura, importantes son los avances conseguidos en el empaquetado de fibras ópticas con el circuito de silicio. Su innovadora integración con estructuras de tipo "*V-groove*" se presenta como un medio para alinear pasivamente conjuntos de múltiples fibras a un mismo circuito integrado fotónico. También, se estudia el empaquetado de conjuntos de múltiples fibras usando acopladores tipo "*grating*", resultando en un prototipo de empaquetado de reducido tamaño.

Resum

Interès de la investigació: Aquesta tesi tracta de resoldre el problema de la interconnexió (acoblament) entre un circuit integrat fotònic de silici (xip) y el món exterior, és dir, una fibra òptica monomode. Aquest és un del temes més importants als que s′enfronta hui en dia la comunitat científica en òptica integrada de silici. Tot i que es poden implementar circuits integrats fotònics de silici d′alta qualitat utilitzant ferramentes estàndard de fabricació CMOS, la interfície amb la fibra òptica continua sent la causa més important de pèrdues, degut a la gran diferència entre el tamany de la fibra òptica monomode i de les guies dels circuits integrats fotònics. El tractament del tema és, per tant, molt important per a la utilització dels circuits integrats fotònics en una aplicació pràctica.

Objetctius: L′objectiu d′aquest treball és fer front a aquest problema en el interfície fibra-xip, emfatitzant l′ensamblament o empaquetament final dels circuits. Per tant, els objectius principals són: 1) estudi, modelat i optimització dels dissenys de tècniques eficients d′acoblament entre fibres òptiques i circuits integrats fotònics de silici, 2) fabricació i demostració experimental dels dissenys obtinguts, 3) ensamblament i empaquetament d′alguns dels prototips d′acoblament fabricats.

Metodologia: Aquest treball es desenvolupa al voltant de dos línies, corresponents a les dos estratègies principals d′acoblament existents a la literatura: acoblament de llum verticalment sobre la superfície del circuit (estructura "grating coupler") i horitzontalment per la seua vora (estructura "inverted taper"). El manuscrit comença amb una introducció (capítol 1) que inclou la motivació i el context de la investigació, la definició del problema d′acoblament fibra-circuit en fotònica de silici i els objectius i organització del treball. L′estat de l′art de les dos estratègies d′acoblament s′inclou al capítol 2. Cadascuna de les estratègies (acoblador "grating" i "inverted taper") s′analitza àmpliament de manera separada als capítols 3 i 4 respectivament, incloent els principis de funcionament dels dispositius, fabricació, i els resultats de les proves experimentals de dissenys fabricats amb la finalitat de comprovar la seua validesa. Al capítol 5 s′estudien les solucions d′empaquetament per a les dos tècniques d′acoblament fibra-xip desenvolupades i s′examina l′estat de l′art d′empaquetament de circuits fotònics de

silici. A tals efectes, l'objectiu principal és l'empaquetament de circuits integrats fotònics de silici multiport basat en components disponibles comercialmet. A l'últim capítol, s'inclou un resum del resultats obtinguts, així com les perspectives de treball futur.

Resultats: Tant per al cas de "grating" com per a les estructures "inverted taper", són importants els avanços produïts sobre l'estat de l'art. Respecte al "grating", s'han demostrat dos tipus d'estructures. D'una banda, s'han demostrat "gratings" adequats per a l'acoblament a guies de silici convencionals. D'altra banda, s'ha demostrat per primera vegada el funcionament dels "gratings" per a guies de silici tipus "slot" horitzontal, que son guies molt prometedores per a aplicacions d'òptica no lineal. Respecte a l'acoblament amb "inverted taper", s'ha demostrat una estructura innovadora basada en aquest tipus d'acoblament. Amb aquesta estructura són importants els avanços aconseguits en relació amb l'empaquetament de fibres òptiques amb el circuit de silici. La integració amb estructures de tipus "V-groove" es presenta com una solució per a alinear passivament conjunts de múltiples fibres a un mateix circuit integrat fotònic. També s'estudia l'empaquetament de conjunts de múltiples fibres amb acobladors "grating", resultant un prototipus d'empaquetament de reduït tamany.

Preface

This work is on silicon photonics. It is about the manipulation of light or photons. Light that carries information all over the planet. Light for fiber-optic communication systems. Silicon photonics is the application of these photonic systems which use silicon as an optical medium. Silicon photonics is about the manipulation of light on sub-micron (even nano) scale devices for many applications, and so for communications in particular.

When I started my work at NTC as engineering student in 2005, the NTC was almost starting to research in the field, specially in the fiber-chip coupling topic. I had so the pleasure to continue researching on the field as a PhD student, under supervision of Pablo, to whom I am very grateful for that. In the past five years, silicon photonics research has become an active activity in the group, with at least ten people working on different research topics. Over the years, we have developed a thorough understanding of the intricacies of silicon photonics. This is one of the purposes of this book: to share these insights.

Many of the ideas here are a result of fruitful discussions with colleagues both from within the group and other research groups. At the risk of forgetting someone, I would like to mention a number of people by name.

Thank you Javier for giving me the opportunity to join the NTC, where I have met very nice and friendly people I will never forget during these almost five years. Thank you Alex for your last corrections of the thesis.

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Thank you to the promising packaging team it is coming consolidated at NTC: Giani, and recently Mercè. I hope we continue collaborating together for many years, specially regarding the alignment bench lab, where we will continue having great times.

This work would not have been possible without the hands of the fabrication team people at NTC in UPV, who, in order to get our experiments made, processed as many wafers as necessary, and spent all the time required. Thank you, Amadeu, Jose, Juan, Laurent, Paco, for you always good fabrication work and for your always helpful discussions on fabrication processes and methods. Also thank you to the facilites team, Alfredo, Luis, Antonio and Glenn, for making possible to "build" our almost new cleanroom place (remember, the cleanest place in Spain).

Also, the partners of the ePIXnet and HELIOS projects deserve a big thank you. Much of my work has been carried out in the framework of these projects, and without the collaborations, things would have been very different. Special thanks to our colleagues Lars and Tolga, to whom I met thanks to our collaboration within those projects. Thank you again Tolga for you kind hosting in Berlin during the summer of 2009. I will never forget it.

Outside of my work, there are some other people who have kept me on my feet in those years. In some ways, they have contributed to my work, too. Dad and Mom, thanks for all the support (including financial) that helped me through university. Sister, thank you for being part of my blood.

And most of all, thank you, Ariana. You were always there for me, still are, and I hope you will always be.

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Jose Vicente Galán

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Abstract

Research interest: This thesis deals with the interconnection (coupling) problem between a silicon photonic integrated circuit (chip) and the outside world, (i. e., a single mode fiber). This is one of the most important problems that the silicon integrated optics scientific community is facing nowadays. While very high quality silicon photonic integrated circuits can be realized using standard CMOS fabrication tools, the interface with the optical fiber remains the most important source of loss, due to the large difference in mode size between the single mode fiber and the waveguides on the photonic integrated circuits. Addressing the issues is therefore very important to apply silicon photonic integrated circuits in a practical application.

Objectives: The aim of this work is so to tackle this fiber-chip coupling interface problem, with an emphasis on the packaging. Thus, the main objectives are: 1) study, modelling and design optimization of efficient coupling techniques between optical fibers and silicon photonic integrated circuits, 2) fabrication and experimental demonstration of the obtained designs, 3) assembling and packaging of some of the fabricated coupling prototypes.

Methodology: This work develops along two investigation lines, in accordance with the two main strategies that can be found in literature, namely diffractive grating coupler structures (the fiber couples vertically onto the circuit surface) and inverted taper structures (horizontal fiber coupling onto the circuit end). The manuscript starts with an introduction (chapter one), including the motivation and research context, the definition of the fiber-chip coupling problem in silicon photonics, as well as the objectives and organization of the thesis. The state-of-the art of the two coupling strategies to be investigated is therefore included in chapter two. Each strategy (grating coupler and inverted taper) is then extensively discussed in a separate chapter (chapters three and four, respectively), including the device operation principle, the design and fabrication strategy followed, as well as experimental testing results of fabricated designs, in order to cross-check their validity. In chapter five, the packaging solutions based on both fiber-chip coupling techniques are discussed, where also briefly the

state-of-the-art of silicon photonic packaging is reviewed. Hereto, the main focus is multichannel silicon photonic integrated circuits and their packaging based on commercial available components. In last chapter, the achieved results are summarized and future perspectives are discussed.

Obtained results: Both in the case of diffractive grating couplers and in the case of inverted taper structures, important advances are made over the state-of-the-art. Concerning diffractive gratings, two types of structures have been demonstrated. On one hand, grating couplers suitable for conventional silicon waveguides have been achieved. On the other hand, diffractive grating structures are shown to work on horizontal slot waveguide structures for the first time, which are very promising for nonlinear optics applications. With regard to the coupling via inverted taper, a novel inverted taper-based structure is experimentally demonstrated. Using this structure, important advances are made in the packaging of optical fibers with the silicon waveguide circuit. Its innovative integration with V-groove structures is presented as a means to passively align arrays of fibers to a photonic integrated circuit. Also, packaging of fiber arrays using diffractive grating couplers is studied, resulting in a prototype of small form factor package.

List of Publications and Patents

Publications

Peer-reviewed Journals

Main contributions

J1. **J. V. Galan**, P. Sanchis, J. Martí, "Una técnica de acoplo eficiente entre fibra óptica y circuitos integrados ópticos de silicio," ITECKNE: Innovación e investigación en Ingeniería, vol. 4, pp. 51-54 (2007).

J2. **J. V. Galán**, P. Sanchis, G. Sánchez, and J. Martí, "Polarization insensitive low-loss coupling technique between SOI waveguides and high mode field diameter single-mode fibers," Opt. Express, vol. 15, no. 11, pp. 7058-7065 (2007).

J3. **J.V. Galan**, P. Sanchis, J. Blasco, A. Martinez, J. Marti, "High efficiency fiber coupling to silicon sandwiched slot waveguides," Optics Communications, vol. 281, no. 20, pp. 5173-5176 (2008).

J4. **J.V. Galan**, P. Sanchis, J. Blasco and J. Marti, "Study of High Efficiency Grating Couplers for Silicon-Based Horizontal Slot Waveguides," IEEE Photon. Technol. Lett., vol.20, no.12, pp.985-987 (2008).

J5. **J.V. Galan**, P. Sanchis, J. Blasco, A. Martinez, J. Marti, J.M. Fedeli, E. Jordana, P. Gautier, and M. Perrin, "Silicon sandwiched slot waveguide grating couplers," IEE Electron. Lett., vol. 45, p. 262 (2009).

J6. **Jose Vicente Galan**, Pablo Sanchis, Jaime Garcia, Javier Blasco, Alejandro Martinez, and Javier Martí, "Study of asymmetric silicon cross-slot waveguides for polarization diversity schemes," Appl. Opt., vol. 48, no. 14, pp. 2693-2696 (2009).

J7. **Jose Vicente Galan**, Tolga Tekin, Giovani B. Preve, Antoine Brimont and Pablo Sanchis, "Standard compatible packaging solution for silicon photonic integrated circuits with vertical coupling to fiber," submitted to IEEE J. Lightw. Technol. (2010).

J8. Experimental results on V-groove coupling (in progress, Optics Letters, 2010).

Other contributions

J9. P. Sanchis, **J. V. Galan**, A. Griol, J. Marti, M. A. Piqueras, J. M. Perdigues, "Low-Crosstalk in Silicon-On-Insulator Waveguide Crossings With Optimized-Angle," IEEE Photon. Technol. Lett., vol.19, no.20, pp.1583-1585 (2007).

J10. Pablo Sanchis, Pablo Villalba, Francisco Cuesta, Andreas Håkansson, Amadeu Griol, **José V. Galán**, Antoine Brimont, and Javier Martí, "Highly efficient crossing structure for silicon-on-insulator waveguides," Opt. Lett., vol. 34, no. 14, pp. 2760-2762 (2009).

J11. J. Palaci, G. E. Villanueva, **J. V. Galan**, J. Marti, B. Vidal, "Single Bandpass Photonic Microwave Filter Based on a Notch Ring Resonator," IEEE Photon. Technol. Lett., IEEE , vol.22, no.17, pp.1276-1278 (2010).

J12. Antoine Brimont, **Jose Vicente Galán**, Jose Maria Escalante, Javier Martí, and Pablo Sanchis, "Group-index engineering in silicon corrugated waveguides," Opt. Lett., vol. 35, no. 16, pp. 2708-2710 (2010).

J13. A. Martínez, J. Blasco, P. Sanchis, **J. V. Galán**, J. García-Rupérez, E. Jordana, P. Gautier, Y. Lebour, S. Hernndez, R. Guider, N. Daldosso, B. Garrido, J. M. Fedeli, L. Pavesi, J. Martí, "Ultrafast All-Optical Switching in a Silicon-Nanocrystal-Based Silicon Slot Waveguide at Telecom Wavelengths," Nano Letters, vol. 10, no. 4, pp. 1506-1511 (2010).

J14. J. Blasco, **J. V. Galán**, P. Sanchis, J. M. Martínez, A. Martínez, E. Jordana, J. M. Fedeli, J. Martí, "FWM in silicon nanocrystal-based sandwiched slot-waveguides," Optics communications, vol. 283, no. 3, pp. 435-437 (2010).

J15. Sara Mas, José Caraquitena, **José V. Galán**, Pablo Sanchis, and Javier Martí, "Tailoring the dispersion behavior of silicon nanophotonic slot waveguides," Opt. Express, vol. 18, pp. 20839-20844 (2010).

Conference Proceedings

Main contributions

C1. **J. V. Galán**, P. Sanchis and J. Martí, "Low-loss coupling technique between SOI waveguides and standard single-mode fibers," Proceedings of 13th European Conference on Integrated Optics, p. ThG11 (2007).

C2. **J. V. Galan**, P. Sanchis, B. Sanchez, J. Marti, "Polarization insensitive fiber to SOI waveguide experimental coupling technique integrated with a V-Groove structure," Proceedings of 4th IEEE International Conference on Group IV Photonics, pp. 110-112 (2007).

C3. **J. V. Galan**, P. Sanchis, J. Blasco and J. Marti, "Horizontal slot waveguide-based efficient fibercouplers suitable for silicon photonics," Proceedings of 14th European Conference on Integrated Optics, ThP16, pp. 248-250 (2008).

C4. **J. V. Galan**, J. Blasco, P. Sanchis, A. Martinez, J. Marti, J. M. Fedeli, E. Jordana, P. Gautier, M. Perrin, "Vertical grating couplers for silicon sandwiched slot waveguides," Proceedings of 5th IEEE International Conference on Group IV Photonics, pp. 105-107 (2008).

C5. **J. V. Galan**, P. Sanchis, J. Blasco, and J. Marti, "Broadband and highly efficient grating couplers for silicon-based horizontal slot waveguides," Proceedings of SPIE, vol. 6996, p. 69960Q (2008).

C6. P. Sanchis, **J. V. Galan**, A. Brimont, A. Griol, J. Hurtado and J. Marti, "High efficiency coupling in silicon photonic devices," Proceedings of Conferencia Espaola de Nanofotnica, pp. 45-46 (2008).

C7. A. Griol, J. Hurtado, **J. V. Galan**, P. Sanchis, G. Sanchez, J. Marti, G. Petersson, B. Nilsson and J. Halonen, "Experimental realization of a high efficient coupling technique for SOI devicesbased on inverted taper and V-groove integration"Proceedings of NanoSpain Conference (2008).

C8. A. Griol, J. Hurtado, **J. V. Galán**, P. Sanchis, J. A. Ayúcar, J. Martí;, "Physical implementation of an efficient coupling technique for SOI devices employing inverted tapers and V-groove integration," Proceedings of 34th International Conference on Micro and Nano Engineering, p. 560 (2008).

C9. **J. V. Galan**, A. Griol, J. Hurtado, P. Sanchis, G. B. Preve, A. Håkansson, J. Marti, "Packaging of silicon photonic devices: grating structures for high efficiency coupling and a solution for standard integration," Proceedings of 17th European Microelectronics and Packaging Conference, pp. 1-6 (2009).

C10. **J. V. Galan**, P. Sanchis, J. Marti, S. Marx, H. Schröder, B. Mukhopadhyay, T. Tekin, S. Selvaraja, W. Bogaerts, P. Dumon, L. Zimmermann, "CMOS compatible silicon etched V-grooves integrated with a SOI fiber coupling technique for enhancing fiber-to-chip alignment," Proceedings of 6th IEEE International Conference on Group IV Photonics, pp.148-150 (2009).

C11. **J. V. Galan**, P. Sanchis, J. Garcia, A. Martinez, J. Blasco, J. M. Martinez, A. Brimont, J. Marti, "Silicon cross-slot waveguides insensitive to polarization," Proceedings of IEEE LEOS Winter Topicals Meeting, pp. 32-33 (2009).

C12. **J. V. Galan**, M. Aamer, P. Sanchis, A. Griol, L. Bellieres, J. Ayucar, J. Marti, "A compact and broadband polarization splitter in SOI," Proceedings of 23rd Annual Meeting of the IEEE Photonics Society, pp.309-310 (2009).

C13. T. Tekin, L. Zimmermann, H. Schröder, P. Dumon, W. Bogaerts, **J. V. Galan**, P. Sanchis, W. Whelan-Curtin, D. Beggs. "Generic packaging concepts in the frame of network of excellence ePIXnet," Proceedings of SPIE, vol. 7604, p. 7604-17 (2010).

Other contributions

C14. P. Sanchis, **J. V. Galan**, A. Brimont, A. Griol, J. Marti, M. A. Piqueras, J. M. Perdigues, "Low-crosstalk in silicon-on-insulator waveguide crossings with optimized-angle," Proceedings of 4th IEEE International Conference on Group IV Photonics, pp. 159-161 (2007).

C15. R. Spano, **J. V. Galan**, P. Sanchis, A. Martinez, J. Marti, L. Pavesi, "Group velocity dispersion in horizontal slot waveguides filled by Si nanocrystals," Proceedings of 5th IEEE International Conference on Group IV Photonics, pp. 314-316 (2008).

C16. A. Brimont, P. Sanchis, **J. V. Galan**, J. M. Fedeli, A. M. Gutierrez, and J. Marti, "Experimental demonstration of moderately low group velocity in silicon rib photonic Wire Bragg Gratings," Proceedings of 23rd Annual Meeting of the IEEE Photonics Society, pp. 713-714 (2009).

C17. C. Garcia-Meca, M. Tung, **J. V. Galan**, R. Ortuno, F. J. Rodriguez-Fortuno, J. Marti, and A. Martinez, "Light compression without reflections," Proc. SPIE, vol. 7711, p. 771121 (2010).

C18. P. Sanchis, C. J. Oton, **J. V. Galan** and J. Marti, "High Q Microring Demultiplexer Filter for 60GHz Microwave Photonics Applications," Proceedings of 7th IEEE International Conference on Group IV Photonics, pp.84-86 (2010).

C19. S. Mas, J. Caraquitena, **J.V. Galán**, P. Sanchis, J. Martí, "Tailored chromatic dispersion in silicon-on-insulator slot waveguides," Proceedings of 15th European Conference on Integrated Optics, p. ThP28 (2010).

C20. Rakesh Sambaraju, **Jose Vicente Galan-Conejos**, Javier Herrera, Amadeu Griol, Claudio Oton, Pablo Sanchis, and Alejandro Martinez, "RF frequency transparent 90° hybrid based on silicon on insulator photonic circuit," Proceedings of SPIE, vol. 7719, p. 771914 (2010).

Meeting Abstracts

A1. **J. V. Galan**, P. Sanchis, W. Bogaerts, P. Dumon and L. Zimmermann, "V-Groove approach for inverted taper coupling in silicon photonics," ePIXnet Spring School on Technology for Photonics Integration, Elba island, Italy, 11-17 May (2008).

Patents

P1. **Jose Vicente Galán Conejos**, Giovanni Battista Preve, Pablo Sanchis Kilders, Javier Martí Sendra, G*ü*nter Lang, Sebastian Marx, Jan Krissler, Tolga Tekin, "CONCEPT AND APPARATUS OF PACKAGING SEVERAL PHOTONIC INTEGRATED CIRCUITS WITH VERTICAL FIBER COUPLING" (Spanish application P201031898, pending European extension).

Contents

Chapter 1

Introduction

The aim of this thesis is to tackle the fiber-chip coupling interface problem in silicon photonic technology. This chapter gives an introduction of the innate evolution from fiber optics to integrated photonics towards all-optical networks. Therefore, the main advantages of using silicon photonics are addressed. The fiber-to-chip coupling problem in silicon photonics is then introduced. Finally, we present the main objectives and the organization of this work.

1.1 Motivation and research context

Signal transmission and processing by means of optical beams rather than electrical currents or radio waves has been a very interesting topic since the 1960s [1]. Low loss, high data rate capabilities, noise rejection and electrical isolation are just a few of the important features that make fiber optic technology ideal for the transport of information in communication networks [2]. In current telecom and datacom network scenarios, the optical fibers are used to transport the information in the form of light from point A to point B, and is usually installed in the backbone and backhaul network[1], whilst copper wire or coaxial cable is

[1] In a hierarchical telecommunications network the backhaul portion of the network comprises the intermediate links between the core network, or backbone, of the network and the small subnetworks at the edge of the entire hierarchical network.

commonly used in the access network[1] for *last mile*[2] links. One reason is the relatively high cost to bring the fiber closer to the end user. However, these links are several kilometers long, and the fiber significantly outperforms copper and coaxial cables in this range. So, replacing at least part of these links with fiber shortens the remaining copper segments and allows them to run much faster. Following this approach, new emerging technologies such as FTTH (Fiber-To-The-Home)[3] started to arouse the interest of consolidated Telecom operators all over the world. The key objective was to be able to offer to the customers a higher speed and broadband access, by bringing the fiber link directly to their homes. An overview on FTTH technology standards and deployments is reported in [3]. Even in FTTH technology, the network equipment mainly remains electronic circuitry, and the optical signals are just used to transport the data, nor for data processing. So, in the network nodes, the routing and signal processing is performed electrically, and the electrical signal is converted back into light and sent on the output fiber and transport it towards the next node. These opto-electronic conversions cause an increase of the latency of the whole transport network, and the benefits of high velocity capability of using optical fibers is unfortunately wasted. This fact represents the real bottleneck in current communication networks. Current fiber-based networks use so electronic switching and are therefore limited to electronic speeds of a few gigabits per second. The most efficient way for making the most of optical fiber advantages is to replace microelectronic circuitry with optical circuits capable for all-optical signal processing. For enabling higher speeds up to terabit per second that support optical fiber, it is important that the signal remains in the photonic domain throughout its path. Such networks, which use optical switching and routing, are called all-optical. Fortunately, besides the main function of guiding light, optical fibers can also be developed as attractive photonic components performing desired optical signal

[1] An access network is that part of a communications network which connects subscribers to their immediate service provider.

[2] In telecommunications, the *last mile* or *last kilometer* is the final leg of delivering connectivity from a communications provider to a customer in the access network.

[3] $FTTH$ is a broadband network architecture that uses optical fiber to replace all or part of the usual metal local loop used for last mile telecommunications in which the fiber reaches the boundary of the living space, such as a box on the outside wall of a home.

processing, through corresponding modifications on the fiber core. For instance, very selective optical filters can be obtained by adding a periodic variation (or grating[1]) to the refractive index of the fiber core [4], and very good performance erbium doped fiber amplifier (EDFA) can be achieved by doping the fiber core with erbium material [5]. Moreover, more complex devices and systems can be obtained by combining several of those discrete single elements. However, optical fiber-based devices result in high cost and large discrete elements. The key to make more advanced and cheaper components is the integration of these optical components on a single chip. This integration should enable the replacement of the large racks of equipment used in the network nodes today by a few photonic chips. When the optical components are integrated on chip, we talk about photonic integrated circuits (PICs), and the term photonics is then used, as the realization of these photonic components deals with the manipulation of light or photons. Following same approach as in microelectronic devices, the commitment towards a process of photonic device integration and miniaturization has stirred up the interest of industry, and thereby integrated photonics emerges [6]. Hybrid technologies based on alloys of III-V compounds, such as indium phosphyde (InP) or gallium arsenide (GaAs), had initially a stronger impact for the development of PICs. The main reason was that it was easier to obtain light emitting sources with these materials, due to their direct fundamental energy bandgap compared to indirect bandgap of silicon at telecom wavelengths[2] [9,10]. The main objective in III-V photonics research has been to find a technology in which a variety of PICs can be easily fabricated in a generic foundry process. This concept is well known in silicon microelectronics, but in III-V photonics it was new and lead to a high cost technology development. As happend with silicon microelectronics, photonic technology to the mass market may happen only if one can bring high volume manufacturing at low cost. It was possible because microelectronic integration processes support the integration of a set of basic building blocks, which make possible more complex circuits by simple interconnection between them,

[1] Also known as Fiber Bragg Grating (FBG).

[2] Although first electro-optical free carrier injection laser prototypes have recently been achieved in silicon technology [7], electrically pumped pure silicon-based lasers continue being the Holy Grail in silicon photonics [8]

but was not initially a trivial task in III-V photonics. So, the idea of using silicon and its mature technologic platform for developing photonics started to make sense driven by the increasing demand for low-cost mass-production [11].

1.2 Silicon Photonics

The leading motivation in favor of silicon photonic technology is that it aims to achieve a compact convergence between photonics and electronics. The directions are to use silicon, which has been the base material for electronic circuits, to replace the various non-silicon materials currently used to form optical devices and to integrate ultrasmall silicon optical circuits and silicon electronic circuits on the same chip. The use of silicon lets us utilize the advanced planar mass-production facilities that have enabled the low-cost production of electronic circuits (i. e. mature silicon complementary metal-oxide semiconductor (CMOS) microelectronic manufacturing). Therefore, it is expected to provide an economical benefit by achieving advanced functionality in optical devices that support the network at a lower cost. It is also expected to minimize the total power consumption in network systems through the development of photonic-electronic convergence equipment that consumes less power while achieving even more advanced functionality. Fig. 1.1 depicts a graph summarizing the silicon photonics industry direction towards a photonic-electronic convergence by courtesy of *NTT Microsystem Integration Laboratories*[1] [12]. Moreover, the possibility for getting high-quality and cheap Silicon-on-Insulator (SOI) wafers makes the motivation more attractive. With the availability of platforms like SOI technology, creating planar waveguide circuits becomes even more feasible. An example of a commercial $8''$ SOI wafer is illustrated in Fig. 1.2(a). Fig. 1.2(b) depicts a schematic of a conventional strip SOI waveguide showing the SOI wafer layerstack and its main layer thickness values. The strong light confinement in SOI, given by the high index contrast between silicon core ($n = 3.48$ at $\lambda = 1550nm$) and silicon dioxide (SiO_2) ($n = 1.45$ at $\lambda = 1550nm$), makes it feasible to scale photonic devices to the hundreds of nanometer level. Moreover, it is possible to reduce the minimum bending radius

[1] https://www.ntt-review.jp/archive/2010/201002.html

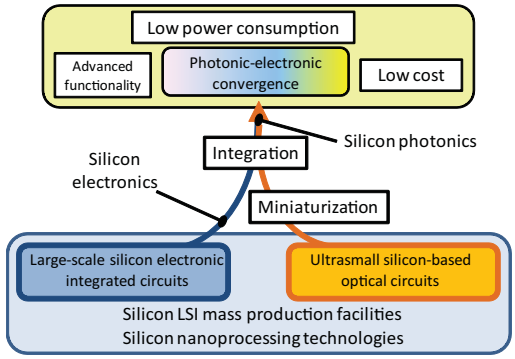
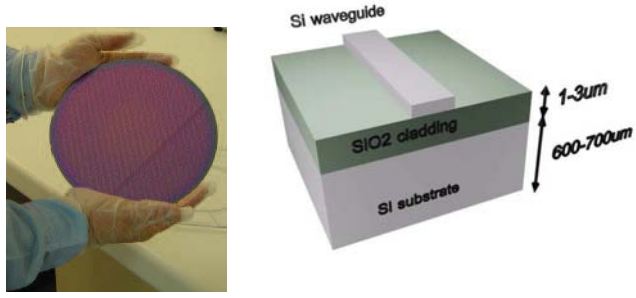


Figure 1.1: Silicon photonics industry direction towards a photonic-electronic convergence by courtesy of *NTT Microsystem Integration Laboratories* [12].



(a) (b)

Figure 1.2: (a) Commercial $8''$ *SOI* wafer. (b) Schematic of a *SOI* strip waveguide showing section layerstack of *SOI* wafers. The thickness of the silicon waveguiding layer is between 200 nm and 400 nm.

to the micrometre range, also offering the possibility of an ultra-high scale of integration of photonic circuits. This can so extremely decrease the cost of silicon devices. The most illustrative example of a compact device in SOI platform is a ring resonator. Fig. 1.3 depicts an atomic force microscope (AFM) image of a $5\mu m$ diameter SOI ring resonator based on singlemode SOI waveguides with 500 nm $\times$ 220 nm cross-section dimension. Small waveguides with small bending

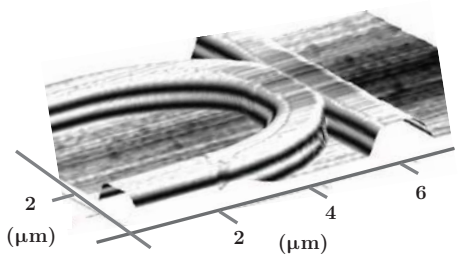


Figure 1.3: AFM image of a $5\mu m$ diameter SOI ring resonator based on strip waveguides with 500 nm $\times$ 250 nm cross section dimension.

radii can improve the characteristics of basic photonic devices such as modulators and optical filters [13, 14]. Moreover, such small waveguides can realise an ultra-high optical power density, which can be as much as 1000 times that in a conventional singlemode fiber, enhancing nonlinear optical effects in chipscale devices [15]. This interesting outcome has enabled important features, such as optical amplification [16], Raman lasing [17], all optical switching [18] and wavelength conversion [19], among others; functions that until recently were perceived to be beyond the reach of silicon. Novel potential applications even beyond optical communications have so emerged, such as environmental monitoring, imaging, biomedicine, spectroscopy, lab-on-a-chip, and optical logic, among others [20].

1.2.1 The fiber-to-chip coupling problem

Conventional singlemode SOI strip waveguides are about 220 nm thick and 500 nm wide. Because of their small dimensions, and also because the related fabrication tolerances are in the nanometer range, we use the term nanophotonic[1] waveguides. However, standard singlemode fibers (SMF) are very large size compared to nanophotonic SOI waveguides. Typical core diameter size of a standard

[1]Nanophotonics or Nano-optics is the study of the behavior of light on the nanometer scale. It is considered as a branch of optical engineering which deals with optics, or the interaction of light with particles or substances, at deeply subwavelength length scales. The study of nanophotonics involves two broad themes: studying the novel properties of light at the nanometer scale and enabling highly power efficient devices for engineering applications.

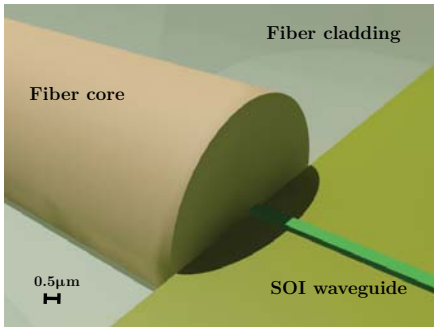


Figure 1.4: The fiber-to-chip coupling problem. Optical fiber and nanophotonic SOI waveguide drawn on same scale.

SMF is about $8\mu m$. Thus, injecting (coupling) light from an optical fiber to a nanophotonic waveguide becomes a difficult task. This is depicted in Fig. 1.4, where an optical fiber and a nanophotonic SOI waveguide are drawn on same scale. The high difference in the dimensions between the fiber and the waveguide causes a high mismatch between their optical modes. Due to this mismatch, a coupling structure is needed to adapt a wide fiber to a narrow silicon waveguide improving the coupling loss. Typically, a direct butt coupling between a single-mode fiber (mode field diameter MFD=10 μm) and a nanophotonic waveguide (MFD <1 μm) leads to more than 20dB insertion (coupling) loss. The insertion loss between an optical fiber and a nanophotonic circuit is definitively a big issue as it is directly linked with performances such as the link reach, the signalling rate, the receiver sensitivity, and so on. Moreover, in order to be compatible with functions for FTTH or wavelength division multiplexing (WDM) applications for instance, a good coupling structure is also required to be broadband and polarization insensitive. Finally, considering the packaging cost, the footprint of a coupling structure must be kept small and have sufficient alignment tolerances.

To solve the fiber-chip coupling problem, two main strategies have appeared in literature, depending on the physical direction in which the fiber is coupled to the PIC: vertical and lateral (horizontal) coupling techniques. So, this work

develops along these two lines, in accordance with the literature.

1.3 Objectives and organization of this work

The basic objective of the work reported on this thesis is to develop efficient fiber-to-chip coupling techniques in SOI technology. To achieve this objective, we will mainly focus on the study of the fiber coupling problem in SOI waveguides, by designing efficient vertical and lateral coupling structures. Hence, the final goal of this work is the experimental realization of the studied coupling techniques. To carry out this study, we first need to understand the performance of SOI waveguides, as well as their coupling issues to these vertical and horizontal coupling techniques. Second, the ability for electromagnetic modelling of the photonic structures involved is also needed. Once modelling and design optimization in finished, the designs will be fabricated using standard CMOS fabrication tools, in order to crosscheck experimental and theoretical results. We will also apply the studied coupling techniques to other kinds of waveguiding structures in silicon, such as slot waveguides. Finally, after successing in the realization of these coupling techniques prototypes, the assembly and packaging of some of the developed practical examples will be done, as an starting point for functional SOI chips for practical applications. Our main researching tasks are so described as follows:

1. Study, modeling and design optimization of efficient vertical coupling techniques between optical fibers and silicon photonic integrated circuits.

2. Study, modeling and design optimization of efficient horizontal coupling techniques between optical fibers and silicon photonic integrated circuits.

3. Apply the studied techniques to other kinds of silicon waveguides (i. e., slot waveguides).

4. Fabrication and experimental demonstration of the obtained designs.

5. Assemble and package of some of the developed coupling prototypes.

To reach the score objectives, this work is organized as follows: Chapter 2 gives an overview on the background of silicon nanophotonic waveguides, and the coupling to fiber problem is discussed. A summary of the state-of-the art of the already existing solutions for an efficient coupling to fiber is presented. The polarization problem is also explained. Novel kinds of silicon slot waveguides are also introduced. Chapter 3 deals with vertical coupling techniques. As we will focus on grating coupler-based structures, design, modelling as well as fabrication and characterisation results of grating-based fiber couplers are included. We also include here slot-waveguide based grating couplers for coupling to silicon slot waveguides. Chapter 4 deals with lateral (horizontal) coupling techniques. As we will focus on inverted taper-based structures, design, modelling as well as fabrication and characterisation issues of inverted taper-based fiber couplers are included. We also include here slot waveguide-based inverted taper couplers for coupling to silicon slot waveguides. Chapter 5 is focused on packaging solutions of our coupling approaches. A generic packaging solution for multiport grating coupler silicon photonic devices is studied in detail. As a result, s demonstrator prototype based on this packaging approach is achieved. Finally, in chapter 6 we present our main conclusions and perspectives for future work.

Chapter 2

Background

The aim of this thesis was introduced in chapter one by bringing into context the fiber-to-chip coupling problem in silicon photonics. Before starting to tackle the problem, this second chapter encloses the background and state-of-the-art. Subsequently, our work contributions will be introduced in the consecutive chapters.

2.1 Photonic Waveguides

The essential building block of a PIC is a waveguide. A waveguide plays a double role in a PIC. On one hand, the components on the PIC are linked to each other by means of waveguides. On the other hand, an access waveguide acts as the interface between the PIC and the outside world. Most of the optical waveguides used in communications are singlemode: they support only one guided mode for each polarization. For taking the most of the strong light confinement in silicon photonic technology, such as SOI platform, the SOI nanophotonic strip waveguide (or silicon nanowire) is the most attractive waveguiding structure, as its cross-section dimension is in the nanometer range.

2.1.1 SOI nanophotonic waveguides

SOI nanophotonic waveguides will make it possible to integrate a lot of functions on one chip, thus enabling important cost reductions. Fig. 2.1(a) depicts the cross-section drawing of an asymmetric strip SOI nanophotonic waveguide

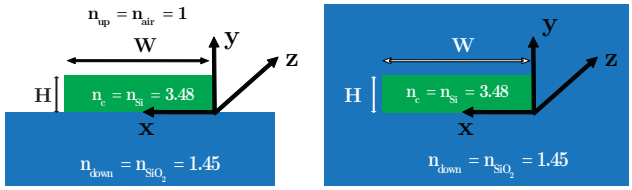
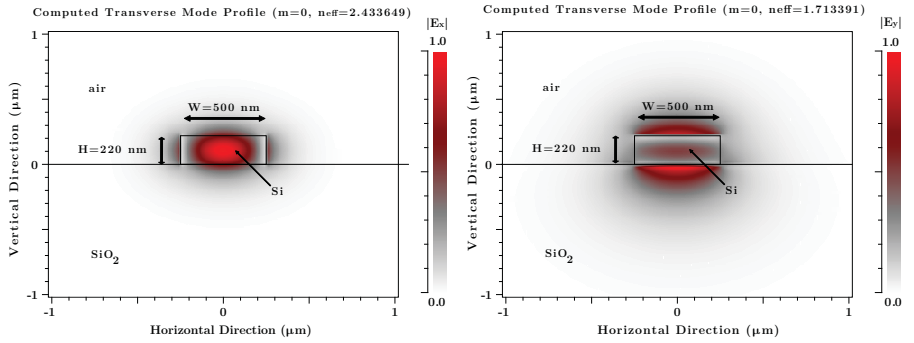


Figure 2.1: (a) Asymmetric and (b) symmetric SOI nanophotonic waveguides.

(shallow etch[1]), which is covered by air (air refractive index: n_{up} =n_{air} = 1), as well as Fig. 2.1(b) depicts the cross-section drawing of a symmetric SOI strip waveguide which is covered by SiO_2 (SiO_2 refractive index: n_{down} =n_{SiO_2} = 1.45 @ $\lambda = 1.55\mu m$). The refractive index of the waveguide silicon core is also shown in Figs. 2.1(a) and 2.1(b), and is equal to n_c =n_{Si} = 3.48 @ $\lambda = 1.55\mu m$. The waveguide width is W, and the waveguide thickness is H in both cases. Propagation direction is along the z-axis, and (x,y) axis are with the cross-section of the waveguide, according to axis definition of Fig. 2.1. For propagation by total internal reflection (TIR) in the waveguide core, we have $n_c > n_{up}$ and $n_c > n_{down}$. Multimode waveguides are undesirable in SOI circuits, as their performance can be compromised by the presence of multiple modes, causing undesirable effects such as intermodal dispersion or optical signal distorsion, among others. Singlemode condition in these kinds of waveguides basically depends on both boundary conditions (polarization state of light, and waveguide material refractive indices) and waveguide dimensions. Regarding the waveguide height (H), and considering commercial SOI wafers, typical values are H = 200 nm, H = 220 nm, and H = 250 nm. To achieve SOI singlemode waveguides, typical width value is W = 500 nm and W = 450 for asymmetric and symmetric waveguides, respectively [21].

Figs. 2.2(a) and 2.2(b) respectively depict the Transverse Electric (TE) and the Transverse Magnetic (TM) electric field profiles ($|E_x|$ and $|E_y|$, respectively)

[1]When just the silicon is etched, we call the waveguide shallow etch, as well as the waveguide is called deep etch wire when also the oxide is etched. Shallow etch wires are desirable because the wire losses without oxide etch are much lower [21].



(a) (b)

Figure 2.2: Electric field profile for (a) the TE ($|E_x|$) and (b) the TM ($|E_y|$) fundamental modes of asymmetric SOI waveguide @ $\lambda = 1.55\mu m$.

of the optical mode of a 500 nm wide singlemode asymmetric SOI waveguide for $H = 220$ nm and $\lambda = 1.55$ μm. For the calculation of the modes in Fig. 2.2 we have used a full-vectorial mode solver based on the Beam Propagation Method (BPM). As in three dimensional (3D) structures do not exist exact solutions for pure orthogonal TE and TM modes when solving the wave equation, they are respectively referred in literature as TE-like and TM-like modes. Simplifying, we will just name them here as TE and TM. In Fig. 2.2, we can see that a stronger confinement in the waveguide core is obtained for the TE mode, compared to the TM one. It can also be corroborated by obtaining a higher mode effective index (n_{eff}) for the case of TE polarization (see Fig. 2.2). The effective index of an optical mode (n_{eff}) is related to its propagation constant (β) according to the following equation [22]:

$$\beta = k_0 n_{eff} \tag{2.1}$$

where $k_0 = 2\pi/\lambda$ is the wave number in vacuum. Assuming that $n_c > n_{up}$, $n_c > n_{down}$ and $n_{up} \leq n_{down}$, we have $k_0 n_{up} \leq k_0 n_{down} < \beta < k_0 n_c$, and, consequently, $n_{up} \leq n_{down} < n_{eff} < n_c$ for the guided modes in the waveguide. So, as $n_{eff,TE} \neq n_{eff,TM}$, we have $\beta_{TE} \neq \beta_{TM}$, and the SOI waveguides are strongly polarization dependent, and a strongly birefringent medium. This high birefringence can

cause a polarization beating between TE and TM modes, thus confusing the polarization. Due to a stronger confinement of the TE mode, most existing SOI devices work with TE polarization. So, the polarization should be controlled externally in order to assure the propagation of the TE fundamental mode, also minimizing the TM mode propagation in the waveguide, and so the polarization beating effect.

2.1.1.1 Polarization: polarization transparency

Regarding the polarization in the waveguides, when both TE and TM modes propagate in the waveguide, we can define the birefringence parameter (B) as [23]:

$$B = \frac{2\pi\delta n}{\lambda_0} \tag{2.2}$$

where λ_0 is the free space wavelength, and $\delta n = n_{eff,TE} - n_{eff,TM}$ is the difference between the effective indices of the optical modes of each polarization. The waveguide length for 2π polarization rotation is definded as the beating length and is expressed as [23]:

$$L_p = \frac{2\pi}{B} \tag{2.3}$$

So, the waveguide length for $\pi/2$ polarization rotation can be defined as $L_p/4$, and it corresponds to the waveguide length in which TE and TM polaritations (orthogonals) are 90 degrees rotated, thus confusing them. For the effective indices obtained in Fig. 2.2 for the asymmetric 500 nm wide SOI waveguide and $\lambda = 1.55\mu m$, we obtain $B = 2.92 rad/\mu m$, and $L_p/4 = 0.538\mu m$. So, in just a 538 nm short distance, each polarization has rotated 90 degrees and may be confused with its orthogonal polarization. Hence, a control of the polarization of light has to be implemented externally in every SOI circuit.

A more elegant solution for transparency to polarization in SOI devices is the implementation of polarization diversity schemes [24]. One example of a polarization diversity circuit is shown in Fig. 2.3. Light coming from the input fiber (with random polarization) is launched into the circuit and then splitted in two orthogonal polarizations (TE and TM) using a polarization splitter component. The TM arm is also TE rotated by using a polarization rotator component.

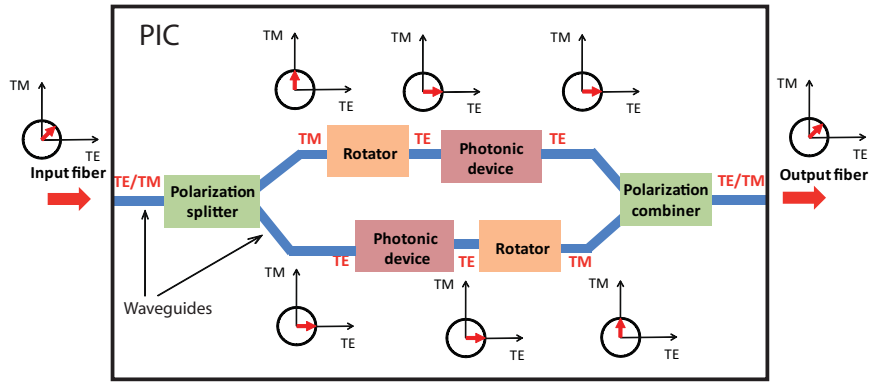


Figure 2.3: Example of polarization diversity circuit in silicon photonics [24]. The polarization state of light is shown along the circuit.

Then, by duplicating same photonic device in both arms, just TE polarization interacts with the devices, which are previously optimized for optimum TE polarization performance. At the output of the polarization diversity circuit, same configuration as at the input is implemented for rotating the other arm, combine them by using a polarization combiner, which is equal to the input splitter, and finally coupled into the output fiber. Recently, we have experimentally demonstrated very compact and broadband SOI polarization splitters less than 5 μm long [25]. Regarding polarization rotators in SOI, slanted angle [26] and triangular waveguide [27] based devices have been proposed in literature for better rotating the optical axis of the modes. However, fabrication of such devices is not trivial, as their physical geometry is not compatible with planar fabrication proceses. Novel planar-compatible devices based on the breaking symmetry of an almost square waveguide also recently appeared in literature [28]. The problem continues being the fabrication tolerances of such devices, and postcompensation methods are required by modifying the reflractive index of the upper cladding layer for achieving the rotation efficiently [28]. Polarization rotators are so the most difficult building block device in polarization diversity schemes.

For an efficient implementation of a polarization diversity scheme in SOI, efficient fiber-to-chip coupling structures insensitive to polarization are required for light coupling into the waveguides in the access ports of the polarization

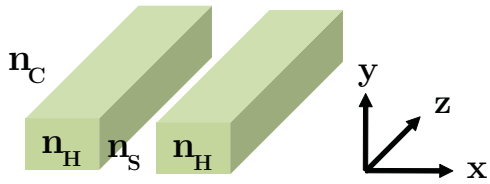


Figure 2.4: Schematic of a slot-waveguide [29, 30]. Light propagates along the z-direction.

diversity circuit in Fig. 2.3. So, the fiber-to-chip coupling problem is strongly linked to the polarization problem for transparency to polarization purposes in SOI devices.

2.1.2 SOI slot waveguides

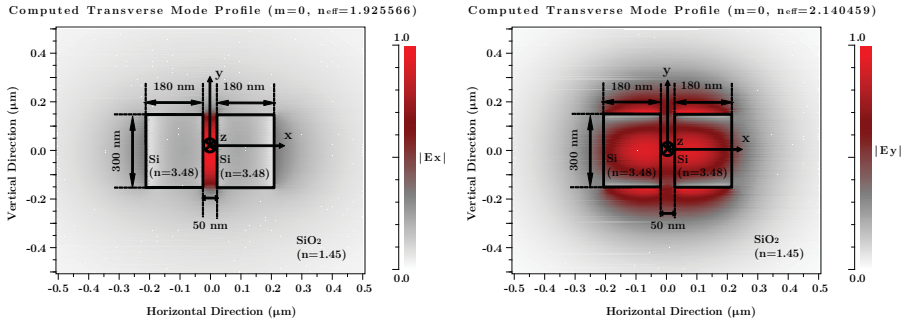
A slot-waveguide [29, 30] is a waveguide that guides strongly confined light in a subwavelength-scale low refractive index region by TIR. A slot-waveguide (see Fig. 2.4) consists of two strips or slabs of high-refractive-index (n_H) materials separated by a subwavelength-scale low-refractive-index (n_S) slot region and surrounded by low-refractive-index (n_C) cladding materials. This kind of waveguide is also called vertical slot waveguide.

The principle of operation of a slot-waveguide is based on the discontinuity of the electric field (E) at high-refractive index contrast interfaces. Maxwell equations state that, to satisfy the continuity of the normal component of the electric displacement field (D) at an interface, the corresponding E-field must undergo a discontinuity with higher amplitude in the low refractive index side. That is, at an interface between two regions of dielectric constants ϵ_S and ϵ_H, respectively [29]:

$$D_S^N = D_H^N \tag{2.4}$$

$$\varepsilon_S E_S^N = \varepsilon_H E_H^N \tag{2.5}$$

$$n_S^2 E_S^N = n_H^2 E_H^N \tag{2.6}$$



(a) (b)

Figure 2.5: E-field distribution of the fundamental mode in a SOI slot waveguide @ λ=1.55 μm and for (a) TE and (b) TM polarizations.

where the superscript N indicates the normal components of $\vec{D}$ and $\vec{E}$ vector fields. Thus, if $n_S << n_H$, then $E_S^N >> E_H^N$. Given that the slot critical dimension (distance between the high-index slabs or strips) is comparable to the exponential decay length of the fundamental eigenmode of the guided-wave structure, the resulting E-field normal to the high-index-contrast interfaces is enhanced in the slot and remains high across it. The power density in the slot is much higher than that in the high-index regions. Since wave propagation is due to TIR, there is no interference effect involved and the slot-structure exhibits very low wavelength sensitivity [29]. Figs. 2.5(a) and 2.5(b) depict the E-field distribution of the fundamental mode in a SOI slot waveguide with a SiO_2 filled 50 nm wide slot region for TE and TM polarizations, respectively, and an operating wavelength λ=1.55 μm. For the calculation of the modes in Fig. 2.5 we have used a full-vectorial mode solver based on the BPM. Waveguide dimensions are also depicted in both figures. Strong confinement in the slot region is just with Fig. 2.5(a), in which major E-field component is parallel to the x-axis (TE polarization). Fig. 2.6 depicts a horizontal cut at $y = 0$ of the E-field distribution profile in the slot waveguide for TE polarization, better showing the strong E-field intensity in the slot region.

Multiple slot regions in the same guided-wave structure (multi-slot waveguide) have also been proposed in order to increase the optical field in the low-refractive-

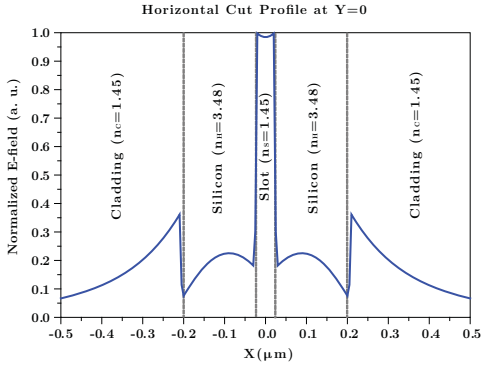


Figure 2.6: Horizontal cut at $y = 0$ of the E-field distribution in Fig. 2.5(a).

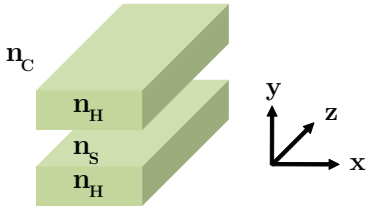


Figure 2.7: Schematic of a sandwiched slot waveguide [33]. Light propagates in the z-direction.

index regions [31,32]. For achieving a strong confinement in the slot region for TM polarization, sandwiched (horizontal) slot waveguides have also been implemented in literature [33]. Fig 2.7 depicts an schematic of a sandwiched slot waveguide. Due to the 90 degrees rotation compared to slot waveguide in Fig. 2.4, the strong confinement in the slot region is now with TM polarization. Fig 2.8 depicts the E-field distribution of the fundamental mode in a SOI horizontal slot waveguide @ λ=1.55 μm and for TM polarization, calculated via 3D-BPM based full-vectorial mode solver simulations. Compared to vertical slot waveguides, fabrication of sandwiched slot waveguides is easier, as its sandwiched geometry allows to use industrial microelectronic fabrication tools, especially deep-UV lithography [34].

A slot-waveguide produces high E-field amplitude, optical power, and optical intensity in low-index materials at levels that cannot be achieved with conventional waveguides. This property allows highly efficient interaction between

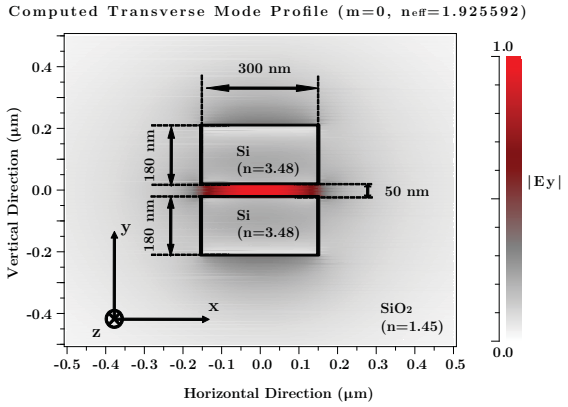


Figure 2.8: E-field distribution of the fundamental mode in a SOI slot waveguide @ λ=1.55 μm and for TM polarization.

fields and active materials, which may lead to all-optical switching [35], optical amplification [36] and optical detection [37] on integrated photonics. As firstly pointed out in [29], the slot waveguide can be used to greatly increase the sensitivity of compact optical sensing devices ([38]– [41]) or to enhance the efficiency of near-field optics probes. Strong E-field confinement can be localized in a nanometer-scale low-index region. This can so efficiently exploited in such nonlinear applications, where the change of the refractive index (Δn) of the slot material due to the Kerr effect[1] can be modelled as [42]:

$$\Delta n = 2n_2 I \tag{2.7}$$

where n_2 is the nonlinear refractive index and I is the optical intensity, which can also be expressed as [42]:

$$I = \frac{P}{A_{eff}} \tag{2.8}$$

where P is the optical power and A_{eff} is the effective area. So, the only way for achieving an increase in Δn is to increase either n_2 or I, which is also equivalent

[1]The Kerr effect, also called the quadratic electro-optic effect, is a change in the refractive index of a material in response to an applied electric field. The Kerr effect is distinct from the Pockels effect in that the induced index change is directly proportional to the square of the electric field instead of varying linearly with it.

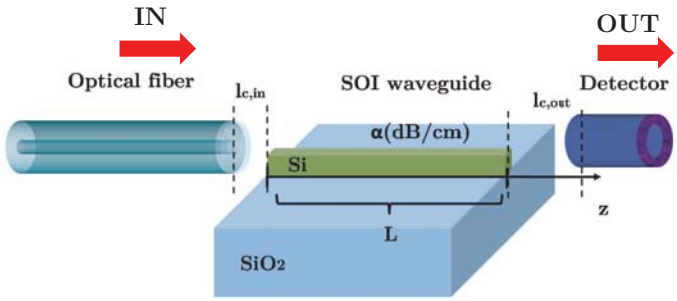


Figure 2.9: Schematic for loss contribution in SOI waveguides.

to reduce A_{eff} for a given optical power, according to Eq. 2.8. Thus, due to light strong confinement in a lower nanometer sized region, the slot waveguide can achieve a stronger nonlinear Kerr effect compared to conventional SOI waveguides. Moreover, if the slot is filled with a nonlinear material with higher n_2, the nonlinear effect can be even stronger. Recently, silicon nanocrystals (Si-nc) embedded in SiO_2 has demonstrated very promising characteristics for nonlinear applications [43]. Its Kerr coefficient is approximately two orders of magnitude higher than in silicon [44]. Design of slot waveguides filled with Si-nc/SiO_2 material for optimum nonlinear performance is presented in [45]. Recently, we experimentally demonstrated all-optical switching at telecom wavelengths in a horizontal silicon slot waveguide-based ring resonator filled with highly nonlinear Si-nc/SiO_2 [46]. We also proposed silicon cross-slot waveguides insensitive to polarization, which are also suitable for the implementation of the access waveguides in polarization diversity schemes in slot waveguide based devices [47, 48].

2.1.3 Coupling to optical fiber

When the light coming from an optical fiber with power P_{in} is launched into a SOI waveguide, output detected power (P_{out}) can be expressed as (see Fig. 2.9):

$$P_{out}(mW) = P_{in}(mW) \cdot \eta_{c,in} \cdot \eta_{c,out} \cdot e^{-\alpha(Np/cm)\cdot L(cm)} \tag{2.9}$$

where $\eta_{c,in}$, $\eta_{c,out}$ are the input and output insertion (coupling) factors or coupling efficiencies ($0 \leq \eta_c \leq 1$), respectively, L is the waveguide length expressed in cm,

and α is waveguide propagation loss, which is expressed in Np/cm. Eq. 2.9 can also be expressed in the following logarithm form:

$$P_{out}(dBm) = P_{in}(dBm) - L_{c,in}(dB) - L_{c,out}(dB) - \alpha(dB/cm) \cdot L(cm) \quad (2.10)$$

where $L_{c,in}$ and $L_{c,out}$ are the input and output coupling losses, respectively, and $\alpha(dB/cm)$ are the waveguide propagation losses, expressed in dB/cm. The relation between Np/cm and dB/cm is (for power units):

$$\alpha(dB/cm) = 10\log_{10}e \cdot \alpha(Np/cm) \approx 4.34 \cdot \alpha(Np/cm) \quad (2.11)$$

as well as coupling efficiencies are related to coupling loss by means of the expression:

$$L_c = -10\log_{10}(\eta_c) \quad (2.12)$$

The major cause for propagation loss in a SOI waveguide operating at λ=1.55 μm is the waveguide sidewall roughness, which is introduced by imperfections in the waveguide fabrication processes [49]. For obtaining low propagation loss below 1 dB/cm, very precise fabrication processes and very accurate lithography machinery are needed [50]. Novel strategies have recently been demonstrated for achieving ultra-low loss silicon waveguides fabricated without any silicon etching, achieving propagation loss downto 0.3 dB/cm [51].

The most important source of loss in SOI waveguides is so the coupling to the optical fiber. It is basically due to the large difference in both mode size and index contrast[1] between the singlemode fiber and the waveguide.

For evaluating the coupling loss factor due to difference in mode size between the fiber and the SOI waveguide, we can calculate the power overlap integral between the electric field profile of the fundamental mode in the fiber (E_f) and in the waveguide (E_{wg}) at the fiber-waveguide interface (i. e. the position $z = 0$) [22]:

$$\Gamma = \left(\frac{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} |E_{wg}(x,y,z=0)||E_f(x,y,z=0)|dxdy}{\sqrt{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} |E_{wg}(x,y,z=0)|^2 dxdy \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} |E_f(x,y,z=0)|^2 dxdy}} \right)^2 \quad (2.13)$$

[1]The index contrast is defined as $\Delta = \frac{n_{core}^2 - n_{cladding}^2}{2n_{core}^2}$ and is approximately equal to 0.36 % for the optical fiber, and to 40 % for the SOI waveguides.

where the denominator is simply a normalising factor. The factor Γ lies between 0 and 1, and therefore represents the range between no coupling and total coupling due to field overlap.

For evaluating the coupling loss factor due to impedance mismatching also due to the difference in the index contrast we can use the expression for the normal reflexion in a discontinuity between two materials [23]:

$$R = \left| \frac{n_{eff,f} - n_{eff,wg}}{n_{eff,f} + n_{eff,wg}} \right| \tag{2.14}$$

where $n_{eff,f}$ and $n_{eff,wg}$ are the fiber and waveguide fundamental mode effective indices, respectively.

Finally, power input coupling loss (L_c) taking into account both factors or terms, and so expressed in dB, is:

$$L_c(dB) = -10\log_{10}\Gamma - 10\log_{10}\left[(1-R)^2\right] \tag{2.15}$$

For solving Eq. 2.13, the electric field profile of the optical mode in the fiber (E_f) can be approximated by a Gaussian-like profile, according to the following expression [52]:

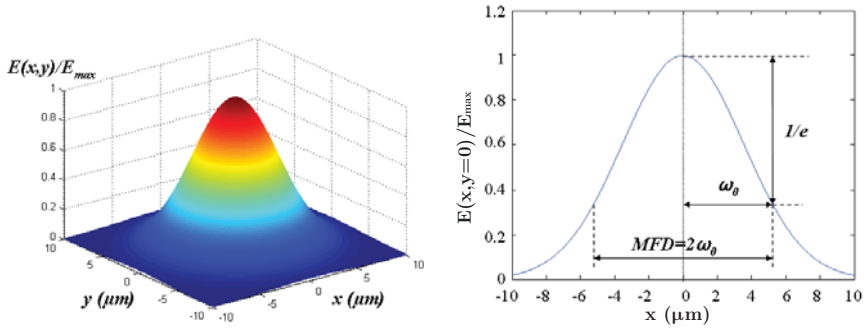
$$|E_f(x,y,z=0)| = E_{max} \cdot e^{-\left(\frac{x^2+y^2}{\omega_0^2}\right)} \tag{2.16}$$

where ω_0 is defined as the diameter of the beam for which the electric field amplitude has decayed to $(1/e)$ of its maximum value, E_{max}. The mode field diameter of an optical fiber (MFD) is related to ω_0 by means of [52]:

$$MFD = 2\omega_0 \tag{2.17}$$

Fig. 2.10(a) depicts the normalized electric field profile of a Gaussian beam for MFD=10 μm, corresponding to the MFD of a standard SMF. Fig. 2.10(b) depicts a transversal cut of the normalized electric field profile of the Gaussian beam for $y = 0$ graphically explaining the meaning of the parameters ω_0 and MFD.

Fig. 2.11 depicts theoretical results for the coupling losses @ λ=1550 nm and TE polarization between an optical fiber and a 500 nm $\times$ and 220 nm section SOI waveguide as a function of the fiber MFD, by solving Eq. 2.15. For calculating the



(a) (b)

Figure 2.10: (a) Normalized electric field profile of a gaussian beam with a MFD=10 μm, corresponding to the MFD value of an standard SMF. (b) Transversal cut of the Gaussian beam for $y = 0$ illustrating the meaning of the parameters ω_0 and MFD.

electric field profile of the SOI waveguide mode (E_{wg}) we used 3D BPM (BPM) simulations. We used $n_{eff,f}$=1.46 as the fundamental mode effective index for the optical fiber. Using also BPM simulations we computed $n_{eff,wg}$=2.43 as the fundamental mode effective index for the SOI waveguide, both for a wavelength λ=1.55 μm. As expected, the higher the fiber MFD, the higher the coupling losses are, as shown in Fig. 2.11. For a standard SMF (MFD=10 μm) we calculated more than 26.7 dB coupling losses, which of course is inacceptable. Furthermore, as results in Fig. 2.11 are per connection, if we consider both the input and output of our SOI chip fiber-connected, the total coupling losses of our SOI chip increase up to twice the coupling loss values calculated in Fig. 2.11. From Fig. 2.11 we can also see as coupling loss extremely decreases when optical fibers with lower MFD are used (i. e. MFD$\leq$2 μm). For instance, lensed fibers with a MFD downto 2.5 μm are commercially available[1]. However, as these kinds of fibers are made from a standard fiber which is lensed/tapered down, the MFD specified by the manufacurer is just assured in a short working distance, and they may present big problems while their alignment with the circuit. Moreover, these fibers are

[1] http://www.ozoptics.com/ALLNEW_PDF/DTS0080.pdf

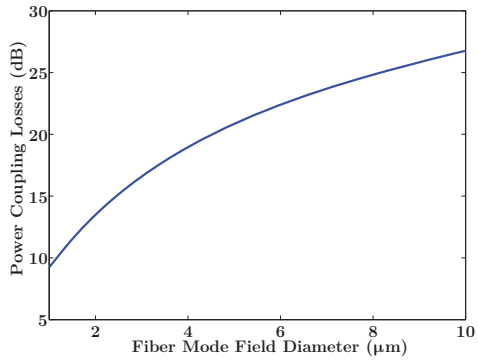


Figure 2.11: Butt-Coupling losses between an optical fiber and a 500 nm × 220 nm section SOI waveguide as a function of the fiber MFD @ λ=1550 nm and TE polarization, graphycally solving Eq. 2.15.

usually more expensive, and the use of standard SMF fibers is preferred.

Beside from the fact that high coupling losses are obtained when butt-coupling an optical fiber to a SOI waveguide, there exists another important fact to be considered in the coupling. Due to reflections in the fiber-waveguide coupling plane, the waveguide behaves as a Fabry-Perot cavity. So, when the light is injected into the waveguide, output optical intensity (I_o) is related to input intensity (I_i) according to the following well-known Fabry Perot formula [22]:

$$\frac{I_o}{I_i} = \frac{(1-R)^2 e^{-\alpha L}}{(1-R\cdot e^{-\alpha L})^2 + 4\cdot R\cdot e^{-\alpha L} sen^2(\varphi/2)} \tag{2.18}$$

where R is the reflection in the waveguide edges (assuming it is the same in the input as in the output), α is the waveguide propagation loss, L is the waveguide length, and φ is the phase difference between each succeeding reflection in the cavity, and is related to the wavelength (λ) by (for normal incidence) [22]:

$$\varphi = \left(\frac{2\pi}{\lambda}\right) 2nL \tag{2.19}$$

where n is the refractive index in the cavity. Fig. 2.12 illustrates the graphical solution of Eq. 2.18 as a function of λ for the case of $n = 2.8$ (corresponding

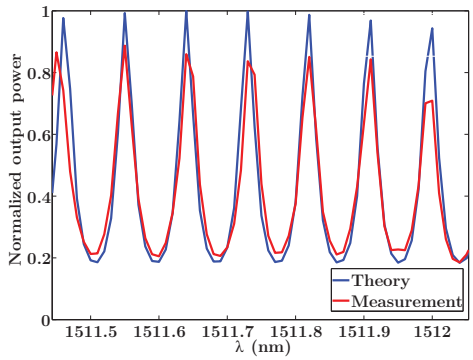


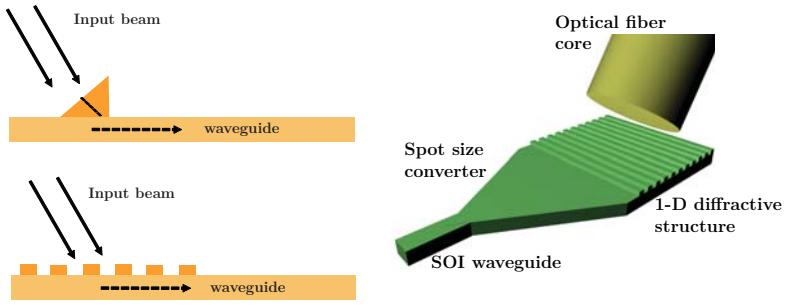
Figure 2.12: Theoretical and experimental results for the output power spectrum in a 3 μm wide and 4.58 mm long SOI waveguide.

to the effective index of the SOI 3-layer structure: air-silicon(200 nm thick)-SiO_2), R=0.4 (reflection between at air-silicon interface), L=4.58 mm and α=0.01 Np/cm. Fig. 2.12 depicts the experimental results for a 3 μm wide and 4.58 mm long SOI waveguide, obtaining propagation losses close to α=0.04 dB/cm. As shown in Fig. 2.12, normalized output power varies from 0.2 to 1 due to the interferences of multiple waves inside the cavity. The periodicity of the peaks of the spectrum in Fig. 2.12 strongly depends on the waveguide length. Maximum and minimum values of the peaks also depend on R as well as on α. This Fabry-Perot effect is undesirable in SOI circuits, as it may disguise the spectral response of our devices.

So, an efficient fiber-to-chip coupling structure will basically try to acomplish two main objectives. On one hand, it will try to decrease as much as possible the coupling losses between the optical fiber and the SOI access waveguide of the chip. On the other hand, it will try to overcome the Fabry-Perot resonance effect, thus trying to get a flat spectral response.

2.2 Efficient coupling to fiber in SOI waveguides

Many solutions to overcome an efficient fiber-to-chip coupling have been proposed, and keep appearing in literature, following one of these approaches: lateral cou-



(a) (b)

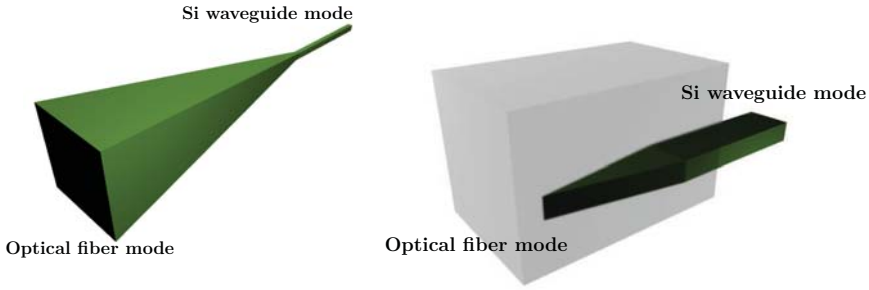
Figure 2.13: (a) Different vertical coupling techniques: prism coupling (up) and grating coupler (down) [22]. (b) Schematic of a SOI waveguide grating coupler [53].

pling (in-plane coupling) and vertical coupling (out-of-plane coupling).

2.2.1 Vertical coupling

In vertical coupling techniques, light is injected onto the surface of the waveguide at a specific angle. We call them vertical coupling techniques because the optical fiber is vertically placed over the waveguide. The most important vertical coupling techniques are the prism coupling and the grating coupler [22]. The principles of these coupling techniques are shown schematically in Fig. 2.13(a).

For the purposes of semiconductor waveguide evaluation, prism coupling is not particularly useful. The conditions of coupling are such that the material from which the prism is made should have a higher refractive index than the waveguide; this seriously restricts the possibilities, particularly for silicon which already has a relatively high refractive index. There are materials available, however, such as germanium which could be used, although other limitations mean that the technique is still inferior to alternative techniques. These limitations are that prism coupling can damage the surface of the waveguides, it is not suitable if a surface cladding is used, it is best suited to planar waveguides, and it is certainly not suited to material systems that utilise rib waveguides such as the silicon technology [22]. So, we will further focus on grating couplers as vertical



(a) (b)

Figure 2.14: (a) 3-D silicon Taper [54]. (b) 2-D single stage inverted silicon taper with polymer waveguide on top [55].

coupling technique. A grating coupler is basically a one dimensional (1D) diffractive structure that can be designed for coupling light onto the waveguide surface by means of one of its orders of diffraction. One of the pioneer grating coupler for efficiently coupling singlemode fibers to compact planar SOI waveguides was demonstrated for the first time in [53], and is illustrated in Fig. 2.13(b).

2.2.2 Lateral coupling

Lateral coupling involves shining light onto the end of the waveguide, and is also known in literature as end-fire or butt-coupling. As a direct butt-coupling between a standard SMF and a nanophotonic SOI waveguide means getting ultra high coupling loss (see Fig. 2.11), a solution for an efficient butt-coupling relies on the use of tapered spot size converters (SSC) [56]. A tapered spot-size converter (or taper) is a waveguide whose dimensions change along the propagation direction from chip to fiber, creating a transition from a small to a large mode. It is so able to convert the small size optical mode of the nanophotonic waveguide into a larger size optical mode, and vice-versa. If the transition is slow enough, the conversion is 100% efficient and the taper is called adiabatic. The most suitable theoretical solution to the waveguide-fiber mode conversion problem is a 3-D tapered waveguide, having increasing size both laterally and vertically in the direction chip-to-fiber (see Fig. 2.14(a)) [54]. Due to the high difference in size

between the optical modes of the fiber and the waveguide, such a taper should be on the order of several milimiters long. Moreover, the fabrication of such 3-D structure is rather complicated, as it is not compatible with planar CMOS mass-production processes. Another solution is based on the fact that the optical mode in the waveguide is expanding out from the core as the waveguide core gets smaller. So, a 3-D taper with decreasing dimensions both laterally and vertically along the waveguide-to-fiber direction (also known as inverted taper or inverse taper) is proposed [57]. Although shorter tapers can be obtained, fabrication of this structure is still beyond planar fabrication limits, as it still remains a so complicated 3D structure. Actually, no experimental results have been reported in literature. A more elegant solution which is planar geometry is a planar single stage inverted taper [55] (Fig. 2.14(b)). The nanophotonic waveguide is just tapered down laterally till its tip width is of the order of tens of nanometers. Thus, the mode is forced to get out of the silicon waveguide and starts propagating into another low-medium index contrast fiber-adapted waveguide which is placed over the silicon material (see Fig. 2.14(b)). Due to its planar geometry (constant height), this structure can be fabricated using conventional CMOS compatible machinery. The main drawback of this structure is the high lithography resolution needed for achieving such narrow inverted taper tip in many cases. When studying horizontal coupling techniques, we will so focus on single stage planar inverted taper-based structures.

2.2.3 Grating coupler vs Inverted taper

Table 2.1 summarizes the most relevant properties of the major SOI fiber coupling techniques (grating coupler and inverted taper) presented in literature [58], for a wavelength λ=1.55 μm, and considering standard singlemode fibers (SMF).

Typical coupling loss are about 5-6 dB for a conventional 1D grating coupler structure, with a footprint area of 10 μm $\times$ 10 μm, when coupling to a butt-fiber with 10 μm MFD [59]. For coupling via inverted taper by using the same fiber, a double stage coupling structure is usually used in literature, as a single stage is not enough for achieving an efficient mode conversion to 10 μm MFD standard butt-fibers. In double stage inverted taper structures, the mode conversion is

achieved in two different steps by using a bottom taper on top of a lower taper, thus creating a so complicated 3D structure. Typical coupling loss of 1.5 dB are achieved for a 800-1000 μm long double stage inverted taper, and a 9 μm $\times$ 9 μm cross-section dimension fiber-adapted waveguide [60, 61]. However, the complexity of the fabrication process is larger than doubled compared to the case of a single stage inverted taper coupler. In single stage inverted taper structures, the mode conversion is achieved with one less complex inverted taper structure in just one step (see Fig. 2.14(b)). Most of the inverted taper structures existing in literature are so single stage, but are optimized for coupling to lensed fibers with a lower spot size diameter of 2.5-4 μm. In this case, minimum coupling loss lower than 1 dB can be obtained. One of the pioneer inverted taper presented in literature is found in [55]. They demonstrate less than 1dB coupling loss from 0.3 μm $\times$ 0.3 μm square silicon waveguides to singlemode fibers with 4.3 μm MFD for the TE mode, for an inverted taper length of 200μm, and using a polymer fiber-adapted waveguide on top of the inverted taper with cross-section dimensions 3μm $\times$ 3μm. A insensitive to polarization behaviour of the structure is also observed for inverted taper tip width values below 40 nm. In order to decrease the taper length, in [62] it is proposed a novel configuration consisting of using a SiO_2 slab layer on top of a parabolic shape taper, insted of using a polymer waveguide. The optimal length of the taper is reduced to 40μm due to the quadratic shape of the taper, but achieveing a polarization dependency to the inverted taper tip width. 0.5dB coupling loss to 4.9μm MFD fibers are achieved for optimal desings with 120nm and 50nm tip width for TE and TM polarization, respectively. The main problem with this configuration is that the device is needed to be cleaved exactly by the inverted taper tip, and may require special cleaving and polishing techniques. In [63], such a coupler was fabricated using standard CMOS technology and an insertion loss of 1.9 dB to 2.5 μm MFD fibers was achieved for the TE mode, by using a 3μm $\times$ 1.3μm BCB type polymer waveguide on top. The optimal obtained length of the taper is 175μm, and the inverted taper tip width is 175nm, thus being compatible with CMOS UV lithography. In [64], the coupler is optimized for the TE mode and achieved a 0.5 dB insertion loss. In [65], a similar coupler for a silicon rib waveguide with a 0.7 dB coupling loss for TE mode is reported. Recently, the optimization

for inverted taper for TM mode has been proposed in [66], for the case of ridge waveguides. They obtain coupling losses of 0.36 dB and 0.66 dB for the TM and TE modes, respectively. However, extra excess loss are achieved mainly due to the fiber lensing process of the lensed fibers used, so that final average insertion loss of about 3 dB are obtained in many cases. A SOI polarization insensitive fiber-to-fiber coupler fabricated on a 200-mm wafer with the standard CMOS technology has also recently been demonstrated in literature, in which our Institute collaborated in the testing of the structures in context of the still ongoing EU-funded FP7-project HELIOS[1] [67]. Coupling losses from a 2.5μm MFD lensed fiber into a 500-nm-wide SOI waveguide were measured to be less than 1 dB in the 1520 nm to 1600 nm wavelength spectral range and below 3 dB between 1300 nm and 1600 nm. Table 2.2 shows a review of some of the most relevant inverted tapers existing in literature from different prestigious research groups.

With respect to grating couplers, coupling loss can be reduced downto 1 dB (near 80% coupling efficiency) by implementing more complex grating coupler designs. To obtain lower loss grating couplers, different strategies have been proposed in literature. By adding a bottom mirror to redirect the downward diffracted light to the waveguide coupled to the grating, coupling losses downto 1 dB can be obtained. This can be either a metallic mirror [68] or a distributed Bragg reflector-type (DBR) mirror [69]. Another possibility to decrease coupling loss downto 1 dB is to deposit a poly-silicon overlay over a non-uniform grating structure for increasing the grating direccionality, and then optimize the design parameters of the grating periods individually [70]. With this solution, a modification in the effective index along the grating is obtained by chirping the grating, so that the radiated electric field profile of the grating can be Gaussian-like reshaped for better matching to the optical fiber beam. A new generation of SOI fiber-to-chip grating couplers which use a silicon overlay to enhance the directionality and thereby the coupling efficiency has recently been presented [71].

[1]The mission of the large scale integrating project HELIOS is to make CMOS photonics accessible to a broad circle of users. During 4 years, the HELIOS consortium will develop innovative means to combine a photonic layer with a CMOS circuit, using microelectronics fabrication processes. See http://www.helios-project.eu

However, an advanced CMOS-compatible SOI platform is required for the fabrication of that kind of structures [71]. Another possibility for an efficient effective index modification of the grating coupler is the use of subwavelength waveguide gratings [72].

All the previous design configurations need for slightly tilting the optical fiber with respect to the grating normal direction to avoid a large second-order Bragg reflection back into the SOI waveguide, which dramatically increases coupling loss. This fact is important for practical applications, which implies either angled polished fibers or mounting the fiber holder under an angle with respect to the grating normal direction, which also implies to increase the final cost of the photonic component assembling and packaging [73]. To avoid this, slanted [74] and stratified [75] grating couplers were proposed to achieve low coupling loss for perfectly vertical coupling. The design of an asymmetric grating structure based on vertically etched slits has also been proposed in literature [76]. But implementing all these more complex grating designs is costly equivalent to have to develop more complex fabrication processes, thus increasing both the complexity of the designs and the fabrication process. In many cases, this is not suitable from an integration point of view [68, 69], and in some other cases the restrictions on the design parameters are beyond optical lithography limits [70, 76]. So, there is always a commitment between cost and optimum performance. Table 2.3 summarizes some relevant grating results reported in literature from several prestigious research groups. An important feature in grating couplers development is achieved by *Luxtera, Inc.* in the holographic lens type grating in [77]. They demonstrate a high efficiency structure, with a focusing triangular footprint area, so that there is no need to use a long spot size converter between the wide grating coupler and the narrow SOI waveguide.

Regarding the fiber to chip alignment tolerances, the grating coupler features higher alignment tolerances than the inverted taper. Coupling tolerances of about ± 1 μm for 1 dB penalty are found for the case of the grating [59], whereas in the case of the inverted taper, just ± 300 nm tolerances are found for the same penalty loss. When talking about wavelength dependence of the structures, we find that the inverted taper is broadband (> 100 nm bandwidth), while the grating coupler presents strongly wavelength dependency (3 dB bandwidth is about

50-60 nm). However, it is supposed to be enough for covering the C-band[1] in optical communication systems. With respect to polarization dependency, weak polarization dependent inverted taper designs can be obtained by choosing an optimum inverted taper tip width in many cases [83], whereas grating couplers are found to be strongly polarization dependent [84]. Finally, and due to the alignment tolerance issue, grating couplers are suitable for coupling multiple I/O fibers (i. e. fiber array (FA)[2]) to multiport circuits, whilst generally inverted tapers are not due to lower alignment tolerances [58]. A very nice review of different mechanisms for coupling light from silicon nanophotonic waveguides to different types of structures, which are added to improve the functionality of the basic waveguides, is presented in [85]. They compare different vertical horizontal coupling mechanisms applied to different applications, and obtained that the method chosen for a given application will depend on the required coupling efficiency, the desired bandwidth, the available footprint and technological considerations.

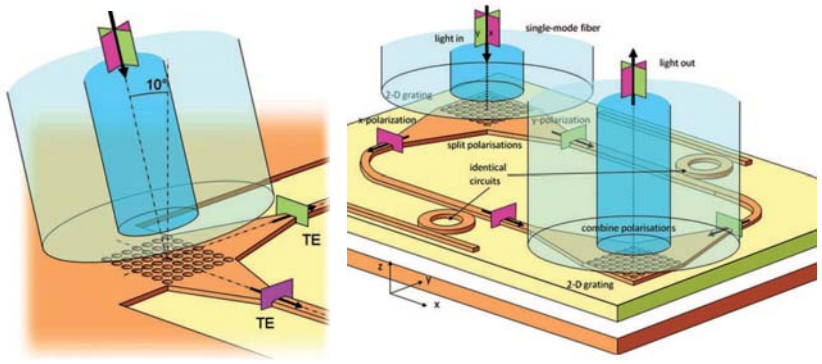
We can so conclude that both coupling techniques have their advantages and drawbacks when compared to each other. So, there is always little to either acceptance or rejection of the coupling approach to be implemented, being its choice in close connection with the device application and also with the available technology know-how in particular.

2.2.4 2D-gratings for transparency to polarization

As seen in section 2.1.1.1, the use of high refractive index contrast waveguide structures implies that the photonic integrated circuit behaves very differently for TE and TM polarized light. This is also the case for the 1D grating coupler discussed in the previous section. For practical applications often polarization independent operation of the photonic integrated circuit is required, since the polarization of the light in the optical fiber is unknown and varying over time. The use of 2D grating structures allows tackling this problem using a polarization diversity configuration. This is schematically depicted in Fig. 2.15(a) [86]. The

[1] The conventional wavelength window, known as the C-band, covers the wavelength range 1.53-1.57 μm

[2] Fiber arrays containing up to 48 singlemode fibers with 250 μm standard fiber spacing can be commercially obtained (http://www.ozoptics.com)



(a) (b)

Figure 2.15: Operation principle of a two-dimensional grating structure (a) and using this two-dimensional grating structure in a polarization diversity configuration (b) to obtain polarization insensitive operation of high index contrast waveguide structures [86].

2D grating structure can be seen as the superposition of two 1D grating structures, which are identical and which are designed to efficiently couple a single polarization (i.e., TE) to the waveguide circuit. By placing these one-dimensional grating structures orthogonal to each other, hence creating a square lattice grating structure, this 2D grating structure allows to efficiently interface with both polarizations of light in the optical fiber, by coupling the orthogonal polarizations in the optical fiber to identically (TE) polarized modes in orthogonal waveguides. This approach allows realizing polarization independent operation of (intrinsically very polarization dependent) high index contrast waveguide structures by having two identical photonic integrated circuits in both arms of the polarization diversity configuration as shown in Fig. 2.15(a) [86]. It should be noted that this approach does not need a polarization rotator. This is a major advantage because polarization rotators are difficult to integrate on a chip. Although the two-dimensional grating structure is an elegant way of solving both the fiber-chip coupling problem and the polarization dependence of photonic integrated circuits, the limited bandwidth over which low polarization dependence is obtained can be an issue in practical applications [86].

2.3 Summary and conclusions

An overview on the background of the main aspects related to the topic of this work has been reported in this chapter. Some issues regarding silicon photonic waveguides were first introduced, and the need for transparency to polarization in high index contrast silicon waveguide based devices was also discussed. The link between the coupling to fiber problem and the polarization diversity solution was then conclude, and efficient coupling techniques insensitive to polarization are strongly recommended. Silicon based slot waveguides were then introduced, emphasizing the fact that the strong confinement of the electromagnetic fields of the optical modes in a sub-micron sized slot region can be efficiently exploited for enhancing nonlinear effects, which is of high importance for potential nonlinear optical applications. The coupling to fiber problem in silicon photonic waveguides was then analyzed, by easily modelling the two main coupling loss contributions: the mode size difference and the impedance mismatch between the fiber and the waveguide. After calculating the coupling losses between the fiber and the waveguide, we concluded that efficient coupling techniques are needed, as obtained coupling loss were extremely high (more than 25 dB coupling loss for standard SMF fiber with $MFD = 10$ μm, λ=1.55 μm and TE polarization). Fabry-Perot resonance problem due to reflections in the fiber-waveguide interface was also introduced as one more problem to be solved with the effcient coupling techniques to be studied. Then, the most important SOI coupling techniques existing in literature were presented: grating coupler (out-of-plane coupling) and inverted taper (in-plane coupling). A comparison of both coupling techniques was also discussed, taking into accout their advantages and drawbacks, as pointed out in Table 2.1. We also discussed most relevant grating coupler and inverted taper design configurations reported in literature. At the end, we also introduced the use of 2D grating structures to alleviate polarization issues.

	Inverted taper	**Grating coupler**
Structure dimensions	- (single stage)	Footprint area: 10 μm × 10 μm
	Fiber-adapted waveguide cross-section: 9 μm × 9 μm; Taper length: 800-1000 μm (double stage)	
Coupling loss to SMF (butt fiber, 10 μm MFD)	- (single stage)	5-6 dB (conventional 1D grating)
	1.5 dB (double stage)	1dB (complex design)
Coupling loss to SMF (lensed fiber, incl. excess loss due to lens, MFD=2-4 μm)	< 1dB (single stage, best)	-
	3 dB (single stage, typical)	
Coupling tolerances for 1 dB penalty	± 0.3 μm (single stage)	± 1.0 μm
3 dB bandwidth	Broadband (>100 nm)	50-60 nm (conventional grating)
Polarization dependence	Weak	Strong (but can be solved with 2D grating and polarization diversity approach)
Suitable for multiple fiber I/O	Difficult (due to small tolerances)	Yes

Table 2.1: Most relevant properties of the major SOI fiber coupling techniques @ λ=1.55 μm [58].

Year	Research group	Fiber MFD	Coupling loss	Remarks
2002	NTT Labs [55]	4.3 μm	0.8dB (measured)	TE mode
2003	Cornell [62]	4.9 μm	0.5dB (measured)	Pol. sensitive
2005	IMEC-Ghent Univ [63]	2.5 μm	1.9dB (measured)	TE mode
2003	IBM Zurich [64]	2.5 μm	0.5dB (measured)	TE mode
2008	NTT Labs. [65]	2.5 μm	0.7dB (measured)	TE mode
2010	DTU Photonik [66]	2.5 μm	0.36dB (measured) 0.66dB (measured)	TM mode TE mode
2010	CEA-Léti Minatec [67]	2.5 μm	<1dB (measured)	TE and TM mode

Table 2.2: Review of some of the inverted tapers reported in literature.

Year	Type of grating	Research group	Coupling efficiency
2007	Bottom mirror [78, 68]	IMEC	69% (experimental)
2010	Silicon overlay [71]	IMEC	69% (experimental)
2003	Top mirror [79]	University of California	95% (theoretical)
1992	Slanted grating [80]	Osaka University	59% (theoretical)
2007	Slanted grating [81]	IMEC	16% (experimental)
2008	Chirped grating [82]	University of Hong Kong	34% (experimental)
2007	Holographic lens [77]	Luxtera	70% (experimental)

Table 2.3: Review of some of the gratings reported in literature.

Chapter 3

Grating-based fiber-to-chip coupling

After reviewing the state-of-the-art in chapter two, this chapter goes into detail about the first of the coupling strategies we are going to study in this thesis: the grating coupler. Theory, design, fabrication, as well as experimental results of grating-based SOI coupling structures, are addressed. We also report design and experimental results on multiport grating coupler SOI devices for fiber array interconnection, as well as on special grating couplers for coupling to horizontal slot waveguides.

3.1 Diffraction gratings

When the light is incident on the grating surface, it is diffracted due to the grating grooves. In effect, each groove becomes a very small source of reflected and/or transmitted light. This can be visualized in Fig. 3.1 which shows a plane wavefront with wave-vector $\vec{k}_i$, incident from a dielectric medium with refractive index n_1 to an infinitively long grating in other dielectric medium with refractive index n_2, at an angle θ_i. It is easy to see that the geometrical path difference between the light diffracted by successive grooves in a direction $\vec{k}_m$ is simply $|\Lambda \sin\theta_i - \Lambda \sin\theta_m|$, where θ_m is the angle of the diffracted light with respect to the grating normal, and Λ denotes the groove spacing, or grating period (see Fig. 3.1). The principle of interference dictates that only when this difference equals

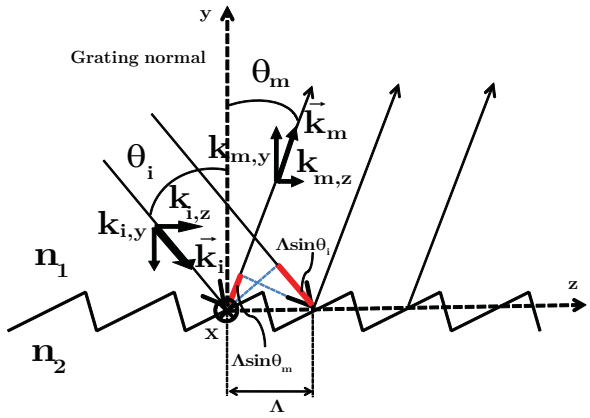


Figure 3.1: Diagram for phase relation between the rays diffracted from adjacent grooves in a diffraction grating. Bragg condition [87].

the wavelength of light (λ), the diffracted light will be in phase. The relationship between the wave-vectors of the incident and diffracted waves is so described by means of the well-known Bragg condition [87][1]:

$$k_{m_z} = k_{i_z} + m\frac{2\pi}{\Lambda}, \qquad m = 0, \pm 1, \pm 2, ... \tag{3.1}$$

where $k_{m_z} = k_m \sin\theta_m$ and $k_{i_z} = k_i \sin\theta_i$ are the z-axis wave-vector components of the diffracted and the incident wave, respectively, $k_m = k_i = k_0 n_1$ in material 1 and $k_m = k_i = k_0 n_2$ in material 2, being k_0 the wave number in vacuum (see Fig. 3.1). m is an integer numbering the diffraction orders so that the specular reflected one is numbered as 0. The order number m represents the number of wavelengths between light reflected from successive grooves. When $m = 0$, the grating acts as a mirror, all wavelengths being superimposed. When $m \neq 0$ the angle of diffraction depends on the wavelength value so that the wavelengths are separated angularly. The quantity [88]:

$$K = \frac{2\pi}{\Lambda} \tag{3.2}$$

[1] A particular case of this equation when there is no grating in the interface between two materials ($d = \infty$) is the well known Snell′s Law, which describes the refraction at the interface between two materials.

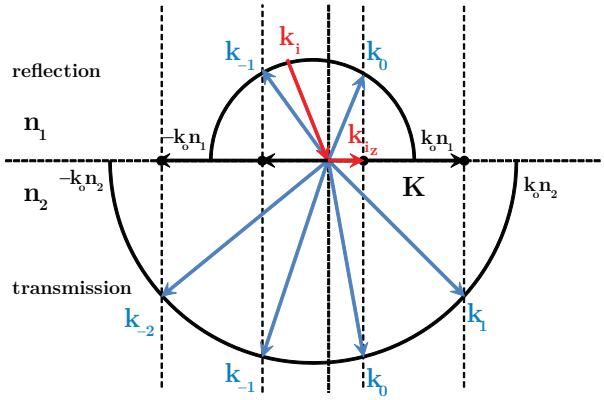


Figure 3.2: Example of wave-vector diagram. Graphical representation of the Bragg condition in Eq. 3.1.

is called *grating wavenumber* (or *grating vector*). The Bragg condition can be graphically represented in a wave-vector diagram as shown in Fig. 3.2. The Bragg condition only tells us which diffraction orders can occur, but it does not say anything about the efficiencies of these diffractions. A special class of gratings are waveguide gratings, where the periodic structure is made in or close to a waveguide. Waveguide gratings have always played a key role in integrated optics, even from the early 80s [89]. Some examples of device applications of waveguide gratings are fiber bragg grating filters (FBG), distributed feedback lasers (DFB), distributed Bragg reflector (DBR) lasers and fiber-to-waveguide couplers, among others [87].

3.2 Grating couplers theory

For a waveguide grating coupler, a similar formula to Eq. 3.1 can be written. In this case, the incident wave is replaced by the guided mode of the waveguide, which is characterized by its propagation constant β. The equation is [88]:

$$k_{m_z} = \beta + mK \tag{3.3}$$

where $\beta = \frac{2\pi}{\lambda} n_{eff}$, being n_{eff} the effective index of the optical mode in the grating waveguide. So, waveguide gratings are polarization dependent, as n_{eff} depends

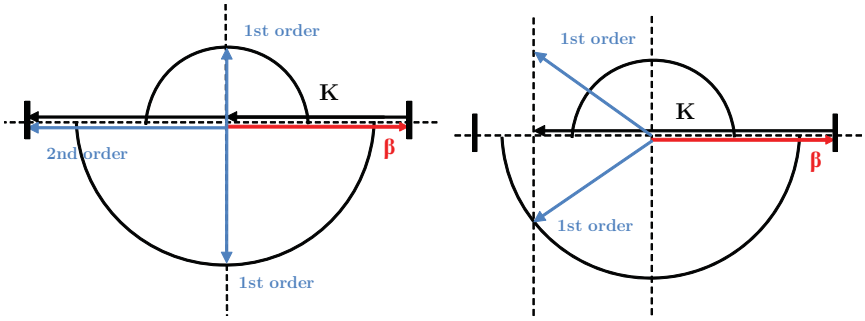


Figure 3.3: Example of wave-vector diagram for (a) a second-order waveguide grating coupler and (b) a grating with only one diffraction order.

on the polarization. Fig. 3.3 depicts two examples of wave-vector diagrams of waveguide grating couplers with two diffraction orders (Fig. 3.3(a)) and with just one diffraction order (Fig. 3.3(b)). The structure in Fig. 3.3(a) is called second-order grating, as the second order of diffraction is reflected back into the waveguide (counter-propagation direction), which is not suitable for practical devices. In that case the first diffraction order is vertically coupling out of the waveguide. This first order of diffraction is useful to couple to a fiber. The case of exactly vertical coupling occurs when $K = \beta$ or $\lambda = n_{eff}\Lambda$ (see Eq. 3.3). If the grating period is slightly different, the coupling is no longer exactly vertical but near vertical and the second diffraction order is minimized (ideally avoided) (see Fig. 3.3(b)). Even in this case, there still exist two possible diffraction orders, one up and one down (see Fig. 3.3(b)), but is preferred compared to the case of prefectly vertical coupling. It should be pointed out that the Bragg condition is only exact for infinite structures. For finite structures, there is not exactly one discrete wave-vector for which diffraction occurs, but a range of wave-vectors around the one predicted by the Bragg condition.

Fig. 3.4 sketches a schematic of the 1D waveguide grating coupler for near vertical coupling light to a tilted optical fiber (angle θ) due to the 1st order of diffraction. It consists of a squared-shape corrugation (period Λ, etching depth ed) made on top of a waveguide. We call it 1D grating, as the corrugation

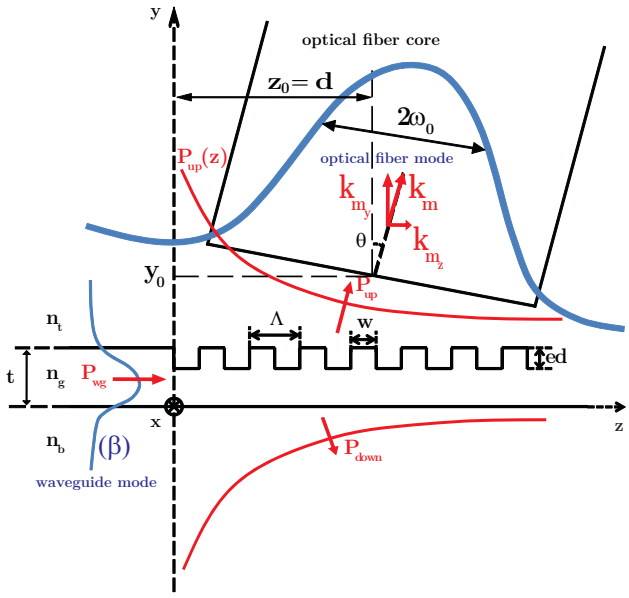


Figure 3.4: 1D waveguide output grating coupler with one diffraction order for coupling light to/from an optical fiber.

is just along the propagation direction of the waveguide (z-axis in Fig. 3.4). Here we only treat 1D gratings. These structures are also known in literature as corrugated waveguides. The waveguide has a core (n_g) of thickness t and an upper (n_t) and bottom (n_b) cladding. In general there can be additional layers, such as the substrate, depending on the waveguiding technology. Considering the grating as an output coupler (see Fig. 3.4), when the grating is excited with the optical mode of the waveguide (power P_{wg}), some light is diffracted upwards (power P_{up}), as well as some other amount is diffracted downwards (power P_{down}), at the resonant angle (θ), respectively due to the up ($m = 1$) and down ($m = -1$) diffraction orders. As there is no feedback of radiated diffraction orders to the guided wave in the grating waveguide, the part of the guided wave energy radiated by a single groove is carried away from the waveguide and the mode enters the next groove with diminished amplitude. Assuming slow change of the mode amplitude within one groove period, the amplitud of the electromagnetic fields of

the upwards diffracted wave (E, H) (i. e. $a(z)$) can be described by the following single differential equation [87]:

$$\frac{da(z)}{dz} = -\alpha a(z) \tag{3.4}$$

where α is the loss factor of the grating, and mainly depends on the grating physical parameters. The solution of Eq. 3.4 is an exponentially decaying amplitude:

$$a(z) = a(0)e^{-\alpha z} \tag{3.5}$$

Therefore, $P_{up}(z)$ due to the upwards diffracted light in Eq. 3.5 is (if there is no coupling between the forward and backward propagating guided mode):

$$P_{up}(z) = P_{wg}(z = 0)e^{-2\alpha z} \tag{3.6}$$

where the factor 2α is called the coupling strength or leakage factor of the grating. Eq. 3.6 is only exact for weak detuned gratings (small α). So, here we will treat weak gratings. The coupling length of the grating is defined as [90]:

$$L_c = \frac{1}{2\alpha} \tag{3.7}$$

and is related to the fiber mode field waist ω_0 by means of the equation [90]:

$$\omega_0 = 1.37 L_c \cos(\theta) \tag{3.8}$$

which allows the determination of the optimal fiber beam waist that has to be used for the given grating coupler parameters. Also, the optimal distance d between the center of the input fiber beam and the end of the grating coupler (see Fig. 3.4) is [90]:

$$d = L_c \tag{3.9}$$

Because we use singlemode fibers, the coupling efficiency from fiber to waveguide is the same as from waveguide to fiber due to the reciprocity theorem, and can be calculated using the following integral [88]:

$$\gamma = \frac{\left| \iint E \times H^*_{fib} \right|^2}{\mathrm{Re} \iint E \times H^* \cdot \iint E_{fib} \times H^*_{fib}} \tag{3.10}$$

where E, H are the electromagnetic fields of the diffracted wave from the grating, and E_{fib}, H_{fib} are the electromagnetic fields of the optical mode in the fiber. Equation 3.10 is only exact in uniform media and for weakly guiding structures. But, it does not take into account the reflection at the interface. However, it is a good approximation, even in the case in which the grating is covered by air instead of silica (there exist reflections in the fiber facet). If the electromagnetic fields in the grating and the fiber are normalized, Eq. 3.10 becomes [70]:

$$\eta = \left| \iint_S E \times H^*_{fib} dS \right|^2 \tag{3.11}$$

where S is the fiber facet.

Therefore, waveguide grating couplers can couple light from the top into a planar waveguide, and can also be used to inject or extract light anywhere in a PIC and not only at the edges. This type of coupler is so called surface coupler. Another advantage of surface couplers compared to edge couplers is that there is no need to polish facets. And because the entire surface of the chip can be used for input-output, a higher number of fibers can be connected to one chip. The main disadvantage of grating couplers is the limited bandwidth and/or coupling efficiency to fiber. Regarding the bandwidth, and taking into account finite structures, the coupling strenght of the grating coupler will limit the extent of the range of wave-vectors around the one predicted by the Bragg condition, and it will also limit the bandwidth of the grating coupler. Regarding the limited coupling efficiency, the most importat issue is that the overlap between the exponential profile of radiated field of the grating coupler (see Eq. 3.6)and the Gaussian-like profile of the optical fiber mode will rely on a low value. One more reason is that power P_{down} is lost towards the substrate, causing also a decrease in the coupling efficiency.

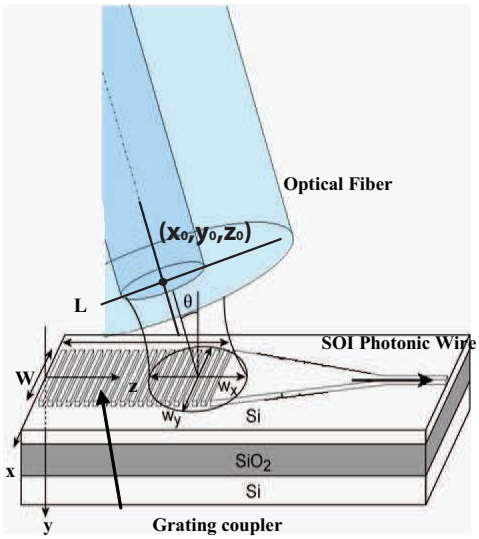


Figure 3.5: Schematic of a grating coupler in SOI technology.

3.3 SOI grating coupler engineering

3.3.1 Modelling

Fig. 3.5 illustrates a schematic of a grating coupler in SOI technology. The grating is patterned over a wide SOI waveguide with footprint area $W \times L$. A long taper is then used to adapt the grating waveguide width to the width of the SOI photonic wire. The complete coupling problem is a 3D problem, by solving Eq. 3.11 at the fiber facet interface, for the working polarization. Here, we will only treat TE polarization ($\vec{E} = E_x\hat{x}$). In the case of 1D gratings it can be reduced to two 2D problems, as the width of the SOI waveguide is much larger than the height and the wavelength. Fig. 3.6 shows the E-profile of the fundamental TE mode of a 12 μm wide and 250 nm thick SOI waveguide, caculated with a full vectorial mode solver based on the BPM. Because of the large width of the waveguide, it is a very good approximation to write the field $E_x(x, y) \approx E_x(x) \cdot E_x(y)$, where $E_x(y)$ represents the field component of the slab waveguide, and $E_x(x)$ is a lateral mode profile (see Fig. 3.6). The validity of this approximation is confirmed by

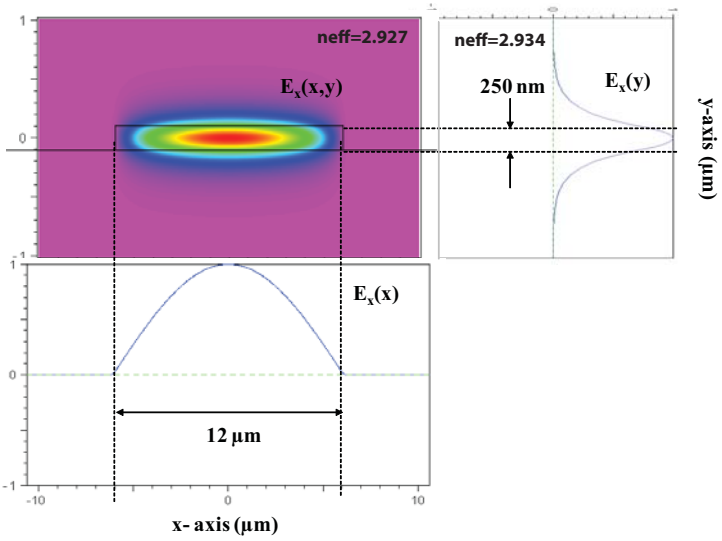


Figure 3.6: E-field profile of the fundamental TE mode of a 12 μm wide SOI waveguide. $E_x(x,y) \approx E_x \cdot E_x(y)$ because of the large width of the waveguide.

the fact that the effective index of the waveguide mode, also calculated with a full vectorial mode solver (2.927) is almost identical to the effective index of the SOI slab mode (2.934). The fiber mode in Eq. 3.11 is approximated by a Gaussian beam with beam diameter $2\omega_0$=10 μm. When neglecting the smaller field components, taking into account that $\cos(\theta) \approx 1$, by choosing a small fiber tilt angle θ, and neglecting the beam divergence in the x-direction, Eq. 3.11 can be written as [88]:

$$\eta = \left| \iint E(x)E(y=y_0,z)Ae^{-\frac{(x-x_0)^2+(z-z_0)^2}{\omega_0^2}} e^{\left(jn\frac{2\pi}{\lambda}z\sin\theta\right)}dxdz \right|^2 \tag{3.12}$$

where θ is the fiber tilt angle, (x_0, y_0, z_0) is the position of the fiber with respect to the grating coupler, and n is the refractive index on top of the grating, being equal to one when the grating is covered by air and the fiber is cleaved straight (see Figs. 3.4 and 3.5). The constant A represents the normalization of the Gaussian beam. For the fiber tilt angle we choose $\theta = 10^\circ$ in our designs. Regarding the position of the optical fiber in Eq. 3.12 (x_0, y_0, z_0) on top of the grating coupler,

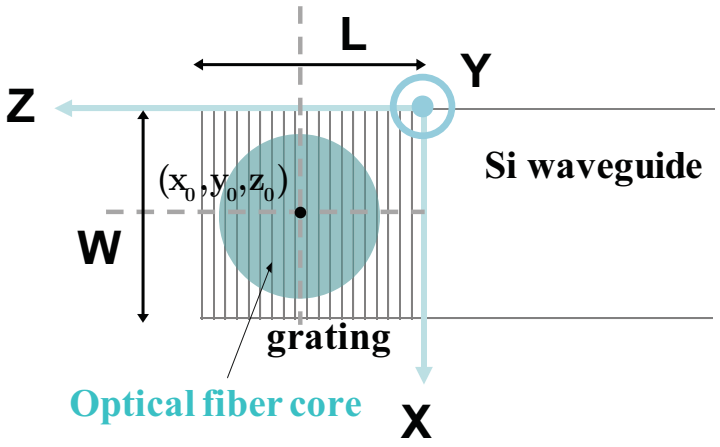


Figure 3.7: Schematic of the position of the optical fiber placed on top of the grating coupler of footprinc area $W \times L$.

it will depend on both the diffraction of the Gaussian beam, and on the grating coupler parameters. Fig. 3.7 illustrates the position of the optical fiber placed on top of the grating coupler. The optimal position of the fiber along the x-axis (x_0) is centered on the grating coupler, so $x_0 = W/2$. The position of the fiber along the y-axis depends on the diffraction properties of the Gaussian beam. The equations of the beam divergence and the phase delay of a Gaussian beam are presented in most textbooks on the fundamentals of optics or photonics [91] and we will not include them here. As an illustration, Fig. 3.8 depicts the beam radius divergence and the longitudinal phase delay of a Gaussian beam with waist radius ω_0=5 μm. At the origin, the beam has a planar phase front, which is a property of a plane wave. Far away from the origin, the phase front becomes spherical. At 10 μm distance from the origin, the phase is approximately 10° at the beam radius. At 20 μm distance from the origin, the phase is already 20° at the beam radius and further away the beam is expanding rapidly. We can conclude that for butt-coupling to fiber, the distance to the fiber (y_0) should be kept as small as possible and certainly < 10 μm. In our simulations we have chosen y_0=1 μm, as we will further discuss. The optimal longitudinal position of the fiber z_0 depends on the grating and on the working wavelength. According

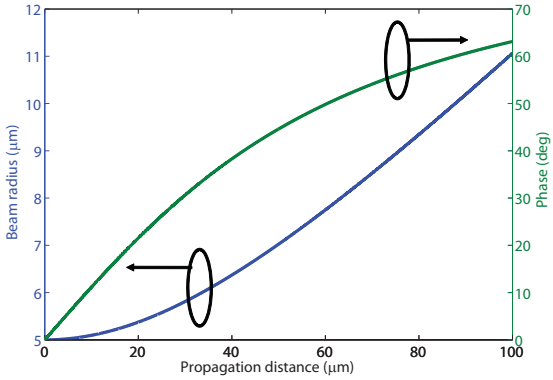


Figure 3.8: Diffraction and longitudinal phase delay of a Gaussian beam with waist radius 5 μm.

to Eq. 3.9, this optimal position is equal to the coupling length of the grating (L_c), and inversely proportional to the leakage factor of the grating 2α (see Eq. 3.7), being α the loss factor of the grating (see also Eq. 3.6). Fig. 3.9 shows the overlap between a Gaussian profile and the exponential profile of radiated energy of the grating (proportional to $e^{-2\alpha z}$) as a function of α. The maximum overlap is obtained for α=0.13 μm^{-1}, which corresponds to a coupling length of L_c=3.8 μm according to Eq. 3.7. This agrees with Eq. 3.8 for a fiber tilt angle of $\theta = 10\,^\circ$.

For easily solving the 3D problem summarized in Eq. 3.12, this formula is able to be splitted in two terms, respectively depending on x and z. If the x-dependent term is ξ, the coupling efficiency is the coupling efficiency of a 2D problem multiplied by ξ. For a W=12 μm wide SOI waveguide and ω_0=5 μm, we obtain $\xi \simeq 1$ using a full vectorial mode solver based on the BPM for the calculation of the optical mode. Then, we will use W=12 μm in our furthcoming grating coupler realization. So, the 2D problem is a very good approximation for the grating coupler design for a grating width of W=12 μm.

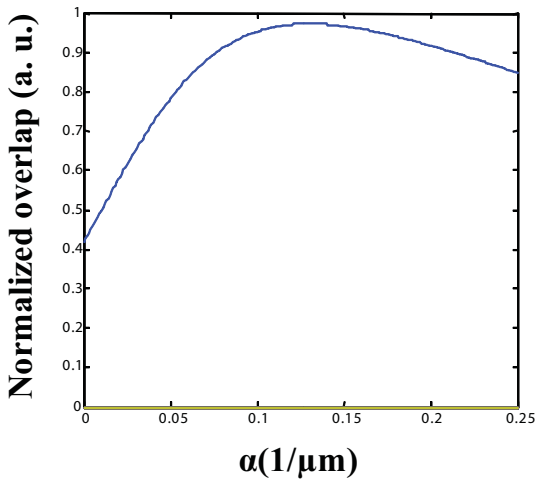


Figure 3.9: Overlap between Gaussian beam of waist radius 5 μm and an exponential profile $e^{-2\alpha z}$.

3.3.2 Design and simulations

Fig. 3.10 depicts a schematic of the 1D SOI grating coupler to be designed. The grating waveguide has a core (thickness t_{core}) and a cladding (thickness t_{clad}) and a silicon substrate. As we are going to use SOI wafers of 250 nm/3 μm Si/SiO_2 layer thicknesses, we optimize the grating design for t_{core}=250 nm and t_{clad}=3 μm. The uppercladding layer on top of the grating is supposed to be air. The main grating coupler design parameters are the grating period Λ and the etching depth ed. The filling factor or duty cycle of the grating is $ff = w/\Lambda = 0.5$ (see Fig. 3.10). The optimal londitudinal position of the fiber with respect to the grating is $d = 3.8$ μm, according to the explained previously. The height of the fiber h mainly depends on the diffraction performance of the Gaussian-like beam of the fiber, as pointed out before, and needs to be < 10 μm in any case. Because we are going to use 2D Finite Difference Time Domain (FDTD) simulations, we have to optimize the fiber height for reducing our simulation region as much as possible, as the FDTD method is slow and highly memory/time consuming if the simulation region is too big. We choose $h = 1$ μm for our simulations, as also our results were similar compared to some other results presented in literature

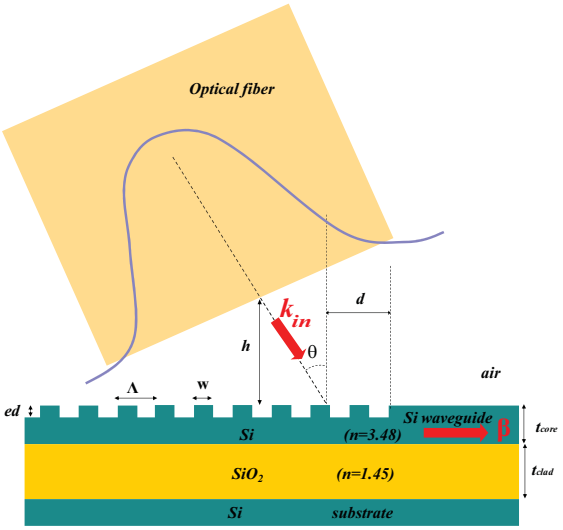


Figure 3.10: Schematic of the SOI 1D grating coupler to be designed via 2D approximation.

for this value. For the grating in Fig. 3.10 we can write the following Bragg condition equation, similarly to Eq. 3.3:

$$k_{in} \sin\theta + m\frac{2\pi}{\Lambda} = \beta \tag{3.13}$$

where $k_{in} = 2\pi/\lambda$ and $\beta = (2\pi/\lambda)\, n_{eff}$. So, the grating period is (for diffraction order $m = +1$):

$$\Lambda = \frac{\lambda}{n_{eff} - \sin\theta} \tag{3.14}$$

where the effectice index of the fundamental mode in the grating waveguide n_{eff} depends on the waveguide grating parameters. If the filling factor of the grating is $ff = 0.5$, and considering a grating coupler with an even number of periods (typically 20), $n_{eff} \simeq (n_{eff,p} + n_{eff,u})/2$, being $n_{eff,p}$ and $n_{eff,u}$ the effective index of the perturbed (thickness: t_{core}) and unperturbed (thickness: $t_{core} - ed$) grating regions, respectively (see Fig. 3.10). Using a full vectorial mode solver based on the BPM, we calculate $n_{eff,p} = 2.6777$ and $n_{eff,u} = 2.927$ for a grating core thickness of t_{core}=250 nm and ed = 70 nm, both for TE polarization and

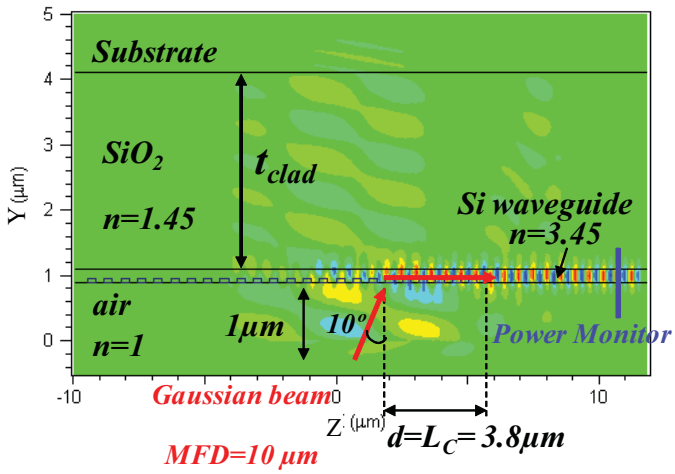
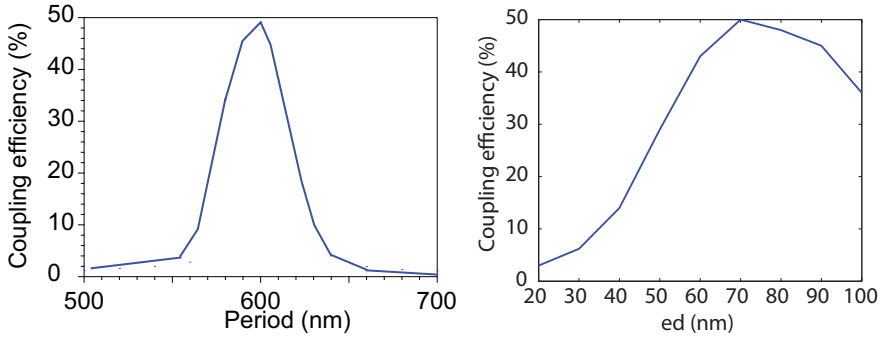


Figure 3.11: E-Field distribution in the grating coupler when optimizing the grating period via 2D FDTD simulations.

λ=1550 nm. So, we have n_{eff} = 2.8. Then, the theoretical value of the grating coupler period is Λ=590 nm, taking into account an etching depth of ed=70 nm[1]. After calculating the theoretical period, we optimize this value via 2D FDTD simulations. Fig. 3.11 depicts the simulation layout and the obtained results on the E-field distribution in the grating during the simulation for TE polarization. As depicted in Fig. 3.11, we launch a θ=10° tilted Gaussian beam on top of the grating at the optimal position as discussed previously. A power monitor is placed in the waveguide for measuring the coupling efficiency. Fig. 3.12(a) shows simulation results for the obtained coupling efficiency as a function of the grating period for t_{core}=250 nm, t_{clad}=3 μm and ed=70 nm. The polarization is TE and λ=1550 nm. We obtain near maximum 50% coupling efficiency for a grating period of 600 nm, which is in a very good agreement to the expected from theory. So, optimum simulation grating period is Λ=600 nm. After optimizing the grating period via 2D FDTD simulations, we also sweep the etching depth for the grating period obtained before. Fig. 3.12(b) shows the simulation results for the grating

[1]It is important to remind that our model is only valid for weak gratings with small loss factor α, which is physically equivalent to small etching depths ed compared to the core thickness t_{core}. Then, we have $ed < 0.3t_{core}$



(a) (b)

Figure 3.12: 2D FDTD simulation results for the grating coupling efficiency as a function of (a) the grating period and (b) for t_{core}=250 nm and t_{clad}=3 μm. In (a), ed=70 nm, and Λ=600 nm in (a). Polarization is TE and λ=1550 nm.

coupling efficiency as a function of the etching depth for Λ=600 nm, t_{core}=250 nm, t_{clad}=3 μm. Polarization is TE and λ=1550 nm. We obtain 50% maximum coupling for an etching depth of ed=70 nm, so the grating design is properly optimized for Λ=600 nm and ed=70 nm. For these optimum design parameters, spectrum in telecom band is also computed. Fig. 3.13 depicts theoretical spectral response of the designed grating coupler obtained via 2D FDTD simulations. A 1dB bandwidth of about 40nm is obtained.

Sensitivity to fabrication and alignment tolerances of the structure has also been analyzed. To study fabrication tolerances, simulations were performed with different filling factors as well as different etching depths for the previously designed grating coupler. Fig. 3.14(a) shows coupling efficiency results when varying those parameters. It is obtained coupling efficiency higher than 40% for etching depth values of about $ed = 70 \pm 15$ nm or filling factor values of $ff = 50 \pm 15$ %. To study alignment tolerances, the incident angles as well as the horizontal fiber positions were varied. Fig. 3.14(b) shows coupling efficiency results when varying those parameters. Coupling efficiency up to 40% is obtained for $\theta = 10 \pm 3$ degrees or horizontal fiber positions of $d = 4 \pm 2$ μm, which corresponds to alignment tolerances of ± 2 μm @ 1dB penalty of minimum coupling loss.

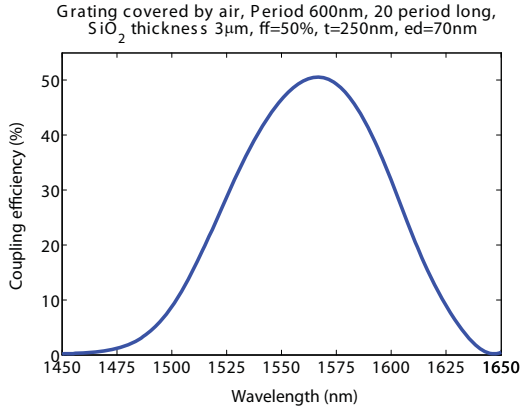
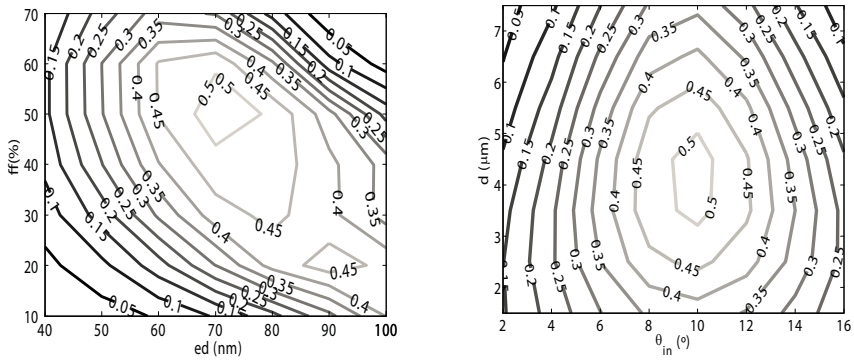


Figure 3.13: Simulation results for spectral response of designed grating coupler.



(a) (b)

Figure 3.14: Simulation results for the coupling efficiency of the designed grating coupler, showing its (a) fabrication and (b) alignment tolerances.

3.3.3 Fabrication and experimental results

For the fabrication of designed grating couplers we generated the layout depicted in Fig. 3.15. The layout is composed by three different devices (D1, D2 and D3). Each device consists of a 500 nm wide SOI waveguide, which is input and output grating coupled. The length of the SOI waveguides are 100 μm, 1 mm and 2.4

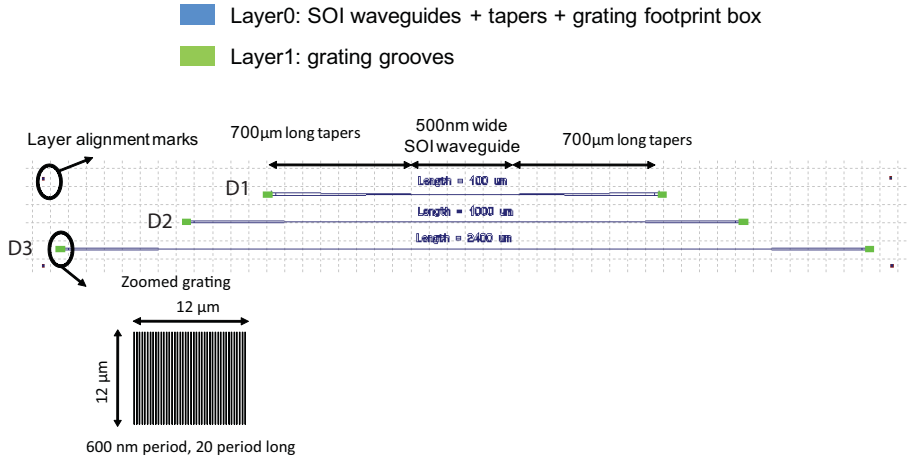
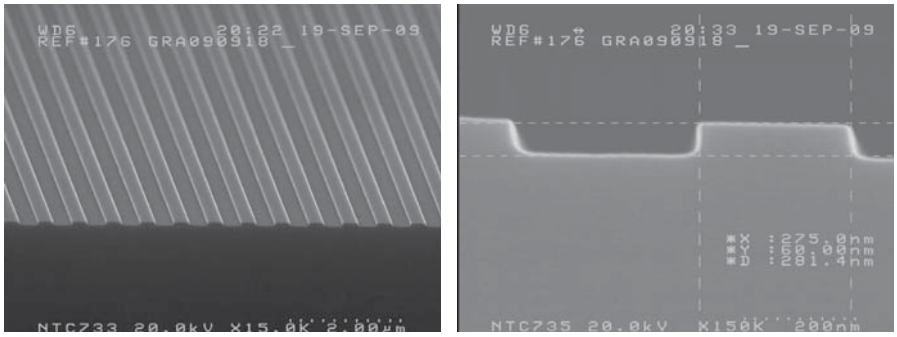


Figure 3.15: Generated layout for the fabrication of designed grating couplers.

mm, for devices D1, D2 and D3, respectively (see Fig. 3.15). A 700 μm long taper is used as grating-SOI waveguide spot size converter for all the devices. Each grating is 12 μm $\times$ 12 μm area, 600 nm period, 20 period long and 50 % duty cycle. The layout so consists of two different layers, each one corresponding to a different and consecutive lithography step for fabrication. Layer 0 contains the definition of the SOI waveguides, the tapers and the footprint box of the grating couplers. Layer 1 contains the definition of the grating grooves to be patterned on the grating box. For the alignment of the two layers during the lithography process, we use the marks depicted in Fig. 3.15. The samples were fabricated in the Nanophotonics Technology Center (NTC)[1] of the Universidad Politécnica de Valencia. For the fabrication we used commercial SOI wafers with 250 nm top silicon thickness, and 3 μm buried SiO_2 thickness. The fabrication process of the grating structures was carried out by using e-beam lithography over PMMA (polymethyl methacrylate) resist. The electron dose was adjusted in order to

[1]The Valencia Nanophotonics Technology Center (NTC) is a research center inside the Universidad Politécnica de Valencia (UPV). The NTC place at UPV measures 3500 square metres with space for 100 professionals including a 500 square metre cleanroom (class 10-100-10.000). The aim of the NTC is to encourage regional development by transferring university research results to industry. See http://www.ntc.upv.es



(a) (b)

Figure 3.16: (a) SEM image of grating couplers. (b) Detail of SEM image of fabricated gratings showing actual grating non-grooved region width, after fabrication.

achieve the optimized design dimensions as much as possible. After developing the sample, the patterned resist was employed as a mask in the following fabrication step consisting on dry etching by using an Inductive Coupled Plasma (ICP) system. This process was also optimized in order to reach grating design dimension (etching depth 70nm, period 600nm, and filling factor 50%). A Scanning Electron Microscope (SEM) image of fabricated gratings is depicted in Fig. 3.16(a). Fig. 3.16(b) depicts a SEM image showing measured actual grating non-grooved region width and actual grating etching depth after fabrication. Actual grating non-grooved region width and etching depth are $w = 275$ nm and $ed = 60$ nm, respectively. So, the actual grating filling factor is about $ff = 275/600$=45.8 %. For measured dimensions, the grating coupling efficiency is expected to be around 40%, according to theoretical fabrication tolerance graph depicted in Fig. 3.14, for an etching depth of 60 nm and a grating filling factor of about 45.8 %.

A block diagram of the measurement setup is drawn in Fig. 3.17. The I/O fibers are mounted under a 10 degree angle on two different 5-axis (X,Y,Z,ϕ,θ) translation stages for controlling the fiber position over the gratings, as well as te fiber tilt angle. The sample is mounted on a vacuum chuck on a 2-axis (X,Y) stage. A tunable laser source and a polarisation controller are used at the input side. The output power is detected by a power meter. The laser and the power meter are

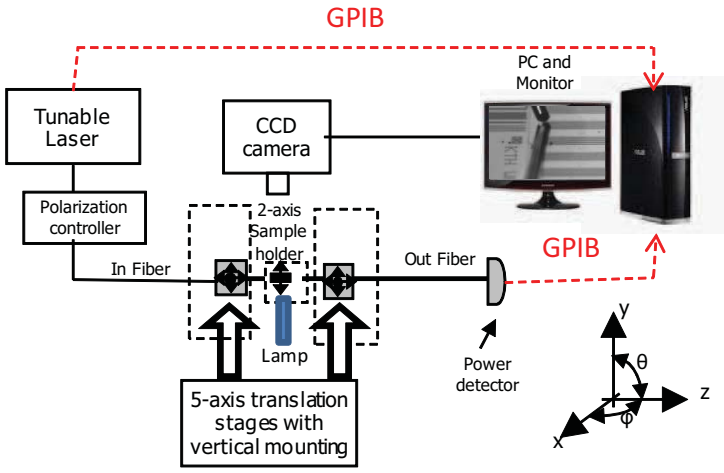


Figure 3.17: Block diagram of measurement setup for grating coupler samples.

GPIB-connected to a computer for enabling sweeping the laser wavelength and measure the optical poer automatically in tranmission spectrum measurements. A visual charge coupled device (CCD) camera with a 50X objective is mounted under a 30 degree angle from the table plane in order to visualize structures and fibers, and also to make easier the fiber-grating alignment. A lamp illuminates the sample and the fibers with somewhat diffuse light. The image from the camera is displayed on a monitor for the alignment. The camera is put on some XY translation stage for moving all over the sample. A photo of the measurement setup is showed in Fig. 3.18. During the fiber-chip alignment process, the lamp is first positioned so that diffuse light illuminates the sample, and the camera and objective are focused on the sample, and the sample area appears on the screen. The input and output fibers are then positioned roughly over the area where the fiber couplers are. This is done with the fibers at a safe vertical distance from the sample (typically higher than 2 mm distance). Now, the fibers are brought closer to the sample vertically, so that the fiber or its shadow or both appear on the screen. The fiber coupler, which should be visible at the beginning of the alignment waveguide as a small rectangle of slightly different colour, is then positioned between the edges of the fiber and its shadow. This is illustrated

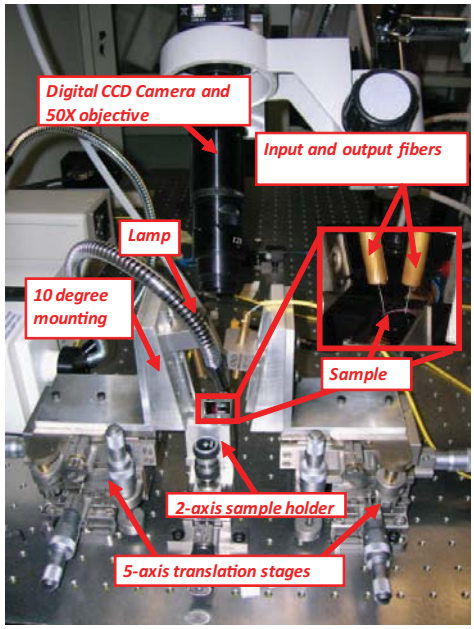


Figure 3.18: Photo of measurement setup for grating coupler samples.

Device	Length (cm)	Output power (dBm)
D1	0.01	-10.85
D2	0.1	-11.55
D3	0.24	-12.45

Table 3.1: Measured output power for devices D1-D3 @ λ=1550 nm.

in Fig. 3.19. After both the input and output side have been positioned as depicted in Fig. 3.19, measurable power already comes through an alignment waveguide or structures with a high enough transmission at the set wavelength. The transmission is optimized by changing the polarization of the input light (TE polarization), and the fibers can be moved closer to the sample to optimize transmission even more. With some experience, the height of the fiber above the sample is estimated from the camera image, with an accuracy of around 10 μm.

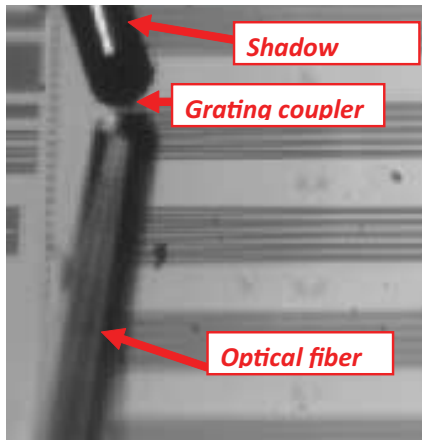


Figure 3.19: Aligning the fiber with a fiber coupler by controlling the fiber height and its shadow on the monitor.

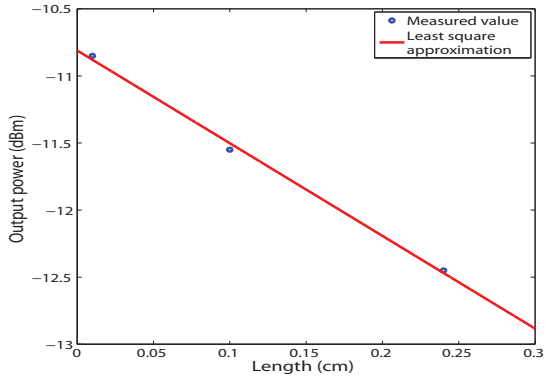


Figure 3.20: Measured output power as a function of the SOI waveguide length in each device, and least square approximation for calculating propagation and excess loss.

Table 3.1 reports measured output power in each device for its corresponding SOI waveguide length at λ=1.55 μm. Results in Table 3.1 include coupling loss in the gratings, taper loss, as well as propagation loss in the SOI waveguides. From these results we can obtain the propagation loss in the waveguide, taking

into account the SOI waveguide length in each device. Fig. 3.20 depicts a graph containing three points corresponding to the measured output optical power of each device for its corresponding SOI waveguide length. Using the least square method, we can calculate the line which interpolates these three points (see red line in Fig. 3.20), and whose slope is the propagation loss in the waveguides, expressed in dB/cm. Using the least square method, we obtain propagation loss of (6.91 ± 0.36) dB/cm. The excess loss (corresponding to the add of coupling loss of the gratings and the loss in the tapers) can also be extracted from the interpolation line by means of the least square method in Fig. 3.20, for the case in which the length is equal to zero (similarly, a zero long waveguide). We calculated (10.81 ± 0.05) dB excess loss. As we can not obtain experimentally the losses in the tapers from the measurements, we assume excess loss are mainly due to coupling loss of the gratings, so that we have about 5 dB coupling loss per grating. This value corresponds to a coupling efficiency in each grating of about 31 %. This value is in good agreement with the expected from theory (40 % coupling for actual grating parameters measured after fabrication), taking into account that real experimental coupling efficiency will be a bit higher than calculated due to taper loss. Finally, measured transmission loss spectrum of device D3 is illustrated in Fig. 3.21. A 1 dB bandwidth of 30 nm is experimentally obtained.

3.3.3.1 Multiport grating coupler SOI chips experiments

The goal here is to experimentally check the alignment tolerances of grating couplers, and also to prove the advantages of using grating couplers in multiport SOI devices. For this purpose, we generated the layout illustrated in Fig. 3.22. A total of eight equal devices (D1-D8) were drawn on the same layout. All devices contain a total of eight grating couplers, four of them acting as input grating couplers (G1-G4) and four of them acting as output grating couplers (G5-G8). Input and output gratings are interconnected to each other by means of 500 nm wide singlemode SOI waveguides, so that we can define four different optical paths (G1-G8, G2-G7, G3-G6, G4-G5) with a different length for the SOI waveguides (see Fig. 3.22). The footprint area of each grating coupler is 12 μm

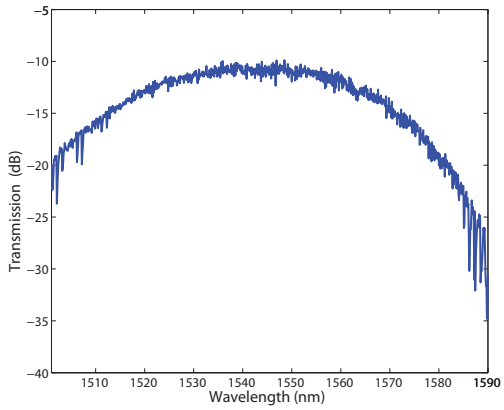


Figure 3.21: Measured transmission loss spectrum of grating coupler device D1.

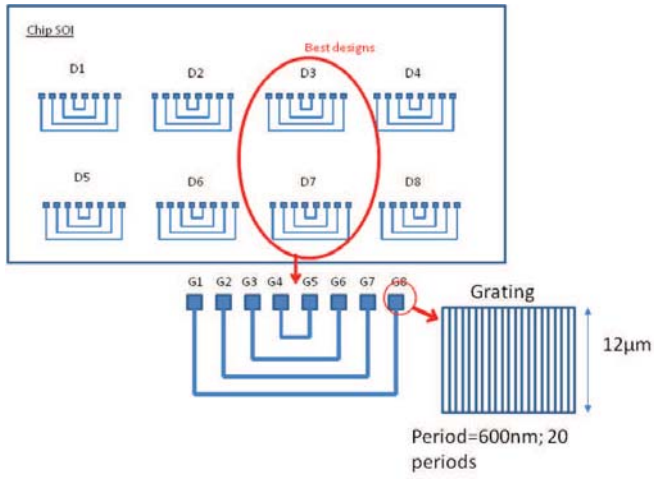


Figure 3.22: Schematic of the layout for the fabrication of the designed multiport grating coupler SOI chips.

$\times$ 12 μm. A detailed view of each individual device is illustrated in Fig. 3.23. The layout consists of two different layers. Layer 0 contains the definition of the SOI waveguides, the tapers and the footprint box of the grating couplers. Layer 1 contains the definition of the grating grooves to be patterned on the

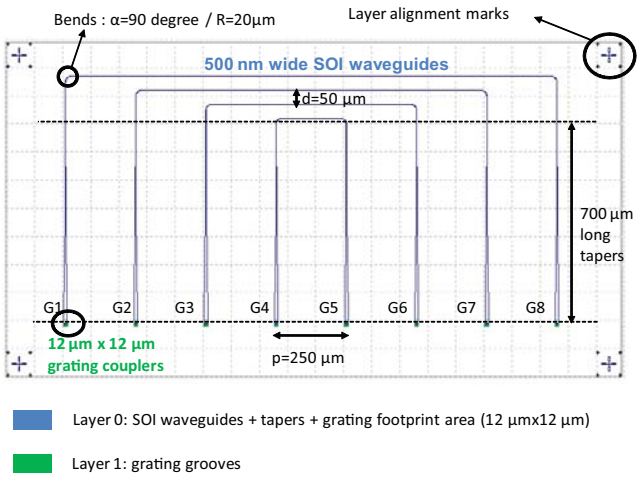


Figure 3.23: Detail of the layout of each individual multiport device.

grating box. For the alignment of the two layers during the lithography process, we use the marks depicted in Fig. 3.23. The standard fiber spacing in the commercial fiber arrays we are going to use is 250 μm. So, the distance between the grating couplers in each device is p=250μm too. Again, a 700 μm long taper is used as spot size converter between grating and the 500 nm wide singlemode SOI waveguide. We use R=20 μm radius bends for 90 degree rotation of the SOI waveguides for changing their orientation in each optical path (see Fig. 3.23). The SOI waveguides are vertically spaced a distance d=50 μm for avoiding crosstalk. Table 3.2 shows the calculation of the length of each SOI waveguide in each optical path, taking into account the design parameters of the layout in Fig. 3.23. The samples were fabricated at the NTC in the UPV. The fabrication process of the samples is similar to the previous process described in section 3.3.3. Fig. 3.24 depicts a SEM image of fabricated devices. SEM images detailing the fabricated grating couplers are showed in Fig. 3.25, thus showing the actual grating period (Fig. 3.25(a)) and the grating groove width and etching depth (Fig. 3.25(b)) after fabrication. After fabrication, the actual grating etching depth was found to be 55 nm, as well as actual grating period and actual grating groove width were found to be 600 nm and 287.5 nm, respectively (see Fig. 3.25). Thus, the

Path	SOI waveguide length expression	Length value
G1-G8	$(7p - 2R) + 2\left(\frac{\pi}{2}R\right) + 2\,(3d)$	2072.83 μm
G2-G7	$(5p - 2R) + 2\left(\frac{\pi}{2}R\right) + 2\,(2d)$	1472.83 μm
G3-G6	$(3p - 2R) + 2\left(\frac{\pi}{2}R\right) + 2\,(d)$	872.83 μm
G4-G5	$(p - 2R) + 2\left(\frac{\pi}{2}R\right)$	272.83 μm

Table 3.2: SOI waveguide lengths in each optical path.

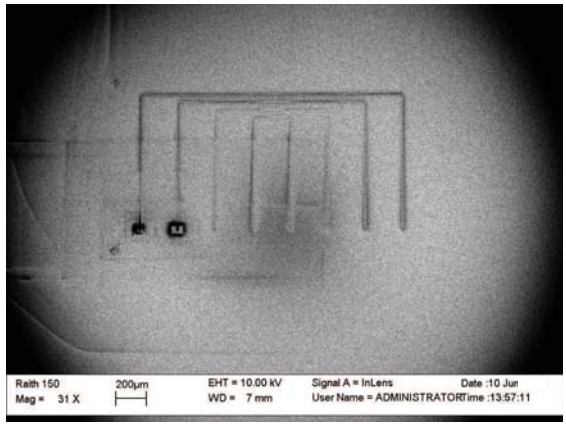


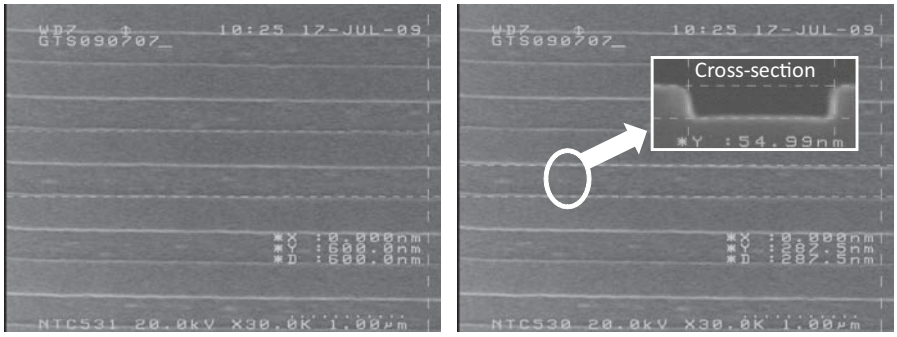
Figure 3.24: SEM image of fabricated devices.

actual grating filling factor (or duty cycle) is $ff = (600 - 287.5)/600 = 52\%$. According to the obtained parameters of the fabricated grating couplers, the expected theoretical coupling efficiency of the grating couplers is 30 %, taking into account the theoretical results on the grating fabrication tolerances of the graph in Fig. 3.14, for an etching depth of 55 nm and a filling factor of 52 %.

Fig. 3.26 depicts a block diagram of the measurement setup used in Fraunhofer Institute for Reliability and Microintegration (Fraunhofer IZM)[1] in Berlin (Germany) for the measurements of fabricated samples, in close collaboration within the *ePIXnet* Network of Excellence [2]. The instrumentation used in the

[1] http://www.izm.fraunhofer.de/

[2] The European Network of Excellence on Photonic Integrated Components and Circuits



(a) (b)

Figure 3.25: SEM image of fabricated grating couplers showing (a) actual grating period and (b) actual grating groove width and etching depth, after fabrication.

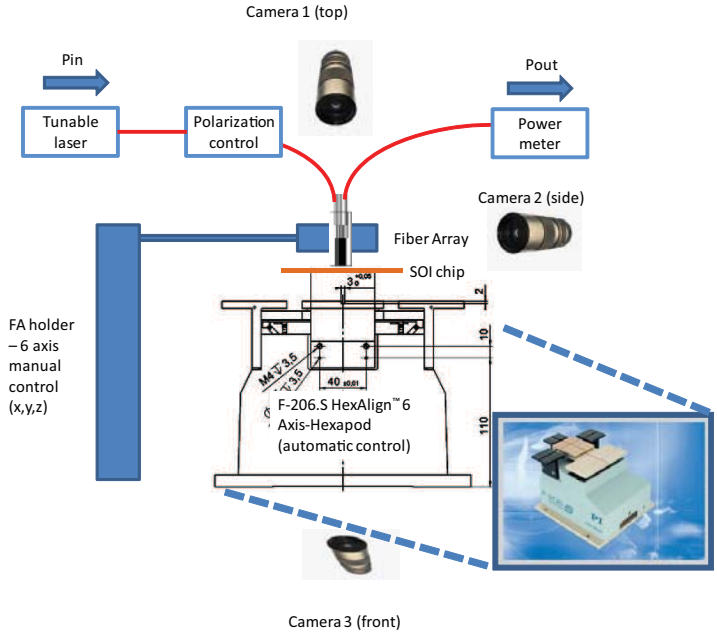


Figure 3.26: Block diagram of the measurement setup.

ePIXnet (http://www.epixnet.org), was launched by the European Commission in 2004, as part of the 6th framework program (http://ec.europa.eu/research/fp6/index_en.cfm), with a focus on photonic integrated components and circuits. This network consisted of 50 partners, both full and affiliate, with a good mix of universities (22), research institutes (11) and companies (17).

setup in Fig. 3.26 for the measurements was:

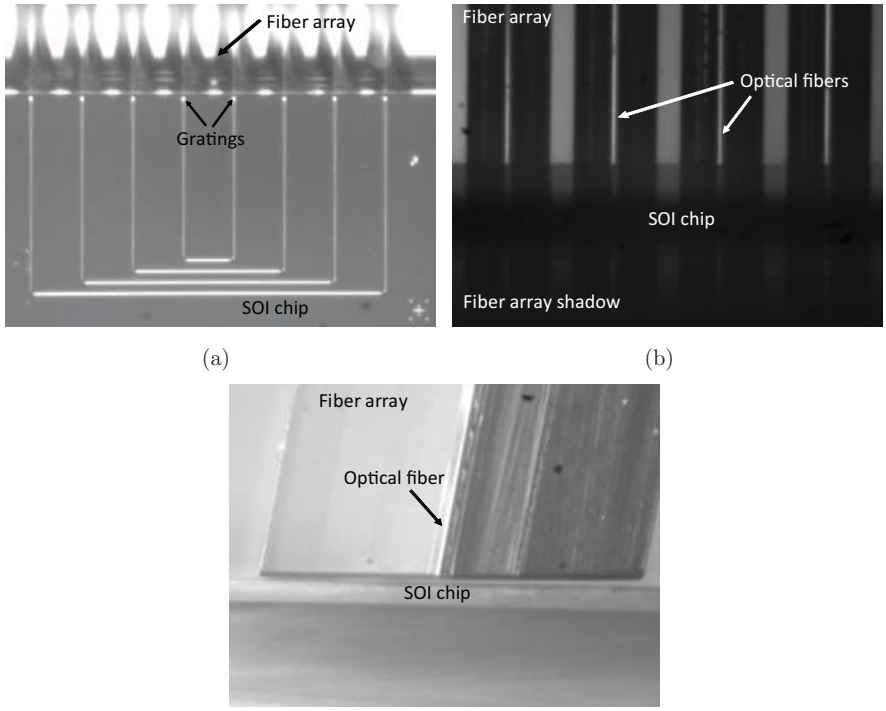
- 1 HEXAPOD F-206 6-axis control (automatic control for the SOI chip) [1]
- 1 MANUAL 3-axis holder (for controlling the fiber array position)
- 1 LASER HP 8168A (tunable laser, [1530,1580] nm)
- 1 POWER METER HP 8153A (detector @ 1550nm, 100 nm bandwidth)
- 3 digital cameras, zoom 1000x (top, front & side views)
- 1 commercial fiber array from OZOptics DTS0083(8 fibers, fiber spacing 250 μm)[2]
- 1 polarization controller (input)

Basically, the HEXAPOD holds the SOI chip, which is automatically controllable in 6-axis (x, y, z and rotation angle of each axis, respectively). A manual 3 axis controller holds the fiber array on top of the SOI chip. The tunable laser is connected via optical fiber to a polarization controller for controlling the polarization at the input port, and then interconnected to the input fiber of the fiber array. The output optical fiber of the fiber array is then connected to a power meter for measuring output power (transmission spectrum measurements). For controlling the alignment between the chip and the fiber array, we use three optic cameras (top, side and front views of the chip and the fiber array). Figs. 3.27(a), 3.27(b) and 3.27(c) respectively depict a photo of the top, front and side camera views during the alignment process.

Fig. 3.28(a) depicts a photo of the measurement setup, as well as Fig. 3.28(b) depicts a detailed photo of the fiber array placed on top of the SOI chip during the alignment procedure. For the measurements, we first actively align the fiber array to the chip by optimizing the optical power of the most critical path (G1-G8). Once this optical path is properly aligned, the other optical paths are also properly aligned with the fiber array, as their grating couplers are in line with

[1] PI Physik Instrumente Datasheet details:
http://www.physikinstrumente.com/en/products/prdetail.php?sortnr=700820

[2] http://www.ozoptics.com/ALLNEW_PDF/DTS0083.pdf

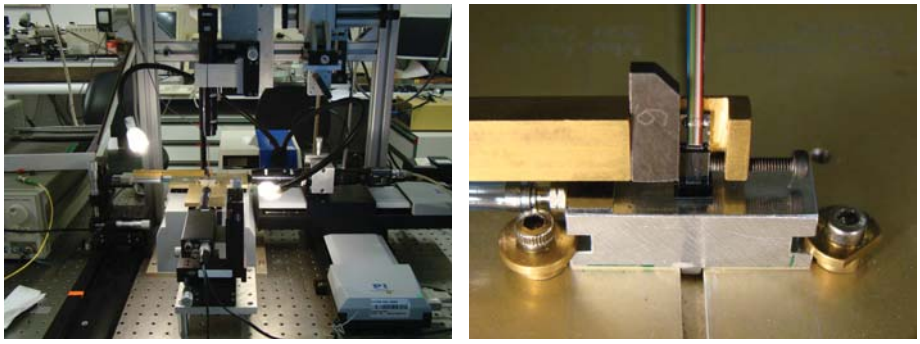


(a) (b)

(c)

Figure 3.27: Photos of the (a) Top, (b) front and (c) side views of the SOI chip and the fiber array taken with the optical cameras of the measurement setup during the alignment procedure.

the grating couplers of the optical path G1-G8 (see Fig. 3.23). Setting the input power of the laser to 0dBm, measured optical power at the output corresponds to the transmission losses of our device. Once the chip is aligned to the fiber array, we optimized the polarization by adjusting the input polarization controller. Once polarization is optimized, we also measure optical power in the other paths. After testing all the devices (D1-D8), we obtain that the best devices are D3 and D7; so we decided to use device D3 for the measurements. Table 3.3 summarizes measured optical power of optical paths in device D3 for a wavelength λ=1550 nm. Results in Table 3.3 include coupling loss in the gratings, taper loss, as well



(a) (b)

Figure 3.28: (a) Photo of the measurement setup. (b) Detailed photo of the fiber array placed on top of the SOI chip in the alignment procedure.

Optical Path	**Output Power (dBm)**	**Deviation from path G4-G5 (dB)**
G1-G8	-13.7	-1.1dB
G2-G7	-13.2	-0.6dB
G3-G6	-13.1	-0.5dB
G4-G5	-12.6	-

Table 3.3: Measured output power for device D3 @ λ=1550 nm.

as propagation loss in the SOI waveguides. From these results we can obtain the propagation and excess loss in the waveguide by using the least square method, taking into account the previously calculated length of each optical path.

Fig. 3.29 depicts a graph containing four points corresponding to the measured output optical power of each optical path for its corresponding length in the device D3, as well as the interpolation line obtained through the least square method. We obtain propagation loss of (5.67 $\pm$ 0.9) dB/cm and excess loss of (12.48 $\pm$ 0.12) dB. As we can not obtain experimentally the losses in the tapers from the measurements, we assume excess loss are mainly due to coupling loss of the gratings, so that we have about 6.24 dB coupling loss per grating. This value corresponds to a coupling efficiency in each grating of about 24 %. This

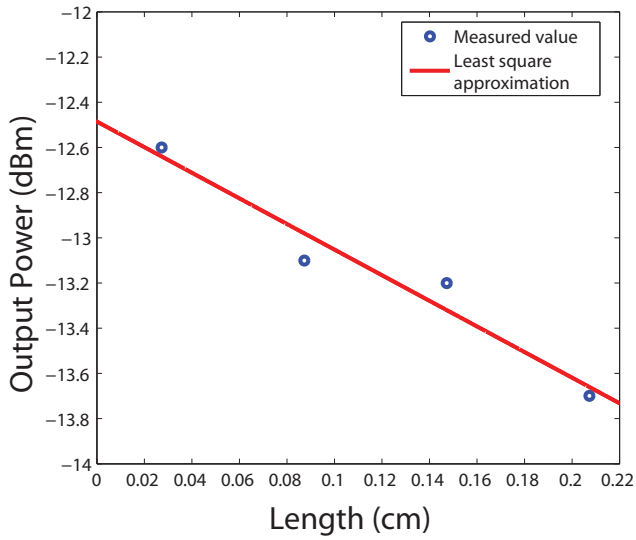


Figure 3.29: Measured output power for each optical path length, and least square approximation for calculating propagation and excess loss in device D3.

value is in good agreement with the expected from theory (30 % coupling for actual grating parameters measured after fabrication). We finally measured the alignment tolerances of the fabricated gratings by doing an automatic scan on the grating surface (x, y plane). Fig. 3.30 depicts measured transmission loss as a function of the fiber displacement within the (x, y) plane. The coordinate (0,0) corresponds to the optimal fiber position for the coupling. It can be seen as the alignment tolerances along the x-axis are about ± 2 μm for 1dB loss penalty, as expected from theoretical results. Moreover, the alignment tolerances along the y-axis are found to be larger (about ± 3 μm for 1dB loss penalty, according to Fig. 3.30). It is mainly due to the use of slightly wider gratings (12 μm wide for our case), instead of using lower grating widths (i. e. standard 10 μm wide gratings [59]). The consideration of slightly wider gratings is important for fiber pigtailing issues, as it implies more relaxed fiber-to-chip alignment tolerances along the grating width. This is very important while fixing the optical fiber to the chip, and may make the process easier, as we will further discuss in chapter 5. Finally, Fig. 3.31 depicts the measured transmission spectrum of fabricated

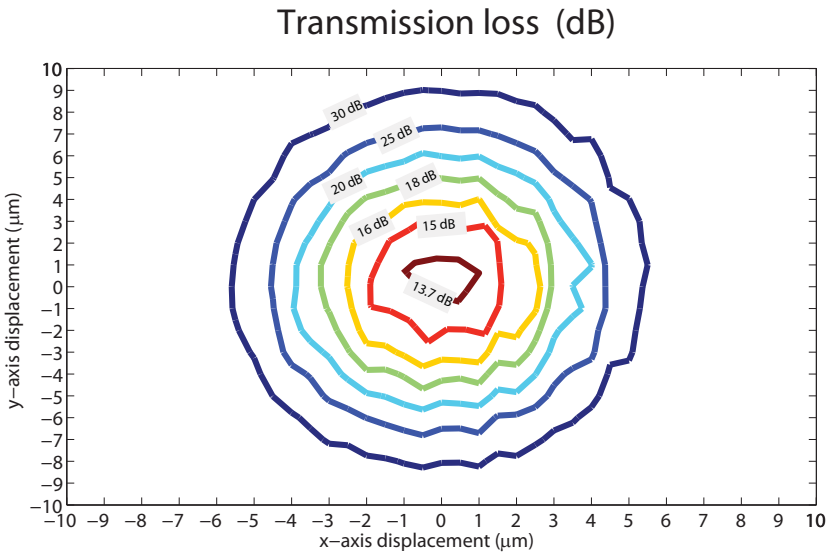


Figure 3.30: Measured alignment tolerances for device D3.

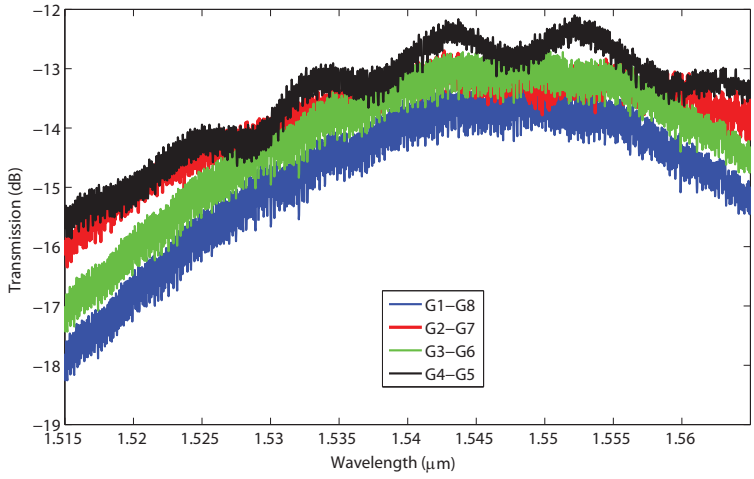
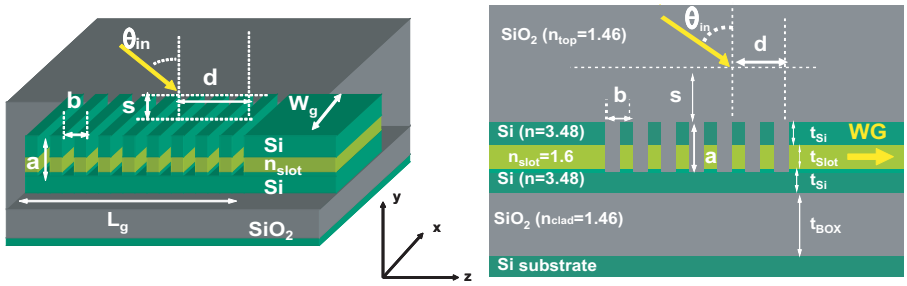


Figure 3.31: Measured transmission spectrum of fabricated gratings in design D3.



(a) (b)

Figure 3.32: (a) Proposed grating coupler structure. (b) Detail of the main parameters. Filling factor is 50%.

gratings in design D3.

3.4 Horizontal slot waveguide grating couplers

The proposed horizontal slot waveguide grating coupler structure is shown in Fig. 3.32(a). The entire grating is surrounded by a silica (SiO_2) index matching glue, so that fiber facet reflections are minimized. The grating is chosen to be 20 period long. Fig. 3.32(b) shows the design parameters used. Parameters of thicknesses of the slot waveguide layers are chosen so that the nonlinear performance in the waveguide is optimized, according to simulation results in [45]. The obtained silicon thickness is t_{Si}=200 nm. The considered t_{slot}=50 nm slot thickness is chosen to increase nonlinear performance in the slot region [45, 92]. As the slot is supposed to be composed of $Si-nc/SiO_2$ (SiO_x material) with x=10 % concentration of $Si-nc$, the slot refractive index (n_{slot}) is:

$$n_{slot} = (1-x)\cdot n_{SiO_2} + x \cdot n_{Si} = 1.65 \tag{3.15}$$

Light confinement in the slot is achieved for TM polarization, whose main electric field component lies along the y-axis direction (see Fig. 3.32(a)). The most important design parameters are the grating length (L_g), the grating width (W_g), the grating period (b) and the grating groove depth (a), which are also

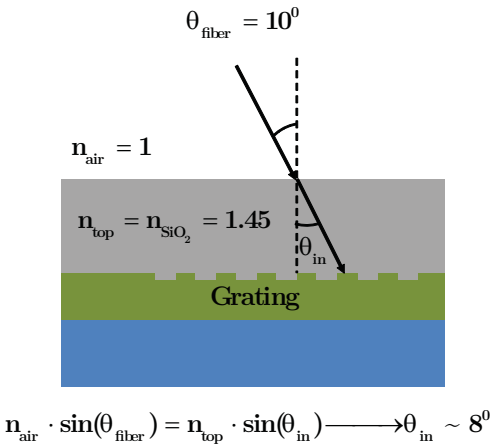


Figure 3.33: Snell′s law in the air-SiO_2 interface for calculating the incident angle in the grating coupler.

depicted in Fig. 3.32(a). As usual in conventional SOI grating coupler designs, the filling factor is initially ff=50%. The incident light in the grating slightly tilted (θ_{in}) to minimize the effect of second order diffraction, so that first order diffraction predominates (m=1). The fiber core center is also vertically separated from the grating by a distance s, and horizontally by a distance d. Parameters have been optimized to achieve maximum coupling efficiency for λ=1550 nm and TM polarization. If we consider a typical fiber tilt angle of θ_{fiber}=10 °, and taking into account that the fiber comes from air on top of the uppercladding layer (n_{top}), we can calculate the angle with which the light incides on the grating coupler by using the Snell′s law, resulting in θ_{in}∼8 ° (see Fig. 3.33).

3.4.1 Design

Similarly to Eq. 3.14, the grating period (b) can be here expressed as:

$$b = \frac{\lambda}{n_{eff} - n_{top}\sin(\theta_{in})} \tag{3.16}$$

As we have chosen $ff = 50\%$, n_{eff} in Eq. 3.16 will be the average value between the effective indices of the unperturbed and perturbed grating waveguide

regions, so depending on the etch depth (a). Since in slot grating couplers the field is highly confined between two high index contrast layers, the grating has to be deeply etched, so $a > t_{slot}+t_{Si}$. An average effective index of n_{eff}=2.1 was calculated for a fixed initial etching depth value of a=280 nm using a fully vectorial mode solver for a 12μm wide grating. For a grating covered by silica (n_{top}=1.46) and λ=1550 nm, the theoretical grating period is b=817 nm for θ_{in}=8°. Theoretically, the optimum horizontal fiber position (d) is equal to the grating coupling length (L_C). This coupling length is directly related to the fiber beam radius (ω_0) according to Eq. 3.8. For θ_{in}=8° and standard single mode fibers with 10 μm mode field diameter (MFD), ω_0=5 μm, so d= L_C =3.83 μm.

The grating width is chosen to be Wg=12 μm as before, so that we can study the 3D coupling problem via 2D simulations. The grating has been designed employing 2D finite-difference time-domain (FDTD) simulations. To calculate the power coupling efficiency in the slot waveguide, the grating in Fig. 3.32(b) is excited from the top by a 8° tilted Gaussian beam with normalized power. A power monitor placed in the slot waveguide measured the portion of the power of the launched field which has coupled to the waveguide (coupling efficiency). The grating is 20 period long (L_g=20b). An infinite silica BOX thickness (t_{BOX}) was chosen so the silicon substrate was not initially considered in the simulations. The fiber was also vertically separated from the grating by a distance s=1 μm. The first design step was to optimize the grating groove depth (a) to achieve the maximum coupling efficiency by using the grating period (b) and the horizontal fiber position (d) obtained theoretically. Fig. 3.34 depicts the simulation layout on the E-field distribution in the slot grating during the 2D FDTD simulation for TM polarization. For maximum coupling efficiency and a 50% filling factor, an optimum grating groove depth of a=265 nm was obtained. Simulations were used to verify the theoretical period calculations.

In Fig. 3.35 the simulation results show the power coupling efficiency as a function of the grating period, for a=265 nm, d=3.83 μm and ff=50%. The optimum grating period in terms of coupling efficiency is b=807 nm for θ_{in}=8°. This result is in good agreement with the theoretical values. Coupling efficiency of 32% is achieved. The second order diffraction efficiency was also evaluated

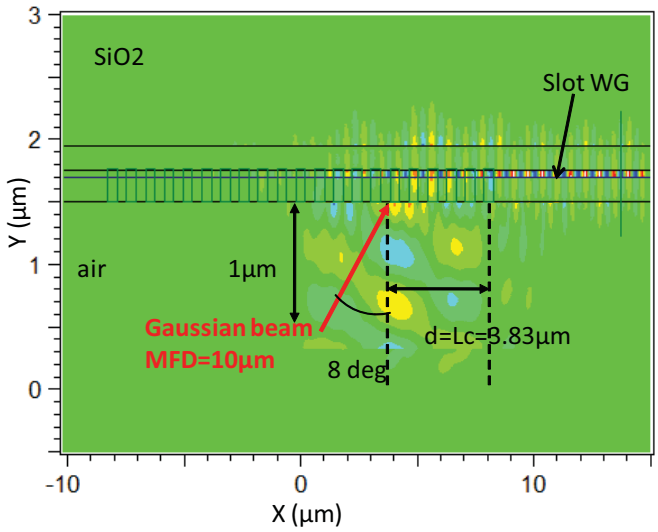


Figure 3.34: E-field distribution in the slot grating when optimizing the grating groove depth via 2D FDTD simulations for TM polarization.

by obtaining light diffracted in negative z direction (see Fig. 3.32). Negligible second order diffraction efficiency was obtained.

Having optimized the fiber position and both the grating period and the grating groove depth, the next step was to optimize the silica BOX thickness, t_{BOX}. The grating creates upward and downward propagating waves. Downward waves partially reflect at the oxide-substrate interface and interfere with the upward waves. Depending on the oxide buffer thickness, constructive or destructive interference can occur. Fig. 3.36 shows simulation results for the power coupling efficiency as a function of the silica BOX thickness. It can be seen that coupling efficiency follows a sinusoidal curve as a function of the silica BOX thickness so that coupling efficiency significantly changes from 16% to 48%. The average value of the coupling efficiency curve in Fig. 3.36 corresponds to the obtained coupling efficiency for the previous studied case in Fig. 3.35, in which the substrate effect was not considered. Maximum power coupling efficiency increases to 48% if, for example, a silica BOX thickness of t_{BOX}=2.2 μm is chosen.

Sensitivity to fabrication and alignment tolerances of the structure has also

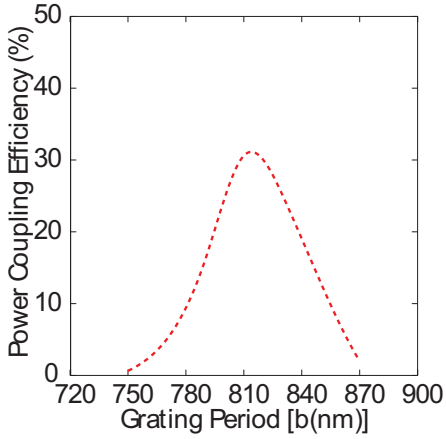


Figure 3.35: Simulation results for the power coupling efficiency as a function of the grating period for a=265nm, s=1.5μm, d=3.83μm, θ_{in}=8° and ff=50%. An infinite silica BOX thickness is chosen.

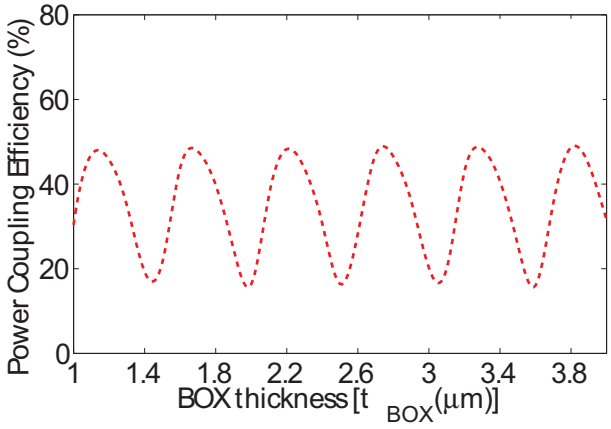


Figure 3.36: Simulation results for the power coupling efficiency as a function of the silica BOX thickness (t_{BOX}) for a=265nm, s=1.5μm, d=3.83μm, ff=50%, θ_{in}=8° and optimum grating periods obtained in Fig. 3.35.

been analyzed. To study fabrication tolerances, simulations were performed with different filling factors as well as different etching depths for the previously de-

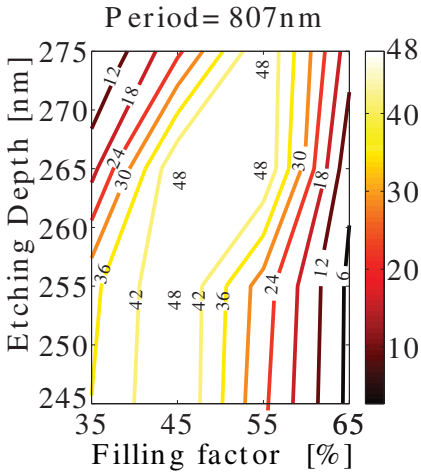


Figure 3.37: Simulation results for the power coupling efficiency (in %) as a function of the filling factor and the etching depth.

signed grating coupler. The filling factor is defined as $ff = w/b$, being b the grating period, and w the unperturbed grating half-period width. Fig. 3.37 shows coupling efficiency results when varying those parameters. It is obtained that the coupling efficiency is almost constant for etching depth variations of ± 10 nm or filling factor changes of $\pm 5\%$ (which is equivalent to period changes of ± 17 nm and ± 20 nm for the negative and the positive detuned grating, respectively). To study alignment tolerances, the incident angles as well as the horizontal fiber positions were varied. Fig. 3.38 shows coupling efficiency results when varying those parameters. The coupling efficiency is also almost constant for tilt angle variations of $\pm 2^\circ$ or horizontal fiber position changes of ± 3 μm.

Once the design for λ=1550 nm is finished, the spectral response of the power coupling efficiency has been calculated. Fig. 3.39 shows the power coupling efficiency as a function of the wavelength for the optimum design. A 35 nm 1dB-bandwidth is achieved.

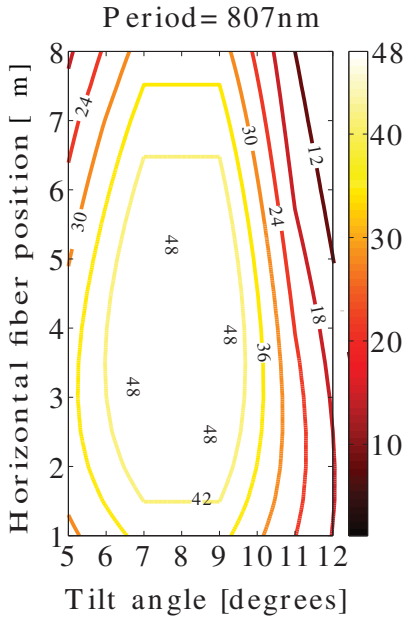


Figure 3.38: Simulation results for the power coupling efficiency (in %) as a function of the tilt angle and the horizontal fiber position.

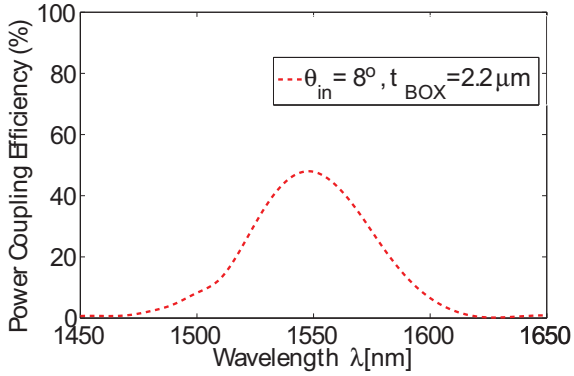


Figure 3.39: Simulation results for the spectral response of the coupling efficiency for optimum designs.

3.4.2 Fabrication and experimental results

The samples were fabricated in CEA-Leti[1] (Grenoble-France), within the framework of the FP6-IST-NMP PHOLOGIC project [2]. As fabrication production line in LETI is with commercial wafers with 220 nm/2 μm Si/SiO_2 thicknesses values, designs were redesigned for this layer thicknesses, following the same procedure as the previously described. So, here t_{Si}=220 nm for the same slot thickness t_{slot}=50 nm and ff=50 % filling factor. We first calculated the effective index in the slot waveguide to see how different it is compared to the silicon thickness used in the design section. As the effective index did not differ so much (as the optical mode is highly confined in the slot region), and according to Eq. 3.16, we can conclude that the optimum design value of the period of the grating will be the same, so b=807 nm. With this optimum grating period, we calculated using 2D-FDTD simulations the optimum etching depth for obtaining maximum couplign efficiency for a SiO_2 BOX thickness of t_{BOX}=2 μm. Fig. 3.40 depicts simulation results for the coupling efficiency as a function of the etching depth (a). It is obtained that the maximum coupling efficiency is 27 % for an optimum etching depth of a=305 nm.

Horizontal slot waveguides were first fabricated on commercial SOI wafers of a 220 nm Si layer on top of a 2 μm thick buried oxide, using CMOS compatible microelectronic tools at CEA-LETI. A 50 nm thick Si-nc/SiO_2 (SiO_x) layer was grown by plasma-enhanced chemical-vapor deposition (PECVD), and annealed at 1000 ° in order to promote Si-nc formation by Si/SiO_2 phase separation. The Si-nc/SiO_2 material (SiO_x) was also formed by embedding 10% concentration of crystalline Si (Si-nc) in SiO_2. The wafers were then covered by amorphous silicon for the Si top-slab layer of the sandwich structure. Fig. 3.41(a) depicts a SEM image of fabricated slot waveguides in LETI, showing actual layer thickness of all

[1]Located in the heart of an exceptional scientific environment, the CEA-Leti Institute for micro- and nanotechnology research offers researchers and students alike a rewarding place to work. See http://www-leti.cea.fr

[2]PHOLOGIC project was intended to explore the mass-manufacturing compatibility of nonlinear photonic materials (CdTe and Si-nc) and their associated fabrication processes with CMOS processing lines using a highly scalable photonic logic gate structure as functional validation device (http://http://www.ist-phologic.org).

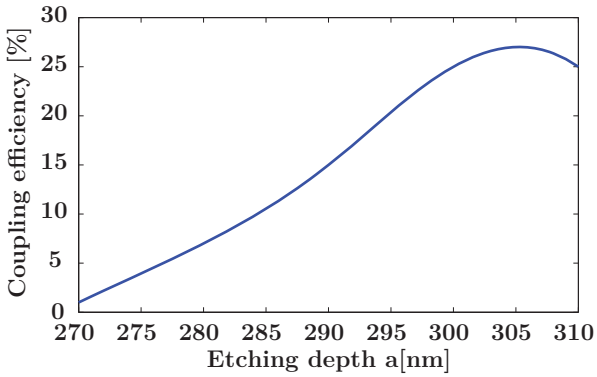
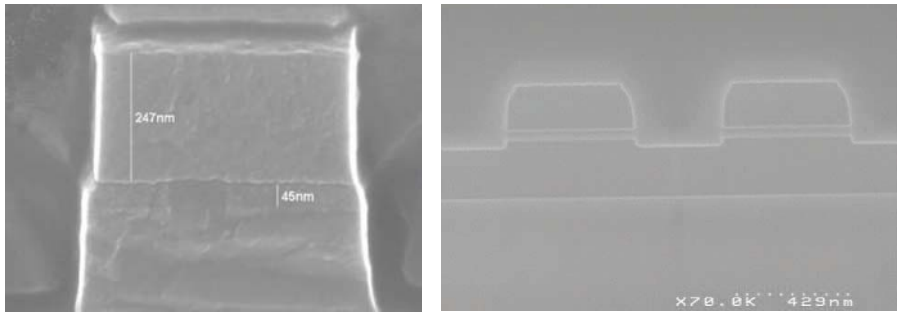


Figure 3.40: Simulation results for the coupling efficiency as a function of the etching depth.



(a) (b)

Figure 3.41: (a) SEM image of the fabricated slot waveguide at LETI. (b) SEM image of the fabricated grating couplers.

the layers after fabrication. An actual slot thickness of t_{Si}=45 nm and top silicon thickness of $t_{Si,up}$=247 nm is obtained.

A 150 nm thick SiO2 layer was then deposited over the wafer for performing the grating mask. To transfer the grating and the waveguide layouts to the wafer, deep-UV lithography at 193 nm was then applied. Finally, in order to protect the structures, a SiO_2 top cladding was deposited by PECVD. Fig. 3.41(b) depicts a Scanning Electron Microscope (SEM) image of the fabricated grating couplers.

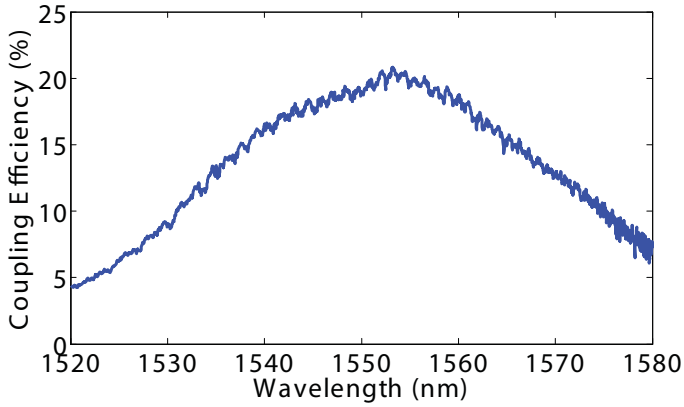


Figure 3.42: Experimental coupling efficiency spectral response.

SEM measurements of the gratings were performed, so that actual grating period is 808 nm, and actual thickness of the SiOx layer was found to be 45 nm. A 310 nm grating etching depth was also measured.

The measured spectral response of the fabricated sample is depicted in Fig. 3.42. 20% experimental maximum coupling efficiency is obtained. From design simulations, a maximum theoretical coupling efficiency of 25% was expected to obtain for t_{BOX}=2 μm and the actual etching depth measured after fabrication a=310 nm, according to Fig. 3.40. So, obtained experimental results are in a good agreement with theoretical expected results. According to experimental results on Fig. 3.42, a 20 nm 1dB-bandwidth spectral response is also obtained.

3.5 Summary and conclusions

In this chapter we have studied in detail the fiber-to-chip coupling via grating couplers, and provided theory, simulation, fabrication, as well as experimental results of the studied grating coupler structures. We first started with some theoretical basics related to diffraction gratings to introduce waveguide grating couplers, and the most important formulas regarding the coupling problem in SOI based grating couplers were then reviewed. After reviewing theoretical aspects,

Design param.	**Sim. results**	**Fab. tol. @ 1dB penalty**	**Align. tol. @ 1dB penalty**
Period Λ=600 nm	50% coupling efficiency	ed: $\pm$10 nm	θ: $\pm 2^\circ$
Etch depth ed=70 nm	40 nm 1dB bandwidth	ff: $\pm$10 %	d: ± 2 μm

Table 3.4: Summary of optimal design of the proposed air-covered grating coupler and obtained simulation results @ λ=1.55 μm, for SOI wafers with 250 nm/3 μm Si/SiO_2 thicknesses. We considered coupling to standard singlemode optical fibers with MFD=10 μm.

the modelling for solving the coupling problem via two dimensional approximation was proposed, and concluded its validation for the case of 12 μm $\times$ 12 μm area sized proposed gratings, and considering coupling to standard singlemode optical fibers with MFD=10 μm. We focused our design on SOI wafers with 250 nm/3 μm Si/SiO_2 thicknesses, considered an air uppercladding on top of the grating, forced a grating filling factor or duty cycle to ff=50%, and fixed a fiber tilt angle of θ=10° (weak detuned gratings). A brief discussion regarding the optimal position of the optical fiber on the surface of the proposed SOI grating design was also addressed, concluding that optimal distance for our case is d=3.8 μm. After applying theoretical issues previously pointed out, we designed our SOI grating structure for optimum coupling at telecom wavelength λ=1.55 μm. For the simulations we used 2D-FDTD tools. Table 3.4 summarizes the obtained optimal design parameters of the grating couplers, as well as the main obtained simulation results. The fabrication of designed grating couplers was then carried out, through e-beam lithography and ICP dry etching fabrication processes. A particular measurement setup was also built for characterizing the fabricated samples. Table 3.5 summarizes the best obtained experimental results for the grating coupler efficiency and 1 dB bandwidth @ λ=1.55 μm, for actual measured grating coupler parameters (etch depth and filling factor) after fabrication, and compared the obtained efficiency with the expected from simulation of fabrication tolerance analysis. In conclusion, the highest measured efficiency is 31 %, which is close to the 40 % efficiency expected from fabrication tolerance

Etch depth	Filling factor	Efficiency (expected)	Efficiency (measured)	1 dB bandwidth (measured)
60 nm	45.8 %	40 %	31 %	30 nm

Table 3.5: Summary of measured actual grating parameters after fabrication, and experimentally obtained 1dB bandwidth and coupling efficiency @ λ=1.55 μm, compared to the expected efficiency from fabrication tolerance simulation results.

Etch depth	Filling factor	Efficiency (expected)	Efficiency (measured)	Align. Tol. (measured)
55 nm	52 %	30 %	24 %	$\pm$2 μm @ 1dB penalty

Table 3.6: Summary of measured actual grating parameters after fabrication, and experimentally obtained alignment tolerances and coupling efficiency @ λ=1.55 μm for multiport SOI chip when coupling to a fiber array.

simulations. For experimentally obtaining the alignment tolerances of grating couplers, we studied the coupling between a commercial 8-fiber fiber array and a multiport SOI chip containing 8 grating couplers. A specific layout for this task was performed, according to the fiber array specifications, such as the fiber spacing of 250 μm. In this case, the gratings were fabricated as previously explained, and according to same grating design summarized in Table 3.4. Table 3.6 summarizes the best obtained experimental results for the grating coupler efficiency and alignment tolerances @ λ=1.55 μm, for actual measured grating coupler parameters (etch depth and filling factor) after fabrication, and compared the obtained efficiency with the expected from fabrication tolerance simulations. In conclusion, the highest measured efficiency is 24 %, which is close to the 30 % efficiency expected from fabrication tolerance simulations. Also in conclusion, the obtained $\pm$2 μm @ 1dB penalty experimental alignment tolerances are the same than expected from theoretical results, also previously pointed out in Table 3.4. Moreover, $\pm$3 μm @ 1dB penalty alignment tolerances were experimentally obtained along the grating width, due to the use of 12 μm wider gratings. After

Si slot thickness	SiO_2 buffer thickness	Etch depth	Efficiency
200 nm	∞	265 nm	32%
200 nm	2.2μm	265 nm	48%
220nm	2μm	305 nm	27%

Table 3.7: Summary of optimal design of the proposed horizontal slot waveguide grating coupler and obtained simulation results @ λ=1.55 μm, for a grating period of 807 nm, a 50 nm thick slot region, and different silicon and SiO_2 buffer layer thickness. The grating is supposed to be covered by SiO_2, and the slot region is filled with SiO_x with x=10%. We considered coupling to standard singlemode optical fibers with MFD=10 μm, with a fiber tilt angle of θ_{fiber}=10 °.

finishing with the conventional SOI grating coupler design and experimentation, specific designs of gratings for horizontal (sandwiched) slot waveguides were proposed, for coupling to standard singlemode optical fibers with MFD=10 μm. We first focused our designs on horizontal slot waveguides with a 200 nm silicon thickness for both upper and low slot wavegudie silicon layers, and a 50 nm thick intermediate slot region layer, thus optimizing the nonlinear performance of the waveguides @ λ=1.55 μm. We also supposed that the slot region was filled with silica rich on silicon nanocrystals (SiO_x material), with x=10% concentration of silicon. The grating was also supposed to be covered by SiO_2, and considered a filling factor of ff=50 %. An infinite thickness for the SiO_2 layer of the SOI wafer was initially taken into account. We studied the case of θ_{fiber}=10 ° fiber tilt angle, which corresponds to θ=8 ° incident angle on the grating surface, taking into account the SiO_2 uppercladding layer effect. Applying the previous studied grating coupler theory, and performing an exhaustive design via 2D-FDTD simulations, optimum designs were then obtained. Table 3.7 summarizes the obtained optimal design of the proposed horizontal slot waveguide grating coupler and obtained simulation results @ λ=1.55 μm, for obtained optimum grating period of 807 nm. After optimizing the slot waveguide grating coupler, we also performed simulation results for the coupling efficiency as a function of the SiO_2 layer thickness of the SOI wafer. We obtained maximum coupling efficiency for particular

Period	Etch depth	SiO_x thickness	Si top thickness	Efficiency (measured)	1dB bandwidth (measured)
808 nm	310 nm	45 nm	247 nm	20%	20 nm

Table 3.8: Summary of actual slot grating dimensions after fabrication and main obtained experimental results.

values of the SiO_2 layer thickness, as also shown in Table 3.7. Then, the fabrication of the structures was carried out in CEA-LETI using CMOS compatible fabrication tools. As SOI wafers with 220nm/2μm Si/SiO_2 layer thicknesses were going to be used for the fabrication, we first optimized the grating etch depth for slot waveguide with 220 nm thickness for both upper and low silicon layers, 2μm thick SiO_2 buffer layer, and mantaining a 50 nm thick intermediate SiO_x slot layer. Table 3.7 summarizes the optimal obtained simulation results for this particular case, also for a grating period of 807 nm. Then, the fabrication of the slot waveguides and the gratings was performed in LETI, basically based on deep-UV lithography, PECVD annealing to promote the SiO_x layer, amorphous silicon deposition on top for the Si top-slab layer of the sandwich structure, and PECVD deposition for the SiO_2 uppercladding. After characterisation of the samples, by using the same experimental setup than previously used for conventional grating couplers, the actual measured dimensions of the fabricated gratings and the main experimental results are summarized in Table 3.8. In conclusion, experimental 20% coupling efficiency was demonstrated, in comparison with 27% coupling efficiency expected from fabrication tolerance graph simulations, for actual grating dimensions after fabrication.

So, we have demonstrated grating structures for both conventinal and horizontal slot based silicon waveguides. Grating couplers have interesting advantages such as wafer testing capability. Due to their capability for injecting and extracting light from the wafer surface, the whole wafer can be tested easily after fabrication without the need for cut processing the dies individually. Moreover, from our experience when testing the grating based devices, measurable power is observed just by positioning the fibers roughly over the grating area without

doing a so exhaustive fine alignment, which can be more than enough to know if the device works properly in a quick way. This can be extended to in-wafer device testing, and a good feedback about the performance of the devices after fabrication can be obtained almost immediately. We have also demonstrated the benefits of using grating couplers for coupling to fiber in multiport SOI devices, due to the relatively large alignment tolerances offered by the grating couplers. This important outcome can be smartly exploited for performing the pigtailing of multiple optical fibers to the devices in a efficient way, and obtaining coupling loss after pigtailing process similar to the previously expected. This issue will be studied in detail in chapter 5.

One of the main problems that the silicon photonics community is facing nowadays is to improve the coupling efficiency of the grating couplers. Although we have not done so much work in that way, we will address in the perspective section of the last chapter some little work and further improvements for the development of more efficient grating couplers.

Chapter 4

Inverted taper-based fiber-to-chip coupling

This chapter goes into detail about the second of the coupling strategies we deal with in this thesis: the inverted taper. Theory, design, fabrication, as well as experimental results of different inverted taper-based fiber coupler configurations are addressed.

4.1 Introduction

An inverted taper is basically known in literature as a SOI waveguide whose width decreases with the propagation direction from chip to fiber. Fig. 4.1 depicts an example of a SOI linear inverted taper of length L. Basically, the SOI waveguide (width ω_0, thickness h) is laterally tapered down along the propagation direction ($z > 0$), so its tip width is $w_t < w_0$. Thus, the taper width (W) depends on z: $W = W(z)$. The entire structure is supposed to be surrounded in SiO_2. The electric field distribution of the TE fundamental mode propagating along the taper is depicted in Fig. 4.2, for different waveguide widths and λ=1.55 μm. At the origin ($z = 0$), the optical mode is well confined in the waveguide core ($W(z = 0) = w_0 = 500$ nm). At a certain position for which the taper width is $W = 250$ nm, the optical mode is less confined in the waveguide core, and a major part of the energy of the mode is localized in the waveguide cladding. In fact, the actual effective index of the optical mode (n_{eff}=1.85) is lower than the

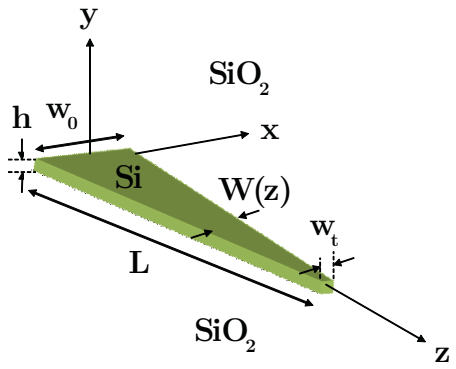


Figure 4.1: Example of a SOI inverted taper of length L. Basically, the SOI waveguide (width ω_0, thickness h) is linearly tapered down along the propagation direction chip-to-fiber ($z > 0$), so that the inverted taper tip width is w_t. Thus, the taper width (W) depends on z: $W = W(z)$. The entire structure is surrounded in SiO_2.

effective index of the optical mode at the origin (n_{eff}=2.498), and is now closer to the refractive index of the cladding (SiO_2, $n = 1.45$) than to the refractive index of the core (Si, $n = 3.48$). At another position for which the taper width is now $W = 125$ nm, the optical mode is even less confined in the waveguide core, compared to the case of $W = 250$ nm. Now, almost the total energy of the mode is localized in the waveguide cladding, and the effective index of the mode ($n_{eff} = 1.5$) is even closer to the refractive index of the waveguide cladding. So, the optical mode is expanding evenescently from the waveguide core along the propagation direction. If the taper is sufficiently adiabatic (L large enough[1]), it is achieved 100% efficient conversion between the optical mode at the origin and the optical mode at the inverted taper tip w_t [56]. This fact is smartly used for

[1]For the case of the linear taper in Fig. 4.1, $W(z) = \pm\left[w_0 - \frac{(w_0 - w_t)}{L} z\right]$, with $w_0 > w_t$, being $W(z = 0) = w_0$ the SOI waveguide width (typically w_0=500 nm), and $W(z = L) = w_t$ the taper tip width, which is a fixed value, depending on the mode profile size required for coupling to the desired fiber. Adiabatic means an extremely relaxed slope, so $\frac{w_0 - w_t}{L} <<< 1$, or $L >>> w_0 - w_t$. As both w_0 and w_t are expressed in [nm], L is expressed in [μm], and 1 μm = 1000 nm, we obtain $L > 1000 \cdot (w_0 - w_t)$.

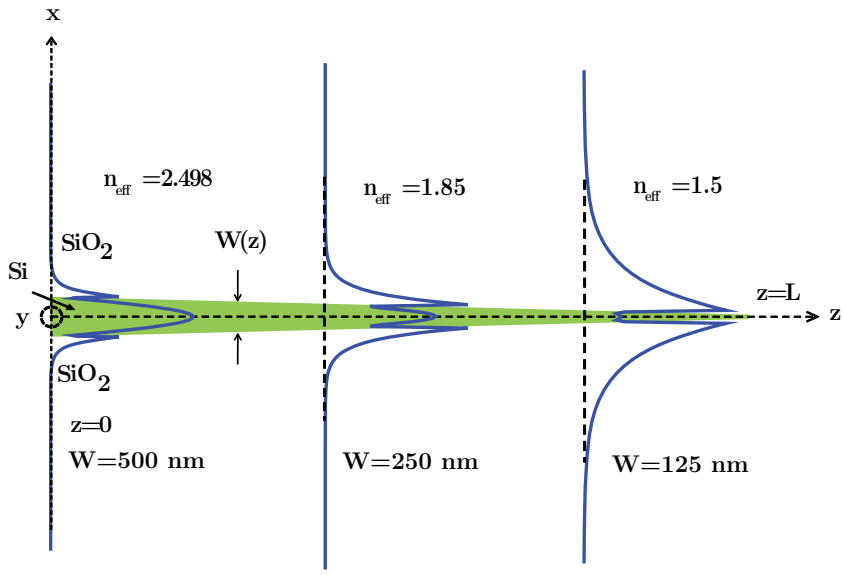


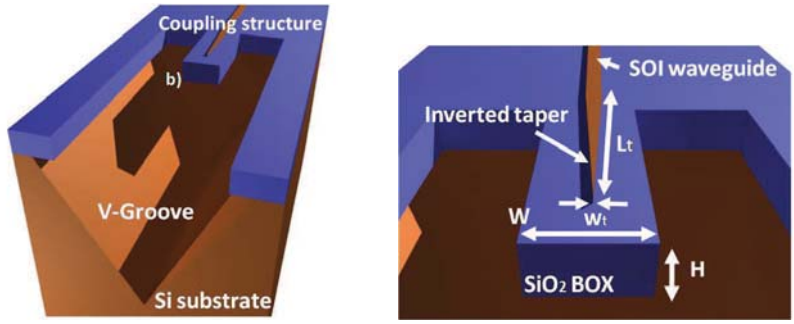
Figure 4.2: E-field distribution of the TE fundamental mode propagating through the SOI inverted taper depicted in Fig. 4.1 for different waveguide widths and λ=1.55 μm.

coupling SOI photonic waveguides to singlemode fibers. The keys are to choose both optimal tip width (w_t) and taper length (L) for which the optical mode at the inverted taper tip is wide enough for matching to the fiber mode, assuring that the mode conversion along the taper length is achieved efficiently. It is important to notice that the effective index of the tip mode also has to be as close as possible to the effective index of the optical fiber mode. Under this coupling mechanism, different configurations have been proposed in literature, and were reviewed in chapter two. As seen, most of the inverted taper configurations already published are single stage, and they offer a good performance for coupling to low MFD fibers, such as lensed fibers, with typically 2.5-4μm MFD. The main reason why is that it is not enough efficient to get a good mode conversion with just one taper stage for achieving a good coupling to standard butt-fibers with 10μm MFD. It will imply to get a wider optical mode at the inverted taper tip edge, which is not really easy to get with a single stage inverted taper. Inverted

taper structures provide low coupling loss, a large bandwidth (>100nm) and can also be designed for polarization independency. However, their mechanical alignment tolerances remain substantially below 1 μm, mainly due to the dependency of the distribution of the optical power in the multimode fiber-adapted waveguide with the optical fiber displacement, which is crucial for pigtailing and packaging, especially in the case of multiple fiber attachment. However, the fabrication of inverted taper structures is rather complicated compared to grating couplers. First, getting the required nanotip of the taper is, in some cases, beyond UV lithography limits, as it can be even below 100 nm width. Second, the fabrication of the fiber-adapted waveguide on top of the taper makes the fabrication much more complicated, as it implies new lithography and etching steps in the fabrication process, also doing the final process longer and more expensive. Moreover, the integration of polymers with silicon in the same platform is also disadvantageous, as they require specific and particular processes, which, in many cases, it is not easy to integrate with conventional fabrication processes for silicon material used in CMOS fabrication lines. Trying to overcome such limits, here we propose a concept, which is also integrated with V-groove structures for enhancing the fiber-chip alignment, and will be studied in detail in the next sections. Basically, the use of the SiO_2 buffer layer of the SOI wafer is proposed for using as the fiber-adapted waveguide for the coupling, thus avoiding the need for incorporating new materials for the fabrication. For being able to do this, the substrate of the wafer under the SiO_2 material needs to be removed from the wafer, and the creation of a V-groove structure can be performed in the sample substrate, thus also allowing to place the fiber strategically for alignment improving porpuses. Moreover, the design is also carried out to be polarization insensitive.

4.2 Inverted taper approach for V-groove integration

The proposed inverted taper-based coupling structure able for V-groove integration is shown in Fig. 4.3(a). A drawing detailing all design parameters of the structure is also shown in Fig. 4.3(b). The main design parameters are the SiO_2



(a) (b)

Figure 4.3: (a) Proposed inverted taper-based structure and (b) detail of its main design parameters.

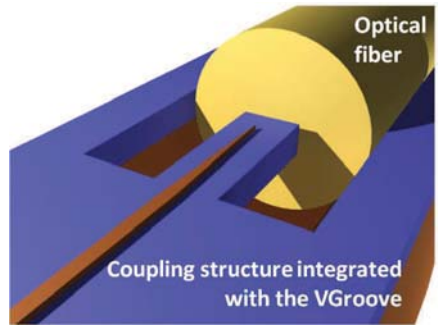


Figure 4.4: Optical fiber placed on the VGroove integrated with the proposed coupling structure for self-alignment purposes.

waveguide dimensions (width W and height H) and the taper parameters (length L_t and tip width w_t). The realization of the structure is fully compatible with standard CMOS production lines. The most important feature of the proposed structure is that it is fully integrable with V-groove structures as illustrated in Fig. 4.4.

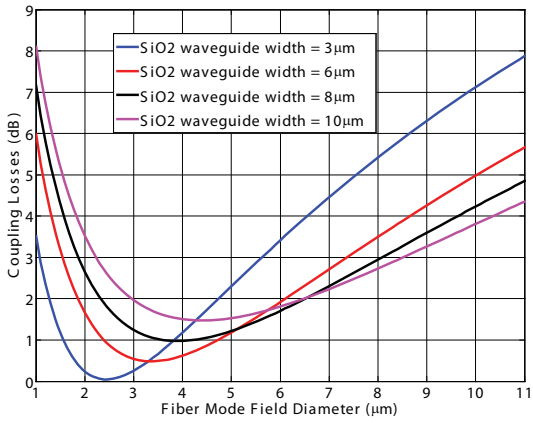


Figure 4.5: Coupling losses between the SiO_2 waveguide and the optical fiber as a function of the fiber mode field diameter for different waveguide widths, λ=1550nm and both TE and TM polarizations.

4.2.1 Design

SOI wafers of 205nm/3μm Si/SiO_2 layer thicknesses were initially considered in the design, as they were the only wafers available at the Nanophotonics Technology Center of the Universidad Politécnica de Valencia. Due to the SiO_2 SOI wafer layer thickness, the height of the SiO_2 waveguide (H) here is fixed to 3μm. The objectives are to find the optimum SiO_2 waveguide width (W) and the optimum inverted taper parameters (W_t and L_t) to achieve the lowest coupling loss between the proposed structure and the optical fiber. The choice of the optical fiber is also important, due to fabrication tolerances of optical fibers, as the fabrication of silicon etched V-groove is very difficult, as we will further discuss. The fabrication tolerances of the optical fiber are so very critical for the alignment mainly due to imperfections in the V-grooves also due to the very precise control of the micromachining used for their fabrication. The design is also carried out to obtain a polarization insensitive structure. A step by step design analysis of the proposed inverted taper-based structure is explained on the following sections. The analysis starts with the SiO_2 waveguide design and the choice of the optical

fiber to achieve the lowest coupling losses to high mode field diameter singlemode fibers, and taking into account these fibers because they offer better alignment tolerances. Then, the optimum inverted taper tip width and length are designed.

4.2.1.1 SiO_2 waveguide design and optical fiber choice

The objective is to find the optimum SiO_2 waveguide width (W) to get the lowest coupling losses between the SiO_2 waveguide and the optical fiber. For the calculation of the coupling loss (CL), expressed in dB, we can use the logarythm form of the overlap integral used for grating couplers in Eq. 3.11 in the fiber-waveguide interface (S):

$$CL(dB) = -10\log_{10}\left[\left|\iint_S E \times H^*_{fib} dS\right|^2\right] \tag{4.1}$$

where the E-field normalized profile of the fundamental mode in the SiO_2 waveguide (E) is obtained, for different SiO_2 waveguide width values, by means of a 3D mode solver based on the BPM, and the H-field normalized profile of the fiber mode (H_{fib}) is approximated by a Gaussian-like beam as a function of its mode field diameter (MFD). Fig. 4.5 shows the estimated coupling losses between the SiO_2 waveguide and the fiber as a function of the fiber MFD for different SiO_2 waveguide width values and λ=1550 nm. A polarization insensitive behaviour of the coupling efficiency in the SiO_2 waveguide-fiber interface is achieved so results shown in Fig. 4.5 are valid for both TE and TM polarizations. Regarding the fiber MFD, it strongly has an impact in the choice of the optical fiber. As seen in Fig. 4.5, almost negligible coupling loss are obtained in the fiber-SiO_2 waveguide interface for a waveguide width of W=3 μm if a fiber with MFD=2.5 μm is chosen. Unless commercial tapered-lensed fibers with MFD downto 2.5 μm can be obtained, fabrication tolerances of such kind of optical fibers may make it difficult to achieve an accurate alignment between the fiber and the coupling structure when placing the optical fiber in the V-groove.

Table 4.1 depicts the most important fabrication tolerances in terms of fiber-waveguide alignment reported in literature of commercial lensed fibers from OZOp-

	Lensed fiber	***HNA* fiber**	**SMF fiber**
MFD	2.5 ±0.3 μm	5±1 μm	10.4±0.8 μm
Cladding diameter	125 ±0.7 μm	125±1 μm	125±0.7 μm
Core-Cladding concentricity	≤±0.7 μm	≤±0.5 μm	≤±0.5 μm
Total tolerances	≥±1.7 μm	≥±2.5 μm	≥±2 μm

Table 4.1: Fabrication tolerances of different kinds of optical fibers related to the fiber-waveguide alignment @ λ=1550 nm.

tics company[1]. Total estimated tolerances rely on more than ±1.7 μm, which is of the order of the fiber MFD (here MFD=2.5 μm), thus making very difficult the alignmnet of the optical fiber with the coupling structure in the V-groove. Moreover, the fabrication parameters of tapered fibers are only valid for distances between the edge of the fiber and the coupling plane lower than the working distance fabrication parameter, which typical value is 14±2 μm for OZOptics fibers. We can so think of using high numerical aperture (HNA) fibers for the coupling. Ultra-High NA fibers provide excellent coupling efficiencies to high NA waveguides. Typical MFD of a HNA fiber is 5μm. As seen in Fig. 4.5, 1.5 dB coupling loss are obtained in the fiber-SiO_2 waveguide interface for a waveguide width value of W=6-8μm. Fabrication tolerances of commercial HNA fibers from NUFERN company[2] are also depicted in Table 4.1. Total estimated tolerances are higher than ±2.5 μm, which is half of the fiber MFD (5 μm), being also inacceptable as in the case of the lensed fiber. As a final choice, the use of standard singlemode fibers (SMF) is then proposed. Table 4.1 also depicts fabrication tolerances of commercial SMF fibers from CORNING company[3]. Total important tolerances of SMF fibers in terms of fiber-waveguide alignment rely on ±2 μm. This value is about the fifth of the MFD (10.4 μm), thus making easier the fiber-waveguide alignment in the V-groove. So, due to the tolerances, SMF would be the better solution for this paticular application. As it is shown in Fig. 4.5, the estimated coupling losses for an 8μm wide SiO_2 waveguide and a single-mode

[1] http://www.ozoptics.com/ALLNEW_PDF/DTS0080.pdf
[2] http://www.nufern.com/specsheets/psgsf3125.pdf
[3] http://www.photonics.byu.edu/FiberOpticConnectors.parts/images/smf28.pdf

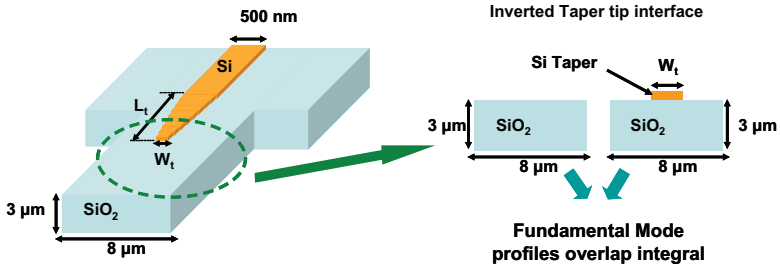


Figure 4.6: Detail of the interface between the fiber-adapted SiO_2 waveguide with and without the inverted taper on top. Procedure to evaluate the coupling losses in that interface.

fiber with MFD=10μm are around 4.3dB. If the SiO_2 waveguide gets wider (e.g. 10μm width), the estimated coupling losses are only about 0.4dB less than for the 8μm wide SiO_2 waveguide. Therefore, in order to minimize as much as possible the SiO_2 waveguide dimensions, the 8μm wide SiO_2 waveguide case has been chosen.

4.2.1.2 Inverted taper design

The interface depicted in Fig. 4.6 has been considered to find the optimum tip width (W_t) of the inverted taper. According to Fig. 4.6, it is possible to obtain the fundamental mode profiles of both the fiber-adapted SiO_2 waveguide with and without the inverted taper on top, as it is shown in Fig. 4.6. The electric field of the fundamental mode profiles were calculated using a full vectorial mode solver based on the BPM. Coupling losses are then calculated by means of their overlap integral. Fig. 4.7 shows the coupling losses between the SiO_2 waveguide with and without the inverted taper on top as a function of the tip inverted taper tip width for TE and TM polarizations and λ=1550 nm. As it can be seen in Fig. 4.7, almost negligible coupling losses for both TE and TM polarizations are achieved when the inverted taper tip width is lower than 200 nm. On the other hand, coupling losses also do not significantly change as the inverted taper tip width is higher than 400 nm. This occurs because the mode is mainly located in the high index contrast silicon waveguide and therefore only a small part of

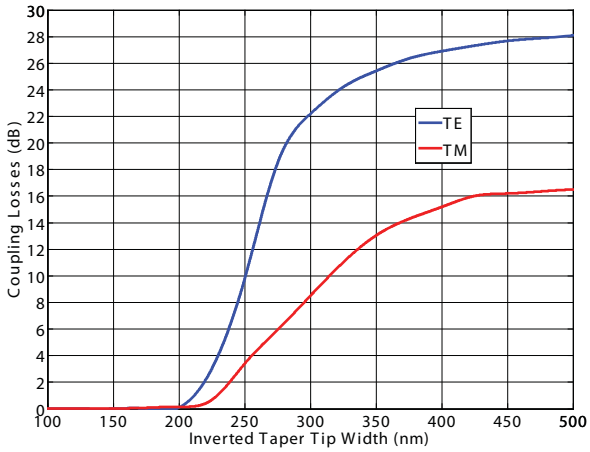


Figure 4.7: Coupling losses between the SiO_2 waveguide with and without the inverted taper on top as a function of the inverted taper tip width, λ=1550nm and for both TE and TM polarizations.

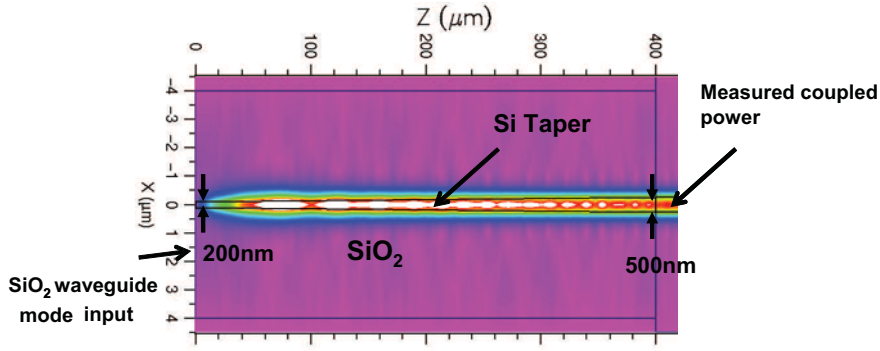


Figure 4.8: Electric field distribution in a 400μm long inverted taper obtained by means of a 3D-BPM simulation.

the mode profile overlaps with the mode profile of the SiO_2 waveguide. In our case, inverted taper tip widths lower than 200 nm are desirable to achieve a polarization insensitive coupling structure. However, wider taper tips are more

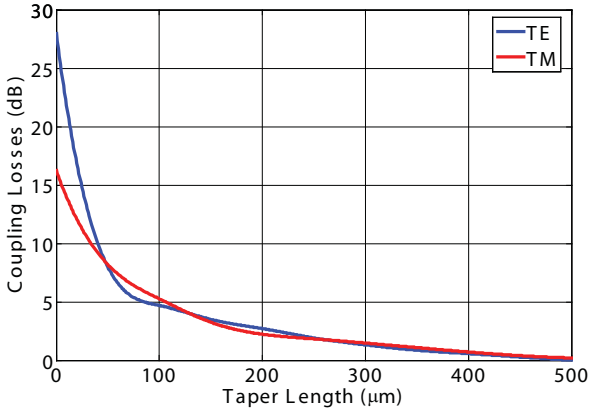


Figure 4.9: Coupling losses as a function of the inverted taper length for both TE and TM polarizations and a 1550nm input signal wavelength.

suitable to reduce the complexity of the fabrication. Therefore, the optimum value will be W_t=200 nm. The optimum inverted taper length (L_t) has been designed by means of 3D-BPM simulations using the inverted taper tip width (W_t=200nm) and the SiO_2 waveguide width (W_g=8μm) that were found to be the optimum ones in the previous sections. Fig. 4.8 shows the electric field distribution in a 400m long inverted taper obtained by means of a 3D-BPM simulation. The structure is excited by the SiO_2 waveguide fundamental mode at λ=1550 nm for each polarization. The power coupled at the 500 nm wide Si waveguide is measured to evaluate coupling losses.

Fig. 4.9 shows the coupling losses as a function of the inverted taper length for both TE and TM polarizations and λ=1550 nm. Looking at Fig. 4.9, it can be seen that coupling losses decrease as the inverted taper gets longer due to a lower mode mismatching. Furthermore, it is interesting to notice that this improvement is similar for both TE and TM polarization. On the other hand, it can be seen that the highest coupling losses for the case of a zero length taper are in agreement with the results shown in Fig. 4.7 for the case of 500nm width. An inverted taper lengh of L_t=400 μm has been chosen as the most optimum one taking into account the trade off between minimum coupling losses and short lengths for

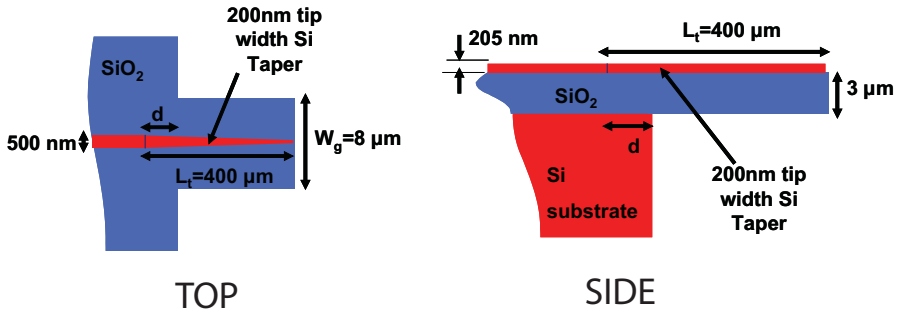


Figure 4.10: Top and side views of the simulated structure to analyze the influence on the coupling performance of the position of the inverted taper (d parameter) on the SiO_2 waveguide.

both polarizations. For this length value, 0.5dB coupling losses are achieved for TE polarization while 0.7dB coupling losses are achieved for TM polarization. It is important to remind that as the fiber-SiO_2 waveguide interface has not been considered in the 3D BPM simulation on Fig. 4.9 the total coupling losses of the structure will be the sum of the coupling losses in the fiber-SiO_2 waveguide interface, which were estimated in 4.3dB for both polarizations, and the 0.5dB and 0.7dB coupling losses estimated in Fig. 4.9 for a 400μm long inverted taper and TE and TM polarizations respectively. Therefore, the total coupling losses of the coupling structure for λ=1550 nm will be 4.8dB for TE polarization and 5dB for TM polarization.

The influence on the coupling performance when part of the 400μm long inverted taper is located on top of the SiO_2/Si layers instead on being completely located on top of the SiO_2 waveguide has also been investigated in order to reduce the length of the SiO_2 waveguide that is hanging on air and thus increasing the mechanical robustness of the structure. Fig. 4.10 shows a description of the simulated structure where the objective is to find the minimum value of the d parameter without degrading coupling losses. Coupling losses as a function of the d parameter for both TE and TM polarizations are shown in Fig. 4.11. It can be seen that coupling losses increase for high d values due to leakage losses into the silicon substrate. However, coupling losses are almost flat for d values smaller

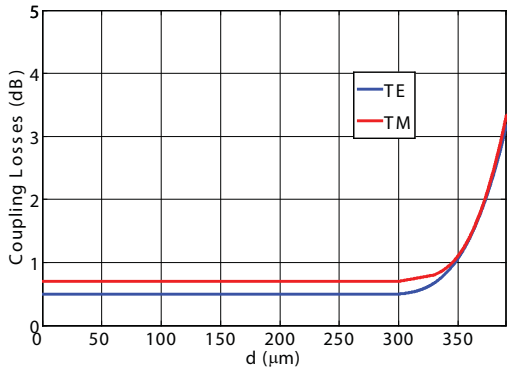


Figure 4.11: Coupling losses as a function of the d parameter depicted in Fig. 4.10 for both TE and TM polarizations.

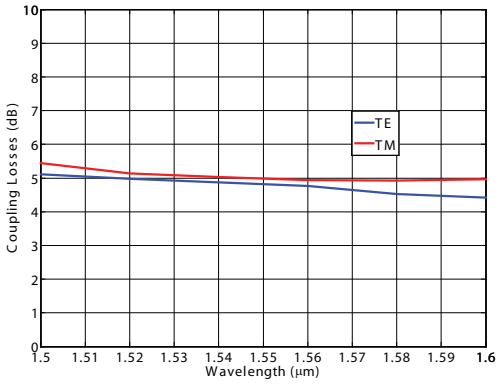


Figure 4.12: Spectral response of the coupling losses between a 500nm wide single-mode SOI waveguide and a 8μm MFD single-mode fiber by means of the proposed coupling structure.

than 325μm indicating that light quickly couples from the SiO_2 waveguide to the higher index of the inverted taper, as it can also be observed in Fig. 4.8. Therefore, it can be concluded that only the first 75μm of the inverted taper length must be necessary located on top of the SiO_2 waveguide.

Finally, the spectral response of the proposed coupling structure has also

been obtained taking into account the design parameters calculated previously for λ=1550 nm. Fig. 4.12 shows the spectral response of the coupling losses of a 500 nm wide single-mode SOI waveguide coupled to a 10μm MFD single-mode fiber by means of the proposed coupling structure. It can be seen an almost flat spectral response in the considered wavelengths range for both TE and TM polarizations. This flat spectral response is achieved because the coupling structure does not rely on any resonant effect due to an efficient fiber-to-SOI waveguide coupling. It is also important to point out that coupling losses could be reduced by using fibers with a lower MFD, as it can be seen in Fig. 4.5. However, alignment tolerances for V-groove integration are more critical, as previously discussed.

4.2.2 Realization

The structures were fabricated in close cooperation between IMEC[1] (Leuven-Belgium), the Photonics Research Group[2] at the Department of Information Technology ($INTEC$) of Ghent University (Belgium), the Research Center for Microperipheric at Technische Universitaet Berlin[3] (TUB) and also the joint laboratories of the System Integration and Interconnection Technologies Department of the TUB cooperation partner Fraunhofer IZM [4] (Fraunhofer IZM), in context of FP6-ePIXnet and FP7-HELIOS projects. As the CMOS production line facilities of IMEC are with commercial SOI wafers with 220nm/2μm Si/SiO_2 thicknesses, the SiO_2 waveguide thickness here is H=2μm. The design procedure for H=2 μm is similar to the previously detailed. Table 4.2 summarizes optimized design parameters and obtained coupling loss for this particular design

[1] IMEC performs world-leading research in nano-electronics and nano-technology. Its staff of more than 1,750 people includes over 550 industrial residents and guest researchers. Imec′s research is applied in better healthcare, smart electronics, sustainable energy, and safer transport. See http://www.imec.be

[2] http://photonics.intec.ugent.be/

[3] http://www.becap.tu-berlin.de/

[4] Together with the Research Center for Microperipheric Technologies at the TU Berlin the Fraunhofer IZM represents an efficient research, development and service potential, especially in the areas of Substrate Integration Technologies, Wafer Level Integration Technologies, Materials, Reliability and Sustainable Development and System Design. See http://www.izm.fraunhofer.de

L_t	W_t	**W**	**H**	**Coupling loss**
400 μm	200 nm	8 μm	2 μm	6 dB

Table 4.2: Optimum simulation parameters @ λ=1.55 μm when coupling to a SMF witn 10 μm MFD for both TE and TM polarizations.

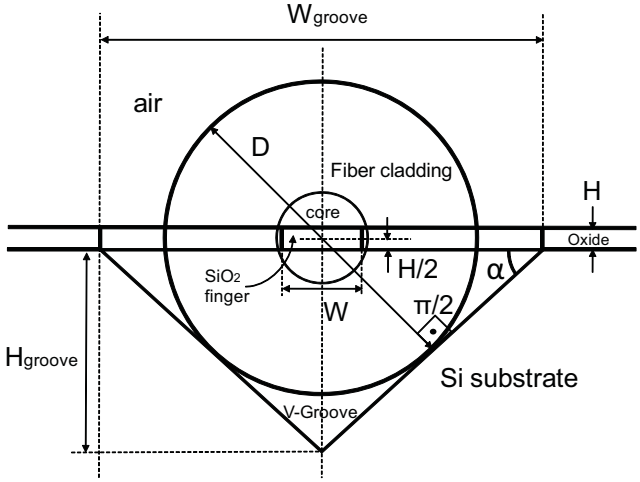


Figure 4.13: Schematic showing the cross section of the V-groove with the optical fiber placed in the optimum position for the coupling.

with H=2 μm when coupling to a SMF with 10 μm MFD for both TE and TM polarizations. It is obtained 6 dB theoretical coupling loss to 10 μm mode field diameter (MFD) standard optical fibers (SMF), and a polarization insensitive behaviour for optimized design. It is important to remark that just 75 μm of the SiO_2 waveguide are hanging on air, as it was found it was enough from simulation results in the previous section, thus increasing mechanical robustness of the structure.

4.2.2.1 V-Groove design

Fig. 4.13 depicts an schematic showing the cross section of the V-groove with the optical fiber placed in the optimum position for the coupling. The theoretical window dimension of the V-groove (W_{groove}) was also studied, in order to calculate

the optimum dimensions of the mask needed for etching the silicon substrate for creating the V-groove, as well as the silicon etching time needed for achieving the calculated V-groove height (H_{groove}). The optimum position of the optical fiber (cladding diameter D, radius $D/2$) in the V-groove corresponds to the position in which the SiO_2 finger of the inverted taper structure (thickness H and width W) is centered with the geometrical center of the optical fiber. That means that the center of the fiber is vertically shifted from the oxide-silicon interface a distance $H/2$, where H is the thickness of the SiO_2 layer of the SOI wafer (see Fig. 4.13). As a KOH (Potassium hydroxide) etching of monocrystalline silicon is going to be used in the fabrication, preferentially in the {100} plane, it produces a characteristic anisotropic V-etch, with sidewalls that form an angle of α=54.74° with the surface (see Fig. 4.13). Assuming we are going to use standard singlemode fibers with cladding diameter D=125 μm, and also assuming that $D \gg H$ (here H=1 μm) the optimum V-groove width is (see Fig. 4.13):

$$\frac{W_{groove}}{2} \approx \frac{D/2}{\sin\alpha} \rightarrow W_{groove} \approx 153\mu m \tag{4.2}$$

and also the optimum V-groove height is:

$$H_{groove} \approx \frac{D/2}{\cos\alpha} \rightarrow H_{groove} \approx 108\mu m \tag{4.3}$$

A very precise control of the KOH silicon etching is needed in order to obtain the desired V-groove dimensions. KOH is a nontoxic, economical and commonly used alkali metal hydroxide silicon etchant which requires simple etch setup and provides high silicon etch rate, high degree of anisotropy, moderate Si/SiO_2 etch rate ratio and low etched surface roughness [93]. Different experiments for controlling V-groove dimensions were initially developed in the Nanophotonics Technology Center of the Universidad Politécnica de Valencia, by varying different temperatures, concentrations and etching times. Table 4.3 summarizes the results obtained in these experiments. Fig. 4.14 depicts SEM images of fabricated prototypes of V-grooves showing actual V-groove dimensions after fabrication. It is important to notice that it is not easy to fabricate V-grooves on silicon for obtaining exactly the V-groove dimensions theoretically obtained for achieving the optimum coupling position of the optical fiber in the fiber-chip alignment,

Experiment	Etching (μm)	Time (min)	Conc. (% p/p)	Temp. ($^{\circ}C$)	Etch rate (μm/min)
1	82	98	25	75	0.837
2	31	150	25	65	0.207
3	90	420	25	65	0.214
4	88	150	25	72	0.587
5	90	90	35	80	1
6	101	90	35	80	1.122

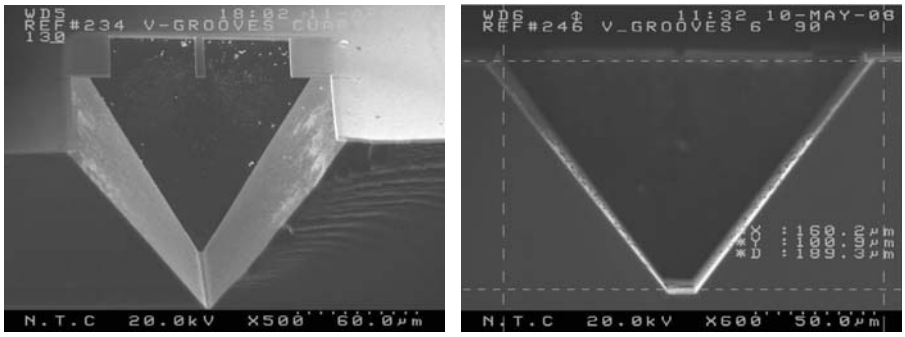
Table 4.3: KOH experiments and obtained silicon V-groove etching rates.

due to possible constrains regarding to the fiber diameter, and the tolerance in the fabrication of the fibers depicted in Table 4.1. For this reason, taking into account the fiber tolerances previously explained in Table 4.1, and for other internal issues of IZM experts, related to V-groove fabrication and fiber pigtailing, final fabrication of V-grooves for experimental testing were designed with different section dimensions for the worst case, as shown in Fig. 4.15. Basically, a 183μm wide V-groove is finally chosen, for having space to put the glue. For this new V-groove width, the optimal height is found to be 74.6μm (see Fig. 4.15). A specific hole is also needed for fixing the fiber to the substrate underneath the V-groove, with the dimensions also specified in Fig. 4.15. A safe distance of 500μm between the taper edge and the hole is also considered, and 5mm long V-groove space is also considered for avoiding mechanical problems once the fiber is glued to the sample.

4.2.2.2 Fabrication and experimental results

For the fabrication of the V-groove samples we generated the layout depicted in Fig. 4.16. It consists of I/O inverted taper coupling structures integrated with its corresponding V-groove, and interconnected to each other by means of 2000μm long 500nm wide SOI waveguides. In Fig. 4.16 it is also shown the three different layers integrated in the layout, corresponding to the silicon, silica and V-groove substrate etching steps during the fabrication process.

The test circuits with inverted tapers were fabricated in IMEC using SOI



(a) (b)

Figure 4.14: (a) SEM image of fabricated V-groove examples for optimizing the V-groove dimensions (b) detail of actual V-groove dimensions after fabrication.

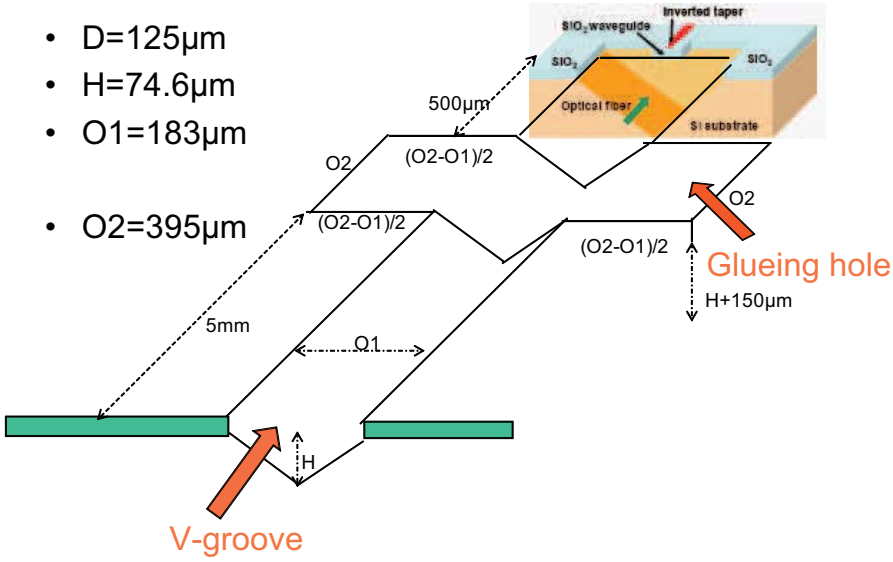


Figure 4.15: Schematic showing the proposed V-groove dimensions for the fabrication.

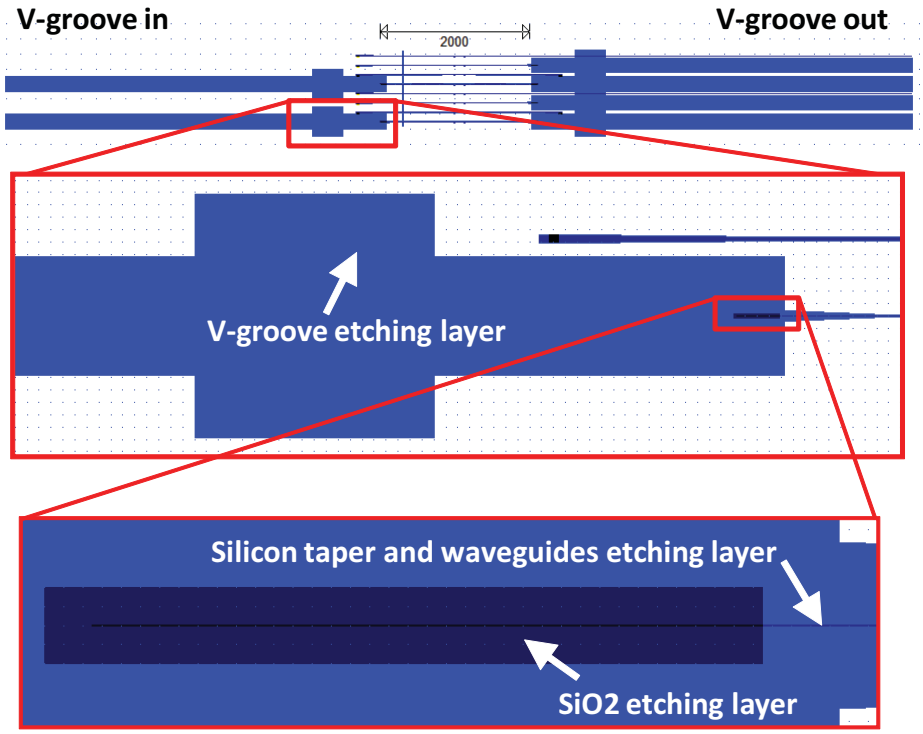


Figure 4.16: Layout generated for the fabrication of the V-groove samples, and detail on the different masks for the different etching fabrication steps.

wafers with a 220 nm silicon layer and 2 μm buried oxide (BOX). First, passive silicon structures containing the waveguides and inverted tapers were defined in a 193nm deep UV (DUV) lithography step. Second, waveguides and tapers were etched 220 nm, and then covered with 750 nm of SiO_2 for performing the lithography step for the definition of the V-grooves. A new hard-mask based process was then developed to fully open the 2.75 μm of SiO_2 as etch pattern for definition of the V-grooves. Fig. 4.17 depicts a scanning electron microscope (SEM) image of window in the oxide for definition of the V-grooves.

The fabrication of the V-grooves was performed in Fraunhofer IZM. The fabrication of small 3D silicon structures such as V-grooves requires very precise micromachining technologies like anisotropic etching of monocrystalline silicon.

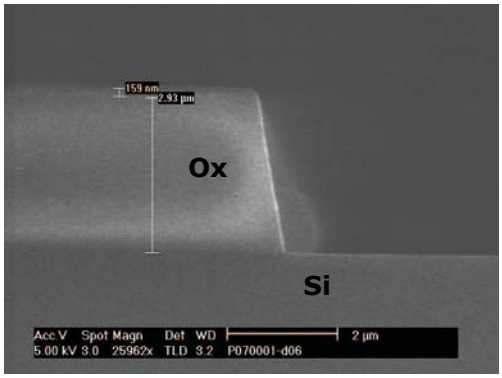
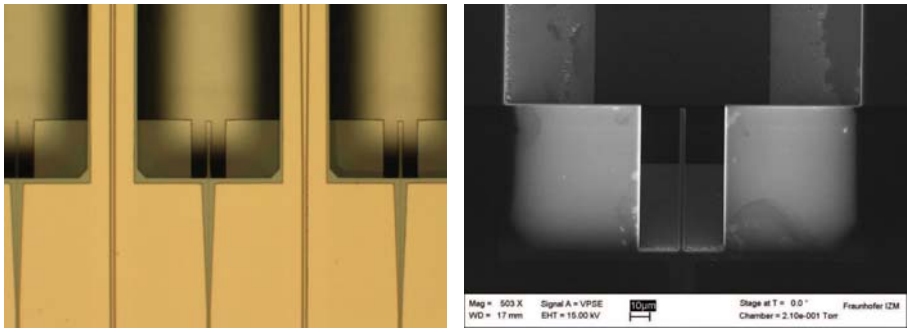


Figure 4.17: Edge of window in the oxide for definition of the V-grooves.



(a) (b)

Figure 4.18: (a) Optical microscope and (b) SEM images of fabricated V-groove samples.

Aqueous KOH is widely used in this technique. The control of the involved physical and electrochemical processes are challenging. For device fabrication, these issues are of great economical importance. It should be ensured that the etching behaviour is stable and predictable. In particular the anisotropy ratio (etch depth divided by the lateral underetching of the mask) should be reproducible with high accuracy and the etched surfaces should be smooth. To understand mechanism involved in anisotropic KOH etching process a model was proposed to explain and to calculate the microscopic 3D shapes [94]. Based on theoretical

and experimental investigations [95] a controllable process for three dimensional structuring by means of anisotropic KOH etching was developed. Fig. 4.18(a) and Fig. 4.18(b) depict optical and scanning electron microscope (SEM) images of fabricated V-grooves, respectively. As known from former detailed experimental investigations [94, 95] silicon dioxide etch masks are not the best etch mask material due to a not negligible etch rate as can be seen in Fig. 4.18(a) and Fig. 4.18(b). Such underetching caused by the etch mask material and some possible misalignments of the etch mask with respect to the {100} silicon crystal direction cause uncertainties of V-groove width. In order to avoid geometrically constrains regarding to the fiber diameter we only controlled the etch depth by etching time and used and oversized V-groove, as previously depicted in Fig. 4.15.

Fig. 4.19 depicts a block diagram graph of the measurement setup developed at Fraunhofer IZM for performing the experimental measurements of fabricated samples. The instrumentation used in the setup for the measurements was:

- 2 HEXAPOD F-206 6-axis control (very precise control for the input/output fibers in the Vgroove)
- 1 MANUAL 3-axis holder (for controlling the SOI chip position)
- 1 LASER HP 8168A (tunable laser, [1530,1580] nm)
- 1 POWER METER HP 8153A (detector @ 1550nm, 100 nm bandwidth)
- 2 digital cameras, zoom 1000x (top and side views)
- 2 commercial SMF fibers with 10 μm MFD
- 1 polarization controller (input side)

A photo of the measurement setup is illustrated in Fig. 4.20(a), as well as Fig. 4.20(b) depicts a detailed photo of the input/output fibers and the SOI sample while measuring the samples.

Fig. 4.21 depicts experimental measurements for transmission spectrum and TE polarization of fabricated samples. Top and side view images of optical fiber placed in the V-groove while measuring the samples are also shown in Figs.

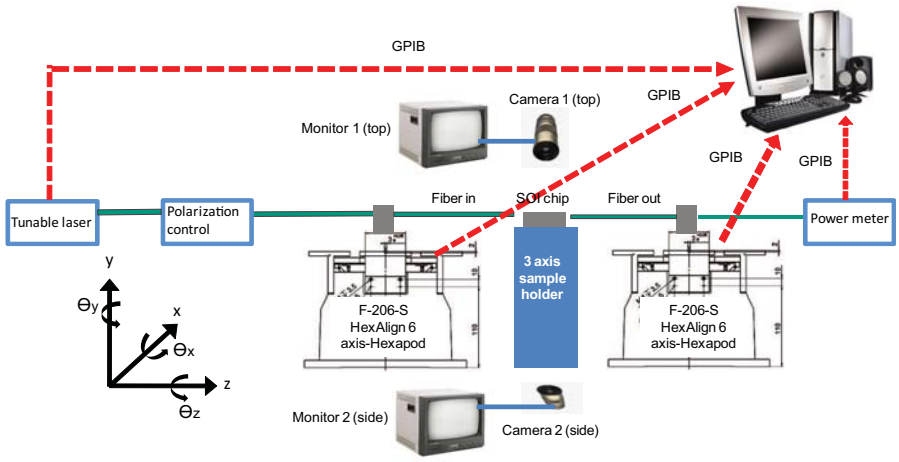
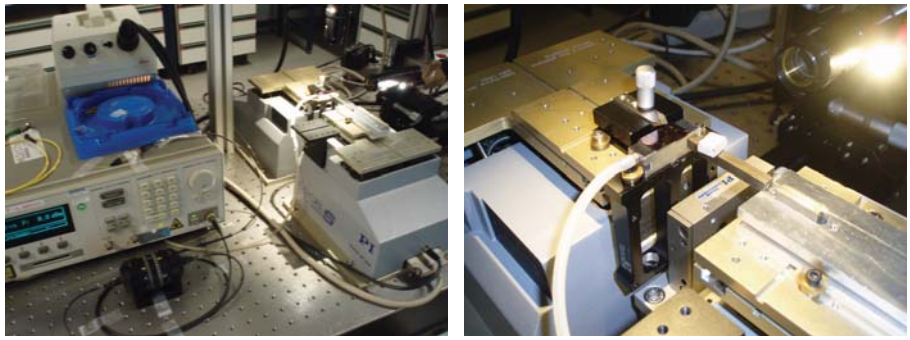


Figure 4.19: Block diagram of the measurement setup for the V-groove samples.



(a) (b)

Figure 4.20: (a) Photograph of the measurement setup; (b) detailed photograph of the input/output fibers and the SOI sample while measuring the samples.

4.22(a) and 4.22(b), respectively. We obtained 7.5 dB coupling loss at λ=1.55 μm. Obtained experimental results slightly differ from those previously obtained theoretically mainly due to small differences in dimensions of the structures. Fig. 4.23 depicts two different SEM images showing actual section dimensions of SiO_2 waveguide after fabrication. We measured a waveguide width of 6.7 μm as well as a waveguide thickness of 1.689 μm, whilst design values were 8 μm and 2

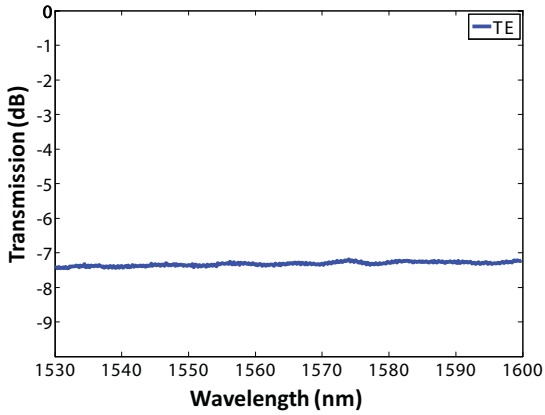
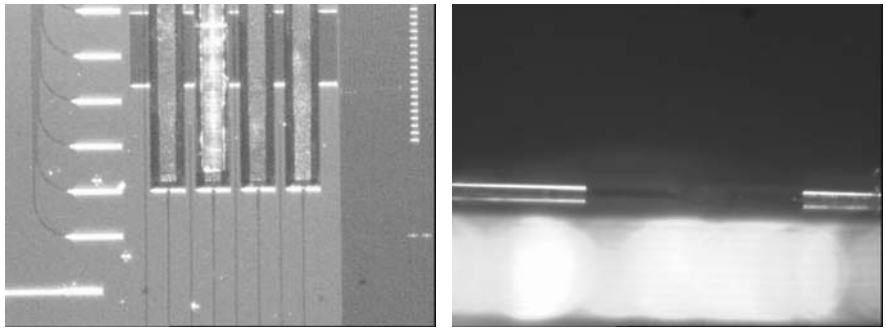


Figure 4.21: Transmission spectrum measurements of the fabricated samples.

μm, respectively. By changing polarization at the input of the structure, we also obtained a small variation of $\pm$0.5 dB on results depicted in Fig. 4.21. So, we also can corroborate that our coupling structure is polarization insensitive, as expected from simulation results. Moreover, obtained spectral response is almost flat in a wavelength bandwidth higher than 70nm, as shown in Fig. 4.21. It is important to notice that lower coupling loss (1-2dB) may be achieved by adding a 6-7 μm uppercladding layer on top of the SOI wafer, better mode matching to optical fiber mode, as we will discuss in the conclusion chapter.

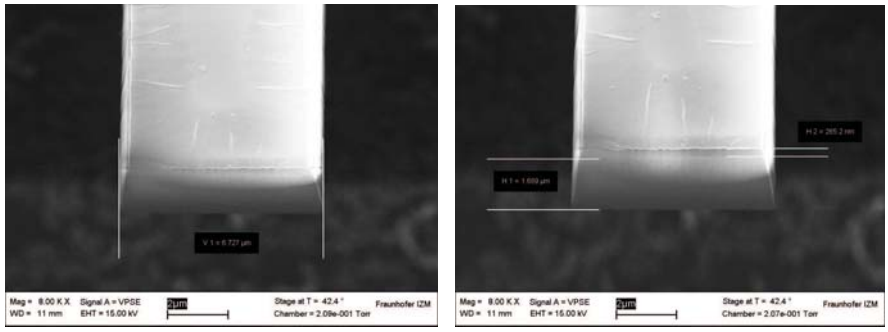
As a proof-of-concept, we also performed the fiber pigtailing to the V-groove samples. The glueing process was the same that the previously explained for the multiport grating samples. Fig. 4.24 depicts a photo of the V-groove sample after fiber pigtailing.

However, after fiber pigtailing we could not perform any experimental measurement, as, due to V-groove dimension after fabrication, the V-groove hole was too deep, and the fiber was misaligned from the coupling struture after glueing. This can also be visualized in Fig. 4.18, where it can be seen that the obtained fabricated structure is kind of $\sqcup$-like shape, instead of the desired $\vee$ shape. This is mainly caused because of the underetching due to the use of a silicon dioxide mask for the etching, and also due to the use of an oversized V-groove mask for fiber diameter geometrical constrains and so on, as previously discussed.



(a) (b)

Figure 4.22: (a) Top and (b) side view images of optical fiber placed in the V-groove while measuring the samples.



(a) (b)

Figure 4.23: SEM images showing detailed view of actual section dimensions of the SiO_2 waveguide.

4.3 Inverted taper structures for horizontal slot waveguides

Fig. 4.25 shows a schematic of the proposed structure. The coupling structure is based on a horizontal (sandwiched) slot waveguide on top of a silica cladding layer, which is tapered down to create the inverted taper for coupling to the fiber. This geometry allows using commercial SOI wafers. A fiber adapted waveguide

Figure 4.24: Photo of the V-groove sample after pigtailing.

on top of the inverted taper is used to efficiently guide light from the taper to the fiber (see Fig. 4.25). Fig. 4.25 also shows the layer stack used for the slot waveguide configuration. The low refractive index (n_S) slot layer is sandwiched between two silicon high refractive index (n_H) layers. In the sandwiched slot waveguide case, the electric field discontinuity at the interface between the high index contrast silicon waveguides occurs in the vertical direction. Therefore, the highest field confinement is achieved for TM polarization (y-axis direction in Fig. 4.25). The silicon layers thickness is h, the slot layer thickness is w_s, and the slot waveguide width is w, as shown in Fig. 4.25. Silicon′s refractive index (n_H=3.48 @ λ=1.55 μm) is also indicated in Fig. 4.25. Furthermore, the slot is made of $Si-nc$ embedded in silica (SiO_2) and has a refractive index (n_H =1.6 @ λ=1.55 μm). Finally, the fiber adapted waveguide on top of the inverted taper uses a polymer with a refractive index of n_p=1.6, the same refractive index as the $Si-nc/SiO_2$ slot layer. Previously to the coupler design, the sandwiched slot waveguide configuration was analyzed to determine the optimum parameters to achieve maximum field confinement. The optimum waveguide parameters are those that give minimum effective area in the slot region [45]. All analysis was performed at λ= 1550 nm and for TM polarization. Optimum performance was obtained for a slot thicknesses of w_s=50 nm, a silicon layer thickness of h=200 nm and a slot waveguide width of w=350 nm [45].

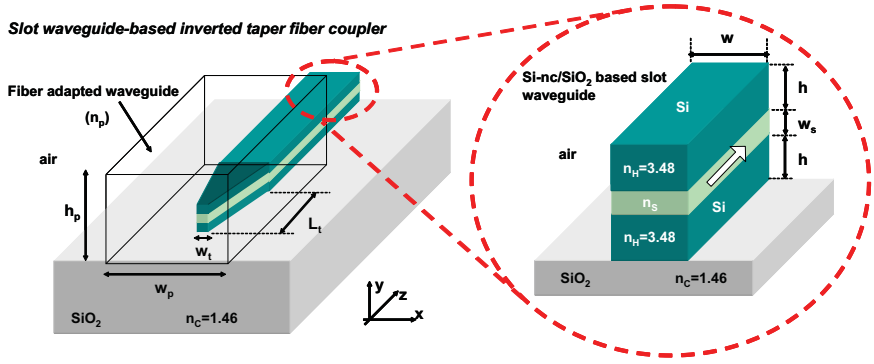


Figure 4.25: Schematic of the proposed structure for efficient light coupling to sandwiched slot waveguides. A detailed view of the considered layer stack of the sandwiched slot waveguide is also shown.

4.3.1 Design

The main design parameters of the proposed inverted taper coupling structure are the inverted taper length (L_t), the inverted taper tip width (w_t), and the dimensions of the fiber adapted waveguide on top of the coupler (w_p, h_p), as depicted in Fig. 4.25. Optimization is performed to obtain maximum coupling efficiency. To simplify the design, the dimensions of the fiber adapted waveguide have been chosen to be w_p=h_p=3 μm. The mode mismatch between the optical fiber and the fiber adapated waveguide fundamental modes has been evaluated by means of the overlap integral:

$$\eta = \frac{\left| \iint\limits_S \vec{E}(x,y) \times \vec{H}^*_{fib}(x,y) dxdy \right|^2}{\mathrm{Re}\left\{ \iint\limits_S \vec{E}(x,y) \times \vec{H}^*(x,y) dxdy \iint\limits_S \vec{E}_{fib}(x,y) \times \vec{H}^*_{fib} dxdy \right\}} \tag{4.4}$$

where $\{E, H\}$ are the TM polarization electromagnetic fields of the fiber adapted waveguide fundamental mode, and $\{E_{fib}, H_{fib}\}$ are the electromagnetic fields of the fiber fundamental mode for TM polarization. The fundamental mode of the fiber adapted waveguide was obtained by using a three dimensional (3D) mode

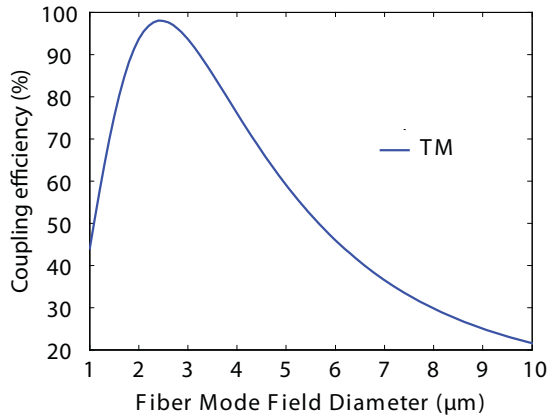


Figure 4.26: Coupling efficiency calculations using the overlap integral between fundamental mode profiles of both optical fiber and fiber-adapted waveguide as a function of the fiber Mode Field Diameter (MFD). Cross-section dimensions of the fiber adapted waveguide are w_p=h_p=3 μm.

solver based on the BPM method. The fundamental mode of the optical fiber was obtained by means of a Gaussian beam function.

Fig. 4.26 shows the coupling efficiency calculated with Eq. 4.4. It can be seen that for the considered fiber adapted waveguide dimensions (w_p=h_p=3 μm), 98% coupling efficiency may be achieved with a optical fiber with a mode field diameter (MFD) of 2.5 μm. So, the design is aimed to be used with lensed fibers with MFD=2.5 μm, which are very common for testing silicon devices, and are standard commercially available. It is important to remark that the design can also be optimized for coupling to standard single-mode optical fibers with MFD=10 μm by changing the fiber adapted waveguide cross-section dimensions.

4.3.1.1 Inverted taper tip width optimization

The next optimization parameter is the inverted taper tip width (w_t). The optimum inverted taper tip width, which minimizes the mode mismatch for TM polarization, has been designed by means of the overlap integral between the fundamental mode of the fiber adapted waveguide and the inverted taper tip

waveguide, assuming an infinitely long waveguide having the same cross-section as the taper tip. The design process is depicted in Fig. 4.27 for infinitely waveguides along the z-axis, according to axis definition in Fig. 4.27. However, the effective index of the guided mode at the taper tip interface was also first calculated as a function of the taper tip with and for different slot thicknesses. The obtained results are shown in Fig. 4.28(a). The effective index increases with the taper tip width for the three considered slot thicknesses owing to the higher confinement in the slot waveguide. However, the effective index remains almost equal to the effective index of the fiber adapted waveguide (w_t=0 case), when taper tip is less than 40 nm wide, so that the lower mode mismatching is achieved at the taper tip interface. As a result, and taking into account that nonlinear effects in the slot region are higher for lower slot thicknesses, a slot thickness of ws=50nm has been chosen. Furthermore, an inverted taper tip width of w_t=40 nm seems also to be optimum as the effective index does not significantly change compared to the refractive index of the fiber adapted waveguide so the highest mode matching will be achieved at the taper tip interface. Mode mismatching at the taper tip interface has been calculated by means of the overlap integral. Fig. 4.28(a) shows the power coupling efficiency between the fundamental modes of the structures depicted in Fig. 4.27. For TM polarization, it is obtained that coupling efficiency gets lower than 95 % if the inverted taper is wider than 40 nm. So, in agreement with results shown in Fig. 4.28(a), it can be concluded that the optimum taper tip width will be w_t=40 nm.

4.3.1.2 Inverted taper length optimization

The optimum inverted taper length has been designed by means of 3D BPM simulations using the optimum taper tip width (w_t=40nm), which was previously obtained, and the polymer fiber adapted waveguide dimensions (w_p=h_p=3 μm). Fig. 4.29(a) shows the electric field distribution in a 150 μm long inverted taper obtained by means of a 3D BPM simulation. To obtain coupling efficiency, the structure is excited at z=0 by the fiber adapted waveguide fundamental mode and a 1550 nm wavelength and for TM polarization, according to axis definition in Fig. 4.25. The power coupled at the 350 nm wide slot waveguide is then measured

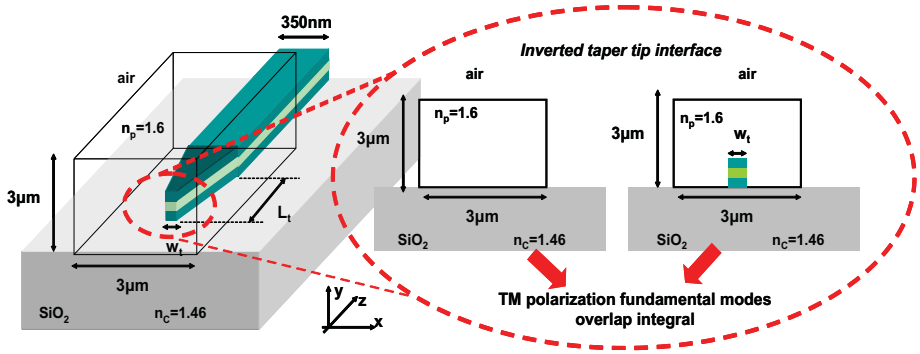
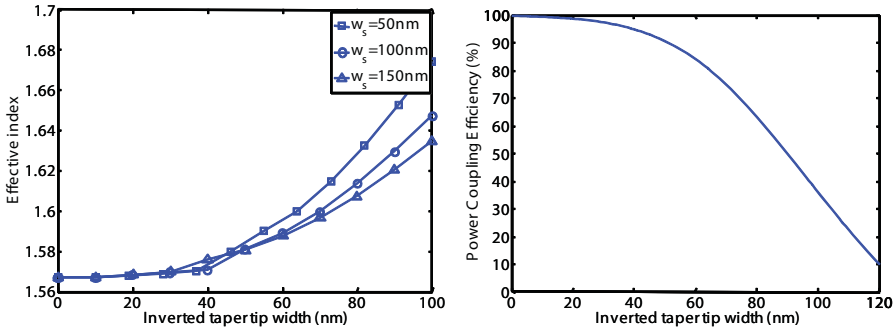


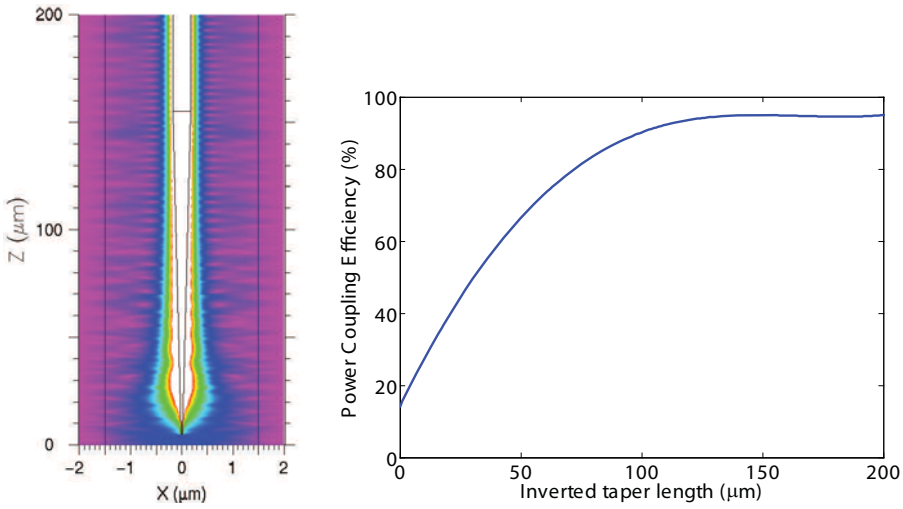
Figure 4.27: Schematic of the design process to find the optimum inverted taper tip.



(a) (b)

Figure 4.28: (a) Effective index as a function of the taper tip width (w_t) for different slot thicknesses (w_s) and (b) coupling efficiency as a function of the inverted taper tip width, for a slot thickness of w_s=50 nm.

to evaluate coupling efficiency. Fig. 4.29(a) shows the coupling efficiency as a function of the inverted taper length. It can be observed that coupling efficiency increases as the inverted taper gets longer due to the lower mode mismatching. Furthermore, if the inverted taper is longer that 150 μm, coupling efficiency gets constant with the taper length, and 95 % coupling efficiency is achieved. As maximum coupling efficiency is achieved for a 150 μm longer inverted taper, a taper length of L_t=150 μm has been chosen. The obtained coupling efficiency



(a) (b)

Figure 4.29: (a) Field distribution in a 150 μm long sandwiched slot waveguide based inverted taper obtained by means of 3D-BPM simulations. (b) Coupling efficiency as a function of the inverted taper length.

is in a very good agreement with the results shown in Fig. 4.28 which were calculated using the overlap integral. It is also important to point out that the structure analyzed in the simulations is excited by the fiber adapted waveguide fundamental mode, so the coupling efficiency results shown in Fig. 4.29(b) for a taper length of L_t=150 μm is only due to the mode mismatching at the taper tip interface. Therefore, as mode mismatching at the fiber interface is not considered in the simulation results depicted in Fig. 4.29(b), the total coupling efficiency will be the product of the coupling efficiency obtained in Fig. 4.29(b) and the coupling efficiency previously obtained in Fig. 4.26 at the fiber interface. The final result is a 93 % total coupling efficiency for TM polarization and λ=1550 nm.

SiO_2 waveguide cross-section	Taper tip width	Taper length	Coupling loss
8μm × 3μm	200 nm	400 μm	4.8dB (TE) 5dB (TM)

Table 4.4: Summary of obtained optimal design parameters of the inverted taper structure, and theoretically obtained coupling efficiency @ λ=1.55 μm, for standard optical fibers with 10μm MFD.

4.4 Summary and conclusions

In this chapter we have studied in detail the coupling to fiber via inverted taper in SOI waveguides, and provided theory, simulation, fabrication, as well as experimental results. An explanation on the coupling to fiber mechanism via inverted taper in SOI waveguides was first addressed. The justification of the design of our proposed inverted taper based coupling structure was addressed, and remarked the most important target features, such as CMOS compatible, insensitive to polarization, capability of integration with V-groove structures for enhancing the fiber-chip alignment, and the utlization of the SiO_2 buffer layer of the SOI wafer for acting as the fiber-adapted waveguide of the inverted taper. Starting with the design optimization @ λ=1.55 μm, we focused on SOI wafers with 205nm/3μm Si/SiO_2 layer thicknesses. As the starting point for the design, the optimal SiO_2 waveguide dimensions were first obtained, by evalutaing the mode mismatch between the SiO_2 waveguide and the optical fiber via the overlap integral of the fundamental modes in both structures. The choice of standard fibers with 10μm MFD was justified for the particular case of the integration of our coupling technique with V-groove structures. After obtaining optimal SiO_2 waveguide dimensions, the optimal taper tip width and the taper length were then designed. For obtaining the optimal inverted taper tip width, we evaluated the overlap integral in the inverted taper tip interface. For obtaining the optimal inverted taper length, 3D-BPM simulations were performed. Table 4.4 summarizes the obtained optimal design parameters, and the obtained theoretical coupling loss of the proposed design @ λ=1.55 μm. Basically, we obtained

Taper length	Taper tip width	SiO_2 thickness	Coupling loss
400 μm	200 nm	2μm	6 dB

Table 4.5: Summary of optimization of the inverted taper @ λ=1.55 μm for SOI wafers with 2μm SiO_2 thickness, when coupling to a SMF with 10 μm MFD for both TE and TM polarizations.

that a polarization insensitive behaviour of our design is observed, for a taper tip width of 200 nm, and a taper length of 400 μm, and using a SiO_2 fiber-adapted waveguide with cross-section dimension 8μm $\times$ 3μm. Minimum coupling loss of 4.8dB and 5dB were obtained in the simulations for TE and TM polarizations, respectively, and for λ=1.55 μm. As a 400μm long taper may cause some instability of the structure and possible mechanical problems, we influenced on having just a bit of the taper coming out from the substrate. We obtained that just the first 75μm of the 400μm long taper must be necessary to be located on top of the SiO_2 waveguide. The spectrum of the structures was then computed, and obtained that the spectral response is almost flat in a wavelength range >100 nm. The experimental realization of the structure was then carried out. As the structure was going to be fabricated in IMEC, and they use SOI wafers with 2μm SiO_2 buffer layer thickness, we re-design the structure for this buffer layer, and the obtained results are summarized in Table 4.5. A consideration on the V-groove dimensions for optimizing the coupling to our structure were then discussed, and obtained the optimal V-groove parameters for the coupling, considering the fabrication was going to be performed with silicon KOH etching. A modification on the V-groove dimensions was then discussed, taking into account some issues related to the V-groove fabrication and fiber pitailing. Then, the fabrication of the strucrue was carried out using deep-UV lithography and chemical etching for both SiO_2 and silicon etching steps needed. A specific experimental setup for the measurements was performed. In the setup we used a 6-axis automatically controlable holder for placing the fiber in the V-groove. A SEM measurement of fabricated sample was also performed in order to know actual strucrue dimensions. The obtained structure dimensions as well as experimental results after characterisation of the samples are summarized in Table 4.6. We experimentally demonstrated

Actual SiO_2 width	Actual SiO_2 thickness	Coupling loss	Bandwidth
6.7 μm	1.689 μm	7.5dB	>70 nm

Table 4.6: Summary of measured actual SiO_2 waveguide dimensions and obtained experimental results of the inverted taper structure @ λ=1.55 μm.

7.5dB coupling loss for actual measured dimensions of the structure after fabrication. A polarization insensitive of the struture was also observed, as, by changing the polarization at the input, just a ±0.5dB deviation of the transmission measurements were obtained. Although the coupling structure was demonstrated, the aim of the integration of the coupling structure with V-groove structures for enhancing the fiber-to-chip alignment was not fully successful. The proposed V-groove integration was initially intented to be a proof-of-concept of the first step towards passive alignment in silicon chips. Passive fiber-to-chip alignment in silicon waveguides is an important fact, as the alignment of such waveguides to the optical fiber is difficult due to relatively low alignment tolerances, which is of high importance when fiber pigtailing to the silicon chips. A V-groove structure is a very good candidate for such alignment in horizontal inverted taper-based coupling. The possibility of the fabrication of V-groove structures using KOH etching makes the choice of V-groove structures more attractive, as the etching process is relatively fast and easy, and also compatible with CMOS standard fabrication processes. The problem is that crystalline orientation imposes an etch angle, and the fabrication of these kind of structures is not easy, as we have seen. Taking also into account fiber tolerances, and so fiber pigtailing issues and the underetching caused by the silicon dioxide etching material, the used of an oversized V-groove mask is impossed. The final conclusion is that, obviously, the active alignment between the fiber and the coupling structure can be performed successfully (as we have demonstrated the coupling), but the supposed V-groove role of enhancing the alignment is unfortunately wasted. Much effort may be put on the fabrication of the V-grooves for improving the results regarding the V-groove alignment. However, our experience is that, the desired passive alignment when using these kind of structures is still a long way off. Other strategies for creating more accurate V-grooves on silicon substrate can also be studied, such as

Polymer waveguide	Taper length	Taper tip width	Efficiency
3 μm × 3 μm	150 μm	40 nm	93%

Table 4.7: Summary of simulation results of the inverted taper coupler for $Sinc/SiO_2$ based sandwiched slot waveguides @ λ=1.55 μm and TM polarization.

the possibility to practice the V-groove directly in the substrate in a mechanical way by using an accurate special blade.

Finally, we have reported simulation results of a highly efficient fiber coupler for light coupling between optical fiber and $Sinc/SiO_2$ based sandwiched slot waveguides. Parameters were optimized to achieve maximum coupling efficiency for TM polarization and λ=1550 nm by means of 3D-BPM simulations and overlap integral calculations, and are summarized in Table 4.7. According to simulation results, maximum 93% coupling efficiency was achieved for an inverted taper of 150 μm length and 40 nm tip width, when coupling from a lensed fiber with MFD = 2.5 μm, and taking into account a polymer fiber adapted waveguide (n=1.6) of 3 μm × 3 μm cross-section dimensions. The main problem to bring this structure to practise is that the inverted taper tip is too narrow (40 nm). Of course this value is beyond depp-UV lithography limit (usually 100 nm resolution), and of course the fabrication of the structure is not CMOS compatible. Other kind of lithography can be used for the fabrication of the structure can be used, such as e-beam lithography, with higher resolution (10-20 nm best case). However, achieving a 40 nm tip width inverted taper is even difficult with this technology, and may require development of special processes and tests, as the achievable resolution depends on the resist used in the lithography fabrication process.

Chapter 5

Generic packaging solutions for SOI chips

This chapter encloses some examples of packaging solutions for the SOI coupling techniques previously studied in this thesis. First, a brief review on the state-of-the-art of silicon photonics packaging applied to our coupling techniques is introduced. Second, a specific packaging consideration for SOI devices with grating couplers for coupling to the optical fiber is studied in detail, and a first demonstrator prototype based on this packaging technique is experimentally demonstrated.

5.1 Silicon Photonics Packaging

As packaging is necessary to achieve a reliable device on basis of the silicon photonic chips, the fiber-to-chip challenge has to be overcome by a packaging solution providing standard optical interfaces, but maintaining the advantage of size and coupling efficiency. Alignment, reliability, standardization, and mass production suitability are the most important issues. Due to technical problems, i.e. an overriding mode mismatch of nanowires and standard single-mode fibers, as well as alignment tolerances in the coupling, fiber pigtailing and the packaging of nanowaveguide circuits are key technologies in the realization of nanophotonic applications. Hence, the development of smart and cost effective packaging solutions for silicon photonics is integrally connected with the competent design of efficient coupling structures, requiring innovative coupling structures for low

coupling loss and large alignment tolerances, as well as passive alignment to make easier the alignment of the SOI device with the optical fiber, thus offering the possibility of low cost device assembly.

5.1.1 Fiber Pigtailing

Fiber pigtailing ought to implement a reliable joint between a photonic device and a single fiber or a set/array of single-mode fibers. Pigtailing is a fundamental prerequisite for testing and application of photonic devices, and is also the first step of packaged devices. Keeping in mind applications in telecom, a fiber-device-joint should introduce as little as possible additional loss, low back-reflection, and low polarization dependence. Following the study of fiber couplers in previous chapters, we may distinguish between two kinds of pigtailing presently used in silicon photonics:

1. Pigtails using lensed/tapered/high-NA fibers, typical spot diameter $\sim$3 μm, horizontal coupling (example : Infinera).

2. Pigtails using standard butt-fibers, spot diameter $\sim$10 μm, horizontal and vertical coupling (examples: Kotura, Luxtera).

Pigtailing with a 3 μm spot diameter is a common technique for InP-based devices due to waveguide mode size in that technology. As an example, Fig. 5.1 depicts a photo of the InP-based 100 Gb/s DWDMLS-PIC transmitter module of Infinera, pigtailed with single lensed fibers [96]. Similar approaches can be adapted to silicon photonic devices. Coupling with 3 μm spot diameter has to cope with alignment tolerances below 0.5 μm to achieve a penalty $<$ 1 dB. Such requirements necessitate active alignment and low shrinkage fixation of the fiber. Solutions are based on metal-can housings and soldering techniques (epoxy shrinkage during curing is difficult to control). This may be a problem for multiple fiber pigtailing in silicon photonics i. e. by using fiber arrays. Note that a 3 μm coupling is incompatible with the silicon bench V-groove alignment techniques used for fabrication of fiber arrays, since the position accuracy of fiber cores in a V-groove base is insufficient (see Fig. 5.2). Virtually all applications of 3 μm spot diameter are therefore single fiber solutions (i.e. 1-side in, 1-side out),

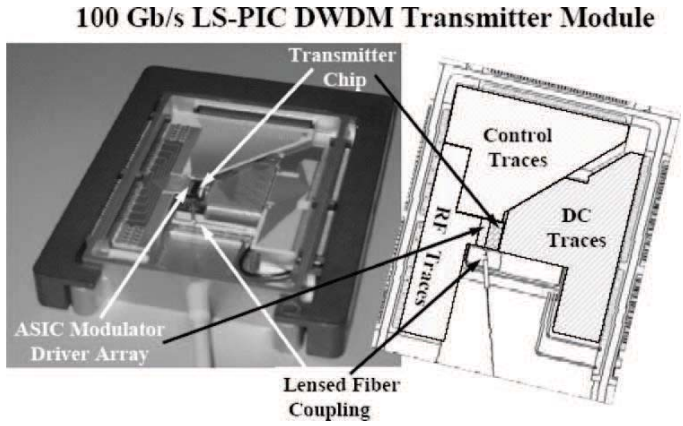


Figure 5.1: Photograph and schematic of InP-based the 100 Gb/s DWDMLS-PIC transmitter module of Infinera with the hermetic lid removed [96].

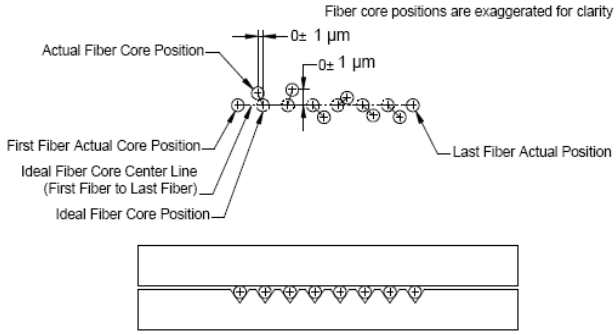


Figure 5.2: Position accuracy of a linear fiber-array based on a silicon V-groove bottom (OZOptics). Misalignment stems from nonuniform fiber diameters, fiber core excentricity, and etch depth variations of the v-groove array.

with very few fiber-array demonstrators so far. The key to ease pigtailing lies in the mode size coming from the chip. The desired mode size with affordable tolerances ($\pm$ 1 μm) matches SMF (about 10 μm spot diameter). Notably, also on InP some groups have demonstrated mode size tapering up to standard single mode fiber (SMF) dimensions [97] to allow for integration with planar-lightwave

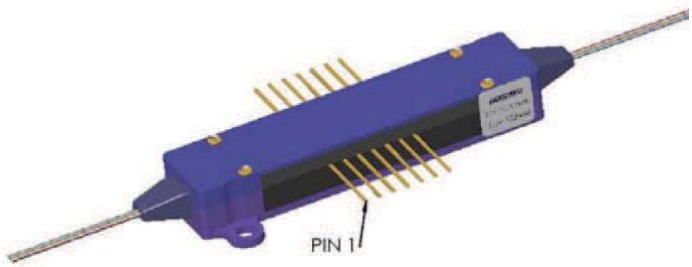
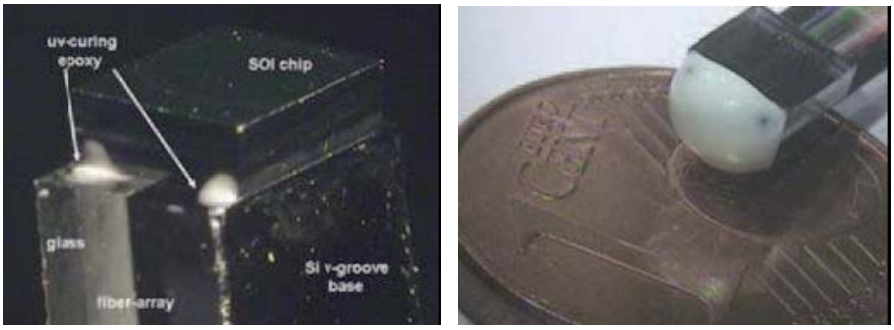


Figure 5.3: UltraVOA module of Kotura. The module uses standard telecom packaging techniques (butterfly housing, SMF coupling). Pigtails with 4 or 8 fibers are available.

technologies and to reduce packaging costs. Current silicon photonics applications are mostly based on coupling to SMF mode size, either via lateral taper structures (Kotura) or via grating couplers (Luxtera). To illustrate the present, telecom oriented approach of Kotura we depicted their UltraVOA module[1] in Fig. 5.3. The device comes in 4 or 8 channel configuration, and is based on a classic butterfly housing. Pigtailing of the fiber arrays is based on an adiabatic taper [98]. The voltage operated attenuator is edge-coupled using SMF (butt). Kotura′s SOI waveguides have about 3 μm spot diameter. Therefore, Kotura′s packaging approach is not compatible with advanced silicon nanowire technologies (sub-micron sized spot diameter). Recent work has shown that vertical coupling via grating couplers can be a viable technique to multifiber interfacing of silicon nanophotonic circuits (i. e. using fiber arrays). However, gratings also evoke the need for entirely new smart packaging solutions due to the effect of out-of-plane coupling. New approaches are required to handle issues of mechanical stability, and reliability while preserving at least partially the compactness of the underlying devices. At the same time, these approaches should be derived from micro-electronic packaging to keep costs as low as possible.

[1] UltraVOA application note, Kotura Corp.
http://www.kotura.com/products/uvoa.html



(a) (b)

Figure 5.4: (a) Fiber-array pigtailing solution without glob top. The SOI chip is mounted face down on the fiber array. (b) Encapsulated SOI chip on fiber array (8 fibers) in comparison to 1 Euro Cent coin [99].

5.2 Packaging of multiport silicon PICs with vertical coupling to fiber

Fig. 5.4 depicts the packaging solution developed in the frame of the ePIXpack[1] platform, within the ePIXnet network of excellence, which offers a compact solution for an 8-port fiber array interface [99]. The package uses a commercial fiber array connector as a base to mount the Silicon photonic chip. Such arrays provide up to 32 i/o-ports without the need for a dedicated fiber array design. Glass lid and V-groove bottom of the fiber array are polished to provide the correct angle for coupling. The chip is sealed by an appropriate glob top encapsulation. A very compact package with multiple optical ports can be realized in this way. Due to the large mode size of grating coupler devices high uniformity (±1 dB) with low penalty (1 dB) can be achieved for fiber array pigtails. Out of plane pigtails

[1]The Photonics Packaging Platform ePIXpack provides technical advice and a broad packaging technology base to parties inside and outside of ePIXnet who seek packaging of their photonic devices. They can offer solutions ranging from fiber pigtailing to advanced optoelectronic RF packages. The platform focuses on packaging at the pre-prototype stage to assist in particular the academic community, but also serves prototype packaging demands up to small batch size. See http://http://www.epixpack.eu/

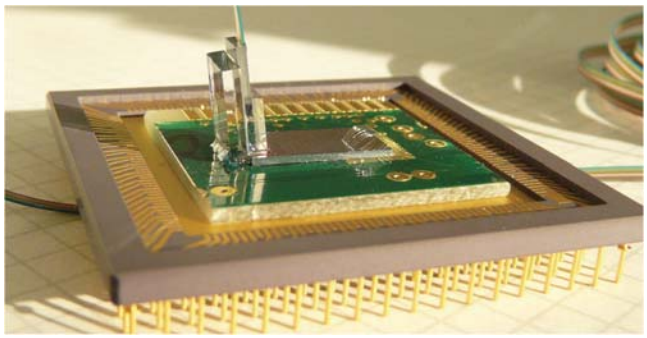


Figure 5.5: High profile packaging solution for silicon PICs with vertical coupling fiber array optical interconnection [58].

have problems for mechanical stability, reliability and compactness of such modules. These problems can partly be alleviated if the V-groove bottom itself acts as support (as shown Fig. 5.4). However, this solution is only valid for passive PICs.

A generic package approach for prototyping should therefore handle both optical and electrical pin-out. Following this approach, a generic approach also incorporating electrical ports was then developed, also in the frame of the ePIXpack platform, within the ePIXnet network of excellence [58]. This prototype is designed for vertical fiber couplers, with a fiber array up to 32 fibers. A first example with an eight fiber array was also firstly developed in [100] and is shown in Fig. 5.5. This approach makes use only of commercially available components such as the fiber array and the ceramic pin grid array carrier. The package can be configured to provide only electrical, only optical, or both electrical and optical connectivity. It is based on an SOI chip design, which uses standardized pitches for grating couplers and bond pads. A similar approach has been taken by Luxtera [101], which is depicted in the Fig. 5.6. However, such vertical orientation is not easy to adapt to standard layouts for optoelectronics devices where, quite often, we have horizontal orientation. Also it is not really attractive in general to have such a loss of space on the top of the final device (we can have many mm of lost space in thickness). Thus, this approach offers a high profile packaging, which might be a problem, for instance, when inserting the package in a board

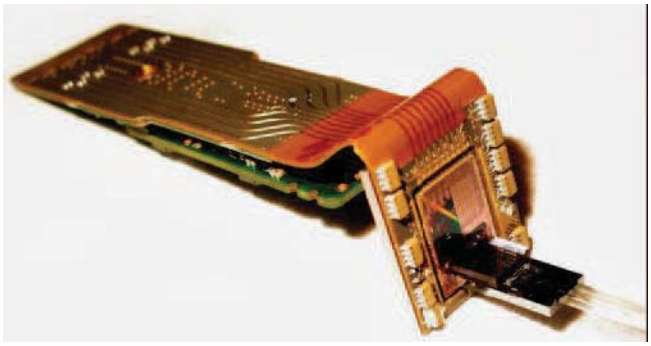


Figure 5.6: Luxtera packaging solution. CMOS 4x10 Gb/s WDM die on flexible circuit and fiber-array pigtail [101].

(see Fig. 5.5).

5.3 Packaging solution for grating coupler SOI devices

Trying to overcome such limit, we started to think of developing a generic packaging solution to allow the possibility to use such pigtailed components inside standard dual-in-line (DIL) or Butterfly Packages, a solution that could permit, where necessary, not to change the usual horizontal orientation of the completed packaged device as well to have a more rational footprint. The simple concept arises from well known pin-diodes die-attachment applications where it is very usual to have substrates where to attach and connect the dies in the proper and most suitable way. In our particular case we know that we have to change the fibers orientation from vertical, as requested by the grating structure, to horizontal, so we think that the best approach is to consider the SOI component as a simple die and to attach it, using UV epoxy for instance, to the lateral side of a sub-mount substrate carrier (i. e. dielectric, metal or ceramic, depending on the application requeriments), designed in such a way that the eventual transmission lines or electrical connection runs from the lateral side to the top side, as showed in Fig. 5.7. Thus, the required CMOS electronic chip can be placed on top of

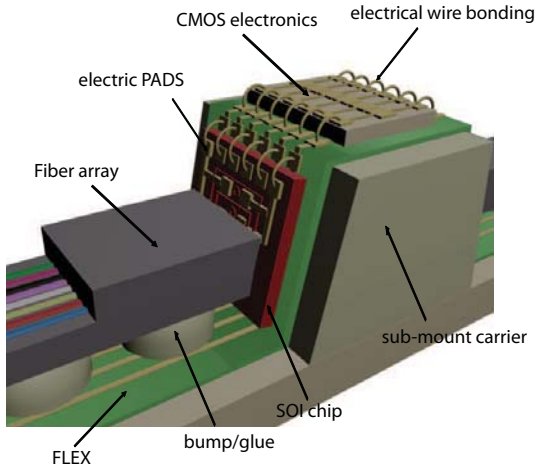


Figure 5.7: Scheme of subassembly for orientation change.

the carrier, and wire bonded to the electrical PADS of the photonic chip. A flexible wiring layer (FLEX) underneath the circuits and the fiber array can be used for improving the electrical connections when needed, thus making easier the electrical wire bonding between photonics and electronic circuitry (see Fig. 5.7). As a matter of fact we create a sub-assembly that can be, in a second step, easily mounted inside a package cavity, in the preferred position, and it is simple to imagine that the fibers can exit from the package throught a frontal cavity properly designed or a ferrule. Looking at the drawing in Fig. 5.7 it is clear that, with the use of such a submount, it is easy to connect, later on, the gold pads on the top of the same substrate directly to the package outputs. It is also possible, eventually, to integrate components on the submount itself, both on the lateral side and the top side. In Fig. 5.8 we show an example of design, placing our sub-assembly inside a cavity of a butterfly package. In this example, we consider two identical SOI chips attached to the carrier, each of them coupled to a different 8-fiber fiber array. The electronic chip is placed on top of the carrier. It can also be shown the flexibility of using the FLEX also to wire bond electronic wires to the external PINs of the package.

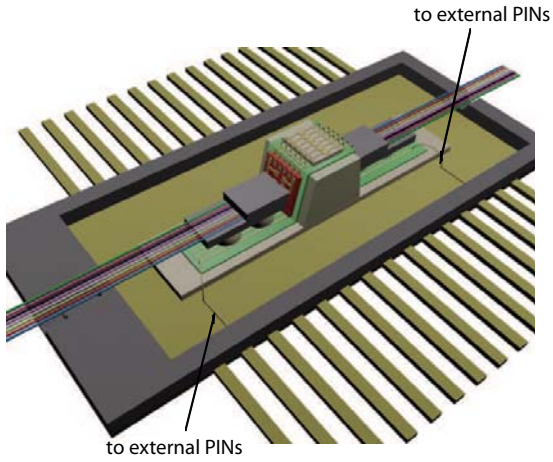


Figure 5.8: Package design concept with a butterfly package.

5.3.1 Description of the packaging solution

The objective of the proposed packaging solution is to achieve low profile packaging of PICs with vertical fiber coupling containing either individual fibers, a fiber ribbon or multiple optical ports with a fiber array interconnection. The proposed approach is basically based on the utilisation of a metallic/dielectric/ceramic sub-mount carrier to build an apparatus for placing on their sides the PICs perpendicular to the fibers, thus offering a horizontal orientation for the fibers which is more suitable for standard low profile packaging solutions, where, quite often, there is lateral (horizontal) orientation. In the case of applications that need electrical connections for the PICs, the electronic circuit is placed on top of the carrier, and their contact pads interconnected by i. e. wire bonding. For making easier the electrical wiring between electronic and photonic circuits, a FLEX is glued on top of the carrier and underneath all the circuits. The circuits can then first be connected to the wires in this FLEX by using any existing wiring technique such as wire bonding, and then place the FLEX containing all circuits on top of the carrier, thus allowing in plane bonding, which is strongly desired especially because of the corners of the carrier. The use of a FLEX for electrical connections also allows the design of the proposed technique for multiple fiber

array interconnections, just by designing the carrier with the proper shape for containing as much fiber arrays as desired. This fact dramatically increases the functionality of the proposed solution, as it is possible to reduce the total volume of the package but exponentially increasing the number of optical fibers attached to the same package, thus offering very smart low profile packaging. The carrier containing both the electronic circuit, the FLEX as well as the PICs, also attached to the optical fibers, can then be easily placed in any existing kind of standard package, such as butterfly or surface mounting technologies, depending on the specific application requirements. Bonding the electrical connections to the pins of the package is also improved by the use of the FLEX, as it offers a very flexible way for the wiring. Moreover, also depending on the application, and due to the utilisation of this FLEX, for particular cases of the invention, the carrier can be directly wired to the board without using any further packaging level, and also by properly designing the structure. Furthermore, and also due to the flexibility of using the FLEX, the electrical connections on this flexible layer can be directly attached to any connector for the interconnection of the carrier to any circuit board without having to use any further packaging level when desired, thus making the carrier acting as a package itself. It is important to emphasize that all elements and pieces thought for taking this solution into practise are standard elements that can be easily obtained commercially, which is very suitable for cost effective and smart photonics packaging.

5.3.2 Detailed description

Fig. 5.9 provides a three dimensional drawing of the basic configuration of the packaging solution showing the aspect of the submount carrier (1) for placing the circuits in a particular case when packaging two different PICs (2,3) with vertical fiber coupling also attached to a different fiber array (4,5) containing 8 optical fibers (6,7) each. In this configuration, we consider we want to attach two different opto-electronic circuits to its corresponding fiber array, so that we consider a submount carrier as the depicted in Fig. 5.9 for placing at its faces the circuits. The fiber arrays (4,5) can also be individual fibers or a fiber ribbon. Although fiber arrays with 8 fibers are considered in the drawing, same solution

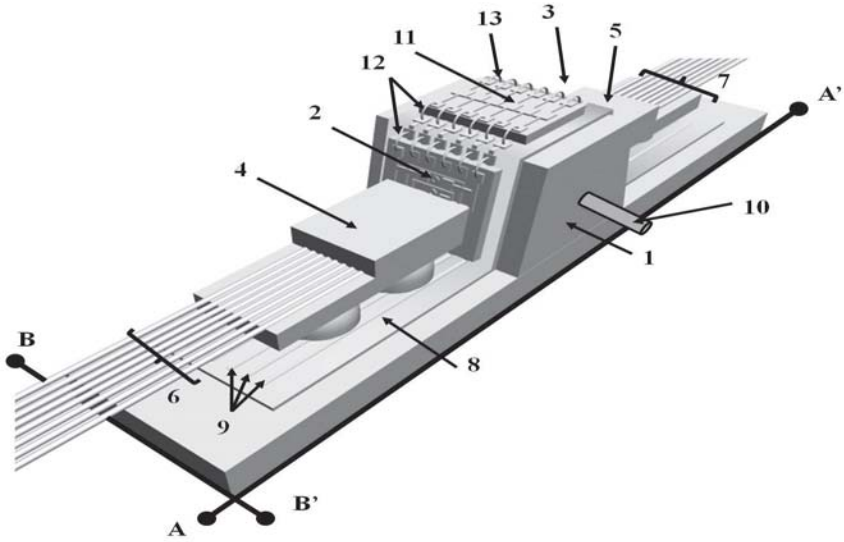


Figure 5.9: Three dimensional drawing of the generic packaging solution for multi-port grating coupler SOI devices.

can be adopted for any kind of fiber array containing up to 48 fibers. The material for the carrier should be either any metal or any dielectric material depending on the application and on the heating. When using a metallic carrier, the carrier itself can also act as a heat dissipater of the circuits. A thermistor (10) can also be attached to the carrier in this particular case for temperature/heating control and feedback, and peltiers can also be integrated to the photonic circuits also for this temperature/heating control. The carrier is covered by a FLEX (8) containing the electrical wires (9) for electrical signal distribution to the circuits, and the photonic circuits (2,3) are placed over of the FLEX in each side of the carrier. The electronic circuit (11) for processing and distributing the electrical signals to the photonic circuits is placed on top of the carrier. Then, electronic an photonic circuits are wire bonded (12,13) to the FLEX, thus making easier the bonding, as there is no need to bond in the corners of the sub mount carrier due to the presence of the FLEX. Fig. 5.10 depicts cross and top section views of the package solution in Fig. 5.9 along lines AA' and BB', respectively. It can be

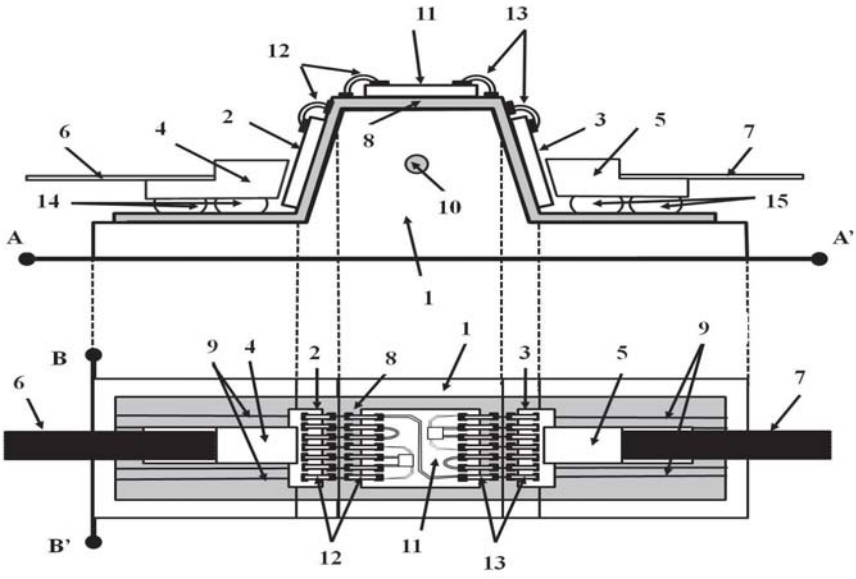


Figure 5.10: Cross and top section views of the package solution in Fig. 5.9.

seen as the sides of the sub mount carrier (1) are slightly tilted depending on the coupling angle of the resonant vertical fiber coupling technique of the photonic circuits (2,3). The whole carrier is covered by the FLEX (8) for the electrical connections (9). The electronic circuit (11) which drives electrical signals to the photonic circuits is placed on the top of the carrier. By using the FLEX, the electrical connections of all the circuits can be first wire bonded (12,13) to the flexible layer and then attach the flexible layer containing the circuits to the carrier, thus avoiding an out of plane wire bonding, which would be much more complicated, especially because of the high slopped corners of the carrier. The fiber arrays (4,5) holding the optical fibers can then be aligned and attached to the sub mount carrier containing all the circuits electrically interconnected through the FLEX underneath. For fixing the fiber arrays to the carrier, it can be used, for instance, any kind of bump/glue (14,15) underneath the fiber arrays, as well as for fixing all circuits to the FLEX. Having bump/glue below the fiber arrays cannot be good, and maybe it is better to leave the fiber arrays floating

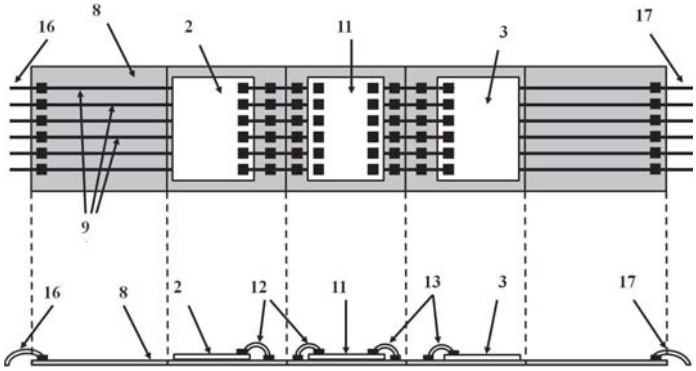


Figure 5.11: Top and section views of first possible configuration for the FLEX.

on the sub mount holder. The reason is to reduce stress and movements during thermal cycles for instance. In that cases it can be avoid the use of bump/glue underneath the fiber arrays, or they can even be fixed in a different way than using bump/glue.

5.3.2.1 Extensions for different shape FLEX designs

The major flexibility of the proposed packaging approach is due to the use of the FLEX for the electrical interconnections. Actually, for the design of the FLEX we can think of many different possibilities. Fig. 5.11 depicts both top and side section views of one of the possible configurations for the FLEX, also corresponding to the case depicted in Figs 5.9 and 5.10. In this configuration, the flexible layer (8) occupies the whole carrier. The photonic circuits (2,3) an the electronic circuit (11) are then wire bonded (12,13) to the wires (9) of the FLEX. The electrical interconnections of the FLEX to the outside world (i. e. to external pins) can so be done through the edges of the flexible layer (16,17) underneath the fiber arrays by using either wire bonding to the external package pins, or just by connecting the FLEX edge (16,17) to any existing kind of connector if the application does not require any other further packaging level.

Fig. 5.12 depicts other possibility for the design/implementation of the FLEX (8). A detail of the side and top view of the FLEX configuration is depicted

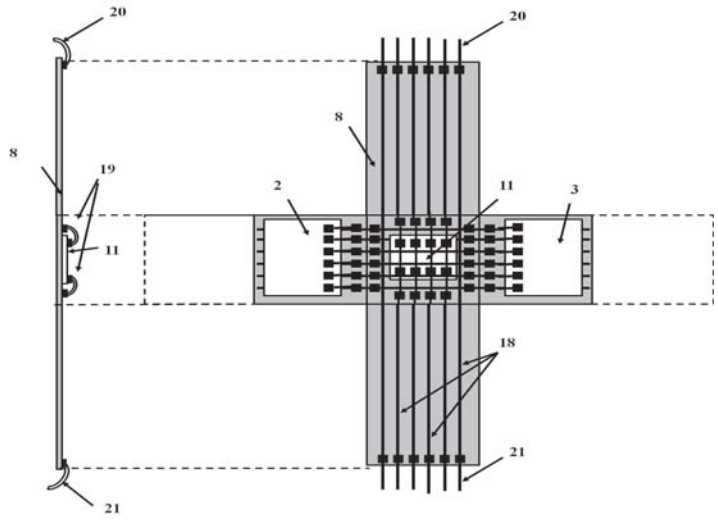


Figure 5.12: Top and section views of second possible configuration for the FLEX.

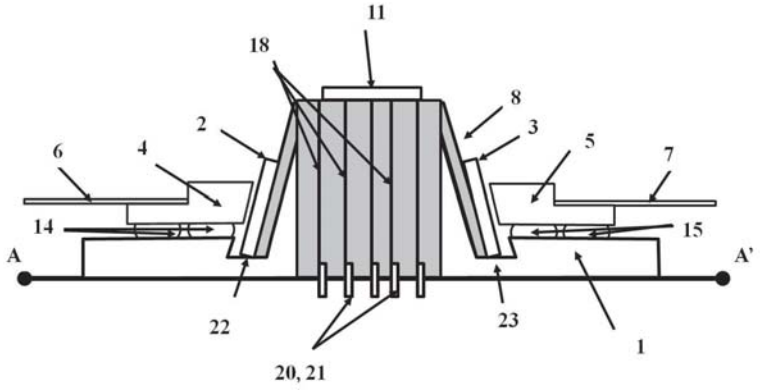


Figure 5.13: Solution for solving the problem when the couplers are disposed in a very high position with respect to the fibers in the fiber array.

in Fig. 5.12. In this case, the FLEX (8) just occupies the space in which the photonic (2,3) and electronic (11) circuits are attached to, so that there is no wiring layer underneath the fiber arrays. For connecting to the outside world (20,21), the FLEX is designed to be extend to the sides of the carrier opposite to

the photonic circuits sides (see Figure 4b). This solution is more flexible for the alignment and glueing of the fiber arrays to the photonic circuits. Again, electrical interconnections of the FLEX to the outside world can so be done through the edges of the flexible layer (20,21) by using either wire bonding to the external package pins, or just by connecting the FLEX edges (20,21) to any existing kind of connector if the application does not require any other further packaging level. Fixing the fiber arrays with bump/glue (14,15) underneath the fiber arrays can be in general a problem for the alignment to the optical fibers, especially if the thickness of the glue is so high. Moreover, even in the case we decide not to use bump/glue and leave the fiber arrays floating on the sub mount carrier holder, the alignment can be more problematic as the photonic circuit has to be fixed to the carrier in a specific position, strongly depending on the fiber array position. If the couplers are disposed in a very high position with respect to the fibers in the fiber array, the space needed between the fiber array and the bottom of the carries will be higher, also relying on a thicker layer for the bump/glue. With the configuration in Fig. 5.12, this problem can be solved with the solution depicted in Fig. 5.13, by implementing a hole with the proper dimensions at each side of the carrier (22,23) in which has to be attached the photonic circuits. By doing these holes, the flexibility in the alignment increases, making possible an easier control of the space between the fiber array and the bottom of the carrier for better fixing performance. This configuration is also more flexible for the case in which no bump/glue (14,15) is used underneath the fiber arrays. Fig. 5.14 depicts other possibility for the implementation of the FLEX. It consists of the utilisation of FLEX pieces (24,25,26,27) just in the link between the photonic (2,3) and electronic (11) integrated circuit as well as in the link to the external connection (31,32). The circuits can then be individually attached to any kind of printed circuit board (PCB) (28,29,30) and linked them through the FLEX pieces (24,25,26,27). When integrating this solution with the approach described in Fig. 5.12 we obtain a new solution as the depicted in Fig. 5.15 for connecting the FLEX to the outside world (20,21) through the sides of the carrier opposite to the photonic circuits. Again, the electrical interconnections of the FLEX to the outside world can so be done through the edges of the flexible layer (20,21) by using either wire bonding to the external package pins, or just by connecting

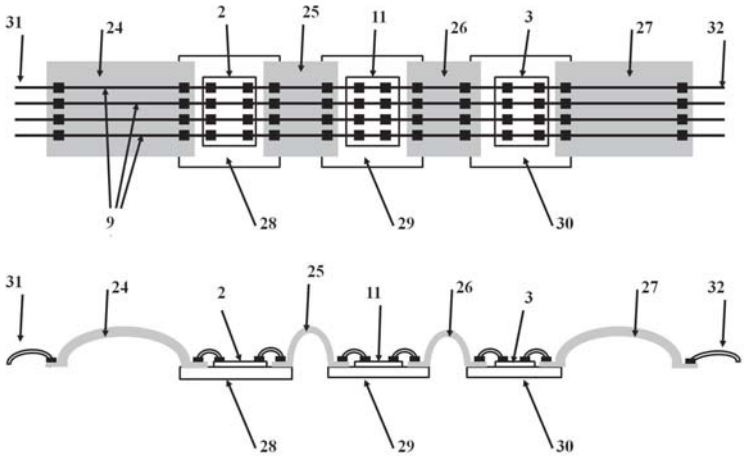


Figure 5.14: Top and section views of third possible configuration for the FLEX.

the FLEX edges (20,21) to any existing kind of connector if the application does not require any other further packaging level. This configuration can also be integrated with the idea described in Fig. 5.13 of making the holes in the bottom of the carrier for having more flexibility in the alignment with the fiber arrays for a better glueing/fixing to the carrier.

5.3.2.2 Mirroring and arrays

The implementation of an arrayed package with the adopted solution can also be carried out by mirroring the carrier (1) along the section line AA', as shown in Fig. 5.16(a). By doing this, different packages can be piled up for implementing a more complex package solution thus extremely increasing the flexibility on the compactness of the proposed packaging approach, as shown in Fig. 5.16(b). Although in Fig. 5.16(b) it has just depicted an array of four elements showed in Fig. 5.16(a), it can also easily extended to a higher number of elements just by adding them on top of each other following same approach than the illustrated in Fig. 5.16(b). The flexibility of using FLEX can go even further. We can design the wiring layer properly with a determined shape for attaching more than two photonic circuits to the same carrier. According to the depicted top view of the

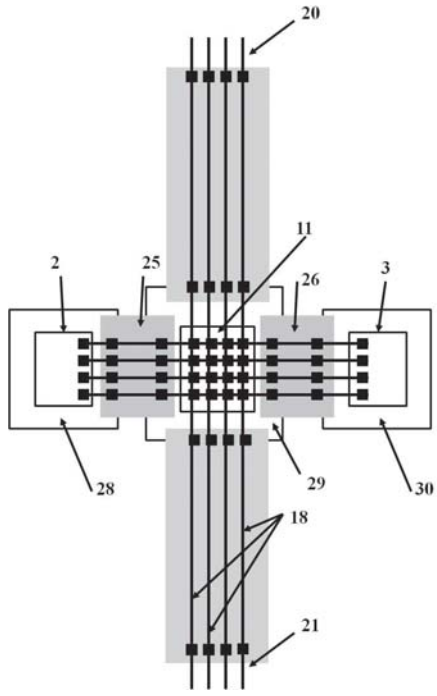
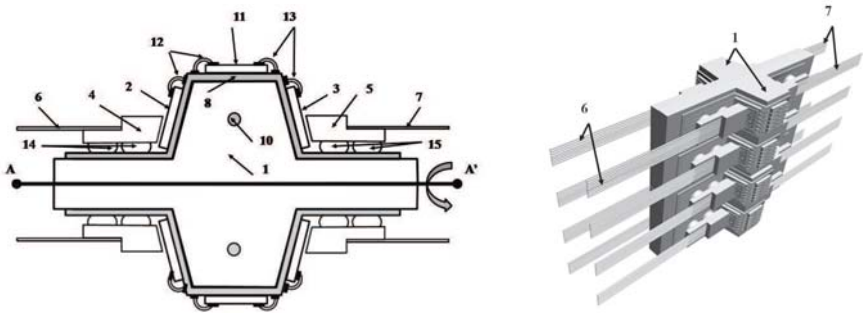


Figure 5.15: Top and section views of fourth possible configuration for the FLEX.



(a) (b)

Figure 5.16: (a) Mirroring of the adopted packaging solution for creating arrays. (b) Example of an array package composed by four elements showed in (a).

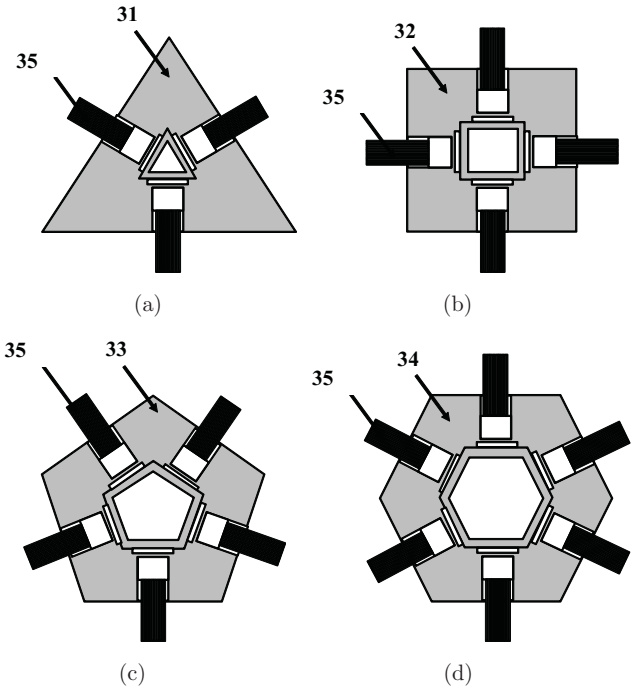
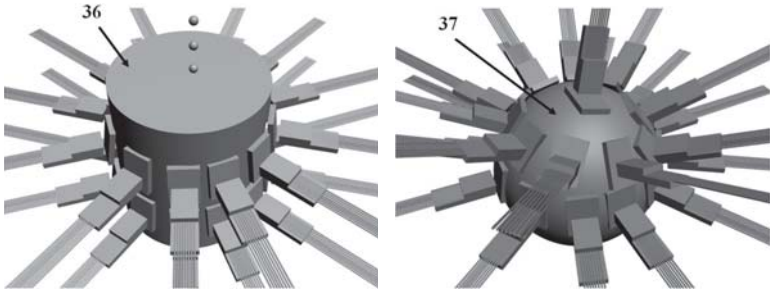


Figure 5.17: Possibility for creating arrays in a planar way just by designing a FLEX with (a) triangular, (b) squared, (c) pentagonal and (d) hexagonal shape.

proposed packaging approach in Fig. 5.17(a), by designing a triangular shape FLEX (31), we can interconnect up to 3 fiber arrays (35) to the same carrier. Moreover, as depicted in Fig. 5.17(b), a squared shape FLEX (32) can hold up to 4 fiber arrays (35) in the same carrier. Interpolating these results to a higher number of sides of the carrier, and as depicted in Figs. 5.17(c) and 5.17(d) respectively, by designing a pentagonal (33) and hexagonal (34) shape FLEX, the same carrier can even hold up to 5 and 6 different fiber arrays (35), respectively. This can also extrapolated to carrier shapes with more than 6 facets for attaching as much as circuits and fiber arrays as needed. All extensions for multiple fiber array interconnections depicted in Fig. 5.17 are for sure planar arrays, as the array is extended just in a plane. For future packaging solutions, a three dimensional package extension of the invention can be made when considering the extension



(a) (b)

Figure 5.18: 3D packaging solutions based on the proposed approach, showing (a) cylinder and (b) sphere FLEX shape based designs.

of the arrays in more than one plane. Fig. 5.18(a) illustrates an example of extension of a three dimensional package considering a cylinder shape FLEX (36). In this case, the array of fiber arrays is in one plane but can be extended all around the cylinder height. In Fig. 5.18(a) we depicted an example with two levels of packaging along the cylinder height but for sure it can be extended to higher levels, as well as in the same plane the number of fiber arrays can be higher, depending on the size of the cylinder basis. Fig. 5.18(b) depicts another extension to three dimensional packaging when considering a sphere shape FLEX (37). Fig. 5.18(b) consists of the most generic approach one can imagine for future three dimensional packaging, but of course the FLEX can have any arbitrary shape.

5.3.3 Demonstrator prototyping

After the study and investigation of the proposed packaging approach previously presentd, we started to fabricate a demonstrator prototype in collaboration with Fraunhofer IZM Institute and Technical University of Berlin. For the realization of the demonstrator, we will focus in the configuration previously depicted in Fig. 5.9. In our demonstrator we will not include any electronic circuitry on top of the submount carrier for the time being. So, our demonstrator will include two different SOI chips attached to the submount carrier in the package, each of them also attached to a different fiber array (see Fig. 5.9). The first step for

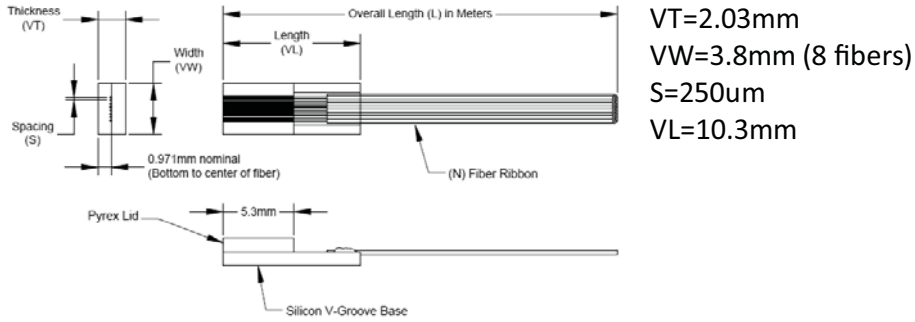


Figure 5.19: Dimension specifications for a fiber array with 8 optical fibers from the company OZOptics.

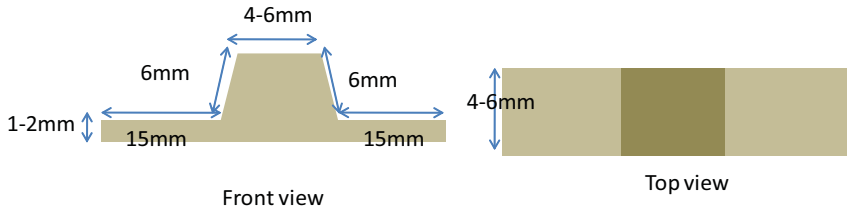
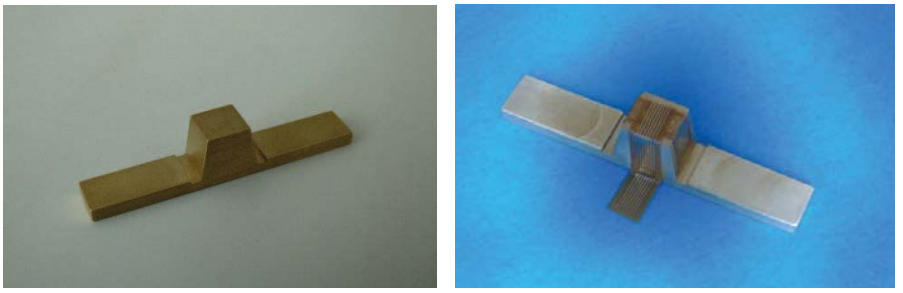


Figure 5.20: Dimensions of the built submount carrier.

building our demonstrator of the proposed packaging approach was to fabricate the submount carrier. We chose a metallic submount carrier for our demonstrator. The dimensions of the submount carrier depend on the dimensions of the SOI chip, as well as on the dimensions of the fiber array. The dimensions of the fiber array can be checked in the specification datasheet from the manufacturer. We used fiber arrays from the company OZOptics, and the dimensions for a fiber array of an array of 8 optical fibers are depicted in Fig. 5.19. So, we decided to build a submount carrier with the dimensions depicted in Fig. 5.20 After fabricating the submount carrier, the next step was to fix the flexible layer (FLEX) on top of the submount carrier. In our demonstrator we used conventional glue. In real applications it has to be taken into account the proper bump, glue or any other kind of fixing material, also considering thermal issues of the device and so on. Next step in the fabication of our prototype is the fiber array pigtailing to the



(a) (b)

Figure 5.21: Photo of the fabricated submount carrier (a) without and (b) with the FLEX layer on top.

SOI chips. Previous to the glueing, the SOI chip and the fiber array were aligned for optimum coupling to fiber, using the same chips previously characterized in Fig. 3.31 (device D3, see section 3.3.3.1). For the glueing, we used the glue OP-4-20647, whose refractive index @ λ=1550 nm is 1.45, similar to the optical fiber core refractive index. This glue has also to be cured after deposited on top of the chip with UV light. Fig. 5.22 depicts a photo while epoxy curing after the fiber-to-chip alignment for fixing the fiber arrays to the SOI chips. We noticed that just 1dB extra loss was obtained after glueing in the output power of the gratings for λ=1550nm. This extra loss is mainly due to the fact that the grating couplers of the used SOI chips were optimized for an air refractive index uppercladding (n=1), whereas the glue used on top for the fiber pigtailing has a refractive index of n=1.45 for λ=1550 nm. Fig. 5.23 depicts a photo of the SOI chips glued to the fiber arrays after fiber pigtailing in comparison to a 1 Euro cent coin. Then, the SOI chips glued to the fiber arrays were afterwards glued to the submount carrier for building our demonstrator using conventional glue. To fill the gap underneath the fiber array, we used a piece of glass and glued it to the submount as well as to the fiber array. In real applications it has to be taken into account the proper bump, glue or any other kind of fixing material, also considering thermal issues of the device, as well as mechanical robustness of the device and so on. Fig. 5.24 depicts a photo of the fabricated demonstrator, in comparison to a 1 Euro cent coin. Finally, Fig. 5.25 depicts experimental measurements of the transmission

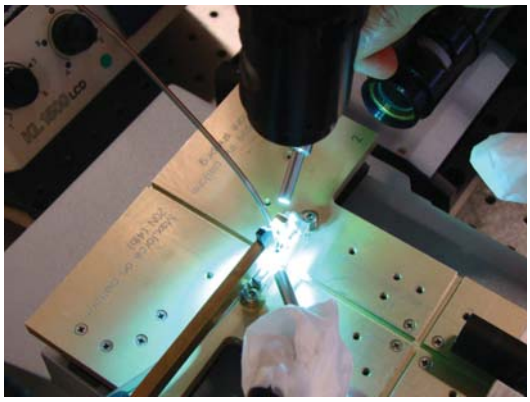


Figure 5.22: Photo of the epoxy (glue) curing process after the fiber-to-chip alignment for the fiber array pigtailing to the SOI chips.

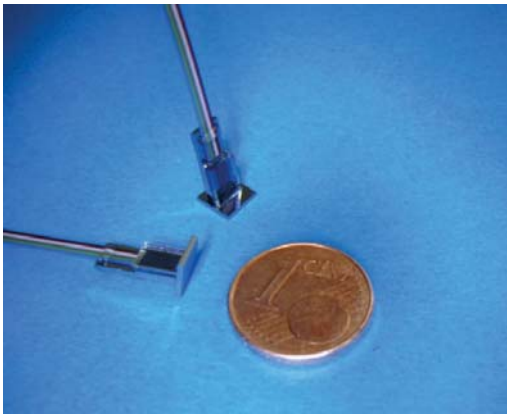


Figure 5.23: Photo of the SOI chips glued to the fiber arrays after fiber pigtailing in comparison to 1 Euro cent. coin.

spectrum of the grating couplers of the demonstrator after glueing. Comparing the spectrum in Fig. 5.25 to the spectrum in Fig. 3.31 (same chips after and before glueing, respectively), we observe that a more clean spectral response is obtained after glueing process, due to the index matching glue. 1dB extra loss is observed in the transmission spectrum, as previously discussed. A slight shift of about Δ=0.005λ to higher wavelengths of the spectral response is also observed

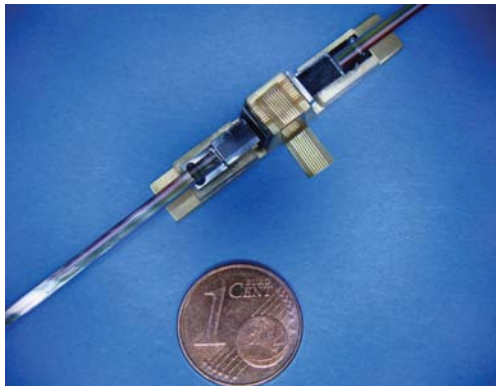


Figure 5.24: Photo of fabricated demonstrator prototype in comparison to 1 Euro cent. coin.

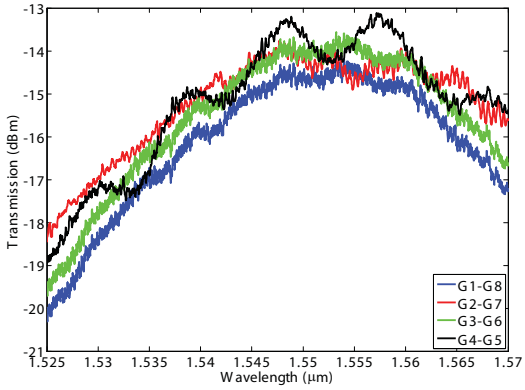


Figure 5.25: Experimental measurements on the transmission spectrum of the grating couplers of the demonstrator after glueing.

after glueing.

5.4 Summary and conclusions

In this chapter we have seen several packaging solutions for SOI chips incorporating the coupling techniques previously developed in this thesis. First, a brief

overview on silicon photonics packaging was introduced. Here we pointed out the strong relation between the coupling to fiber and the fiber pigtailing, which is the previous step towards the packaging and assembly of silicon devices. We show the importance of fiber pigtailing in multiport silicon devices, and the benefits of using grating couplers for multiple fiber pigtailing mainly due to large alignment tolerances of the gratings. Then, we reviewed some examples existing in literature of packaging of multiport silicon devices with vertical coupling to fiber via grating couplers. All these configurations offer a vertical orientation of the optical fibers, which may be a problem in standard integration of such devices where, quite often, we have horizontal orientation. Trying to overcome such limit, we present a novel configuration of packaging for multiport grating coupler SOI devices, which offers a horizontal orientation of the optical fibers in the package, by placing the silicon device at the sides of a submount carrier for pigtailing the fibers to the device perpendicularly. A detailed study of the proposed packaging approach was reported. We initially focused on fiber pigtailing using a 8-fiber fiber array, but the proposed packaging approach can be easily extended to a higher number of fibers. The basic configuration of the proposed approach was with the pigtailing of two equal SOI chips inside the package. The use of flexible wiring layer (FLEX) on top of the submount carrier is also explained, for electrical signal wiring in the package, thus offertin both electrical and optical interconnection. Different configurations of the proposed approach with different FLEX shape designs were discussed, overcoming all the benefits and drawbacks. A discussion on creating arrays of the proposed package approach was then addressed. This possibility o array packaging is then used to introduce novel futurist 3D packaging solutions based on the proposed approach. Finally, a demonstrator based on the basic configuration of the packaging approach was performed. The fabrication of a metallic submount carrier was first done, for further attaching the FLEX on top. Then, the pigtailing of two SOI chips to their corresponding fiber array was made, by using UV curing epoxy glueing. Then, the attachment to the submount carrier of the SOI devices pigtailed to the fiber arrays was done. Experimental measurements of the transmission spectrum of the gratings after pigtailing were finally reported. In conclusion, 1dB extra loss after pigtailing was

obtained, compared to experimental measurements of transmission spectrum of the gratings before fiber pigtailing.

Chapter 6

Conclusions and perspectives

This last chapter deals with the main findings and conclusions of this work. Some ideas and prospects that are based on the presented results for possible future research work and lines are also discussed.

6.1 Conclusions

Silicon photonics has seen some impressive developments in recent years, and the main breakthrough of silicon photonics community is still to transfer all the research results and highlights to the industry. Fig. 6.1 summarizes the natural process from research to industry in silicon photonics. We can distinguish three main stages: 1) research, 2) technology transfer and 2) industrialization. Stages 1) and 2) can be considered to be included in a wider stage that we call $R\&D\&I$, as both sub-stages require research, development and investigation issues, previous to the technology industrialization.

Basically, the process starts with the identification of a problem in a specific technology, and the first stage is dedicated to get a research-level component to solve the problem previously identified. This research stage so involves theory, modelling, simulation, fabrication and testing of these research-level components. The obtained component is the input of the next technology transfer stage, so that, together with possible new demonstrator parameters and closed specs, will try to get a demonstrator prototype as a first step to convince the industry the possibility of commercializing the technology. In the technology transfer stage,

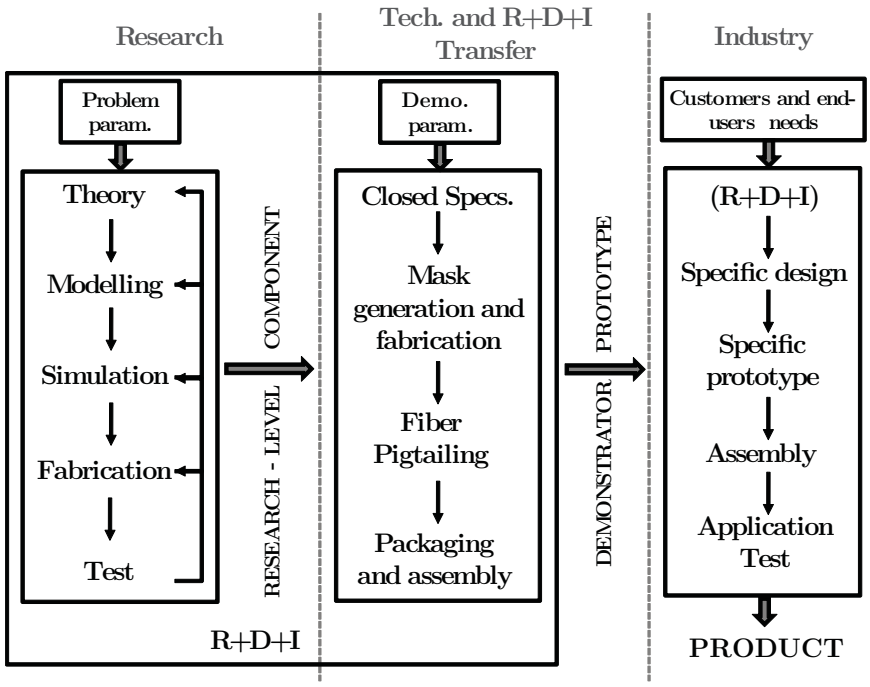


Figure 6.1: From research to industry in silicon photonics.

new mask generation, fabrication and testing of the component may be needed, according to the possible new closed specifications. At the end of this stage, fiber pigtailing and packaging and assembly of the prototype is also performed for the first time, and after successful work, the demonstrator prototype is so transferred to the industry. This prototype, together with novel specifications from the end users for a particular application, will serve to the creation of a specific design, together with final fabrication, packaging and test for this particular application.

The key technological problem to solve in this research work has been the coupling between optical fibers and silicon photonic integrated circuits. In this work, we have covered the first stage of the process depicted in Fig. 6.1 and obtained research-level components based on the investigated efficient coupling techniques in SOI technology. We also focused a bit on the second stage, by taking as input the research level components previously obtained, for finally

demonstrating a prototype of a packaged device. Of course, for transferring to the industry all research work developed in this thesis, lower coupling loss may be needed, as industry requeriments in terms of coupling are stronger, and may rely on <1dB in most cases. This will be discussed in the next section.

So, the main highlights concerning the obtained results in this work are listed as follows:

- Experimental demonstration of SOI grating couplers with 31% coupling efficiency, and expected near maximum 50% efficiency from the obtained simulation results.
- Experimental demonstration of multiport SOI devices with grating couplers for coupling to a 8-fiber fiber array with 24% measured coupling efficiency and ± 2 μm @ 1dB penalty experimental alignment tolerances, and expected near 50% efficiency from the obtained simulation results.
- Experimental demonstration of grating couplers for horizontal slot waveguides with measured 20% coupling efficiency, and expected near maximum 48% efficiency for particular designs, according to simulation results.
- Experimental demonstration of CMOS compatible silicon etched V-grooves integrated with a SOI inverted taper-based fiber coupling technique for enhancing standard SMF fiber-to-chip alignment with measured 7dB coupling loss, and expected near 5dB loss from simulation results in particular designs.
- Theoretical study of inverted taper-based coupling technique for SOI horizontal slot waveguides with 93% maximum theoretcial coupling efficiency according to simulation results.
- Demonstrator prototype of a novel low-proflie packaging concept for multiport grating coupler SOI devices with horizontal orientation of the fiber array in the package, thus being integrable standard compatible.

A list of the publications and patents enclosing all the results obtained in this thesis was presented at the beginning of this thesis. The results directly obtained

within this work have been published in various peer-reviewed journal papers (J1-J8) and presented at various conferences (C1-C13), as well as one international meeting abstract (A1). The use of the obtained coupling techniques has also applied to different applications in silicon photonic devices, and led to other contributions to both journal papers (J9-J15) and conference proceedings (C14-C20). Moreover, the work on the proposed packaging approach for multiport SOI devices with grating couplers has been the subject of a patent application (P1).

6.2 Perspectives

There are several topics that could be the subject for further work. The first one is the investigation of more efficient grating couplers. Different strategies can be followed for reaching this. One strategy can be the investigation of chirped gratings, for changing the grating radiation properties for better matching to the Gaussian-like mode profile of the optical fiber [70]. Other strategy is the use of thicker gratings for improving the grating directionality for getting also higher coupling efficiencies [59]. Also adding a mirror in the SiO_2-Si substrate interface of the SOI wafer, the light which is in principle lost towards the substrate can be redirected to the waveguide top and interfere constructively with the light coupled to the waveguide, thus also improving coupling efficiency [68]. The main problem of all these strategies is that they require a very advanced technological platform in many cases. Based on the the combination of the strategies in [59,68], we were collaborating with IMEC-Ghent University in close cooperation within the context of EU-FP7-HELIOS project in the fabrication of non-uniform grating couplers with a DBR bottom mirror for achieving theoretical 92% coupling efficiency, according to theoretical results performed by our colleagues from Ghent University. A SEM image of fabricated samples by NTC and IMEC is shown in Fig. 6.2. The fabrication of the structures is not easy, as each grating period is different from each other, and some of them are below 20 nm size, so that e-beam lithography is needed to pattern the grating on the SOI wafer. Although the fabrication of the structures was performed successfully, the obtained experimental coupling efficiency was 69-70%, and comparable to the case of DBR mirror but

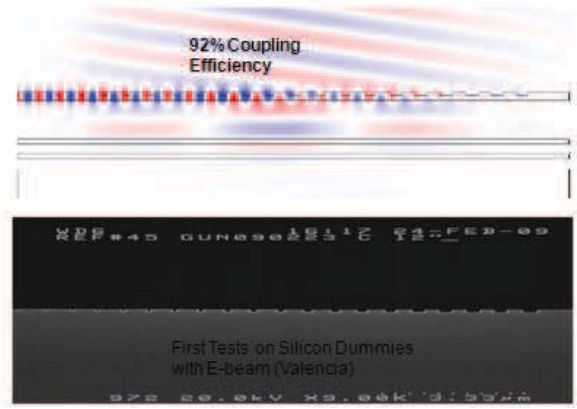
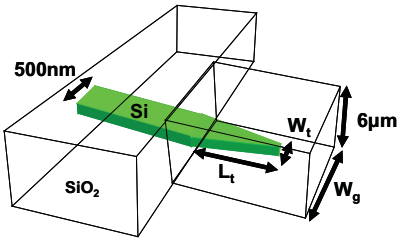


Figure 6.2: Diffracted field profile of an optimized non-uniform grating with bottom DBR mirror and a microscope image of the non-uniform grating structure.

uniform grating in [68]. The investigation on why we did not get any improvement when using a non-uniform grating is still under study.

The second topic that could be the subject for further work is the development of a more efficient inverted taper-based coupling structure for V-groove integration. One possibility could be using the same studied structure, but depositing on top of the structure a thicker SiO_2 layer, so that the mode matching with the wide optical mode of the fiber is more efficient. An schematic of the proposed structure and its main design parameters and coupling efficiency is shown in Fig. 6.3. Although we have done some theoretical investigations based on a 6μm thicker SiO_2 waveguide, and got coupling loss below 2dB, the fabrication of thicker SiO_2 layers on top of the SOI wafer is not easy and new samples are still running with a good fabrication progress, hoping to achieve good experimental results soon. The fabrication of the V-groove etched on silicon also needs to be improved, for getting an efficient fiber pigtailing and packaging prototypes.

Recently, we started to investigate the possibility of the integration of BCB polymer waveguides as fiber adapted waveguide on top of the silicon inverted taper. Conventional polymer integrated approach is shown in Fig. 6.4(a) and has been widely studied in literature before. The major problem of the approach

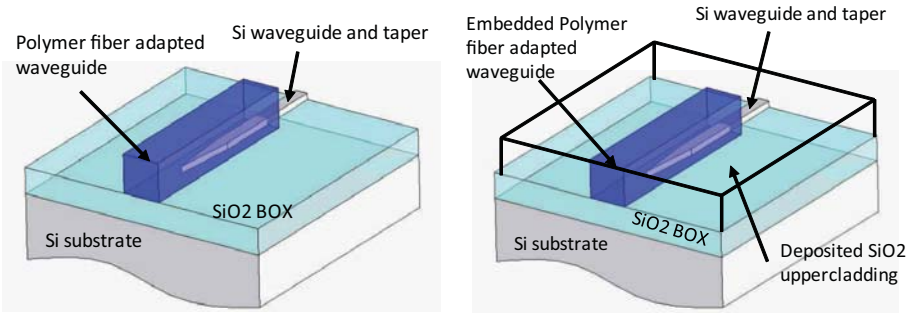


Parameters @ λ=1550nm, TE polarization, standard SMF fibers (MFD=10µm)			
L_t	W_t	W_g	Coupling loss
200µm	120nm	10µm	1.7dB

Figure 6.3: Proposed inverted taper-based structure for improving the coupling efficiency and theoretical parameters.

shown in Fig. 6.4(a) is the instability of the polymer on top of the SOI wafer, and the difficulty of covering the samples with a SiO_2 uppercladding layer on top, as the needed temperature for spin coating the SiO2 after BCB processing is quite high, and it may destroy the polymer waveguide. An alternative solution to this problem is to embed the BCB polymer waveguide in SiO_2 by doing first the SiO_2 deposition and opening etching windows for BCB filling, relying on the structure purpose depicted in Fig. 6.4(b). Optimum design parameters in terms of minimum coupling loss to standard SMF with MFD=2.5 μm are an inverted taper tip width downto 100 nm, a taper length ∼300 μm, and a polymer waveguide cross section dimension of 3 μm × 3 μm. The expected theoretical coupling loss are <1dB. The process flow for the realisation of the proposed structure depicted in Fig. 6.4(b) is shown in Fig. 6.5. A SEM image of preliminar fabrication of the structures is shown in Fig. 6.6. Fabrication improvement of the structure is still ongoing.

A third topic for future work will be the experimental demonstration of the inverted taper-based structure for horizontal slot waveguides. The main techno-



(a) (b)

Figure 6.4: (a) Polymer low index waveguide integration with inverted taper. (b) Embedded polymer low index waveguide integration with inverted taper solution.

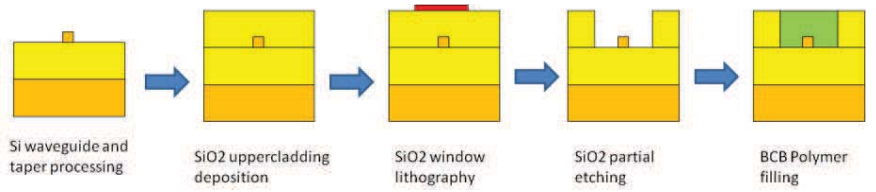


Figure 6.5: Process flow for the realisation of the proposed structure.

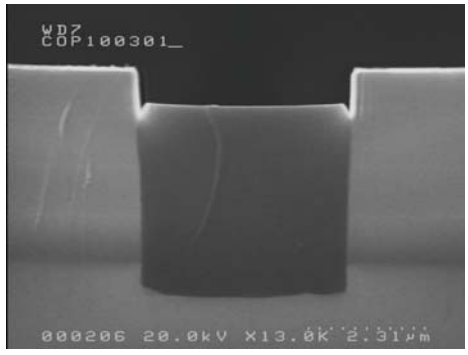


Figure 6.6: SEM image of preliminar fabricated structures.

logical problem concerning this will be getting such a narron inverted taper tip width of 40 nm, and may require of highly accurate e-beam lithography fabrication processes.

As a fourth possible topic for future work we can add the possibility of getting packaging concepts based on the ones investigated in this thesis, but applied to the new developed more efficient coupling techniques.

As a final topic, we can of course propose the realization of a complete demonstrator prototype based on the one developed in the thesis for multiport grating coupler SOI devices, but being more application orientated and also incorporating microelectronic circuitry driver on top of the submount carrier, an also allowing the opportunity of becoming a real product for the industry in the near future.

6.3 Summary of achieved results

Both in the case of diffractive grating couplers and in the case of inverted taper structures, important advances are made over the state-of-the-art. Concerning diffractive gratings, two types of structures have been demonstrated. On one hand, grating couplers suitable for conventional silicon waveguides have been achieved. On the other hand, diffractive grating structures are shown to work on horizontal slot waveguide structures for the first time, which are very promising for nonlinear optics applications. With regard to the coupling via inverted taper, a novel inverted taper-based structure is experimentally demonstrated. Using this structure, important advances are made in the packaging of optical fibers with the silicon waveguide circuit. Its innovative integration with V-groove structures is presented as a means to passively align arrays of fibers to a photonic integrated circuit. Also, packaging of fiber arrays using diffractive grating couplers is studied, resulting in a prototype of small form factor package.

Bibliography

[1] K. C. Kao and G. A. Hockham, "Dielectric-fiber surface waveguides for optical frequencies," *Proc. IEE*, vol. 113, pp. 1151–1158, 1966.

[2] W. A. Gambling, "The Rise and Rise of Optical Fibers," *IEEE J. Sel. Topics in Quantum Electron.*, vol. 6, pp. 1084–1093, 2000.

[3] J. Paul E. Green, "Fiber to the Home: The Next Big Broadband Thing," *IEEE Communications Magazine*, pp. 100–106, 2004.

[4] I. C. M. Littler, M. Rochette, and B. J. Eggleton, "Adjustable bandwidth dispersionless bandpass FBG optical filter," *Optics Express*, vol. 13, pp. 3397–3407, 2005.

[5] L. Yi, L. Zhan, W. Hu, Q. Tang, and Y. Xia, "Tunable gain-clamped double-pass Erbium doped fiber amplifier," *Optics Express*, vol. 14, pp. 570–574, 2006.

[6] C. Pollock and M. Lipson, *Integrated Photonics*. Springer, 2003.

[7] M. Lipson, "Guiding, Modulating, and Emitting Light on Silicon-Challenges and Opportunities," *IEEE J. Lightw. Technol.*, vol. 23, p. 4222, 2005.

[8] G. T. Reed, *Silicon Photonics: the state of the art.* John Wiley & Sons Ltd., 1st ed., 2008.

[9] B. Jalali, M. Paniccia, and G. Reed, "Silicon Photonics," *IEEE Microwave Magazine*, 2006.

[10] K. Uomi, S. Sasaki, T. Tsuchiya, H. Nakano, and N. Chinoe, "Ultralow Chirp and High-speed 1.55 μm Multiquantum Well λ4-Shifted DFB Lasers," *IEEE Photon. Technol. Lett.*, vol. 2, pp. 229–230, 1990.

[11] B. Jalali and S. Fathpour, "Silicon Photonics," *IEEE J. Lightw. Technol.*, vol. 24, pp. 4600–4615, 2006.

[12] S.-i. Itabashi, "R&D Trends in Silicon Photonics," *NTT Technical Review*, vol. 8, 2010.

[13] F. Y. Gardes, G. T. Reed, N. G. Emerson, and C. E. Png, "A sub-micron depletion-type photonic modulator in silicon on insulator," *Optics Express*, vol. 13, pp. 8845–8854, 2005.

[14] G. T. Reed, W. R. Headley, F. Y. Gardes, B. D. Timotijevic, S. P. Chan, and G. Z. Mashanovich, "Characteristics of rib waveguide racetrack resonators in SOI," *Proc. SPIE*, vol. 6183, p. 61830G, 2006.

[15] K. Yamada, H. Fukuda, T. Watanabe, T. Tsuchizawa, T. Shoji, and S.-I. Itabashi, "Functional photonic devices on silicon wire waveguide," *Proc. LEOS 2nd Group IV Photonics*, pp. 186–188, 2005.

[16] Y. Kuo, H. Park, A. W. Fang, J. E. Bowers, R. Jones, M. Paniccio, and O. Cohen, "High speed data amplification using hybrid silicon evanescent amplifier," *Proc. of CLEO 2007*, 2007.

[17] H. Rong, R. Jones, A. Liu, O. Cohen, D. Hak, A. Fang, and M. Paniccia, "A continuous-wave Raman silicon laser," *Nature*, vol. 433, pp. 725–728, 2005.

[18] V. R. Almeida, C. A. Barrios, R. R. Panepucci, and M. Lipson, "All-optical switching on a silicon chip," *Optics Lett.*, vol. 29, pp. 2867–2869, 2004.

[19] Q. Xu, V. R. Almeida, and M. Lipson, "Micrometer-scale all-optical wavelength converter on silicon," *Optics Lett.*, vol. 30, pp. 2733–2735, 2005.

[20] H. Zimmermann, *Silicon Optoelectronic Integrated Circuits*. Springer, 2004.

[21] R. Baets, W. Bogaerts, D. Taillaert, P. Dumon, P. Bienstman, D. Van Thourhout, J. Van Campenhout, V. Wiaux, J. Wouters, and S. Beckx, "Low Loss Nanophotonic Waveguides and Ring Resonators in Silicon-on-Insulator," *Majorana School of Quantum Electronics 39th Course: Microresonators as Building Blocks for VLSI Electronics, Erice, Italy, October 18-25*, 2003.

[22] G. T. Reed and A. P. Knights, *Silicon Photonics: an introduction*. John Wiley & Sons Ltd., 1st ed., 2004.

[23] K. Okamoto, *Fundamentals of optical waveguides*. Academic Press, 2000.

[24] H. Fukuda, K. Yamada, T. Tsuchizawa, T. Watanabe, H. Shinojima, and S. Itabashi, "Silicon photonic circuit with polarization diversity," *Optics Express*, vol. 16, pp. 4872–4880, 2008.

[25] J. V. Galan, M. Aamer, P. Sanchis, A. Griol, L. Bellieres, J. Ayucar, and J. Marti, "A compact and broadband polarization splitter in SOI," *Proc. of IEEE LEOS Annual Meeting, Antalya, Turkey*, pp. 309–310, 2009.

[26] H. Deng, D. O. Yevick, C. Brooks, and P. E. Jessop, "Design Rules for Slanted-Angle Polarization Rotators," *IEEE J. Lightw. Technol.*, vol. 23, pp. 432–445, 2005.

[27] J. Yamauchi, M. Yamanoue, and H. Nakano, "A Short Polarization Converter Using a Triangular Waveguide," *IEEE J. Lightw. Technol.*, vol. 26, pp. 1708–1714, 2008.

[28] Z. Wang and D. Dai, "Ultrasmall Si-nanowire-based polarization rotator," *J. Opt. Soc. Am. B*, vol. 25, pp. 747–753, 2008.

[29] V. Almeida, Q. Xu, C. Barrios, and M. Lipson, "Guiding and confining Light in void nanostructure," *Optics Lett.*, vol. 29, pp. 1209–1211, 2004.

[30] Q. Xu, V. Almeida, R. Panepucci, and M. Lipson, "Experimental demonstration of guiding and confining light in nanometer-size low-refractive-index material," *Optics Lett.*, vol. 29, pp. 1626–1628, 2004.

[31] N.-N. Feng, J. Michel, and L. Kimerling, "Optical field concentration in low-index waveguides," *IEEE J. Quantum Electron.*, vol. 42, p. 885, 2006.

[32] X. Tu, X. Xu, S. Chen, J. Yu, , and Q. Wang, "Simulation Demonstration and Experimental Fabrication of a Multiple-Slot Waveguide," *IEEE Photon. Technol. Lett.*, vol. 20, pp. 333–335, 2008.

[33] E. Jordana, J.-M. E. Fedeli, L. El Melhaoul, P. Lyan, J. Colonna, N. Daldosso, L. Pavesi, P. Pellegrino, B. Garrido, B. Vilá, and Y. Lebour, "Fully CMOS-compatible Fabrication of Slot Waveguides and Sandwiched Waveguides for Nonlinear Applications," in *Proc. European Conference on Integrated Optics (ECIO)*, 2007.

[34] E. Jordana, J.-M. Fedeli, P. Lyan, J. Colonna, P. Gautier, N. Daldosso, L. Pavesi, Y. Lebour, P. Pellegrino, B. Garrido, J. Blasco, F. Cuesta-Soto, and P. Sanchis, "Deep-UV Lithography Fabrication of Slot Waveguides and Sandwiched Waveguides for Nonlinear Applications," in *Proc. Group IV Photonics Conference*, 2008.

[35] C. A. Barrios, "High-performance all-optical silicon microswitch," *Electron. Lett.*, vol. 40, pp. 862–863, 2004.

[36] C. A. Barrios and M. Lipson, "Electrically driven silicon resonant light emitting device based on slot-waveguide," *Optics Express*, vol. 13, pp. 10092–10101, 2005.

[37] T. Baehr-Jones, M. Hochberg, G. Wang, R. Lawson, Y. Liao, P. A. Sullivan, L. Dalton, A. K.-Y. Jen, and A. Scherer, "Optical modulation and detection in slotted silicon waveguides, ," *Optics Express*, vol. 13, pp. 5216–5226, 2005.

[38] C. A. Barrios, "Ultrasensitive nanomechanical photonic sensor based on horizontal slot-waveguide resonator," *IEEE Photon. Technol. Lett.*, vol. 18, pp. 2419–2421, 2006.

[39] C. Barrios, K. Gylfason, B. Sanchez, A. Griol, H. Sohlstrm, M. Holgado, and R. Casquel, "Slot-waveguide biochemical sensor," *Optics Lett.*, vol. 32, pp. 3080–3082, 2007.

[40] C. Barrios, M. Bauls, V. Gonzalez-Pedro, K. Gylfason, B. Sanchez, A. Griol, A. Maquieira, H. Sohlstrm, M. Holgado, , and R. Casquel, "Label-free optical sensing with slot-waveguides," *Optics Lett.*, vol. 33, pp. 708–710, 2008.

[41] J. Robinson, L. Chen, and M. Lipson, "On-chip gas detection in silicon optical microcavities," *Optics Express*, vol. 16, pp. 4296–4301, 2008.

[42] G. P. Agrawal, Nonlinear Fiber Optics. Ed. Academic Press, 2001.

[43] L. Pavesi, L. Dal Negro, C. Mazzoleni, G. Franzo, and F. Priolo, "Optical gain in silicon nanocrystals," *Nature*, vol. 480, pp. 440–444, 2000.

[44] G. Vijaya, M. Cazzanelli, Z. Gaburro, L. Pavesi, F. Iacona, G. Franzo, and F. Priolo, "Nonlinear Optical Properties of Silicon Nanocrystals Grown by Plasma-Enhanced Chemical Vapor Deposition," *J. Appl. Phys.*, vol. 91, p. 4607, 2002.

[45] P. Sanchis, J. Blasco, A. Martinez, and J. Marti, "Design of Silicon-Based Slot Waveguide Configurations for Optimum Nonlinear Performance," *IEEE J. Lightw. Technol.*, vol. 25, pp. 1298–1305, 2007.

[46] A. Martínez, J. Blasco, J. V. Sanchis, P. Galán, J. García-Rupérez, E. Jordana, P. Gautier, Y. Lebour, S. Hernndez, R. Guider, N. Daldosso, B. Garrido, J. M. Fedeli, L. Pavesi, and J. Martí, "Ultrafast All-Optical Switching in a Silicon-Nanocrystal-Based Silicon Slot Waveguide at Telecom Wavelengths," *Nano Letters*, vol. 10, pp. 1506–1511, 2010.

[47] J. V. Galan, P. Sanchis, J. M. A. Garcia, J. Blasco, and J. Marti, "Study of asymmetric silicon cross-slot waveguides for polarization diversity schemes," *Appl. Optics*, vol. 48, pp. 2693–2693, 2009.

[48] J. V. Galan, P. Sanchis, J. Garcia, A. Martinez, J. Blasco, J. M. Martinez, A. Brimont, and J. Marti, "Silicon Cross-Slot Waveguides insensitive to polarization," *Proc. of IEEE LEOS Winter Topicals, Innsbruck, Austria*, pp. 32–33, 2009.

[49] K. Pei Yap, A. Delge, J. Lapointe, B. Lamontagne, J. H. Schmid, P. Waldron, B. A. Syrett, and S. Janz, "Correlation of Scattering Loss, Sidewall Roughness and Waveguide Width in Silicon-on-Insulator (SOI) Ridge Waveguides," *IEEE J. Lightw. Technol.*, vol. 27, pp. 3999–4008, 2009.

[50] A. Samarelli, M. Gnan, R. M. De la Rue, and M. Sorel, "Low propagation loss photonic wire and ring resonator devices in silicon-on-insulator using hydrogen silsesquioxane electron-beam resist," *Proc. of 14th European Conference on Integrated Optics (ECIO)*, vol. ThD1, pp. 309–312, 2008.

[51] J. Cardenas, C. B. Poitras, J. T. Robinson, K. Preston, L. Chen, and M. Lipson, "Low loss etchless silicon photonic waveguides," *Optics Express*, vol. 17, pp. 4752–4757, 2009.

[52] B. E. A. Saleh and M. C. Teich, *Fundamentals of Photonics*. John Wiley & Sons, 1991.

[53] D. Taillaert, W. Bogaerts, P. Bienstman, T. F. Krauss, P. Van Daele, I. Moerman, S. Verstuyft, K. De Mesel, and R. Baets, "An Out-of-Plane Grating Coupler for Efficient Butt-Coupling Between Compact Planar Waveguides and Single-Mode Fibers," *IEEE J. Quantum Electron.*, vol. 38, pp. 949–955, 2002.

[54] A. Sure, T. Dillon, J. Murakowski, C. Lin, D. Pustai, and D. Prather, "Fabrication and characterization of three-dimensional silicon tapers," *Optics Express*, vol. 11, pp. 3555–3561, 2003.

[55] T. Shoji, T. Tsuchizawa, T. Wanatabe, K. Tamada, and H. Morita, "Low loss mode size converter from 0.3 μm square Si wire waveguides to single-mode fibers," *Electron. Lett.*, vol. 38, pp. 1669–1670, 2002.

[56] K. D. Mesel, *Spot-size converters for photonic integrated circuits*. PhD thesis, Information Technology Group, Gent University, 2002.

[57] L. Vivien, S. Laval, E. Cassan, L. Roux, and D. Pascal, "2-D taper for low-loss coupling between polarization-insensitive microwaveguides and single-mode optical fibers," *IEEE J. Lightw. Technol.*, vol. 21, pp. 2429–2433, 2003.

[58] L. Zimmermann, T. Tekin, H. Schroeder, P. Dumon, and W. Bogaerts, "How to bring nanophotonics to application - silicon photonics packaging," *IEEE LEOS Newsletter December 2008*, pp. 4–14, 2008.

[59] D. Taillaert, F. Van Laere, M. Ayre, W. Bogaerts, D. Van Thourhout, P. Bienstman, and R. Baets, "Grating Couplers for Coupling between Optical Fibers and Nanophotonic Waveguides," *Japanese J. of Appl. Phys.*, vol. 45, pp. 6071–6077, 2006.

[60] J. K. Doylend and A. P. Knights, "Design and Simulation of an Integrated Fiber-to-Chip Coupler for Silicon-on-Insulator Waveguides," *IEEE J. Sel. Topics Quantum. Electron.*, vol. 12, pp. 1363–1370, 2006.

[61] A. Barkai, A. Liu, D. Kim, R. Cohen, N. Elek, H.-H. Chang, B. H. Malik, R. Gabay, R. Jones, M. Paniccia, and N. Izhaky, "Double-Stage Taper for Coupling Between SOI Waveguides and Single-Mode Fiber," *IEEE J. Lightw. Technol.*, vol. 26, pp. 3860–3865, 2008.

[62] V. R. Almeida, R. R. Panepucci, and M. Lipson, "Nanotaper for compact mode conversion," *Opt. Lett.*, vol. 28, pp. 1302–1304, 2003.

[63] G. Roelkens, P. Dumon, W. Bogaerts, D. Van Thourhout, and R. Baets, "Efficient Silicon-on-Insulator Fiber Coupler Fabricated Using 248-nm-Deep UV Lithography," *IEEE Photon. Technol. Lett.*, vol. 17, pp. 2613–2615, 2005.

[64] S. J. McNab, N. Moll, and Y. A. Vlasov, "Ultra-low loss photonic integrated circuit with membrane-type photonic crystal waveguides," *Opt. Express*, vol. 11, pp. 2927–2939, 2003.

[65] T. Tsuchizawa, K. Yamada, T. Watanabe, H. Fukuda, H. Nishi, H. Shinojima, and S. Itabashi, "Spot-Size Converters for Rib-Type Silicon Photonic

Wire Waveguides," *Proc. of IEEE Group IV Photonics Conference*, p. 200, 2008.

[66] M. Pu, L. Liu, H. Ou, K. Yvind, and J. M. Hvam, "Ultra-low-loss inverted taper coupler for silicon-on-insulator ridge waveguide," *Optics Com.*, vol. 283, p. 36783682, 2010.

[67] B. B. Bakir, A. Vazquez de Gyves, R. Orobtchouk, P. Lyan, C. Porzier, A. Roman, and J.-M. Fedeli, "Low-Loss (<1dB) and Polarization-Insensitive Edge Fiber Couplers Fabricated on 200-mm Silicon-on-Insulator Wafers," *IEEE Photon. Technol. Lett.*, vol. 22, pp. 739–741, 2010.

[68] F. Van Laere, G. Roelkens, J. Schrauwen, D. Taillaert, P. Dumon, W. Bogaerts, D. Van Thourhout, and R. Baets, "Compact Grating Couplers Between Optical Fibers and Silicon-on-Insulator Photonic Wire Waveguides with 69Coupling Efficiency," *Proc. of Optical Fiber Communication Conference and Exposition and The National Fiber Optic Engineers Conference, Technical Digest*, p. PDP15, 2006.

[69] D. Taillaert, P. Bienstman, and R. Baets, "Compact efficient broadband grating coupler for silicon-on-insulator waveguides," *Optics Lett.*, vol. 29, pp. 2749–2751, 2004.

[70] G. Roelkens, D. Van Thourhout, and R. Baets, " High efficiency Silicon-on-Insulator grating coupler based on a poly-Silicon overlay," *Optics Express*, vol. 14, pp. 11622–11630, 2006.

[71] D. Vermeulen, S. Selvaraja, P. Verheyen, G. Lepage, W. Bogaerts, P. Absil, D. Van Thourhout, and G. Roelkens, "High-efficiency fiber-to-chip grating

couplers realized using an advanced CMOS-compatible Silicon-On-Insulator platform," *Opt. Express*, vol. 18, pp. 18278–18283, 2010.

[72] P. Cheben, D.-X. Xu, S. Janz, and A. Densmore, "Subwavelength waveguide grating for mode conversion and light coupling in integrated optics," *Optics Express*, vol. 14, pp. 4695–4702, 2006.

[73] P. Dumon, W. Bogaerts, D. Van Thourhout, D. Taillaert, R. Baets, J. Wouters, S. Beckx, and P. Jaenen, "Compact wavelength router based on a Silicon-on-insulator arrayed waveguide grating pigtailed to a fiber array," *Optics Express*, vol. 14, pp. 664–669, 2006.

[74] B. Wang, J. Jiang, and G. P. Nordin, "Compact slanted grating couplers," *Optics Express*, vol. 12, pp. 3313–3326, 2004.

[75] B. Wang, J. Jiang, D. M. Chambers, J. Cai, and G. P. Nordin, "Stratified waveguide grating coupler for normal fiber incidence," *Optics Lett.*, vol. 30, pp. 845–847, 2005.

[76] G. Roelkens, D. V. Thourhout, and R. Baets, "High efficiency grating coupler between silicon-on-insulator waveguides and perfectly vertical optical fibers," *Optics Letters*, vol. 32, pp. 1495–1497, 2007.

[77] C. Gunn, "Fully Integrated VLSI CMOS and Photonics," *IEEE Symposium on VLSI Tecnology*, pp. 6–9, 2007.

[78] F. Van Laere, G. Roelkens, M. Ayre, J. Schrauwen, D. Taillaert, D. Van Thourhout, T. F. Krauss, and R. Baets, "Compact and Highly

Efficient Grating Couplers Between Optical Fibre and Nanophotonic Waveguides," *IEEE J. Lightw. Technol.*, vol. 25, pp. 151–156, 2007.

[79] A. Narasimha and E. Yablonovitch, "Efficient optical coupling into single mode Silicon-on-Insulator thin films using a planar grating coupler embedded in a high index contrast dielectric stack," *Proc. of Conference on Lasers and Electro-Optics/Quantum Electronics and Laser Science Conference, Technical Digest*, p. CWA46, 2003.

[80] M. Matsumoto, "Analysis of the Blazing Effect in Second-Order Gratings," *IEEE J. Quantum Electron.*, vol. 28, pp. 2016–2023, 1992.

[81] F. Van Laere, M. Kotlyar, D. Taillaert, D. Van Thourhout, T. F. Krauss, and R. Baets, "Compact Slanted Grating Couplers Between Optical Fibre and InPInGaAsP Waveguides," *IEEE Photon. Technol. Lett.*, vol. 19, pp. 396–398, 2007.

[82] C. Chen, X. Li and H. Ki Tsang, "Fabrication-Tolerant Waveguide Chirped Grating Coupler for Coupling to a Perfectly Vertical Optical Fibre," *IEEE Photon. Technol. Lett.*, vol. 20, pp. 1914–1916, 2008.

[83] J. V. Galan, P. Sanchis, G. Sanchez, and J. Marti, "Polarization insensitive low-loss coupling technique between SOI waveguides and high mode field diameter single-mode fibers," *Optics Express*, vol. 15, pp. 7058–7065, 2007.

[84] C. Peng and W. A. Challener, "Input-grating couplers for narrow Gaussian beam: influence of groove depth," *Optics Express*, vol. 12, pp. 6481–6490, 2004.

[85] D. Van Thourhout, G. Roelkens, R. Baets, W. Bogaerts, J. Brouckaert, P. DEbackere, P. Dumon, S. Scheerlinck, J. Schrauwen, D. Taillaert, F. Van Laere, and J. Van Campenhout, "Coupling mechanisms for a heterogeneus silicon nanowire platform," *Semicond. Sci. Technol.*, vol. 23, p. 064004, 2008.

[86] G. Roelkens, D. Vermeulen, F. Van Laere, S. Selvaraja, S. Scheerlinck, D. Taillaert, W. Bogaerts, P. Dumon, D. Van Thourhout, and R. Baets, "Bridging the Gap Between Nanophotonic Waveguide Circuits and Single Mode Optical Fibers Using Diffractive Grating Structures," *J. Nanosci. Nanotechnol.*, vol. 10, p. 15511562, 2010.

[87] E. G. Loewen and E. Popov, *Diffraction gratings and applications*. Marcel Dekker Inc., 1997.

[88] D. Taillaert, *Grating couplers as Interface between Optical Fibres and Nanophotonic Waveguides*. PhD thesis, Universiteit Gent, 2005.

[89] A. Yariv and M. Nakamura, "Periodic structures for integrated optics," *IEEE Journal of Quantum Electronics*, vol. 13, pp. 233–253, 1977.

[90] L. Vivien, D. Pascal, S. Lardenois, D. Marris-Morini, E. Cassan, F. Grillot, S. Laval, J. M. Fédéli, and L. El Melhaoui, "Light Injection in SOI Microwaveguides Using High-Efficiency Grating Couplers," *IEEE J. Lightw. Technol.*, vol. 24, pp. 3810–3815, 2006.

[91] B. Saleh and M. Teich, Fundamentals of Photonics. John Wiley & Sons Ltd., 1991.

[92] J.-M. Fedeli, E. Jordana, P. Lyan, J.-P. Colonna, P. Gautier, N. Daldosso, P. Pavesi, Y. Lebour, P. Pellegrino, B. Garrido, J. Blasco, F. Cuesta-Soto, and P. Sanchis, "Deep-UV Lithography Fabrication of Slot Waveguides and Sandwiched Waveguides for Nonlinear Applications," *Proc. of 4th Group IV Photonics Conference (GFP)*, pp. 222–224, 2007.

[93] K. Biswas and S. Kal, "Etch characteristics of KOH, TMAH and dual doped TMAH for bulk micromachining of silicon," *Microelectron. Journal*, vol. 37, p. 519525, 2006.

[94] H. Schröder, E. Obermeiery, and A. Steckenbornzk, "Effects of the etchmask properties on the anisotropy ratio in anisotropic etching of {100} silicon in aqueousKOH," *J. Micromech. Microeng.*, vol. 8, p. 99103, 1998.

[95] H. Schröder and E. Obermeier, "A new model for $Si_{\{100\}}$ convex corner undercutting in anisotropic KOH etching," *J. Micromech. Microeng.*, vol. 10, pp. 163–170, 2000.

[96] R. Nagarajan, C. Joyner, J. Schneider, R.P., J. Bostak, T. Butrie, A. Dentai, V. Dominic, P. Evans, M. Kato, M. Kauffman, D. Lambert, S. Mathis, A. Mathur, R. Miles, M. Mitchell, M. Missey, S. Murthy, A. Nilsson, F. Peters, S. Pennypacker, J. Pleumeekers, R. Salvatore, R. Schlenker, R. Taylor, H.-S. Tsai, M. Van Leeuwen, J. Webjorn, M. Ziari, D. Perkins, J. Singh, S. Grubb, M. Reffle, D. Mehuys, F. Kish, and D. Welch, "Large-scale photonic integrated circuits," *IEEE J. Sel. Topics in Quantum Electron.*, vol. 11, pp. 50–65, 2005.

[97] G. Maxwell, A. Poustie, C. Ford, M. Harlow, P. Townley, M. Nield, T. Lealman, S. Oliver, L. Rivers, and R. Waller, "Hybrid integration of monolithic semiconductor optical amplifier arrays using passive assembly," *IEEE Electronic Components and Technology Conference*, vol. 2, pp. 1349– 1352, 2005.

[98] I. Day, I. Evans, A. Knights, F. Hopper, S. Roberts, J. Johnston, S. Day, J. Luff, H. Tsang, and M. Asghari, "Tapered silicon waveguides for low insertion loss highly-efficient high-speed electronic variable optical attenuators," *Proc. Optical Fiber Communications Conference (OFC)*, vol. 1, pp. 249– 251, 2003.

[99] L. Zimmermann, H. Schrder, P. Dumon, W. Bogaerts, and T. Tekin, "ePIXpack - Advanced Smart Packaging Solutions for Silicon Photonics," *Proc. of 14th European Conference on Integrated Optics*, pp. 33–36, 2008.

[100] L. Zimmermann, H. Schröder, T. Tekin, W. Bogaerts, and P. Dumon, "g-Pack a generic tested package for Silicon photonics devices," *Proc. 5th IEEE International Conference Group IV Photonics, Sorrento (Italy)*, p. 371, 2008.

[101] P. De Dobbelaere, B. Analui, E. Balmater, D. Guckenberger, M. Harrison, R. Koumans, D. Kucharski, Y. Liang, G. Masini, A. Mekis, S. Mirsaidi, A. Narasimha, M. Peterson, T. Pinguet, D. Rines, V. Sadagopan, S. Sahni, T. Sleboda, Y. Wang, B. Welch, J. Witzens, J. Yao, S. Abdalla, S. Gloeckner, and G. Capellini, "Demonstration of First WDM CMOS Photonics

Transceiver with Monolithically Integrated Photo-Detectors," *Proc. 34th European Conference on Optical Communication (ECOC).*, pp. 1–2, 2008.

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