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Advancing Logic Circuits With Halide Perovskite Memristors for Next-Generation Digital Systems

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ABSTRACT

The potential of all-inorganic halide perovskite-based memristors as a solution to the limitations of traditional memory systems, particularly in the context of edge computing and next-generation digital architectures, is investigated. The rapid expansion of data-driven applications demands more efficient, secure, and scalable memory technologies, prompting this exploration of memristors for their unique resistance-switching properties. The research aims to address the challenges of data security and processing efficiency by integrating memristors into logic circuits, enabling both memory and logic operations within a single device. The study is structured around the experimental fabrication and characterization of $Cs_3Bi_2I_6Br_3$ perovskite memristors. A simple solution-processed spin coating method with antisolvent-assisted crystallization was employed to fabricate the memristor devices. The experimental characterization of memristors, including X-ray diffraction (XRD) analysis and electrical measurements, confirmed their structural integrity and memristive behavior, with distinct hysteresis loops indicative of non-volatile memory properties. To analyze the behavior of the memristors in electronic circuits, a Verilog-A mathematical model was developed, and simulations were conducted using the Cadence Virtuoso Electronic Design Automation (EDA) suite. The Verilog-A model demonstrates strong agreement with measured results and validates the device's hysteresis behavior. Key findings demonstrate that metal halide perovskite (MHP) memristors exhibit excellent switching characteristics, repeatability, and integration potential with complementary metal-oxide-semiconductor (CMOS) technology. These properties make them suitable for implementing various logic gates, such as IMPLY, AND, and OR gates, as well as more complex digital circuits like multiplexers and full adders. The results highlight the feasibility of using these memristors for in-memory computing, where both data storage and processing occur within the memory cells, significantly enhancing computing efficiency and security. The study concludes that MHP-based memristors offer a promising path toward more compact, energy-efficient, and secure computing architectures.

1 | Introduction

The rapid growth of the Internet of Things (IoT) has led to an explosion of data, making efficient edge computing essential. Edge computing processes data closer to its source, improving immediacy and security for applications like autonomous driving. These devices manage sensitive information, such as biometrics and financial data, making them prime targets for cyberattacks. To counter these threats, hardware cryptographic solutions are being developed, as software security alone is

insufficient. Traditional cryptographic methods rely on nonvolatile memory to store secret keys, but these are difficult to keep secure over time. Next-generation memory devices, such as phase-change memory (PCM), magnetic random-access memory (MRAM), and resistive switching memory (RSM), offer advantages like nonvolatility and fast operation.

RSM is a type of nonvolatile memory that stores data by changing the resistance across a dielectric solid-state material, typically using a metal-insulator-metal structure [1]. RSM boasts several advantages, such as easy fabrication, excellent scalability, fast operation speed, long data retention, and compatibility with existing complementary metal-oxide-semiconductor (CMOS) technology [2]. Various materials, including oxides, organics, and biomaterials, have been evaluated for use in RSM devices [3, 4]. A new approach within RSM involves using memristors, which are resistive switching devices that not only regulate the flow of electrical current but also remember the amount of charge that has passed through them. Memristors enhance RSM by providing faster switching speeds, lower power consumption, and higher data retention, making them a promising technology for next-generation memory applications. Consequently, RSM offers a competitive solution for future digital memory [5].

A memristor is a two-contact device that can change its resistance based on applied voltage stimuli. This unique ability makes it useful for new kinds of computing, such as storing information in a manner different from traditional methods. Unlike traditional memory systems, where data is stored in fixed, predictable locations, a memristor dynamically adjusts its resistance. This adaptability introduces an additional layer of security, as the changing resistance makes it more challenging for hackers to pinpoint and access sensitive information. It was first imagined by a scientist named Chua in the 1970s, and in 2008, a practical version was made by HP Labs using a thin film of titanium oxide. This device can do both logic and memory tasks, opening up exciting possibilities for the future of computers [6, 7].

Metal halide perovskite (MHP) materials, with the typical structure comprising ABX_3 (A = monovalent organic/inorganic cation, B = Central metal cation, X = halide anion), have emerged as promising candidates for RSM devices. These materials have been extensively used in optoelectronic devices like solar cells and photodetectors due to their exceptional properties, including high charge carrier mobility, tunable bandgap, and long diffusion length. MHP materials exhibit hysteresis in their current–voltage (*I*–*V*) characteristics, which is advantageous for RSM devices. Additionally, their fast ion migration, low-cost processing, and tunable band gap make them ideal for resistive switching. MHPs have been investigated for their potential use in memristors, where their mixed electronic-ionic conduction behavior offers opportunities for energy-efficient optoelectronic memristors [8, 9]. Recent research has demonstrated that encapsulating MHP-based RSM devices improves their stability, making them suitable for practical memory applications [10, 11]. These materials exhibit strong coupling of photonic, electronic, and ionic processes, enabling multilevel biomimetic behavior suitable for in-sensor computing applications. Overall, MHP materials hold significant promise for the future of advanced multifunctional memristors and in-sensor computing [12]. The environmental stability of MHPs is a critical consideration for their practical application in electronic devices. Recent studies have demonstrated significant progress in improving the stability of perovskite-based devices through encapsulation techniques [13, 14], compositional engineering [15, 16], and interface modifications [17]. For instance, encapsulation with hydrophobic layers has been shown to protect perovskite materials from moisture and oxygen, while compositional engineering, such as the incorporation of cesium or formamidinium, has enhanced thermal and environmental stability. Additionally, interface modifications, including the use of passivation layers, have been effective in reducing defect densities and improving device longevity.

Using memristor-based MHP for logic applications in computing is an increasing need. These materials have special properties, allowing them to switch between different conductivity states quickly from high resistance state (HRS) to low resistance state (LRS). This makes them perfect for tasks like making decisions and processing information fast. Plus, they're affordable to make and can have adjustable characteristics such as crystal structures and bandgap, related to the resistive switching properties, making them even better for logic tasks. By tapping into these unique features of MHP-based memristors, future computer systems could become much more efficient and powerful, opening up exciting new possibilities for advanced logic operations in technology.

In recent years, several memristive logic design families have emerged, each with unique characteristics and applications [18, 19]. Notable among these are Memristor Aided Logic (MAGIC) and Material Implication (IMPLY), both of which enable logic computations within memristive memory systems to address the memory wall problem. MAGIC relies solely on memristors for creating various logic gates, while IMPLY uses two memristors and one resistor for the material implication operation. These methods allow for efficient logic gate mapping to the crossbar architecture, facilitating in-memory computing [20, 21].

Another significant design style is Memristor-Ratioed Logic (MRL), a hybrid of memristors and CMOS technology aimed at implementing conventional combinational logic circuits, the building blocks of digital systems. MRL seeks to replace as many transistors with nano-scale memristors as possible while maintaining the functionality of traditional digital architectures. Unlike other memristive logic styles, MRL matches conventional CMOS in using voltage as the state variable, making it highly suitable for integration into existing CMOS designs. This integration can effectively exploit the density and scalability of memristive devices through the crossbar structure, which arranges memristors above the CMOS layer [22–24].

Additionally, recent advancements have proposed new synthesis approaches for mapping logic gates, such as NOR and NOT, directly onto memristor crossbars. For instance, a transpose crossbar architecture allows NOR gates to be mapped to columns as well as rows, enabling more efficient in-memory computing. This approach simplifies gate mapping and

enhances the potential for scalable, high-performance computing architectures using memristors [25].

This paper demonstrates the potential of MHP-based memristors for circuit logic through a combination of experimental fabrication, characterization, and computer simulations. In the initial phase, we detail the fabrication process of $Cs_3Bi_2I_6Br_3$ perovskite memristors, including the solution-processed spin coating method with antisolvent-assisted crystallization, and the structural verification using X-ray diffraction (XRD) analysis. The electrical characterization, conducted under dark conditions using a KEYSIGHT Semiconductor Analyzer, confirms the memristor's switching behavior and hysteresis properties, which are critical for nonvolatile memory applications. In the next phase, we describe the mathematical model governing memristor behavior, implemented in Verilog-A for circuit simulations using Cadence's Spectre simulator. This model accurately replicates the experimental *I–V* characteristics, including the nonlinear resistance and voltage-dependent hysteresis, providing insights into the memristor's switching dynamics and memory effects. In the final phase, we compare the hysteresis curves obtained from both the fabricated devices and the simulated model, validating the accuracy of the proposed behavioral model. Furthermore, we demonstrate the implementation of basic logic gates, such as IMPLY, AND, and OR, using memristors, where logic operations and data storage are integrated within the same device. Additionally, a performance comparison between NMOS-based and memristor-based logic gates is conducted, highlighting the advantages of memristors in terms of energy efficiency and integration density for in-memory computing applications. This paper is organized as follows: Section 2 provides the experimental methods, Section 3 presents the mathematical model, Section 4 discusses the experimental and simulation results, and Section 5 concludes the paper.

2 | Experimental

2.1 | Device Fabrication

The MHP-memristor devices were composed of layers of Indium tin oxide (ITO) glass, MHP($Cs_3Bi_2I_6Br_3$), and Ag metal electrode. First, we washed the ITO glass substrates by sonication in detergent with deionized water (DIW), acetone, and isopropyl alcohol (IPA) each for 15 min, followed by an airgun-blow drying process.

The precursor solution of MHP ($Cs_3Bi_2I_6Br_3$) was prepared by mixing cesium bromide (CsBr, 99.999% trace metals basis, Sigma-Aldrich) and bismuth (III) iodide (BiI_3, 99% trace metals basis, Sigma-Aldrich) with molar ratio of 3:2 in mixed N,N-dimethylformamide (DMF, 99.8%, VWR Chemicals) and dimethyl sulfoxide (DMSO, 99.7%, Sigma-Aldrich) solvent. The fully dissolved precursor solution (orange-red color) was filtered using a syringe filter of PTFE-H (pore size 0.22 μm) in Figure S1A. Before the deposition of the MHP precursor solution onto the cleaned ITO substrates, the substrates were treated with UV-ozone (UVO). The MHP precursor solution was spin-coated onto the UVO-treated ITO substrates at 1000 r/min for 10 s and 5000 r/min for 30 s. At 10 s after the start of the second spin-coating step, diethyl ether (99.8%, VWR Chemicals) was dripped onto the wet film, and the as-spun film was annealed at 100°C for 15 min on a hot plate. The MHP film stacked on the ITO glass substrate showed an orange-red color in Figure S1B. All the precursor preparation and fabrication processes were done in an Ar-filled glove box. Finally, we deposited 100 nm of silver (Ag) top contacts onto MHP-coated ITO substrates by thermal evaporation using a dot-shaped shadow mask.

2.2 | Device Structure and Characterization

The MHP-memristor schematic device configuration used in this study is shown in Figure 1A, and the real device picture is shown in Figure 1B. Electrical measurements using the fabricated memristor are carried out with the aid of the selected electrical measuring units. The fabricated memristor possesses a square shape with the dimensions of 2.0 cm × 1.5 cm cut from an ITO/glass substrate. The silver electrodes on the surface in the form of a dot-shaped with a diameter of 200 μm are used for the terminal contacts of the memristor, as shown in Figure 1B. To characterize the electrical behaviors, the memristor terminals are contacted with needles in the probe station, used for the measuring setup, which is shown in Figure 1C. Dark conditions were maintained during the testing. A KEYSIGHT Semiconductor Analyzer Source (B1500A series), connected to the needles and probe station, was used to provide the electrical stimulus and measure simultaneously. The XRD patterns of $Cs_3Bi_2I_6Br_3$ film on an ITO/glass substrate (Figure S1B) were obtained with a CUBIX XRD DY0822 X-ray diffractometer (Cu Kα radiation, wavelength = 1.54056°) from PANalytical Ltd. The scan was performed in the 2θ range from 10° to 70° with 0.02°, as shown in Figure 1D. The XRD patterns were well-matched with the previous reports of a trigonal space group $P\bar{3}m1$ [26–29].

To evaluate the thickness and uniformity of the spin-coated $Cs_3Bi_2I_6Br_3$ perovskite layer, we performed both 3D optical profilometry and cross-sectional SEM imaging. The results (Figure 2) confirm a uniform film with an average thickness of approximately 150 nm across multiple batches. This uniformity is further supported by consistent switching behavior observed across 125 memristor cells distributed across a 1.5 cm × 2.0 cm substrate, indicating high reproducibility and spatial uniformity of the active layer.

3 | Modeling

3.1 | MHP Memristor Model

Resistive switching systems have been studied for a long time, and scientists are still working to explore new possibilities in this technology [30]. These systems have been widely recognized as memristors in recent years, based on Chua's theory [31]. A memristor is a special type of system that has memory and changes based on one or more state variables, referred to as x_i [32]. These variables are essential for predicting the future behavior of the system based on its current state and inputs [33]. To describe the typical behavior of memristors, we define a

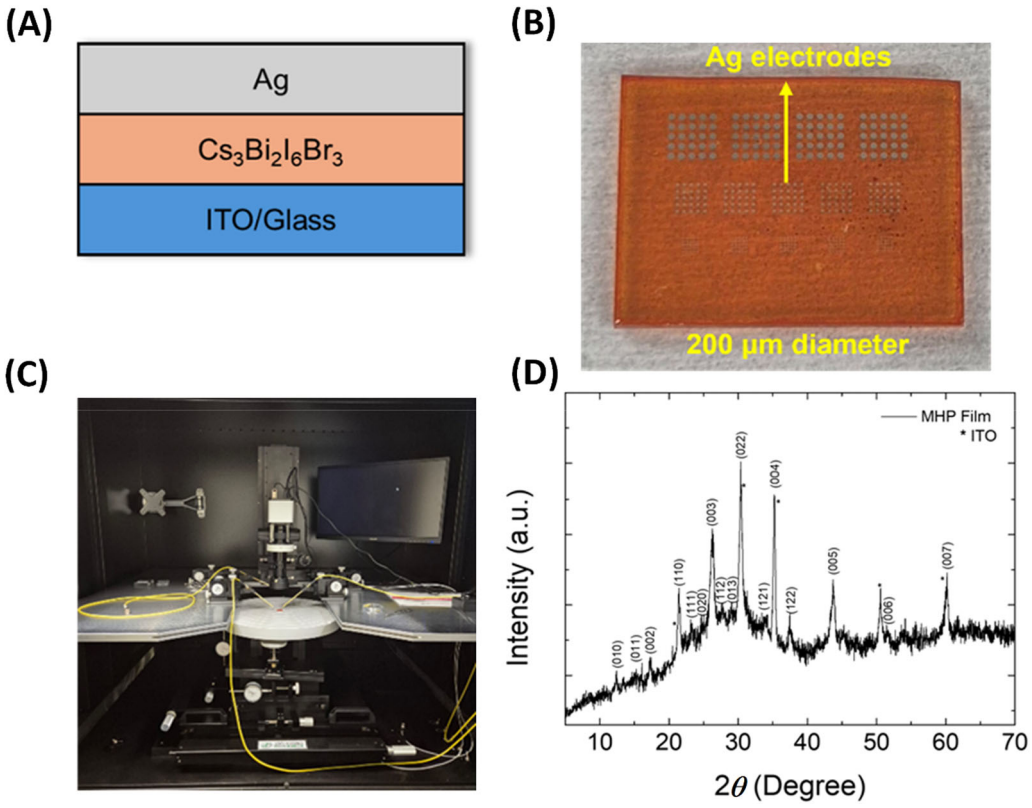

FIGURE 1 | (A) Schematic diagram of MHP memristor, (B) top view of MHP memristor, (C) measuring setup used in this study, and (D) XRD patterns of MHP Film deposited onto ITO/glass substrate.

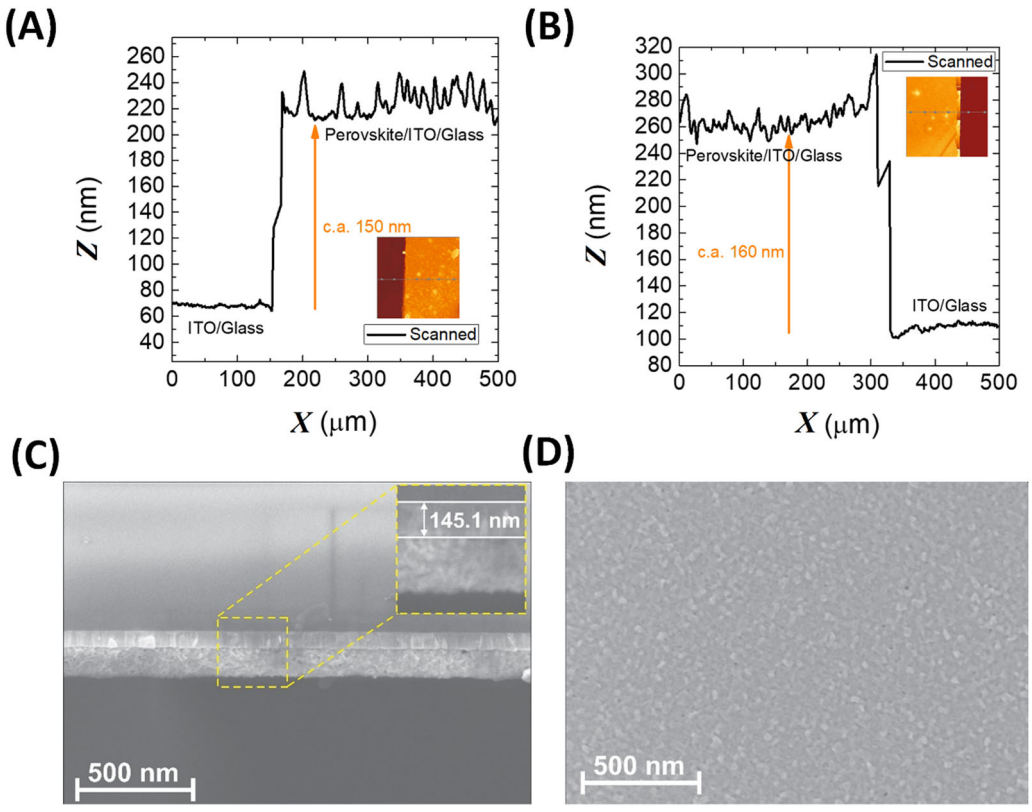

FIGURE 2 | (A, B) Film thickness measurements of spin-coated $Cs_3Bi_2I_6Br_3$ perovskite layers from two separate batches using 3D optical profilometry, showing an average thickness of ~150 ± 10 nm. (C) Cross-sectional SEM image of the MHP layer on ITO/glass substrate, showing a thickness of ~145.1 nm. (D) Surface SEM image demonstrating uniform morphology across the device area.

general model for memristive devices. We introduce Equation (1) to create the standard framework [32, 34] for a voltage-controlled memristor as shown below:

$$I_{\text{tot}} = C_{\text{m}}\frac{\mathrm{d}V}{\mathrm{d}t} + G(V, x_i) \tag{1}$$

$$\tau_{\text{k}}\frac{\mathrm{d}x_i}{\mathrm{d}t} = H(V, x_i) \tag{2}$$

In this model, τ_{k}, $G(V, x_i)$, and $H(V, x_i)$ represent the kinetic time constant, the general conduction function, and the general adaptation function, respectively. C_{m} is an intrinsically constant capacitance that generates a fast capacitive current within the device. Equations (1) and (2) show that the device's current depends not only on the applied voltage but also on its internal state and its dynamics. Equation (2) further clarifies that changes in this internal state are influenced by both the current state and the external stimulus. To describe an MHP memristor, we define a specific conduction function in which the conductance varies between a minimum value g_{L} and a maximum value g_{H}, as determined by a state variable x that ranges from 0 to 1 [35, 36]. Therefore, the current is expressed as follows:

$$I_{\text{tot}} = C_{\text{m}}\frac{\mathrm{d}u}{\mathrm{d}t} + [g_{\text{L}} + (g_{\text{H}} - g_{\text{L}})x]u \tag{3}$$

Since we have already changed the notation from V, representing the externally applied experimental voltage, to u, denoting the internal voltage of the device, we thereby disregard any potential small series resistance that may be present. In this way, the change in the system conductance, and consequently the electrical behavior of the memristor, is entirely determined by the state variable x. When x reaches its maximum value ($x = 1$), the system attains its highest conductance g_{H}, whereas when x is at its minimum value ($x = 0$), the device operates at its lowest conductance g_{L}. As previously mentioned, this variable varies as a function of the applied voltage and also exhibits an intrinsic voltage-dependent dynamic behavior. The stationary form of this variable as a function of voltage can be described as follows [35, 36]:

$$x_{\text{ss}}(u) = \frac{1}{1 + \mathrm{e}^{-\frac{u - V_{\text{th}}}{V_{\text{m}}}}} \tag{4}$$

It is a typical sigmoidal function with an onset parameter V_{th} and steepness V_{m}.

Thus, the system will not only transition between these two conductance states but will also be capable of achieving a continuum of intermediate states, which is crucial for synaptic operations. To complete the model, it is required to establish the time evolution equation that defines the dynamic response of x to the applied voltage. From Equation (2), we write [35, 36]:

$$\tau_x(u)\frac{\mathrm{d}x}{\mathrm{d}t} = x_{\text{ss}}(u) - x \tag{5}$$

where the dynamic behavior of the state variable in our device, relative to the steady-state value it should attain, is entirely determined by a voltage-dependent relaxation time $\tau_x(u)$. In MHP memristors, significant variations in relaxation times can occur, allowing the device's volatility degree to be adjusted [37]. To describe this behavior, we make certain modifications to the general model developed by Bisquert et al. [35], obtaining the following expression:

$$\tau_{\text{k}}(u) = \frac{\tau_{\max} + \tau_{\min_{\text{OFF}}}\mathrm{e}^{-\frac{u - V_{\text{OFF}}}{V_-}}}{1 + \mathrm{e}^{-\frac{u - V_{\text{OFF}}}{V_-}}} - \frac{\tau_{\max} - \tau_{\min_{\text{ON}}}}{1 + \mathrm{e}^{-\frac{u - V_{\text{ON}}}{V_+}}} \tag{6}$$

The voltage dependence of $\tau_x(u)$ is affected by several key factors: the maximum ($\tau_{\max}$) and minimum ($\tau_{\min_{\text{OFF}}}$ and $\tau_{\min_{\text{ON}}}$) kinetic time constants, the threshold RESET voltage (V_{OFF}) along with its corresponding ideality factor (V_-), and the threshold SET voltage (V_{ON}) with its associated ideality factor (V_+). The influence of these parameters on the switching behavior is detailed in reference [35], where we have modified it to independently describe the minimum time required for the rupture and formation of the high-conductance state. Specifically, we have replaced the $\tau_{\min}$ factor from the previous model with $\tau_{\min_{\text{OFF}}}$ and $\tau_{\min_{\text{ON}}}$ on either side of the maximum response time.

3.2 | Definition of an MHP Memtistor Relationship in Verilog-A

Verilog-A, a subset of Verilog-AMS, is a hardware description language designed for users of SPICE class simulators to create models for simulations. Unlike regular programming languages, Verilog-A is specifically made for describing analog hardware, while Verilog mainly describes digital hardware. As an industry-standard for modeling analog circuits and part of Verilog-AMS, Verilog-A helps represent complex MEMS designs. It provides a high-level framework using modules to describe the structure and behavior of analog systems across electrical, mechanical, fluid dynamic, and thermodynamic domains [38].

Here, we aim to implement Equations (3)–(6) in Verilog-A code. These equations describe a memristor device, a key electronic component whose resistance changes based on the history of applied voltages. They capture the behavior of the memristor within an analog circuit environment, detailing the currents through components, such as capacitors, resistors, and the memristor itself, as well as their relationships to voltages and conductance. Additionally, the equations model the evolution of internal states within the memristor, represented by variables, such as "x_{ss}" and "τ," which influence its behavior over time.

Since the code includes two derivative definitions, we define two virtual nodes. The current through a memristor depends on its conductance, the voltage across it, and the voltage across an internal node. In these equations, the state variable (x_{ss}) of the memristor is based on a sigmoidal function, representing the internal state of the memristor, which influences its behavior. The Memristor State Transition Equation (τ) describes how the memristor transitions between different states based on its voltage.

After explaining the theoretical framework and illustrating the model characteristics in the Cadence software, we use our biological-inspired model to replicate the results obtained from the MHP-based memristor described in reference [10]. A two-terminal element was created using a Verilog-A model, which serves as the foundation for capturing the basic features and functions of a memristor. The main goal of this approach is to understand and analyze the complex behavior exhibited by the memristor in the circuit. By making the memristor the central element, various operational scenarios are applied to thoroughly examine its behavior.

4 | Result and Discussion

4.1 | Experimental *I–V* Characterization

In the characterization of the *I–V* curve for the ITO/$Cs_3Bi_2I_6Br_3$/Ag device, the voltage was applied to the top Ag electrode with a 200 μm diameter while the bottom ITO electrode was grounded. A direct current (DC) voltage sweep was administered in the sequence 0 V → +1.0 V → 0 V → −1.5 V → 0 V at a compliance current of 1 mA in Figure 3. The *I–V* characterizations were conducted using a semiconductor analyzer (B1500A, KEYSIGHT), utilizing a two-electrode configuration. Measurements were taken under dark and ambient conditions at a sweep rate of 100 V/s with a voltage step size of 0.01 V. The MHP memristor device shows the typical bipolar resistive switching behavior with the forming step at the first sweep for stable initialization of the resistive switching. The resistance state transitions from the high-resistance state (HRS) to the low-resistance state (LRS) in the positive voltage region, representing the SET process, while the opposite transition corresponds to the RESET process. After the initial forming step, the MHP memristor underwent repeated resistive switching, as shown in Figure 3A. To evaluate the reproducibility of MHP-based memristors, we analyzed random *I–V* sweeps from 15 different devices fabricated in separate batches using the same method (Figure 3B). The statistics of HRS, LRS, and ON/OFF ratio on the device-to-device reproducibility test are presented as box plots in Figure S2A,B, where resistances were measured at +0.1 V. The average HRS, LRS, and ON/OFF ratios were 5.44×10^5, 2.72×10^2, and 2.56×10^3 Ω at the forming steps and 3.59×10^3, 2.21×10^2, and 2.02×10^1 Ω at the switching steps.

Additionally, cell-to-cell reproducibility tests were conducted to further examine the consistency of the memristor's performance, as shown in Figure S2C,D. The statistics of the cell-to-cell reproducibility test were obtained by measuring 30 different cells within a single device, using the same reading voltage of +0.1 V. The statistical average HRS, LRS, and ON/OFF ratios were each 4.19×10^5, 3.55×10^2, and 1.98×10^3 Ω at the forming steps and 4.07×10^3, 2.16×10^2, and 1.98×10^1 Ω at the switching steps. The statistical analysis of randomly selected *I–V* sweeps from both device-to-device and cell-to-cell reproducibility tests confirmed the reliable performance of the MHP-based memristor. Furthermore, to assess device stability, 40 consecutive *I–V* curves were measured, as shown in Figure S3. Even after 4 weeks of air exposure (room temperature and ambient conditions), a slight increase in current was observed due to degradation. However, the bipolar resistive switching properties remained intact, despite the absence of encapsulation for the MHP layer.

Although halide vacancy migration is often associated with degradation in perovskite optoelectronic devices, in MHP memristors, it serves a functional and controllable role in enabling resistive switching. Under an applied electric field, halide vacancies migrate locally, facilitating the formation and rupture of conductive filaments that define the high- and low-resistance states. This process is experimentally confined using a compliance current, which prevents excessive defect accumulation during electrical cycling. To validate the stability and non-volatile behavior of this mechanism, we conducted a series of experimental tests summarized in Figure 4. The log-scale *I–V* hysteresis curve (Figure 4A) demonstrates bipolar switching, where the device maintains its LRS even after the voltage sweep is reversed, unless a RESET voltage is applied, highlighting its

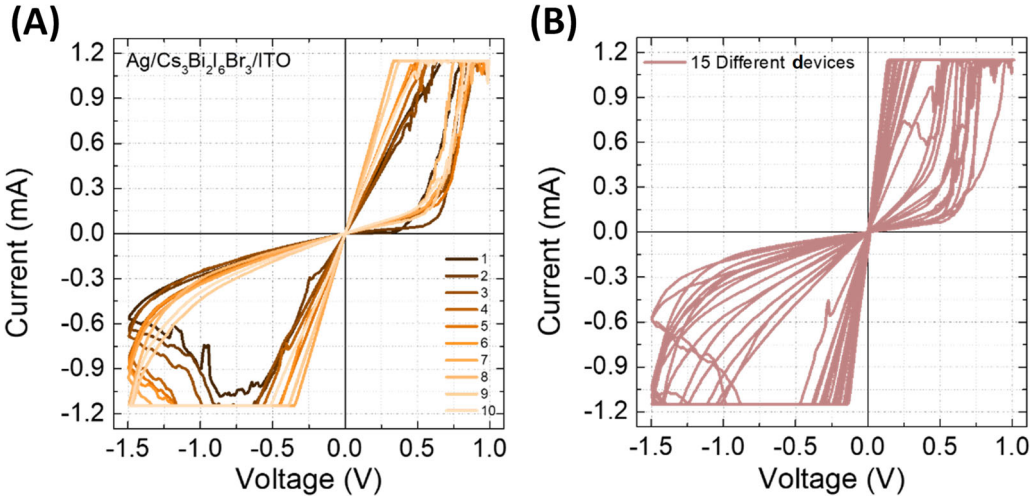

FIGURE 3 | Characterization of the *I–V* curves for the Ag/$Cs_3Bi_2I_6Br_3$/ITO device, which is applied with +1.0 V for SET processes and −1.5 V for RESET processes at a compliance current of 1 mA. (A) 10 repetitive cycles in one cell and (B) Random cycles collected from 15 devices in different batches.

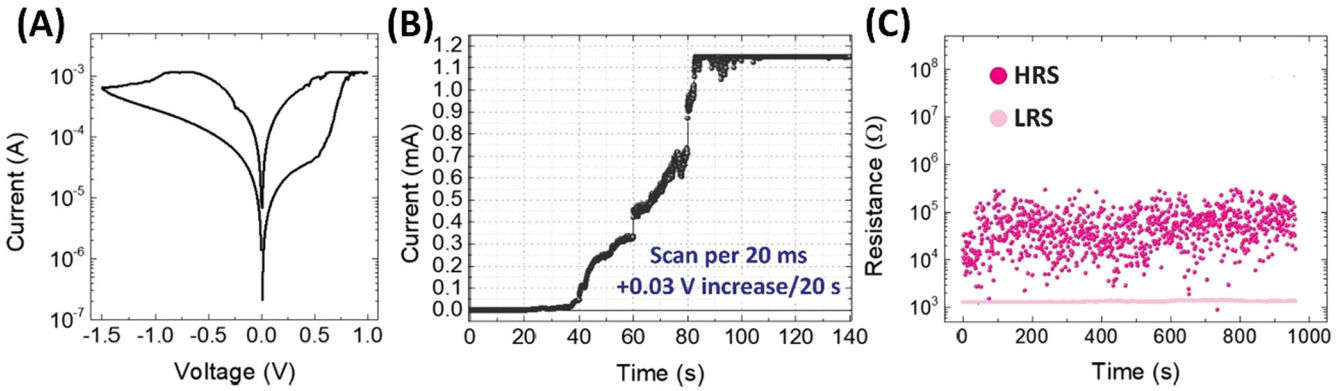

FIGURE 4 | (A) Log-scale *I–V* hysteresis curve of the MHP memristor showing stable bipolar switching behavior. (B) Time-resolved current evolution during retention testing, demonstrating stable LRS retention under periodic read pulses (+0.03 V every 20 s, scan rate: 0.02 s). (C) Long-term retention performance measured by applying +1.0 V (SET) and −1.5 V (RESET) pulses and reading at +0.1 V, confirming the nonvolatile stability of both resistance states.

intrinsic nonvolatility. The time-resolved retention test (Figure 4B) further confirms this by showing stable current under repeated +0.03 V read pulses every 20 s. In addition, long-term retention measurements (Figure 4C), performed by applying +1.0 V (SET) and −1.5 V (RESET) pulses and reading at +0.1 V, show consistent and distinguishable resistance levels over time for both states. Collectively, these results provide strong experimental evidence that the device reliably preserves its resistance state, demonstrating robust nonvolatile memory performance and operational stability suitable for memory applications.

The methodology ensured precise control and measurement of the electrical properties, facilitating an accurate analysis of the device's performance under the specified conditions. Figure 5A,C,E shows the applied voltage and measured current of the devices under continuous current sweeping at scan rates of 500, 100, and 50 V/s, between −1.5 and +1.0 V, in the dark environments. The measured current vs. applied voltage under the same conditions is presented in Figure 4B,D,F.

Also, Figure S4 shows the different *I–V* curves experimentally (Figure S4A) and through simulations (Figure S4B) at varying scan rates from 10 to 500 V/s. In practice, the device shows a cutoff by using a compliance current to prevent deterioration caused by excessive current in Figure S4A. In addition, the gradient change trend with different scan rates is consistent with both the experimental *I–V* curves and the simulated models. Typically, the curve shows a gradual increase in conductivity with rising voltage, indicating the memristor's transition from HRS to LRS. This transition is reversible, as evidenced by the loop-shaped hysteresis, where the current response depends on the previous voltage history. Hysteresis is typically observed in the *I–V* curve for this configuration, with a distinct separation between the forward and backward scans, even when measurements are conducted in the dark to exclude the photo-responsive possibility of MHPs. *I–V* hysteresis was also scanned under illumination using a white light source equipped on the probe station for contacting the cells, as shown in Figure S5. Under illumination, the hysteresis *I–V* curve of MHP-based memristors can change due to the interaction of photons with the perovskite material. Photon absorption leads to the generation of electron-hole pairs within the MHP layer, significantly altering its electrical properties. This phenomenon results in a reduction in resistance at lower applied voltages compared to the dark condition, indicating an increase in conductivity. The extent of this change is influenced by factors such as the intensity, wavelength, and duration of light exposure, as well as the specific composition and morphology of the MHP material [39]. Moreover, the shape and size of the hysteresis loop provide critical information about the memristor's stability and performance under different lighting conditions. Variations in the loop's area or asymmetry indicate the device's sensitivity to light, which is essential for applications such as optoelectronic memories and neuromorphic computing [40, 41].

The hysteresis behavior is complex, showing significant variation with different scan rates. This type of hysteresis is closely linked to the presence of both capacitive and inductive currents [42]. The concept of a chemical inductor refers to a class of dynamic phenomena typically driven by chemical reactions that produce a formal inductive response in impedance and transients, independent of electromagnetic effects. The inductance is incorporated into the middle element of Figure S6, represented by the *x* function in our memristor model. This *x* function plays a key role in defining the system's behavior, linking the inductance to the memristor's internal state and conduction mechanism.

In halide perovskites, this chemical inductance is associated with slow ion-controlled electronic phenomena occurring in the active layer of the device. In MHP memristors, migrating ions that reach the external contacts generate a capacitive current as the contacts compensate for their charge to maintain electroneutrality, essentially acting like a capacitor [43]. In these materials, the capacitance also varies with external stimulus intensity, showing an increase in electrically induced capacitance. Various species, such as halide vacancies, cations, and electrochemically active metal ions, migrate at different rates under an applied external voltage [9, 44]. Halide vacancies are the fastest migrating species in MHPs. When a positive voltage is applied at the silver electrode, halide vacancies move towards the electrode, leading to a surplus concentration of halide anions from the electrode/MHP interface. Conversely, the same

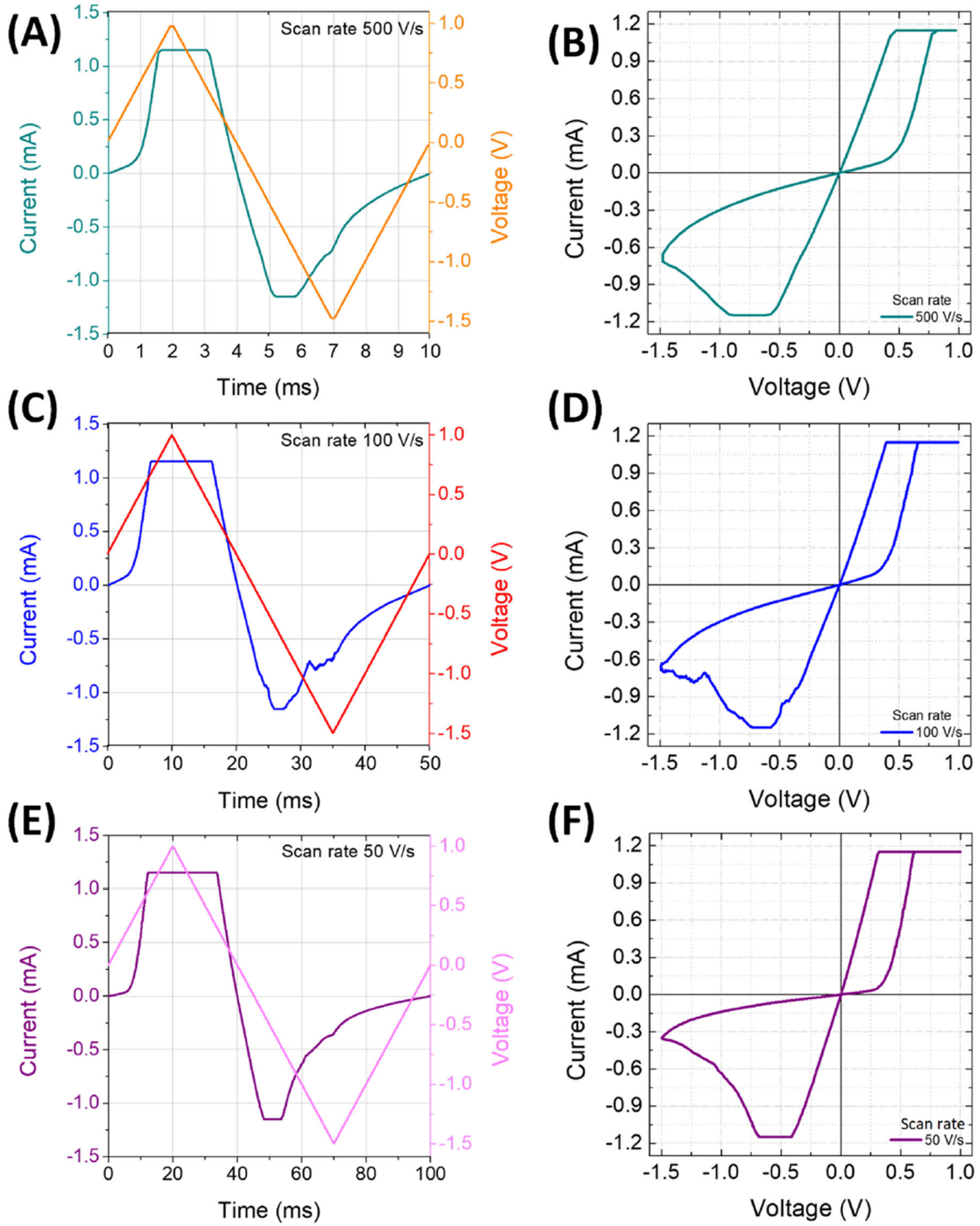

FIGURE 5 | Characterization of the *I–V* curve for the Ag/$Cs_3Bi_2I_6Br_3$/ITO device with different scan rates. Applied voltage and measured current under continuous current sweeping at a scanning rate of (A) 500, (C) 100, and (E) 50 V/s between −1.5 and +1.0 V in the dark conditions. (B), (D), and (F) Measured current vs. applied voltage under the same conditions as (A), (C), and (E), each.

process happens in reverse when a positive voltage is applied at the opposite contact [45, 46].

4.2 | Simulation Results

According to Equations (3)–(6), various parameters are used to describe the behavior of the memristor. Table 1 presents the definitions, values, and units of these parameters. By examining the shape and characteristics of the *I–V* curve at different scan rates and various maximum applied voltages obtained from experimental measurements, key parameters can be extracted. We choose parameters from the model's characteristic functions, as listed in Table 1, to simulate electrical measurements that replicate the experimental trends observed in the electrical measurement presented in Figure S6 of MHP memristors.

TABLE 1 | Definition, unit, and value of parameters describing the MHP memristor.

Parameters	Definition	Unit	Value
C_m	Internal device capacitance	(nF)	0.20
g_L	Low conductance	(mS)	0.15
g_H	High conductance	(mS)	6.00
V_{th}	Threshold voltage	(V)	0.10
V_m	Voltage modulation factor	(V)	0.06
τ_{max}	Maximum state transition time	(s)	1500
V_{OFF}	Voltage offset for state transition	(V)	−0.20
V_-	Voltage offset factor for state transition	(V)	0.03
$\tau_{min_{OFF}}$	Minimum offset state transition time	(ms)	5.00
V_{ON}	Voltage onset for state transition	(V)	0.16
V_+	Voltage onset factor for state transition	(V)	0.0
$\tau_{min_{ON}}$	Minimum onset state transition time	(ms)	1.10

4.2.1 | *I–V* Characterization

After establishing the theoretical framework and demonstrating the model's characteristics, we apply our biologically inspired model to replicate the experimental results obtained from the MHP-based memristor discussed in the previous section.

For this purpose, we will plot the same experimental responses obtained in the previous section but using the parameters derived from the model. Initially, we simulated the transient response of the output current alongside the input voltage. Figure 6A,C,E confirms that the memristor behaves as a nonlinear resistor as designed. Additionally, these figures reveal that the resistance of the memristor varies depending on the range, polarity, and duration of the applied voltage, as discussed in the previous section for the experimental results and replicating them. To further analyze the behavior of the MHP-based memristor, we also generated a hysteresis plot by plotting current vs. voltage. This plot, shown in Figure 6B,D,F highlights the memristor's distinctive hysteresis characteristic, again replicating the previous experimental results, which is a hallmark of memristive behavior.

To further validate the model's applicability, the supporting information includes Figure S4B, which compares simulated results with experimental data for the device at different scan rates. The model successfully reproduces the experimental hysteresis behavior across varying voltage sweep rates, including the onset shifts and current decay trends. Minor discrepancies between simulation and experiment may result from compliance with current constraints and the inherent simplifications in the state-variable dynamics.

Additionally, Figure S7 presents the steady-state system state variable x_{ss} and the system response time τ_x, as defined by Equations (4) and (6), respectively, plotted against voltage. In all simulations, the same parameter values listed in Table 1 were consistently used.

The origin of the hysteresis can be attributed to several factors: (a) defect density within the perovskite layer or at its interfaces, (b) interstitial ion migration, and (c) dipole polarization induced by the ferroelectric properties of MHP materials [47]. The hysteresis loop signifies the presence of memory effects in the device, where the current response depends not only on the applied voltage but also on its history. The shape and area of the loop offer insights into the switching dynamics and resistive states of the memristor, highlighting its potential for nonvolatile memory applications. Furthermore, the observed hysteresis behavior reinforces the memristor's suitability for neuromorphic computing and adaptive electronics.

To investigate device scalability, we fabricated additional MHP memristors with top electrode diameters of 50 and 100 μm, in addition to the 200 μm reference devices. As shown in Figure S8, all sizes exhibited stable bipolar switching behavior with similar ON/OFF ratios, demonstrating the feasibility of scaling down the device dimensions toward CMOS-compatible geometries.

4.2.2 | Effect of Scan Rate and Voltage Amplitude

Regarding the adequacy of the experimental results to the model and simulations, we observe that, while not exactly identical, they follow the same trend, exhibiting two distinct conductance states and transitioning between them with a relaxation time and a memory-dependent variable. When the variable x changes rapidly, it lacks sufficient time to adapt to the expected conductance states due to the relaxation time. Consequently, the maximum and minimum current values are constrained, reducing the hysteresis loop area in both height directions. Conversely, when the variable evolves more slowly, it has ample time to fully transition to the appropriate conductance state, thereby increasing the maximum and minimum heights of the hysteresis loop.

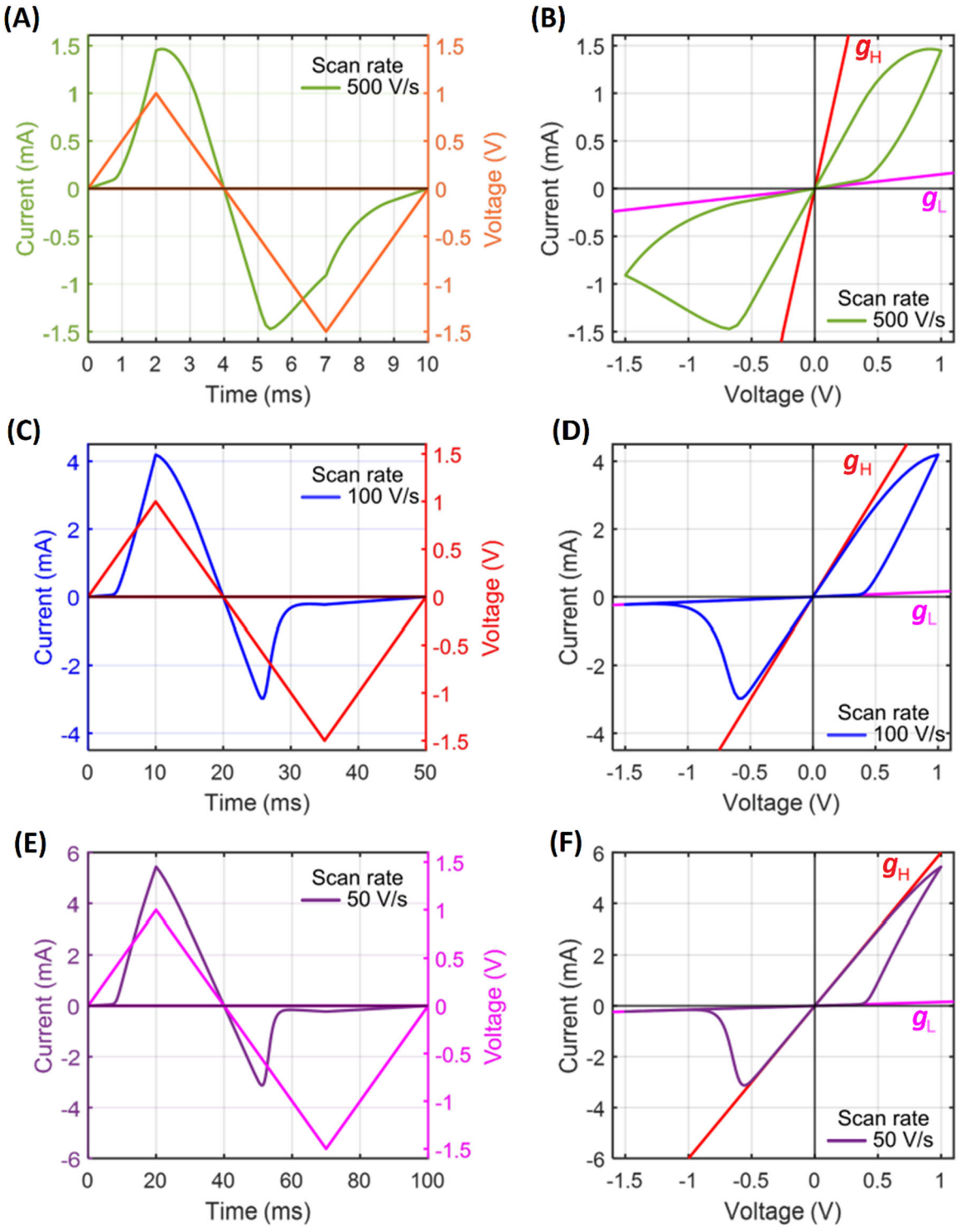

FIGURE 6 | Simulation of the model reproducing the response of an MHP-based memristor under different voltage scan rates. (A, B) 500 V/s; (C, D) 100 V/s; (E, F) 50 V/s. (A, C, E) Output current characteristic curve compared with the input voltage. (B, D, F) Hysteresis plot of current vs. voltage.

Thus, the scan rate, or the rate at which the voltage is swept, significantly impacts the hysteresis loop of a perovskite memristor. At lower scan rates, the ions and defects within the perovskite layer have sufficient time to respond to the changing voltage, resulting in a higher but narrower hysteresis loop, indicating a strong memory effect [48], but lower synaptic learning capacity. The slow scan rate allows for better alignment of dipoles and migration of ions, contributing to a more stable and larger hysteresis high. As the scan rate increases, the ions and dipoles have less time to align or migrate fully in response to the voltage changes, making the hysteresis loop wider and smaller and the memory effect less pronounced. At high scan rates, the voltage changes too rapidly for the ions and dipoles to respond effectively, leading to a wider and smaller hysteresis loop, indicating a weaker memory effect [45, 49], but greater synaptic learning capacity. Thus, the scan rate can be used to tune the hysteresis properties of

the perovskite memristor, which is important for applications requiring specific memory, switching characteristics, and synaptic properties [10, 50].

Figure S4 illustrates the scan rate-dependent characteristics of the *I–V* curves, providing insight into the inductive response of the MHP-based memristor. As the scan rate increases, the forward scan current decreases, and the hysteresis width narrows. This behavior is attributed to changes in memristor conductance, where higher frequencies limit ion migration and charge redistribution. Understanding and controlling both the scan rate and input voltage frequency enables the optimization of MHP-based memristors for applications requiring precise memory retention and switching properties.

In the following analysis, we examined the impact of varying the input voltage range on current characteristics. Figure S9 presents the *I–V* curves under different voltage ranges at a constant scan speed of 100 V/s, spanning +0.5 to +2.0 V in the positive region and −0.75 to −3.0 V in the negative region, shown on a linear scale. The applied voltage amplitude significantly influences the hysteresis loop, affecting switching thresholds and saturation currents, which reflect the nonlinear and adaptive nature of MHP-based memristors. This voltage-dependent modulation highlights the sensitivity of these devices to external electrical stimuli, impacting their stability, switching dynamics, and potential applications in neuromorphic computing [51, 52].

4.2.3 | IMPLY Gate Implementation

IMPLY logic, also known as implication or conditional logic, is a fundamental concept in mathematics and computer science. It involves a compound proposition with an antecedent ("if" part) and a consequent ("then" part), where the IMPLY operator dictates that if the antecedent is true, the consequent must also be true. If the antecedent is false, the truth value of the compound proposition is indeterminate. This logic is crucial for decision-making and problem-solving in digital circuit design, programming, and artificial intelligence [53]. The truth table and circuit symbol of the IMPLY gate are shown in Figure S10.

IMPLY logic implemented with memristors is an innovative method that uses the unique properties of memristive devices to perform logical operations. Memristors are electronic components whose resistance changes based on the history of applied electric fields, effectively remembering their previous states. This ability makes them suitable for mimicking synaptic behavior in neuromorphic computing and for implementing various types of logic, including IMPLY logic. In IMPLY logic with memristors, the state or conductance of the memristor represents the truth values of the antecedent and consequent propositions [54]. In the IMPLY gate, the states of the memristors (R_{OFF} and R_{ON}) correspond to the logical state variables (0 and 1), respectively. As shown in Figure S11, the gate consists of two memristors labeled *P* and *Q*, along with the resistor R_G.

As shown in Figure 7A, a schematic circuit has been designed based on a Cadence software IMPLY gate in Figure S11. The conductance of the memristor is modulated based on the input conditions and its historical states. When the antecedent condition is satisfied (e.g., input V_{in1} is true), the memristor adjusts its conductance accordingly. Subsequently, the conductance state of the memristor influences the output condition (e.g., output V_{in2} is true). If the antecedent condition is met (memristor conductance corresponds to input V_{in1} is true), the memristor transitions to a state representing a true output (consequent). Conversely, if the antecedent condition is not met, the memristor remains in a state where the output condition is undetermined.

To implement the logic depicted in Figure 7A, the circuit was connected to a differential pair followed by a buffer circuit as shown in Figure 7B. Figure 7C illustrates the input to the memristors and the final output of the circuit, demonstrating that the truth table requirements shown in Figure S10 are met. Additionally, Figure 7D presents the branch voltage V_T, which is the main voltage value of the memristor (*Q* or *P*) before the amplifier stage. It is evident that the input variations for each memristor differ across various modes.

In this context, the memristive properties of perovskites, including their nonvolatile resistance switching and high on/off ratios, play a critical role in ensuring reliable logic gate functionality. These results are significant as they demonstrate the potential of MHP-based memristors for use in logic circuits, which can lead to more energy-efficient and scalable computing architectures. The experimental setup involved characterizing the input-output relationships and ensuring the stability of the memristive states under repeated switching conditions. The data, as shown in Figure 7, corroborate the theoretical expectations and suggest that the unique electronic properties of perovskites could be harnessed to develop advanced computational elements. This study contributes to the growing body of evidence supporting the feasibility of integrating MHP memristors in next-generation memory and logic devices.

4.2.4 | Logic Gates Implementation

The memristor's resistance changes as current flows through it. In the memristor-based logic system, resistance changes are converted into voltage to represent logical values. Memristors can easily work with standard CMOS technology and serve as adjustable switches. These circuits save space and energy because they use fewer transistors, which enhances their functionality and increases the number of logic operations they can perform. Boolean logic gates, such as AND and OR, can be constructed using two memristors with opposite charges placed side by side.

The AND logic gate can be implemented using two memristors connected in parallel as shown in Figure 8A. In this context, we assign the high voltage (V_{high}) to the binary state "1" and the low voltage (V_{low}) to the binary state "0." When both inputs are the same, for example, $V_{inA} = 1$ and $V_{inB} = 1$, there is no voltage drop between the two terminals, and no current flows through the device. As a result, the output will match the inputs. The output expression for the AND gate for asymmetric inputs is provided in Equation (7). Figure 8B illustrates a logic

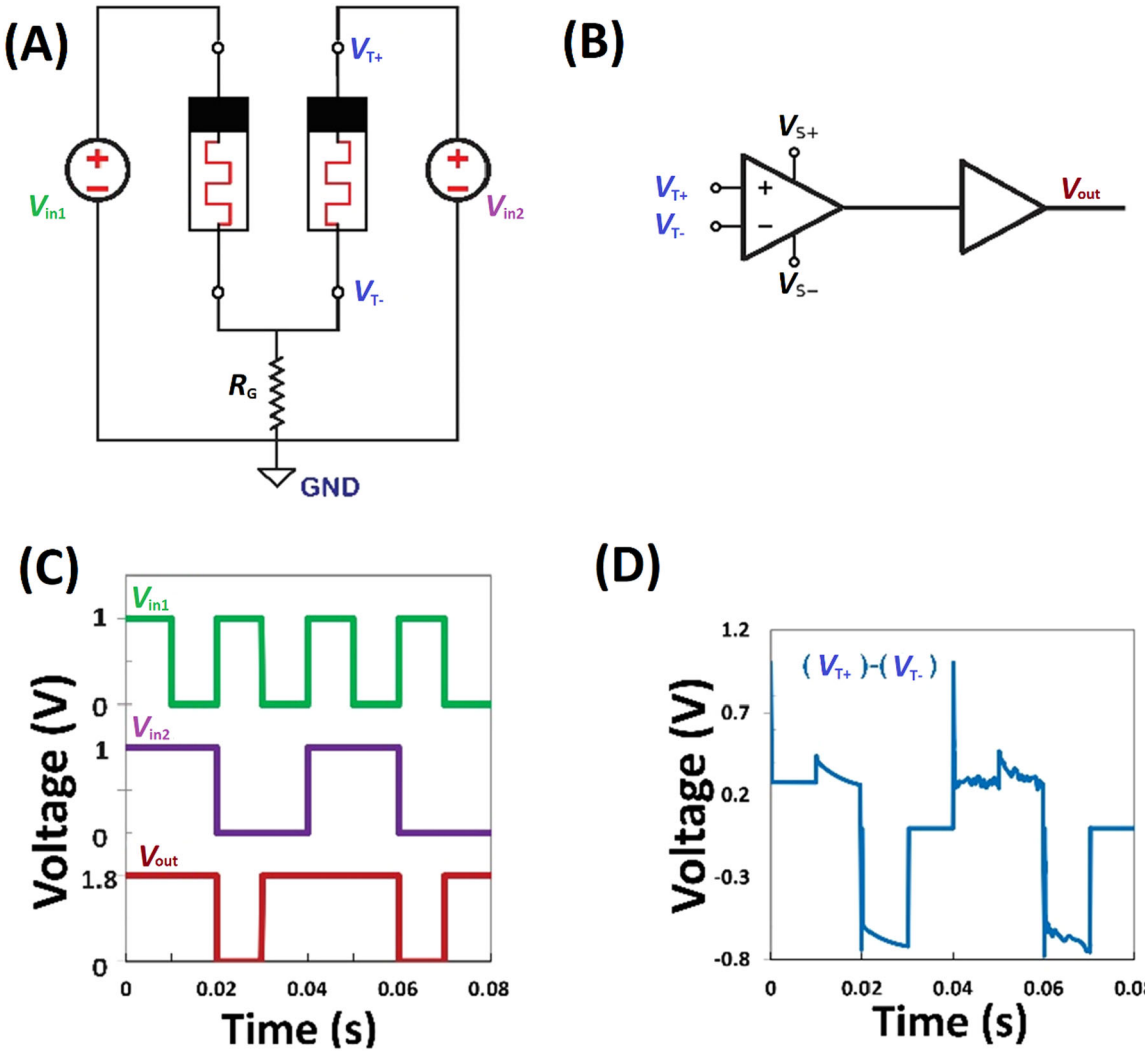

FIGURE 7 | (A) Schematic of the IMPLY gate designed in Cadence software. (B) Logic circuit connected to a differential pair and buffer. (C) Inputs to the memristors and final output, meeting the truth table in Figure S10. (D) The voltage across one of the memristors before the differential amplifier and buffer stage.

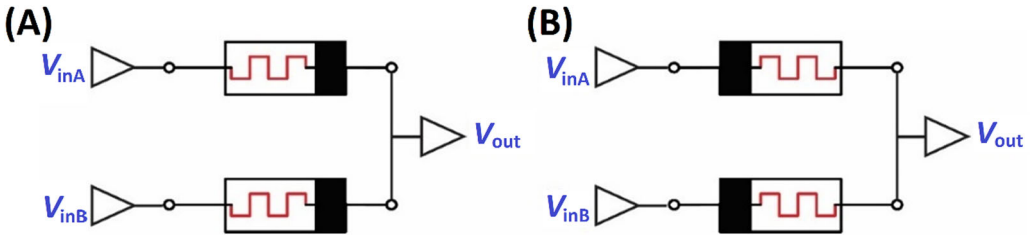

FIGURE 8 | Implementation of logic gates using perovskite memristors: (A) AND gate and (B) OR gate.

OR gate implemented using two memristors. A logic OR operation using a memristor can be implemented similarly to an AND gate, but with opposite polarity. The output voltage for the OR gate for asymmetric inputs is given in Equation (8).

$$V_{out} = \frac{R_{LRS}}{R_{LRS} + R_{HRS}} V_{high} \approx V_{low} \quad (7)$$

$$V_{out} = \frac{R_{HRS}}{R_{LRS} + R_{HRS}} V_{high} \approx V_{high} \quad (8)$$

In OR and AND gate circuits, the output signals are generated using voltage dividers, which can slightly weaken the signals. According to Equation (8), the output voltage is almost equal to the high voltage "1," but this minor drop does not have a significant impact on a single AND or OR gate. However, as the circuit complexity increases and multiple gates are cascaded, this signal degradation can accumulate, potentially affecting overall circuit performance. To address this issue, we can use a buffer in CMOS technology. Buffers help restore signal strength, ensuring reliable logic levels throughout the circuit. Additionally, placing a

NOT gate at the output of AND or OR gates not only solves this problem but also allows for the creation of NAND and NOR gates. Figure 9A demonstrates the implementation of a gate using an inverter in CMOS technology. As illustrated by the voltage diagram of the output node in Figure 9B, the logic operation of the gate is confirmed. This approach not only improves signal integrity but also expands the versatility of basic logic gate designs. Here, a threshold voltage of 0.5 V is used to define the logic levels. Voltages greater than 0.5 V are interpreted as logic high (1), while voltages less than 0.5 V are interpreted as logic low (0).

Figure 9C illustrates the output voltage (V_t) of the AND gate before the inverter stage. As expected, the voltage at this point represents the inverse of the circuit's binary logic output. Additionally, the voltage response reveals the presence of a glitch. A glitch is observed at the output of the gate during the simultaneous transition of its two inputs. This phenomenon occurs when one input switches from a high state to a low state while the other input transitions from a low state to a high state. The root cause of the glitch lies in the propagation delay differences within the gate. During this brief period, the intermediate nodes within the gate's logic circuit may temporarily assume unintended logic levels due to the misalignment in the arrival times of the input signals. As a result, the output momentarily deviates from its expected stable state, producing a transient voltage spike commonly referred to as a glitch. This behavior is particularly prevalent in circuits where the input signals have closely matched but not identical timing characteristics [55].

4.2.5 | Logic Circuit Implementation

In this section, the feasibility of creating complex digital logic circuits using MHP-based memristors is examined by investigating two different circuits.

4.2.5.1 | 1-Bit Numeric Comparator. A comparator is a fundamental component in digital circuits, designed to compare two binary inputs and determine their relationship. Specifically, a 1-bit numeric comparator compares two single-bit inputs (A and B) and produces outputs indicating whether A is greater than, less than, or equal to B. Comparators are essential in a wide range of digital applications, including arithmetic operations, sorting algorithms, and decision-making processes in

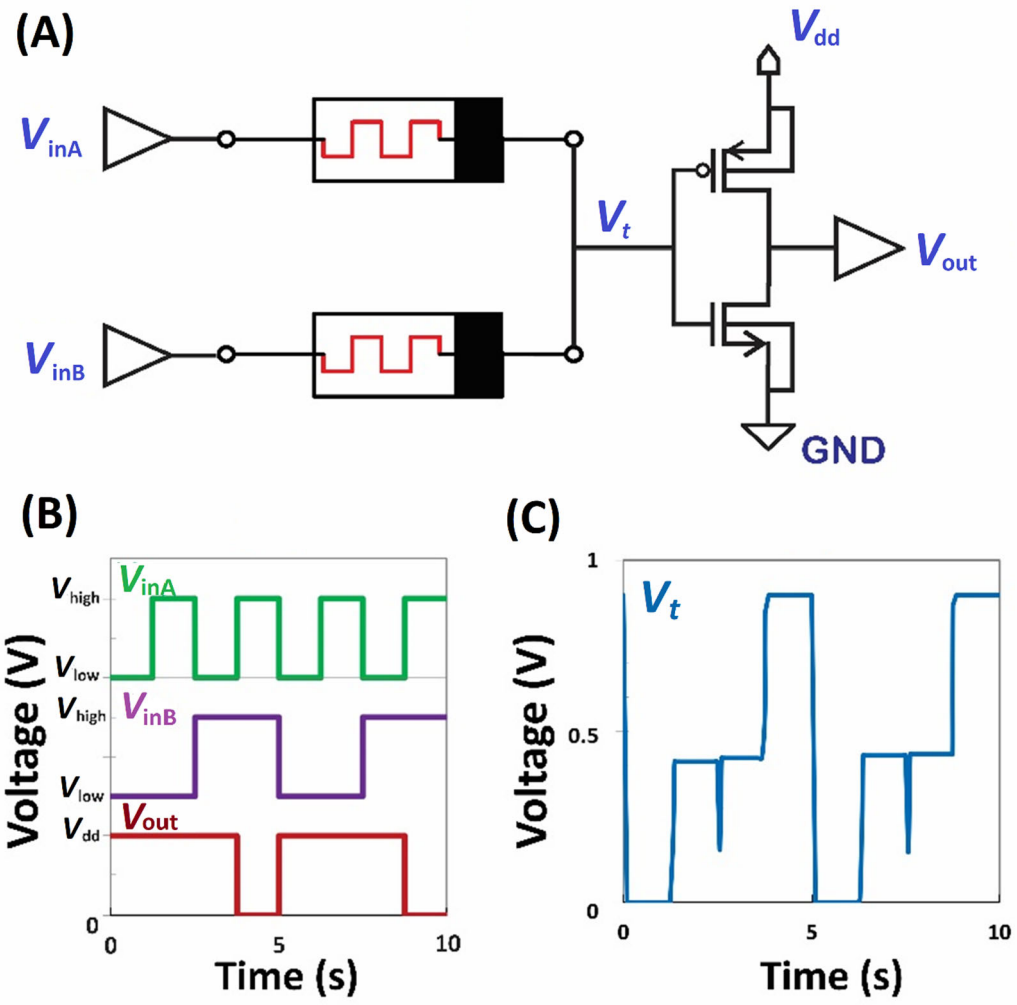

FIGURE 9 | (A) Implementation of NAND gates using MHP-based memristors. (B) Inputs and outputs of NAND gates. The output voltage result precisely matches the expected values according to the NAND gate truth table. (C) The actual AND gate output voltage before the inverter stage.

digital systems. They are integral to the functioning of various digital logic circuits, enabling complex operations such as magnitude comparisons, equality checks, and conditional branching, which are foundational to computer architecture and digital signal processing. A 1-bit comparator functions by evaluating the relationship between two binary inputs, A and B. The comparator generates three possible outputs: $A > B$, $A < B$, and $A = B$. These outputs are derived through a combination of basic logic gates.

Implementing a 1-bit comparator using memristors offers several advantages over traditional CMOS-based designs, particularly when using advanced materials like perovskite. One significant benefit is size compared to the circuit based on CMOS gates and the potential for increased integration density. Figure 10A shows the designed circuit for the 1-bit comparison operation. This circuit includes four NMOS transistors and four memristors. In this circuit, we consider a high voltage as a logical one and a low voltage as a logical zero. The table shown in Figure 10B indicates the conditions of all three output ports based on the voltage applied to the input pins. When both input voltages are the same, all transistors will be in the same state, and the $A = B$ output will follow the V_{dd}. When both inputs are low, all transistors will be off. Conversely, when both inputs are high, the upper transistors turn on. It is worth mentioning that when the transistors are on, there will be a slight voltage drop at the $A = B$ output. Here we have defined a reference voltage of 750 mV to determine the high and low states. On the opposite side, if the inputs are symmetrical, the corresponding ($A < B$ and $A > B$) outputs are connected to each input. Figure 10C shows the $A = B$ output voltage in different input modes (A and B). We consider any voltage higher than the reference line to be a logical one, and any voltage lower than the reference line to be a logical zero.

4.2.5.2 | Full Adder. A full adder is a fundamental building block in digital circuits, responsible for performing the arithmetic operation of addition on three input bits. Specifically, it adds two significant bits and an additional carry bit from a previous operation, producing a sum and a carry output. The full adder is essential in constructing arithmetic circuits, such as adders in processors, which enable the addition of multi-bit binary numbers by cascading multiple full adders in series. It is a critical component in the design of more complex arithmetic operations and is foundational to various digital logic circuits, making it indispensable in modern computing systems. A full adder is a digital circuit that performs binary addition on three inputs: two binary digits (A and B) and a carry-in bit (C_{in}). It outputs a sum bit (S) and a carry-out bit (C_{out}). The sum is calculated using an XOR operation on A, B, and C_{in}, while the carry-out is determined using a combination of AND and OR gates. The full adder enables multi-bit binary addition by cascading multiple adders, making it essential in arithmetic logic units (ALUs) and other computational circuits [56].

Implementing a full adder using memristor gates offers several advantages that can revolutionize digital circuit design. Memristors inherently retain their resistance state even when power is removed, eliminating the need for additional memory storage elements. This nonvolatility reduces the circuit's overall

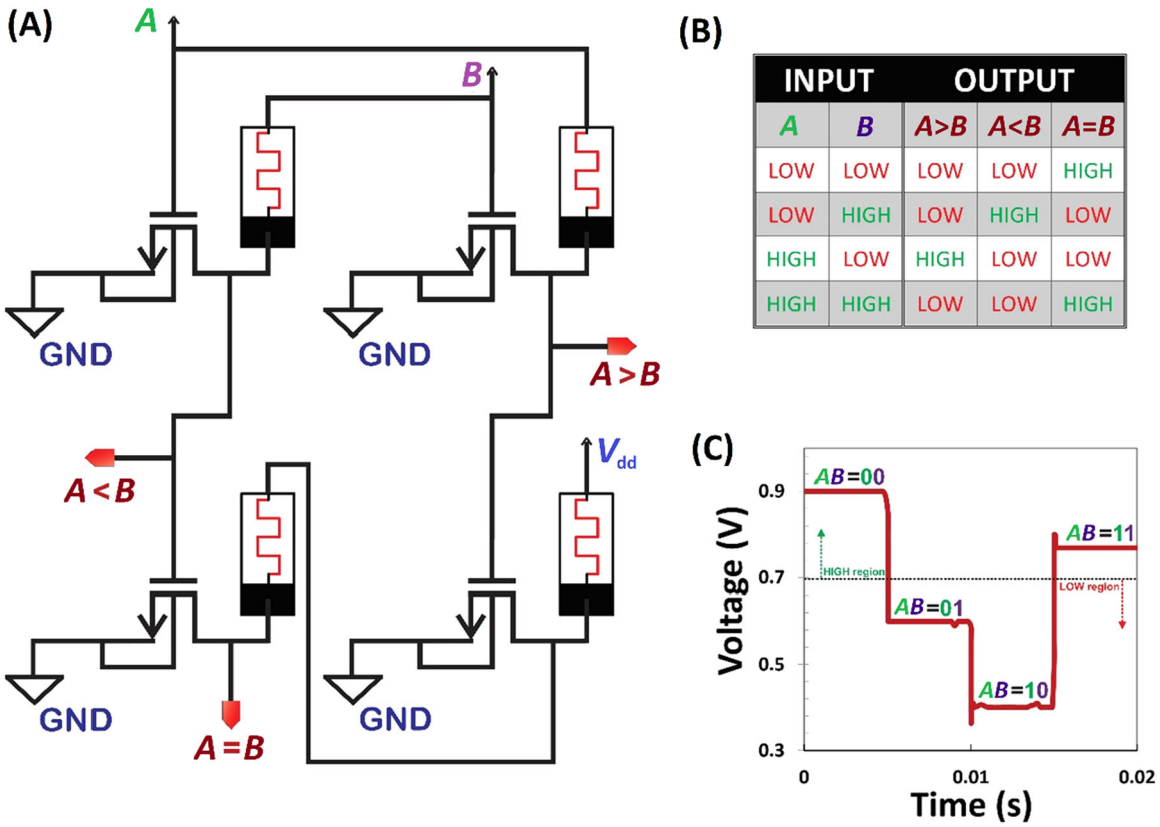

FIGURE 10 | (A) 1-bit comparator circuit using MHP-based memristors, demonstrating a compact design compared to CMOS-based circuits. High and low voltages are defined as logical 1 and 0, respectively. (B) Truth table showing output conditions for ports $A = B$, $A < B$, and $A > B$ based on input voltages. (C) $A = B$ output voltage for different input modes.

complexity and power consumption, making the system more efficient. Additionally, memristors can be fabricated at a very small scale, allowing for higher integration density compared to traditional CMOS-based logic gates. This property enables the creation of more compact full adders, paving the way for the development of ultra-dense memory and logic circuits in future computing systems. Furthermore, memristor-based circuits typically consume less power compared to their transistor-based counterparts, which is particularly advantageous in applications where energy efficiency is critical, such as in portable electronic devices and large-scale data centers. Additionally, the switching speed of memristors is comparable to or faster than that of traditional transistors, which translates to faster computation times in digital circuits [57]. This feature is crucial for high-speed arithmetic operations, making memristor-based full adders highly suitable for high-performance computing applications. By leveraging these advantages, the design of a full adder using memristor gates not only demonstrates the feasibility of memristor-based logic gates but also highlights the potential for significant improvements in computational efficiency, circuit density, and energy consumption. These benefits position memristor technology as a promising alternative to conventional digital circuit design, particularly in the context of next-generation computing architectures.

The schematic diagram of a 1-bit full adder designed using a CMOS inverter is illustrated in Figure 11A. The design incorporates six AND logic gates using memristors, three OR logic gates also based on memristors, and four CMOS inverters. In this design, we have matched the output voltage levels of the gates to the input logic levels by using voltage buffers. As the results presented in Figure 11B show, the correctness of the full adder circuit,

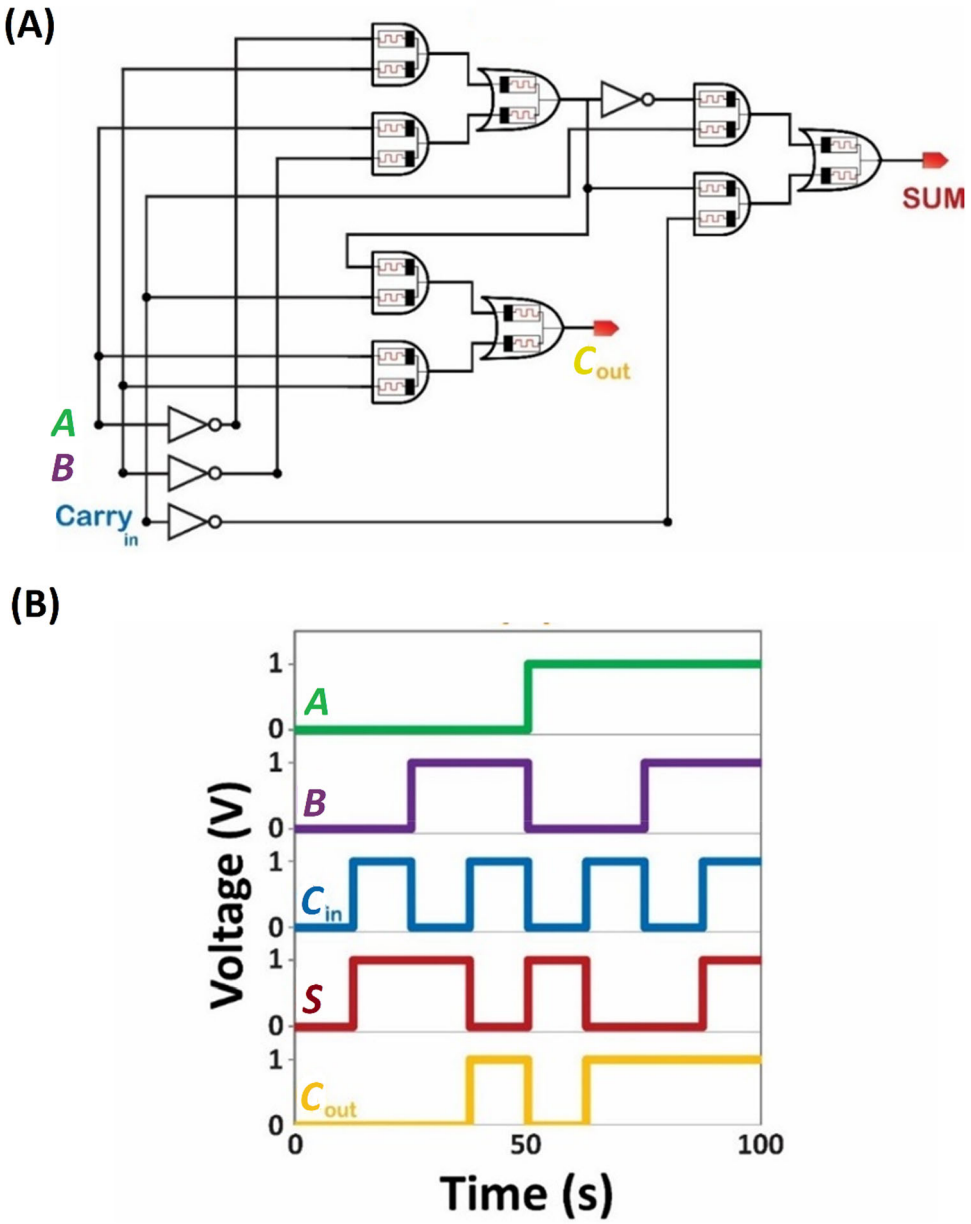

FIGURE 11 | (A) Schematic diagram of a full adder designed using AND and OR gates based on MHP-based memristors. (B) Inputs (A, B, and C_{in}) and output voltage levels for SUM and C_{out}, confirming the correct operation of the full adder circuit based on the applied input bits.

based on the applied input bits, can be confirmed by the voltage levels in the two outputs: SUM and C_{out}.

4.2.5.3 | Multiplexor. A multiplexer, or "mux," is a fundamental digital circuit that selects one of several input signals and forwards the chosen input to a single output line. It acts as a data selector, allowing multiple input signals to share a single communication channel or resource, effectively reducing the number of data paths needed. Multiplexers are essential components in digital circuits because they enable efficient data routing in systems like processors, communication devices, and memory management, where space and power efficiency are crucial. As shown in Figure 12A a multiplexer uses select lines, which are binary signals, to determine which input signal should be connected to the output. For an m-to-1 multiplexer, there are 2^m input lines and m select lines. The selected lines are used to form a binary number that determines which input is chosen [58].

Memristor-based multiplexers are particularly suitable for high-speed and energy-efficient computing applications, where performance and power consumption are critical. Another significant advantage of using memristors in multiplexer design is their inherent reconfigurability. Memristors can be programmed to emulate various logic gates, providing flexibility in circuit design. This adaptability allows a single memristor-based multiplexer circuit to be reconfigured dynamically, offering multiple functionalities and simplifying the overall design.

Figure 12B illustrates the implementation of a 4-to-1 multiplexer using designed memristors. This design includes four three-input AND gates in the first stage; each connected to an input bit and the selector address lines. When both address lines are in a high-voltage state, the corresponding input data is transmitted. In the second stage, parallel NMOS transistors function as OR gates, transferring the outputs of the memristors to the output stage. Due to a phase shift of 180° introduced by the transistors, a NOT gate is included in the output stage. In this design, the V_{dd} is equal to the high voltage of the input signals, with R_D and R_L set to 220 Ω and 1 MΩ, respectively. Figure 12C shows the input signals, selector signals, and the output of the multiplexer, demonstrating that the selector signal determines which input line is transferred to the output.

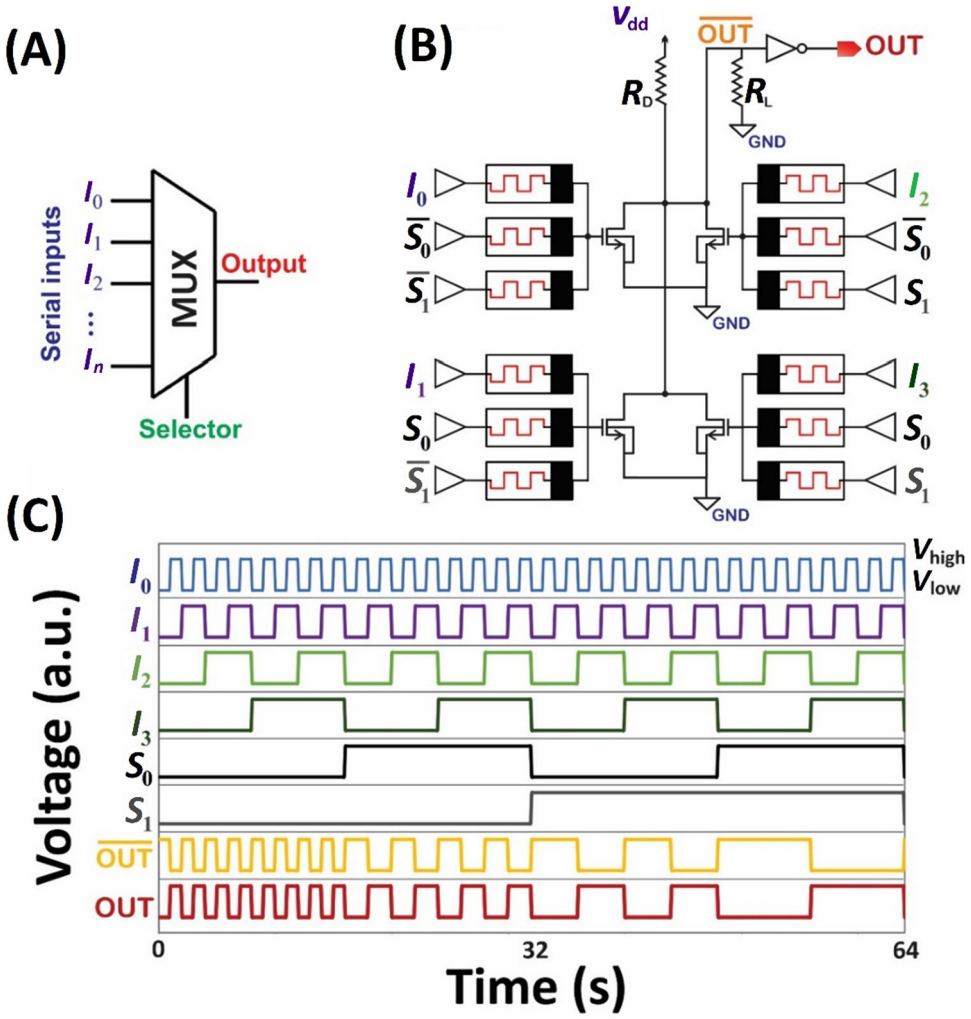

FIGURE 12 | (A) A conventional multiplexer diagram illustrating the use of select lines to determine the input-output mapping. (B) Design of a 4-to-1 multiplexer using memristors, showcasing the circuit's stages including three-input AND gates, NMOS transistors, and a NOT gate for phase correction. (C) Timing diagram displaying input signals, selector signals, and corresponding output, validating the correct operation of the memristor-based multiplexer.

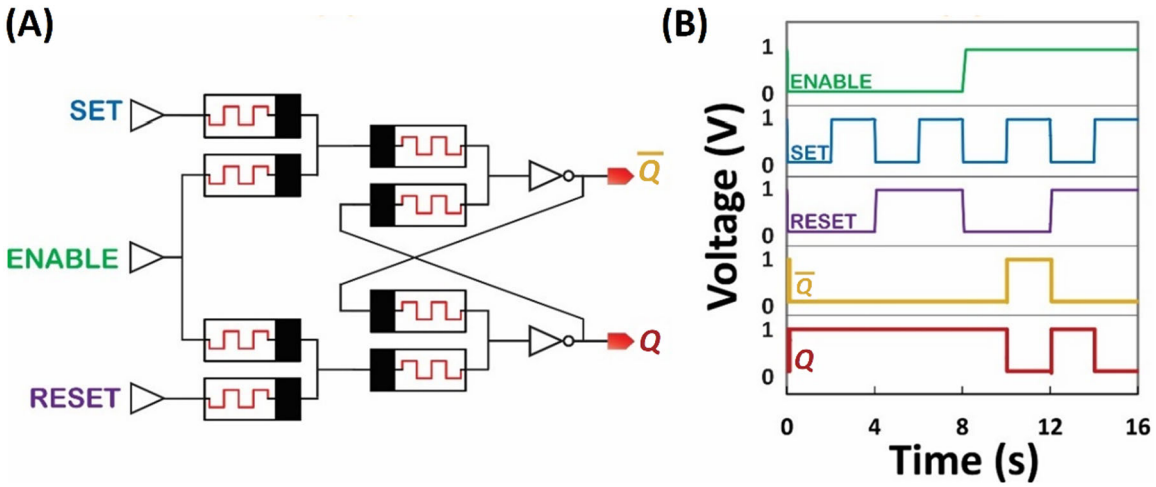

FIGURE 13 | (A) Diagram of an SR flip-flop using an MHP-based memristor. (B) Input signals, selector signals, and simulation corresponding to the output circuit-based SR flip-flop.

4.2.5.4 | SR Flip-Flop. A flip-flop is a basic bistable circuit used in digital electronics to store a single bit of data, functioning as a memory element that has two stable states. It is a fundamental building block in sequential logic circuits, which are essential for storing state information and enabling complex operations in digital systems, such as data storage, synchronization, and state machines. Flip-flops are crucial components in registers, counters, memory devices, and various control circuits in digital electronics, making them indispensable for a wide range of computing and communication applications. A flip-flop works by maintaining its output state until it is triggered to switch states by an input signal, such as a clock pulse. The most common types of flip-flops include SR (Set-Reset), D (Data or Delay), JK, and T (Toggle) [59].

An SR flip-flop with the proposed MHP-based memristor is designed as shown in Figure 13A based on using memristor gates. This circuit operates as a memory element that stores a single bit of data based on the states of the Set and Reset inputs, controlled by an enable signal. When the enable signal is active (ENABLE = 1), the flip-flop responds to the S and R inputs to determine its output states, Q and Q'. As Figure 13B shows, if SET = 1 and RESET = 0, the flip-flop enters the set state, making $Q = 1$ and $\bar{Q} = 0$. If $S = 0$ and $R = 1$, it enters the reset state, setting $Q = 0$ and $\bar{Q} = 1$. When both SET and RESET are 0, the flip-flop holds its previous state, maintaining its current outputs. However, if both SET and RESET are 1, it results in an invalid state where both Q and $\bar{Q}$ are 0, which contradicts the normal operation, as Q and Q' should always be complementary. This configuration allows the flip-flop to store data based on input conditions, making it a fundamental component in digital circuits for data storage and sequential logic.

4.2.6 | Performance Comparison of NMOS and Memristor-Based Gates

In this section, we provide a comparative analysis of gates implemented using NMOS transistors vs. memristors, focusing on key performance metrics that are critical to digital logic design. By leveraging Cadence ADXL for detailed simulations, we evaluate and contrast these two implementations across several specifications, including delay, power consumption, noise margin, and leakage current. This comparison aims to highlight the advantages and limitations of each technology, offering insights into their suitability for various applications and future integration into advanced digital systems.

Figure 14A shows the basic NAND gate structure in Resistor–Transistor Logic (RTL), while Figure 14B depicts the basic AND gate structure using memristors, as described in Section 4.2.4 (Logic gate implementation). To implement an AND gate in the RTL class, it is necessary to add an inverter to the circuit shown in Figure 14A. This addition of an inverter can affect the parameters being compared. Therefore, we use these two basic structures as evaluation criteria. The gate designed in Figure 13A using the CAD simulator with XFAB 180-nanometer technology includes two NMOS transistors, each with a channel length of 180 nm, a width of 1 μm, and an R_D of 100 kΩ. For both circuits, the input signals are applied similarly, with an amplitude of 900 mV, with a second for rise and fall time and periods of 100 s and 50 s, respectively. Also, the power supply (V_{dd}) is set to the same as the high voltage value of 900 mV.

For our comparison, the gate implemented with NMOS transistors and the gate using memristors both have a large propagation delay of approximately 273 ms for NMOS and 21 ms for memristors. For the propagation delay calculation, the time interval between the input and output signals is measured at 50% of the maximum pulse amplitude. In this calculation, both the rising and falling times are set to 1 s. This means the delay is evaluated based on when the signal reaches half of its maximum value during both the rise and fall of the pulse. The observed high delay in the NMOS-based gate can be attributed to the low supply voltage and input signal voltage levels. Operating at a supply voltage of 900 mV, the NMOS transistors experience reduced drive strength, which limits the drain current available for switching. This reduced current leads to longer charging and discharging times of the load capacitance, directly contributing to increased delay. Additionally, if the

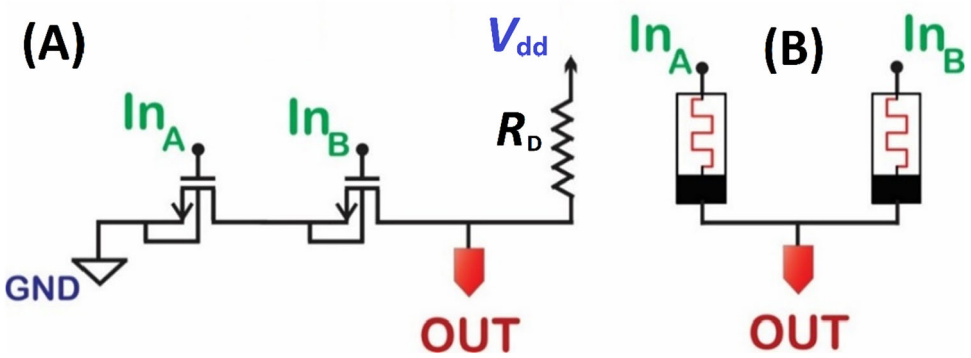

FIGURE 14 | (A) Basic 2 input NAND gate structure in Resistor–Transistor Logic (RTL). (B) Design of an AND gate using MHP-based memristors.

input signal voltages are also around 900 mV, the transistors may not fully switch between their on and off states. This incomplete switching can cause the transistors to operate in the linear region instead of the saturation region, further increasing the delay due to slower transition times.

Power consumption is a critical parameter in evaluating the efficiency of digital logic gates. It comprises both dynamic powers, associated with switching activities, and static power, which arises due to leakage currents when the circuit is idle. In our simulations over a 100-s period, covering four different states for each gate type, the memristor-based AND gate exhibited significantly higher power consumption compared to the NMOS-based AND gate. For the memristor-based AND gate, the power consumption was measured at 54.53 mW for Source 1 and 55.17 mW for Source 2. In contrast, the NMOS-based AND gate showed considerably lower power consumption, with values of 2.53 fW for Source 1, 5.97 fW for Source 2, and 188 μW for the power supply.

The higher power consumption in the memristor-based gate is likely due to the intrinsic properties of memristors, which typically have larger leakage currents and higher static power dissipation. Memristors also consume more power when switching due to their resistive nature, contributing to greater dynamic power consumption compared to the NMOS gate, which benefits from more efficient switching characteristics and lower leakage currents. These results highlight the trade-offs between using memristor-based gates and traditional transistor-based gates in terms of power efficiency. It should be noted that, due to the very low resistance of memristors at similar voltages, a large current passes through them, leading to increased energy consumption. Therefore, reducing the voltage range can be helpful in decreasing power consumption. In the Verilog model defined according to Equations (3)–(6), the effect of noise is not considered, so more accurate measurements are needed to account for it. Meanwhile, the high and low noise margins of the NMOS gate were calculated as 110 mV and 504 mV, respectively. On the other hand, since there is no power supply in the memristor gate, there will be no leakage current in the idle state. However, in the NMOS gate, the leakage current in the idle state is 1.15 pA.

Monte Carlo analysis is a statistical technique used in circuit design to assess the impact of variations in manufacturing processes, component mismatches, and environmental conditions on the performance of electronic circuits. By simulating a circuit multiple times with randomly varied parameters, Monte Carlo analysis provides a comprehensive understanding of how these variations can affect key performance metrics such as delay, power consumption, noise margin, and leakage current. The necessity of Monte Carlo analysis in modern integrated circuit design stems from the increasing variability in fabrication processes as device sizes shrink and densities increase. These variations can lead to significant differences in the behavior of supposedly identical circuits, potentially impacting yield and reliability [60]. Monte Carlo analysis allows designers to predict and mitigate these effects by identifying the statistical distribution of circuit performance across different process corners and operating conditions.

Here, we have defined a Verilog-A model for the gate based on our MHP-based memristor design. This model captures the idealized behavior of the memristor-based gate without incorporating the specific fabrication parameters that would typically introduce variability into the device's characteristics. Because the Verilog-A code is an idealized representation, it does not account for the process variations, mismatches, or environmental fluctuations that are inherent in real-world manufacturing and operation. As a result, when we apply Monte Carlo analysis to the memristor-based AND gate as shown in Figure 14B using this idealized Verilog-A model, we observe that the results do not change across different simulation runs. This lack of variability is because the model does not include any parameters that would vary from one simulation to another, such as threshold voltage variations, resistive deviations, or other process-induced discrepancies. While for the NMOS-based NAND gate presented in Figure 14A, Monte Carlo simulations typically reveal how variations in manufacturing processes, such as changes in channel length, oxide thickness, or dopant concentrations, affect performance metrics like delay, power consumption, and noise margin.

Because we have used MHP-based memristors to create the logic gates in this study, the performance is significantly influenced by the memristor's HRS and LRS. These two resistance states are crucial as they directly impact the overall functionality of the memristor-based gate. To simulate the effects of process variations on these memristor-based gates, we need to consider which parameters as presented in Table 1 might

influence the resistance states of the memristors. By identifying and varying these parameters in simulations, we can predict how they might cause unwanted changes in the resistance of the memristors. This type of analysis allows us to anticipate potential manufacturing issues and understand the variability in performance that could arise from such variations.

In Figure 15, the Monte Carlo results for the voltage state of the gates in Figure 14 are presented. These results demonstrate the consistency of the gate's performance under various simulated conditions according to the fabrication process. Figure 15A illustrates the Monte Carlo results for the NMOS-based gate over 1000 samples, focusing on the gate output in the high voltage state. The standard deviation (Std dev) observed in these results indicates a very small impact of fabrication conditions on the output, suggesting that the NMOS-based gate is relatively robust against variations in the manufacturing process. In this Monte Carlo simulation, statistical variations were considered for both process and mismatch modes, and the sampling method was randomly selected to simulate realistic fabrication variations. This approach allows for a comprehensive assessment of how process inconsistencies and component mismatches can influence circuit behavior.

Figure 15B depicts the Monte Carlo curve for the memristor-based AND gate, also using 1000 samples. In this gate, for the same input conditions, the output voltage does not exhibit changes due to the zero current, indicating that fabrication

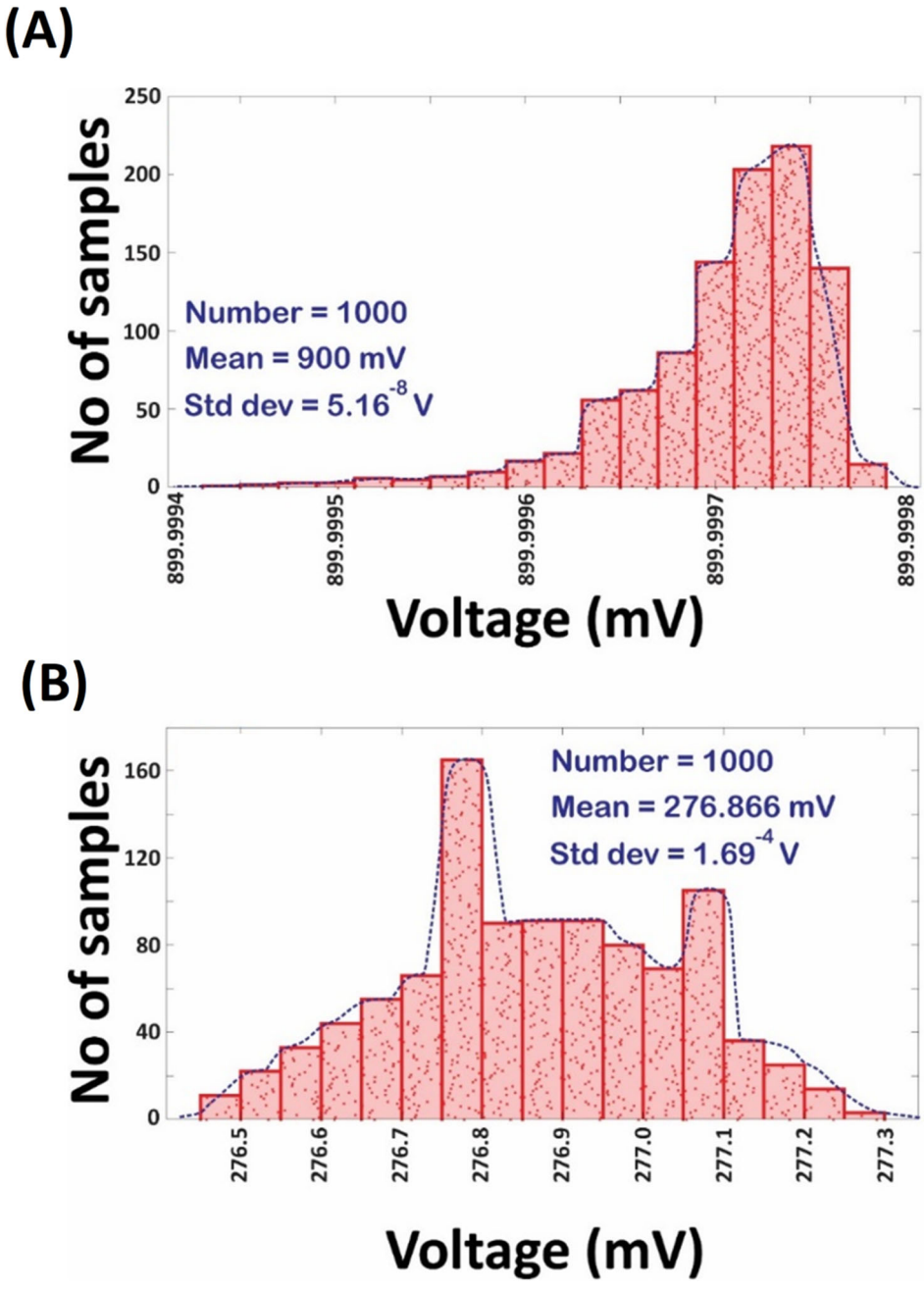

FIGURE 15 | Monte Carlo analysis results showing voltage states for NMOS-based in high state (A) and memristor-based in low state (B) gates across 1000 samples.

conditions have no impact on the output under symmetrical input conditions. However, when the inputs are asymmetrical, slight variations in output voltage can occur due to the intrinsic characteristics of the memristor. To capture these potential changes, a scenario with a nonzero low output mode was tested. For this purpose, parameters g_H, g_L, and V_t were altered by 2%, a variation range selected based on the experimental data presented in the supporting material. The gate output was simulated thousands of times with different permutations of these parameters, and the results were recorded to analyze the impact of these variations. The Monte Carlo plot for the memristor-based gate also shows minimal changes in the results, highlighting the stability of the memristor's performance under slight variations. It is worth noting that within this range of variability, the changes do not adversely affect the logical operation of the gate. This indicates that the memristor-based gate logic is inherently robust to small parameter variations, ensuring reliable performance even when slight deviations from the ideal are present.

5 | Conclusion

The research presented in this paper addresses the growing need for efficient, secure, and scalable memory technologies, particularly within the context of edge computing and next-generation digital systems. The study focuses on the development and application of MHP-based memristors in logic circuit design, highlighting their potential to revolutionize computing architectures. The problem at the core of this study is the need to overcome limitations in traditional memory systems, particularly concerning data security and processing efficiency, which are becoming increasingly critical as data-intensive applications proliferate.

The key findings from this study demonstrate that MHP-based memristors not only provide superior resistance-switching characteristics but also offer significant advantages in terms of integration with existing CMOS technology, making them a promising candidate for future memory and logic applications. The experiments and simulations detailed in the paper confirm the feasibility of using these memristors in a variety of logic gate designs, such as IMPLY gates, AND, OR, and more complex digital circuits like multiplexers and full adders. These circuits show that memristors can perform both memory and logic operations, which is crucial for in-memory computing systems.

The significance of this study lies in its potential to pave the way for more energy-efficient, compact, and secure digital systems. By integrating memristors into standard computing architectures, it is possible to reduce the physical footprint of circuits while improving their performance and security features. The paper also opens up several avenues for future research, including the exploration of other MHP materials, further refinement of memristor models, and the development of more complex digital systems utilizing this technology. These advancements could have far-reaching implications for the future of computing, particularly in areas requiring high-density memory and low-power consumption.

Acknowledgments

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Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available in Supporting Information S1 of this article.

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Supporting Information

Additional supporting information can be found online in the Supporting Information section.

Figure S1: a) Orange-red colored MHP precursor solution and b) Top-view of MHP Film used in this study. **Figure S2:** Reproducibility test of the MHP memristor devices. Static boxplots of HRS, LRS, and ON/OFF ratio collected in (a-b) 15 different device-to-device reproducibility test and (c-d) 30 different cell-to-cell reproducibility tests. **Figure S3:** Stability test of the MHP memristor device. Consecutive 40 cycles of *I–V* were measured 4 weeks. **Figure S4:** *I–V* curves depending on the scan rate from 10 V/s to 500 V/s (a) Experimental and (b) simulations. **Figure S5:** *I–V* scanned in the dark condition and under illumination with white light source. **Figure S6:** Fundamental components MHP-based memristor models. **Figure S7:** The voltage dependence of the stationary system state variable in red and the system response time in blue. **Figure S8:** Comparison of *I–V* characteristics for MHP memristors with different top electrode diameters (A) 50 μm, (B) 100 μm, and (C) 200 μm, demonstrating consistent bipolar switching behavior and scalability toward CMOS-compatible dimensions. **Figure S9:** *I–V* curves for different applied voltage amplitudes: (A) −0.75 V to +0.5 V, (B) −2.25 V to +1.5 V, and (C) −3 V to +2 V. **Figure S10:** (A) Truth table and (B) Circuit symbol of the IMPLY gate. **Figure S11:** IMPLY gate using memristors, with states of memristors representing logical variables (0 and 1), and components including two memristors (P and Q) and resistor RG.