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ABSTRACT

Memristors are key elements for building synapses and neurons in advanced neuromorphic computation. Memristors are made with a wide range of material technologies, but they share some basic functionalities to reproduce biological functions such as synapse plasticity for dynamic information processing. Here, we explain the basic neuromorphic functions of memristors, and we show that the main memristor functionalities can be obtained with a combination of ordinary two-contact circuit elements: inductors, capacitors, resistors, and rectifiers. The measured *IV* characteristics of the circuit yield clockwise and counterclockwise loops, which are like those obtained from memristors. The inductor is responsible for the set of resistive switching, while the capacitor produces a reset cycle. By combining inductive and capacitive properties with gating variables represented by diodes, we can construct the full potentiation and depression responses of a synapse against applied trains of voltage pulses of different polarities. These results facilitate identifying the central dynamical characteristic required in the investigation of synaptic memristors.

I. INTRODUCTION

With the rapid advancement of artificial intelligence (AI), artificial neural networks (ANNs) have sparked a growing interest in novel computational models. Complementary metal–oxide semiconductor (CMOS)-based data processing technologies previously used in ANN systems have been replaced by other next-generation memory-processing technologies with a view to overcome the huge energy consumption caused by the von Neumann bottleneck.[1] Among various processing technologies for ANNs, neuromorphic memristors have emerged as a promising approach to design and mimic the biological brain circuit systems because of their striking similarities with the human brain regarding information processing and low energy consumption.[2–6] These advancements aim to create systems capable of real-time, efficient, and adaptive information processing akin to the human brain.

Memristors were discovered theoretically and experimentally in 1971[7] and 2008,[8] respectively, and they were defined as the fourth fundamental circuit element at that time because they enable unique functionalities. More specifically, and in contrast with common elements of electrical circuitry, the internal resistance of a memristor can change drastically when an external stimulus is applied to the device. This property is critical for the development of neural circuits because it provides the possibility of potentiating or depressing the signal transmission associated with individual units composing the circuit, or in other words, it confers synaptic weight related to the conductance change.[9,10] At the same time, it allows establishing memory variables with plasticity that are crucial for dynamic learning, memorizing/forgetting/storing processes, pattern recognition, etc.[11–13]

So far, many memristive systems based on different physical mechanisms and material structures have been studied.[5,6] These technologies share in common that an internal property of the memristor modulates the device conductance and it can be manipulated by electrical pulses.[14–19] They show *IV* curves consisting of hysteresis loops that cross at the origin and they have shown a more or less appropriate response to applied stimulus.

Since the range of memristors that have been investigated spans a remarkably wide class of materials (e.g., chalcogenide materials,[20] HfO_2,[21] metal oxides[22,23] and other ion carriers,[11,24,25] electrochemical metallization cells,[26] phase change materials,[27] and halide perovskites[28–32]), the focus of their interpretation is often on specific mechanisms responsible for resistive switching, and the neuromorphic operation is demonstrated by certain measurement protocols. The neuromorphic applications have been reviewed in many works,[33–37] and advanced models to describe the neuromorphic properties have been developed.[26,38–44]

The aim of this paper is to obtain fundamental insight into the neuromorphic behavior based on the known temporal response of capacitive–inductive circuits and to show the essential backbones of memristive dynamics. In the first part of the paper, we provide a brief introduction to the typical memristor characteristics that enable synaptic functions. In the second part of the paper, we build elementary operational circuits that reproduce the essential dynamic characteristics of synaptic functions. We do not aim to review or produce general models of the complicated mechanistic properties. Instead, this analysis will provide insight into a common denominator of dynamical properties of memristors that can be applied in neural network circuits.

Currently, available memristors are indeed constructed from conventional electronic components, as shown in the example of Fig. 1.[45] It can be observed that the circuit uses multiple transistors to generate the memristor characteristics. In fact, creating nonlinear circuits using classical electrical elements has been a fundamental practice in electrical engineering for over a century, dating back to the inception of the field. Circuits that emulate neurons have been constructed by combining a negative resistance element and matched *RC* elements, leading to relaxation oscillations.[46–48] Inductive components have been remarked in memristors and neurons.[49–52] Recently, the connections of inductors and hysteresis have been generally described.[53]

However, in this paper, we do not address oscillatory systems. Here, we would like to raise the question of whether it is possible to substitute or emulate the main functions of the behavior of synaptic memristors with a simple electrical circuit. For example, as the memristor is a two-contact element, using three-contact transistor components seems an increase in complexity. Therefore, we have described the electrical response of elementary components separately such as an inductor and a capacitor, and based on the obtained results a circuit that includes additional elements such as rectifiers has been proposed and analyzed experimentally. We show a combined circuit that produces the main functionalities of a synapsis element. The study paves the way for identifying the central

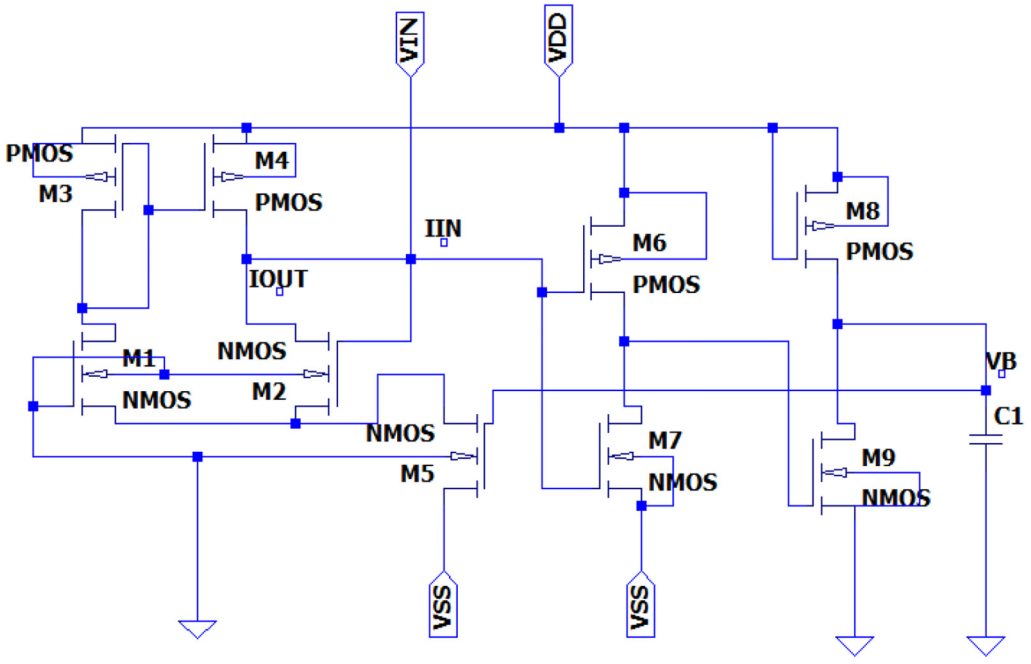

FIG. 1. Proposed memristor emulator circuit. Reproduced from P. K. Ghosh, S. Z. Riam, M. S. Ahmed, P. Sundaravadivel, Electronics **12**, 1654 (2023). Copyright 2023 Author(s), licensed under a Creative Commons Attribution (CC BY) license.

dynamical characteristic required in the investigation of synaptic memristors.

II. NEUROMORPHIC CIRCUITS

Neuromorphic circuits and synapses are inspired by the brain's ability to process and store information through highly complex, dynamic interactions. One of the most significant challenges in emulating biological brain computation is replicating the functions of biological synapses. These synapses rely on ions and neurotransmitters to mediate response delays, playing a central role in processes such as learning, memory, and inference.[35,54,55] Key characteristics of biological synapses include:

(1) Synaptic plasticity is the ability of synapses to strengthen or weaken over time in response to changes in their activity. It encompasses two main types: long-term potentiation (LTP), a sustained increase in synaptic strength resulting from repeated co-activation of neurons, often regarded as the cellular basis of learning and memory, and long-term depression (LTD), a prolonged decrease in synaptic strength caused by low-frequency stimulation, which helps refine neural networks by weakening less functional connections.
(2) Spike-Timing Dependent Plasticity (STDP). The brain's ability to learn and memorize through the precise timing of neural spikes is known as STDP. It relies on neuroplasticity mechanisms like LTP and LTD, where synaptic strengths are adjusted over time based on specific activity patterns.
(3) Dynamic Information Processing: Synapses aid in real-time information transmission and adaptation. Their reliance on biochemical processes such as neurotransmitter release makes them highly sensitive to activity-induced changes, enabling rapid adjustments.

In most artificial neuromorphic analog circuits, the neurons and synapses operate electrically. The neurons are the nodes that emit the impulse signals as spikes according to the received signals. The synapse conductivity can be modulated to provide the computational weights in a neural network link between neurons, as indicated in Fig. 2(a). In accordance with the biological operation, the synapse weight must be adapted by the incoming impulses, as shown in two successive potentiation steps in Fig. 2(b). We remark that the increase in current with a certain characteristic time τ is

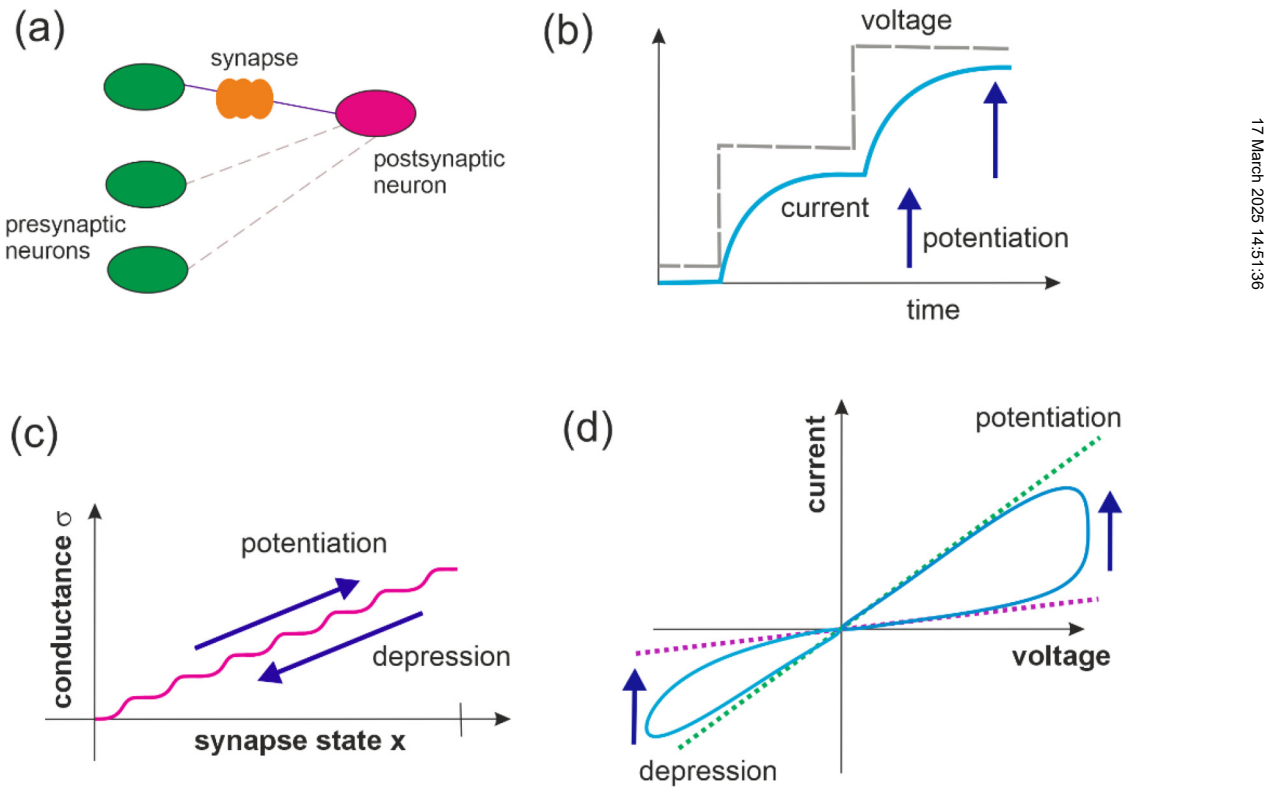

FIG. 2. (a) A synapse weights the signal transmission between two neurons in the neural network. (b) The voltage impulses increase the conductivity of the synapse element in the potentiation process. (c) By changing the internal state of the synapse, the conductance is increased (decreased) stepwise in potentiation (depression) cycles. (d) A memristor is a two-contact element in which the conductance can be modulated between a high resistance state (pink line) and a high conductance state (green line). A voltage increase produces potentiation, and a negative excursion produces depression.

the standard transient response of an inductor element (with a resistor), as we explain in more detail later.

The synapse must be formed by an element with an internal variable that modulates and maintains a variable conductance, as shown in Fig. 2(c). Therefore, the role of synapses is often taken by memristor devices where the conductivity can be changed between two contacts by external stimuli.[11,33,39–41,56,57] The properties of the memristor enable an increase in conductance, at positive voltage (a *set* process), and a decrease in conductance, by a negative voltage excursion (*reset* process), as shown in Fig. 2(d). These properties rely on hysteresis features that correspond to an internally delayed dynamics in the current–voltage response.[53] The hysteresis can be traced to certain internal capacitive-like and inductive-like properties that underlie memristor dynamics in general.[58] Therefore, in this paper, we use raw capacitors and inductors to illustrate the memristor dynamics that produces the desired synapse plasticity. But before turning to the construction of simple element circuitry, we will revise the realistic properties of memristors in Secs. III and IV.

III. EXPERIMENTAL RESPONSE OF NEUROMORPHIC MEMRISTORS

Figures 3 and 4 show the characteristic experimental responses of different memristive systems. Figure 3 corresponds to a self-organized nanowires network.[59,60,62] In Fig. 3(a), the current–voltage curve, measured at a certain cycling velocity, shows two hysteresis loops at positive and negative voltages, respectively. The curve self-crosses at the origin and consequently the loops have opposite circling directions: the one at positive voltages is counterclockwise, and the one at negative voltages is clockwise. We call these types of loops inductive and capacitive,[53] respectively. When a positive voltage impulse is applied, an increase in the slope of the *IV* curve [Fig. 3(a)] occurs that finally determines two conductance states, defined by two different slopes, occurring at different stages of the cycle. In Fig. 3(a), the curve sections next to arrows 1 and 4 correspond to a system state with a lower conductance than those next to arrows 2 and 3 and it is crucial that the system allows switching between both states. As shown in Figs. 3(b) and 3(d), the inductive feature produces a rise of the conductance, also called a resistive switching phenomenon, and a potentiation effect in the context of synapse behavior. In fact, the inductive rise of the current is associated with the *set* process, and the capacitive part with the *reset* process of the memristor. Additionally, in a different experiment, it was found that a sequence of positive pulses produces a progressive rise in conductance [Fig. 3(c)]. In summary, these phenomena confirm the properties outlined in Fig. 2 that permit the operation of the memristor as a synapse, in which the conductance can be modulated by the incoming voltage stimuli.[33]

Figure 4 shows the behavior of a very different system that consists of a membrane with conical nanopores that conduct ions in a fluid medium [Fig. 4(a)].[61,63–65] The *IV* curves, shown in Figs. 4(b), 4(c), and 4(e), yield the same self-crossing loops as those of Fig. 3(a), but here the experiments, performed at different cycling frequencies [Fig. 4(b)], allow observing additional features. While the curve at the lowest frequency (f = 0.01 Hz), which corresponds to stationary conditions, does not show hysteresis, the other cycles show loops with decreasing slope as the frequency increases. In fact, the system remains almost at the lowest conductance state when the cycle is performed at the highest frequency because in this case the cycling time is shorter than the characteristic relaxation time of the state variable (the conductance).[66] This is another intrinsic feature of an inductive system. Figure 4(d) shows the increase in conductivity produced by applying a train of positive voltage pulses, similarly to the experiment in the previous system [Fig. 3(c)]. These results show the sensitivity of the memristor to the frequency of the stimuli.

Furthermore, in Fig. 4 it is studied the behavior of the system when such pulses are applied in the capacitive region, i.e., with negative potential. In this case, the conductance progressively decreases, which enables to set the synapse weight at lower values when desired. Finally, another important feature of a memristor that appears in this system, because of the pore asymmetry, is a rectifying behavior. In addition, the inductive and capacitive sides and, therefore, the potentiation/depression loops can be exchanged with each other by modifying the pH of the solution[61] [Figs. 4(e) and 4(f)].

IV. NEUROMORPHIC MEMRISTOR BEHAVIOR

From the previous examples, we can extract the general properties required for a system to work as a neuromorphic element. A memristor is usually characterized as a system that obeys the following dynamical equations:[6,56,57]

$$I_{tot} = F(V, x), \tag{1}$$

$$\tau_k(V)\frac{dx}{dt} = h(V, x). \tag{2}$$

In Eq. (1), F is a conductivity function that describes the conduction current (I_{tot}) with respect to both the voltage V and a state or memory variable, x, which is necessary to determine the future behavior of the system when the present state and the inputs are known.[57] Equation (2) expresses that changes in the state variable x are controlled by an adaptation function $h(V, x)$ with the characteristic time τ_k. In equilibrium, we have an equilibration function $x_{eq}(V)$ defined by the condition $dx/dt = 0$,

$$h(V, x_{eq}) = 0. \tag{3}$$

As a concrete example, we now describe summarily a model validated experimentally in several types of memristors[58,66–69] and widely used in neuronal dynamics.[70,71] In this model, the memory variable $x = \sigma$ modulates the conductance state of the system in a range of values between two extremal conductance states, a minimum (g_L, $\sigma = 0$) and a maximum (g_H, $\sigma = 1$),[66,67]

$$I_{tot}(u) = [g_L + (g_H - g_L)\sigma]u + C_m\frac{du}{dt}, \tag{4}$$

$$\tau_k(u)\frac{d\sigma}{dt} = \sigma_{eq}(u) - \sigma. \tag{5}$$

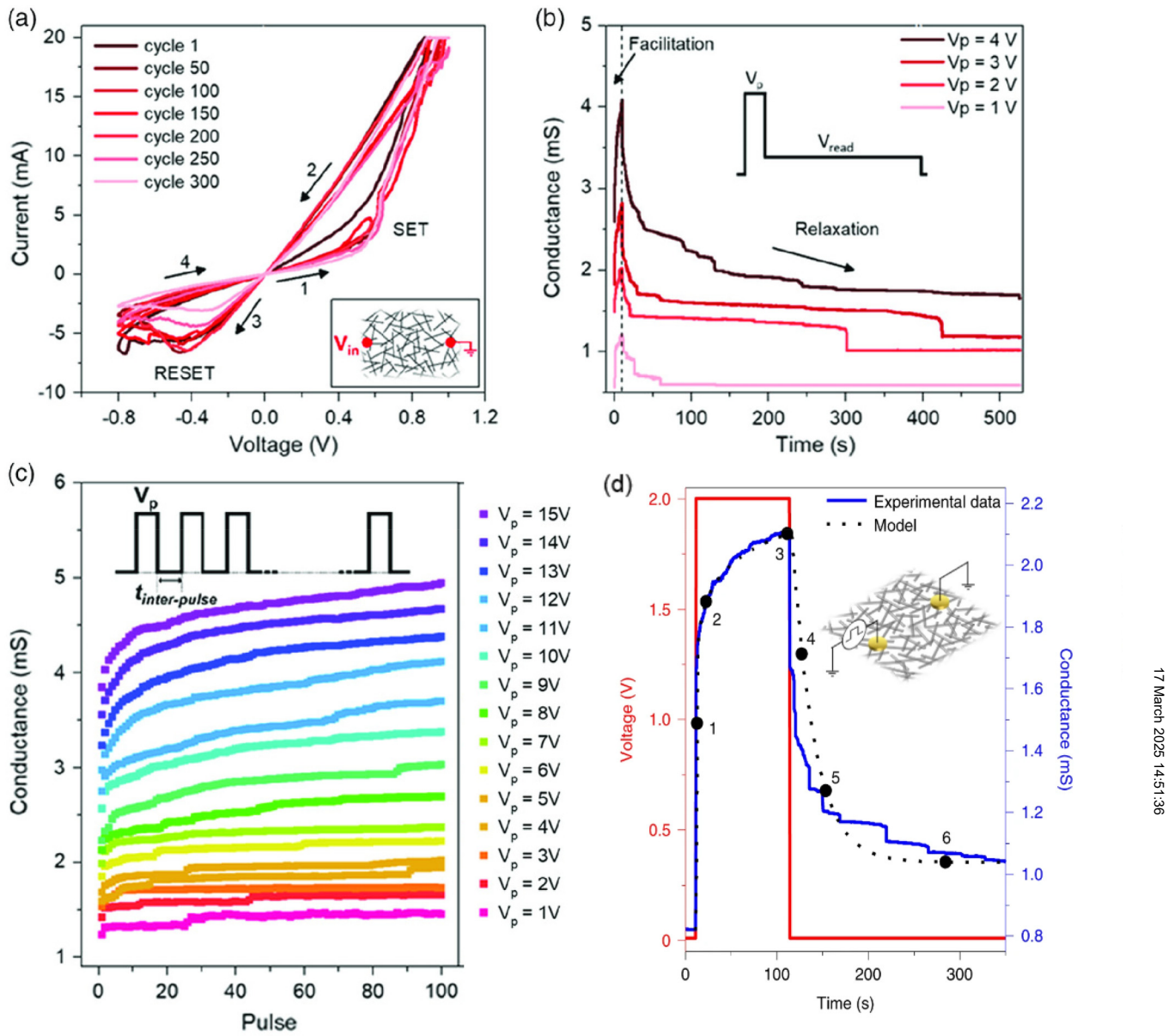

FIG. 3. Memristive response of a self-organized nanowires network. (a) Resistive switching behavior measured in a two-terminal configuration as schematized in the inset. (b) Gradual increase in conductance (synaptic facilitation) observed by applying a 10 s voltage pulse and subsequent conductance relaxation due to a volatile resistive switching behavior, read with a voltage of 50 mV. (c) Experimental demonstration of paired-pulse facilitation (PPF) with a gradual increase in conductance by stimulating the network with a train of 500 μs voltage pulses separated by 500 μs interpulse intervals. Reprinted with permission from G. Milano, G. Pedretti, M. Fretto, L. Boarino, F. Benfenati, D. Ielmini, I. Valov, and C. Ricciardi, Adv. Intell. Syst. **2**, 2000096 (2020). Copyright 2020 Author(s), licensed under a Creative Commons Attribution (CC BY) license. (d) Experimental and simulated potentiation and subsequent spontaneous relaxation of the effective conductance upon voltage pulse stimulation (2 V, 100 s) in a two-terminal configuration. Reprinted with permission from G. Milano, G. Pedretti, K. Montano *et al.*, Nat. Mater. **21**, 195–202 (2022). Copyright 2022 SNCSC.

The stationary properties of the model, i.e., the current–voltage, equilibrium function σ_{eq}, and relaxation time τ_k, are shown in Figs. 5(a) and 5(b). This is termed a conductance-activated quasilinear memristor (CALM) model.[69] In Fig. 5(c), we observe standard hysteresis loops with both inductive and capacitive parts (the orange line is at a larger frequency than the blue line). These loops are associated with the cycling of the memory variable shown in Fig. 5(d). In Figs. 5(e) and 5(f), we

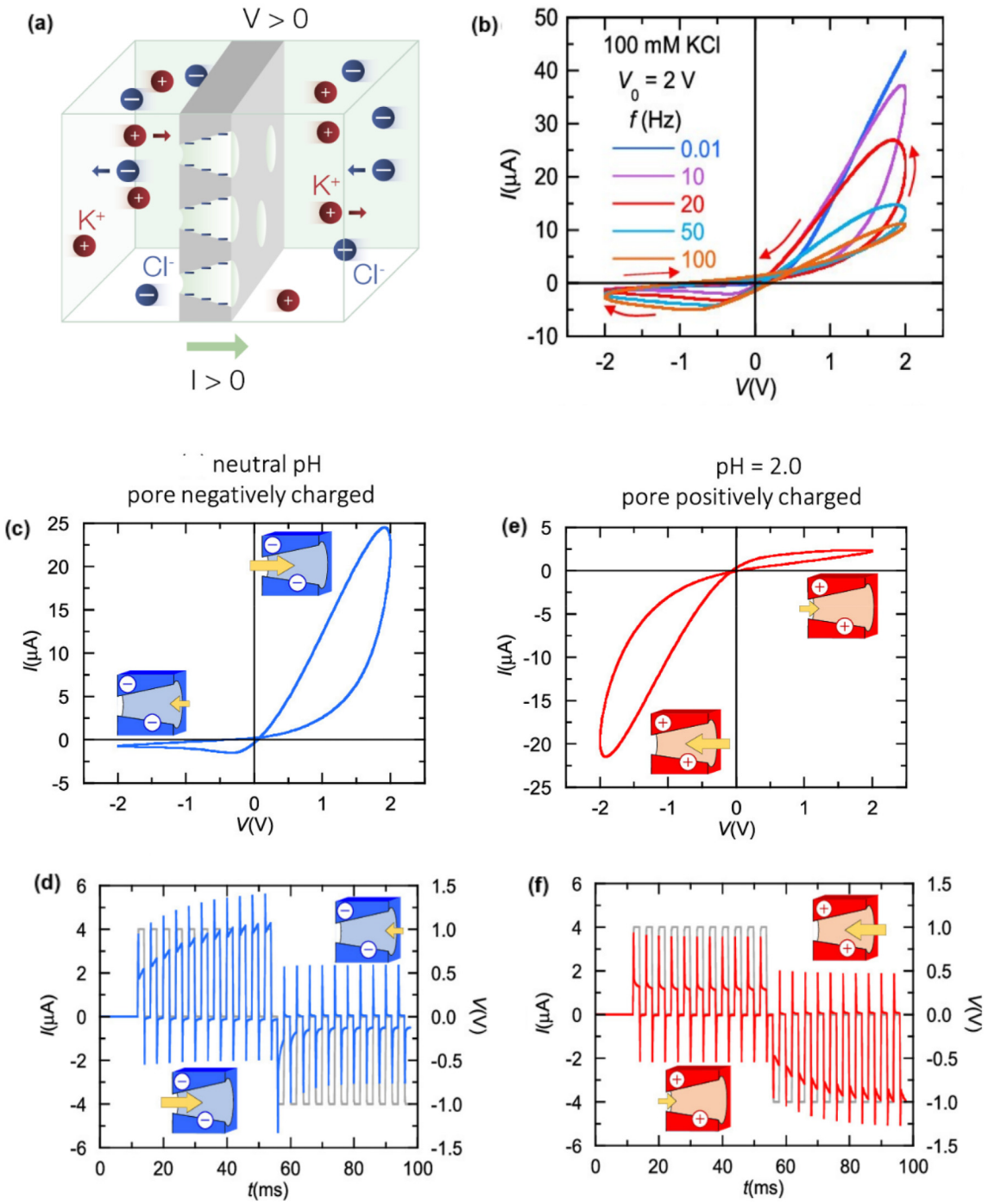

FIG. 4. (a) Ion conduction in a KCl solution through multipore polyethylene terephthalate (PET) membranes containing conical nanopores. (b) I–V curves in a 100 mM KCl solution at neutral pH, at different cycling frequencies with a voltage amplitude of 2 V. The arrows indicate the signal time evolution. (c) I–V curve of (b) corresponding to 10 Hz. (d) Current response to a sequence of 2 ms positive voltage pulses showing a gradual conductance potentiation followed by a sequence of negative voltage pulses, which reset the multipore membrane to the low conductance state for neutral pH. (e) and (f) Same experiments as (c) and (d), respectively, except for the pH = 2.0. Reprinted with permission from P. Ramirez, V. Gomez, J. Cervera, S. Mafe, and J. Bisquert, J. Phys. Chem. Lett. **14**, 10930–10934 (2023). Copyright 2023 American Chemical Society.

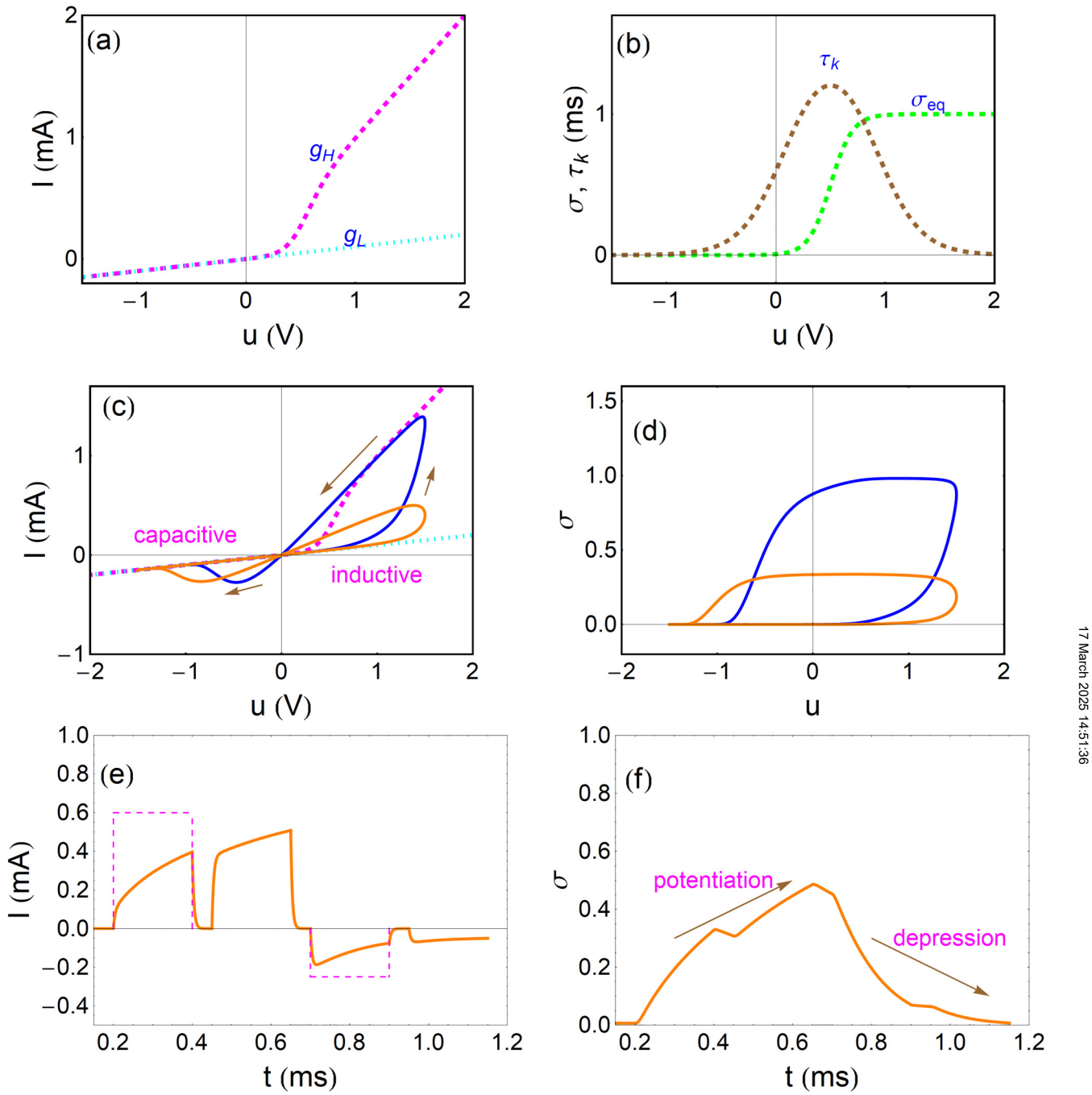

FIG. 5. A conductance-activated model. (a) Current–voltage curve (purple) indicating the low conductance branch (cyan). (b) Equilibrium value of the memory variable σ, and the relaxation time τ_k as a function of voltage. (c) Hysteresis in *IV* curves and (d) memory variable under sinusoidal stimulation $u = U_0 \sin(\Omega_s t)$ at amplitude $U_0 = 1.5$ V and different frequencies: Blue line $f_\Omega = 0.5$ Hz, orange line $f_\Omega = 5$ Hz. (c) Current–voltage loops. The straight lines are the dc (purple) and low (cyan) conductance. (d) σ-variable loops, indicating the σ_{eq} (green) and the relaxation time (brown). (e) Current in response to four voltage pulses applied to the model: (ΔV_+, ΔV_+, ΔV_-, ΔV_-) (outlined in dashed line). Transient parameters $V_0 = 0$ V, $\Delta V_+ = 1.2$ V, $\Delta V_- = -0.5$ V, $\Delta t_p = 0.2$ ms, $\Delta t_r = 0.05$ ms. (f) Memory variable. The model functions $\sigma_{eq} = 1/(1 + e^{-(u-V_{Bx})/V_m})$, $\tau_k^{-1} = \tau_M^{-1} + \tau_0^{-1}\left(\exp\left(\frac{u-V_A}{n_A V_m}\right) + \exp\left(-\frac{u-V_D}{n_D V_m}\right)\right)$. Model parameters $g_L = 0.1$ mS, $g_H = 1$ mS, $V_m = 0.1$ V, $\tau_0 = 1$ ms, $\tau_M = 1.5$ ms, $V_{Bx} = 0.5$ V, $V_A = 1$ V, $n_A = 2$, $V_D = 0$ V, $n_D = 2$.

observe that the model produces the potentiation at positive voltage and depression at negative voltage pulses.[67]

Based on the example of Fig. 5, we can obtain more general insights about memristor behavior. Consider an initial state $\sigma(V=0)=0$, with a current $I_{\text{fast}}=F(V,0)$. This is the branch of low conductance g_L in Fig. 5(a), which will be measured under a fast scan, as indicated in Fig. 5(c). But at slow scan velocity, the current becomes $I_{dc}=F(V_{\text{app}},\sigma_{\text{eq}}(V_{\text{app}}))>I_{\text{fast}}$. Since the current makes a transition from I_{fast} to a larger I_{dc}, as shown in the blue curve of Fig. 5(c), we can say that the system shows resistive switching from a low to a high conductance state.[72–74] This is a defining property of memristors when they are used for neuromorphic applications, as the synapses are required to obtain an increase in conductance under voltage pulses that represent the action potentials of adjacent neurons, as shown in Figs. 5(e) and 5(f).[11,12,25,33] The example of Fig. 5 represents a relatively fast relaxing memristor, where the gained conductance will be lost in a short time if the voltage stimulus is removed. This property enables a gradual potentiation of the synapse. On the other hand, the same approach can describe an abrupt and nonvolatile memristor, by changing the properties of the relaxation time.[69]

It is important to note that a memristor-like structure can provide other functionalities different from the ones shown so far.[40,64] For example, Fig. 6 shows hysteresis curves that are symmetric, showing capacitive loops at both sides. These structures are termed "complementary memristors."[75,76] They can be formed by two elementary neuromorphic memristors connected in antiseries, as then the high resistance side of each one prevails at both polarities,[77] hence the capacitive response. The complementary resistive switching is a useful solution to reduce the sneak current in a cross-bar memory without using any external component.[76,78,79]

Seen from another perspective, as the system of Eqs. (4) and (5) produces an increase in current, we can view it as an inductor element, as already discussed in connection to Fig. 3. This conclusion can also be obtained more generally from Eqs. (1) and (2) by studies of impedance spectroscopy of many systems that do *not* contain an electromagnetic inductor; hence, Eqs. (1) and (2) were termed a *chemical inductor*.[80] We have shown experimentally the inductive components in small signal ac impedance spectroscopy and their implications for neuromorphic responses in different specific systems.[58,66,81]

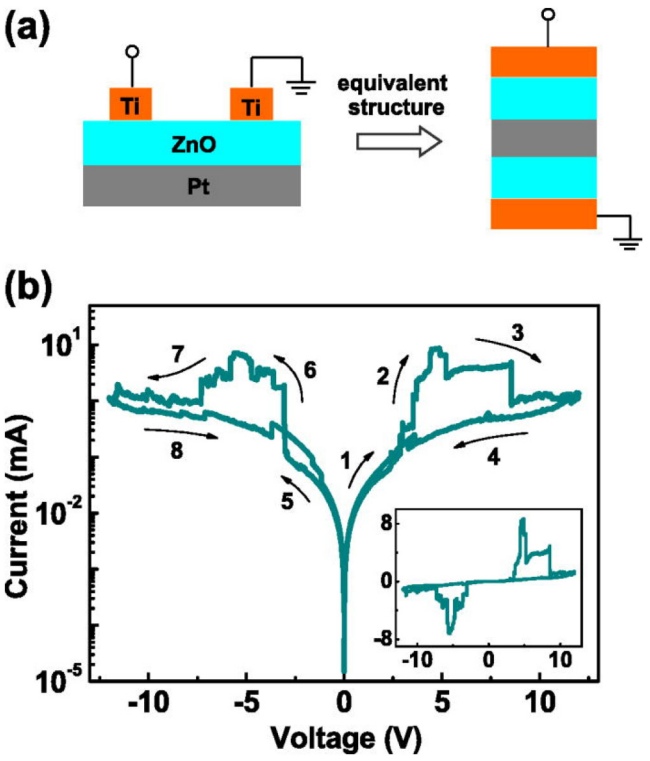

FIG. 6. (a) Complementary memristive device structure constructed by connecting two Ti/ZnO/Pt devices anti-serially. (b) Typical I–V characteristics of such a complementary structure. The inset shows the curves on a linear scale. Reproduced with permission from J. Wang, R. Pan, H. Cao, Y. Wang, L. Liang, H. Zhang, J. Gao, and F. Zhuge, Appl. Phys. Lett. **109**, 143505 (2016). Copyright 2016 AIP Publishing LLC.

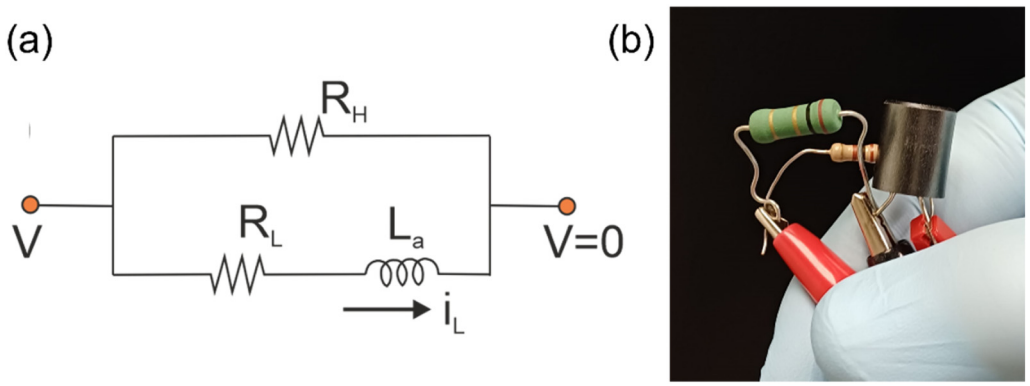

FIG. 7. (a) Scheme of an inductive circuit and (b) photo of the circuit.

Based on this understanding, in Sec. V, we show that the memristors contain an inductive mechanism that is the heart of resistive switching. To prove this, we will develop circuits based on elementary two-contact components, to progressively build the standard memristor responses in *IV* curves and potentiation/depression features.

V. THE INDUCTIVE CIRCUIT

We have found that the rise of the conductance with time under an applied voltage is a defining characteristic of neuromorphic memristors. We aim to build such a process with elementary circuit elements. We first propose a two-branch circuit, Fig. 7(a), in which the current starts at a high resistance R_H. A low-resistance branch R_L is activated over time by the inductor L_a.

Using Kirchoff rules, we obtain the equations

$$I_{tot} = \frac{V}{R_H} + i_L, \tag{6}$$

$$\tau_L \frac{di_L}{dt} = \frac{V}{R_L} - i_L. \tag{7}$$

Here, the inductor characteristic time is

$$\tau_L = \frac{L_a}{R_L}. \tag{8}$$

Equations (6) and (7) clearly realize the general conditions (1) and (2). The memory variable $x = i_L$ is the current in the inductor branch. The equilibration function is $i_{L,eq} = V/R_L$. The fast current and stationary dc current are

$$I_{\text{fast}} = \frac{V}{R_H}, \tag{9}$$

$$I_{dc} = \left(\frac{1}{R_H} + \frac{1}{R_L}\right) V. \tag{10}$$

The simulated responses of the inductive circuit of Fig. 7(a) are shown in Figs. 8(a)–8(c). In order to achieve hysteresis effects, the voltage is swept at a constant angular frequency Ω_s ($f_\Omega = \Omega_s/2\pi$) as follows:

$$V = U_0 \sin(\Omega_s t). \tag{11}$$

Figure 8(a) shows the stabilization of a counterclockwise *IV* Lissajous type loop, at a frequency of 50 Hz, from the starting point (V = 0 V and I = 0 mA) when the perturbation is connected. At the initial stage, the system is in the low conductance state and the *IV* curve (dashed blue line) follows the dashed purple line consequently. However, after the dynamic cycling has been established (continuous blue line), the curves do not follow either the low (purple) or the high conduction (green) line. Figure 6(b) shows *IV* curves at two extreme frequency regimes: 500 and 5 Hz (orange and green continuous lines, respectively). These occur according to a low conductance state (dashed purple line) where the current is

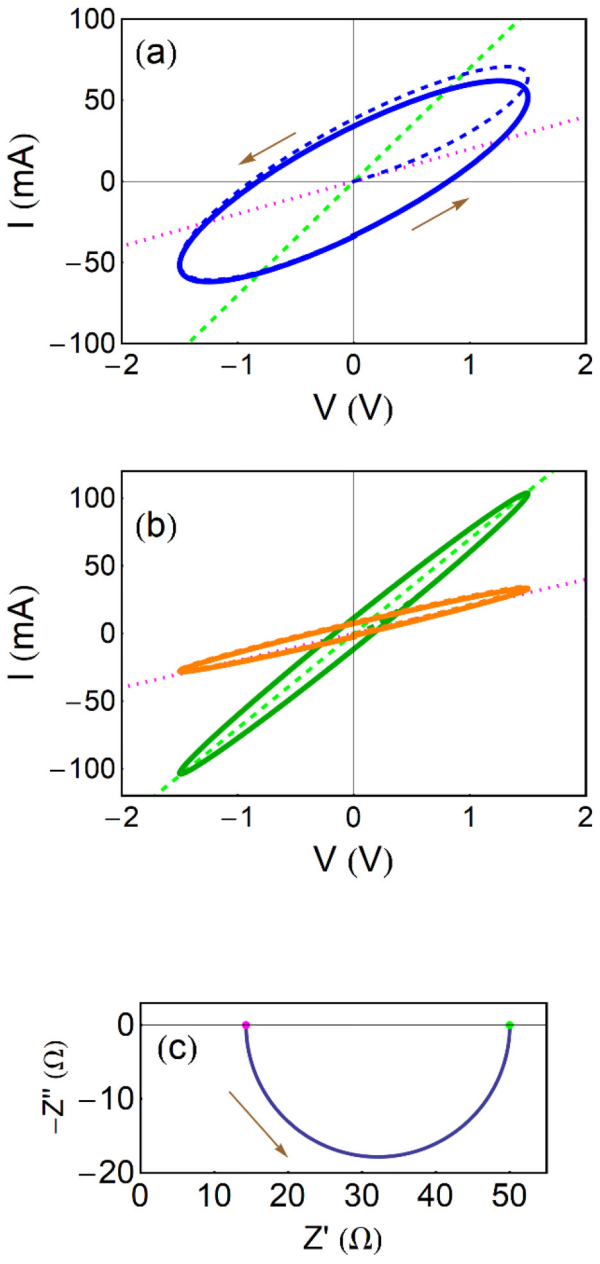

FIG. 8. Simulated response of the inductor circuit of Fig. 5(a) with parameters: $R_L = 20\ \Omega$, $R_H = 50\ \Omega$, $L_a = 0.1\ H$, $\tau_L = 5$ ms, under sinusoidal stimulation ($V = V_0 \sin(\Omega_s t)$, $V_0 = 1.5$ V) at different frequencies ($f_\Omega = \Omega_s/2\pi$). (a) *IV* curves at $f_\Omega = 500$ Hz (orange line) and at $f_\Omega = 5$ Hz (green line) illustrating the two conductance states of the circuit. The arrows indicate the direction of the cycles, and the straight dashed lines correspond to I_{fast} (purple) and I_{dc} (green). (b) *IV* curve at $f_\Omega = 50$ Hz from the first stages (dashed blue line) and after the dynamic cycling has been established (continuous blue line). The straight dashed lines corresponding to the two conductance states have been plotted. (c) Circuit impedance (Z) at varying frequency from Eq. (12) in the complex plane. The arrow indicates the direction of increasing frequency. The magenta point corresponds to Z(0) and the green point to Z(∞).

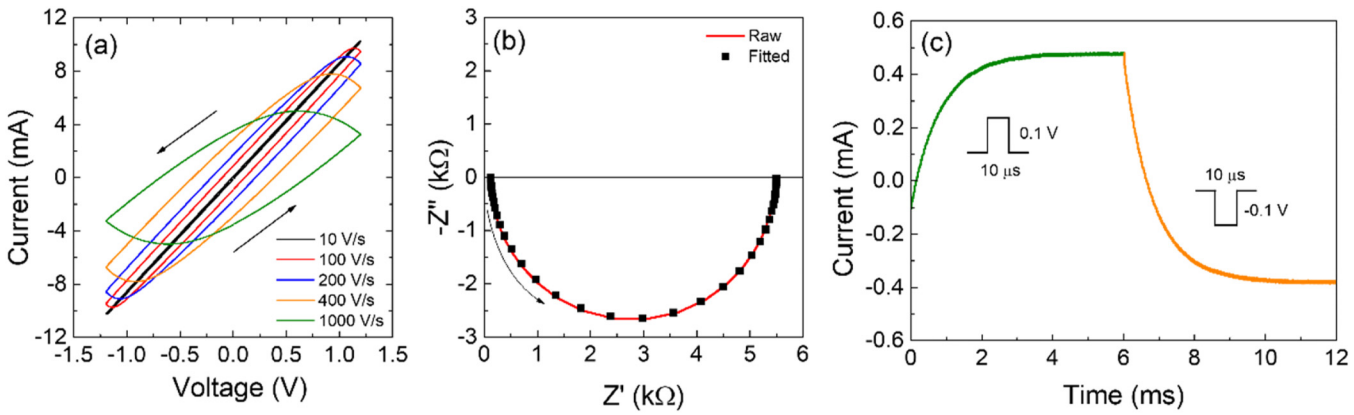

FIG. 9. Measured response of the inductor circuit of Fig. 5(a), with parameters: $R_L = 100\ \Omega$, $R_H = 5600\ \Omega$, $L_a = 0.1$ H (internal resistance 18.5 Ω), $\tau_L = 0.84$ ms. (a) *IV* curves at different scan rates s ($V = st$) with amplitude $U_0 = \pm 1.2$ V and initial condition $V_0 = 0$. (b) Impedance response scanned in the frequency range from 0.01 to 10^5 Hz (the arrow indicates the direction of increasing frequency). (c) Potentiation characteristic response measured by applying pulse trains of $V_{pulse} = +0.1$ V (green curve) and $V_{pulse} = -0.1$ V (orange curve) with a pulse width and separation of 10 μs and $V_{read} = +0.01$ V.

I_{fast} [Eq. (7)] for the high cycling rates (short measurement times) and according to a high conductance state (dashed green line) where current is I_{dc} [Eq. (8)] for the low cycling frequency (long measurement times).

The ac impedance response of Eqs. (6) and (7) at angular frequency ω is given by the function

$$Z = \left(\frac{1}{R_H} + \frac{1}{R_L}\frac{1}{1 + i\,\tau_L\omega}\right)^{-1}. \tag{12}$$

As shown in Fig. 8(c), Eq. (12) produces a semicircle in the fourth quadrant of the complex plane, typical of an inductive behavior (also termed a negative capacitance feature).

Measurements on the inductive circuit of Fig. 7(a) were carried out under the same scheme as that used for simulations but with different circuit parameters (see the caption of Fig. 9). The obtained *IV* curves, realized at different scan rates or frequencies, confirmed the counterclockwise Lissajous loops [Fig. 9(a)] with a narrow loop at the lowest studied frequency corresponding to a high conductance state (black line) and other loops whose width and slope increase and decrease, respectively, with increasing frequency. However, a clear low conductance state with a narrow loop and a small slope was not achieved because of experimental limitations of the measuring apparatus. The impedance response [Fig. 9(b)] also showed a negative arc, which is consistent with the equations of the model [Eq. (10)] for the inductive circuit. In addition, and most importantly, the synaptic potentiation/depression characteristics were investigated by applying trains of +0.1 V pulses of 10 μs of duration and separation, well below the circuit relaxation time followed by a similar train but with −0.1 V of height [see green and orange curves, respectively, in Fig. 9(c)]. It is important to stress that a rise of current is observed, at both positive and negative voltage trains, as expected because of the circuit symmetry. Therefore, only synaptic potentiation can be achieved with the inductive circuit of Fig. 7(a).

VI. THE CAPACITIVE CIRCUIT

The circuit of Fig. 7(a) presents a typical synaptic *set* process. However, the electrical response is fully symmetrical with respect to voltage V, i.e., it produces the same conductance change with both polarities. Thus, the only way to switch from low to high conductance states or vice versa is to apply different stimulation times. But, this is not acceptable with regard to the practical functioning of a neuromorphic device. We have seen that the *IV* cycles of the neuromorphic memristors of Figs. 2–4 include not only counterclockwise but also clockwise loops that produce a decrease in conductance. Therefore, a more effective *reset* mechanism is required. Clockwise loops can be produced with capacitive elements. For this reason, we have studied the behavior of a circuit like that of Fig. 10.

Using Kirchoff rules, in the same way as in the inductive circuit, we obtain the equations

$$I_{tot} = \left(\frac{1}{R_H} + \frac{1}{R_L}\right)V - \frac{u}{R_L}, \tag{13}$$

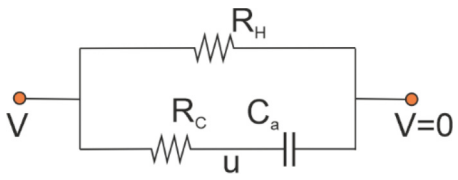

FIG. 10. Scheme of a capacitive circuit.

$$\tau_C \frac{du}{dt} = V - u. \tag{14}$$

Here, the capacitor characteristic time is

$$\tau_C = R_C C_a. \tag{15}$$

However, unlike the inductive circuit, here the equivalent state variable of Eqs. (1) and (2) is the voltage, $x = u$, across the resistance R_C, the equilibration function is $u_{eq} = V$, and the fast and dc currents are

$$I_{\text{fast}} = \left(\frac{1}{R_H} + \frac{1}{R_C}\right) V, \tag{16}$$

$$I_{dc} = \frac{V}{R_H}. \tag{17}$$

In contrast with the inductive circuit, here the cycling starts at the high conductance branch [Fig. 11(a)], producing clockwise loops and high/low conductance states are achieved at high/low frequencies, respectively [Fig. 11(b)]. In addition, the ac impedance can be calculated from the function

$$Z = \left(\frac{1}{R_H} + \frac{1}{R_L}\frac{1}{1 + \frac{1}{i\,\tau_C \omega}}\right)^{-1}. \tag{18}$$

In this case, it yields an arc in the first quadrant [Fig. 11(c)].

The capacitive circuit of Fig. 10 was studied experimentally in a similar way as the inductive circuit, Fig. 12, with circuit parameters detailed in the figure caption. The *IV* curves confirmed the appearance of clockwise loops with increasing width as the scan rate increases [Fig. 12(a)], and the impedance response showed a positive arc. The capacitive circuit produces the features of the reset process and synaptic depression, i.e., a conductance decrease with applying positive or negative voltage pulses [Fig. 12(c)], which are obtained at negative voltages in Figs. 3 and 4.

In summary, capacitive and inductive circuits differ in what concerns phase relationships, impedance, and time-domain current responses. The properties of both circuits are summarized in Fig. 13.[53]

VII. THE RECTIFIER CIRCUITS

As we have seen in Secs. V and VI, our preliminary inductive and capacitive circuits in Figs. 7 and 10 provide voltage symmetric response, hence by applying voltage pulses they provoke exclusively potentiation or depression (conductance increase or decrease, respectively), no matter the polarity of the pulses. Clock- and counterclockwise loops cannot be obtained in the same circuit in *IV* scan measurements as they occur in real neuromorphic systems (Figs. 3 and 4). This is because they lack an onset gating variable as the σ shown in Fig. 5, which occurs in most physical memristors, causing rectification (the current increase is much larger in one of the polarities).[5,66,71]

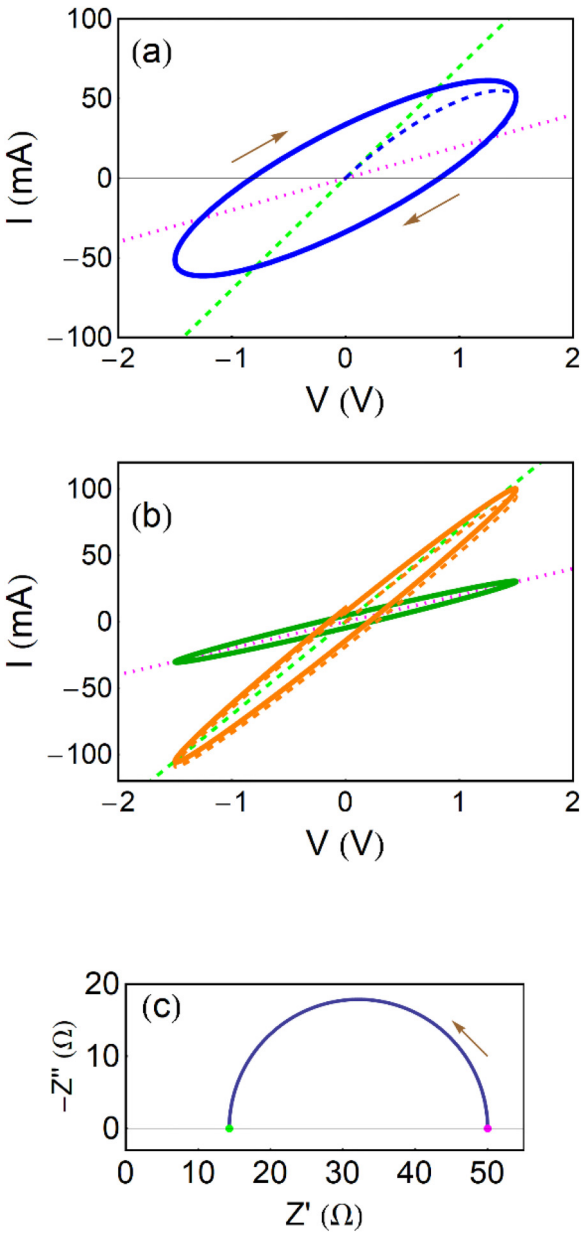

FIG. 11. Simulated response of the capacitive circuit of Fig. 8 with parameters: $R_L = 20\ \Omega$, $R_H = 50\ \Omega$, $C_a = 0.1$ mF, $\tau_C = 2$ m, under sinusoidal stimulation [$u = U_0 \sin(\Omega_s t)$ where $U_0 = 1.5$ V] at different frequencies ($f_\Omega = \Omega_s/2\pi$). (a) *IV* curves at $f_\Omega = 500$ Hz (orange line) and at $f_\Omega = 5$ Hz (green line) illustrating the two conductance states of the circuit. The arrows indicate the direction of the cycles, and the straight dashed lines correspond to I_{fast} (green) and I_{dc} (purple). (b) *IV* curve at $f_\Omega = 50$ Hz from the first stages with initial condition $U_0 = 0$ V (dashed blue line) and after the dynamic cycling has been established (continuous blue line). The straight dashed lines corresponding to the two conductance states have been plotted. (c) Circuit impedance (Z) at varying frequency from Eq. (18) in the complex plane. The arrow indicates the direction of increasing frequency. The magenta point corresponds to Z(0) and the green point to Z(∞).

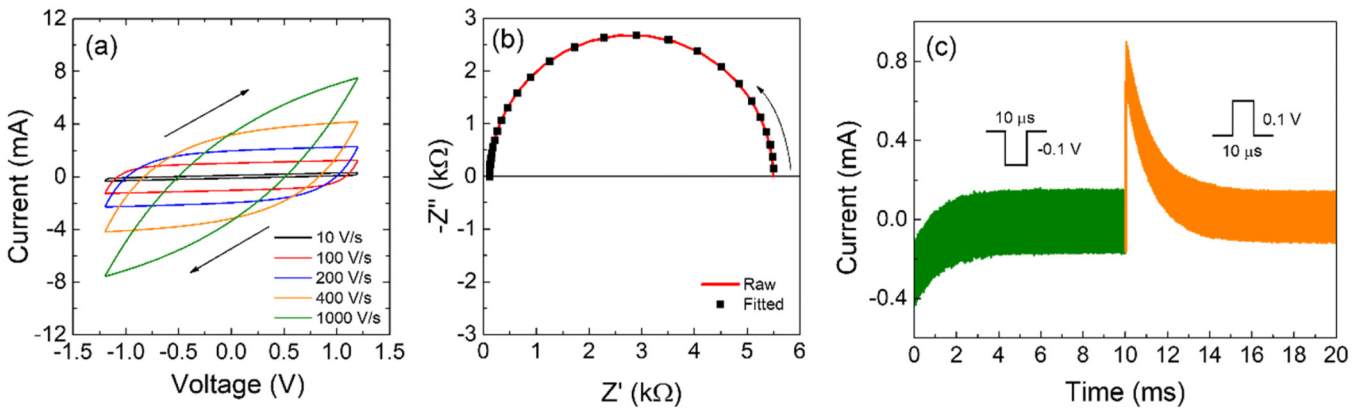

FIG. 12. Measured response of the capacitive circuit of Fig. 8, with parameters: $R_L = 120\ \Omega$, $R_H = 5600\ \Omega$, $C_a = 10\ \mu F$, $\tau_C = 1.20$ ms. (a) *IV* curves at different scan rates s ($V = st$) from 10 V/s (black, slow) to 1000 V/s (green, fast) at amplitude $U_0 = \pm 1.2$ V. Initial condition $V_0 = 0$. (b) Impedance response scanned in the frequency range from 0.01 to 10^5 Hz. (c) Depression characteristic response measured by applying pulses trains of $V_{pulse} = -0.1$ V (green curve) and $V_{pulse} = +0.1$ V (orange curve) with a pulse width and separation of 10 μs and $V_{read} = +0.01$ V.

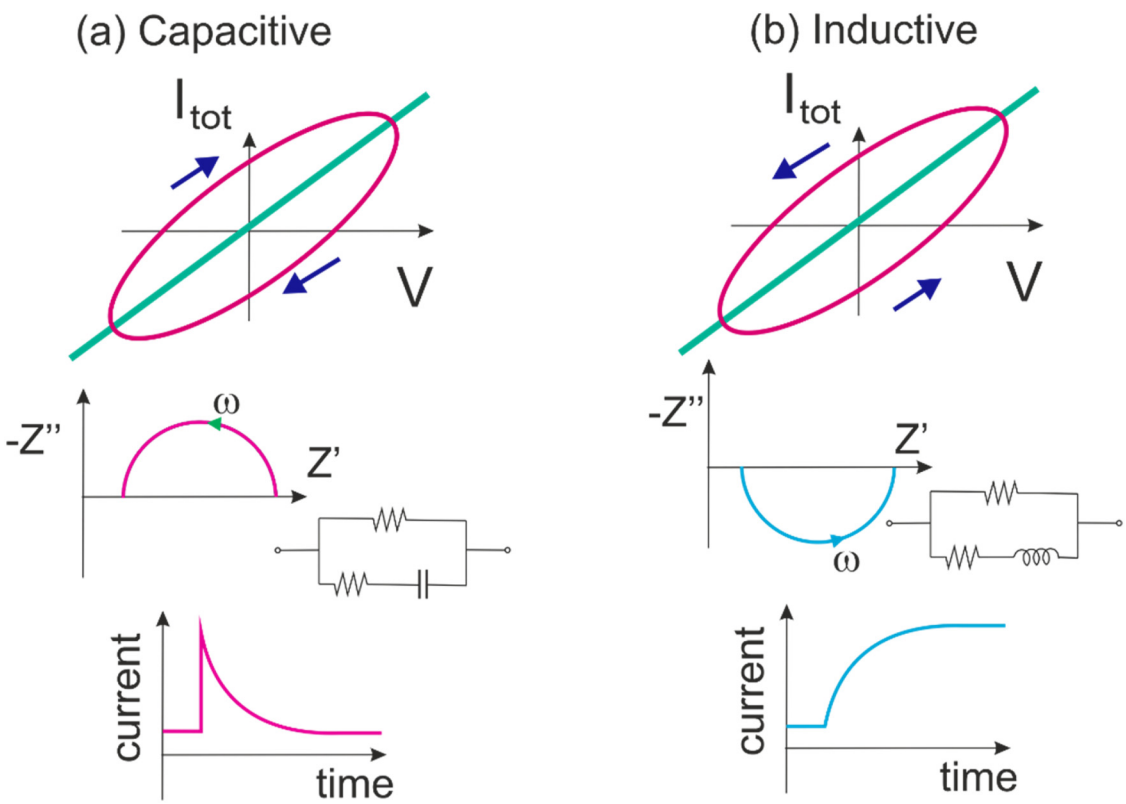

FIG. 13. Summary of hysteresis, impedance, and time transient response in (a) capacitive and (b) inductive circuits.

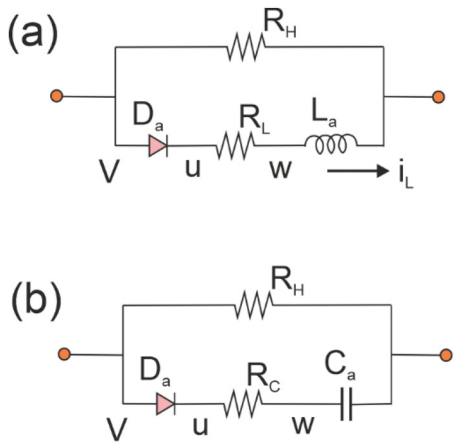

FIG. 14. The inductive (a) and capacitive (b) circuits of Figs. 7 and 10 including each respective rectifier diode.

To approximate the gating variable, we introduce a diode in Fig. 14(a) that provides the current–voltage relation

$$i_L = i_0\left(e^{\frac{V-u}{V_m}} - 1\right), \tag{19}$$

where i_0, V_m are constants. For the lower branch, we obtain the equation

$$V = L_a\frac{di_L}{dt} + R_L i_L + V_m ln\left(1 + \frac{i_L}{i_0}\right). \tag{20}$$

The resistance in the lower branch is

$$R_{DL} = R_L + R_D, \tag{21}$$

where the resistance of the diode is

$$R_D = \frac{V_m}{i_0 + i_L}. \tag{22}$$

To investigate the rectifying characteristics in the real circuit systems with diode element, the inductor-diode circuit system (Fig. 15) and capacitor-diode circuit system (Fig. 16) were executed with the same configuration as Fig. 14.

Figure 15 shows the *IV* curves with different scan rates and potentiation/depression responses in one of the rectifying circuits [Fig. 14(a)]. By adding a diode to the inductor circuit covered in Figs. 7–9, the existing inductive current-flow direction is maintained as the counterclockwise loop [Fig. 8(a)] in the scanned positive region, and the rectifying characteristics are represented in the negative region, confirming that the diode element leads to the rectifier circuit. The faster the scan rate is swept, the lower the conductance line, such as the *IV* hysteresis characteristics of inductive circuit [Fig. 8(b)]. Subsequently, the observed neuromorphic devices' main characteristics, potentiation, and depression were scanned with positive and negative pulses, and it can be confirmed that only potentiation occurs in the positive pulses and there is no

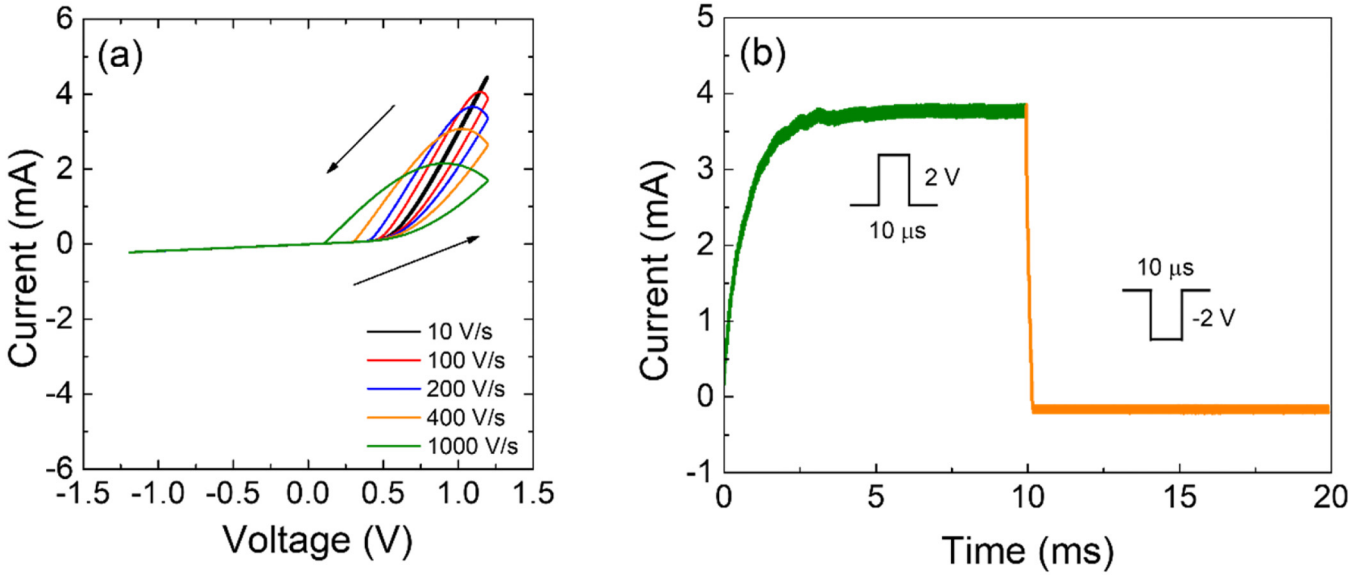

FIG. 15. Experimental inductive circuit including a rectifier diode element: (a) *IV* curves of the rectifying circuit with different scan rates from 10 V/s (black, slow) to 1000 V/s (green, fast) at amplitude $U_0 = \pm 1.2$ *V*. Initial condition $V_0 = 0$. (b) Potentiation characteristic response measured at $V_{pulse} = +2.0$ V (green) and $V_{pulse} = -2.0$ V (orange) with a pulse width of 10 μs at $V_{read} = +0.20$ V. For this experimental inductor circuit, circuit parameters of $R_L = 100\ \Omega$, $R_H = 5600\ \Omega$, $L_a = 0.1$ H (internal resistance 18.5 Ω) and diode (1*N*4148) were used.

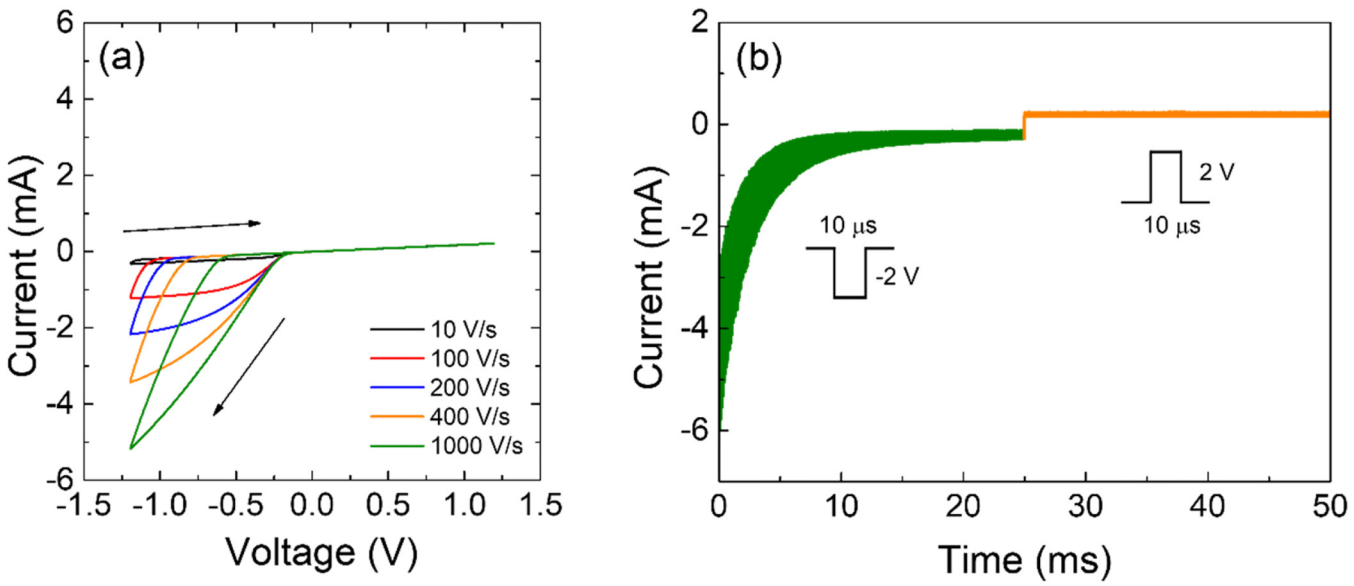

FIG. 16. Experimental capacitive circuit including a rectifier diode element: (a) *IV* curves of the capacitive circuit with different scan rates from 10 V/s (black, slow) to 1000 V/s (green, fast) at amplitude $U_0 = \pm 1.2$ V. Initial condition $V_0 = 0$. (b) Depression characteristic response measured at $V_{pulse} = -2.0$ V (green) and $V_{pulse} = +2.0$ V (orange) with a pulse width of 10 μs at $V_{read} = +0.20$ V. For this experimental capacitor circuit, the circuit parameters of $R_C = 120\ \Omega$, $R_H = 5600\ \Omega$, $C_a = 10\ \mu F$ and diode(1*N*4148)were used.

conductance change in the negative pulses. This approach based on diodes can reproduce only volatile memristor characteristics. The diode element determines the onset voltage, and the other elements establish the hysteresis properties.

To express the rectifying properties occurring at the opposite side, this time, the rectifier diode element was added to the capacitive circuit (Fig. 10) in Fig. 14(b) and the *IV* characteristics are shown in Fig. 16. *IV* curves were scanned from 10 V/s (black, slow) to 1000 V/s (green, fast) at amplitude $U_0 = \pm 1.2$ V, where the circuit with a diode element leads to the rectifying characteristics with the clockwise current flowing loops [Fig. 11(a)]. The faster scanned *IV* loop appears with a high conductance range, which is the same aspect described in Fig. 11(b). Similar to Fig. 15, the conductance change of the circuit composed of the capacitor and the rectifier diode was found only at the opposite voltage polarity in the potentiation/depression characteristics in Fig. 16(b), showing neuromorphic characteristics with conductivity changes only at the pulse of −2.0 V and no conductivity changes at the positive pulse given +2.0 V.

Having seen the behavior of inductive and capacitive circuits the question now is if it is possible to build, by a combination of both, an electrical circuit that behaves as the neuromorphic devices of Figs. 2–4. We have found that this can be realized by using rectifying elements placed appropriately. The circuit of Fig. 17 is an example that includes two antiparallel rectifying diodes where inductive and capacitive loops occur in different branches.

Figure 18(a) shows the measured *IV* characteristics of the circuit of Fig. 17 with parameters indicated in the figure caption. At the positive polarity, the *IV* curves follow counterclockwise loops while at the negative polarity, they follow clockwise loops. Different scan rates following the voltage cycle: 0 V → + 1.2 V → 0 V → −1.2 V → 0 V, were studied, from 10 to 1000 V/s, and they produced a conductance change that increased with the scan speed. In addition, the potentiation–depression characteristics were successfully obtained [Fig. 18(b)], by applying a train of positive voltage pulses [$V_{pulse} = +2.0$ V (green part)] of 10 μs of width and separation, followed by a similar train but with $V_{pulse} = -2.0$ V (orange part), leading to an increase and decrease in conductance, respectively.

In summary, it has been demonstrated that a memristive behavior can be achieved from electrical circuits composed of inductors, capacitors, rectifier diodes, and resistors. This confirms the view that a memristor can be constructed from more elementary parts.[82] We do not claim, however, that any material

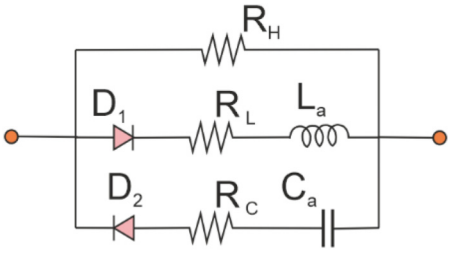

FIG. 17. Capacitive–inductive circuit including two rectifier diode elements.

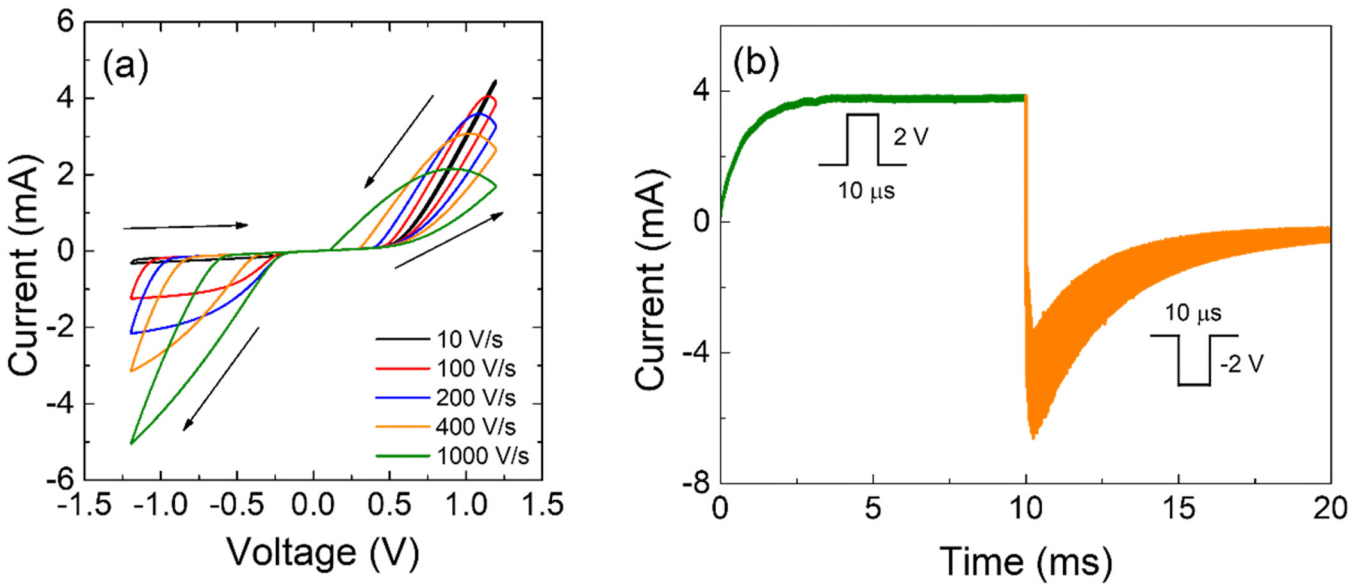

FIG. 18. Measurements performed on the electrical circuit of Fig. 17, with parameters: $R_H = 5600\ \Omega$, $R_L = 100\ \Omega$, $L_a = 0.1$ H (internal resistance 18.5 Ω), $R_C = 120\ \Omega$, $C_a = 10\ \mu F$, and diode(1*N*4148). (a) *IV* curves at different scan rates from 10 V/s (black, slow) to 1000 V/s (green, fast) with voltage amplitudes: $U_0 = \pm 1.2$ V and the positive and negative polarization regions, respectively. Initial condition $V_0 = 0$. (b) Potentiation–depression characteristic response measured with applying pulses trains of $V_{pulse} = +2.0$ V (green) and $V_{pulse} = -2.0$ V (orange) with pulse width and separation of 10 μs and $V_{read} = +0.20$ V.

memristor can be reproduced from such elements, as physical memristors contain a wide variety of physical mechanisms (such as the conductance activation mechanism in Fig. 5) that cannot be reduced to the combined response of basic elements.[34]

VIII. CONCLUSION

The *IV* characteristics with clockwise and counterclockwise loops, as well as the potentiation/depression response of typical memristors based on a single memory variable, have been reproduced by a relatively simple electrical circuit that includes resistors, inductance, capacitance, and rectifying elements. This work clarifies the electrical properties of a memristor by showing the necessary components to obtain the characteristic behavior that can be applied in neuromorphic circuits.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

So-Yeon Kim: Conceptualization (equal); Data curation (equal); Writing – original draft (equal); Writing – review & editing (equal). **Heyi Zhang:** Conceptualization (equal); Data curation (equal). **Gonzalo Rivera-Sierra:** Data curation (equal); Investigation (equal). **Roberto Fenollosa:** Conceptualization (equal); Investigation (equal). **Jenifer Rubio-Magnieto:** Conceptualization (equal); Investigation (equal). **Juan Bisquert:** Conceptualization (equal); Funding acquisition (lead); Writing – original draft (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data presented here can be accessed at https://doi.org/10.5281/zenodo.14184296 (Zenodo) under the license CC-BY-4.0 (Creative Commons Attribution-ShareAlike 4.0 International).

REFERENCES

[1]A. Mehonic, D. Ielmini, K. Roy, O. Mutlu, S. Kvatinsky, T. Serrano-Gotarredona, B. Linares-Barranco, S. Spiga, S. Savel'ev, A. G. Balanov, N. Chawla, G. Desoli, G. Malavena, C. Monzio Compagnoni, Z. Wang, J. J. Yang, S. G. Sarwat, A. Sebastian, T. Mikolajick, S. Slesazeck, B. Noheda, B. Dieny, T.-H. Hou, A. Varri, F. Brückerhoff-Plückelmann, W. Pernice, X. Zhang, S. Pazos, M. Lanza, S. Wiefels, R. Dittmann, W. H. Ng, M. Buckwell, H. R. J. Cox, D. J. Mannion, A. J. Kenyon, Y. Lu, Y. Yang, D. Querlioz, L. Hutin, E. Vianello, S. S. Chowdhury, P. Mannocci, Y. Cai, Z. Sun, G. Pedretti, J. P. Strachan, D. Strukov, M. Le Gallo, S. Ambrogio, I. Valov, and R. Waser, "Roadmap to neuromorphic computing with emerging technologies," APL Mater. **12**, 109201 (2024).

[2]Z. Wang, S. Joshi, S. Savel'ev, W. Song, R. Midya, Y. Li, M. Rao, P. Yan, S. Asapu, Y. Zhuo, H. Jiang, P. Lin, C. Li, J. H. Yoon, N. K. Upadhyay, J. Zhang, M. Hu, J. P. Strachan, M. Barnell, Q. Wu, H. Wu, R. S. Williams, Q. Xia, and J. J. Yang, "Fully memristive neural networks for pattern classification with unsupervised learning," Nat. Electron. **1**, 137–145 (2018).
[3]J. J. Yang, D. B. Strukov, and D. R. Stewart, "Memristive devices for computing," Nat. Nanotechnol. **8**, 13–24 (2013).
[4]G. Indiveri and S.-C. Liu, "Memory and information processing in neuromorphic systems," Proc. IEEE **103**, 1379–1397 (2015).
[5]L. Gao, Q. Ren, J. Sun, S.-T. Han, and Y. Zhou, "Memristor modeling: Challenges in theories, simulations, and device variability," J. Mater. Chem. C **9**, 16859–16884 (2021).
[6]J. B. Roldán, E. Miranda, D. Maldonado, A. N. Mikhaylov, N. V. Agudov, A. A. Dubkov, M. N. Koryazhkina, M. B. González, M. A. Villena, S. Poblador, M. Saludes-Tapia, R. Picos, F. Jiménez-Molinos, S. G. Stavrinides, E. Salvador, F. J. Alonso, F. Campabadal, B. Spagnolo, M. Lanza, and L. O. Chua, "Variability in resistive memories," Adv. Intell. Syst. **5**, 2200338 (2023).
[7]L. Chua, "Memristor-The missing circuit element," IEEE Trans. Circuit Theory **18**, 507–519 (1971).
[8]D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," Nature **453**, 80–83 (2008).
[9]Z. Wang, S. Joshi, S. E. Savel'ev, H. Jiang, R. Midya, P. Lin, M. Hu, N. Ge, J. P. Strachan, Z. Li, Q. Wu, M. Barnell, G. L. Li, H. L. Xin, R. S. Williams, Q. Xia, and J. J. Yang, "Memristors with diffusive dynamics as synaptic emulators for neuromorphic computing," Nat. Mater. **16**, 101–108 (2017).
[10]S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale memristor device as synapse in neuromorphic systems," Nano Lett. **10**, 1297–1301 (2010).
[11]T. Serrano-Gotarredona, T. Masquelier, T. Prodromakis, G. Indiveri, and B. Linares-Barranco, "STDP and STDP variations with memristors for spiking neuromorphic learning systems," Front. Neurosci. **7**, 2 (2013).
[12]T. Ohno, T. Hasegawa, T. Tsuruoka, K. Terabe, J. K. Gimzewski, and M. Aono, "Short-term plasticity and long-term potentiation mimicked in single inorganic synapses," Nat. Mater. **10**, 591–595 (2011).
[13]M. A. Zidan, J. P. Strachan, and W. D. Lu, "The future of electronics based on memristive systems," Nat. Electron. **1**, 22–29 (2018).
[14]S. Y. Kim, J. M. Yang, E. S. Choi, and N. G. Park, "Layered $(C_6H_5CH_2NH_3)_2CuBr_4$ perovskite for multilevel storage resistive switching memory," Adv. Funct. Mater. **30**, 1–9 (2020).
[15]T. K. Su, W. K. Cheng, C. Y. Chen, W. C. Wang, Y. T. Chuang, G. H. Tan, H. C. Lin, C. H. Hou, C. M. Liu, Y. C. Chang, J. J. Shyue, K. C. Wu, and H. W. Lin, "Room-temperature fabricated multilevel nonvolatile lead-free cesium halide memristors for reconfigurable in-memory computing," ACS Nano **16**, 12979–12990 (2022).
[16]S. Y. Kim, D. A. Park, and N. G. Park, "Synthetic powder-based thin (<0.1 μm) $Cs_3Bi_2Br_9$ perovskite films for air-stable and viable resistive switching memory," ACS Appl. Electron. Mater. **4**, 2388–2395 (2022).
[17]G. Pedretti and D. Ielmini, "In-memory computing with resistive memory circuits: Status and outlook," Electronics **10**, 1063 (2021).
[18]P. Mannocci, M. Farronato, N. Lepri, L. Cattaneo, A. Glukhov, Z. Sun, and D. Ielmini, "In-memory computing with emerging memory devices: Status and outlook," APL Mach. Learn **1**, 010902 (2023).
[19]J. Q. Yang, R. Wang, Z. P. Wang, Q. Y. Ma, J. Y. Mao, Y. Ren, X. Yang, Y. Zhou, and S. T. Han, "Leaky integrate-and-fire neurons based on perovskite memristor for spiking neural networks," Nano Energy **74**, 104828 (2020).
[20]J. Chen, Y. Lu, Z. Yang, Y. Li, and X. Miao, "Neuromorphic devices based on chalcogenide materials," in *Neuromorphic Devices for Brain-Inspired Computing* (Wiley, 2022), pp. 125–147.
[21]Y. Kim, Y. J. Kwon, D. E. Kwon, K. J. Yoon, J. H. Yoon, S. Yoo, H. J. Kim, T. H. Park, J.-W. Han, K. M. Kim, and C. S. Hwang, "Nociceptive memristor," Adv. Mater. **30**, 1704320 (2018).
[22]T. Ahmed, S. Walia, E. L. H. Mayes, R. Ramanathan, V. Bansal, M. Bhaskaran, S. Sriram, and O. Kavehei, "Time and rate dependent synaptic learning in neuromimicking resistive memories," Sci. Rep. **9**, 15404 (2019).
[23]R. Yang, K. Terabe, Y. Yao, T. Tsuruoka, T. Hasegawa, J. K. Gimzewski, and M. Aono, "Synaptic plasticity and memory functions achieved in a WO_{3-x}-based nanoionics device by using the principle of atomic switch operation," Nanotechnology **24**, 384003 (2013).
[24]N. Ilyas, D. Li, C. Li, X. Jiang, Y. Jiang, and W. Li, "Analog switching and artificial synaptic behavior of $Ag/SiO_x:Ag/TiO_x/p^{++}$-Si memristor device," Nanoscale Res. Lett. **15**, 30 (2020).
[25]Z. Q. Wang, H. Y. Xu, X. H. Li, H. Yu, Y. C. Liu, and X. J. Zhu, "Synaptic learning and memory functions achieved using oxygen ion migration/diffusion in an amorphous InGaZnO memristor," Adv. Funct. Mater. **22**, 2759–2765 (2012).
[26]M. Dutta, S. Brivio, and S. Spiga, "Unraveling the roles of switching and relaxation times in volatile electrochemical memristors to mimic neuromorphic dynamical features," Adv. Electron. Mater. **10**, 2400221 (2024).
[27]D. Kuzum, R. G. D. Jeyasingh, B. Lee, and H. S. P. Wong, "Nanoelectronic programmable synapses based on phase change materials for brain-inspired computing," Nano Lett. **12**, 2179–2186 (2012).
[28]S.-Y. Kim, J.-M. Yang, E.-S. Choi, and N.-G. Park, "Layered $(C_6H_5CH_2NH_3)_2CuBr_4$ perovskite for multilevel storage resistive switching memory," Adv. Funct. Mater. **30**, 2002653 (2020).
[29]R. A. John, Y. Demirağ, Y. Shynkarenko, Y. Berezovska, N. Ohannessian, M. Payvand, P. Zeng, M. I. Bodnarchuk, F. Krumeich, G. Kara, I. Shorubalko, M. V. Nair, G. A. Cooke, T. Lippert, G. Indiveri, and M. V. Kovalenko, "Reconfigurable halide perovskite nanocrystal memristors for neuromorphic computing," Nat. Commun. **13**, 2074 (2022).
[30]L. Zhou, S. Han, H. Liu, Z. He, J. Huang, Y. Mu, Y. Xie, X. Pi, X. Lu, S. Zhou, and Y. Hou, "Energy-efficient, stable, and temperature-tolerant neuromorphic device based on single crystals of halide perovskites," Cell Rep. Phys. Sci. **5**, 102078 (2024).
[31]W. Xu, H. Cho, Y.-H. Kim, Y.-T. Kim, C. Wolf, C.-G. Park, and T.-W. Lee, "Organometal halide perovskite artificial synapses," Adv. Mater. **28**, 5916–5922 (2016).
[32]N.-K. Pendyala, C. Gonzales, and A. Guerrero, "Decoupling volatile and nonvolatile response in reliable halide perovskite memristors," Small Struct. **6**(1), 2400380 (2024).
[33]H.-K. He, H.-M. Huang, and R. Yang, "Two-terminal neuromorphic memristors," in *Neuromorphic Devices for Brain-Inspired Computing* (Wiley, 2022), pp. 1–46.
[34]S. Kumar, X. Wang, J. P. Strachan, Y. Yang, and W. D. Lu, "Dynamical memristors for higher-complexity neuromorphic computing," Nat. Rev. Mater. **7**, 575–591 (2022).
[35]S. Jiang, S. Nie, Y. He, R. Liu, C. Chen, and Q. Wan, "Emerging synaptic devices: From two-terminal memristors to multiterminal neuromorphic transistors," Mater. Today Nano **8**, 100059 (2019).
[36]G. W. Burr, R. M. Shelby, A. Sebastian, S. Kim, S. Kim, S. Sidler, K. Virwani, M. Ishii, P. Narayanan, A. Fumarola, L. L. Sanches, I. Boybat, M. Le Gallo, K. Moon, J. Woo, H. Hwang, and Y. Leblebici, "Neuromorphic computing using non-volatile memory," Adv. Phys. X **2**, 89–124 (2017).
[37]W. Huang, X. Xia, C. Zhu, P. Steichen, W. Quan, W. Mao, J. Yang, L. Chu, and X. a. Li, "Memristive artificial synapses for neuromorphic computing," Nano-Micro Lett. **13**, 85 (2021).
[38]Y. Zhuo, R. Midya, W. Song, Z. Wang, S. Asapu, M. Rao, P. Lin, H. Jiang, Q. Xia, R. S. Williams, and J. J. Yang, "A dynamical compact model of diffusive and drift memristors for neuromorphic computing," Adv. Electron. Mater. **8**, 2100696 (2022).
[39]M.-K. Song, J.-H. Kang, X. Zhang, W. Ji, A. Ascoli, I. Messaris, A. S. Demirkol, B. Dong, S. Aggarwal, W. Wan, S.-M. Hong, S. G. Cardwell, I. Boybat, J.-s. Seo, J.-S. Lee, M. Lanza, H. Yeon, M. Onen, J. Li, B. Yildiz, J. A. del Alamo, S. Kim, S. Choi, G. Milano, C. Ricciardi, L. Alff, Y. Chai, Z. Wang, H. Bhaskaran, M. C. Hersam, D. Strukov, H. S. P. Wong, I. Valov, B. Gao, H. Wu, R. Tetzlaff, A. Sebastian, W. Lu, L. Chua, J. J. Yang, and J. Kim, "Recent advances and future prospects for memristive materials, devices, and systems," ACS Nano **17**, 11994–12039 (2023).

[40]I. Vourkas and G. C. Sirakoulis, "Emerging memristor-based logic circuit design approaches: A review," IEEE Circuits Syst. Mag. **16**, 15–30 (2016).
[41]K. Yang, J. Joshua Yang, R. Huang, and Y. Yang, "Nonlinearity in memristors for neuromorphic dynamic systems," Small Sci. **2**, 2100049 (2022).
[42]M. Prezioso, M. R. Mahmoodi, F. M. Bayat, H. Nili, H. Kim, A. Vincent, and D. B. Strukov, "Spike-timing-dependent plasticity learning of coincidence detection with passively integrated memristive circuits," Nat. Commun. **9**, 5311 (2018).
[43]M. Prezioso, F. Merrikh Bayat, B. Hoskins, K. Likharev, and D. Strukov, "Self-Adaptive spike-time-dependent plasticity of metal-oxide memristors," Sci. Rep. **6**, 21331 (2016).
[44]F. Alibart, S. Pleutin, O. Bichler, C. Gamrat, T. Serrano-Gotarredona, B. Linares-Barranco, and D. Vuillaume, "A memristive nanoparticle/organic hybrid synapstor for neuroinspired computing," Adv. Funct. Mater. **22**, 609–616 (2012).
[45]P. K. Ghosh, S. Z. Riam, M. S. Ahmed, and P. Sundaravadivel, "CMOS-based memristor emulator circuits for low-power edge-computing applications," Electronics **12**, 1654 (2023).
[46]J. Nagumo, S. Arimoto, and S. Yoshizawa, "An active pulse transmission line simulating nerve axon," Proc. IRE **50**, 2061–2070 (1962).
[47]T. Voglhuber-Brunnmaier and B. Jakoby, "Understanding relaxation oscillator circuits using fast-slow system representations," IEEE Access **11**, 99452–99469 (2023).
[48]P. Maffezzoni, L. Daniel, N. Shukla, S. Datta, and A. Raychowdhury, "Modeling and simulation of vanadium dioxide relaxation oscillators," IEEE Trans. Circuits Syst. I: Regul. Pap. **62**, 2207–2215 (2015).
[49]A. Mauro, "Anomalous impedance, A phenomenological property of time-variant resistance: An analytic review," Biophys. J. **1**, 353–372 (1961).
[50]S. Dueñas, H. Castán, H. García, ÓG Ossorio, L. A. Domínguez, and E. Miranda, "Experimental observation of negative susceptance in HfO_2-based RRAM devices," IEEE Electron Device Lett. **38**, 1216–1219 (2017).
[51]Y. Liang, Q. Zhu, G. Wang, S. K. Nath, H. H. C. Iu, S. K. Nandi, and R. G. Elliman, "Universal dynamics analysis of locally-active memristors and its applications," IEEE Trans. Circuits Syst. I: Regul. Pap. **69**, 1278–1290 (2022).
[52]X. Liao and N. Mu, "Self-sustained oscillation in a memristor circuit," Nonlinear Dyn. **96**, 1267–1281 (2019).
[53]J. Bisquert, "Inductive and capacitive hysteresis of current-voltage curves. A unified structural dynamics in solar energy devices, memristors, ionic transistors and bioelectronics," PRX Energy **3**, 011001 (2024).
[54]T. V. Bliss and G. L. Collingridge, "A synaptic model of memory: Long-term potentiation in the hippocampus," Nature **361**, 31–39 (1993).
[55]H. Yu, H. Wei, J. Gong, H. Han, M. Ma, Y. Wang, and W. Xu, "Evolution of bio-inspired artificial synapses: Materials, structures, and mechanisms," Small **17**, 2000041 (2021).
[56]L. O. Chua and K. Sung Mo, "Memristive devices and systems," Proc. IEEE **64**, 209–223 (1976).
[57]Y. V. Pershin and M. Di Ventra, "Memory effects in complex materials and nanoscale systems," Adv. Phys. **60**, 145–227 (2011).
[58]J. Bisquert, E. Miranda, and J. B. Roldan, "Hysteresis in memristors produces a conduction inductance and a conduction capacitance effects," PhysChemChemPhys **26**, 13804–13813 (2024).
[59]G. Milano, G. Pedretti, M. Fretto, L. Boarino, F. Benfenati, D. Ielmini, I. Valov, and C. Ricciardi, "Brain-inspired structural plasticity through reweighting and rewiring in multi-terminal self-organizing memristive nanowire networks," Adv. Intell. Syst. **2**, 2000096 (2020).
[60]G. Milano, G. Pedretti, K. Montano, S. Ricci, S. Hashemkhani, L. Boarino, D. Ielmini, and C. Ricciardi, "In materia reservoir computing with a fully memristive architecture based on self-organizing nanowire networks," Nat. Mater. **21**, 195–202 (2022).
[61]P. Ramirez, V. Gomez, J. Cervera, S. Mafe, and J. Bisquert, "Synaptical tunability of multipore nanofluidic memristors," J. Phys. Chem. Lett. **14**, 10930–10934 (2023).
[62]A. Vahl, G. Milano, Z. Kuncic, S. A. Brown, and P. Milani, "Brain-inspired computing with self-assembled networks of nano-objects," J. Phys. D: Appl. Phys. **57**, 503001 (2024).
[63]P. Ramirez, S. Portillo, J. Cervera, S. Nasir, M. Ali, W. Ensinger, and S. Mafe, "Neuromorphic responses of nanofluidic memristors in symmetric and asymmetric ionic solutions," J. Chem. Phys. **160**, 044701 (2024).
[64]P. Ramirez, S. Portillo, J. Cervera, J. Bisquert, and S. Mafe, "Memristive arrangements of nanofluidic pores," Phys. Rev. E **109**, 044803 (2024).
[65]S. Portillo, J. A. Manzanares, P. Ramirez, J. Bisquert, S. Mafe, and J. Cervera, "pH-Dependent effects in nanofluidic memristors," J. Phys. Chem. Lett. **15**, 7793–7798 (2024).
[66]J. Bisquert, "Hysteresis, rectification and relaxation times of nanofluidic pores for neuromorphic circuit applications," Adv. Phys. Res. **3**, 2400029 (2024).
[67]J. Bisquert, M. Sánchez-Mateu, A. Bou, C. S. Law, and A. Santos, "Synaptic response of fluidic nanopores: The connection of potentiation with hysteresis," ChemPhysChem **25**, e202400265 (2024).
[68]E. Miranda and J. Suñé, "Memristive state equation for bipolar resistive switching devices based on a dynamic balance model and its equivalent circuit representation," IEEE Trans. Nanotechnol. **19**, 837–840 (2020).
[69]A. Bou, C. Gonzales, P. P. Boix, Y. Vaynzof, A. Guerrero, and J. Bisquert, "Kinetics of volatile and nonvolatile halide perovskite devices: The conductance-activated quasi-linear memristor (CALM) model," J. Phys. Chem. Lett. **16**, 69–76 (2025).
[70]E. M. Izhikevich, *Dynamical Systems in Neuroscience* (MIT Press, 2007).
[71]A. L. Hodgkin and A. F. Huxley, "A quantitative description of membrane current and its application to conduction and excitation in nerve," J. Physiol. **117**, 500–544 (1952).
[72]R. Waser and M. Aono, "Nanoionics-based resistive switching memories," Nat. Mater. **6**, 833–840 (2007).
[73]M. D. Ventra, Y. V. Pershin, and L. O. Chua, "Circuit elements with memory: Memristors, memcapacitors, and meminductors," Proc. IEEE **97**, 1717–1724 (2009).
[74]T. Prodromakis, C. Toumazou, and L. Chua, "Two centuries of memristors," Nat. Mater. **11**, 478–481 (2012).
[75]E. Linn, R. Rosezin, C. Kügeler, and R. Waser, "Complementary resistive switches for passive nanocrossbar memories," Nat. Mater. **9**, 403–406 (2010).
[76]S. Kim, S. Choi, and W. Lu, "Comprehensive physical model of dynamic resistive switching in an oxide memristor," ACS Nano **8**, 2369–2376 (2014).
[77]F. Lalchhandama, K. Datta, S. Chakraborty, R. Drechsler, and I. Sengupta, "CoMIC: Complementary memristor based in-memory computing in 3D architecture," J. Syst. Archit. **126**, 102480 (2022).
[78]S. Srivastava, J. P. Thomas, X. Guan, and K. T. Leung, "Induced complementary resistive switching in forming-free $TiO_x/TiO_2/TiO_x$ memristors," ACS Appl. Mater. Interfaces **13**, 43022–43029 (2021).
[79]J. Wang, R. Pan, H. Cao, Y. Wang, L. Liang, H. Zhang, J. Gao, and F. Zhuge, "Anomalous rectification in a purely electronic memristor," Appl. Phys. Lett. **109**, 143505 (2016).
[80]J. Bisquert and A. Guerrero, "Chemical inductor," J. Am. Chem. Soc. **144**, 5996–6009 (2022).
[81]C. Gonzales, A. Bou, A. Guerrero, and J. Bisquert, "Capacitive and inductive characteristics of volatile perovskite resistive switching devices with analog memory," J. Phys. Chem. Lett. **15**, 6496–6503 (2024).
[82]I. Abraham, "The case for rejecting the memristor as a fundamental circuit element," Sci. Rep. **8**, 10972 (2018).