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Additional Information

Inverse Design of a Grating Coupler for Multicore Fiber Considering Fabrication Tolerances

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***Abstract*—In this work, the inverse design of a grating coupler for multicore fiber (MCF) connection to a photonic integrated circuit (PIC) using silicon photonics technology is reported. The grating was designed using topological optimization in 2D, taking into account relevant foundry parameters. The grating was evaluated considering the expected ranges for etch width and depth, overlay misalignment, and fiber lateral and tilt alignment. The design was validated through simulations performed in COMSOL Multiphysics. The device exhibits an insertion loss of 0.62 dB and a 1-dB bandwidth of 70 nm, where etch depth and width are the most relevant fabrication parameters. The tolerance analysis shows good robustness across the C-band.**

***Index Terms*—Silicon photonics, photonic integrated circuits, fiber optics, multicore fiber, gratings, optical fiber devices.**

I. Introduction

There is a continuous increase in data processing capacity in state-of-the-art datacenters due to the rapid introduction of artificial intelligence (AI) applications that rely on datacenter computing, as well as the neural network training required by machine learning algorithms in the backend. The increase in datacenter processing capacity is directly reflected in the need for more capable (higher bitrate, longer reach, lower latency, and smaller energy consumption) intra–datacenter connectivity, as data interconnection between CPUs and GPUs in the datacenter is critical [1]. Different solutions have been proposed to address the data connectivity requirements and the space limitations imposed by the dense packing of a large number of processing units. In particular, Avicena proposed a parallel optical link technology based on GaN micro-LEDs, which can be modulated up to 10 Gb/s [2]. TeraPHY has proposed an optical interconnect solution based on microring resonators modulating an external laser source [3].

A particularly interesting solution for AI datacenter connectivity is the use of multicore fiber (MCF) with spatial division multiplexing [4]. Multicore fibers comprise multiple independent cores embedded within a single cladding, which can overcome the capacity limits of conventional single-mode fibers (SMFs) in a more compact and cost-efficient manner [4]. Nevertheless, efficient and easy-to-fabricate connections from the MCF to a silicon photonics transceiver are still a technical challenge. Therefore, developing efficient MCF-PIC connectors from a design-for-fabrication approach is essential. In this work, we propose and evaluate, by simulation, the design of an MCF-PIC grating coupler taking into account precise silicon photonics fabrication tolerances. Fig. 1 shows the schematic of the proposed system for MCF-PIC coupling, designed for standard SOI platform.

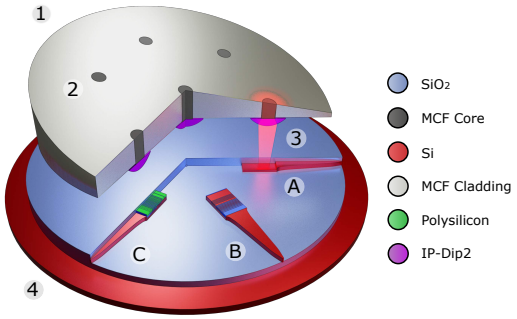


Fig. 1. 3D schematic of the MCF–PIC coupling system including: (1) MCF fiber (7-cores example); (2) MCF core; (3) TPL 3D-printed lens; (4) photonic integrated circuit (PIC); (A) Grating layer 1 – Taper; (B) Grating layer 2 – Taper; and (C) Grating layer 3 – Taper. Vertical dimensions have been increased for clarity. The MCF and PIC cladding are partially removed with a wedge cut out for visualization purposes.

In the proposed architecture, each MCF core is coupled to a grating–taper pair that guides light into a 500 nm-wide waveguide. The MCF is suspended above the PIC by an air gap, and beneath a 3D-printed two-photon lithography lens is positioned. This lens adds extra degrees of freedom to the design and compensates for small variations in the MCF mode. Specifically, it can adjust the angle of incidence, beam waist, and the aspect ratio of the beam.

This work focuses on the 2D design of gratings for the fundamental TE mode. The design consists of two patterns, shown in Fig. 1: the first is formed by Si and SiO_2 through etching the Si, and the second is formed by polysilicon and SiO_2, created by deposition followed by etching of the polysilicon. This double-patterned design improves efficiency in two ways: it allows a better mode matching to the incident Gaussian beam while keeping a fabricable feature size [7], and breaks the vertical symmetry, reducing the fraction of light directed towards the substrate [7] [8].

II. Design Methodology

The grating coupler was designed via topology optimization (TopOp), allowing material properties to vary spatially within the design region. For each point in the design domain, a parameter θ_c is defined and constrained as:

$$0 \leq \theta_c \leq 1 \tag{1}$$

The optimization iteratively searches for the best configuration based on a defined figure of merit (FOM). Since the TopOp allows each point to vary freely between two materials,

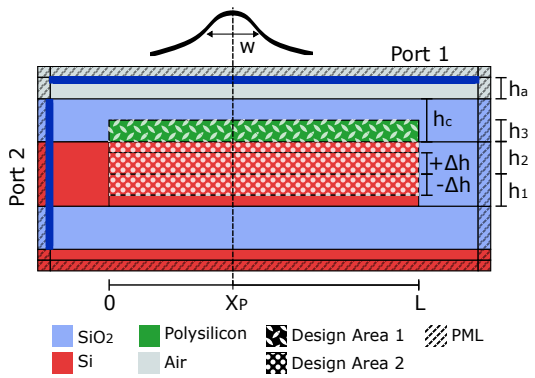


Fig. 2. 2D schematic of the optimization simulation; h_1: Si layer height; h_2: patterned Si/SiO_2 layer height; h_3: polysilicon layer height; h_c: cladding height; h_a: air gap; Δh: variation of the h_1–h_2 interface height; X_p: input pulse center; L: design length; W: Gaussian pulse waist.

the resulting design cannot be directly fabricated, as it would require a continuous properties transition. Furthermore, even after binarization, there may be rapid spatial changes beyond realistic fabrication capabilities. To avoid these, a Helmholtz filter is applied:

$$\theta_f = \theta_c + R_{\min}^2 \nabla_\theta^2 f \tag{2}$$

where θ_f is the filtered parameter and $R_{\min}$ is the minimum feature size (fs) radius. To reduce the intermediate gray areas between materials, a hyperbolic tangent projection is applied

$$\theta = \frac{\tanh\left(\beta(\theta_f - 0.5)\right) + \tanh(0.5\beta)}{2\tanh(0.5\beta)} \tag{3}$$

where β controls the transition steepness. Then, the parameter θ is used to interpolate the material properties. A detailed description of this methodology can be found in [6].

The COMSOL Multiphysics 6.3 simulation setup is depicted in Fig. 2. The input port was modeled as a Gaussian approximation of the fundamental fiber mode with a beam waist of $w = 6$ μm. The incident light is normal and centered at $x = 5$ μm. For simplicity, the beam waist was considered constant across all the wavelengths. The output power was measured at Port 2.

The design region consisted of two blocks of height $h_2 = 120$ nm and $h_3 = 100$ nm. For each layer a set of linear parameters with a mesh size of 20 nm were defined, totalizing 1500 parameters for a length of $L = 15$ μm. Between layer 1 and layer 2 the height was kept constant at 220 nm, which is the standard for SOI platforms. The remaining heights were set to: air gap $h_a = 1$ μm and height cladding $h_c = 0.7$ μm.

To ensure tolerance to fabrication variations, changes in silicon etch depth were also considered. Two simulations were performed with an increased and decreased height of Layer 2 by a value $\Delta h = 7$ nm. As FOM, the transmission at Port 2 was computed for three wavelengths: 1530 nm, 1547.5 nm and 1565 nm. The optimization minimized the function:

$$\text{FOM} = \sum_{\lambda} \sum_{h_2} \left(1 - T(\lambda, h_2)\right)^2 \tag{4}$$

where T is the transmission at each wavelength and height of layer 2 variation.

The optimization was carried out iteratively by increasing the projection parameter β through 8, 12, 16, and 20 to gradually reduce gray regions. Using a high β value at an early stage tends to slow down the convergence of the solution. In all cases, a Helmholtz filter with a radius of 70 nm was applied.

Finally, the designs were binarized using a step function. To ensure compatibility with the 100 nm feature size of the 193 nm deep ultraviolet lithography [5], a post-processing step was implemented in Python. In this step, features smaller than 80 nm were removed and the remaining features were expanded to a minimum size of $fs = 110$ nm.

III. Design Analysis

The performance of the proposed device is shown in Fig. 3(a), where the transmission through Port 2 and the reflection at Port 1 are evaluated in the 1.5 – 1.6 μm range. The insertion loss (IL) at the central wavelength is 0.62 dB, and the 1 dB bandwidth is 70 nm. Across the C-band (1530–1565 nm), IL remains below 1.12 dB and the reflections stay below -14 dB.

These results are comparable to other published double-patterned grating couplers, with IL = 0.41 dB, 1 dB BW = 34 nm, and f_s = 70 nm [8], and IL = 0.91 dB, 1 dB BW = 34 nm, and f_s = 180 nm [7], although the present design exhibits a larger 1 dB bandwidth. This difference may be related to the smaller beam waist of the MCF and its constant value across the wavelength variation.

Device tolerances were studied to evaluate its behavior under fabrication errors and fiber misalignment, as shown in Fig. 4, presenting transmission across the C-band.

Regarding the influence of etch width, Fig. 4(a) shows that for underetch (positive bias) there are significant losses above a 5 nm deviation. In contrast, for overetch (negative bias), even a 20 nm deviation results in losses below 1.72 dB, representing an increase of only 0.6 dB compared to the base design. Therefore, a 5 nm overetch bias is recommended.

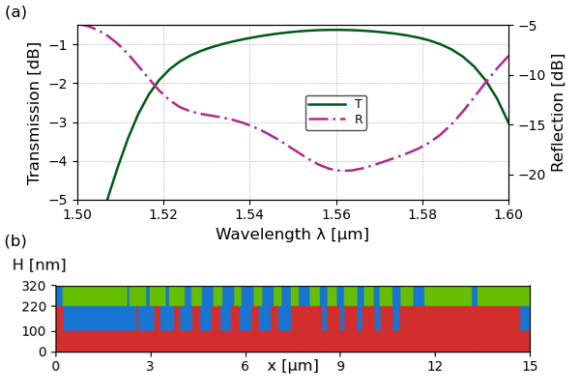


Fig. 3. (a) Transmission and reflection of the designed grating coupler. (b) Material distribution of the designed grating coupler.

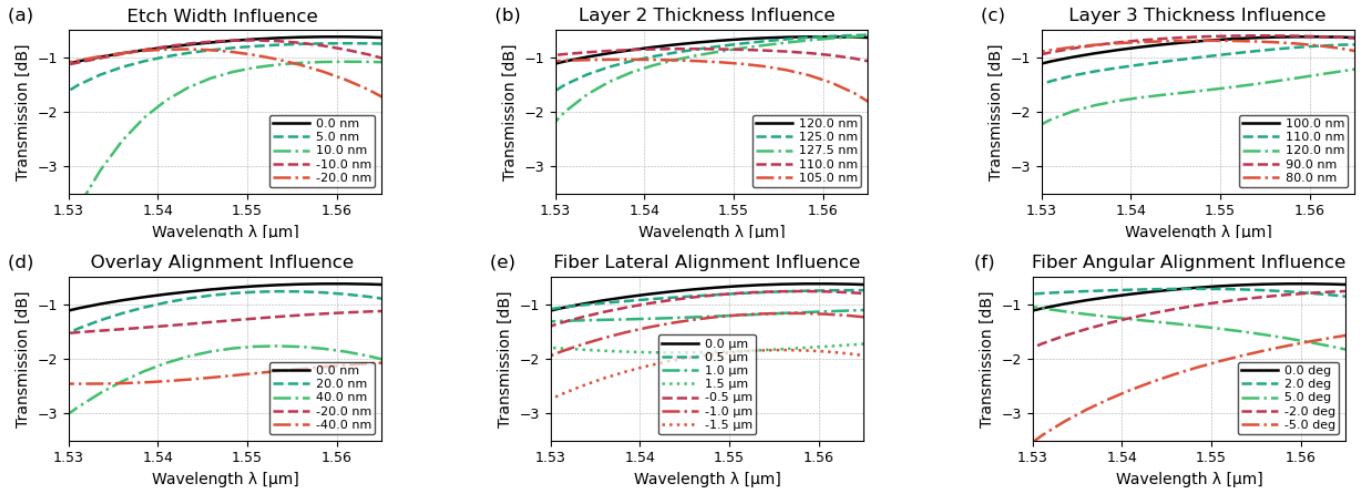


Fig. 4. Influence of different parameters on the designed grating coupler transmission: (a) Variation in the etch width, with overetch (underetch) corresponding to negative (positive) bias. (b) Variation in the etch depth in the silicon, resulting in a larger (smaller) layer 2 for overetch (underetch). (c) Variation in layer 3 thickness. (d) Lateral displacement of the layer 3 pattern, with positive (negative) values toward the front (back) of the grating. (e) Lateral displacement of the fiber, with negative (positive) values toward the front (back) of the grating. (f) Influence of the fiber angle, with negative (positive) values corresponding to the light beam pointing toward the front (back) of the grating.

For the silicon etch depth, Fig. 4(b) shows that the underetch case ($h_2 < 120$ nm) keeps losses below 1.62 dB for deviations up to 5 nm. For the overetch case ($h_2 > 120$ nm), the losses are below 1.8 dB for deviations up to 15 nm. Thus, an overetch bias of 2.5 nm is recommended, resulting in a layer 1 thickness of 97.5 nm and a layer 2 thickness of 122.5 nm. In contrast, the polysilicon overlay layer (layer 3) –shown in Fig. 4(c)– has only a minor influence on the device.

The lateral overlay misalignment of layer 3 –shown in Fig. 4(d)–, corresponding to relative sliding of this layer, shows similar behavior in both directions, and the losses remain below 1.62 dB for deviations up to 20 nm.

Finally, fiber alignment tolerances were also analyzed. The lateral fiber misalignment, shown in Fig. 4(e), exhibits a 1 dB tolerance for displacements of ± 1 μm. For angular variations of the fiber, shown in Fig. 4(f), the device shows large tolerance for forward tilted beams (positive angles). For backward-pointing beams, losses reach 1.8 dB at $-2°$.

IV. Conclusion

Through topology optimization, a double-patterned grating coupler for MCF-PIC coupling was designed. The proposed structure consists of a shallow-etched silicon grating and a patterned polysilicon overlay. The figure of merit used during the optimization included variations in the shallow etch depth to ensure fabrication tolerance. An insertion loss of 0.62 dB and a 1-dB bandwidth of 70 nm were obtained. Additionally, reflections across the C-band were kept below -14 dB.

The tolerance analysis showed good robustness across the C-band. Based on these results, it is recommended to bias the fabrication toward a 5 nm overetch, reducing the minimum feature size to approximately 105 nm, and to increase the shallow etch depth by 2.5 nm.

As future work, the wavelength dependence of the beam waist will be measured experimentally and included in the model. This variation is expected to negatively impact the bandwidth; however, part of this degradation could be compensated by including it during the optimization process. Subsequently, 3D simulations will be performed for validation, and the remaining system elements will be designed.

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