Model-Following control of a three-level Neutral Point Clamped inverter for current harmonics compensation in the medium voltage range

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Abstract – This paper presents a new control technique applied to a three phase shunt active filter based on an NPC inverter, showing the modelling procedure needed to carry out the proposed control. The transfer functions for the control of the currents injected by the active filter are derived. The modelling is based on the *abc/dq* transformation of the AC system variables. The currents injected by the active filter are controlled in the synchronous orthogonal *dq* frame. The proposed control technique improves the line current distortion and the dynamic response of the converter to load steps without the need of a high crossover frequency neither of the current loop nor of the DC-link voltage loop. The viability of the proposed scheme on a *200kVA* system is shown by means of computer simulations using Saber™.

1. Introduction

Research into active power filters for the medium voltage range has been carried out during the last years [1] [2]. Shunt active power filters represent the ideal configuration to eliminate the harmonic contamination caused by nonlinear loads. Medium voltage grids are normally three-wire systems, so that a three-phase three-wire active filter is a suitable solution for harmonics elimination.

Due to the power handling capability of currently available power semiconductors, conventional active filters based on two-level PWM voltage source inverters (VSIs) have to be connected through a coupling transformer to medium voltage grids. In the recent time the use of multilevel converters is prevailing in applications that connect electronic equipment to medium voltage levels without using a coupling transformer [3].

A shunt active filter based on a three-level Neutral Point Clamped (NPC) VSI is considered in this paper in order to compensate both reactive power and harmonic currents of a nonlinear load, following the scheme of Fig. 1(a). The reference currents for the active filter are calculated starting from the sensed currents of the nonlinear load, and applying the well-known synchronous reference frame method [4]. The reference current needed to keep a regulated voltage at the DC-link of the active filter is added to the current loop reference.

The aim of this work is to present a Robust Model-Following (RMF) control structure applied both to the current and to the voltage loop of the NPC VSI working as an active filter. The proposed control was successfully applied to parallel DC-DC converters [5] and to switch-mode rectifiers [6]. It will be shown that, applied to the NPC active filter, both a reduction of the line current distortion and a faster response of the DC-link voltage to load steps are achieved by RMF control, when compared with conventional PI control.

The paper is organized as follows. In section 2 the active filter is modelled in the stationary *abc* frame, and transformed to the rotating synchronous *dq* frame. The transfer functions of interest for the design of the current loop are derived. In section 3 the generation of the reference currents for the inverter is described. In section 4 the control structure of the active filter current loop in *d-q* coordinates is shown, and some considerations for the design of the current loop are described. In section 5 the control structure of the DC-link voltage is explained, and some considerations for the design of the voltage loop are described. In section 6 the proposed RMF control structure is explained, showing the general expressions of its associated controllers and loop gain transfer functions, both for the current and for the voltage loop. For comparison purposes the general expressions of the controllers and transfer functions with conventional PI control are presented. In section 7 the design procedures of PI controllers and of RMF controllers for the active filter are described, and a discussion about PI vs. RMF control is carried out. In section 8 simulation results of a *200kVA* system are shown in order to compare the dynamic performance of the active filter with both control structures.

2. Active Filter modelling

In this section an analytical dynamic model of the active filter is developed in the natural three-phase *abc* frame. After that, the model is transformed into the synchronous reference frame.

2.1. System model in the *abc* frame

Fig. 1(b) shows the equivalent switching structure for the three-level Neutral Point Clamped (NPC) converter. The phase switching functions are defined by (1), where $i \in \{a, b, c\}$, and $j \in \{P, Z, N\}$.

$$S_{ij} = \begin{cases} 1 & \text{if } i \text{ connected to } j \\ 0 & \text{otherwise} \end{cases} \tag{1}$$

Restriction (2) arises from the fact that capacitor voltage sources can't be short circuited and inductor current sources can't be opened.

$$S_{ip} + S_{iz} + S_{in} = 1, \quad i \in \{a,b,c\} \tag{2}$$

Equation (3) expresses the converter output voltages with respect to the DC bus midpoint Z, i.e., the capacitors neutral point (NP). These voltages are expressed as a function of the bus capacitors voltages (v_{C1}, v_{C2}), and of the switching functions S_{ij}. The voltage between the DC bus midpoint Z and the grid neutral is called v_{Z0}, or simply, v_Z.

$$\begin{pmatrix} v_{az} \\ v_{bz} \\ v_{cz} \end{pmatrix} = \begin{pmatrix} S_{ap} & -S_{an} \\ S_{bp} & -S_{bn} \\ S_{cp} & -S_{cn} \end{pmatrix} \cdot \begin{pmatrix} v_{C2} \\ v_{C1} \end{pmatrix} \tag{3}$$

Supposing that the capacitors neutral point Z is balanced and that the DC bus voltage is constant, expression

(4) is fulfilled, so that (3) can be rewritten as (5), where S_i are the phase leg switching functions, defined by (6).

$$v_{C1} = v_{C2} = \frac{V_{BUS}}{2} \tag{4}$$

$$\begin{pmatrix} v_{az} \\ v_{bz} \\ v_{cz} \end{pmatrix} = \begin{pmatrix} S_{ap} - S_{an} \\ S_{bp} - S_{bn} \\ S_{cp} - S_{cn} \end{pmatrix} \cdot \frac{V_{BUS}}{2} = \begin{pmatrix} S_a \\ S_b \\ S_c \end{pmatrix} \cdot \frac{V_{BUS}}{2} \tag{5}$$

$$S_i = S_{ip} - S_{in} \text{, with } i \in \{a, b, c\} \tag{6}$$

Kirchoff's laws for voltages and currents applied at the connection point of the active filter (see Fig. 1(b)) allow to write the differential equations (7) in the stationary *abc* frame.

$$\frac{d}{dt}\begin{bmatrix} i_{fa} \\ i_{fb} \\ i_{fc} \end{bmatrix} = \frac{1}{L}\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \cdot \frac{V_{BUS}}{2} + \frac{1}{L}\begin{bmatrix} v_Z \\ v_Z \\ v_Z \end{bmatrix} - \frac{1}{L}\begin{bmatrix} v_R \\ v_S \\ v_T \end{bmatrix} \tag{7}$$

By calculating the average value over one switching period (8) of the phase leg switching functions, the phase leg duty cycles (9) are obtained. In (8) x is a generic variable of (7), and T_S is the switching period.

$$\langle x \rangle_{Ts} = \frac{1}{T_s} \int_{t-Ts}^{t} x(\tau) d\tau \tag{8}$$

$$d_i = \frac{1}{T_s} \int_{t-Ts}^{t} S_i dt \quad , i \in \{a, b, c\} \tag{9}$$

Applying the average operator (8) to (7), the averaged model (10) of the system can be derived.

For simplicity of notation, in the following it will be supposed that equations are expressed by means of averaged values.

$$\frac{d}{dt}[i_{fi}] = \frac{1}{L}[d_i]\frac{V_{BUS}}{2} + \frac{1}{L}[v_Z] - \frac{1}{L}[v_k] \text{, with } i \in \{a, b, c\} \text{ and } k \in \{R, S, T\} \tag{10}$$

2.2. Model transformation into the synchronous *dq* frame

The transformation matrix **T** to change from the natural *a, b, c* reference frame to the synchronous *d, q, 0* reference frame is shown by (11), where $\theta = \omega \cdot t$ is the rotation angle of the rotating *d-q* axes, which are synchronized with the grid voltage.

$$[T] = \sqrt{\frac{2}{3}}\begin{bmatrix} \cos(\theta) & \cos(\theta - 2\pi/3) & \cos(\theta + 2\pi/3) \\ -\sin(\theta) & -\sin(\theta - 2\pi/3) & -\sin(\theta + 2\pi/3) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{11}$$

When multiplying from the left both sides of (10) by the transformation matrix **T**, expression (12) is obtained. It has been taken into account that in a three-wire system the homopolar current is zero, i.e., $i_0 = di_0/dt = 0$. The

variable v_Z is considered a disturbance input of the system.

$$\frac{d}{dt}\begin{pmatrix} i_d \\ i_q \\ 0 \end{pmatrix} = \omega\begin{pmatrix} i_q \\ -i_d \\ 0 \end{pmatrix} + \frac{V_{BUS}}{2L}\begin{pmatrix} d_d \\ d_q \\ d_0 \end{pmatrix} + \frac{\sqrt{3}}{L}\begin{pmatrix} 0 \\ 0 \\ v_Z \end{pmatrix} - \frac{1}{L}\begin{pmatrix} v_d \\ v_q \\ v_0 \end{pmatrix} \tag{12}$$

In (12) it can be noticed that homopolar components (v_0, v_Z and d_0) don't affect the dynamics of currents i_d and i_q, so that those components can be ignored when designing the control loop of the currents injected by the active filter.

A dynamic small-signal model can be obtained from (12) by perturbation and linearization around an operation point. The following nomenclature is used for any averaged variable: $x = X + \hat{x}$, where x is the averaged variable, X is the variable steady-state value, and $\hat{x}$ is its small-signal value. Neglecting the disturbances of the grid voltage (i.e., $\hat{v}_d = \hat{v}_q = \hat{v}_0 = 0$), and assuming that the DC bus voltage is kept constant by the voltage loop ($\hat{v}_{BUS} = 0$), expression (13) results.

$$\frac{d}{dt}\begin{bmatrix} \hat{i}_d \\ \hat{i}_q \end{bmatrix} = \omega\begin{bmatrix} \hat{i}_q \\ -\hat{i}_d \end{bmatrix} + \frac{V_{BUS}}{2L}\begin{bmatrix} \hat{d}_d \\ \hat{d}_q \end{bmatrix} \tag{13}$$

Applying the Laplace transform with null initial conditions to (13), it results (14).

$$\begin{bmatrix} s & -\omega \\ \omega & s \end{bmatrix} \cdot \begin{bmatrix} \hat{i}_d \\ \hat{i}_q \end{bmatrix} = \frac{V_{BUS}}{2L} \cdot \begin{bmatrix} \hat{d}_d \\ \hat{d}_q \end{bmatrix} \tag{14}$$

Matrix $\mathbf{A}$ is defined by (15).

$$[A] = \begin{bmatrix} s & -\omega \\ \omega & s \end{bmatrix} \tag{15}$$

If both sides of (14) are multiplied from the left by the inverse of matrix $\mathbf{A}$, equation (16) will result. The small-signal model of (16) is the basis for the design of the control loops of the active filter currents in dq coordinates.

$$\begin{bmatrix} \hat{i}_d \\ \hat{i}_q \end{bmatrix} = \frac{V_{BUS}}{2L} \cdot \begin{bmatrix} \frac{s}{s^2+\omega^2} & \frac{\omega}{s^2+\omega^2} \\ \frac{-\omega}{s^2+\omega^2} & \frac{s}{s^2+\omega^2} \end{bmatrix} \cdot \begin{bmatrix} \hat{d}_d \\ \hat{d}_q \end{bmatrix} \tag{16a}$$

$$\begin{bmatrix} \hat{i}_d \\ \hat{i}_q \end{bmatrix} = \begin{bmatrix} Gid_{dd}(s) & Gid_{dq}(s) \\ Gid_{qd}(s) & Gid_{qq}(s) \end{bmatrix} \cdot \begin{bmatrix} \hat{d}_d \\ \hat{d}_q \end{bmatrix} \tag{16b}$$

In the transfer matrix of (16) the following transfer functions can be identified:

- Two identical 'diagonal' transfer functions, given by (17a).
- Two 'cross-coupling' (or 'off-diagonal') transfer functions, given by (17b). The only difference between both 'cross' transfer functions is the sign.

$$Gid_{dd}(s)=\left.\frac{\hat{i}_d(s)}{\hat{d}_d(s)}\right|_{\hat{d}_q=0},\ Gid_{qq}(s)=\left.\frac{\hat{i}_q(s)}{\hat{d}_q(s)}\right|_{\hat{d}_d=0}$$
$$Gid_{dd}(s)=Gid_{qq}(s)=\frac{V_{BUS}}{2L}\cdot\frac{s}{s^2+\omega^2}\equiv Gid_{diag}(s) \quad (17a)$$

$$Gid_{dq}(s)=\left.\frac{\hat{i}_d(s)}{\hat{d}_q(s)}\right|_{\hat{d}_d=0},\ Gid_{qd}(s)=\left.\frac{\hat{i}_q(s)}{\hat{d}_d(s)}\right|_{\hat{d}_q=0}$$
$$Gid_{dq}(s)=-Gid_{qd}(s)=\frac{V_{BUS}}{2L}\cdot\frac{\omega}{s^2+\omega^2}\equiv Gid_{cross}(s) \quad (17b)$$

The aim of the current loop is to control i_d current by means of d_d component, and i_q current by means of d_q component (diagonal or decoupled control) in spite of the cross terms. The 'cross-coupling' between i_d current and d_q duty cycle, and between i_q current and d_d duty cycle will be taken into account for the design of the current controller, to be explained in section 4.

3. Reference currents generator

The load currents i_{La}, i_{Lb}, and i_{Lc} are sensed and transformed to the synchronous reference dq frame via the Park transformation matrix, as shown by (18), where the rotation angle $\theta=\omega\cdot t$ is obtained starting from the grid voltages by means of a phase locked loop (PLL) circuit [7].

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix}=\left[T_{abc\to dq}\right]\cdot\begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (18a)$$

$$T_{abc\to dq}=\sqrt{\frac{2}{3}}\begin{bmatrix} \cos(\theta) & \cos(\theta-2\pi/3) & \cos(\theta+2\pi/3) \\ -\sin(\theta) & -\sin(\theta-2\pi/3) & -\sin(\theta+2\pi/3) \end{bmatrix} \quad (18b)$$

The active filter is intended to compensate both harmonics and reactive power of the nonlinear load. Since the fundamental positive-sequence component of the load currents, responsible for the active power, becomes the DC component of i_{Ld} (18a), it can be filtered out from i_{Ld} by means of a high pass filter [8], obtaining a signal i_d^*. In the present application a second order high pass filter with a cutoff frequency of *10Hz* has been used. If the VSI implementing the active filter were ideal, the reference current for the active filter in the d-channel would be $i_{d\text{-}ref}$ *(ideal)*= i_d^*. Taking into account the inverter losses, the actual reference current in the d-channel must be slightly modified: $i_{d\text{-}ref}= i_d^*-i_{d\text{-}bus}^*$, where $i_{d\text{-}bus}^*$ is an additional signal coming from the DC-link voltage loop. As a matter of fact, $i_{d\text{-}bus}^*$ is the control action of the voltage regulator, which achieves the regulation of the voltage at the DC-link capacitors, compensating the effects of the inverter losses on the DC-link voltage. The q-channel

component of the load currents, i_{Lq} (18a), agrees with the reference current for the active filter in the q-channel, i.e., $i_{q\text{-}ref} = i_q^* = i_{Lq}$, because the active filter is intended to compensate both harmonics (AC components of i_{Lq}) and reactive power (DC component of i_{Lq}) of the nonlinear load.

4. Harmonics current control

Fig. 2 shows the diagonal control structure of the active filter currents in dq coordinates. As it was mentioned in section 2.2, i_d current is controlled by means of d_d component, and i_q current by means of d_q component in spite of the cross-coupling terms. This task is accomplished by the two identical 'diagonal' current regulators, $H_i(s)$, in Fig. 2. It is worth pointing out that the same current regulator is suitable for both channels (d and q), because the diagonal power stage transfer functions to be compensated in both channels are identical, i.e., $Gid_{dd}(s)=Gid_{qq}(s)\equiv Gid_{diag}(s)$, as it was shown by (17a) in section 2. Therefore, the current loop gains are identical in both channels: $T_{i\text{-}d}(s)=T_{i\text{-}q}(s)\equiv T_i(s)=Gid_{diag}(s)\cdot H_i(s)$, so that it is only necessary to perform the design of the current regulator in one channel.

Fig. 2 shows the control structure of the active filter current loops in the d and q channels. That figure also shows the current reference signals in both channels, synthesized as it has been described in section 3. Note that two decoupling terms with a gain $2\omega L/V_{BUS}$ are added to the output of the current regulators, $H_i(s)$, in both channels in order to achieve that i_d current only depends on the output of $H_i(s)$ in the d-channel, and that i_q current only depends on the output of $H_i(s)$ in the q-channel. The decoupling gains can be easily derived from the averaged equations of (12) or from the small-signal equations (13)-(14). For instance, if d_d is synthesized as: $\hat{d}_d = H_i(s)\cdot\hat{\varepsilon}_d(s) - \dfrac{2\omega L}{V_{BUS}}\cdot\hat{i}_q(s)$, being $\hat{\varepsilon}_d(s)=\hat{i}_{d-ref}(s)-\hat{i}_d(s)$, it can be derived from (14) that i_d current only depends on the output $H_i(s)\cdot\hat{\varepsilon}_d(s)$ of the d-channel current regulator yielding (19a). Similarly, if d_q is synthesized as: $\hat{d}_q = H_i(s)\cdot\hat{\varepsilon}_q(s) + \dfrac{2\omega L}{V_{BUS}}\cdot\hat{i}_d(s)$, being $\hat{\varepsilon}_q(s)=\hat{i}_q^*(s)-\hat{i}_q(s)$, i_q current only depends on the output $H_i(s)\cdot\hat{\varepsilon}_q(s)$ of the q-channel current regulator yielding (19b). It is worth pointing out that due to variations on the actual values of L, ω and V_{BUS} the 'perfect' decoupling shown by Fig. 2 and (19) is impossible to achieve in practice, although it is very effective.

$$\hat{i}_d(s) = \frac{V_{BUS}}{2Ls}\cdot H_i(s)\cdot\hat{\varepsilon}_d(s) \tag{19a}$$

$$\hat{i}_q(s) = \frac{V_{BUS}}{2Ls}\cdot H_i(s)\cdot\hat{\varepsilon}_q(s) \tag{19b}$$

The following considerations must be taken into account for the design of the current loop:

1) The crossover frequency, f_{Ci}, of the current loop, $T_i(s)=Gid_{diag}(s)\cdot H_i(s)$, has to be higher than the frequency of the highest harmonic to compensate, which is the thirteenth harmonic in the present application (650*Hz* in *abc* coordinates, i.e., 600*Hz* in the *d-q* frame, because it's a positive sequence harmonic).

2) f_{Ci} is limited by the fact that attenuation enough is needed at the switching frequency, so that the switching ripple in the current sense signals doesn't affect the loop stability.

3) In the medium voltage range the switching frequency is chosen as low as possible in order to minimize switching losses. A switching frequency f_s=5*kHz* has been chosen for this application.

Attending all the previous requirements, a crossover frequency between 600*Hz* and 2*kHz* is to be achieved by the current regulator, $H_i(s)$. The attenuation of the current loop gain at the switching frequency (5*kHz*) should be at least of about 15*dB*.

The modulation used in this application has been the space vector modulation developed in [9], which is effective in balancing the voltage of the DC-link capacitors.

5. DC Bus voltage regulation

If the NPC inverter had no losses, it would only inject reactive power and harmonics to the grid. An ideal active filter doesn't deliver active power to the grid, so that the DC bus voltage is constant once the capacitors have been charged, and no voltage loop is necessary. In a practical active filter a voltage loop is necessary to keep the DC-link voltage constant in spite of the inverter losses. The DC bus voltage level is controlled by acting on i_d (responsible for the active power), following the control structure of Fig. 3(a), which can be simplified according to Fig. 3(b). As is was explained in section 3, the reference for the active filter current in the *d*-channel, $\hat{i}_{d-ref}(s)$, is synthesized by means of subtracting from of the *d*-output of the reference generator, $\hat{i}_d^*(s)$, the voltage regulator output, $\hat{i}_{d-bus}^*(s)$.

In figures 3(a) and 3(b) four new small-signal transfer functions arise:

- $H_v(s)$, the transfer function of the voltage regulator.

- $G_{BUS}(s)$, the transfer function from $\hat{i}_d(s)$ current to the DC bus voltage, $\hat{v}_{bus}(s)$.

- $G_i(s)$, the closed loop transfer function from $\hat{i}_{d-ref}(s)$ to $\hat{i}_d(s)$.

- $T_v(s)=H_v(s)\cdot G_i(s)\cdot G_{BUS}(s)$, the loop gain of the voltage loop.

For the derivation of $G_{BUS}(s)$ it has been taken into account that the DC-link capacitors unbalance is compensated with a dynamics much faster than that of the DC-link voltage control. Therefore, it has been considered that the average value of the NP current 'seen' by the DC-link regulator is zero. Thus, it has been considered that the same current i_{dc} goes through both capacitors of the DC-link. Neglecting converter losses,

the active powers in the DC and AC sides of the converter are equal, so that equation (20) is fulfilled. In (20) the variables can be considered as averaged with a frequency much higher than the DC-link regulator working frequencies.

$$p = i_{dc} \cdot v_{BUS} = v_d \cdot i_d \tag{20}$$

Considering that both capacitors of the DC-link have the same capacitance C, equation (21) can be written, where the sign of i_{dc} is defined in Fig. 1(a).

$$i_{dc} = -\frac{C}{2} \cdot \frac{dv_{BUS}}{dt} \tag{21}$$

Substituting (21) into (20), equation (22) results.

$$-\frac{C}{2} \cdot \frac{dv_{BUS}}{dt} = \frac{v_d}{v_{BUS}} \cdot i_d \tag{22}$$

From (22) a small-signal model can be obtained by means of perturbation and linearization around an operation point. Supposing that the grid voltage doesn't undergo disturbances ($\hat{v}_d = 0$), expression (23) results, where V_d is the steady state grid voltage d-component, V_{BUS} is the bus voltage in steady state, and C is the capacitance of each of the capacitors of the DC bus.

$$-\frac{C}{2} \cdot \frac{d\hat{v}_{BUS}}{dt} = \frac{V_d}{V_{BUS}} \cdot \hat{i}_d \tag{23}$$

Applying the Laplace transform to (23), supposing null initial conditions, expression (24) results. $G_{BUS}(s)$ is the transfer function that allows controlling the DC-link voltage by acting on i_d.

$$G_{BUS}(s) = \frac{\hat{v}_{bus}(s)}{\hat{i}_d(s)} = -\frac{V_d}{V_{BUS}} \cdot \frac{2}{C \cdot s} \tag{24}$$

From figures 2 and 3(a) the closed loop transfer function of the d-channel current, from $\hat{i}_{d-ref}(s)$ to $\hat{i}_d(s)$, can be derived, following (25).

$$G_i(s) = \frac{\hat{i}_d(s)}{\hat{i}_{d-ref}(s)} = \frac{T_i(s)}{1 + T_i(s)} \tag{25}$$

The voltage regulator, $H_v(s)$, is designed for cascade compensation of $-G_i(s) \cdot G_{BUS}(s)$, which is very similar to an integrator with some gain in the low frequency range, where the crossover frequency of the voltage loop gain is placed.

The following practical issue limits the bandwidth of the voltage regulator. The implemented space vector modulation doesn't totally eliminate the NP voltage ripple when working with a high modulation index [10], which is the current case. By the effect of the modulator, the NP 150*Hz* voltage ripple becomes a smaller 300*Hz* voltage ripple. This voltage ripple appears in the DC bus from which the voltage regulator is fed back, so

that the regulator works to compensate it producing an undesired 300*Hz* component at the reference, $i_{d\text{-}ref}$, of the active filter i_d current. This fact is illustrated by figures 3(a) and 3(b). Summing up, a high 300*Hz* harmonic at the output of the voltage regulator would disturb the i_d 300*Hz* component of the current regulator. Therefore, the crossover frequency of the voltage loop is limited in practice to about 50*Hz* in order to properly attenuate the 300*Hz* harmonic coming from the DC-link.

6. Description of the proposed Robust Model Following control structure

A robust model-following control (RMF) technique derived from [5] [6] is proposed for both the current and the voltage loop with two goals: to increase the current harmonics reduction of the active filter, and to improve the dynamic response of the DC-link voltage to load steps. A major property of RMF is that the resulting loop gains don't need a high crossover frequency, so that robustness to modelling errors and noise is achieved. In this paper the dynamic performance of RMF controllers in the voltage and current loop is compared to that of conventional PI controllers.

6.1. Brief description of conventional PI control.

Fig. 4(a) shows a conventional cascade control loop, where:

- $H(s)$≡Controller transfer function.
- $P(s)$≡Any power stage transfer function to be compensated by $H(s)$.
- $T(s)= H(s)\bullet P(s)$≡Loop gain transfer function.
- $r(s)$, $e(s)$, $x(s)$ and $y(s)$ are the reference, error, control action and output signals, respectively.

Table 1 summarizes the general expressions of the power stage transfer functions and of suitable conventional PI controllers, both for the current and for the voltage loop.

6.2. Description of the proposed RMF control structure.

Fig. 4(b) shows the proposed RMF control structure, where the following new transfer functions arise:

- $G_{me}(s)$≡Modelling error controller.
- $G_{ref}(s)$≡Reference model of the power stage.
- $G(s)$≡External controller.
- $T_{int}(s)$≡Internal loop gain.
- $T_{ref}(s)$≡Reference loop gain
- $T_{ext}(s)$≡External loop gain.

Table 2 summarizes the proposed general expressions of the RMF controllers and loop gains, both for the current and for the voltage loop.

Fig. (4b) proposes 3 individual controllers with 3 associated loop gains. It can be shown that the RMF control structure can be reduced to that of Fig. 4(c), where:

- $H_{eq}(s)$≡Equivalent controller transfer function.

- $P(s)$≡Any power stage transfer function to be compensated by $H_{eq}(s)$.

- $T_{eq}(s)= H_{eq}(s)\cdot P(s)$≡Equivalent loop gain transfer function.

The properties of RMF control are the following ones:

1) A high order equivalent controller, $H_{eq}(s)$, is obtained by means of 3 simple controllers, whose design is performed by means of easy loop shaping of 3 individual loop gains. In that sense, complicated controllers are obtained, similar to those typical of H_∞ control, without the need of trial and error efforts for the tuning and weighting functions selection.

2) Neither the individual loop gains nor the equivalent loop gain need high crossover frequencies, so that robustness is achieved combined with a good dynamic response.

3) The design has more degrees of freedom than those of simple PI control.

4) The low frequency behaviour of the equivalent controller is that of a double integrator, improving the tracking of low frequency reference signals, and reducing the loop sensitivity to external disturbances like load changes or DC-link voltage changes.

RMF can be applied to all the control loops in a converter, or only to some of them. In the case of the present active filter based on an NPC converter, it can be applied to both the current and the voltage loop, as it will be shown in the following section. For comparison purposes PI regulators for both loops have been also designed.

7. Design of RMF control vs. conventional PI control

For the design of the controllers it is necessary to know the values of the VSI passive components, DC-link voltage, grid voltage, and so on. The active filter works as a current source connected in parallel to the load as shown in Fig. 1(a). The line voltage of the grid is 1*kV*. The output inductance of the VSI is *L*=2*mH*, the capacitance of each of the series-connected DC-link capacitors is C=1*mF*, and the DC-link voltage is V_{BUS}=2*kV*. The switching frequency is f_S=5*kHz*.

The nonlinear load generating current harmonics consists of a three-phase non-controlled rectifier with line inductors, L_L, an output capacitive filter, C_L, in parallel to a resistive load, R_L. The apparent power of the nonlinear load is *S*=200*kVA*, with L_L=1.44*mH*, C_L=200μ*F* and R_L=9.25Ω.

7.1. Design procedure of conventional PI controllers.

As it has been shown in sections 4 and 5, the control structure of the active filter consists of an inner current loop (in the d and q channels) inside an outer voltage loop. Therefore, the current regulator must be designed before the voltage regulator, either with a PI design procedure or with an RMF procedure.

The proposed design procedure of the PI regulators, following the structure of Fig. 4(a), is as follows:

1) Choose a stabilizing controller, $H(s)$, with the format of Table 1, for cascade compensation of $P(s)$.

In the case the current loop, consider $P(s)=Gid_{diag}(s)$ (17a), and in the case of the voltage loop, take $P(s)= -G_i(s)\cdot G_{BUS}(s)$ (24) (25).

2) Check the crossover frequency f_c and the stability margins of the loop gain, $T(s)$ (Table 1), both of the current and of the voltage loop.

In the case the current loop it should be chosen a crossover frequency $600Hz< f_c \leq 0.4\cdot f_S$ ($2kHz$), as it was explained in section 4. In the case of the voltage loop it should be chosen $f_c \leq 50Hz$, for the reasons explained in section 5.

Table 3 shows the exact expressions of the power stage, the design values of the regulators, the resulting crossover frequencies (f_c) and phase margins (*PM*) when using conventional PI control, both for the current and for the voltage loop.

7.2. Design procedure of the proposed RMF controllers.

The proposed design procedure of the RMF regulators, following the structure of Fig. 4(b), is the following one:

1) Choose a stabilizing controller, $G_{me}(s)$, with the format of Table 2, for cascade compensation of $P(s)$.

In the case the current loop, consider $P(s)=Gid_{diag}(s)$ (17a), and choose $f_{C\text{-}int} \leq 0.4\cdot f_S$ ($2kHz$) of the loop gain $T_{int}(s)$ (Table 2). In the case of the voltage loop, take $P(s)= -G_i(s)\cdot G_{BUS}(s)$ (24) (25), and $f_{C\text{-}int} \leq 50Hz$.

2) Choose a modelling error controller, $G_{ref}(s)$, with the format of Table 2, in order to have a stable loop gain $T_{ref}(s)$ (Table 2) with the previously chosen $G_{me}(s)$. The resulting crossover frequency, $f_{c\text{-}ref}$, is easy to maximize because $T_{ref}(s)$ is composed by transfer functions that do not vary with the inverter operation point. Note that there are two degrees of freedom, $K_{ref\text{-}i}$ and $\omega_{i\text{-}ref}$, in the design of $G_{ref}(s)$ in the case of the current loop, but there is only one degree of freedom in the case of the voltage loop (Table 2).

In the case the current loop, choose $f_{C\text{-}ref} \leq 0.4\cdot f_S$ ($2kHz$). In the case of the voltage loop, take $f_{C\text{-}ref} \leq 50Hz$

3) Choose $G(s)$, with the format of Table 2, in order to have a stable loop gain $T_{ext}(s)$ (Table 2).

In the case of the current loop, choose $f_{C\text{-}ext} \leq 0.4\cdot f_S$ ($2kHz$). In the case of the voltage loop, take $f_{C\text{-}ext} \leq 50Hz$.

4) Check the crossover frequency, $f_{c\text{-}eq}$, and the stability margins of the equivalent loop gain, $T_{eq}(s)$, both of the

current and of the voltage loop.

In the case the current loop it should result a crossover frequency $600Hz < f_{c\text{-}eq} \leq 0.4 \cdot f_S$ ($2kHz$), for the reasons explained in section 4. In the case of the voltage loop it should result $f_{c\text{-}eq} \leq 50Hz$, as it was explained in section 5.

Table 4 shows the exact expressions of the power stage, the design values of the regulators, and the resulting crossover frequencies ($f_{c\text{-}eq}$) and the phase margins (PM) of the equivalent loop gains applying RMF control, both of the current and of the voltage loop.

7.3. Discussion about PI vs. RMF control.

It can be found in table 3 that the crossover frequency of the current loop with the PI regulator results f_c=643Hz, with a phase margin of 81.1^0 and an attenuation of 18dB at the switching frequency. The conventional PI regulator has not enough degrees of freedom to get enough switching frequency attenuation with a higher crossover frequency, which would be desirable for performing a good harmonics reduction by means of the active filter. On the contrary, the RMF regulator (table 4) has enough degrees of freedom for achieving a higher equivalent crossover frequency of the current loop $f_{c\text{-}eq}$=1.59kHz with a phase margin of 54.2^0 and a similar attenuation (16dB) at the switching frequency. Fig. 5(a) shows the Bode plots of the current loop gain with PI controller and with the equivalent RMF controller.

It's important to notice from Fig. 5(a) that the DC regulation error in dq coordinates (i.e., at the 50 Hz fundamental in abc coordinates) of the current loop is zero when using RMF control, because the theoretical DC gain of $T_{i\text{-}eq}(s)$ is infinite. Unlike RMF control, there is a finite DC gain of $T_i(s)$ with PI control, producing a DC regulation error in dq coordinates. Therefore, the fundamental reactive power will be totally compensated by the RMF equivalent controller but not with the conventional PI controller.

It is shown in table 3 that the crossover frequency of the voltage loop with the PI regulator results f_c=20.4Hz, with a phase margin of 90^0 and an attenuation of 23dB at 300Hz. The conventional PI regulator has not enough degrees of freedom to get a suitable 300Hz attenuation with a higher crossover frequency or with a higher low frequency gain, which would be desirable for the transient response of the DC-link voltage. On the contrary, the RMF voltage regulator (table 4) has enough degrees of freedom for achieving a higher equivalent crossover frequency of the voltage loop $f_{c\text{-}eq}$=50Hz with a phase margin of 47.6^0 and a similar attenuation of 22dB at 300Hz. Fig. 5(b) shows the Bode plots of the voltage loop gain with PI controller and with the equivalent RMF controller. It is worth pointing out that the low frequency gain of the voltage loop with RMF control is at least 20dB higher than that achieved by PI control in a wide low frequency range. The low frequency double

integrator behaviour (-40*dB/dec* slope) of the RMF regulator is responsible for that. Therefore, the transient response of the DC-link voltage to load steps, i.e., the load disturbance rejection, is expected to be significantly better with RMF control.

8. Simulation results

In order to validate the improvement of the current harmonics compensation and the better dynamic response of the converter to load steps achieved by RMF when compared with conventional PI control, the system was simulated by means of Saber™ [11]. The system parameters used in the simulations have been shown in section 7.

Load steps have been applied by simulation to the nonlinear load described in section 7, in order to check the converter dynamic response, with RMF vs. PI control. The bus voltage response with both control methods is shown in Fig. 6(a), where a step from 200kVA to 110kVA at t=130*ms* followed by a step back to 200kVA at t=210*ms* has been applied. The typical residual 300*Hz* ripple in steady state can be observed at the DC-link voltage. The RMF control response is faster than the response of PI control, as it was expected. The settling time of the DC-link voltage to an error less than 5% is: 10*ms* for RMF control vs. 30*ms* with PI control. Fig. 6(a) also illustrates that the DC bus withstands a *200V* transient overvoltage with RMF control and *400V* with PI control. Half of this overvoltage is applied to each of the DC bus capacitors and hence to the power transistors, so that RMF control improves the safety of the power transistors. Figures 6(b) and (c) illustrate the line currents achieved by the active filter, with PI and RMF controls, respectively, at the load steps previously described. It can be noticed that the line current waveforms are less distorted when using RMF control.

Fig. 7(a) shows the nonlinear load currents in steady state working with the nominal conditions described in section 7. Those load current waveforms have a distortion of $THD_i=34.9\%$.

Fig. 7(b) shows the currents injected by the active filter and the resulting line currents when working with conventional PI control. The same currents with RMF control are shown in Fig. 7(c).

From Figures 7(b) and (c) it can be noticed that the line current waveforms are less distorted when using RMF control. This fact is confirmed by Table 5, which shows the resulting line current THD in steady state with both control methods, PI vs. RMF, when working with the nominal conditions described in section 7. The improvement of the line current THD by means of RMF is really considerable, *13%* with PI vs. *6.5%* with RMF, specially taking into account the low switching frequency.

9. Conclusions

A robust model-following (RMF) control technique applied to a three-phase medium voltage shunt active filter implemented by means of a three level NPC converter has been shown in this paper. A small-signal model and its associated transfer functions have been derived in order to both control the currents injected by the active filter and to regulate the DC-link voltage. The RMF control method has been applied to both current and voltage loops, and confirmed by simulation. This method has been compared with conventional PI control of both loops. It has been shown that the dynamic response of the DC-link voltage to load steps is appreciably better with RMF control than with PI control, in terms of settling time and overshoot. At a nonlinear load step, the overvoltage at the DC-link capacitors and, consequently, at the power transistors is considerably lower with RMF control. It has been also demonstrated that the THD of the source current in steady state is much lower when using RMF control than with PI control. Moreover, the proposed method achieves a total reactive power compensation, which is not the case of conventional PI control.

10. Acknowledgments

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11. References

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TABLES

Table 1. General expressions of conventional PI control, both of the current and of the voltage loop.

Current control loop	Voltage control loop
$P(s) = k_{P\_i} \cdot \frac{s}{s^2 + \omega_0{}^2}$	$P(s) = \frac{k_{P\_v}}{s}$
$H(s) = k_i \cdot \frac{1 + s/\omega_i}{s}$	$H(s) = k_v$
Current and voltage loop gain	
$T(s) = H(s) \cdot P(s)$	

Table 2. General expressions of RMF control, both of the current and of the voltage loop.

Current control loop	Voltage control loop
$P(s) = k_{P\_i} \cdot \frac{s}{s^2 + \omega_0{}^2}$	$P(s) = \frac{k_{P\_v}}{s}$
$G_{me}(s) = \frac{k_{me\_i}}{s} \cdot \frac{1 + s/\omega_{i1}}{1 + s/\omega_{i2}}$	$G_{me}(s) = k_{me\_v}$
$G_{ref}(s) = k_{ref\_i} \cdot \frac{1 + s/\omega_{i\_ref}}{1 + s/\omega_{i1}}$	$G_{ref}(s) = \frac{k_{ref\_v}}{s}$
$G(s) = \frac{k_{\_i}}{s} \cdot \frac{1 + s/\omega_{i1}}{1 + s/\omega_{i2}}$	$G(s) = \frac{k_{\_v}}{1 + s/\omega_v}$
Current and voltage control loops	
Internal loop gain	$T_{\text{int}}(s) = G_{me}(s) \cdot P(s)$
Reference loop gain	$T_{ref}(s) = G_{me}(s) \cdot G_{ref}(s)$
External loop gain	$T_{ext}(s) = G(s) \cdot GU(s)$ $GU(s) = \frac{\hat{y}(s)}{\hat{u}(s)} = P(s) \cdot \frac{1 + G_{me}(s) \cdot G_{ref}(s)}{1 + G_{me}(s) \cdot P(s)}$
Equivalent loop gain	$T_{eq}(s) = H_{eq}(s) \cdot P(s)$ $H_{eq}(s) = G_{me} + G + G_{me} \cdot G \cdot G_{ref}$

Table 3. Design values of conventional PI control, both of the current and of the voltage loop.

Current control loop	Voltage control loop
$P_i(s) = 5 \cdot 10^5 \cdot \frac{s}{s^2 + 314^2}$	$P_v(s) = \frac{985}{s}$
$H_i(s) = 5 \cdot \frac{1 + s/630}{s}$	$H_v = 0.13$
Current and voltage control loops	
	f_c**(Hz)**	***PM(deg)***
Current loop gain T_i	643	81.1
Voltage loop gain T_v	20.4	90

Table 4. Design values of RMF control, both of the current and of the voltage loop.

Current control loop	Voltage control loop
$P\_i(s) = 5 \cdot 10^5 \cdot \frac{s}{s^2 + 314^2}$	$P\_v(s) = \frac{985}{s}$
$G_{me\_i}(s) = \frac{5}{s} \cdot \frac{1 + s/314}{1 + s/16000}$	$G_{me\_v}(s) = 0.13$
$G_{ref\_i}(s) = 50 \cdot \frac{1 + s/950}{1 + s/314}$	$G_{ref\_v}(s) = \frac{985}{s}$
$G\_i(s) = \frac{2}{s} \cdot \frac{1 + s/314}{1 + s/16000}$	$G\_v(s) = \frac{0.32}{1 + s/380}$
Current and voltage control loops	
	$f_{c\text{-}eq}$**(Hz)**	***PM(deg)***
Equivalent current loop gain $T_{i\text{-}eq}$	1590	54.2
Equivalent voltage loop gain $T_{v\text{-}eq}$	50	47.6

Table 5. Source current THD in steady state and nominal working conditions.

	i_s **THD**
Without active filter	34.9%
With active filter, PI	13%
with active filter, RMF	6.5%

FIGURES AND FIGURE CAPTIONS

FIGURE CAPTIONS

Fig. 1 (a) Three-level NPC VSI shunt active filter in parallel with a nonlinear load. (b) Equivalent switching structure for the NPC converter.

Fig. 2. Diagonal control structure of the active filter currents in synchronous dq coordinates. Note that both channels are identical, because $Gid_{dd}(s)=Gid_{qq}(s)\equiv Gid_{diag}(s)$. Decoupling terms have been added to output of the current regulators.

Fig. 3. (a) Block diagram of the DC-link control loop. (b) Simplified block diagram of the DC-link control loop.

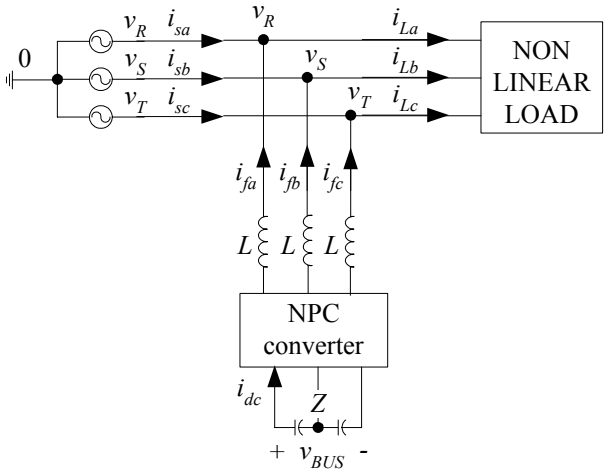
Fig. 4. (a) Conventional cascade control structure. (b) Proposed Robust Model-Following control structure. (c) Equivalent cascade control structure of RMF control.

Fig. 5. (a) Bode plots of current loop gains $T_i(s)$ (conventional PI control) and $T_{i\text{-}eq}(s)$ (RMF control). (b) Bode plots of $T_v(s)$ (conventional PI control) and $T_{v\text{-}eq}(s)$ (RMF control).

Fig. 6. (a) DC-link voltage for nonlinear load steps with conventional PI and RMF controls. (b) Line currents for nonlinear load steps with PI control. (c) Line currents for nonlinear load steps with RMF control.

Fig. 7. (a) Nominal nonlinear load currents in steady state. (b) Line currents and active filter output currents in steady state with PI control. (c) Line currents and active filter output currents in steady state with RMF control.

FIGURES



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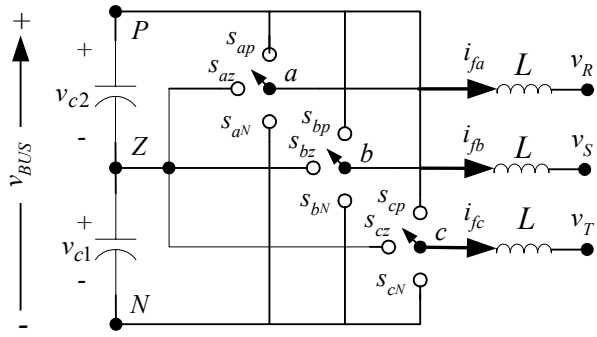

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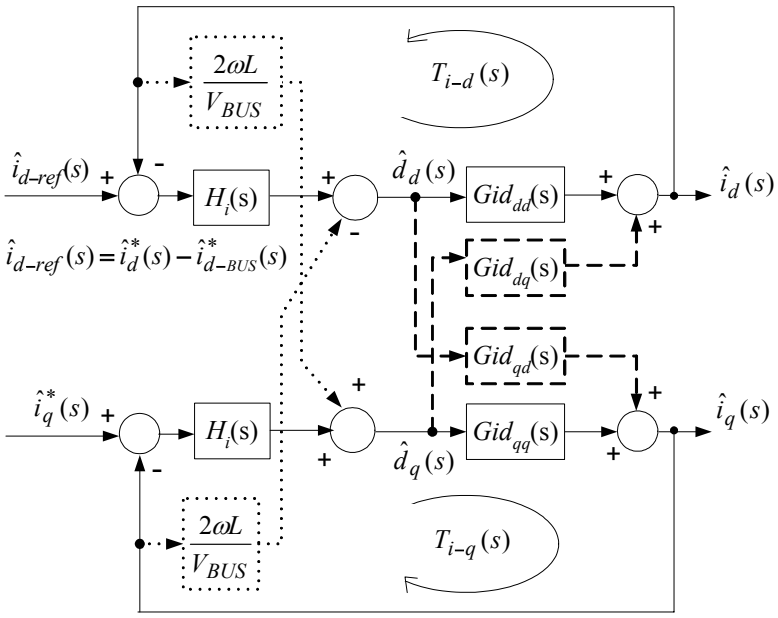

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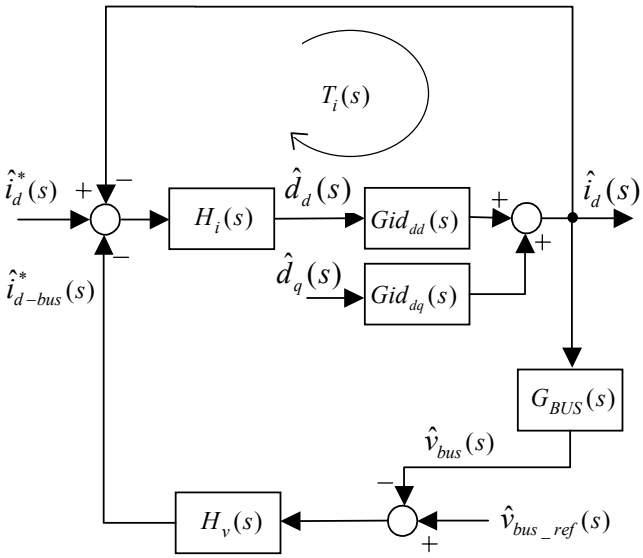

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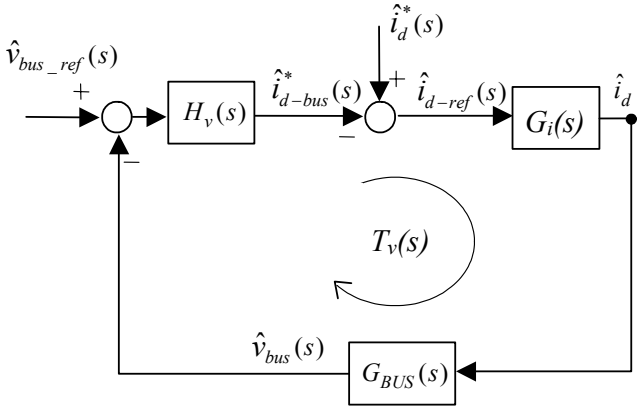

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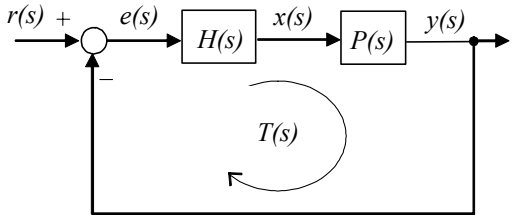

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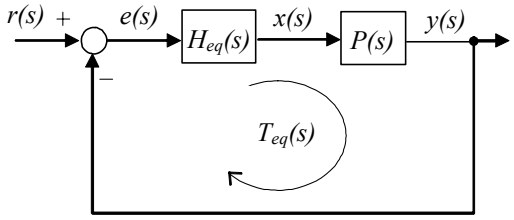

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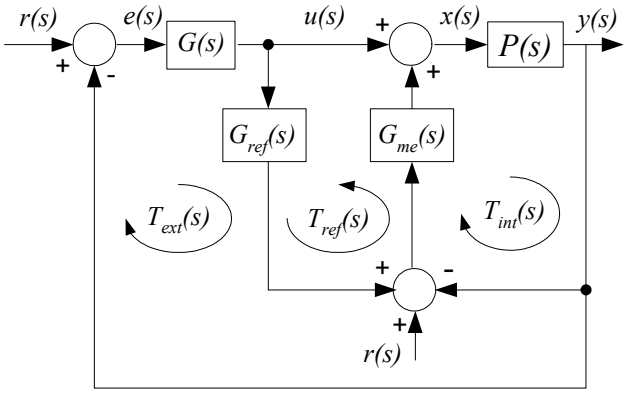

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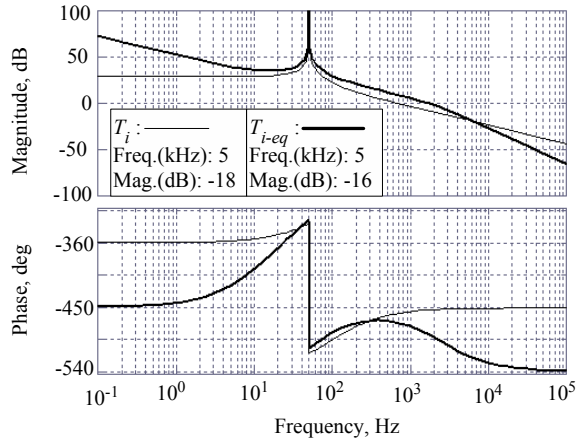

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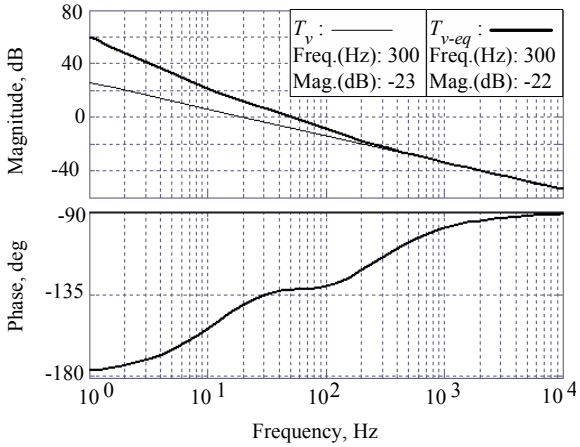

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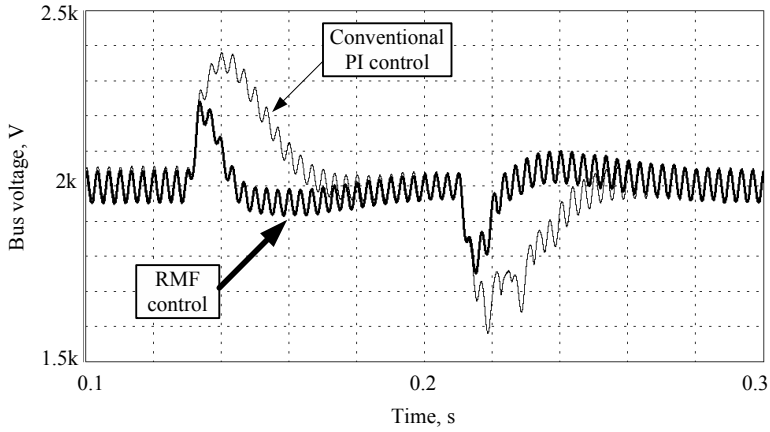

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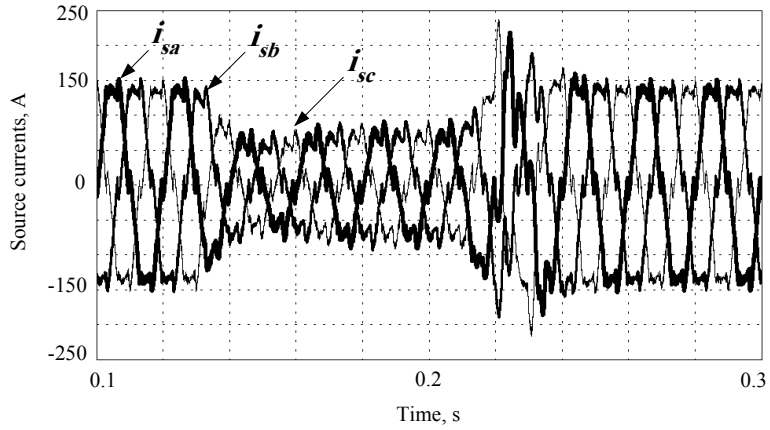

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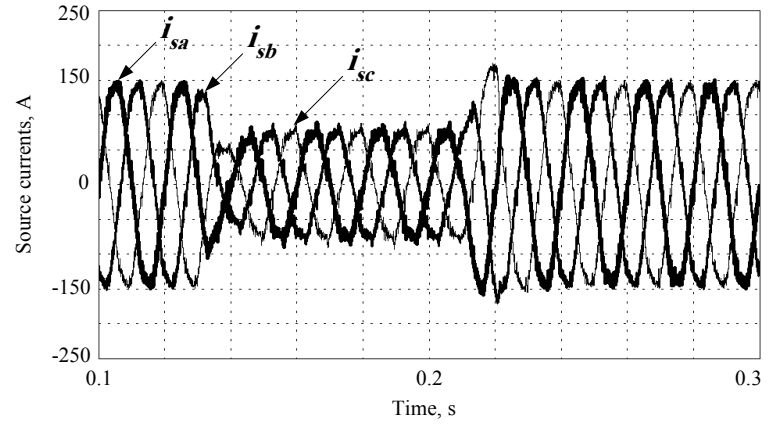

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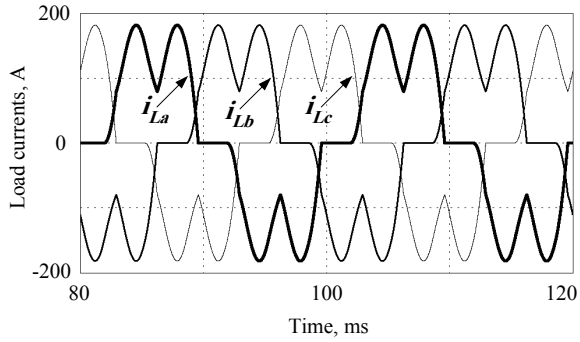

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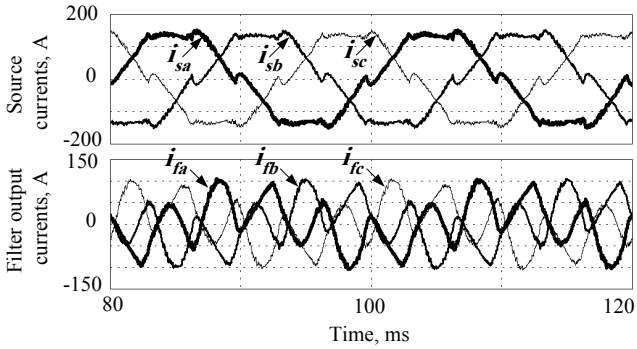

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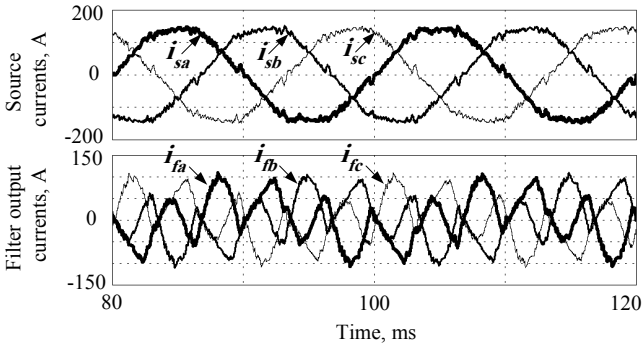

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