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"Speed Optimization of a Multilayer-Board for Multi-Gigabit/s Chip-to-Chip Interconnects"

TRABAJO FINAL DE CARRERA

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Speed Optimization of Multilayer-Boards for Multi-Gigabit/s Chip to Chip Interconnects

Cristina Pleite Moreno
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Abstract

The main aim of this project is to increase the data rate communication between a CPU and a DRAM to above 6.5 GHz by optimization of the Printed Circuit Board (PCB) interconnections (these interconnections include vias, transmission lines and steps), as it's shown in Figure I.

The modeling has been performed using the Electro-Magnetic (EM) simulator HFSS (High Frequency Structure Simulator), a 3D full-wave electromagnetic field software that can be used in circuit, high frequency, signal integrity, and electromechanical simulations, up to 100GHz.

The modeled passive components have been used in the optimization of the Bit Error Rate (BER) and eye-diagram of the total system, including the parasitic elements of the CPU and DRAM packages by using HSPICE and ADS simulators.

In addition, a complete library of these passive structures has been prepared.

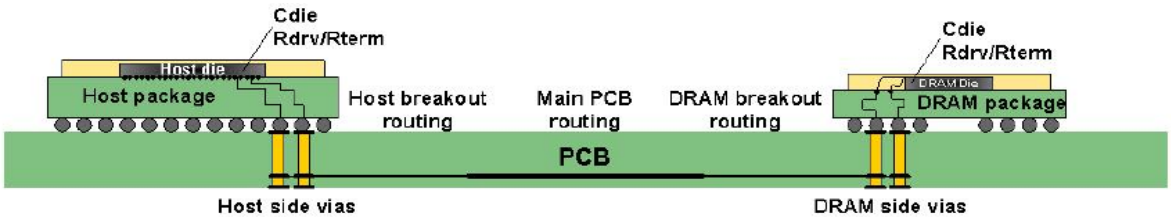


Figure I. Circuit to be optimized

Acknowledgements

I have many people to thank and I would like to start with my professor, Georg Böck, for giving me the opportunity to learn from this great team, the chance to live this unique experience and of course, because without his offer I wouldn't be now writing these lines. All the colleagues at TUB's Microwave Department for all their help and for making my eight months here unforgettable, specially to Amin, who has been a work-mate, a teacher and a friend, and probably the best one I could ever had.

Ana, Cris, Alex, Javi, Arquitos, David, Neus, Marieta, Caminos, Fani, Toni. Most of you have been in my life since I am conscious of it and I am enormously lucky to have you still in it. For one reason or other, or many I would say, you are true friends who have stood there for me through life phases, the good moments and maybe through many more bad ones. Life goes by, we grew up together and now each one follows a different path, but we're still the best of friends and makes me very happy to guess that no matter what it will always be that way.

I've been very lucky to come across great people through all these years; teachers, friends, work-mates, 'family' or strangers. They are so many that I will fill in pages just naming them and I would probably still forget someone at this point, but I need to thank them all as well for being or having been in my life, for their help and for those little unforgettable moments that fill in one's life.

Por ultimo, pero no por ello menos importante, quiero dedicar este trabajo a toda mi familia y en especial a mis padres, Jose y Casilda, por su apoyo incondicional durante toda mi vida y en todas mis decisiones y por la educacion que me han brindado, pues todo lo que he sido y todo lo que soy se lo debo y agradezco a ellos. Tambien a mi abuela, por una vida representando para mi la fuerza, el coraje, la felicidad y el valor para seguir adelante y por ser mi modelo a seguir.

Table of contents

1. Introduction

This is a Signal Integrity (SI) project with the aim of increasing the data rate communication between a CPU and a DRAM up to above 6.5 GHz by optimizing the Printed Circuit Board's (PCB) interconnections (including vias, transmission lines and steps).

SI influences on many electronic design disciplines. However, problems concerning this integrity have become much more common over the past few years. Nowadays, these SI problems are more frequent and worse than before due to the processors' clock velocities, which have been multiplied by several orders of magnitude. The speed increase has strongly influenced the integrated circuits (IC), yet, for physical reasons, PCBs have not evolved at the same pace. The propagation time of the buses that interconnect chips has not changed considerably for years. The sizes have decreased, but there is still the need to improve PCBs to make them more suitable to the actual ICs, connectors, passive components or bus paths, because today's PCBs add distance and distance means time, a speed's enemy.

The following paper aims at studying the contribution of each passive structure in the PCB to the signal distortion and minimize it in order to achieve the best possible signal quality. Eye diagrams are used for the sake of graphing the quality of the transmission. As the eye opens looking more like the ideal one, the signal is more likely to pass the threshold, retransmission won't be needed and this increases the data rate communication.

In order to study the contribution of the passive structures, they have been modeled with HFSS and simulated either with HSPICE or ADS. First of all, different sections of the transmission line, differing in width and spacing, were modeled with HFSS to study the effects of the steps. The simulations therefore were carried out with HSPICE and the eye diagram was plotted using MATLAB. Secondly, the vias, which are considered a major reason for discontinuity, were analyzed. With a 3D HFSS microwave structure, the transmission lines coming out of the via were shifted for different layers and by means of ADS simulated along with the via to examine its behavior. An equivalent model for the vias was prepared using ADS with the aim of saving time while simulating. Finally, the effect of the packaging interconnects was taken into account to study the behavior of the communication between the CPU and the DRAM, resulting in the finding that the parasitics introduced by the package are the major SI problem.

The following project examines the behavior of some passive structures at a very high frequency in a range from 0 to 100 GHz. At these frequencies many problems occur and they affect the signal integrity. Hence, the goal in this project is to find the problems that affect the SI preventing the communication from being good, reliable and high-speed.

1.1 Description Of Components And Tools

Printed Circuit Board (PCB):

The PCB under study has a stack-up as shown in Figure 1.1, with 12 layers where 4 of them are internal signal layers. All the layers are linked through pairs of differential vias that go from the top to the bottom layer and allow a signal to flow through all the planes. [1]

Figure 1.1. PCB stack up

Host package (CPU):

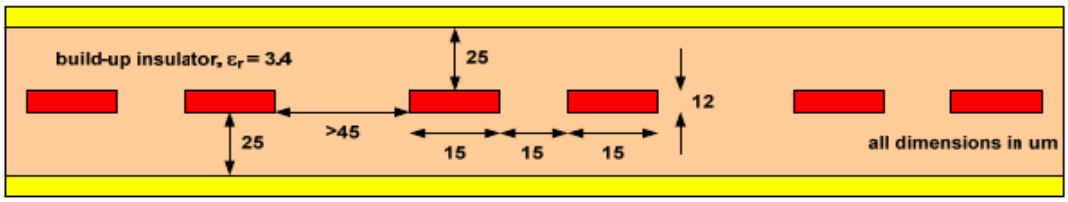


Figure 1.2. Diff-breakout region

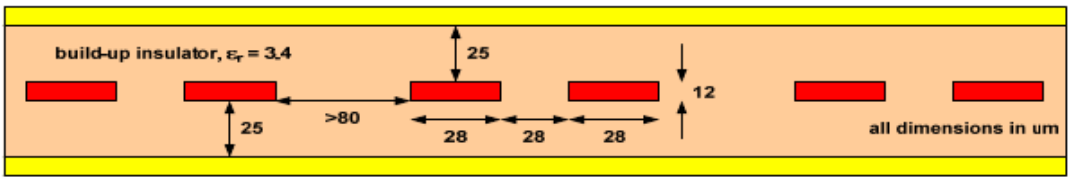


Figure 1.3. Diff-FANout region

DRAM package:

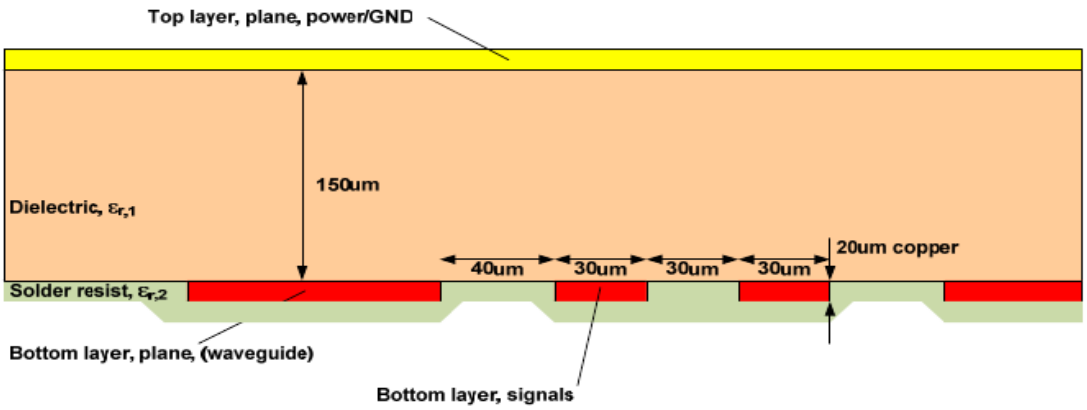


Figure 1.4. DRAM package

Tools:

HFSS (High Frequency Structural Simulator) is a high efficiency simulator of electromagnetic fields used to model 3D devices. Solutions to 3D electromagnetic problems are provided fast and accurate by using the Finite Element Method (FEM). HFSS is here used to model all passive structures. [17]

ADS (Advanced Design System) is an electronic design software for RF, microwave, and high speed digital applications that allows to characterize and optimize an RF design just by using the same tool. In this project, ADS has been used to simulate some passive structures behavior and to model the vias. [16]

HSPICE (Simulation Program with Integrated Circuit Emphasis) is an accurate circuit simulator that enables to accelerate simulations. HSPICE’s recursive convolution algorithm can quickly and accurately simulate S-parameters with over one thousand ports for large packages and other applications. [10], [18]

MATLAB (MATrix LABoratory) is a mathematical software that offers an integrated development environment with an own programming language called M. MATLAB has been used to represent the simulation results in an eye diagram and to plot the package's characteristics. [18]

1.2 Phases Of Realization

In order to find the reasons why the eye diagram was not opening more, the complete structure has been simulated.

First of all, vias and transmission lines were modeled using HFSS and simulated together with HSPICE, taking into account only one differential via and placing the output transmission lines in different layers (layers 2, 5, 8 and 10). Results are shown in chapter 4.2 (EM Simulations).

Secondly, transmission lines and vias have been simulated separately also using HSPICE, but now with steps on them. The width of the transmission lines has been swept from 3.1 mil to 5.1 mil with a step of 0.5 mil, and the spacing between the differential transmission lines has also been swept between 2 and 4 mil with a spacing of 0.5 mil. The modeling has been performed with HFSS and the results can be seen in chapter 4.3 (Interconnection Characteristics).

The next step was to simulate the complete passive structure, now including the packages in the CPU and the DRAM with the aim of finding how the packages would affect the performance of the eye diagram. It was found that the packages itself are a low pass filter that really deteriorate the eye diagram and they worse signal integrity. Results are shown in chapter 4.4 (Effect Of The Packaging).

Finally, a model for the vias has been made using ADS. There are models for the vias when the output transmission lines are in layers 2, 5, 8 and 10. This is shown in chapter 4.5 (Via Modeling).

2. Introduction to Signal Integrity

Signal Integrity (SI) is an engineering field that has the aim of improving design, reliability and performance of digital systems. Because signal integrity is such a multidisciplinary field involving fields within the electrical engineering discipline such as microwaves, RF, Very Large Scale Integration (VLSI) and signal processing but also other fields such as modeling, stamping and contact physics which are in the mechanical engineering or physics field, researchers have to interplay among disciplines in the analysis and design of a working interconnect prototype.

The high frequencies at which modern hardware systems work in addition with the emphasis in low power consumption in electronic devices pushes towards two clear new goals in the development of new products: decreasing signal voltage levels and higher signal to noise ratio (SNR).

Nowadays technologies demand high speed, small size and low power consumption. In order to accomplish these characteristics, electrical effects that could previously be ignored have to be now taken into account using new design practices.

2.1 Signal Integrity Problems

As frequencies increase, a variation of the original signal occurs along the circuit and as a result, the received signal can be distorted. This variation or distortion of the original signal at a high frequency can be caused for many reasons, but these signal integrity problems usually appear at all levels of electronic packaging, they may occur at a chip-to-chip level as well as through the package and the PCB.

Most common signal integrity problems at these levels are interconnect crosstalk, substrate coupling, power and ground grid noise and power electromigration. EMI

Crosstalk is a major SI problem, it can hurt both timing and functionality. When a signal switches, the voltage waveform of a neighboring net may be affected due to cross-coupling capacitance between interconnects. This effect is called crosstalk. It occurs because as chips get smaller, there is a high density of electronic components, traces, vias and layers and they get closer to each other so the coupling capacitance becomes a significant factor, and induces crosstalk effects that cannot be ignored. Due to the coupling, which can be either capacitive or inductive, an unintentional interference between one signal in a neighbor wire, called aggressor, can couple a closer trace or circuit for which a victim signal is propagating, causing distortion on it (see Figure 2.1). Crosstalk analysis determines the noise induced on a net (the victim) by its switching neighboring nets (the aggressors). [15].

Capacitive crosstalk affects the slew rate, which has consequences on transition delay and this either lowers the operative frequency of the chip or makes the chip fail intermittently. Therefore, the operative frequency of the chip is lowered because of a delay degradation while intermittent chip failure is due to a voltage pulse induced in an inactive victim by the switching of one or more neighbor aggressors.

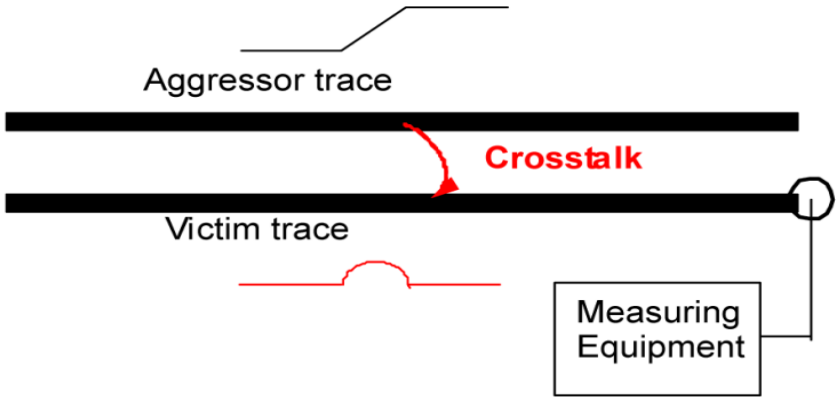


Figure 2.1. Crosstalk

In integrated circuits, all circuits share the same substrate no matter if they are digital, analog or RF circuits. Digital circuits can generate undesired noise currents usually by fast switching from low to high. Since the substrate underneath the circuits is not fully isolated, the noise generated by the digital circuits can easily be injected into the substrate and propagate throughout the entire chip. The noise coming from the digital circuits and propagating through the substrate is called substrate noise, and it affects the sensitive circuits´ performance. Substrate noise generation by capacitive coupling is due to parasitic capacitances.

Power and ground planes and vias form a power distribution network which is usually very complex, what makes it difficult to pattern the electromagnetic effect that the power and ground noise introduce. The big amount of devices changing simultaneously induce transitional currents that can cause fluctuations of voltage between power and ground planes which translates to noise. This noise is either called Simultaneous Switching Noise (SSN), Delta-I noise, or power/ground bounce.

SSN will cause logic error when it couples to inactive signal nets or will mess up the data to be received. It may introduce common mode noise and it may increase radiation at resonant frequencies.

Signal electromigration is a transfer of mass that occurs in a metal as a result of the ions movement under the influence of an electric current. Electromigration causes damage to the metal in an integrated circuit and the transfer of mass may cause shorts or open circuits on neighbor wires. As the size in integrated circuits decreases, the significance of this effect increases. [13]

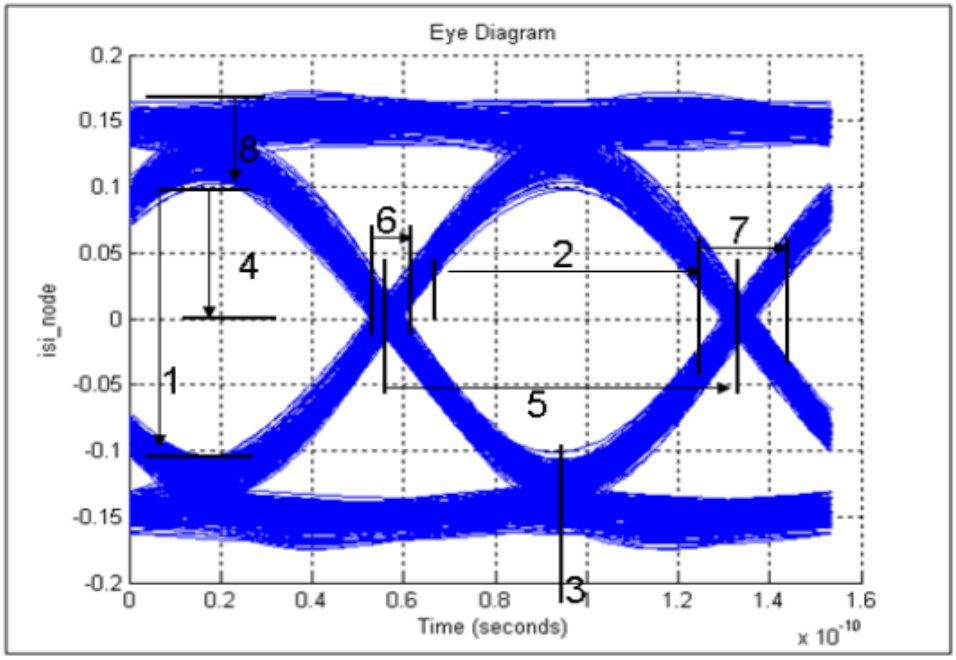
Nowadays, the package interconnection is a bottleneck of high speed design. Packaging design is very important in signal integrity because since the frequency of digital signals is increasing, the package interconnections have to be able to support very fast signals without degrading them to unacceptable levels. Wave propagation, reflection, coupling and resonance are typical EM’s phenomenon that happen inside a packaging during signal transients.

2.2 Definitions

SI in digital circuits may be affected by a deficient path of the PCB, an inappropriate use of the transmission lines properties, coupling between signals, reflections in the transmission lines, parasitics of some components or overload of some circuits.

Stated below are some explanations of SI issues that are relevant in this project or common SI problems that have to be faced.

Eye diagram:



1 → Eye opening
2 → Interval that can be sampled
3 → Best sampling instant
4 → Noise margin
5 → Sampling interval
6 → Distortion in zero crossings
7 → Distortion in zero crossings at 20mV
8 → Greatest distortion

Figure 2.2. Eye diagram and its most important parameters.

An eye diagram is a practical way of studying the effects of noise and distortion (ISI) in a system. The region inside of the eye is called eye opening, and its shape determines the quality of the system. It gives some practical information about the systems performance.

The figure above (Figure 2.2) is an example of an eye diagram with its most important parameters. Eye diagrams allow to find the best sampling instant, the noise margin, the distortion at the sampling instant and the sensibility to timing errors among

other information.

The eye opening widely gives the interval of time during which the signal can be sampled without error whereas the high of the eye sets the margin above the noise threshold for a sampling instant. When the eye closes, the system is not immune to the noise and it is impossible to avoid errors.

Jitter can be caused by amplitude noise, but it is the amount of phase noise at crossing times, so the phase noise (a continuous function of time) can also cause Jitter (a discrete quantity). Jitter causes errors when the timing of a signal transition fluctuates horizontally across the sampling point. The sampling point is the point in voltage and time where the receiver determines whether a bit is a logic one or zero. In Figure x, Jitter is a causer of distortion in zero crossings (6); Jitter causes errors when the signal fluctuates horizontally.

Signal-to-noise ratio is important for the same reason as jitter. A low SNR means a high bit error ratio (BER). So, a low SNR causes bit errors when the signal fluctuates vertically across the threshold ((8) in Figure 2.2). [15].

Differential signaling:

Two traces on a strip geometry are coupled and sourced with signals of equal magnitude (even-mode propagation) and 180° phase shift between them (odd-mode propagation) as can be seen in figures 2.3 and 2.4.

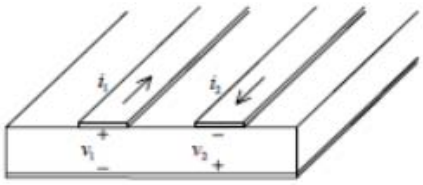


Figure 2.3. Odd-mode propagation

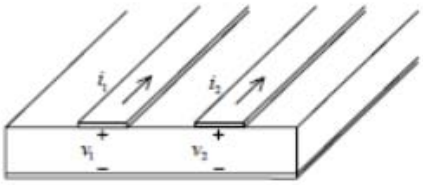


Figure 2.4. Even-mode propagation

Differential signaling has become very used for multi-Gigabit digital applications due to its low noise generation and its large immunity to external common-mode noise, reflection noise and signal attenuation. It also reduces Electromagnetic Interference (EMI) because since the currents are flowing in opposite directions it results in a cancellation of the magnetic field. [7].

ElectroMagnetic Interference (EMI):

Electromagnetic waves exist in nature as a result of the radiation from atoms or molecules when they change from one energy state to another and by natural fluctuations.

EMI is electromagnetic energy that adversely affects the performance of electrical/electronic equipment by creating unwanted responses or complete operational failure of the circuit. EMI is caused by undesirable radiated electromagnetic fields or conducted voltages and currents. The interference is produced by a source emitter that may be any object that carries rapidly changing electrical currents and can be external or internal to the electrical or electronic equipment and they may propagate by radiation or conduction and it is detected by a susceptible victim via a coupling path. Most conducted coupling from external sources occurs through the ac power lines.

EMI can be intentionally used or can occur unintentionally as a result of spurious emissions.

The most common methods of noise reduction include proper equipment circuit design, shielding, grounding, filtering, isolation, separation and orientation, circuit impedance level control, cable design, and noise cancellation techniques. [9].

Power/Ground noise:

Power/ground noise is one of the most difficult EM effects to be modeled in SI analysis because of the complexity of the power/ground distribution system.

In chip package and printed circuit board, power/ground planes with visa form power distribution networks. Transient currents drawn by a large number of devices switching simultaneously can cause voltage fluctuations between power and ground planes, namely the simultaneous switching noise (SSN), or Delta-I noise, or power/ground bounce. SSN will slow down the signals due to imperfect return path constituted by the power/ground distribution system. It will cause logic error when it couples to quiet signal nets or disturbs the data in the latch. It may introduce common mode noise in mixed analog and digital design. And it may increase radiation at resonant frequencies.

Electrical properties of power/ground planes in packaging structures need to be accurately characterized. The power/ground planes are distributed circuits. The physical behavior of SSN between power/ground planes is an EM problem in nature. To accurately simulate SSN; wave propagation, reflection, edge radiation, via coupling, and package resonance are all needed to be considered. [13].

2.3 Tools For Signal Integrity

A good SI tool should have 2D field solvers for extracting RLGC matrices of single/couple transmission lines and single/couple lossy transmission line simulator, 3D field solvers for wire bonds, vias, metal planes and behavior modeling of drivers and receivers. They should take physical layout files as input data and have post process simulation results in time domain (timing and waveform measurement) and frequency domain (impedance parameter and S-parameter).

CAD tools allow addressing many signal integrity issues during simulation. Appropriate simulation improve the understanding of the complex SI phenomena. If the simulation is accurate enough, some SI problems can be foreseen and solved before they occur.

There are two tools for simulating circuits:

→ Simulation Program with Integrated Circuit Emphasis (SPICE) is a standard used to simulate, like PSPICE from Orcad/Cadence, IsSpice from Intusoft, Advance Design System (ADS) from HP Eesof, MaxwellSPICE from Ansoft, Micro-CAP from Spectrum or HSPICE from Avant.

→ Input/output Buffer Interface Specification (IBIS) based simulators. IBIS is a standard used to describe the analog behavior of the Input/Output (I/O) of a digital Integrated Circuit (IC). The behavioral IBIS based models of a device provide the DC current vs. voltage (I-V) curves along with a set of rise and fall time of the driver output voltage and packaging parasitic information of the I/O buffer. IBIS modeling data itself does not provide explicit information on driver transient state transitions beyond the steady-state I-V curves. The extraction of the transient state transition of buffers is necessary for correct SI simulations.

2.4 Research Lines

Pairs of via holes, using differential signaling, have become popular choices for high-speed digital transmission on a PCB. They offer superior immunity to crosstalk and external noise and increase transmission bandwidth. However, they introduce discontinuities which are well known impedance disruptors at high speeds in a PCB.

In section 4.5 (Via Modeling) a model of via holes has been done. Via holes are a major discontinuity source that introduces parasitics that highly affect the circuits performance. Researchers are actually working on this field, studying different characterization methods for differential vias to improve their performances.

→ Laermans et al. used a characterization method to model differential via holes as a cascade of capacitances and inductances. This method used special software, FASTCAP, to calculate the values of the capacitances and inductances at each designated location on via holes, and therefore calculate impedances at those points. [12]

→ Chen et al. analyzed a large number of vias and differential signaling in multilayered structures using the equivalence principle where a vertical via structure was decomposed into an interior and an exterior problem. Full wave modeling for differential signaling was used to extract a differential SPICE via model. The drawback is that these methods are time-consuming. [12]

→ Antoni et al. used an equivalent circuit extraction technique approach for characterization of a single via hole in a PCB. [12]

→ Tao V. Nguyen, Aldo Morales and Sedig Agili extended the equivalent circuit extraction technique for differential via holes characterization on PCB in a fast and accurate manner. They partitioned a differential via hole structure in a multilayered PCB, extracted an equivalent circuit from each partition and obtained the scattering (S) parameters of each equivalent circuit. Then, a complete equivalent circuit for the entire differential via geometry is constructed by cascading all of the elementary equivalent circuit structures using Advanced Design System (ADS) software and comparing them with those obtained from High Frequency Simulation Software (HFSS) turned out to be very close. One of the advantages of the extraction technique is to obtain a circuit model that characterizes the differential via, which in turn, reduces the large amounts of simulation time on a very complex structure. [12]

Parasitics are usually removed by a process called de-embedding. There are different approaches that can be used in the process of de-embedding. In general, de-embedding techniques fall into two broad categories: modeling based approach and measurement based approach.

→ G.Antonini, A. Ciccomancini Scogna and A. Orlandi use the method of Measured S-parameter based approach. This method evaluates the performance of the discontinuities in terms of S-parameters obtained from measurements. This approach starts from the knowledge (by measurements or simulation) of the S parameters of a structure containing the discontinuity to be studied as well as other auxiliary parts such as traces or adapters. The S parameters of these parts are evaluated by means of numerical methods or by analytical formulation. Finally, the S matrix of the discontinuity is extracted from the S matrix of the complete structure by means of the information on the auxiliary parts. The advantage of this method lies in the use of simple matrix operations. [11]

→ J.Song, F. Ling, G. Flynn, W. Blood and E. Demircan use a two-impedance model for de-embedding. For this method, a Device Under Test (DUT) is connected between two adapters (left and right). Impedance models are used, with the left and right adapters considered to be an anti-symmetric combination of a series shunt impedances. Once the admittances and impedances values are obtained, the S parameters of the measured DUT with the adapters are transformed to Y parameters, and then the value of the admittance is subtracted from Y11 and Y22. The remaining Y matrix is transformed to a Z matrix. Finally, the value of the impedance is subtracted from Z11 and Z22 to get the Z matrix of the DUT. The advantage of this method is that it only needs one through measurement of the adapter. The disadvantage is that this setup is only valid for symmetrical adapters. [11]

Another method, is to use the Y parameter based approach whereby both left and right adapters are approximated as single shunt impedance. This method is typically used to characterize on-wafer circuitry by placing vias, pads, interconnects and buffers on the silicon. It requires only a single open circuit measurement. The disadvantage of using this approach is that the series impedances of the vias and metal stubs as part of the adapters are completely ignored. [11]

→ L.V. Hauwermeiren, M. Botte and D. De Zutter use the Fourier transform S parameter based de-embedding method. It works by making a comparison of an embedded DUT scenario with a standard reference setup. So first, the parameter S21 is obtained, which stands for the measurement value as a function of frequency, obtained

after applying the FFT and gating technique in the time domain. Next, the measurement on the reference setup is taken without the DUT to obtain the parameter S21 of the microstrip line. By dividing the S21 parameter of the measurement taken with the DUT and the S21 parameter of the microstrip line taken without the DUT, the S21 parameter of the DUT is obtained. This method of de-embedding is good for amplitude data but not for phase data due to calibration issues and the different propagation modes present in the fixture of interest. [11]

→ C. Schuster and W. Fichner use a Layer Peeling Technique (LPT) and Finite-Difference Time-Domain (FDTD). This technique performs de-embedding by first obtaining the time-domain reflection of the fixture using FDTD and then, the LPT is applied to de-embed the interconnect under extraction. The advantage of this method is that extraction of the DUT can be performed entirely in the time domain, avoiding Fourier transform computation. However, the LPT technique is mostly suitable for electrically medium sized and distributed structures. [11]

3. Fundamentals Of Transmission Lines

In microwave engineering, the circuits used can be divided into two big groups:

→ active microwave circuits, which can add power to the signal they receive and include components such as amplifiers, oscillators and modulators or components that can either be active or passive like antennas, multiplexers or mixers.

→ passive microwave circuits do not add power to the received signal. The components that can be on a passive microwave circuit go from discrete elements such as resistances, inductors or capacitances to more complicated circuits including filters, dividers, couplers and transmission lines.

This project is based on a complete passive structure and for this reason we will focus on the passive elements.

On the other hand, S parameters are used because they are relatively easy to obtain at high frequencies; S parameters of multiple devices can cascade to predict the system's performance; they relate to familiar measurements such as gain, loss or reflection coefficient; H, Y or Z parameters can be obtained easily from S parameters and S parameter files are easy to import and use in our simulation tools.

3.1 Transmission Lines

A transmission line is defined as a metallic conductor system which is used to transfer energy in electromagnetic wave form from point to point. In order to be more specific, we can say that a transmission line consists of two or more conductors separated by a dielectric (with the exception of the waveguide, which is not formed by two conductors but it behaves like a transmission line).

The energy propagation through a transmission line happens to be in a transversal electromagnetic waves (TEM) form, which means that the direction of propagation is perpendicular to the displacement's direction. These waves are mainly transmitted in the dielectric that separates both conductors.

There are many types of transmission lines, but in fact, when transmission lines are used at high frequencies, effects such as dispersion or dissipation make some transmission lines like coaxial cable, pairs cable or twisted cable useless. Therefore, alternatives have been built for high frequencies: the so called flat transmission lines.

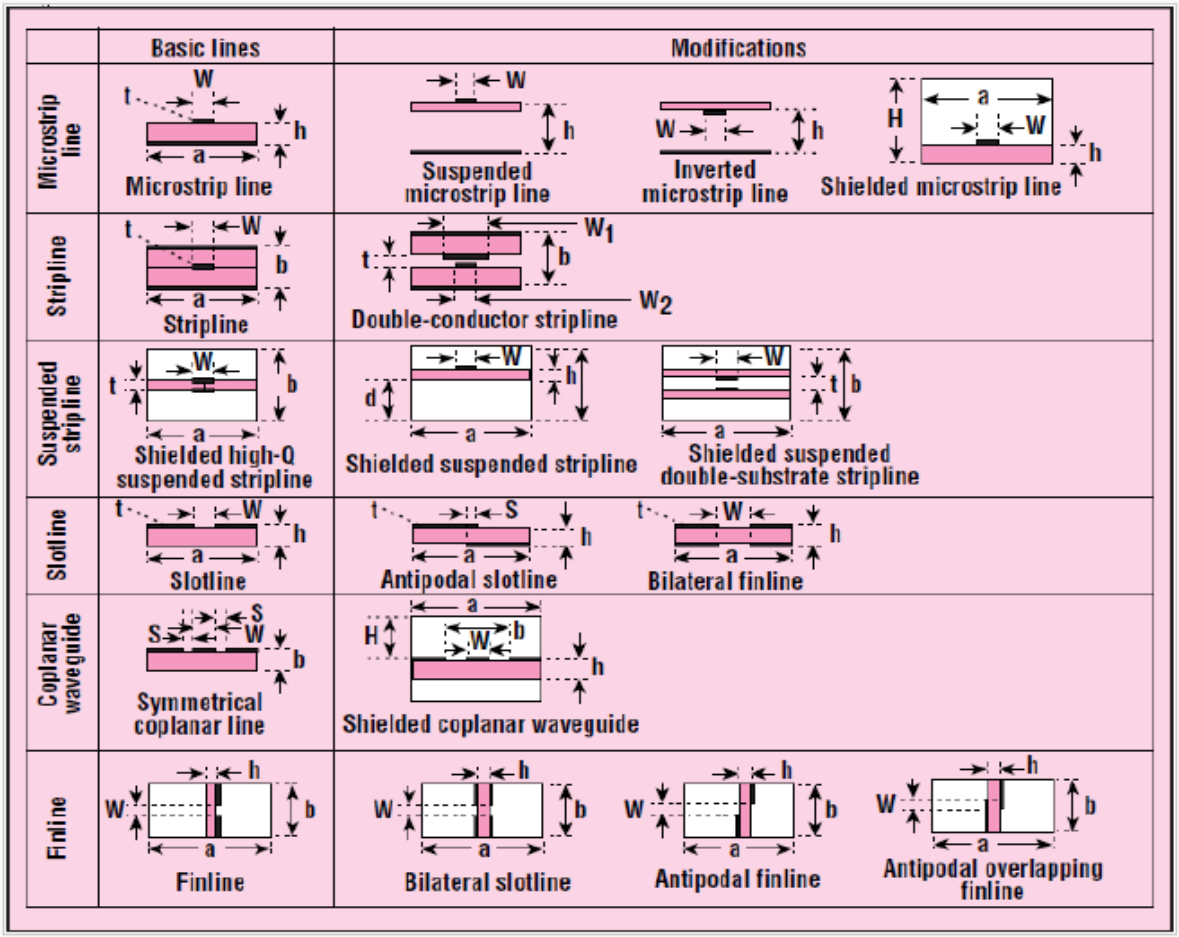


Figure 3.1. Flat transmission lines.

Transmission lines on printed circuits are cheap, easy to fabricate, they make circuits be light and smaller in size and they also offer a big bandwidth. For these reasons they are often used for high frequency circuits.

Flat transmission lines have a dielectric with metal in one or both sides. It is the metallization what changes when it comes to building passive circuits, transmission lines and coupling circuits, likewise it is possible to insert active devices and that is why these complex circuits are cheap and small.

In order to design a flat transmission line, it is very important to determine the characteristic impedance of the line as well as the effective permittivity of the chosen dielectric, both frequency dependent parameters.

Among this family of transmission lines, microstrip is the most common, but there are also striplines, suspended striplines, slotlines, finlines and coplanar waveguides and its modifications as they are showed in Figure 3.1.

In this project, the transmission lines are differential microstrip lines (see Figure 3.2). Differential microstrip lines are commonly used in high-speed digital PCB designs, where signals need to be routed with minimal distortion, avoiding crosstalk and radiation.

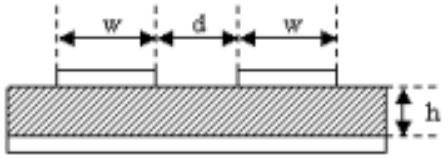


Figure 3.2. Differential microstrip line. W: width, d: spacing, h: high.

It consists of a pair of conducting strips separated a distance d between them and separated from a ground plane by a dielectric layer called substrate.

3.2 S-Parameters

Every device, circuit or system can be defined as a n-port network. A port is a pair of terminals where the signal goes in or out. Figure 3.3 shows a two port network.

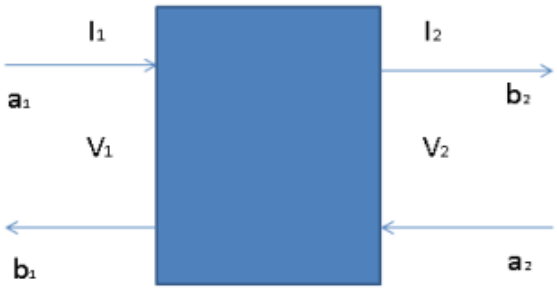


Figure 3.3. Two port network, where I_1 is the input current, I_2 is the output current, V_1 is the input voltage, V_2 is the output voltage, a_1 and b_1 are the terminals in input port and a_2 and b_2 are the terminals of the output port.

By knowing one type of parameters, such as currents or voltages for example, it is possible to immediately calculate the other parameters. There are many type of parameters that can be calculated: impedance or Z, admittance or Y, hybrids or H, transmission or T, inverse transmission or ABCD or dispersion or S.

The difference between the Z, Y, H, T, ABCD parameters and the S parameters is that the first ones need a short or an open circuit to be calculated. However, at high frequencies this is very hard to do, or even impossible. It is also very difficult to measure currents or voltages at high frequencies, plus active devices may be unstable at these frequencies. It is because of these inconveniences that we use the S parameters at high frequencies.

How to calculate the S parameters?

Variables are needed to define the scattering matrix. They are called a and b, where a_i are independent variables that represent the waves going into the device and b_i are dependent variables that represent the waves going out of it (i,j=1,2,3,...,n for an n port network) . Therefore,

$a_i(x) = V_1^+(x)/\text{sqrt } Z_o$ and $b_i(x) = V_1^-(x)/\text{sqrt } Z_o$

$$b_1 = S_{11}a_1 + S_{12}a_2 + S_{13}a_3 + \ldots + S_{1n}a_n$$
$$b_2 = S_{21}a_1 + S_{22}a_2 + S_{23}a_3 + \ldots + S_{2n}a_n$$
$$b_3 = S_{31}a_1 + S_{32}a_2 + S_{33}a_3 + \ldots + S_{3n}a_n$$
$$\vdots$$
$$b_n = S_{n1}a_1 + S_{n2}a_2 + S_{n3}a_3 + \ldots + S_{nn}a_n$$

In our Figure x, i,j=1,2 since it is a two port network and from now on, the explanation will be given for a two port network. Thus,

$$b_1 = S_{11}a_1 + S_{12}a_2$$
$$b_2 = S_{21}a_1 + S_{22}a_2$$

S parameters measure transmission and reflection in the terminals. The reflection measurement can give information about the reflection coefficient, the return losses or the Standing Wave Ratio (SWR) while the transmission measurement can give information about gain, attenuation or insertion loss.

In order to determine S_{11} and S_{21}, a_2 has to be zero. We do this by loading port 2 with a Z_L that has to be matched. We proceed alike to determine S_{12} and S_{22}, where a_1 has to be zero, so we put a load Z_L on port 1. So,

$S_{11} = b_1/a_1|_{a2=0}$ is the reflection coefficient in port 1 when $Z_2 = Z_L$

$S_{22} = b_2/a_2|_{a1=0}$ is the reflection coefficient in port 2 when $Z_1 = Z_L$

$S_{12} = b_1/a_2|_{a1=0}$ is the complex gain from port 2 to port 1 when $Z_1 = Z_L$

$S_{21} = b_2/a_1|_{a2=0}$ is the complex gain from port 1 to port 2 when $Z_2 = Z_L$

The scattering matrix has the following properties:

→ If the network is passive: $|S_{ii}|, |S_{ij}| \leq 1$

→ If the network is lossless: $S^TS = I$

→ If it is a lossy network: $I - S^TS \geq 1$

→ If the network is reciprocal or simetric: $S = S^T$

In order to calculate the reflection coefficient at the input (ρ_{in}), we can use Figure 3.4 and proceed as follows:

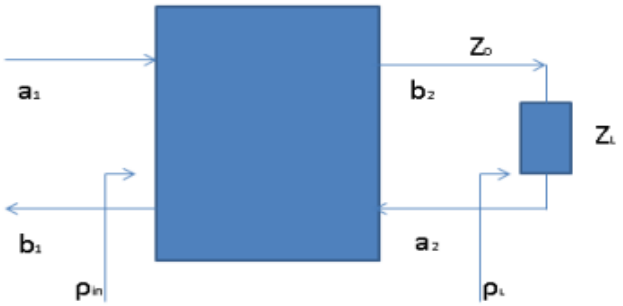


Figure 3.4. Example figure to calculate the reflection coefficient at the input (ρ_{in})

$$\rho_L = \frac{a_2}{b_2} = \frac{Z_0 - Z_L}{Z_0 + Z_L}$$

$$a_2 = \rho_L b_2$$

$$b_2 = S_{21}a_1 + S_{22}a_2$$

$$b_2 = S_{21}a_1 + S_{22}\rho_L b_2$$

$$b_2 = \frac{S_{21}a_1}{1 - \rho_L S_{22}}$$

$$b_1 = S_{11}a_1 + S_{12}a_2$$

$$b_1 = S_{11}a_1 + \frac{S_{12}S_{21}\rho_L a_1}{1-\rho_L S_{22}}$$

$$\rho in = \frac{b_1}{a_1} = S_{11} + \frac{S_{12}S_{21}\rho_L}{1 - \rho_L S_{22}}$$

Both, the transmission and reflection coefficients depend on the characteristic impedance of the line and the ports impedance (or load impedance). When the loads are matched, both impedances have the same value and the reflection coefficient is zero. In this ideal case, there is a perfect transmission where the 100% of the energy is transmitted with no losses. [4].

3.3 Transmission Lines' Behavior At High Frequencies

At high frequencies, where the wavelength is very small, transmission lines behave like a resonant circuit as shown in Figure 3.5. The transmission line characteristics come determined by its electrical and physical properties. These electrical and physical properties determine the primary electric constants (or distributed parameters) and them together make an artificial electrical model of the line. The distributed parameters are:

→ R: Per unit length resistance (Ω/m)

→ L: Per unit length inductance $(\mathrm{H/m})$

→ C: Per unit length capacitance $(\mathrm{F/m})$

→ G: Per unit length conductance $(\mathrm{S/m})$

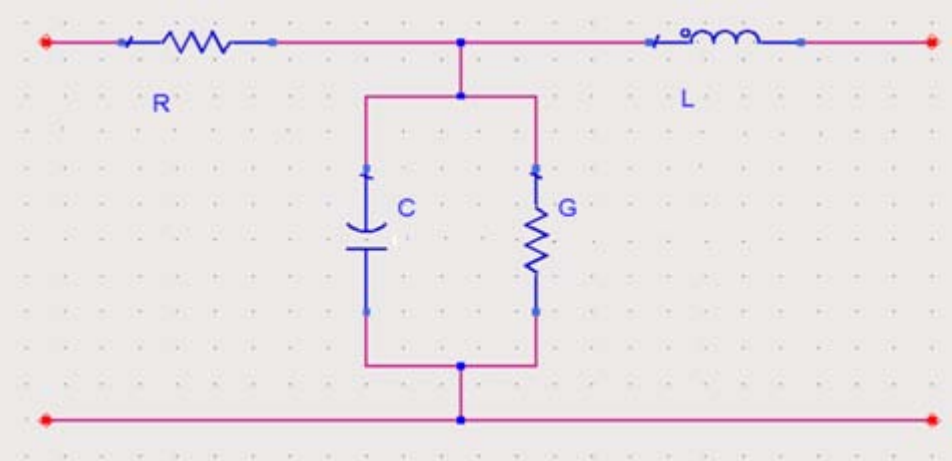


Figure 3.5. Equivalent circuit of a transmission line.

R and L occur along the line, while C and G occur between the conductors. R measures the power loss along the line. L measures the stored energy in the magnetic field along the line. C measures the stored energy in the electric field along the line and G measures the power loss between the two conductors along the line.

The secondary parameters of a transmission line are the characteristic impedance of the line (Z_o) and the propagation constant (γ). These secondary parameters also characterize the transmission line and can be easily deduced from the primary constants with the following equations:

$$Zo = \sqrt{\frac{R+j\omega L}{G+j\omega C}} \qquad \gamma = \alpha + j\beta = \sqrt{(R+j\omega L)(G+j\omega C)}$$

where α is the attenuation constant and β is the phase constant.

For a lossless transmission line and because at high frequencies R is much smaller than jωL and G is also a lot smaller than jωC:

$$Zo = \sqrt{\frac{R+j\omega L}{G+j\omega C}} = \sqrt{\frac{j\omega L}{j\omega C}} = \sqrt{\frac{L}{C}} \qquad \gamma = \alpha + j\beta = \sqrt{(R+j\omega L)(G+j\omega C)} = j\omega\sqrt{LC}$$

At high frequencies in a lossless transmission line, the characteristic impedance of the line is not a frequency dependent parameter anymore, and it is only L and C dependent. Concerning to the propagation constant, it depends on the frequency and the values of L and C. So, for a lossless transmission line, a voltage wave travels in the line with no alteration at the speed $v_p = \frac{1}{\sqrt{LC}}$, dependent on the properties of the transmission line.

If the characteristic impedance of the transmission line presents discontinuities, then reflections along the line will happen. These discontinuities can be capacitive or inductive and the presence of a discontinuity adds delay, and the delay they introduce depends on the values of C or L and Z_o.

When it comes to lossy transmission lines, both L and R have frequency dependence due to the skin effect.

The current that goes through a conductor is distributed in its surface according to frequency (see Figure 3.6). At very low frequencies, the whole conductor's cross section carries uniformly distributed current if it is DC current or non uniformly distributed AC current if the conductor carries DC current, but as the frequency increases, the current distribution is higher at the conductor's surface than at its center. At very high frequencies, all the current flows around the conductor's surface. This is known as skin effect. As frequency increases so does skin effect and due to the skin effect increase, the cross sectional area where the current flows decreases, which increases the resistance and the power loss. [3].

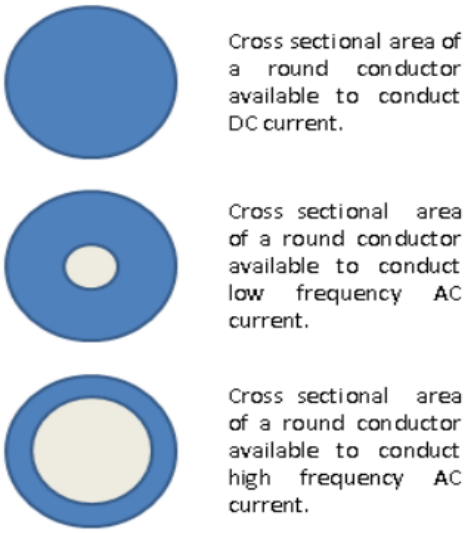


Figure 3.6. Cross sectional area of a round conductor due to skin effect.

So, the conductors of every transmission line have a DC resistance and a frequency variable resistance due to the skin effect for which the current flows through the conductor's surface and not trough its center. Both resistances together define the distributed resistance (R) measured in Ω / m. Furthermore, at high frequencies, the conductors of a line are linked by a variable magnetic field, leading to a distributed inductance (L), measured in (H/m). On the other hand, between the two conductors that form the line there is a difference of potential that results in an electric field, which is why a distributed capacity (C) appears along the line and it is measured in F/m. As well as these and because the dielectric is not perfect, there are losses in parallel with the line characterized by a distributed conductance (G) measured in S/m.

Therefore, the characteristic impedance and the propagation constant of a lossy transmission line are frequency dependent and complex numbers:

$$Zo(\omega) = \sqrt{\frac{R(\omega)+j\omega L(\omega)}{G(\omega)+j\omega C(\omega)}} \qquad \gamma(\omega) = \alpha(\omega) + j\beta(\omega) = \sqrt{(R(\omega) + j\omega L(\omega))(G(\omega) + j\omega C(\omega))}$$

where α(ω) is the attenuation constant and β(ω) is the phase constant.

The velocity $v_p(\omega) = \frac{\omega}{\beta(\omega)}$is also frequency dependent. Because now different frequencies in the spectrum of a pulse travel at different speeds suffering different attenuation, what leads to dispersion. Dispersion is the separation of the waves with different frequencies when they travel through a material. All the materials are more or less dispersive and it affects to all the waves. This is a problem when it comes to high frequencies because with increasing frequency, the effective dielectric constant gradually goes towards the substrate, so the phase velocity decreases and it degrades the signal and it makes the eye diagram close.

The equations for the characteristic impedances of the line and the propagation constants come from the telegraphist's equations that have not been explained here in order to synthesize. [4], [14].

3.4 Via Holes

Via holes are used to connect components located on different layers of a multilayer Printed Circuit Board (PCB). A via is a metal perforation (plated via) that allows uninterrupted electrical conduction from one layer to another.

Via holes can be classified as single or differential depending upon the geometric structure, but they can also be classified as through-hole or full stack, blind or buried depending upon its placement inside the board.

A single via hole is a vertical connection that can go from the top to the bottom layer of a PCB. It is made of a central cylinder and some thin, cylindrical copper pads. Single vias pass through copper ground planes through separation holes called anti-pads. The whole structure is then embedded into a dielectric material.

Differential via holes are pairs of single via holes that interconnect different layers on a PCB but the signal is launched through a pair of transmission lines using differential signaling. Differential via holes offer higher immunity to external noise and crosstalk, a higher transmission bandwidth and can also be designed (based on the PCB's geometrical properties such as thickness, width and spacing and trace lengths) to minimize the reflection and attenuation of the signal. These reasons make differential via holes a good choice for high speed transmission on a PCB, but on the other hand, at high frequencies they introduce discontinuities that highly affect the signal integrity and therefore need to be taken into consideration.

Through-hole (or full stack) via holes go over the entire PCB connecting the top layer with the bottom layer. This type of via is easier and cheaper to make.

Blind vias are usually used in complex designs where more than two layers are needed. Usually, for multilayer design systems, where there are many integrated circuits, energy planes are used (Vcc or Gnd) to avoid routing too many feeding tracks. It is much easier and reliable if the feeding connection is done directly under the chip on followed layers than connecting with long tracks to the power delivery system. Sometimes it is also needed to route a signal track from an external layer to an internal one with the shortest possible length due to the problems that come from working at high frequencies that affect to the signals' integrity. For these types of connections, blinded vias are required; they allow the connection between from an external layer to an internal layer.

Buried vias are similar to blind vias with the difference that buried vias don't start or end at any external layer, they just go through internal layers and they are built between consecutive layers.

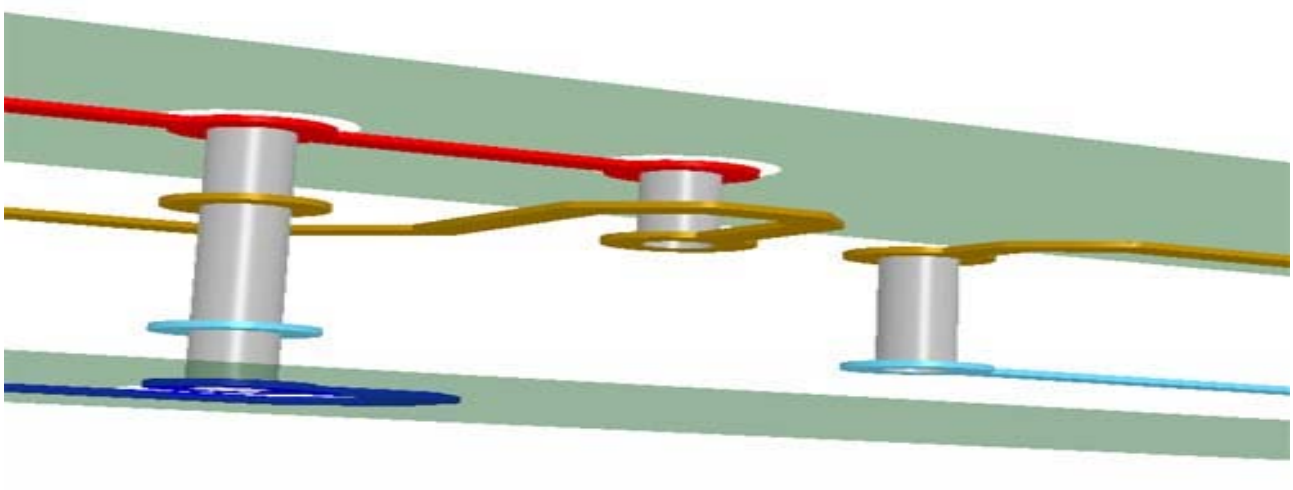


Figure 3.7. Comparison between thru-hole, blind and buried vias.

Figure 3.7 shows a four layer structure where the top and bottom layer are green colored. In this figure three types of vias are shown. Starting from the left, the first one is a through-hole via that goes through the whole structure connecting the top layer with the bottom layer. The via shown in the middle is a blind via that connects the top layer with layer number two (an internal layer). The first via starting from the right is a buried via that connects the internal layers two and three. [5], [8].

4. Results

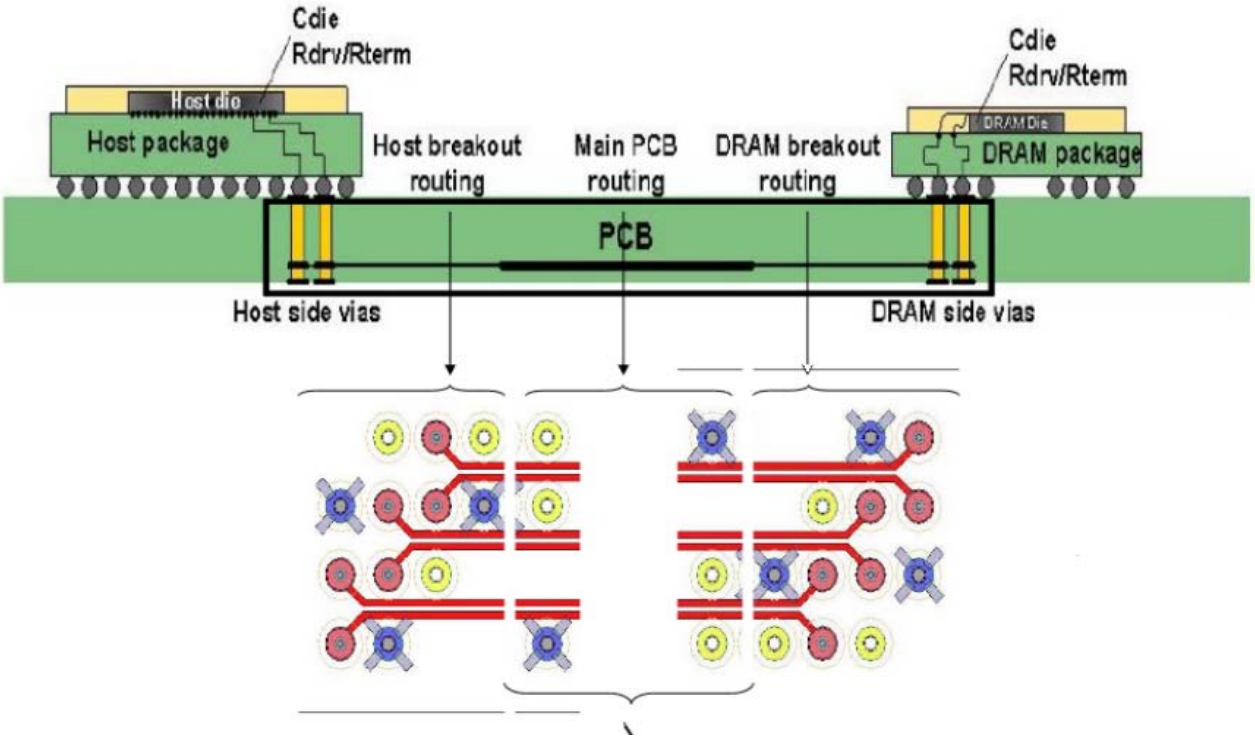


Figure 4.1. Complete structure.

Figure 4.1 is a picture of the complete structure.

Host die is an Integrated Circuit (IC) with a number of pads connected through lines to the pins of the Host package. The pins of this package are connected to the PCB through differential vias.

The Printed Circuit Board (PCB) has 12 layers. There are differential via holes on the host side and on the DRAM side. The vias make a connection between the pins of the host package (or the DRAM package on the other side) with all the layers of the PCB through the interconnects and have an open circuit at the end. Transmission lines go on different layers from the vias of the host side to the DRAM's side vias and vice versa depending if it is reading or writing.

The DRAM package is just physically like the Host package. It has pins that are connected to the pads of the IC called DRAM die. [1].

4.1 Sources Of Problem

There was a need to focus on finding the problems that made the reason why the eye would not open more. After taking a look at the behavior of the structure, including vias, transmission lines and packaging through EM simulations and models, it was found out that the main problems to be faced were the transmission line losses, which increase as the frequency does too, the noise, the transmission line dispersion at frequencies at above 60GHz, the behavior of via-transmission line junction that presents a resonance frequency which deteriorates more the eye diagram as it goes down and the GPU and DRAM packages.

The two first big problems worsening the eye diagram (losses in transmission lines increasing with frequency and noise) where already known and have been explained in chapters 2 (Introduction to signal integrity) and 3 (Fundamentals of transmission lines).

Dispersion is another problem, occurring in the transmission lines at frequencies above 60 GHz. It happens because the signals crash with a rough surface which makes the signal reflect in different directions and this can turn into a change in frequency or in the polarization of the electromagnetic wave. At the same time, and for digital communications, there is a phenomenon, called InterSymol Interference (ISI) that occurs when a previous symbol to the one that is being received at the moment interferes with this one due to one or more reflections. This delay is because the distance covered by the reflected wave is bigger than the distance covered by the transmitted wave. So it was found that dispersion was related to the ISI and this is a reason for why the eye diagram was also closing.

While taking a look at the behavior of the via-transmission line junction it was also found that the vias connecting all the layers in the PCB were another reason for the eye diagram to close. Vias introduce a resonance frequency and as this resonance frequency goes down the eye deteriorates. This led to take into deeper study the vias effect and a model for the vias has been done and it is explained in chapter 4.5 (Modeling).

An EM simulation of the whole structure including GPU and DRAM packages was performed. The results showed a huge change from when they were not being taking into account. The packages are a major source of problem for the signal integrity.

These problems result in lower bit rate.

4.2 EM Simulations

The entire PCB (Vias and transmission lines) has been simulated with HFSS (High Frequency Structural Simulator) up to a frequency of 100 GHz.

In order to simplify and have faster simulation results, only one differential via path instead of three has been considered and the difference on the S21 parameter between considering only one differential via (red) and three differential vias (blue) is shown below (Figure 4.2).

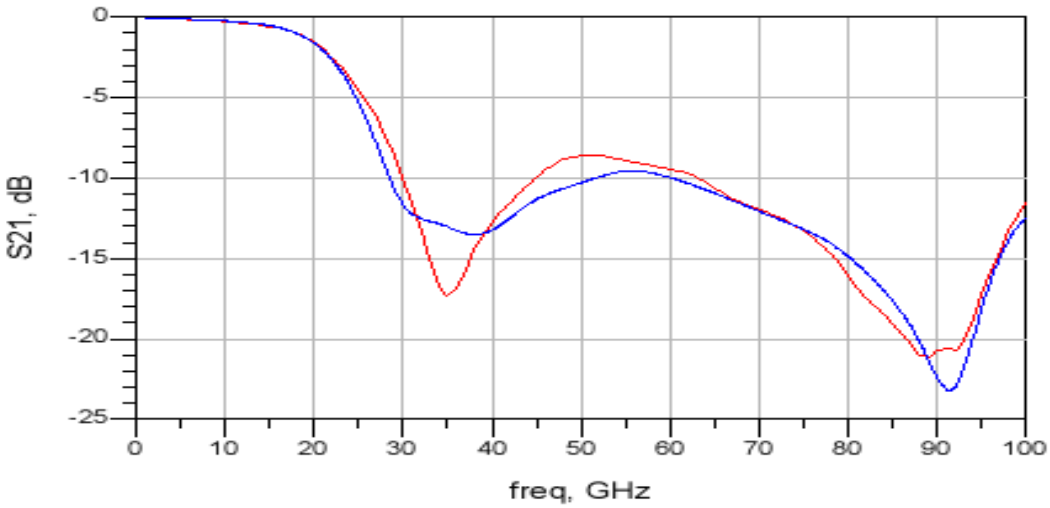
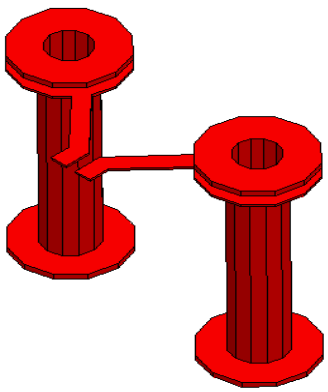


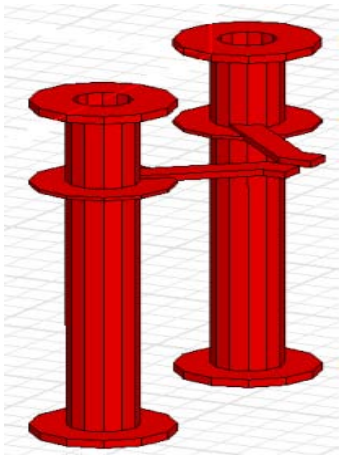
Figure 4.2. S21 of the one versus three differential vias.

Regarding transmission lines, they have been simulated considering a length of 50 mil (vias length is 1200 mil as default) because its effect is negligible and it allows faster simulation.

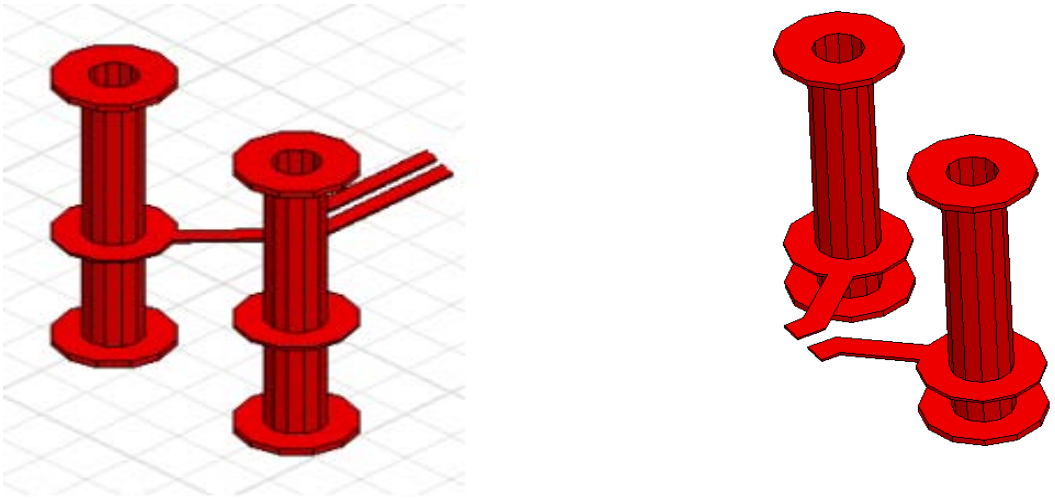
The EM simulation has been performed at four different signal levels, namely, for the transmission lines placed in layers 2, 5, 8 and 10 as it is shown below in Figure 4.3.



a)



b)



c) d)

Figure 4.3. a) transmission lines in layer 2. b) transmission lines in layer 5.
c) transmission lines in layer 8. d) transmission lines in layer 10.

The vias might be a major discontinuity source that may cause disruption in signal integrity so the aim of this is to identify the discontinuity and its characteristics and contribution to the entire PCB behavior based on simulation. De-embedding (Figure 4.4) has been used in order to suppress all the unwanted electromagnetic fields and have accurate data. It is a mathematical process that removes the effects of unwanted artifacts of the structure that are embedded in the measured data by subtracting their contribution. [11].

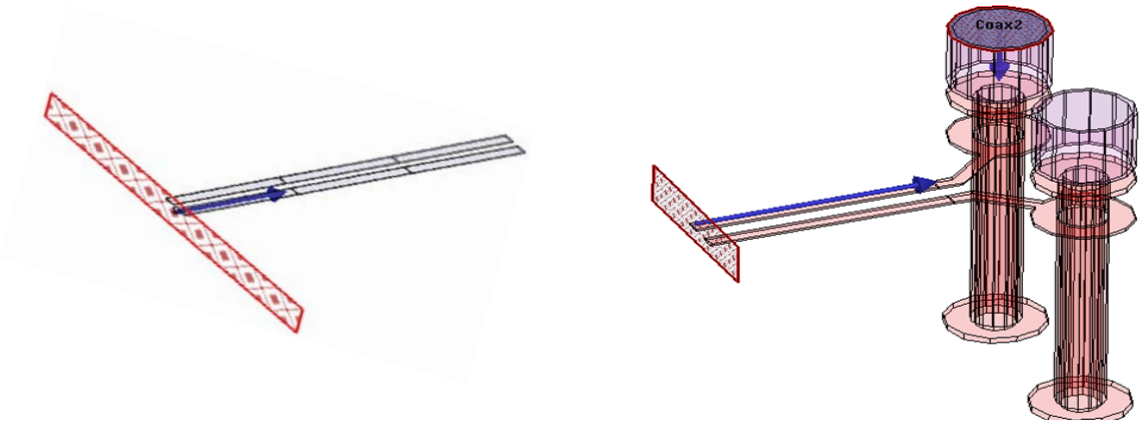


Figure 4.4. De-embedding in HFSS

4.3 Interconnection Characteristics

As another step, transmission lines and via structures have been simulated separately with HFSS to characterize their own behavior and contribution.

When simulating the transmission line with a length of 1200 mil, a spacing 2 mil of and a width 3.1 mil, the characteristic impedance of the line shows a resonance frequency at around 60 GHz (see Figure 4.5), so the transmission line dispersion is at 60 GHz. Transmission lines have an acceptable loss.

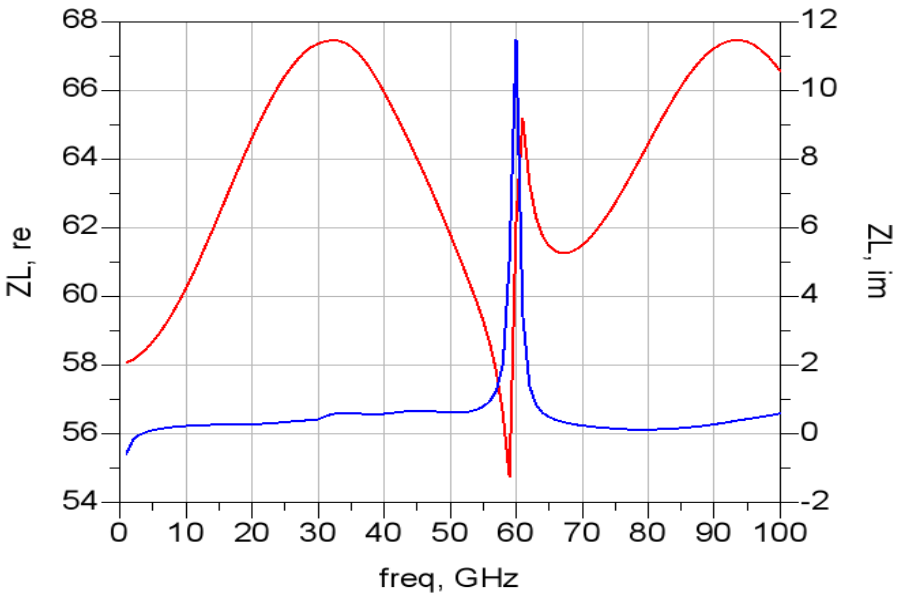


Figure 4.5. Characteristic impedance of a transmission line 1200 mil long with a width of 3.1 mil and a spacing of 2 mil.

The via structures have been characterized with the same technique and they have been simulated for layers 2, 5, 8 and 10. The output transmission line from the via in each layer has also been swept for different width (from 3.1 mil to 5.1 mil with a step of 0.5 mil) and spacing (from 2 mil to 4 mil with a step of 0.5 mil) and simulated together with the via. The way this via structure behaves for the different layers can be seen in the figures below 4.6 through 4.8.

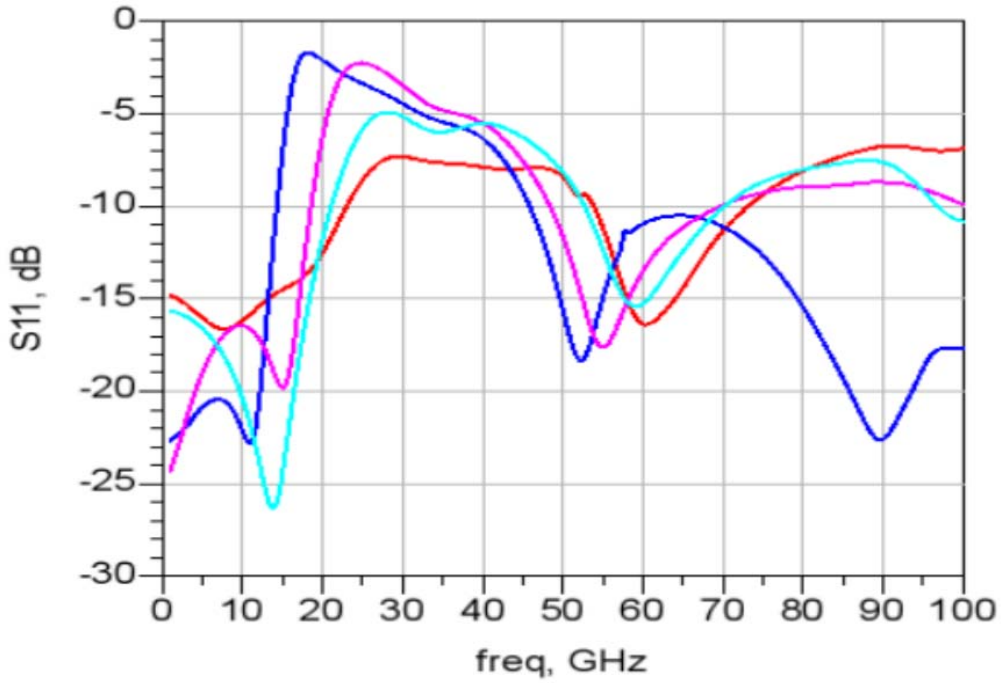


Figure 4.6. S11 of the via structure with an output transmission line (width=3.1mil, spacing=2mil) on layers 2 (blue), 5 (pink), 8 (light blue) and 10 (red).

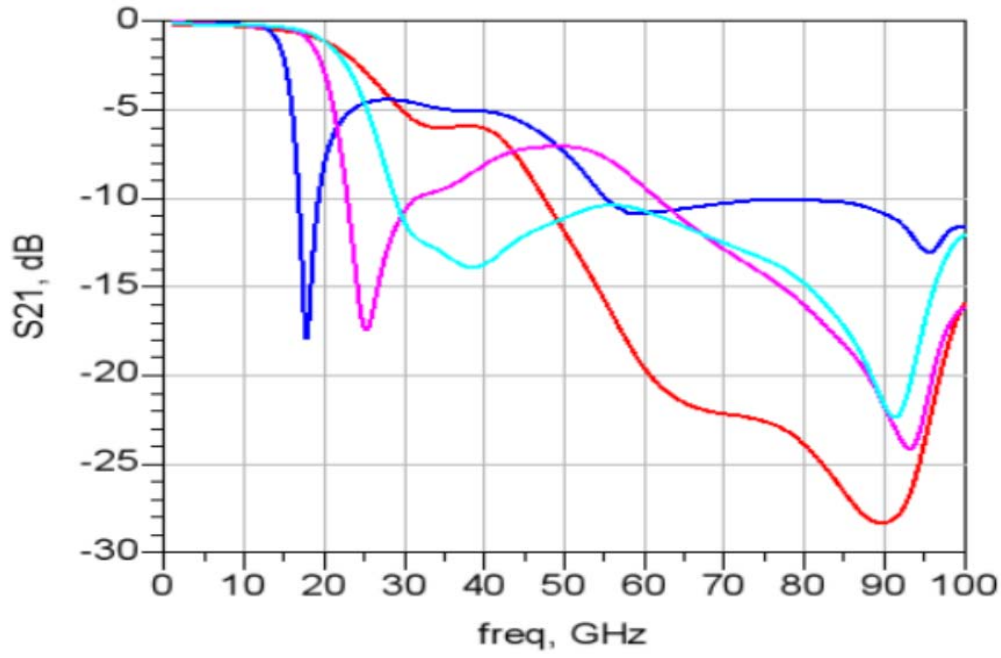


Figure 4.7. S21 of the via structure with an output transmission line (width=3.1mil, spacing=2mil) on layers 2 (blue), 5 (pink), 8 (light blue) and 10 (red).

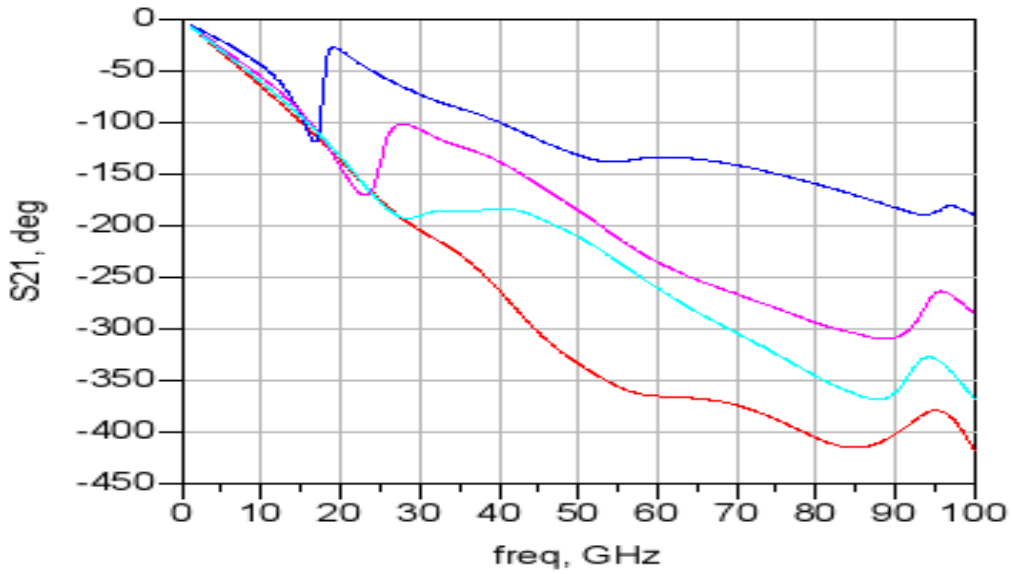


Figure 4.8. Phase of the via structure with an output transmission line (width=3.1mil, spacing=2mil) on layers 2 (blue), 5 (pink), 8 (light blue) and 10 (red).

Figure 4.7 shows that the vias losses are very low at frequencies below 10 GHz, however, after 15 GHz, via losses increase on a significant way and they are higher than the transmission line losses.

As it can be seen on Figure 4.7, the structure presents a resonance frequency at around 17 GHz when the output transmission line is in layer 2, at around 25 GHz when it is in layer 5, at around 35 GHz when it is in layer 8 and past 50 GHz when it is in layer 10.

So what has been found here is that via structures present a resonance frequency at a very low frequency. This is because the resonance frequency occurs when the reflected signal is 180 degrees (a quarter wavelength) delayed and cancels out the signal through the via. The via is an open circuit at the end, so for layer 2, at around 15 GHz there is a quarter wavelength and it becomes a short. Equally for the rest of the layers.

In order to see how this affects to the eye opening, the eye diagrams have been plotted at different bit rates (figures 4.9 through 4.20) using ADS. The results show that the maximum eye occurs at a bit rate of 6.5 GHz and it deteriorates as the bit rates increases. On the other hand, the best eye diagram occurs when the output transmission line is in layer 10, which means that the eye diagrams show the same tendency as the S parameters (see Figure 4.7) and as the S parameters deteriorates the eye width becomes smaller or which is the same, as the resonance frequency goes down the eye closes. The via has more effect on the eye than the transmission lines, specially at higher bit rates.

Note that at a bit rate equal to 30 GHz, the eye for layer 2 completely closes, while it has it's best performance for layer 10.

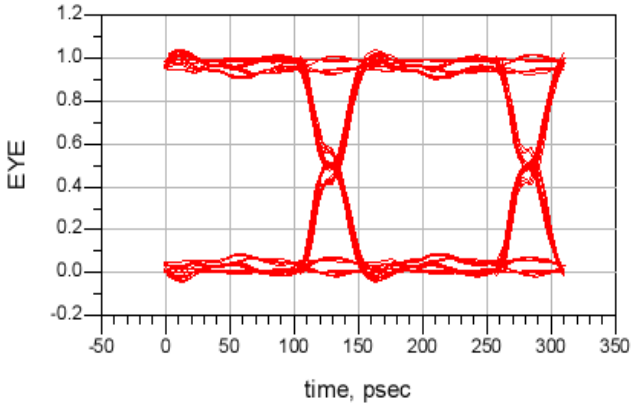


Figure 4.9. Eye diagram of the via structure with transmission line (width=3.1mil, spacing=2mil) output on layer 2 and bit rate = 6.5 GHz

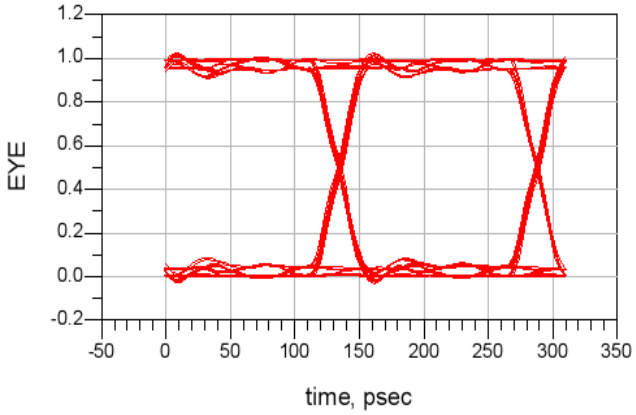


Figure 4.10. Eye diagram of the via structure with transmission line (width=3.1mil, spacing=2mil) output on layer 5 and bit rate = 6.5 GHz

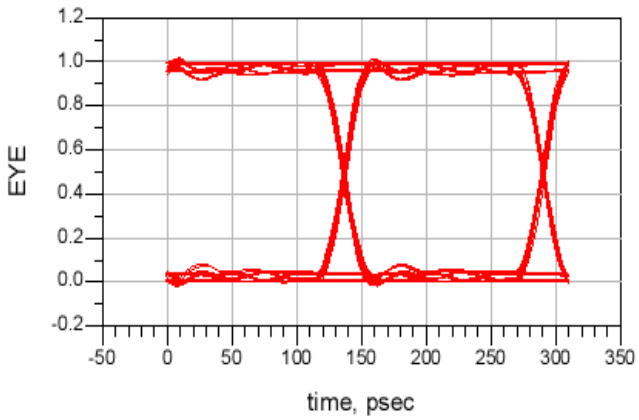


Figure 4.11. Eye diagram of the via structure with transmission line (width=3.1mil, spacing=2mil) output on layer 8 and bit rate = 6.5 GHz

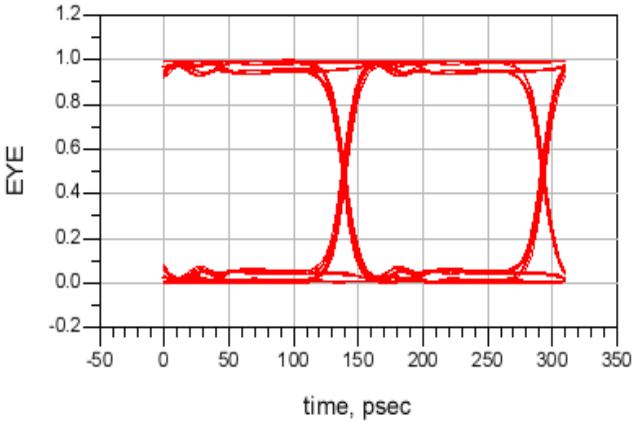


Figure 4.12. Eye diagram of the via structure with transmission line (width=3.1mil, spacing=2mil) output on layer 10 and bit rate = 6.5 GHz

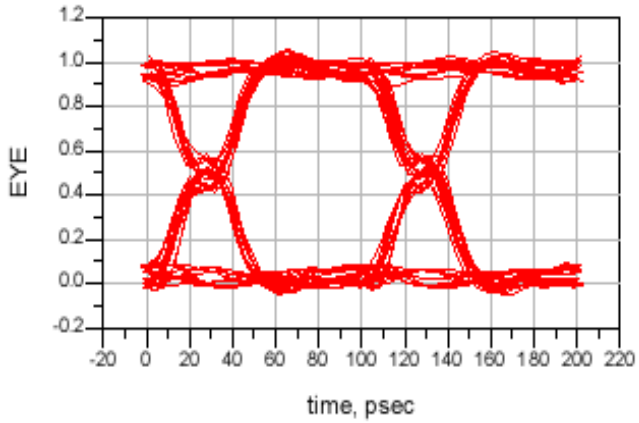


Figure 4.13. Eye diagram of the via structure with transmission line (width=3.1mil, spacing=2mil) output on layer 2 and bit rate = 10 GHz

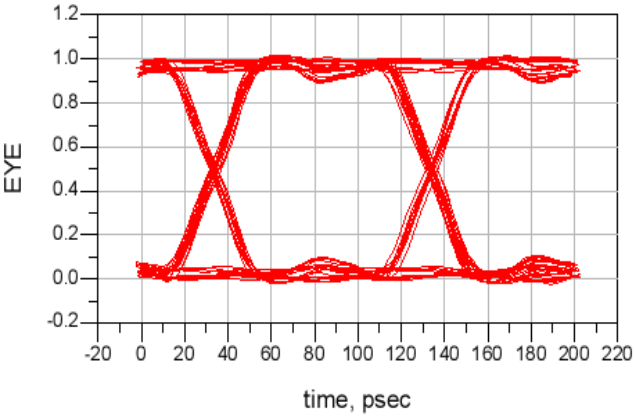


Figure 4.14. Eye diagram of the via structure with transmission line (width=3.1mil, spacing=2mil) output on layer 5 and bit rate = 10 GHz

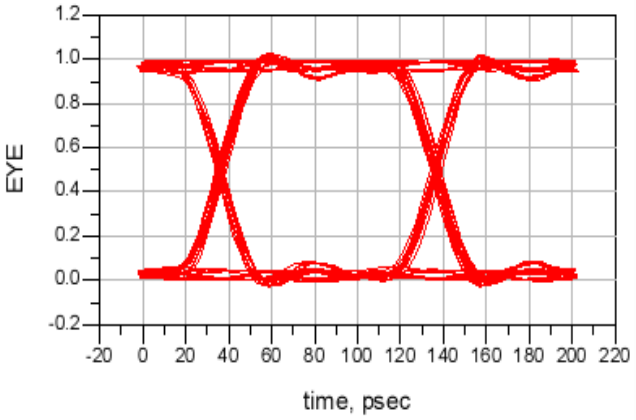


Figure 4.15. Eye diagram of the via structure with transmission line (width=3.1mil, spacing=2mil) output on layer 8 and bit rate = 10 GHz

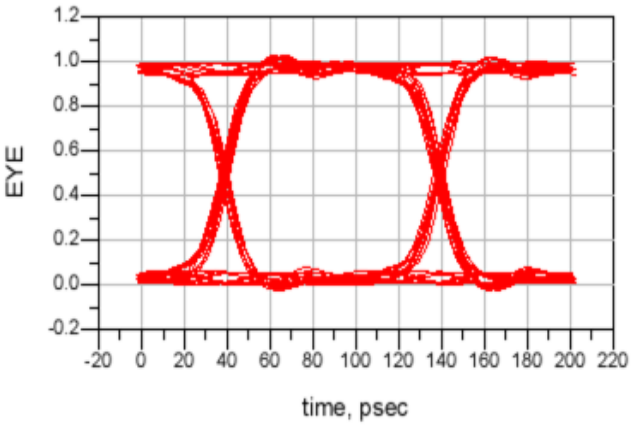


Figure 4.16. Eye diagram of the via structure with transmission line (width=3.1mil, spacing=2mil) output on layer 10 and bit rate = 10 GHz

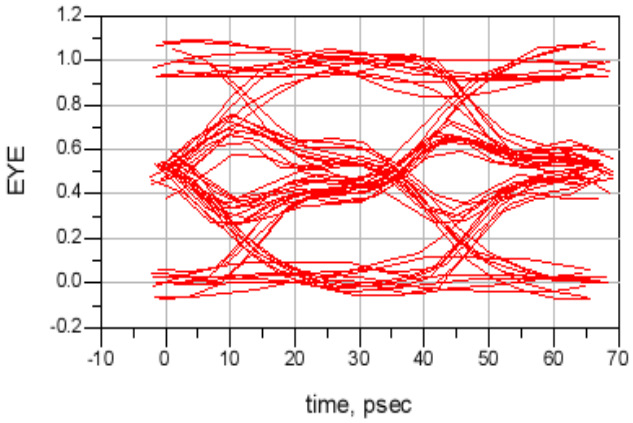


Figure 4.17. Eye diagram of the via structure with transmission line (width=3.1mil, spacing=2mil) output on layer 2 and bit rate = 30 GHz

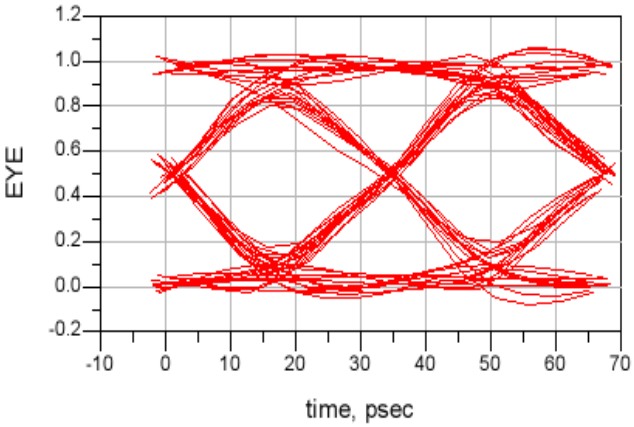


Figure 4.18. Eye diagram of the via structure with transmission line (width=3.1mil, spacing=2mil) output on layer 5 and bit rate = 30 GHz

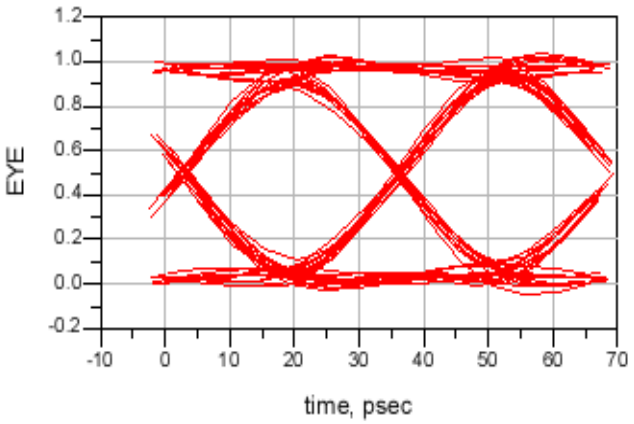


Figure 4.19. Eye diagram of the via structure with transmission line (width=3.1mil, spacing=2mil) output on layer 8 and bit rate = 30 GHz

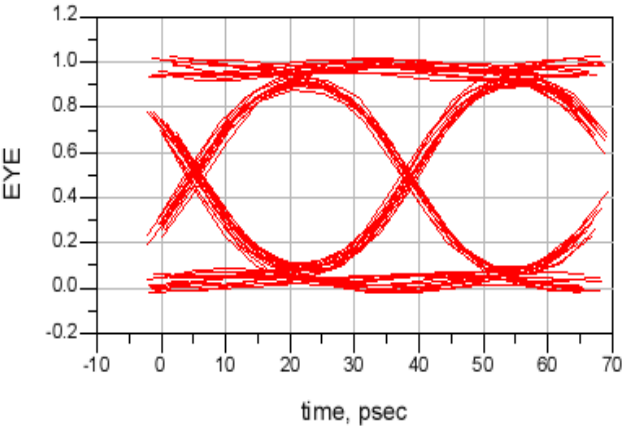


Figure 4.20. Eye diagram of the via structure with transmission line (width=3.1mil, spacing=2mil) output on layer 10 and bit rate = 30 GHz

4.4 Effect Of The Package

In order to see how the package parasitics affect the overall performance of the circuit, both together (package and PCB) have been simulated using HSPICE (Simulation Program with Integrated Circuit Emphasis), and the eye diagram has been plotted with MATLAB.

The simulation has been done for a bit rate of 6.5 GHz as well as 10 GHz. The results, shown in the following figures 4.21 through 4.28, reveal the strong effect that the package parasitics have in the signal since the eye is now a lot more closed than it was without taking the packaging into consideration. It is obvious then, that the package has a lot more effect in the signal degradation than the vias or the transmission lines.

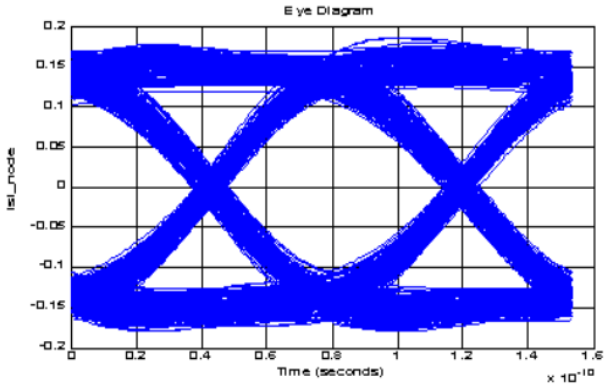


Figure 4.21. Eye diagram of the via structure including the packaging, with transmission line (width=3.1mil, spacing=2mil) output on layer 2 and bit rate=6.5 GHz

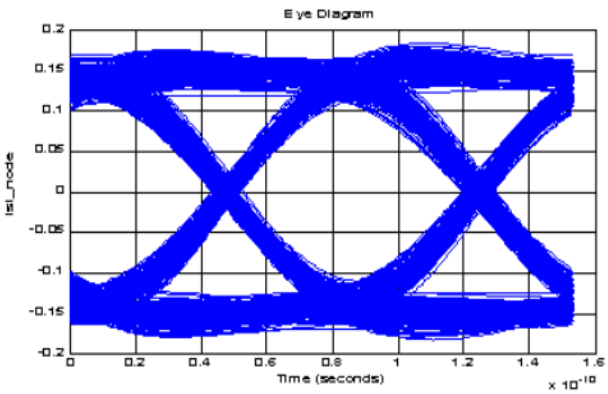


Figure 4.22. Eye diagram of the via structure including the packaging, with transmission line (width=3.1 mil, spacing=2 mil) output on layer 5 and bit rate=6.5 GHz

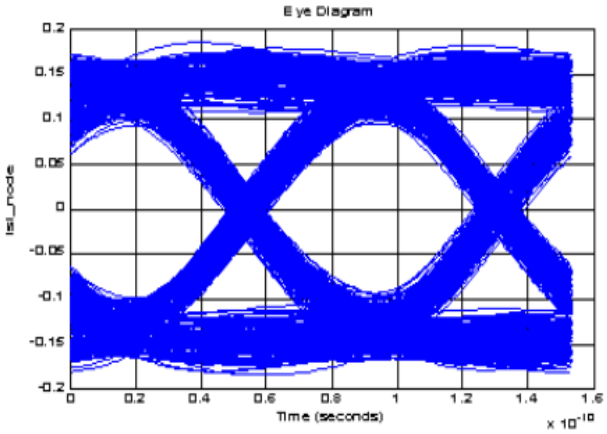


Figure 4.23. Eye diagram of the via structure including the packaging, with transmission line (width=3.1mil, spacing=2mil) output on layer 8 and bit rate=6.5 GHz

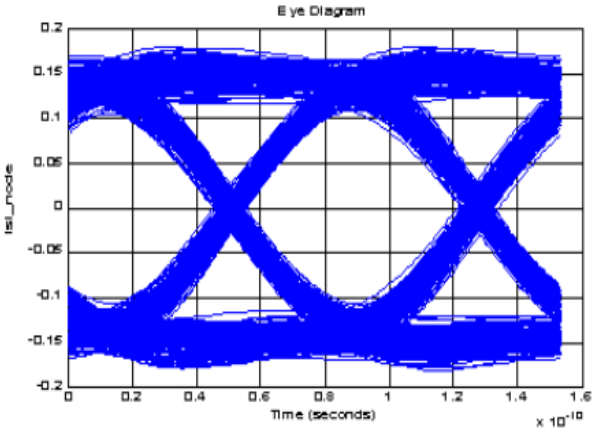


Figure 4.24. Eye diagram of the via structure including the packaging, with transmission line (width=3.1mil, spacing=2mil) output on layer 10 and bit rate=6.5GHz

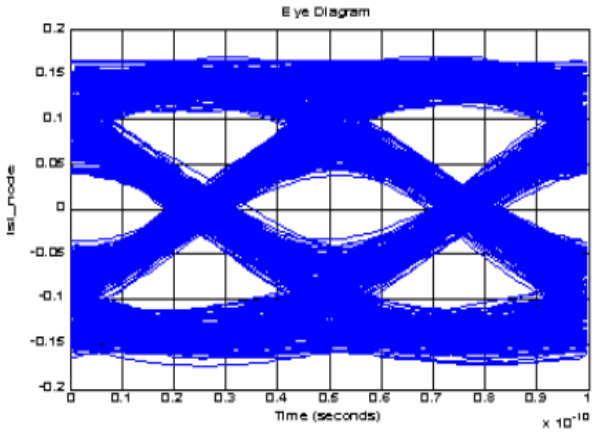


Figure 4.25. Eye diagram of the via structure including the packaging, with transmission line (width=3.1mil, spacing=2mil) output on layer 2 and bit rate=10 GHz

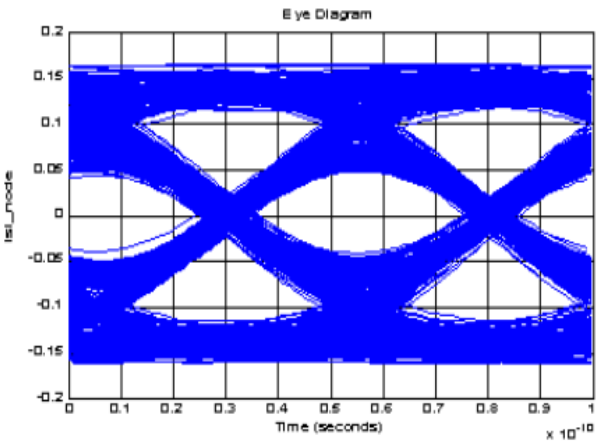


Figure 4.26. Eye diagram of the via structure including the packaging, with transmission line (width=3.1mil, spacing=2mil) output on layer 5 and bit rate=10 GHz

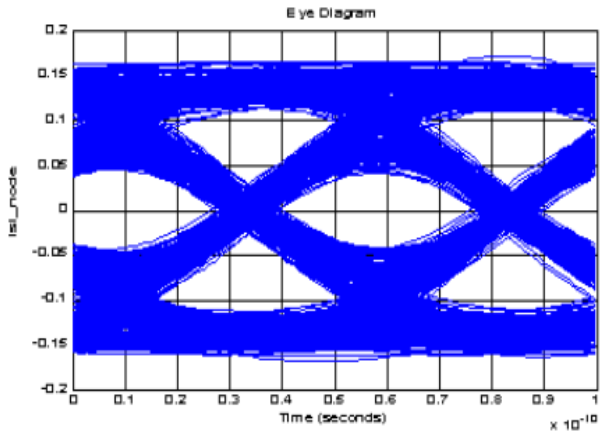


Figure 4.27. Eye diagram of the via structure including the packaging, with transmission line (width=3.1mil, spacing=2mil) output on layer 8 and bit rate=10 GHz

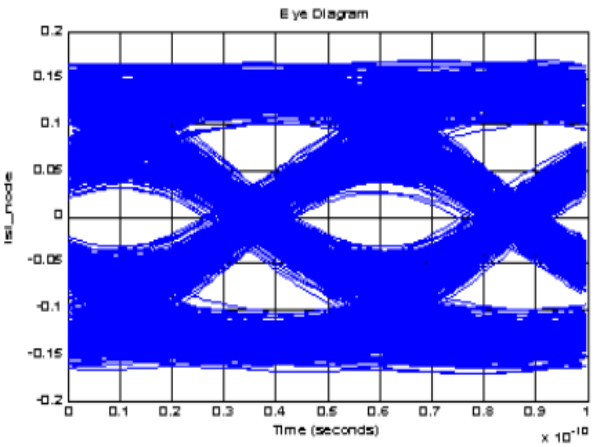


Figure 4.28. Eye diagram of the via structure including the packaging, with transmission line (width=3.1mil, spacing=2mil) output on layer 10 and bit rate=10 GHz

On the other hand, the package itself is low pass, as seen in Figure 4.29.

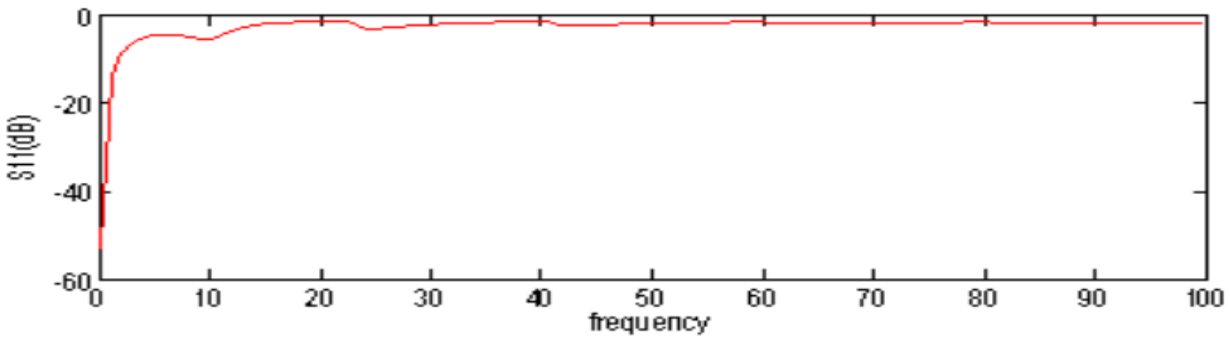


Figure 4.29. S11 of the packaging itself.

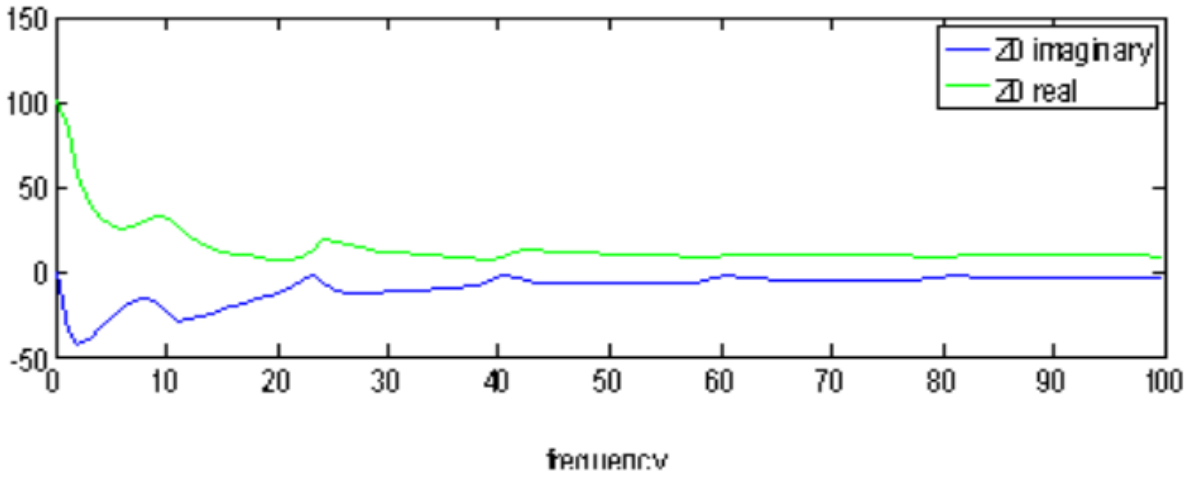


Figure 4.30. Characteristic impedance of the package.

The figure above (Figure 4.30) shows the characteristic impedance of the package. The best eye opening without taking the package into consideration happened for layer 10, instead, while considering the package, the best performance occurs between layer 5 and layer 8 and this is because there, the input impedance is matched with the via's impedance.

Inductive, capacitive and resistive parasitics are associated with the traces, pins, bond wires, input/output pads, and on-chip interconnects at PCB, package, and chip levels. The overall result of these parasitics is that there is a non-zero impedance between the power grids on-chip. While consisting of R, L, and C parasitics, the impedance characteristics are dominated by inductive effects, followed by capacitive and resistive effects. This in turn has a global effect for all the circuits on the chip. [19].

4.5 Via Modeling

The modeling of a single via has been performed with ADS. Figure 4.31 shows an example of the via that has been modeled.

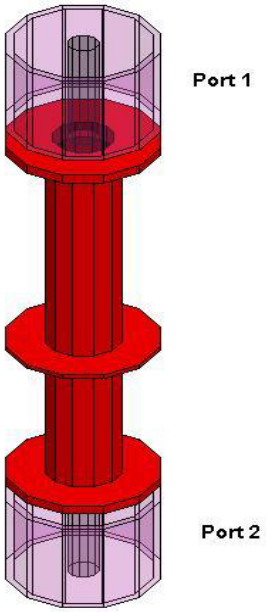


Figure 4.31. Via to be modeled

The via has been modeled up to 100 GHz as a series cascade of RLC circuits like the one showed in Figure 4.32.

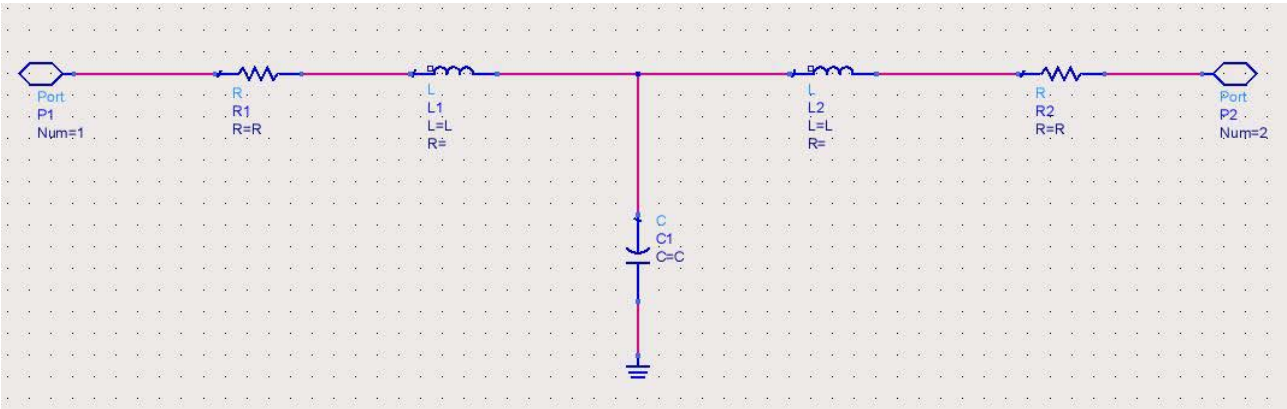


Figure 4.32 RLC circuit used for via modeling

A total number of 80 RLC circuits have been needed to simulate the total length of the via. At 100 GHz, the wavelength is 1.5 mm. The criteria is that the maximum length

that an RLC circuit can model is 20 times smaller than the wavelength, therefore the maximum length for an RLC circuit is 75 micrometers. Since the total length of the via is 60.5 mil, which is 1.5367 mm, 80 blocks (80 cascaded RLC circuits) are needed, as it is shown in Figure 4.33.

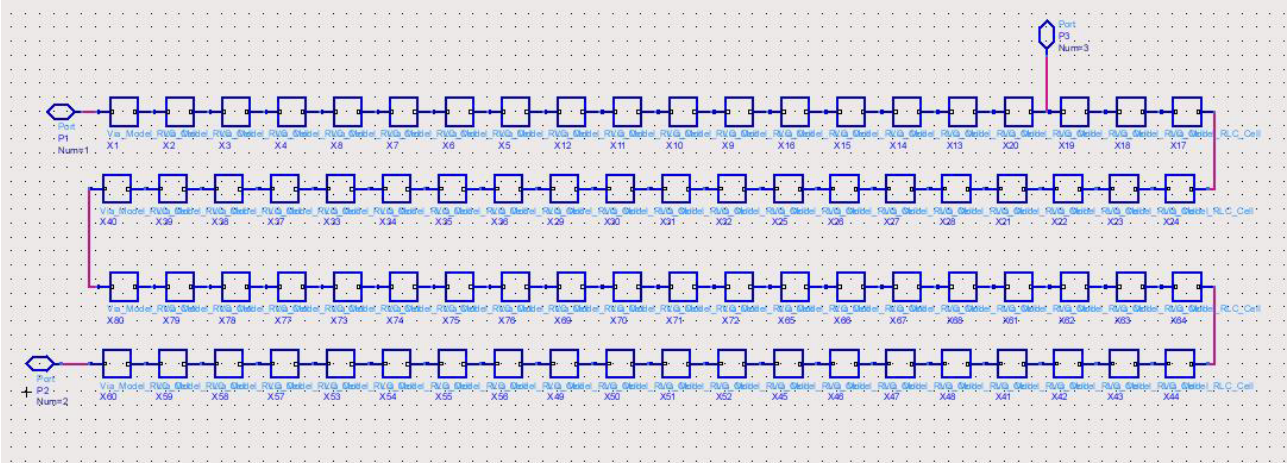


Figure 4.33. 80 blocks of RLC circuits that model the 6.5 mil length of the via.

The simulation of the real via's behavior versus the model's has been performed using the diagram showed below in Figure 4.34.

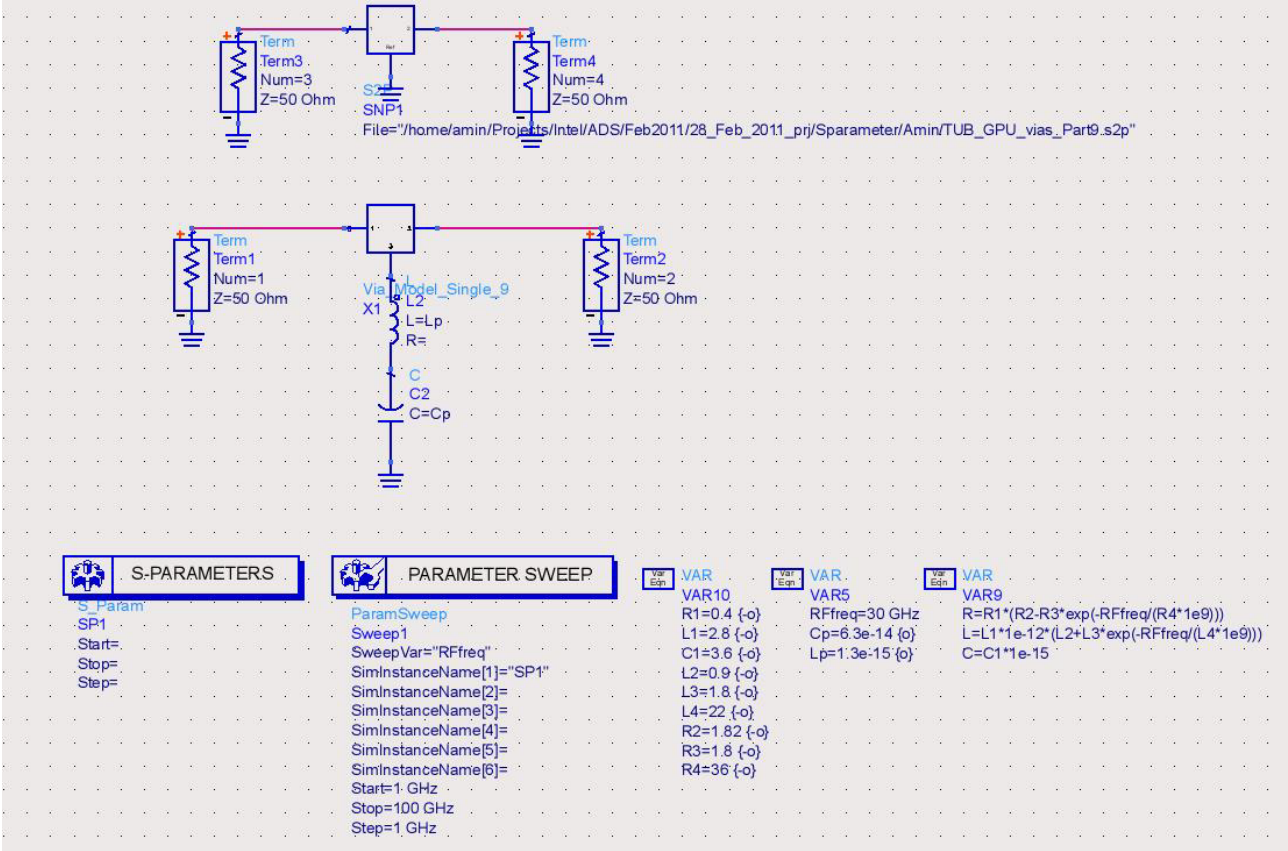


Figure 4.34. Diagram for simulation of the real via's performance versus the model's performance.

The values for R, L and C follow the next equations:

R = R1*(R2-R3*exp(-RFfreq/(R4*1e9)))

L = L1*1e-12*(L2+L3*exp(-RFfreq/(L4*1e9)))

C = C1*1e-15

Where the values of every constant are in the following table (Table 4.1):

COMPONENT	VALUE
R1	0.4
R2	1.82
R3	1.8
R4	36
L1	2.8
L2	0.9
L3	1.8
L4	22
Lp	1.3e-15
C1	3.6
Cp	6.3e-14
RFfreq	30 GHz

Table 4.1. Component values.

The graphic of R and L is showed below in Figure 4.35 while C is constant.

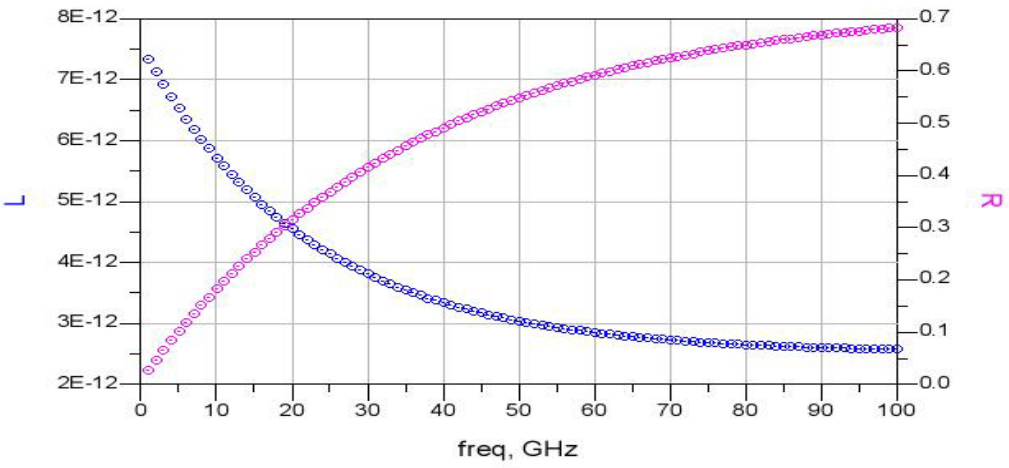


Figure 4.35. R and L graph.

Here below, in figures 4.36 through 4.46 are shown the results of the model (red) in comparison with the real via behavior (blue). The approach is accurate enough and the model is available to use.

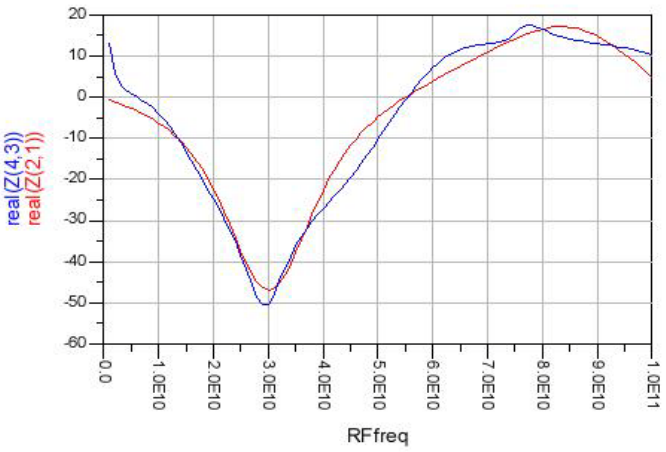


Figure 4.36. Real part of the reflection coefficient.

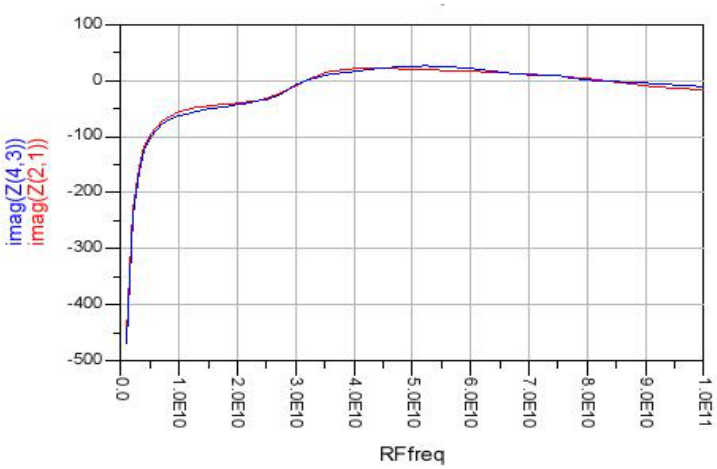


Figure 4.37. Imaginary part of the reflection coefficient.

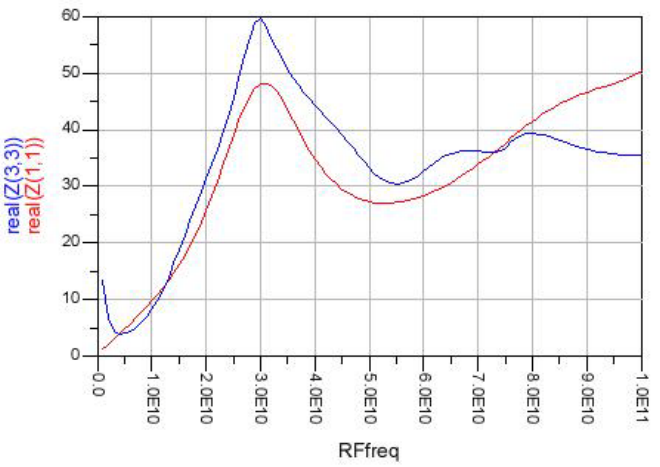


Figure 4.38. Real part of the transmission coefficient.

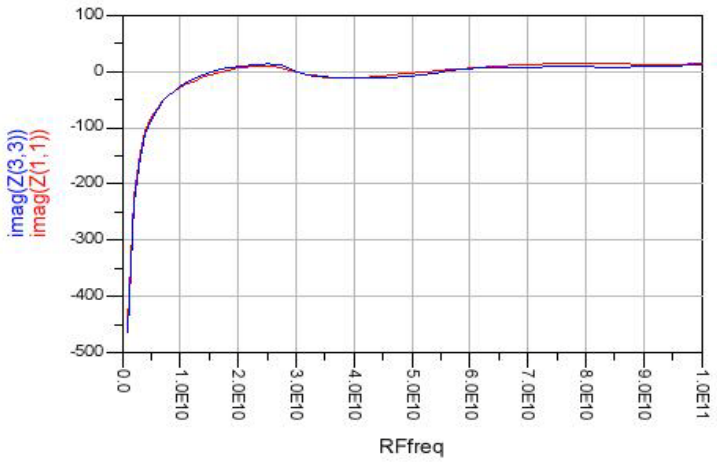


Figure 4.39. Imaginary part of the transmission coefficient.

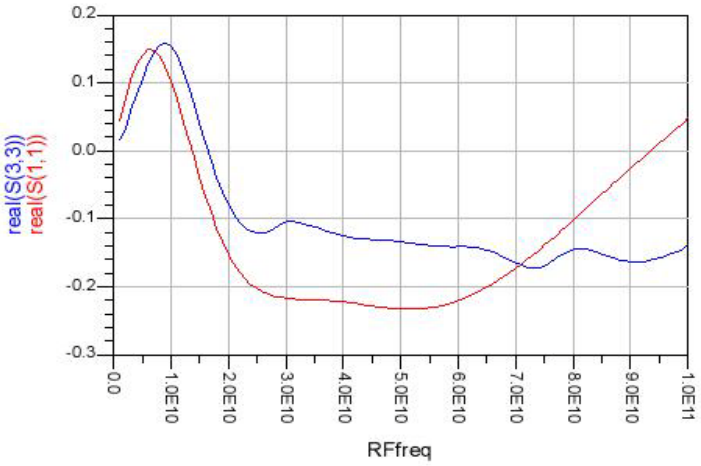


Figure 4.40. Real part of S11

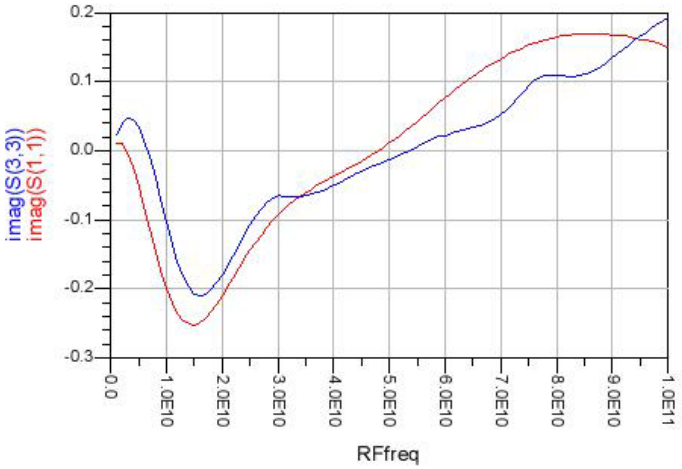


Figure 4.41. Imaginary part of S11

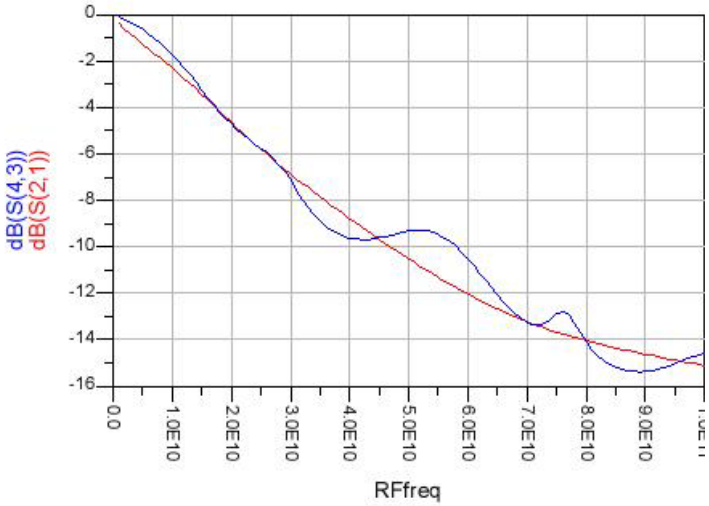


Figure 4.42. S21 in dB

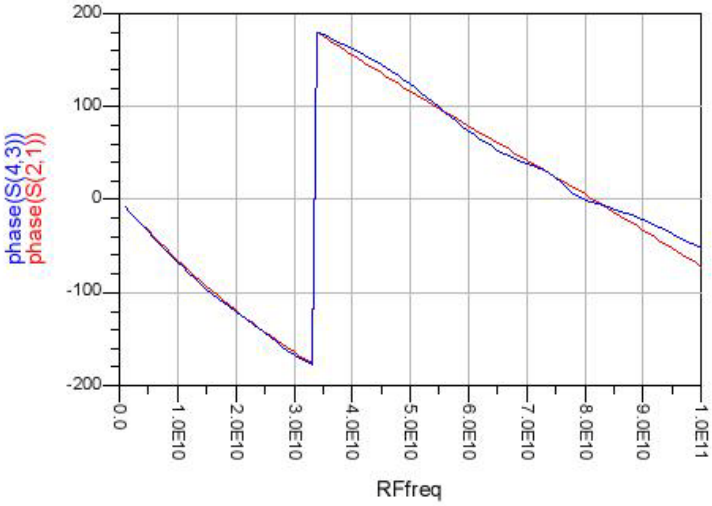


Figure 4.43. Phase of S21

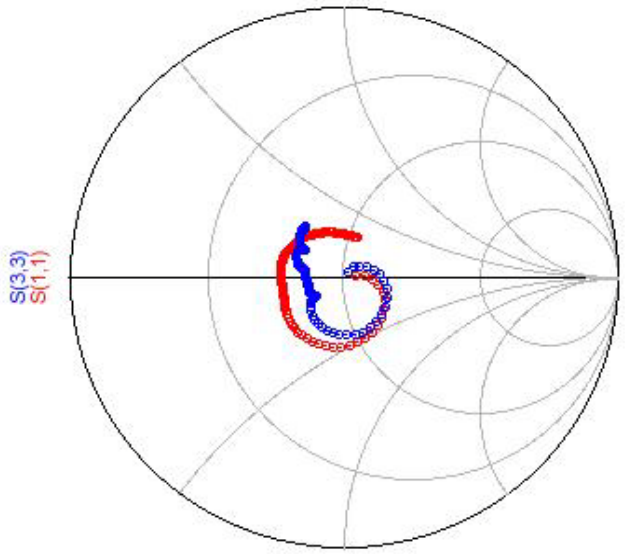


Figure 4.44. Smith Chart for S11

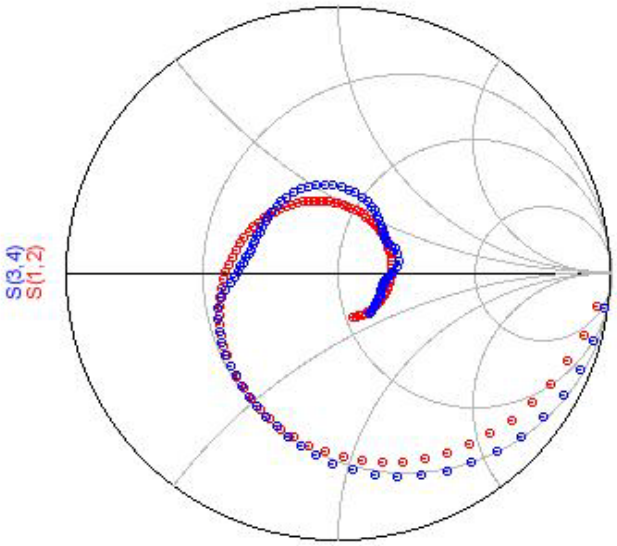


Figure 4.45. Smith Chart for S12

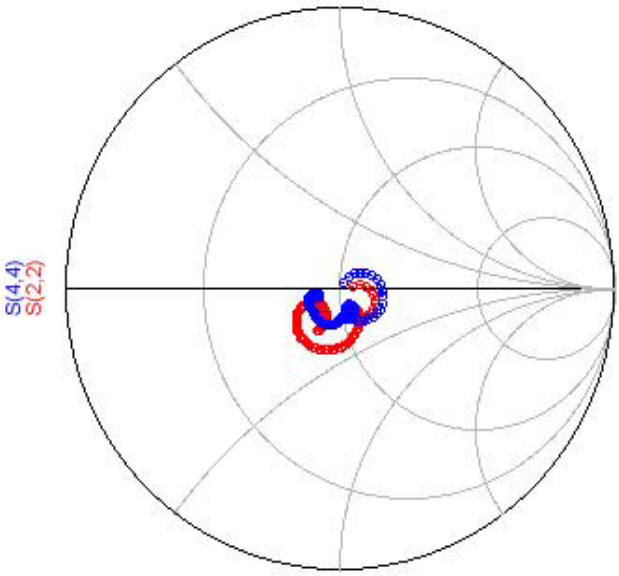


Figure 4.46. Smith Chart for S22

5. Conclusions And Future Work

The purpose of this work was to find the problems that affect the SI worsening the communication between the CPU and the DRAM. After simulating the PCB's interconnections and the package we can conclude that the package is the biggest SI problem.

Among the PCB's interconnections there are vias, transmission lines and steps. Transmission lines present reasonable losses. Regarding the vias, we have seen that they present a resonance frequency at very low frequencies, and as the resonance frequency decreases, the eye deteriorates. Comparing the effect of the vias with the transmission lines' losses, we can see that the vias have much more impact on the eye diagram, specially at higher bit rates. The eye closes as the bit rate increases. About the steps, we can see a little variation between taking by sweeping the transmission lines, but the best performance is for the biggest sweep, a width of 2 mil and a spacing of 3.1 mil; once again, it is seen that as the bit rate increases the eye closes.

By switching the signal layer at different layers in the PCB, we could that the best eye diagram occurs when the transmission lines are in the middle layers (5 and 8) because the impedance there is better matched.

However, when taking the packaging into account, the eye diagram really deteriorates a lot. The package is low pass and introduces parasitics elements that really cause signal integrity failure. This was expected since science has worked a lot towards increasing speed, but the packages have not evolved at the same pace.

EM Interferences increase as speed increases, which produce shorter wavelengths in comparison with the transmission lines' length that make crosstalk increase. In addition, this high speeds usually need high currents to be produced. The high currents tend to cause ground bounce specially in wide transmission lines where many signals switch simultaneously. Moreover, this high currents increase the quantity of radiated electromagnetic energy and with it crosstalk.

The future work on this project would be finding a solution for all this remarked problems in order to solve them and achieve the goal of having a good quality high speed transmission between the CPU and the DRAM. Things such as working towards the study of the package, improving the matching between the it and the vias and improving the via characteristics or changing the substrate should be done.

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List Of Figures