Contents

Acknowledgments **iii**

Abstract **xv**

Resumen **xix**

Resum **xxiii**

1 Introduction **1**

1.1 Motivation 1

1.2 Objectives 4

1.3 Dissertation outline 7

2 Background and State of the art **9**

2.1 Networks on-Chip 10

2.1.1 Systems on-Chip 11

2.1.2 Shared bus 14

2.1.3 A new design paradigm 16

2.1.4 Networks on-Chip components 17

2.1.5 Topology 31

2.1.6 Virtual Channels 33

2.1.7 Networks on-Chip performance evaluation 35

2.1.8 Networks on-Chip physical synthesis evaluation 35

2.1.9 Reference architecture 36

2.1.10 Design challenges for Networks on-Chip architectures . . 41

2.2 State of the Art 44

3 Topology exploration for Networks On-Chip 51
3.1 Introduction . . . 51
3.2 The high level view . . . 53
3.2.1 High level topology properties . . . 53
3.2.2 Topologies for Networks on-Chip . . . 57
3.2.3 High level topology exploration . . . 70
3.3 Networks on-Chip modelling . . . 74
3.3.1 Networks on-Chip behavior abstraction . . . 75
3.3.2 Network traffic generation . . . 76
3.3.3 Validation of Transaction-Level simulator accuracy . . . 77
3.3.4 Case study: Parametrical exploration . . . 81
3.4 Physical design pitfalls . . . 92
3.5 Case study: 16-tiles systems . . . 96
3.5.1 Total wire length . . . 97
3.5.2 Switch degree . . . 100
3.5.3 Link length . . . 101
3.5.4 Link performance boosting . . . 102
3.6 Case study: 64-tiles topologies . . . 110
3.6.1 Characterization methodology . . . 111
3.6.2 Physical implementation . . . 113
3.6.3 Pipeline stage insertion for 64-tiles systems . . . 115
3.6.4 The performance prediction gap . . . 117
3.7 Case study: assessing Multi-stage Interconnection Networks . . . 121
3.7.1 Topologies under test . . . 121
3.7.2 Floorplanning . . . 126
3.7.3 Physical evaluation . . . 129
3.7.4 Performance evaluation . . . 132
3.8 Conclusions . . . 134

4 Virtual Channels for Networks On-Chip 137
4.1 Introduction . . . 138
4.2 Classical virtual channel design . . . 140
4.2.1 Classical virtual channel switch architecture . . . 140
4.2.2 Conventional multi-stage virtual channel switch . . . 142

4.3 Bringing virtual channels to Networks On-Chip 146
4.3.1 Motivation 146
4.3.2 Proposed multi-switch implementation 147
4.3.3 Full network replication 149
4.4 Architecture comparison 150
4.4.1 Physical synthesis 151
4.4.2 Performance comparison 158
4.5 Conclusions 165

5 Design Space Exploration for Networks On-Chip 167
5.1 Introduction 168
5.2 The industry point of view 170
5.2.1 Network architecture 170
5.2.2 Target domain 170
5.2.3 Traffic characterization 171
5.2.4 Core placement strategies 171
5.2.5 Full custom design 172
5.2.6 Simulation framework 173
5.2.7 NaNoC compatibility 173
5.3 LDSET 174
5.3.1 LDSET NoC simulator framework 175
5.3.2 Design space definition 177
5.3.3 Design space initialization 184
5.3.4 Design space exploration 186
5.3.5 Output generation 189
5.3.6 Example 190
5.4 Place & Route 191
5.5 Conlucions 197

6 Conclusions 199
6.1 Conclusions 199
6.2 Future Work 201
6.3 Contributions 203

Bibliography 207