UNIVERSIDAD POLITECNICA DE VALENCIA

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Silica and Silicon Nitride micro-fabrication processes development

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Objective

The general objective of this thesis is the development of processes to perform the oxidation of silicon wafers and the photolithography to etch silicon nitride with the operation of a diffusion furnace, spin-coater, mask aligner and wet chemical bench. Specifically, the objective is to develop the recipes to:

- grow a silicon dioxide layer on silicon wafers with thicknesses up to 270 nm and to characterize the oxidation rate of the furnace of the UPVfab cleanroom (www.fab.upv.es).
- Perform wet chemical etch of silicon nitride with a resolution of 1 micron.

Methodology

- Design and execution experiments consisting on oxidation runs of silicon wafers to obtain the oxidation rates of the diffusion furnace.
- Design and execution of experiments on the photolithography and etch processes to determine the variables allowing to fabricate silicon nitride structures of 1 micron width.

Theoretical developments performed

The work performed within this thesis has been mainly experimental and no theoretical developments have been developed.

Prototypes developments and laboratory work

The prototyping work has consisted on the development of:

- Recipes for the dry oxidation technique of silicon wafers to grow a given silicon dioxide layer.
- Recipes of the photolithographic process to obtain silicon nitride structures of 1 micron width.

The laboratory work has consisted on:

- the operation of a diffusion furnace, hot-plate, spin-coater, mask aligner, wet chemical bench and the use of chemicals for the photolithography process in microfabrication
- and the use of a profilometer and a Scanning Electron Microscope for the observation and characterization.

Results

Regarding the silicon wafers dry oxidation the following conclusions have been obtained:

- The gas density decreases along the furnace tube, producing a lower silicon dioxide thickness growth for the wafer located at the rear side of the wafer boat.
- The number and distribution of wafers in the boat (location and separation) has impact on the gas distribution within the furnace, and results into higher oxide growth at certain locations on wafers, thus increasing the thickness non-uniformities. Once the boat is loaded with a higher

amount of wafers closer one to each other, the non-uniformities decreased notoriously to values below 3%.

- Silicon dioxide layers with thicknesses up to 270 nm have been grown on silicon wafers to characterize the oxidation rate of the furnace of the UPVfab cleanroom, and the Deal-Grove or linear parabolic model has been applied and validated experimentally to predict the kinetics of the dry oxidation of silicon.

Regarding the silicon nitride photolithography process:

- Silicon nitride structures of 1 micron width have been obtained.
- The parameter space for the fabrication of silicon nitride structures of a height of 300nm has been explored, and a starting point for subsequent refinement experiments has been reached.
- The required equipment to fabricate silicon nitride structures with a repeatable result has been identified.

Future work

In the near future we would like to characterize the wet oxidation technique using the diffusion furnace of the UPVfab. In this thesis, only dry oxidation was attempted since several upgrades to the furnace are required for wet oxidation, and were not available at the time of this thesis.

Regarding the silicon nitride photolithography process, we would like to acquire an etching system with reflux of the evaporated water into the phosphoric acid, in order to keep constant the concentration, thus obtaining a constant etching rate and therefore leading to a desired repeatable etching step.

Publications

There have not been publications within this thesis work

Abstract

Two different microfabrication processes are explored in this work: the dry oxidation of silicon wafers and the photolithography of silicon nitride. Four oxidation runs have been performed, along three different oxidation times, to obtain the linear and quadratic oxidation rate constants to validate the Deal-Grove oxidation model of the diffusion furnace at the UPVfab. In addition, the silicon dioxide thickness non-uniformities on wafers upon their distribution on the boat carrier have been evaluated. The silicon nitride photolithography process variables have been determined to obtain structures of 1 micron width. The process variables to obtain 300nm height silicon nitride structures have been approximated and a required etching system with reflux of the evaporated water has been identified to keep constant the phosphoric acid concentration, thus keeping constant the etching rate and therefore allowing for repeatable fabrication.

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Content

1 MOTIVATION AND PRECEDENTS

The work of this thesis has been performed at the Institute of Telecommunications and Multimedia Applications of the Universidad Politécnica de Valencia (iTEAM-UPV), concretely within the Photonics Research Labs. The group has a broad experience on Photonic Integrated Circuits (PICs) through the design and characterization of Array Waveguide Gratings (AWGs) [1], Optical Frequency Domain Reflectometers (OFDRs) [2], Microwave Photonics Filters (MWPs) [3], Programmable Microwave Photonics Processors [4], Optoelectronic Oscillators [5] and many others. The PIC designs have been usually fabricated at external foundries through the participation on different projects and characterized at the group laboratories.

The UPV owns a clean room which was stablished by Siliken, a solar cell manufacturing company aroung 2008-2009, consisting on a 500 m^2 class 100-10000 (ISO-5/7) 6'' MEMS which had been operated by industrial agents since 2015. The operation of the clean room has been recently transferred to the UPV, which is considering to become a reference custom micro fabrication foundry for research, education and semi-industrial manufacturing purposes.

At the moment of this work, part of the clean room facilities were not yet ready to be operated since several maintenance operations needed to be performed by the equipment manufacturers. However two processes of general interest were identified which could be started relatively quickly. One of these processes is based on the use of a diffusion furnace to perform the oxidation of silicon. The other process is related to the photolithography of different materials.

2 INTRODUCTION

Silicon in general is a chemical element which has been widely used in the microelectronics industry since the 60's due to its semiconductor properties which allowed the revolution in the electronics world allowing the integration of semiconductor devices and passive components on a common substrate. Today, Silicon is the dominant material used in the integrated-circuit (IC) industry not only for its semiconductor properties and for its abundancy in nature, but also because of its processing advantages in comparison with other materials.

A derived from silicon is the silica which is a combination of silicon plus oxygen with insulating properties very appreciated in the semiconductor industry. The case of the silicon dioxide (SiO2) is very easy to obtain since it is native in silicon. As occurs with silicon, silica is appreciated not only for its electrical properties but also for its role in IC fabrication processing capabilities being used as a mask to selectively process layer materials below it through different photolithographic processes as we will see in this thesis.

Silicon nitride is another combination of chemical elements, silicon and nitrogen, widely used in the IC manufacturing industry as an insulator and as an etch mask in microfabrication

processes, similar to the silicon dioxide, however with better performance when used as an etching mask. The interest for silicon nitride in this thesis, instead of its processing properties for IC manufacturing, is related to the optical properties of the material that shows a broadband behaviour [6] allowing a wide range of applications such as biophotonics, tele/datacom, optical signal processing and sensing, from visible, through near to mid-infrared wavelengths.

Most of the processes used in semiconductor ICs and materials are suitable for Photonic integrated Circuits (PICs) manufacturing which is the interest research field of the group where this master thesis has been developed.

3 THERMAL OXIDATION OF SILICON

Thermal oxidation is used in microfabrication to produce oxide on the surface of a wafer. It consists on the diffusion of an oxidizing agent into the wafer at high temperature and its reaction with it. Thermal oxidation may be applied to different materials, but the experiments performed during this thesis will only consider oxidation of silicon substrates producing silicon dioxide.

In silicon, a native oxide of several nanometers thickness grows in hours or days, depending on the surface conditions, and similar thin oxides are created using oxygen plasma or in oxidizing wet treatment. The native silicon dioxide is a high-quality electrical insulator and can be used as a barrier material during impurity deposition. These two properties have made the silicon dioxide to be the dominant material for the fabrication of electric integrated circuits. For example, thin oxides (1-20 nm) are used to create capacitor dielectrics, CMOS transistors, electrodes in flash memories and chemical sensors. Thick oxides (100-2000 nm) are used as diffusion and etch and electrical isolation layers. In our case we will use the silicon dioxide in photonics circuits at a functional level in order to confine the optical modes in silicon and silicon nitride waveguides and also at fabrication techniques level as a mask to etch other materials such as silicon nitride.

Other techniques apart from thermal oxidation exist to create oxides, such as Chemical Vapor Deposition (CVD) but it produces less-quality oxide in terms of roughness uniformity, density, electric breakdown, etc. However CVD oxides can create a micrometer oxide layer in minutes while thermal oxidation requires hours or days. CVD oxides have higher wet etch rate in Hydrofluoric acid (HF), but usually they are used when thermal oxidation cannot be employed mainly because of the high temperatures required for it. Other oxidation techniques are used in microfabrication of thin aluminium layers, such as chemical oxidation in acidic solutions or oxygen plasma.

In our work we aim at obtaining high quality thick silicon dioxide (hundreds of nanometers), hence we will resort to thermal oxidation processes. The aim is to develop and characterize a dry oxidation process for Si wafers. Hence, the chapter is structured as follows. Firstly, a short

review on the physics and models to characterize dry oxidation of Silicon is given in sections 3.1 and 3.2. Most of the materials used in this thesis are a summary of references [7] [8] [9].

3.1 THERMAL OXIDATION: DRY AND WET OXIDATION

Thermal oxidation takes place by heating the wafer to a high temperature (900-1200ºC) in an atmosphere containing pure oxygen (dry oxidation) or water vapour (wet oxidation) which diffuse through silicon dioxide. The oxygen arriving at the surface of the silicon reacts/combines with silicon generating silicon dioxide. The chemical reaction at the silicon surface for the dry oxidation process is:

$$Si + O_2 \rightarrow SiO_2 \quad (1)$$

and

$$Si + 2H2O \rightarrow SiO2 + 2H2 \quad (2)$$

for the wet oxidation.

Dry oxide grows at a lower rate, thus achieve a better thickness control compared to wet oxidation. An hour of dry oxidation at 900ºC produces an oxide layer about 30nm thick, while for the same duration, wet oxidation produces a thickness of 130nm. In addition, dry oxides exhibit lower interface charges and trap states, important for transistor operation. Thin oxides also have many auxiliary and sacrificial roles: a thin oxide under certain materials such as nitride films relieves stresses caused by nitride.

Wet oxidation is commonly used to grow oxides 100-2000nm thick in a faster way, and are used for device isolation and as masking layers for ion implantation, diffusion and etching steps.

3.2 THE DEAL-GROVE OXIDATION MODEL

The Deal-Grove or linear parabolic model [7] is used to predict the kinetics of thermal oxidation of silicon. As mentioned previously, in order to grow a layer of oxide, oxygen must reach the silicon interface for its reaction with it. The model assumes that an oxide of some thickness x_i is already present at the surface of the silicon because of a native growth (ambient oxidation) or a previous thermal oxidation process. As oxide grows, the oxygen has to diffuse through a thicker layer and the growth rate decreases over time. Fig. 1 (left) shows the concentration of oxygen reaching the Si-SiO_2 interface which reacts with it. As oxide expands during growth, the silicon is consumed and the final oxide layer is approximately 54% above the original surface of the silicon and 46% below the original surface (Fig. 1 right), although exact percentages depend on the density of the oxide.

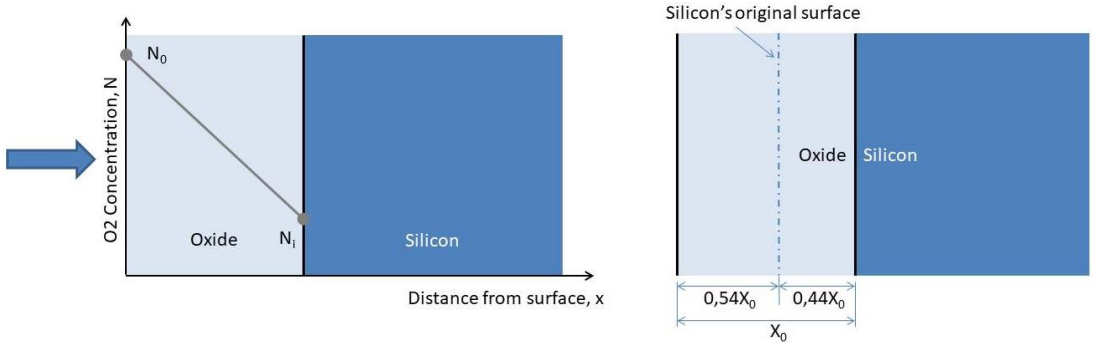

Fig. 1. Concentration of oxidizing species along oxide layer (left). Silicon consumed and resulting oxide expansion during growth (right).

The SiO2 thickness over time can be predicted using the Deal-Grove model using the following differential expression:

$$\frac{x_0^2}{B} + \frac{x_0}{B/A} = t + \tau \tag{3}$$

where:

$$\tau = \frac{x_i^2 + A x_i}{B} \tag{4}$$

$$B = \frac{2DC_0}{C_1} \tag{5}$$

$$\frac{B}{A} = \frac{C^* k_s}{N_1} \tag{6}$$

$\boldsymbol{x_i}$ corresponds to any oxide present at the start of the oxidation and $\boldsymbol{\tau}$ represents the time that would have been required to grow the initial oxide, $\boldsymbol{D}$ is the oxidant diffusivity in the oxide, $\boldsymbol{C_0}$ is the concentration of the oxidizing species at the Si-SiO_2 interface, $\boldsymbol{C_1}$ is the number of the oxidizing species required to produce a unit volume of the oxide, $\boldsymbol{N_1}$ is the number of oxidant molecules incorporated per unit volume of oxide grown and $\boldsymbol{k_s}$ is the rate constant for the reaction at the Si-SiO_2 interface. Solving the parabolic equation leads to the expression for oxide thickness in terms of growth time:

$$x_0 = \frac{A}{2}\left\{\sqrt{1 + \frac{t+\tau}{A^2/4B}} - 1\right\} \tag{7}$$

For short process times with $(t+\tau) \ll A^2/4B$, the linear term dominates the equation EC being the oxide growth proportional to time, and the ratio **B/A** is called the **linear growth rate constant**. In this region, **the growth rate is limited by the reaction at the silicon interface**.

$$x_0 = \frac{B}{A}(t + \tau) \tag{8}$$

For long times with $(t+\tau)>>A^2/4B$ and $t>>\tau$ the oxide growth is proportional to the square root of time, and **B** is called the **parabolic rate constant**. In this region, **the growth rate is limited by the reaction at the silicon interface**.

$$x_0 \approx \sqrt[2]{B(t+\tau)} \tag{9}$$

Values for *B* and *B/A* should be calculated and therefore test the predictions of the linear parabolic model against experiment. However, in fact, **these constants are normally determined experimentally by extraction from the growth data** [9]. The reason for this approach is that we do not know all the parameters in ec. 6 since k_s hide a lot of physics associated with the interface reaction. Figure 2 describes how the oxidation rate constants can be obtained from experimental data. By plotting oxide thickness versus $\left(\frac{t+\tau}{x_0}\right)$, *B* is directly extracted from the slope of the line and *A* from the intercept, and thus *B/A* is retrieved. This approach is suitable for a wide range of conditions. If the experimental data do fall on a straight line when plotted in the form of Fig.2, then the data are well described by a linear parabolic growth law. In fact, there are conditions that do not result in data that lie on a straight line, therefore these are not well modelled by this approach. Oxidations grown on flat un-patterned surfaces using O_2 or H_2O environments with a thickness larger than 20nm are usually well described by the linear parabolic law and values for B and B/A can be extracted.

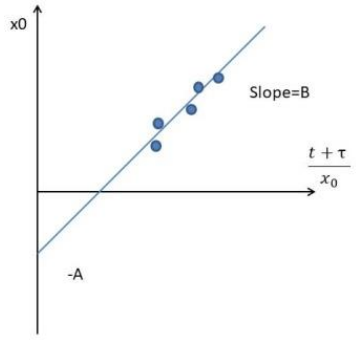

Fig 2. Extraction of rate constants B and A

Figure 3 shows the silicon dioxide growth over time for <100> crystal orientation silicon wafers using dry and wet oxidation at 900 and 1100ºC (from rate constants extracted from [8]). As it can be observed, the oxide growth is much faster for high temperatures, and there is a big difference on the oxidation rate between wet and dry techniques as previously commented. It can also be observed that the oxide growth does not follow a linear law, but a linear-quadratic as mentioned previously.

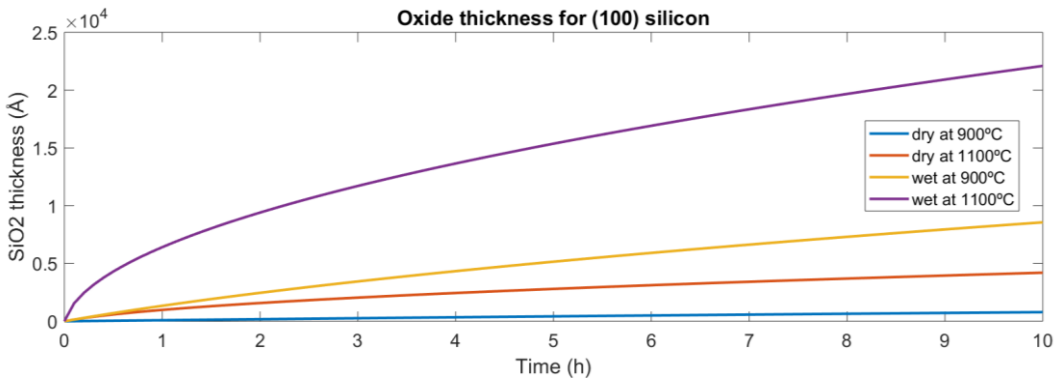

Fig. 3. Oxide growth over time for wet and dry techniques at two different temperatures.

3.3 SILICON WAFERS' DRY OXIDATION EXPERIMENTS

In this section the equipment used for the oxidation of the silicon wafers and the experiments and results are described.

The wafers oxidized in the following experiments have a diameter of 150 mm and are 675 μm thick, polished on one side with a crystal orientation 100 with a resistivity between 10.5 and 19.5Ω/cm.

3.3.1 DESCRIPTION OF THE DIFFUSION FURNACE

The equipment used for the oxidation is a 3 Stack Diffusion furnace, model TS 81003 from Tempress Inc., designed to perform Diffusion/Atmospheric and Low Pressure Chemical Vapour Deposition (LPCVD) processing on wafers. The furnace is installed in the cleanroom at the facitily UPVfab (www.fab.upv.es).

The diffusion system is a modular horizontal furnace designed to process (silicon) wafers as part of the manufacturing technology of semiconductor, optical, MEMS and solar devices. The integrated modular construction provides discrete compartments for control equipment. All electrical wiring, including the basic units of the temperature controller and electrical components are housed in the base of the furnace.

Figure 4 shows an example of the schematic of the system which is divided into four different modules: load station, furnace, gas cabinet and power cabinet. From the load station, the user loads/unloads the boat containing the wafers on a paddle that enters automatically into the furnace for their process. To prevent particles on the wafers during the load/unload process, a constant horizontal laminar flow is created from the load station into the cleanroom. The remote control cabinet in the load station contains TFT-Touchscreens, one for each tube. These supply the user interface for communication with the Digital System Controllers (Digital Process Controller, Digital Temperature Controller and Digital Motion Controller). The furnace cabinet contains 3 tubes with a heating element each. The heat exchanger on the top of the furnace cools the exhausted air. Three phase power transformers are used to maintain a constant

temperature with a minimum of disturbance. The gas cabinet provides the desired flows of (a mixture of) gasses required for the different kind of processes. Each process has its own gas system including pre-plumbing, gas panels and electronic components. The main power cabinet distributes all electrical facilities to the desired tubes, gas cabinet and load station.

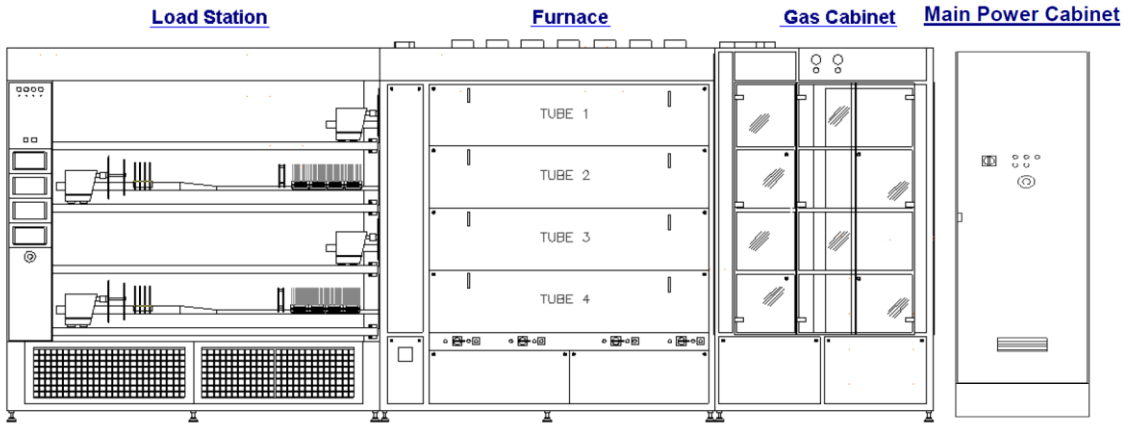

Fig. 4. Schematic of the Diffusion furnace

3.3.2 DRY OXIDATION RECIPE AND PROCESS RUNS

The recommendation by the furnace manufacturer is that the required gas flow should be calculated to obtain a refresh interval of 5 minutes for standby conditions and 3 minutes for processing [10]. In addition, since we are going to operate the furnace at high temperatures, we need to take into account the gas expansion which is 3.6x and 4.7x at 700ºC and 1000ºC respectively [10]. In our case, the tube of the furnace used for oxidation has a volume of 155 litres, so we chose a flux of 8.6 and 11 slm[1] for standby and processing respectively taking into account the recommended gas renewal and the gas expansion for the operation temperatures. Table 1 shows the recipe used for the oxidation experiments which consists on a sequence of actions at a given temperature, duration and gasses fluxes (O_2 and N_2).

During stand-by, nitrogen is introduced as a purge at 8.6 slm until the process recipe is started by the user and then the flux increases to 11 slm since the paddle comes out, that prevents particles coming into the tube. Once the paddle is out, the user can load the boat containing the wafers, then the boat is moved into the tube, the temperature stabilizes at 700ºC and starts a temperature ramp to 1000ºC, the N_2 flux stops and the O_2 is set to 5.5 slm. Next, the tube temperature arrives to 1000ºC the O_2 flux is set to 11slm for the desired oxidation time. After this, an annealing process takes place for 5 min without O_2 and with N_2 at 16.5 slm. The annealing, once no O_2 is being injected (no SiO_2 is growing anymore) and maintaining the 1000ºC temperature, reduces the stress of the SiO_2. Finally, the cooldown step starts to the stand-by temperature, 700ºC, and the paddle moves out. Once the temperature of the boat has

[1] slm stands for “standard liter per minute”, is a unit of volumetric flow rate commonly employed for gas flows. See https://en.wikipedia.org/wiki/Standard_litre_per_minute.

cooldown, the wafers are ready to store them on a closed boat and send them to the CNM for their characterization.

Table 1. Dry oxidation recipe used in the furnace.

Process step	Temperature	Step duration (min.)	O2 flux [slm]	N2 flux [slm]
1 Stand by	700ºC	90	0	8.6
2 Boat out	700ºC	7	0	11
3 Load Wafer boat	700ºC	5	0	11
4 Boat in	700ºC	10	0	11
5 Stabilize	700ºC	10	0	8.6
6 Heat up (10ºC/min)	700ºC-1000ºC	30	5.5	0
7 Dry ox	1000ºC	**180**	11	0
8 Annealing	1000ºC	5	0	16.5
9 Cooldown	1000-700ºC	120	0	11
10 Unload wafer	700ºC	7	0	11

Figure 5 shows the evolution of the temperature along the process steps.

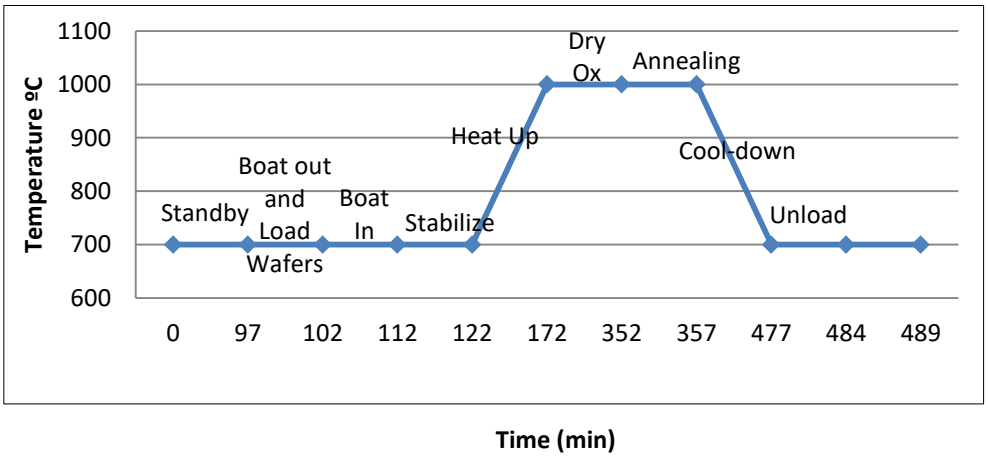

Fig. 5. Temperature evolution of the tube furnace along the dry oxidation recipe.

We used the previous recipe to perform 3 different runs varying the duration of the oxidation step, being: 180, 360 and 540 minutes. On each of the runs we loaded 6 wafers. The wafers were located as follows: 2 at the front of the boat, 2 in the middle and 2 at the rear side as shown in Fig. 6 (left), so as to investigate process uniformity inside the furnace tube.

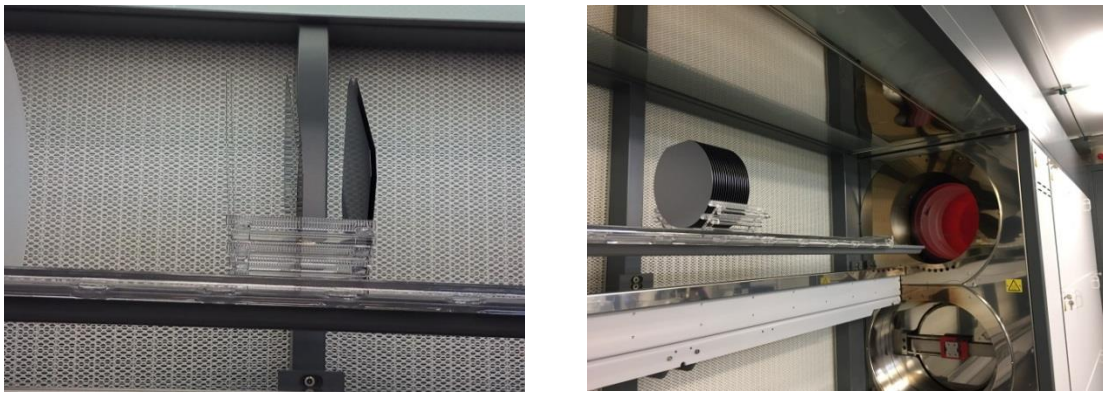

Fig. 6. Boat loaded with 6 wafers on the paddle ready to enter the furnace (left) and image of the furnace at 700ºC (right)

Pictures of wafers from the three runs are shown in Fig. 7, each with a different color, that corresponds to a different oxidation period (oxide thickness). The run corresponding to an oxidation period of 180 min. has resulted on a light/metallic blue, while for 360 and 540 min. has resulted on a light gold and red violet respectively. This is in agreement with well documented Si dry oxidation processes, as for instance in [8].

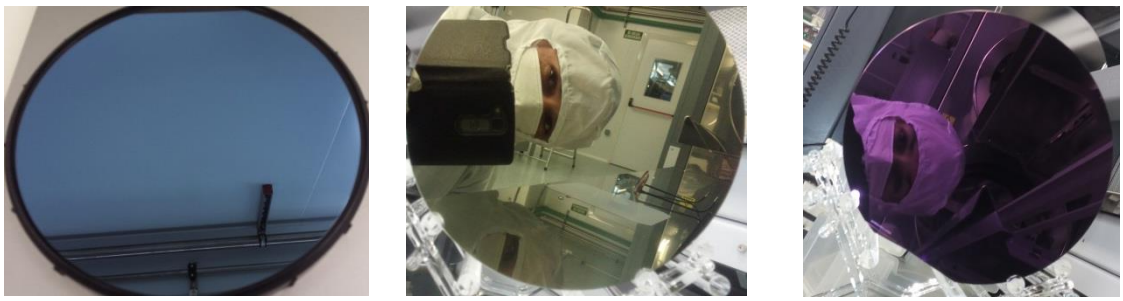

Fig. 7. Dry oxidated wafers for 180 (left), 360 (centre) and 540 min (right)

The thickness of the SiO2 grown in the wafers has been measured using the spectroscopic ellipsometer Auto SE from Horiba Jobin Ybon at a fixed wavelength of 650 nm and an incidence angle of 70º, in cooperation with the Instituto de Microelectrónica de Barcelona, Centro Nacional de Microelectrónica, Consejo Superior de Investigaciones Científicas (IMB-CNM-CSIC, in short CNM). For each wafer, 5 measurement points were taken following the distribution shown in Fig. 8 (left) and avoiding point 5 in the figure. The Fig. 8 (right) shows the mean thickness of the five measurement points for each wafer for the 3 runs. We can observe that the 180min run shows a thickness around 140nm and 220nm for the 360 minutes run, while 540 minutes of oxidation has resulted on a thickness around 270nm. We can also observe for all oxidation durations that the 2 wafers located at the rear side of the boat decrease the thickness respect to the others, probably because the gas density in the tube is decreased due to the barrier created by the wafers in front of them. To verify this we will need to perform a new oxidation process with a higher amount of wafers. Also we notice as described previously that the oxide growth does not follow a linear law.

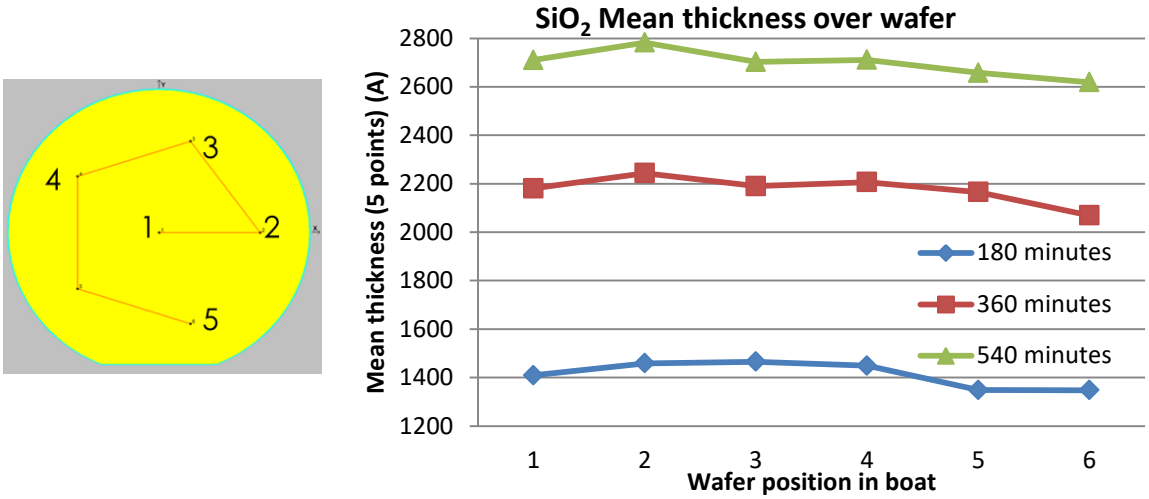

Fig. 8. Distribution of the 5 measurement points (left) and mean thickness for each wafer (right).

The mean values for the thickness and refractive index at the 650 nm wavelength for each sample and the standard deviation and non-uniformity, calculated as (Max-Min)x100/Mean are shown in table 2.

Table 2. Measurements of the oxidized wafers for Run 1, Run 2 and Run 3.

Sample	Identifier	Time (min)	Ellipsometer thickness (nm)	Mean Refractive index	Thickness non-uniformity (%)	Refractive index non-uniformity (%)
Wafer 1	RUN1_UPV_1	180	141±1	1.463±0.001	2.1	0.068
Wafer 2	RUN1_UPV_2	180	146±5	1.462±0.001	8.9	0.137
Wafer 3	RUN1_UPV_3	180	147±1	1.463±0.000	1.4	0
Wafer 4	RUN1_UPV_4	180	145±3	1.462±0.000	4.8	0
Wafer 5	RUN1_UPV_5	180	135±3	1.463±0.001	5.9	0.068
Wafer 6	RUN1_UPV_6	180	135±3	1.463±0.001	5.9	0.068
Wafer 7	RUN2_UPV_1	360	218±8	1.458±0.000	1.8	0.069
Wafer 8	RUN2_UPV_2	360	224±3	1.457±0.000	3.6	0.069
Wafer 9	RUN2_UPV_3	360	219±1	1.459±0.001	0.9	0.069
Wafer 10	RUN2_UPV_4	360	221±2	1.457±0.001	1.8	0.206
Wafer 11	RUN2_UPV_5	360	217±4	1.458±0.002	3.7	0.274
Wafer 12	RUN2_UPV_6	360	207±4	1.459±0.002	5.8	0.411
Wafer 13	RUN3_UPV_1	540	271±1	1.473±0.002	1.1	0.407
Wafer 14	RUN3_UPV_2	540	278±9	1.474±0.001	8.3	0.136
Wafer 15	RUN3_UPV_3	540	270±1	1.473±0.001	0.7	0.136
Wafer 16	RUN3_UPV_4	540	271±2	1.473±0.001	1.5	0.204
Wafer 17	RUN3_UPV_5	540	266±1	1.470±0.003	0.8	0.544
Wafer 18	RUN3_UPV_6	540	262±4	1.463±0.003	4.2	0.478

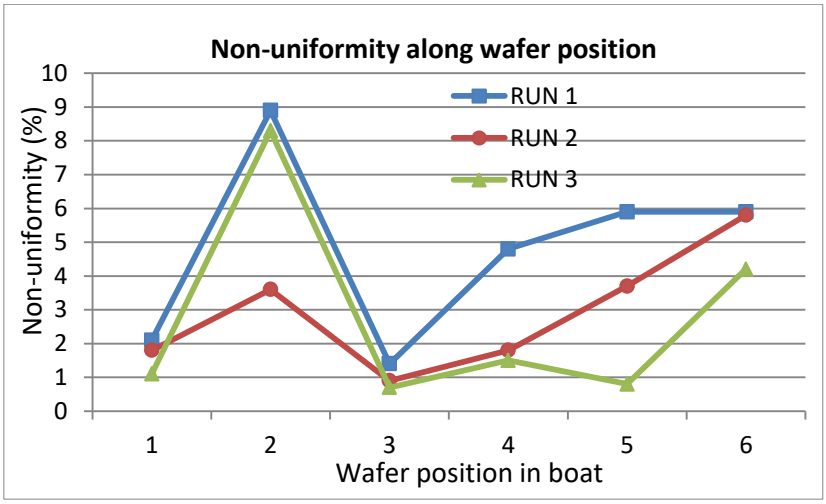

Fig. 9. Thickness Non-uniformities along of each wafer for Runs 1 to 3.

We also observe that the variation of the refractive index does not follow a progressive evolution, the values from the Run2 present values lower than expected. The thickness non-uniformity is quite good, however there is always any sample that presents a value higher than 3% as shown in Fig. 9.

Table 3. Measurements of the wafers for the oxidation Run 4.

Sample	Identifier	Ellipsometer Thickness (nm)	Refractive Index (@ 630nm)	Thickness non-uniformity (%)	Refractive Index non-uniformity (%)
Wafer 1	RUN4_UPV_1	218 ± 1	1,458 ± 0,001	0.7	0.069
Wafer 2	RUN4_UPV_2	222 ± 1	1,457 ± 0,001	1.3	0.069
Wafer 3	RUN4_UPV_3	224 ± 1	1,457 ± 0,000	1.4	0.069
Wafer 4	RUN4_UPV_4	225 ± 1	1,457 ± 0,000	1.4	0.137
Wafer 5	RUN4_UPV_5	223 ± 1	1,457 ± 0,000	0.8	0.000
Wafer 6	RUN4_UPV_6	234 ± 4	1,456 ± 0,001	5.0	0.206
Wafer 7	RUN4_UPV_7	224 ± 2	1,458 ± 0,000	1.8	0.000
Wafer 8	RUN4_UPV_8	223 ± 2	1,457 ± 0,001	2.1	0.137
Wafer 9	RUN4_UPV_9	219 ± 2	1,458 ± 0,001	2.1	0.137
Wafer 10	RUN4_UPV_10	217 ± 2	1,458 ± 0,000	1.8	0.000
Wafer 11	RUN4_UPV_11	214 ± 1	1,459 ± 0,001	0.8	0.137
Wafer 12	RUN4_UPV_12	210 ± 1	1,460 ± 0,000	1.5	0.069
Wafer 13	RUN4_UPV_13	206 ± 1	1,461 ± 0,001	1.0	0.137

Therefore, and in order to check the O_2 density decrease at the rear wafers and the non-uniformities, we performed a new experimental run with and oxidation time of 360 minutes and

with a larger number of wafers inside the furnace. The wafers that we used in Run 4 are the same ones used in the previous runs which we etched and cleaned.

The results obtained for the Run4 are shown in Table 3. It can be observed that the thickness non-uniformity of each wafer has improved considerably since, for the 13 wafers, there is just one which has a non-uniformity higher than 3%, which is comparatively for Runs 1-3, a very good result.

Figure 9 represents the mean thickness and the non-uniformity for wafers in Run 4. It can be observed that the growth oxide thickness is around 220 nm which is in agreement with the previous Run 2, since in both runs the oxidation time is 360 min. However, in the rear wafers of the boat carrier, from 9 to 13, it can be observed a decrease of oxide mean thickness. This confirms that the density of oxygen is impoverishing along the tube length. Regarding to the non-uniformity, we assume that it has been improved due to the thorough cleaning which has left the start silicon surface more uniform and, we presume the higher mean thickness and non-uniformity for wafer 6 is due to a defect in the etching and/or cleaning.

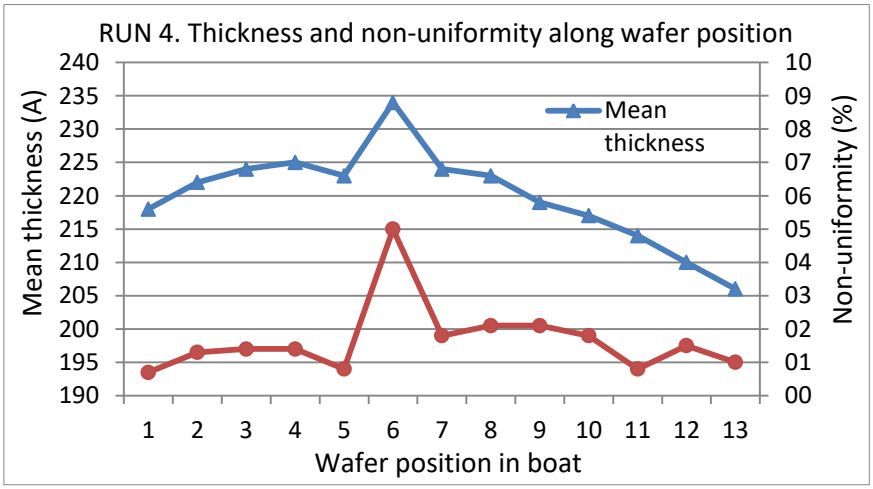

Fig. 9. Measured Grown SiO_2 thickness and non-uniformities of Run 4.

Once the repeatability of the oxide thickness growth along Runs 2 and 4 is verified, we have determined experimentally the linear and parabolic growth rate as described in literature and summarized in section 3.2 of this thesis. For that we have converted the X-axis as shown in Fig. 10 and plotted the measured thickness of the 3 Runs. Then, a fit to a first order polynomial has been made and the **linear and parabolic rate constants** of the furnace have been obtained which have been **A=0.1576µm/hr and B=0.01255µm^2/hr**. Using these values we can predict what will be the expected oxide growth for a given oxidation time, although we need to take into account the initial oxide growth time which is τ=0.5h in our case. If we substitute this values in equation 7 we obtain an expected oxide thickness of 145, 217 and 275nm for an oxidation time of 180, 360 and 540 minutes respectively which agree the measured thicknesses.

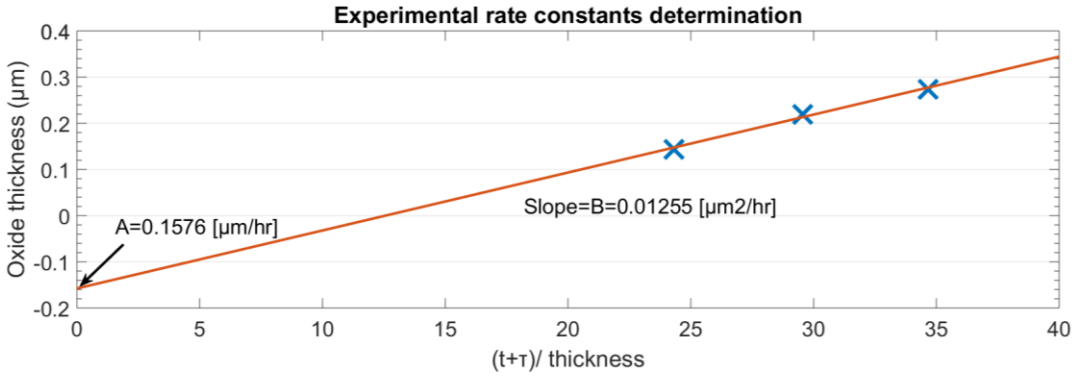

Fig. 10. Experimental extraction of the oxidation rate constants.

3.4 CHAPTER CONCLUSIONS

From the results obtained along the four oxidation runs, the following conclusions can be derived:

- The gas density decreases along the furnace tube, producing a lower silicon dioxide thickness growth for the wafer located at the rear side of the wafer boat.
- The distribution (location and separation) of the wafers in the boat influence gas turbulences, producing a higher oxide growth at certain locations on wafers, thus increasing the thickness non-uniformities. Once the boat is loaded with a higher amount of wafers closer one to each other, the non-uniformities decreased notoriously to values below 3%.
- The Deal-Grove or linear parabolic model has been applied and validated experimentally to predict the kinetics of the dry oxidation of silicon.

4 THE PHOTOLITHOGRAPHY PROCESS OF SILICON NITRIDE

These chapter of the thesis deals with the work performed in order to pattern silicon nitride layers, which are of our group interest for photonic circuits on silicon nitride (Si_3N_4), using the tools at the UPVfab facility (www.fab.upv.es).

The photolithography consists on printing structures on a wafer, and these printed structures that will be used to assist etching and/or ion implant processes to finally obtain the final structure, e.g. in our case (but not limited to) a photonic integrated circuit. Ultraviolet light passing through a mask transfers the pattern to a photoresist which is a light-sensitive film deposited on the wafer surface. The photoresist changes its properties upon exposure to the ultraviolet wavelengths in such a way that the exposed and unexposed resist areas have a different dissolution rate in the developer solution, obtaining a structured photoresist mask. The purpose of the development is to dissolve either the exposed (in the case of positive resists) or the unexposed (in negative resists) resist areas, resulting in the final desired resist structures.

Once the development is performed the next step is the etching of the material that will constitute the patterned structure. Figure 11 shows the photolithography process steps.

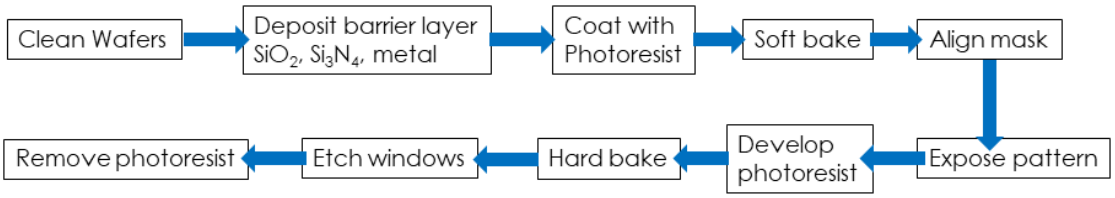

Fig. 11. Photolithography process steps.

4.1 DESCRIPTION OF THE EXPERIMENTS

The mask layout that we used in our experiments consists in 18 parallel straight lines which progressively increase their widths from 1 to 40 μm and are repeated along the mask surface. The reason of such a basic layout is because the straight lines facilitate the observation and characterization of the resulting patterns. In addition, as we will observe in this section, this set of parallel lines will help us validating each of the process variables, such as the energy of the exposure, development and etching time.

At the UPVfab we have not the facilities to fabricate the mask from the layout, so it was provided by CNM. It is fabricated on a quartz substrate which is transparent for the photoresist exposure wavelength. Figure 12 shows two pictures of the mask fabricated by the CNM on a quartz substrate, where the lines are fabricated in chrome. The quartz allows the pass of the ultraviolet light through it while the chrome blocks it, transferring in this way the pattern to the photoresist.

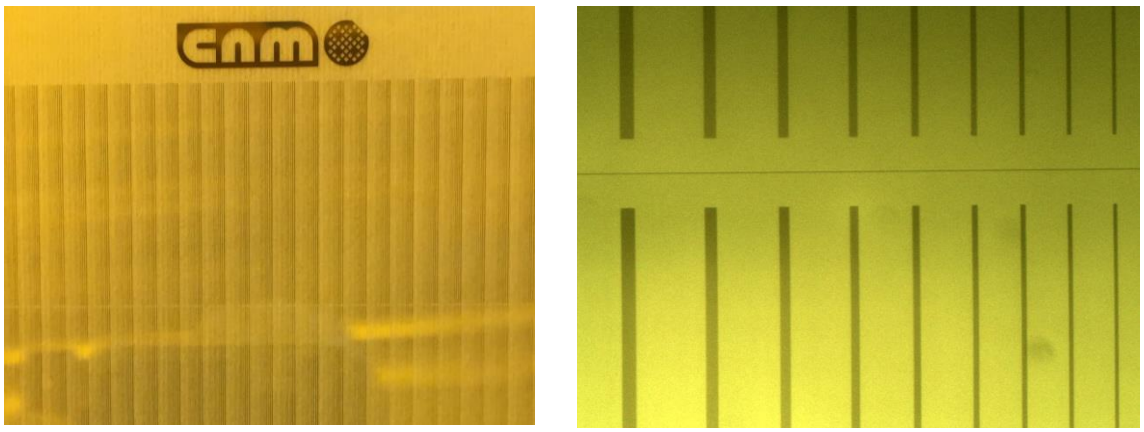

Fig. 12. Mask layout fabricated at the CNM (left) and lines of the mask observed at the microscope (right)

A set of wafers including an oxide layer as a protective mask for the etching of the silicon nitride, were supplied by CNM as well. The wafer layerstack, shown in Fig. 13, is the one commonly used by CNM in cooperation with our group, for manufacturing PICs.

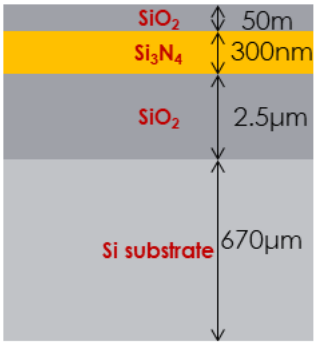

Fig. 13. Layer stack from wafers sent by CNM

On Table 4 are shown the layer thickness specifications and the layers thickness measurements of the delivered wafers.

Table 4. Thickness measurements of the layers at the wafers sent by CNM

Thickness (nm)				
Layer	**Specification**	**Wafer 1**	**Wafer 2**	**Wafer 3**
Thermal S_iO_2	2.500	2570 ± 4	2570 ± 4	2570 ± 4
Si_3N_4 (LPCVD)	300	298 ± 2	298 ± 2	298 ± 2
S_iO_2 (PECVD)	500	49 ± 2	49 ± 2	49 ± 2

Upon delivery of the wafers, we started the photolithography process. Prior to the application of the photoresist, we dried the wafers using a hot plate (Fig. 13) from Brewer Science for 1 minute at 100ºC in order to eliminate humidity. Since SiO_2 is hydrophilic and exhibits a poor affinity for the resin molecules of the photoresist, a primer layer using HexaMethylDiSilizane (HMDS) from Microchemicals GmbH was deposited on the surface, turning it into hydrophobic, and thus improving photoresist adhesion. Then we applied a high resolution (1µm) positive resist (AZ ECI3007) from Microchemicals GmbH using the spin coater LabSpin6 from Suss MicroTec GmbH at 5000rpm for 2 minutes (Fig. 13).

After spin-coating the photoresist, the film still has a high solvent-content, and therefore we proceeded to perform a soft-bake to dry it at 90ºC for 1 minute. The reduction of solvent concentration reduces contamination of the mask with resist, improves the resist adhesion to the substrate and increases its stability [11].

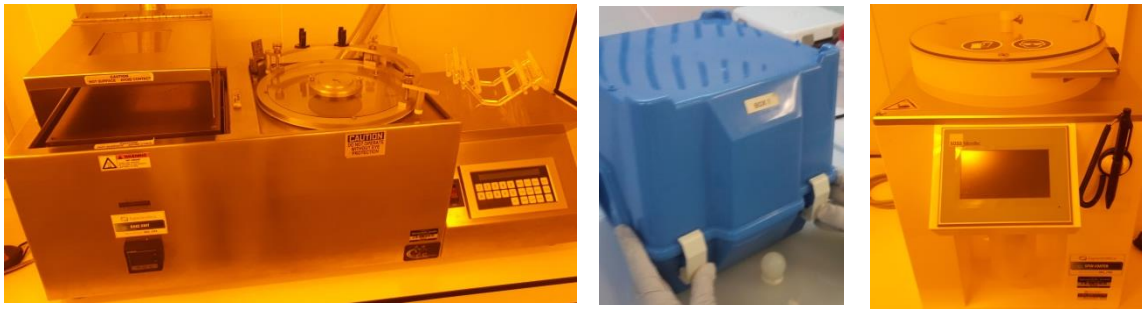

Fig. 13. Photographs of the hot plate (left), the deposition of the HMDS through its vapour on a closed box (centre) and the spin coater (right).

The next process step has consisted on the photoresist exposure through the mask with high-intensity ultraviolet light. We exposed the photoresist using the contact mask aligner from Tamarack Scientific, model M152 (Fig. 14), with an exposure energy of 55mJ/cm^2 for 1.6 seconds. Then, following the manufacturer recommendations from the photoresist AZ-ECI3007 that we used, a post exposure bake was performed in order to complete the photoreaction initiated during exposure.

Fig. 14. Mask aligner and exposer (left) and wafer with developed photoresist (right)

After the post exposure bake we developed the photoresist with the AZ 726 MIF developer from Microchemicals GmbH. For the first photolithography process run we developed the photoresist during 55 seconds. The developed photoresist lines can be observed visually in Fig. 14. For a better understanding of the photolithography process, the drawings of the wafer at each process step are shown on Fig. 15. After the photoresist development, the wafer would in the state of Fig. 15.d.

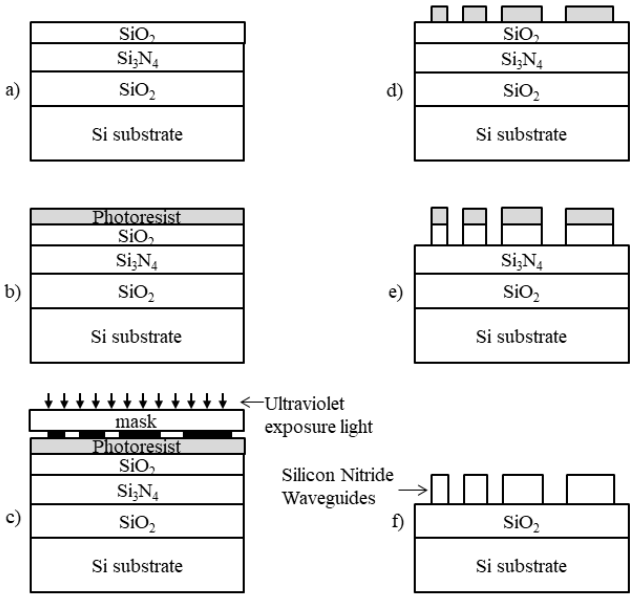

Fig. 15. Wafer drawings through the photolithographic process. (a) Silicon Nitride layer covered with S_iO_2 etching mask layer; (b) photoresist applied on the surface of the wafer; (c) mask alignment and exposure of the photoresist; (d) developed photoresist; (e) etching of the S_iO_2 barrier layer; (g) etched silicon nitride layer.

In the following, we proceed to start the etching steps of the barrier oxide and the silicon nitride. Our approach was to divide the wafer into different parts (Fig. 16), so as to perform a set of experiments in which different variables could be changed in the different steps, such as duration of the etching and temperature. Table 5 provides the values for each process step variable, and for the sections of the wafer. For this first photolithographic process run (Run1), the variables' values were chosen higher than the expected for the physical process to happen, and to be able then to optimize them in subsequent runs.

In order to etch the PECVD (Plasma Enhanced Chemical Vapour Deposition) silicon dioxide used as an etching barrier layer of the silicon nitride, we used buffered hydrofluoric acid (BOE 7:1). It shows an etching rate [12] of 490nm/min on annealed silicon dioxide and 240nm/min when annealing has been performed. Since the BOE does not etch the silicon nitride and its rate is very low for the unexposed resist areas [12] we performed a longer etching time for the 50nm silicon dioxide barrier layer, 120seconds. As a result of this step, a SiO_2 hard-mask to etch the Si_3N_4 has been created (Fig. 15.e).

Hence, once the SiO_2 is removed at the resist exposed areas, the next process step is the etching of the silicon nitride. We used phosphoric acid 85% at 120ºC and 180ºC during 5, 8, 23 and 30 minutes.

Table 5. Etch variables for the wafer from RUN1

Wafer section	Dev time (s)	BOE etch (s)	H3PO4 etch temp (ºC)	H3PO4 etch time(min)
1.1.2	55	no	no	no
1.2.1	55	120	120	5
1.2.2	55	120	120	8
1.3.1	55	120	180	23
1.3.2	55	120	180	30
1.3.3	55	120	180	38

The wafer section 1.1.2 was not etched to use it to observe the photoresist deposition process. A picture of the developed photoresist structure is shown on Fig. 16 (right), corresponding to line number 4 of the mask layout, obtained with the Scanning Electron Microscope (SEM) Ultra55 from Zeiss (Fig. 17).

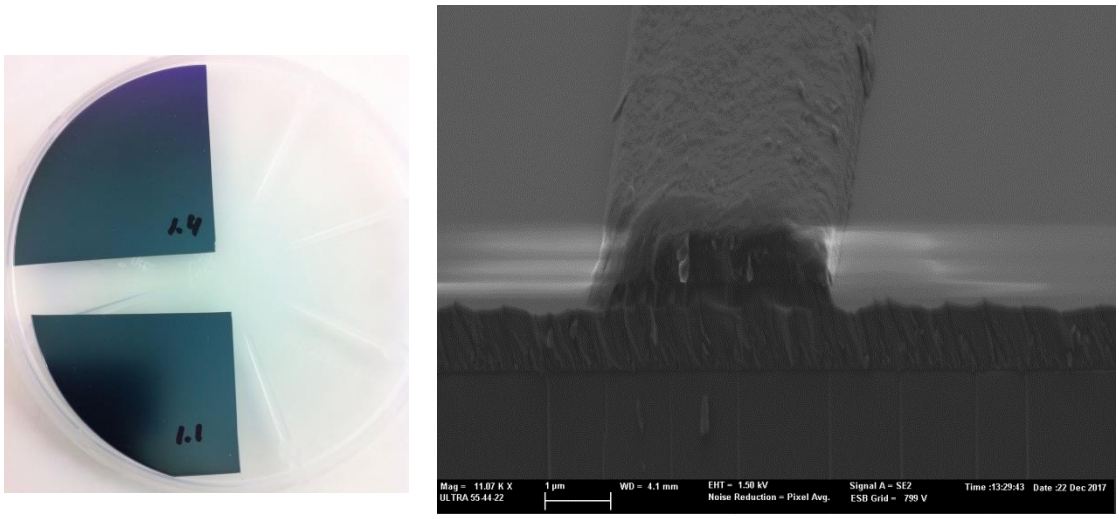

Fig. 16. Two wafer sections of the developed wafer (left) and developed photoresist structure corresponding to line number 4 (right).

Table 6 reports the thickness measurements of different silicon nitride structures after etching, obtained using the profilometer Dektak 150 from Veeco Instruments. The thickness measurements for the photoresist layer prior to the etchings are also shown and we can observe that the thinner line of 1µm is not appearing, probably because it has been overdeveloped. Line number 2 is neither appearing after the etching process for any variable combination because the overdevelopment of the photoresist structure has reduced its width and it has weakened in such a way that the over-etching of the silicon dioxide with BOE and the etching of the silicon dioxide has made it disappear. We will confirm this in the next photolithography run, whose results follow later in this chapter. The silicon dioxide structures from section samples 1.2.1 and

1.2.2 which have been etched for 5 and 8 minutes respectively at 120ºC show a thickness of 62 and 67µm, far away from the target thickness of 300nm, that means that the etching time and/or temperature have not been enough, then we have not completely removed the silicon nitride below the photoresist structures. The best result corresponds to the etching at 180ºC during 23 minutes since the obtained values are closer to the thickness of the silicon nitride layer, 300nm. From this etching time, the 30 and 38 minutes duration etched samples at the same temperature show a thickness decrease over time, since they are over-etched. The silicon dioxide etching protective layer has "finished" and the etching of the target silicon nitride structure has began on the top, decreasing its thickness.

Table 6. Thickness measurements (nm) from the photolithography process of Run 1.

Wafer section	**Line 1**	**Line 2**	**Line 3**	**Line 4**	**Line 5**	**Line 18**
1.1.2	x	443	468	485	490	505
1.2.1	x	x	63	62.5	62.6	62
1.2.2	x	x	65.5	67.6	67	64
1.3.1	x	x	213.3	308.8	305	305
1.3.2	x	x	265	266.3	270	255
1.3.3	x	x	180	194.6	188	170

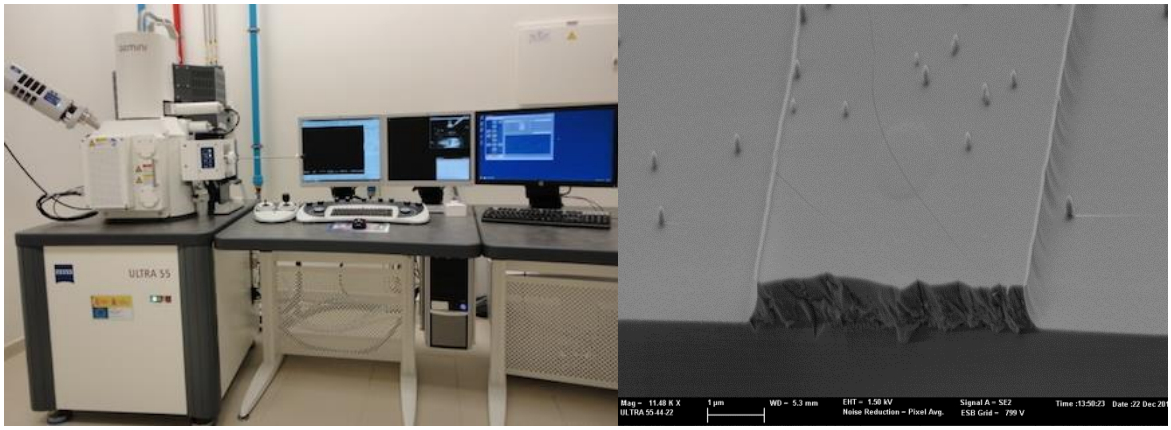

Fig. 17. Picture of the Scanning Electron Microscope (left) and silicon nitride waveguide obtained after the photolithography process (right).

After the first photolithographic run, we performed a second run following the same procedure and variables for the initial steps such as baking, deposition of the primer and photoresist, the exposure and the post exposure bake. In this run we reduced the photoresist development time to 30 seconds. As it can be observed in Fig. 18, now, **the thinnest photoresist structure of 1µm width has been resolved** after photoresist development reaching the resolution specification of the photoresist of 1µm.

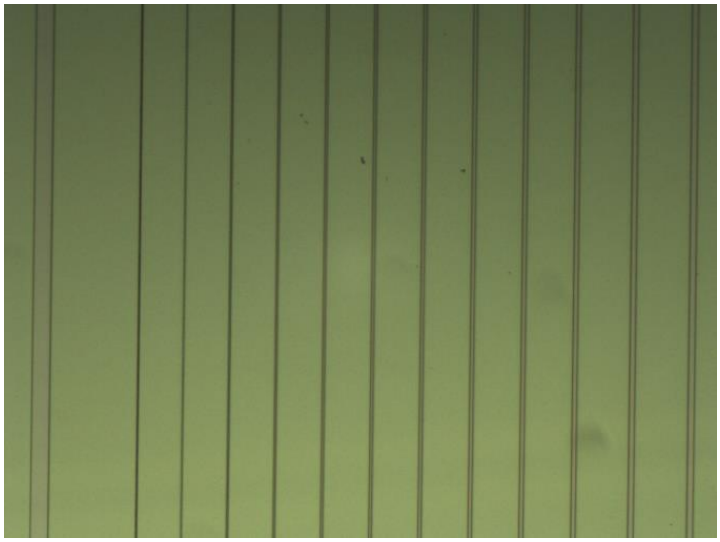

Fig. 18. Developed wafer including the thinnest photoresist structure of 1µm

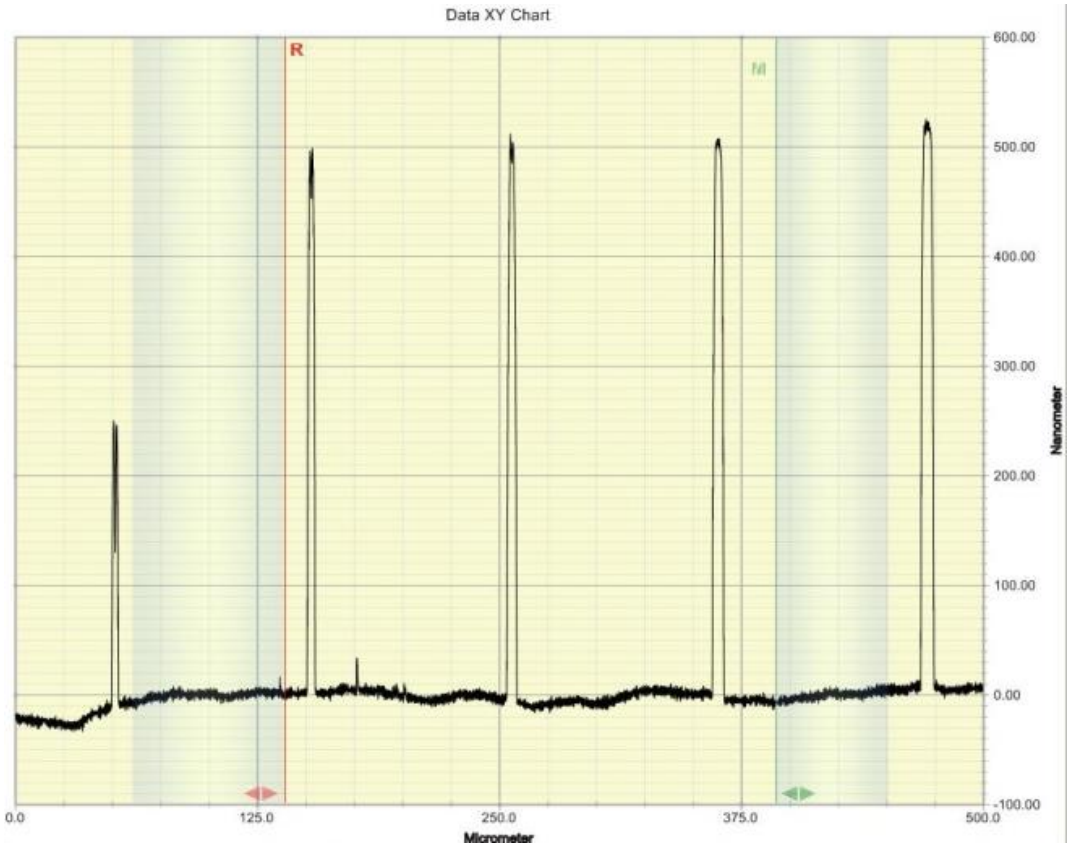

Fig. 19. Measurement of the photoresist structure thickness after its development.

Fig. 19 shows the thickness measurements of the photoresist, which is around 500nm for most of the lines, although line 1 presents a thickness of 250nm that means that the development time could even be reduced several seconds more.

We sectioned the developed wafer of Run2 into two parts where the etching time of the silicon dioxide barrier layer was reduced respect Run1 to 30 and 80 seconds to explore if lateral etch of the oxide below the unexposed lines is happening. The silicon nitride layer of each

sample was later etched with the phosphoric acid at 180ºC temperature for both samples during 21 minutes for sample 2.1 and 23 minutes for sample 2.2. Table 7 reports the thickness measurements of the Run2 photolithography process.

Table 7. Process variables and thickness measurements (nm) from Run2.

Wafer section	Photo-resist dev time (s)	BOE etch (s)	H3PO4 etch temp (ºC)	H3PO4 etch time(min)	Line 1	Line 2	Line 3	Line 4
+2.1	30	40	180	21	260	260	260	260
+2.2	30	80	180	23	120	120	120	120

From the observation of these results we can conclude that in both cases it has incurred on an over-etching since the height of the silicon nitride structure for the 21 minutes etching is 260nm, close to the target of 300nm and 120nm for the longer etching of 23 minutes. The silicon dioxide etching protective layer has "finished" in both cases and the etching of the target silicon nitride structure has begun on the top, decreasing its thickness.

In order to summarize and to compare the results from both runs, the process variables and results are shown in table 8.

Table 8. Summary of the experiments' variables and thickness measurements.

Wafer section	Photo-resist dev time (s)	BOE etch (s)	H3PO4 etch temp (ºC)	H3PO4 etch time(min)	Line 1	Line 2	Line 3	Line 4
1.3.1	55	120	180	23	-	-	213.3	308.8
2.1	30	40	180	21	260	260	260	260
2.2	30	80	180	23	120	120	120	120

1.3.1 is the reference experiment from Run 1 since in Line 4 and in the following lines we get close to the target nitride height (300 nm). But the aim is to have this height also in Line 1 and 2. Line 1 (1 micron width) is not resolved after the photo-resist development (disappears). Line 2 (2 microns width) is not resolved after H3PO4 etch. Hence, we decided (as explained above) to lower photo-resist development time and BOE etch time.

The reduction of the photoresist development time to 30 seconds in experiments of Run 2, 2.1 and 2.2, has led to resolve the 1 micron structure after silicon nitride etching.

The reduction of the silicon dioxide BOE etching time to 40 and 80 seconds for experiments 2.1 and 2.2 respectively, has led to more uniform thickness results since the BOE lateral over-

etching has been avoided, thus preventing the etching of the silicon nitride in the top of the structures.

However, there is apparently a contradiction in the thickness results between experiments 1.3.1 and 2.2, since the same etching time of the silicon nitride with phosphoric acid has been used for both of them. Although a BOE etching time of 120 seconds has been used for 1.3.1 and 80 seconds for 2.2, the thickness results for 1.3.1 are higher than for 2.2. This can be explained from the conclusions of reference [13] that indicates that the silicon nitride etching rate changes upon concentration of phosphoric acid. The boiling phosphoric acid loses water due to evaporation and the etching rate decreases since water is an activator of the chemical reactions as indicated in references [13] [14] [15]. In the experiments from Run2 we inserted the samples to be etched into the phosphoric acid sooner than in Run1, while the acid was still boiling obtaining a higher etching rate. Therefore, the experimental conditions among runs are not exactly the same, and we then attribute the aforementioned contradictions to these.

To control further the process, so as to enforce repeatability in the experiments, an etching system with reflux of the evaporated water into the acid is considered to be required, in order to keep constant the acid concentration and therefore the etching rate of the silicon nitride.

Finally, the results lead to indicate that a valid point for further investigation is experiment 2.1, where the nitride height resulting is 260 nm (close to the 300 nm nitride deposited layer height) and Line 1 is resolved. However, we decided to continue from this point once an etching system with reflux has been acquired.

4.2 CHAPTER CONCLUSIONS

Along the photolithography experiments performed in this section, we have been able:

- To reach the resolution specification of the photoresist which is 1 micron width.
- To obtain an approximation of the etching variables to fabricate the targeted silicon nitride structures of a height of 300nm.
- To understand the issues involving the etching of the silicon nitride, and to propose the means (etch equipment with reflux control) to continue research aimed at obtaining repeatable results.

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