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Empty substrate integrated waveguide technology for *E* plane high-frequency and high-performance circuits

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Key Points:
- First *E* plane device in empty substrate integrated waveguide
- Low reflection transition from microstrip to *E* plane empty substrate integrated waveguide
- High-performance and high-frequency phase shifter in *E* plane empty substrate integrated waveguide

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Abstract Substrate integrated circuits (SIC) have attracted much attention in the last years because of their great potential of low cost, easy manufacturing, integration in a circuit board, and higher-quality factor than planar circuits. A first suite of SIC where the waves propagate through dielectric have been first developed, based on the well-known substrate integrated waveguide (SIW) and related technological implementations. One step further has been made with a new suite of empty substrate integrated waveguides, where the waves propagate through air, thus reducing the associated losses. This is the case of the empty substrate integrated waveguide (ESIW) or the air-filled substrate integrated waveguide (air-filled SIW). However, all these SIC are *H* plane structures, so classical *H* plane solutions in rectangular waveguides have already been mapped to most of these new SIC. In this paper a novel *E* plane empty substrate integrated waveguide (ESIW-E) is presented. This structure allows to easily map classical *E* plane solutions in rectangular waveguide to this new substrate integrated solution. It is similar to the ESIW, although more layers are needed to build the structure. A wideband transition (covering the frequency range between 33 GHz and 50 GHz) from microstrip to ESIW-E is designed and manufactured. Measurements are successfully compared with simulation, proving the validity of this new SIC. A broadband high-frequency phase shifter (for operation from 35 GHz to 47 GHz) is successfully implemented in ESIW-E, thus proving the good performance of this new SIC in a practical application.

1. Introduction

Substrate integrated circuits (SIC) have attracted much attention in the last years because of their great potential. The first practical implementation of these circuits, the substrate integrated waveguide (SIW), was proposed by Deslandes and Wu in *Deslandes and Wu* [2001]. This is a waveguide integrated in a substrate where the lateral walls are synthesized with metallized via holes, and the upper and lower walls are the top and bottom metallization of the substrate.

Many other SIC have been developed since the appearance of the SIW. In the substrate integrated slab waveguide (SISW) *Deslandes et al.* [2003], the guide is synthesized on a substrate by cutting an air hole in the center of a SIW, and the frequency operating bandwidth is increased. The ridge substrate integrated waveguide (RSIW) *Li et al.* [2008] also increases the operation bandwidth by drilling cylindrical air holes in the middle of the SIW. The substrate integrated nonradiative dielectric waveguide (SINRD) *Cassivi and Wu* [2004] uses a specific pattern of air holes as lateral walls and creates a dielectric waveguide channel reducing the radiation losses with respect to the SIW. The half mode substrate integrated waveguide (HMSIW) *Hong et al.* [2006] reduces the size of the SIW to the half, by exploiting the fact that there is a symmetry plane along the propagation direction that is equivalent to a magnetic wall.

The advantage of this new concept of substrate integrated waveguide, when compared with classical planar circuits, is that it is low cost and easy to manufacture with standard printed circuit board (PCB) machinery. Moreover, it presents a higher-quality factor for resonators and filters. Many transitions have been developed from different planar lines (microstrip, coplanar, etc.) to each type of substrate integrated circuit. So the SIC can be embedded in a substrate and easily connected to other planar circuits. When compared to the classical rectangular waveguide, SIC present smaller quality factor and greater insertion losses, but their advantage is that they are low cost, low profile, and can be easily embedded in a PCB.

A full suite of microwave devices have been developed with SIC, e.g., filters *Pourghorban Saghati et al.* [2015]; *Le Coq et al.* [2015], couplers *Djerafi et al.* [2014]; *Chen et al.* [2006], phase shifters *Djerafi et al.* [2015], antennas *Tekkouk et al.* [2016]; *Tan et al.* [2015], and tunable devices *Entesari et al.* [2015]. All these devices prove the interesting characteristics of SIC for being used in the microwave industry. However, the presence of dielectric in these devices limits their performance especially at high frequencies, due to the losses in the substrate that significantly increase insertion losses and decrease the quality factor. In order to solve this problem, a new type of substrate integrated waveguides has appeared where the dielectric is removed, and the losses are decreased, while maintaining the advantages of low cost, low profile, easy manufacturing, and integration in a PCB.

The first one of these waveguides was the empty substrate integrated waveguide (ESIW) *Belenguer et al.* [2014]. In this case the substrate is emptied, metallized, and covered with two metallic layers, so a rectangular waveguide is synthesized within the substrate, and transitions are developed in order to connect to accessing microstrip lines. Coupled cavity filters with very high quality factors *Belenguer et al.* [2014], a calibration kit *Fernández Berlanga et al.* [2015], a horn antenna *Mateo et al.* [2016], and a hybrid directional coupler *Fernandez et al.* [2015] have already been manufactured in ESIW. The next empty SIC that appeared was the hollow substrate integrated waveguide (HSIW) *Jin et al.* [2014], which was manufactured in the low-temperature cofired ceramic (LTCC) technique. The lateral walls are metallized via holes, different from the metallic continuous walls of the ESIW. Consequently, the guided channel is not completely empty, and therefore, the losses are increased. Moreover, the HSIW is accessed with coaxial to rectangular waveguide transitions, so it is not fully integrated in a substrate. Another alternative is the air filled substrate integrated waveguide *Parment et al.* [2015a]. As the HSIW, the lateral walls are a row of metallized via holes in the main substrate. In this case the air filled SIW is manufactured with standard PCB substrate, and transitions are developed which connect the air filled SIW with accessing microstrip ports. A filter with inductive posts in this air filled SIW was presented in *Parment et al.* [2015b]. Finally, a dielectricless substrate integrated waveguide was presented in *Bigelli et al.* [2016]. This waveguide is completely dielectricless, as the ESIW, and assembles the layers using prepeg. The metallic contact is ensured through metallized via holes. The guide is accessed with a coaxial line, and no transition has yet been presented to connect it with planar lines.

All these SIC are waveguiding structures with invariant geometry in the vertical direction, that is, *H* plane structures, where only TE_{m0} modes are excited. There is a large collection of microwave devices that are implemented in classical rectangular waveguides with *H* plane geometry. These solutions can be easily mapped to any of the already mentioned SIC, as it has been demonstrated in many recent publications. However, there are many other classical devices in rectangular waveguides that require the geometry to be *E* plane, that is, invariant in the horizontal dimension, with the fundamental mode TE_{10} propagating and only TE_{1n} and TM_{1n} higher-order modes excited. That is the case, for example, of *E* plane bends and T junctions *Marcuvitz and Institution of Electrical Engineers* [1951]; *Montgomery et al.* [1948], *E* plane classical corrugated filters *Levy* [1973], *E* plane filters with continuously variating profile *Arregui et al.* [2010], *E* plane metal inserts filters *Vahldieck et al.* [1984], *E* plane ridge filters *Budimir* [1997]; *Rong et al.* [1999]; *Uher et al.* [1993], or the case of some *E* plane phase shifters for wideband applications, such as radio astronomy, where sensitivity of the receiver increases with the bandwidth *Tribak et al.* [2014]. So it would be interesting to extend the existing SIC to produce new ones which can easily map existing *E* plane solutions in classical rectangular waveguides.

In this paper the new ESIW is presented which can, at the expense of increasing the number of layers, implement *E* plane structures. This new ESIW has been called ESIW-E. It has the advantage of being an empty SIC, so it is low cost, integrated in a substrate, and, at the same time, low loss since the fields propagate through air and not through dielectric. And it can be used to easily map existing *E* plane solutions in rectangular waveguide.

Section 2 details the structure of the new proposed ESIW-E, the PCB used for its construction, and the transition that has been designed in order to integrate the ESIW-E in a substrate and connect it to accessing microstrip lines. Next, section 3 shows the manufactured back to back transition, and measurements are successfully compared with simulated results. Finally, in section 4, the broadband phase shifter solution of *Tribak et al.* [2014] for rectangular waveguide has been translated to ESIW-E, with the aim of integrating this high-frequency and high-performance phase shifter into a SIC. Measurements are shown that well prove the potential of the new ESIW-E.

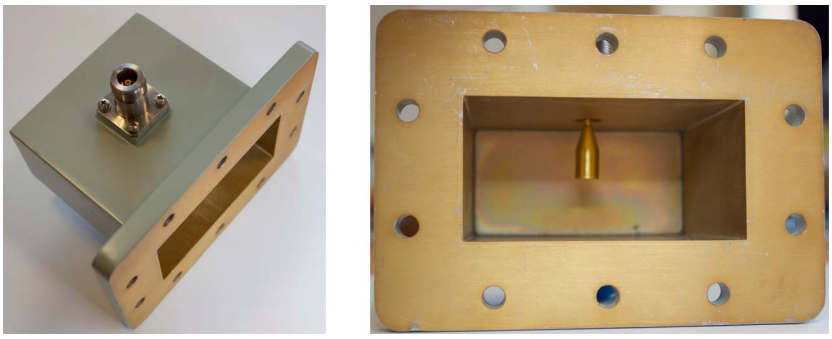


Figure 1. Commercial waveguide launcher incorporating a wideband coaxial to waveguide transition.

2. Design of the Transition From Microstrip to ESIW-E

The proposed structure for the transition from microstrip to ESIW-E is inspired in the typical solution for the transition from coaxial line to rectangular waveguide, usually known as "launcher." In this transition the waveguide is short circuited in one of its ends and, approximately at $\lambda/4$ from the short circuit, the inner conductor of the coaxial line is inserted through a hole mechanized in the upper wall of the waveguide. The external conductor of the coaxial is connected to the waveguide. In order to increase the bandwidth of the transition, the geometry of the inner conductor of the coaxial is properly modified. An example of this type of transition is shown in Figure 1. In this case the width of the inner conductor is increased inside the waveguide by means of a conical taper. The inner conductor reaches approximately to the middle of the waveguide.

As already mentioned, the transition from coaxial to rectangular waveguide will inspire the transition to ESIW-E. In order to build a planar line, using standard planar circuit boards (PCB), as similar as possible to a coaxial line, two PCB are used. In both PCB a microstrip line is milled of the same width on one side of the PCB. And two lines of via holes are drilled and metallized at both sides of the milled strip, at a certain distance. Then both PCB are put together in such a way that the two milled strips are put one in front of the other. The resulting geometry, depicted in Figure 2c, is similar to a stripline but with lateral via holes that can be considered as continuous conducting walls and with a thin air layer of the same width as that of the two milled

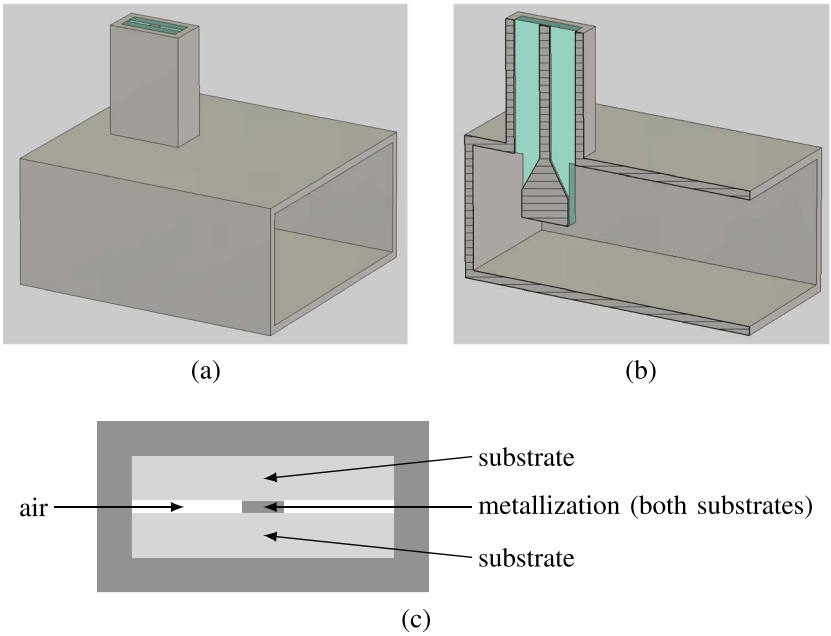
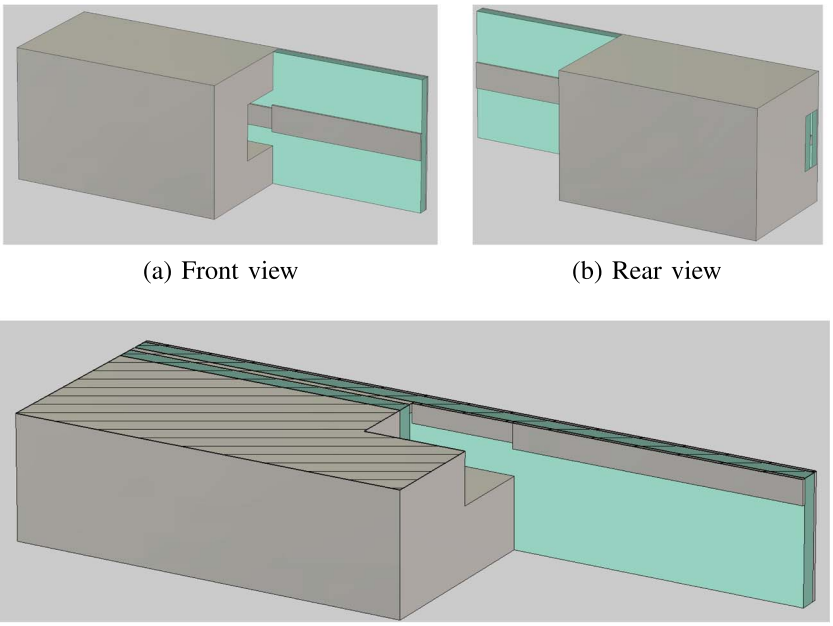


Figure 2. Pseudostripline to rectangular waveguide transition. (a) Perspective of the whole transition. (b) Cut of the transition along the waveguide axes (*E* plane). (c) Cross section of the pseudostripline.



(a) Front view (b) Rear view

(c) Longitudinal cut

Figure 3. Different views of the microstrip to pseudostripline transition. The transition consists of three differentiated stages: the microstrip feeding, an intermediate enclosed microstrip which facilitates the transition to the last stage, and, finally, the pseudostripline output.

strips that have been put together. The resulting structure, which we will call pseudostripline, is very similar to a rectangular coaxial line and has been obtained with standard planar technology.

The ESIW-E will be excited with this pseudostripline, as shown in Figures 2a and 2b. The inner conductor of the pseudostripline is inserted in the ESIW by enlarging and introducing both PCB inside the ESIW. And in order to increase the bandwidth, the width of the inner conductor is increased by means of a linear taper (equivalent to the conical taper in the coaxial) and will reach approximately to the middle of the ESIW.

In order to access the structure with a microstrip line, it is necessary to include a transition from pseudostripline to microstrip. Although both lines could be directly connected, it has been proven that a direct connection does not work properly and produces a high level of reflection. So an intermediate step between the pseudostripline and the microstip line has to be added, which consists on a microstrip line with a metallic enclosure (see Figure 3).

The overall transition from microstrip to ESIW-E will be, therefore, the cascading of the microstrip to pseudostripline transition and the pseudostripline to ESIW-E transition. In order to manufacture this structure with PCB, eight PCB must be used and piled up as shown in Figure 4. As it can be observed, the pseudostripline is formed by the *top central* and *bottom central* PCB. It is convenient that the exciting line is completely symmetric, since symmetry improves impedance matching and increases bandwidth. That is why exciting with the pseudostripline is better than doing it directly with the microstrip line. So in order to preserve the symmetry, the height of the PCB on top and bottom of the central PCB are symmetric. For enclosing the microstrip with metallic enclosure the *top intermediate* and *top layer* PCB have been used, mechanizing a rectangular hole of the adequate dimensions in the *top intermediate* layer. In order to preserve the symmetry, two inferior PCB have also been used (*bottom intermediate* and *bottom layer*). Finally, the structure is closed with the *top cover* and *bottom cover* PCB. The lateral walls of the pseudostripline and the microstrip line with enclosure are synthesized with rows of metallized via holes, as has already been mentioned.

The top and bottom view of the bottom central PCB is shown in Figure 5. In this figure, the dimensions of the different elements that integrate this layer are depicted. There are two semicircular holes at both sides of the element that is inserted in the guide. These holes cannot be avoided if a drilling machine is used, and their diameter is the diameter of the drill bit (d_{cut}). These mechanization defects can be avoided if a laser machine is used to cut the substrate. These holes are important because they are in a place where the field intensity

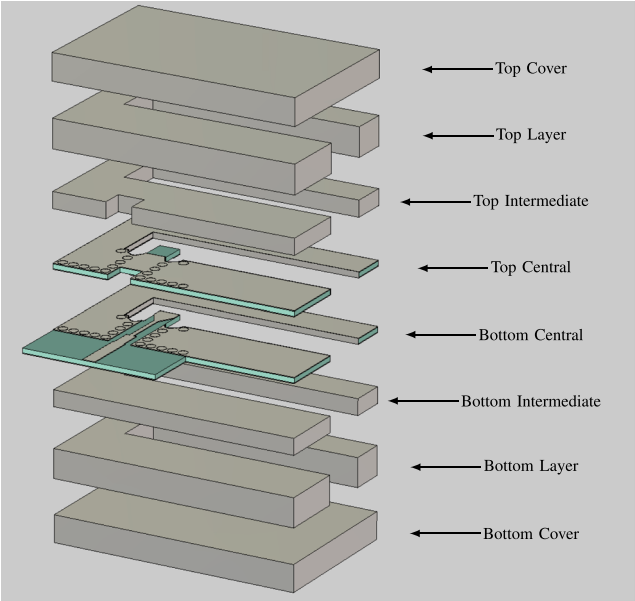


Figure 4. Definitive PCB stack up that has been used to build the ESIW-E and its transition to microstrip.

is high, so they affect the performance of the transitions, and must be taken into account if a drilling machine is used. Similar defects appear in form of rounded corners in the short circuit of the guide, but these defects can be neglected since they are in a place with low levels of field intensity.

Figure 6 shows the top and bottom view of the top central PCB. The dimensions of the elements of this layer are depicted.

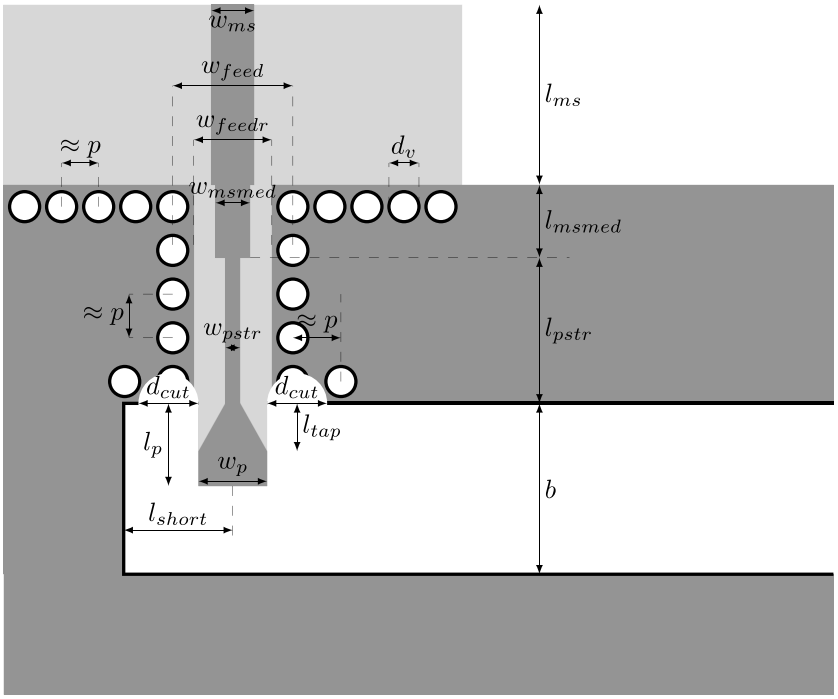
The rest of the PCB is much simpler. Figure 7 shows bottom view (top view is very similar, so it is not included for conciseness) of the top layer, bottom intermediate, and bottom layer PCB, and Figure 8 shows the bottom view of the top intermediate PCB, in which a square gap has been mechanized in order to form the microstrip with enclosure.

2.1. Design Process

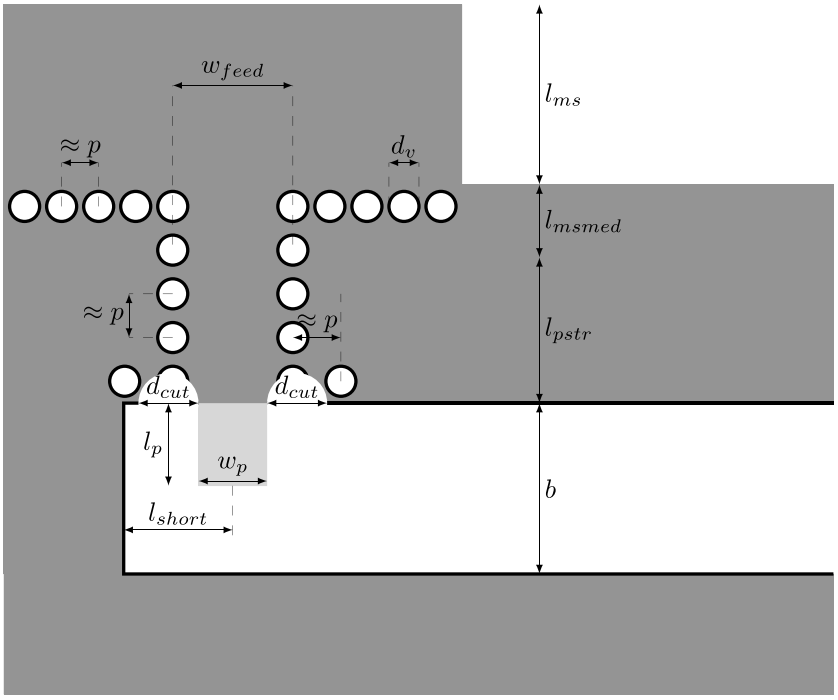
In order to design this structure, the first decision is the selection of the PCB that is going to be used for each layer. Taking into account the operating frequency, the height of the two central PCB are chosen small enough to guarantee that the radiation level of the microstrip line is kept sufficiently low. Next, the height of the remaining PCB is chosen so that the overall height of all the PCB (except the top and bottom cover) is as close as possible to the ideal value of the desired waveguide width a.

Next step is to design the transition from pseudostripline to rectangular waveguide. The following steps are followed:

1. The pseudostripline is designed in order to obtain the same impedance of the microstrip line (i.e., 50Ω). To that purpose, the value of w_{feedr} (see Figure 5) is first chosen so that there is only one propagating mode in the pseudostripline. Then the value of w_{pstr} is optimized in order to obtain the desired impedance.
2. The simplified transition from pseudostripline to rectangular waveguide of Figure 2 is modeled in a full-wave simulator. We have used the *Computer Simulation Technology* (CST) simulator [*Computer Simulation Technology*, 2016]. For the rectangular waveguide, the width a depends on the selection of the PCB, and the height b can be chosen freely. The dimensions of the pseudostripline have already been determined in the former step. For the rest of the parameters, the following initial values will be used: $w_p = w_{\text{feedr}}$, $l_{\text{short}} = \lambda_g/4$, $l_p = b/2$ and $l_{\text{tap}} = b/4$ (see Figure 5).
3. The structure is optimized for w_p, l_{short}, l_p, and l_{tap}, the optimization goal being the maximization of the return losses in the whole frequency band of interest.

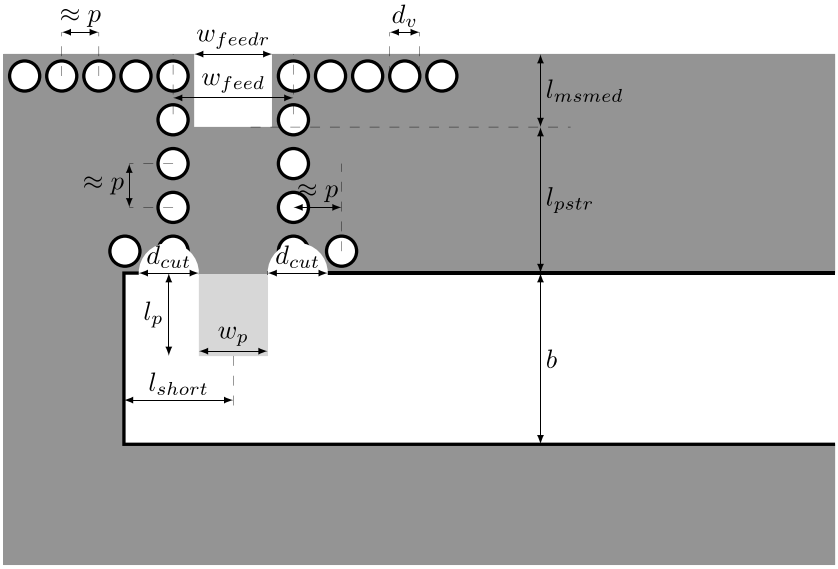


(a) Top view

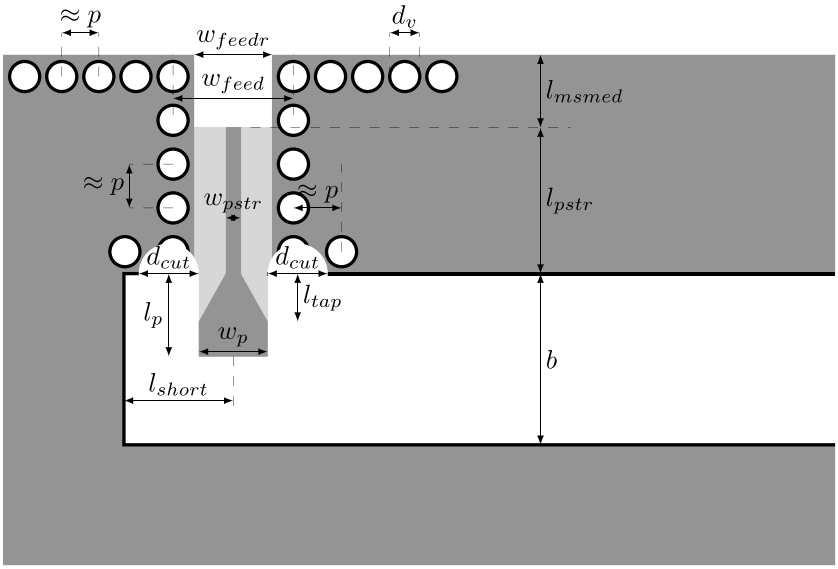


(b) Bottom view

Figure 5. Microstrip to ESIW-E transition in the bottom central PCB. Dark gray is metal covering the substrate. White represents holes emptied in the substrate. Light gray stands for substrate without metallic cover. Black line represents the metallization along substrate edges.



(a) Top view



(b) Bottom view

Figure 6. Microstrip to ESIW-E transition in the top central PCB. Dark gray is metal covering the substrate. White represents holes emptied in the substrate. Light gray stands for substrate without metallic cover. Black line represents the metallization along substrate edges.

The next step is to design the transition from microstrip to pseudostripline, with the following procedure:

1. The microstip is designed to obtain the desired impedance (the same one as the impedance of the pseudostripline).
2. The microstip with metallic enclosure is designed to have the same impedance than the microstrip.
3. The simplified transition from microstrip to pseudostripline of Figure 3 is modeled with the full-wave simulator. For the length of the microstrip with metallic enclosure, l_{msmed}, an initial value of $\lambda_{msmed}/2$ is used, where λ_{msmed} is the wavelength in the line at the central frequency of the band of interest.
4. The structure is optimized for w_{msmed} so that the return losses are maximized in the whole frequency band of interest.

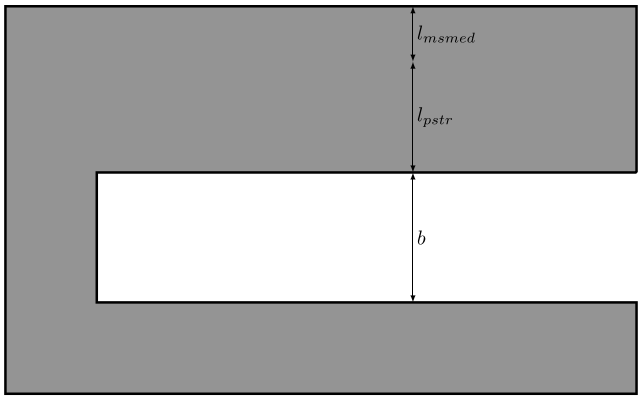


Figure 7. Bottom view of the top layer, bottom intermediate, and bottom layer PCB. Dark gray is metal covering the substrate. Black line represents the metallization along substrate edges.

The last step consists on the analysis of the whole structure with the full-wave simulator, considering a realistic and complete model that includes metallized via holes, and layered structure. The design is finished with the following actions:

1. The initial value of l_{pstr} is calculated. This value must be larger than $2\lambda_{pstr}$, where λ_{pstr} is the wavelength of the pseudostripline at the central frequency. A large value is chosen in order to avoid a strong coupling among the two transitions that have been designed separately.
2. The structure is optimized for l_{pstr}, l_{msmed}, l_{short}, l_p, w_{msmed}, and w_p for maximizing the return losses in the whole frequency band.

Following this design process a transition operating in the band from 33 to 50 GHz has been designed. For the top central and bottom central PCB two Rogers 3003 substrates of 0.254 mm height and 17 μm of copper have been chosen. For the top intermediate and bottom intermediate PCB two FR4 substrates of 0.794 mm height and 35 μm of copper metallization have been chosen and for the top layer and bottom layer PCB another two FR4 substrates but this time with a height of 1.5 mm (and 35 μm of metallization). All the PCB must be metallized with electrodeposition after being drilled, so an additional metallization has been added to all layers (except top and bottom cover that are not drilled or cut). The width of the metallization depends on the metallization time, which is related to each substrate height (estimated width of metallization is 10 μm for top central and bottom central PCB and 20 μm for the other PCB). The characteristics of all these PCB are summarized in Table 1. With these PCB and metallization widths, the total width of the synthesized rectangular waveguide is $a = 5.66$ mm, which is appropriate for working from 33 to 50 GHz. The optimized dimensions for this transition are listed in Table 2.

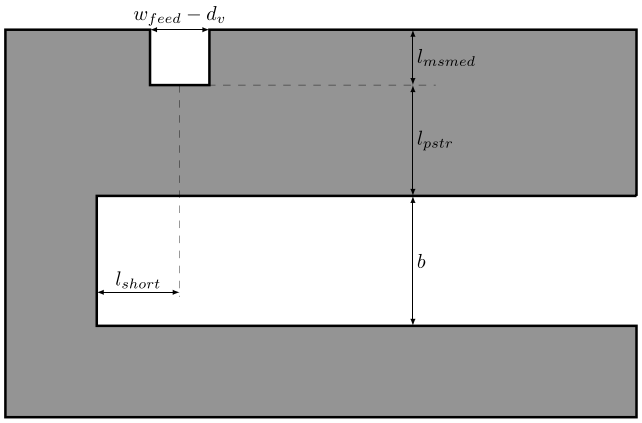


Figure 8. Bottom view of the top intermediate PCB. Dark gray is metal covering the substrate. Black line represents the metallization along substrate edges.

Table 1. Characteristics of All the PCB Used for the Design and Manufacturing of the Back-to-Back Transition[a]

Layer	h	t_1	t_2	h_t	PCB Name
Top cover	1.5	0.035	0	1.57	FR4
Top layer	1.5	0.035	0.020	1.614	FR4
Top intermediate	0.794	0.035	0.020	0.908	FR4
Top central	0.254	0.017	0.010	0.308	RO3003
Bottom central	0.254	0.017	0.010	0.308	RO3003
Bottom intermediate	0.794	0.035	0.020	0.908	FR4
Bottom layer	1.5	0.035	0.020	1.614	FR4
Bottom cover	1.5	0.035	0	1.57	FR4

[a] h is the substrate height, t_1 is the thickness of the substrate metallic layer, t_2 is thickness of the electrodeposited metallic layer, and $h_t = h + 2t_1 + 2t_2$ is the total height of the layer. All dimensions are in millimeters.

3. Manufactured Back-to-Back transition

The prototype was manufactured in the facilities of the University of Cantabria, Spain. Figures 9 and 10 were drawn in Autodesk Inventor and show the different layers needed for the manufacture of the prototype (schematic view with the names of all the layers in Figure 9 and 3-D virtual view of the assembled structure with external dimensions in Figure 10). As it can be seen in Figure 10, commercial coplanar to microstrip transitions have been added. These transitions are necessary because the circuit is going to be measured in a coplanar probe station. Due to the characteristics of the probe station, the maximum separation between the two accessing ports is 17 mm, so a separation of 15 mm has been chosen (see Figure 11). In Figure 11 the two microstrip accessing ports have been simulated on the same side for ease of simulation, although when manufacturing, they have been put on opposite sides, as shown in Figure 10, which is more convenient for measuring the prototype.

As already mentioned, for the top central and bottom central PCB, the Rogers RO3003 substrate ($h = 0.254$ mm, $t_1 = 17\mu$m) was used (see Table 1). The substrate has been emptied and drilled with a high precision laser machine, which provides high accurate results and minimum radii in the corners. For the remaining PCB (FR4 substrates with adequate heights as to obtain the desired width of the ESIW) a drilling machine has been used instead of the laser machine, since the manufacturing precision for these layers is not so critical. A drill bit of 1 mm diameter has been used. All layers except the top cover and bottom cover PCB have been metallized with a copper electrolytic bath. It is assumed that the width of the electrodeposited metallic layer is 20μm, according to previous experience. The measured dimension b of the ESIW is $b = 2.82$ mm.

The PCB have been fixed together using thin tin soldering paste (97SC alloy formed by 96.5% tin, 0.5% copper, and 3% silver). Figure 12 shows the top view of a PCB with a thin bath of soldering paste. When all the PCB have been bathed with the soldering paste, they are piled up and the soldering paste is dried in a reflow oven.

Figure 13 shows the top view of three PCB of the manufactured prototype before being assembled (already cut, metallized, and milled). Figure 13a shows the top view of the bottom central PCB. As it can be observed, this PCB has been cut using a laser machine, so the corners are almost perfectly square. This means that the holes of diameter d_{cut} of Figure 6 do not appear in this prototype, and this has to be taken into account in the simulation with CST (see Figure 14).

Table 2. Optimized Dimensions for the Designed Transition[a]

$w_{ms} = 0.715$	$w_{feedr} = 1.3$	$w_{feed} = 2$	$d_v = 0.5$
$w_{msmed} = 0.578$	$w_{pstr} = 0.247$	$w_p = 1.142$	$l_{short} = 1.816$
$d_{cut} = 1$	$p = 0.7$	$l_p = 1.376$	$l_{tap} = 0.797$
$l_{ms} = 3$	$l_{msmed} = 1.213$	$l_{pstr} = 2.246$	$b = 2.845$

[a] All dimensions are in millimeters.

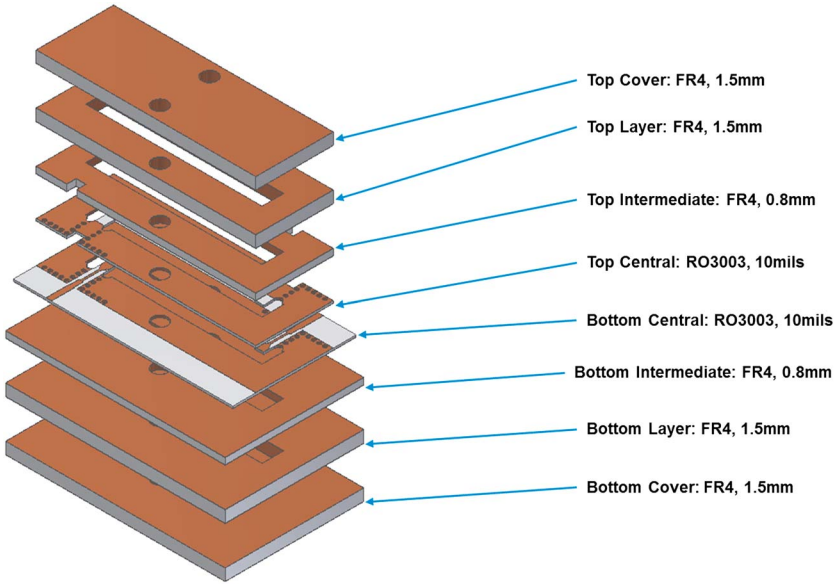


Figure 9. Layout of the PCB used for the manufacturing of the back-to-back transition.

Figure 13b shows the top view of the top intermediate PCB. This PCB is thicker, and its dimensions are not so critical for the performance of the structure as the top and bottom central PCB, so it has not been cut with the laser machine, and a drill machine has been used instead. The diameter of the drill bit is 1 mm, so rounded corners of radius 0.5 mm can be observed in this PCB. These rounded corners need also to be considered in the CST model (see Figure 14).

Finally, Figure 13c shows the top view of the top layer PCB. This layer has also been drilled with a drill machine, and again rounded corners of 0.5 mm of radius can be observed. It can also be observed the greater height of this PCB.

The top layer and top intermediate PCB have been metallized externally to avoid surface waves of the microstrip line to enter into the substrate of these layers, being guided through it, and eventually producing an interfering output signal on the microstrip of the other accessing port.

Figure 15 shows a perspective view of the prototype after all the PCB have been assembled. Great care has been taken to ensure that all layers are well aligned and that there is no soldering paste inside the waveguide. Misalignment could significantly degrade the performance of the device, to an extent that may depend on the type of device. In any case, it would degrade the performance of the transition from microstrip to ESIW, reducing the matching and increasing the return losses. In order to avoid these effects, and to ensure a correct alignment, all layers are mechanized with two holes (see Figure 9) and piled together using two alignment dowel pins and tin soldering paste. After the soldering paste is dried in a reflow oven, the alignment dowel

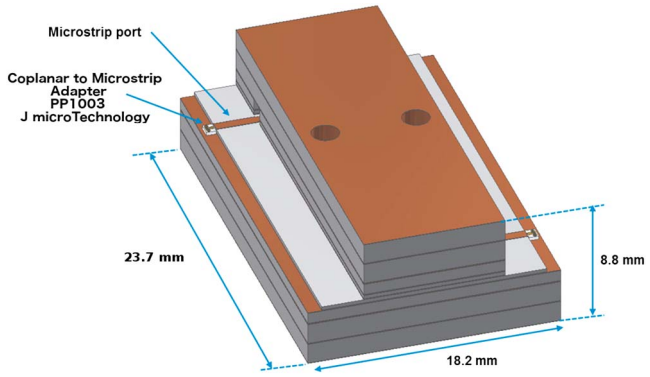


Figure 10. A 3-D model of the back-to-back transition with external dimensions.

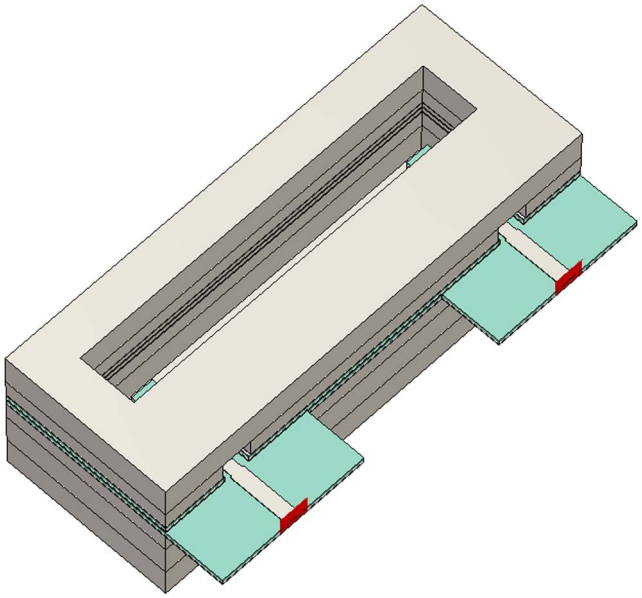


Figure 11. A 3-D model of the back to back transition simulated in CST. Separation between microstrip ports is 15 mm.

pins can be removed (see Figure 15). Figure 16 shows a lateral view of the assembled prototype, where all the PCB piled together can be observed in detail. The width of the synthesized waveguide (ESIW) has been measured, and the total width is 5.6 mm, very close to the ideal value.

The measurement of the structure was performed in a small probe station equipped with coplanar probes of the company PicoProbe (see Figure 17). Commercial adapters from coplanar to microstrip lines of the J microTechnology company *JMicroTechnology* [2016] were used, with reference PP1003 (see Figure 18a). These adapters are connected to the microstrip lines of the prototype using golden strips with tapered shape. This method has proven to give better results than the use of bonding wires. The effect of the adapters can be de-embeded from the measurements with the help of the calibration substrate provided by the company. However, the effect of the golden tapered strips persists. Since this effect cannot be de-embeded, the adapter and the tapered strips have been modeled with the CST full-wave commercial simulator and taken into account in the simulated results (see Figure 18b). The measured physical dimensions of the golden tapered strip shown in Figure 18a have been used for the CST model. Since the coplanar to microstrip adapters are de-embeded from the measurements, in the CST model the reference planes are shifted as shown in

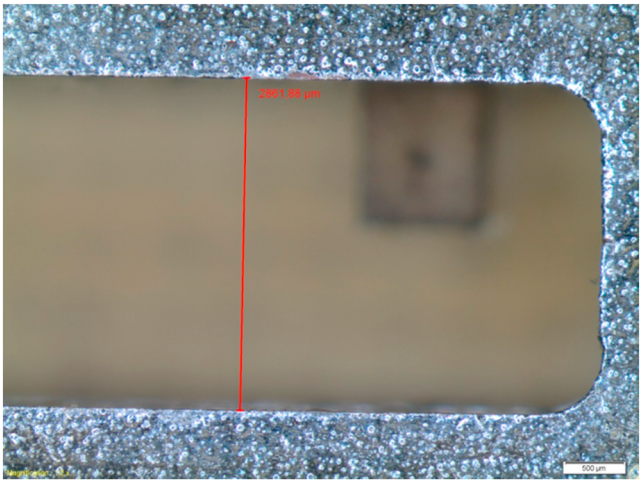
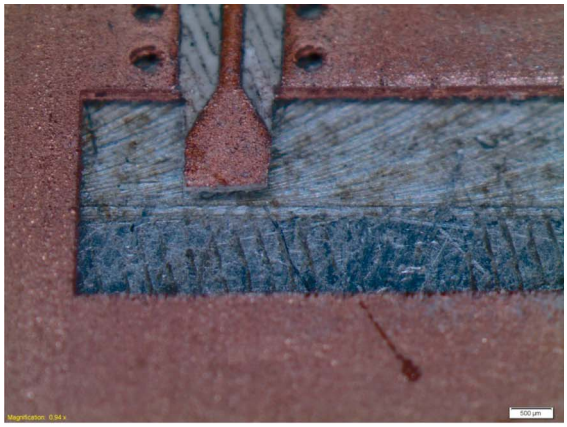
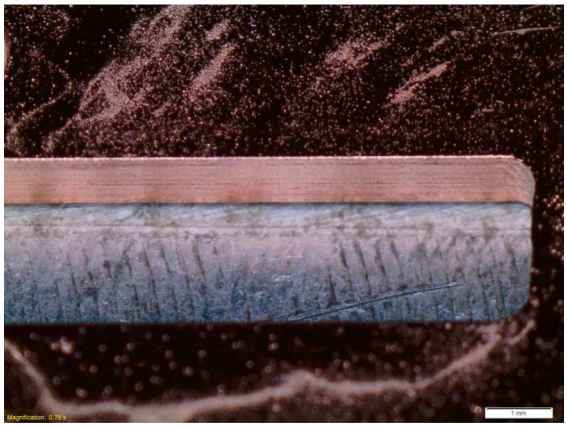


Figure 12. Top view of one PCB with a thin bath of soldering paste.



(a) Bottom central

(b) Top intermediate



(c) Top layer

Figure 13. Perspective view of different PCB of the manufactured prototype.

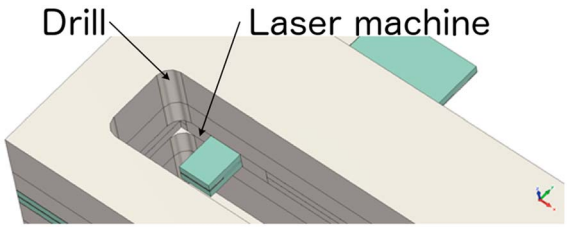


Figure 14. Perspective view of the CST model. Rounded corners have been considered for the drilled PCB, and square corners for the central PCB have been manufactured with a laser machine.

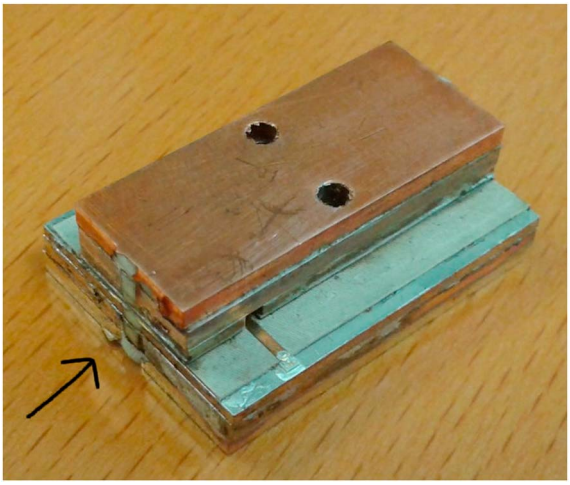


Figure 15. Perspective view of the manufactured back-to-back transition with all the PCB assembled.

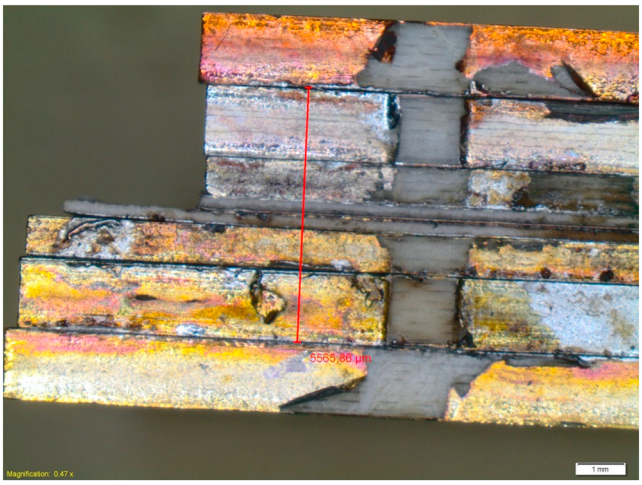


Figure 16. Front view of the assembled back-to-back transition. Point of view is marked with an arrow in Figure 15. The measured width of the ESIW is 5.6 mm.

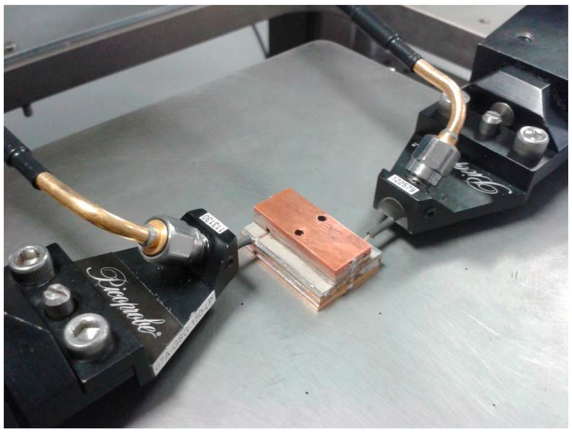
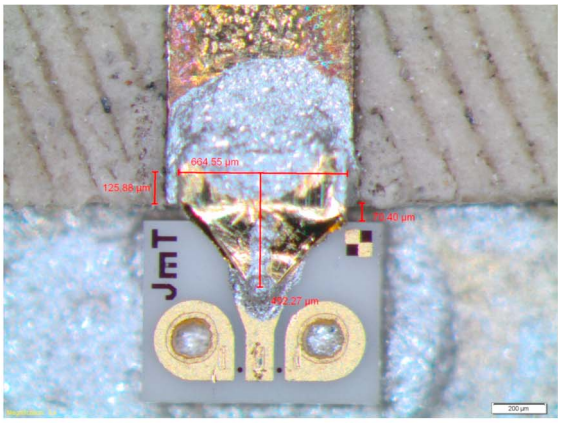
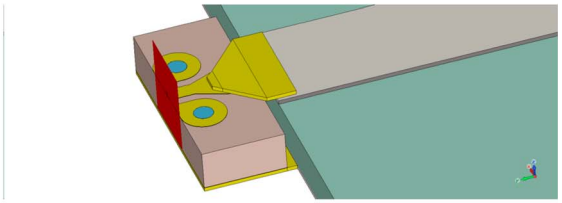


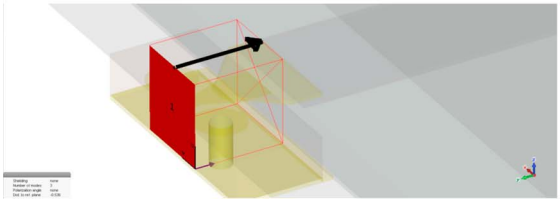
Figure 17. Measurement setup.



(a) J microTecnology adapter



(b) CST model



(c) Shifting of the reference plane

Figure 18. Coplanar to microstrip adapter PP1003 from J microTechnology.

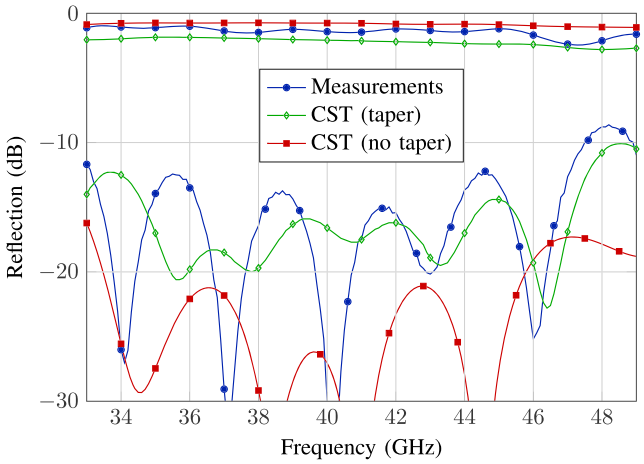


Figure 19. Simulation and measurements for the back-to-back transition of Figure 11.

Figure 18c, so that these adapters are also de-embeded from the simulation, and only the tapered strips are considered both in measurements and in simulation.

An Agilent Technologies network analyzer, model E8364A, was used for the measurements, which are compared with simulations in Figure 19. First, the commercial software CST has been used for simulating the whole structure without the golden tapered transitions of Figure 18. A conductivity of 10^7 S/m has been used to model the conducting surfaces, according to the predicted conductivity of an electrodeposited copper surface with roughness of 19 μm at the operating frequency [see *Chen*, 2007]. This gives an idea of the performance that can be achieved with the ESIW-E. It can be observed that these simulations predict return losses of over 20 dB and insertion losses lower than 1 dB in almost all of the recommended frequency band of operation for the WR22 (from 33 GHz to 49 GHz), which is the rectangular waveguide with the same width as the ESIW-E used for manufacturing this prototype. This proves the validity of the ESIW-E for the implementation of high-performance and high-frequency microwave circuits. This simulated results cannot be directly compared against measurements because the golden tapered transitions cannot be de-embeded from the measurements, as has already been discussed. Therefore, the measurements are compared in Figure 19 with the CST simulation including the golden tapered transition. It can be observed that there is a good agreement between simulation and measurements, which validates the design and the manufacturing process and proves that the performance is worsened as a consequence of the tapered transition. The measured insertion losses are slightly smaller than in simulation. This is probably due to the value of the conductivity that has been used, which was probably smaller than the real conductivity.

4. 90° ESIW-E Phase Shifter

E plane phase shifters for wide band applications and high frequency, such as radio astronomy, where sensitivity of the receiver increases with the bandwidth, are difficult to implement with *H* plane structures.

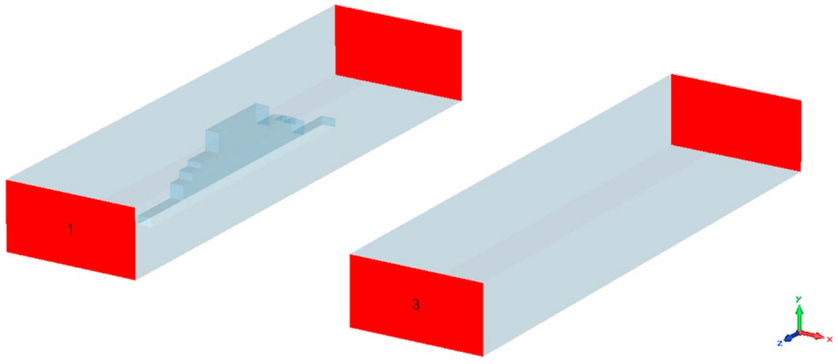


Figure 20. Schematic view of the CST model of the phase shifter and its reference line in a traditional WR-22 waveguide.

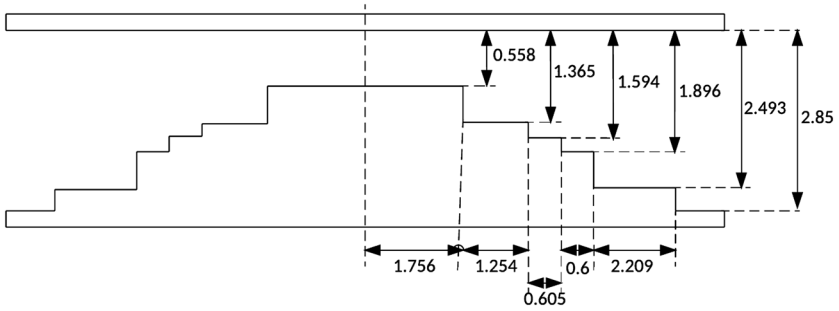
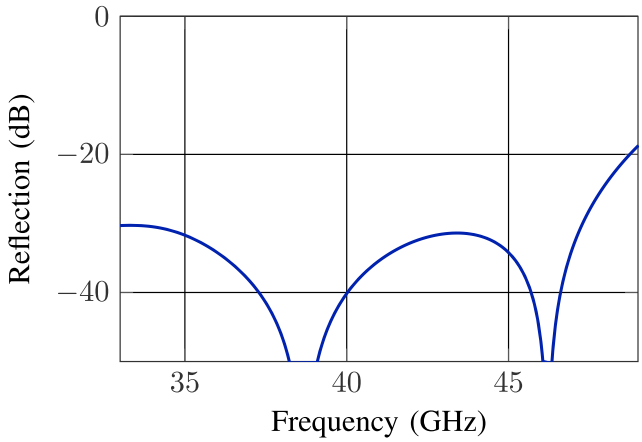
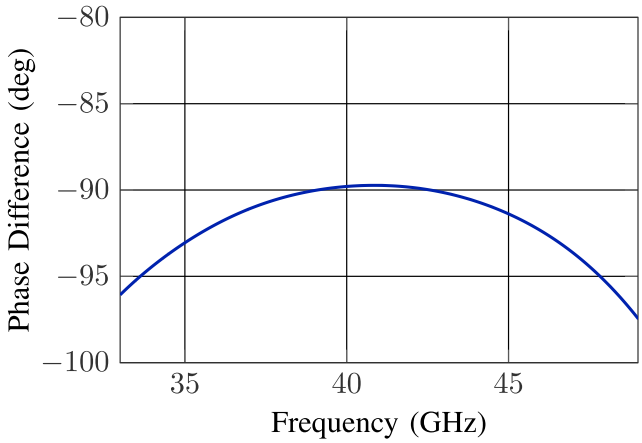


Figure 21. Dimensions of the designed phase shifter. The width of the ridge is $w = 0.6$ mm.

In *Xu et al.* [2005], *Moldovan et al.* [2006], and *Cheng et al.* [2007] SIW phase shifters are presented, but the bandwidth is not very large. The same occurs for the HSIW presented in *Chen et al.* [2007]. A broadband SIW phase shifter is presented in *Cheng et al.* [2010], but at the expense of presenting a physical length larger than that of the reference line. With the same physical length the phase shifter is narrow band. A broadband SIW phase shifter loaded with circular rods has been recently presented in *Djerafi et al.* [2015]. However, this solution would be difficult to implement for higher-frequency bands, where the required diameter of the rods would



(a) Reflection



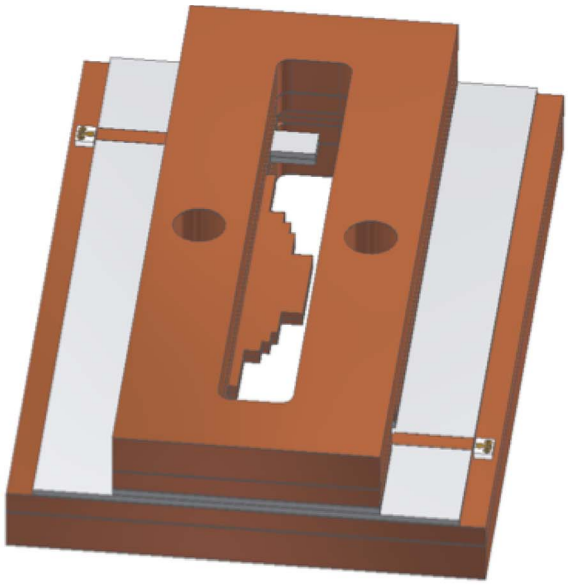
(b) Phase Difference

Figure 22. CST simulation of the ridge phase shifter of Figure 20.

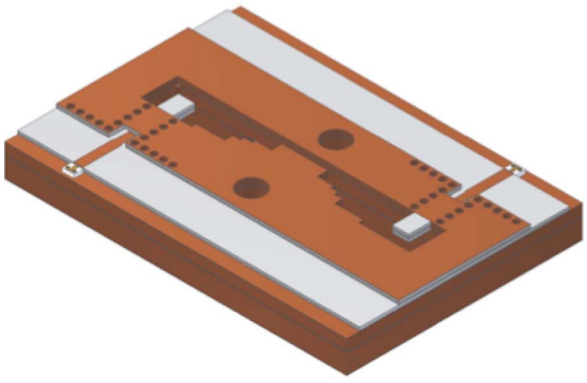
Table 3. Characteristics of All the PCB Used for the Manufacture of the Phase Shifter[a]

Layer	h	t_1	t_2	h_t	PCB Name
Top cover	1.524	0.035	0.010	1.614	RO4003C
Top layer	1.524	0.035	0.010	1.614	RO4003C
Top intermediate	0.813	0.035	0.010	0.903	RO4003C
Top central	0.254	0.017	0.006	0.3	RO3003
Bottom central	0.254	0.017	0.006	0.3	RO3003
Bottom intermediate	0.813	0.035	0.010	0.903	RO4003C
Bottom layer	1.524	0.035	0.010	1.614	RO4003C
Bottom cover	1.524	0.035	0.010	1.614	RO4003C

[a] h is the substrate height, t_1 is the thickness of the substrate metallic layer, t_2 is thickness of the electrodeposited metallic layer, and $h_t = h + 2t_1 + 2t_2$ is the total height of the layer. All dimensions are in millimeter.



(a) Without *top cover* PCB



(b) Without *top cover*, *top layer* and *top intermediate* PCB

Figure 23. Schematic views of the ESIW-E phase shifter.

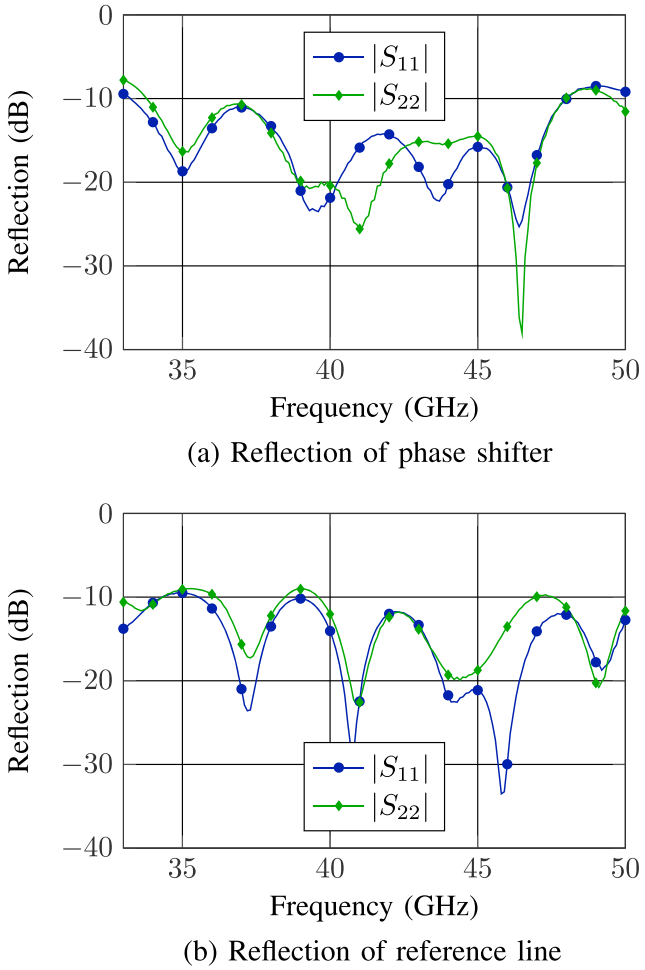


Figure 24. Measured reflections of the ESIW-E phase shifter and the reference line.

be too small. Besides, phase shifters in SIW or HSIW technology present high levels of insertion loss due to the presence of the dielectric. In ESIW-E, insertion losses will be smaller because the waves propagate through the air.

In order to test the performance of the ESIW-E for the implementation of high-frequency and high-performance microwave devices, a 90° phase shifter operating in the Q band (from 35 to 47 GHz) has been designed and manufactured.

The phase shifter provides a fixed phase shift, in this case 90°, with respect to a reference line. Therefore, two circuits must be manufactured, the phase shifter and the reference line.

The topology selected for the phase shifter is a traditional phase shifter in a ridge waveguide, where the waveguide is the ESIW-E and the ridge is manufactured using the two central PCB. Therefore, the width of the ridge is fixed by the height of these two central PCB ($w = 0.6$ mm).

Figure 20 shows the CST model of the phase shifter and its reference line implemented in a traditional WR-22 ridge waveguide.

For the design of the phase shifter in WR-22 the classical deign procedure of *Tribak et al.* [2014] can be used, with the only limitation that the width of the ridge must be the width of the two central PCB ($w = 0.6$ mm with the choice of commercial substrates that we have used). As in *Tribak et al.* [2014], after finding an initial point with an equivalent monomode circuit, the full-wave multimode simulator μWave of *Mician* [2016] is used for optimizing, since it is highly efficient and allows a rapid optimization. The final dimensions of the designed phase shifter in WR-22 are shown in Figure 21.

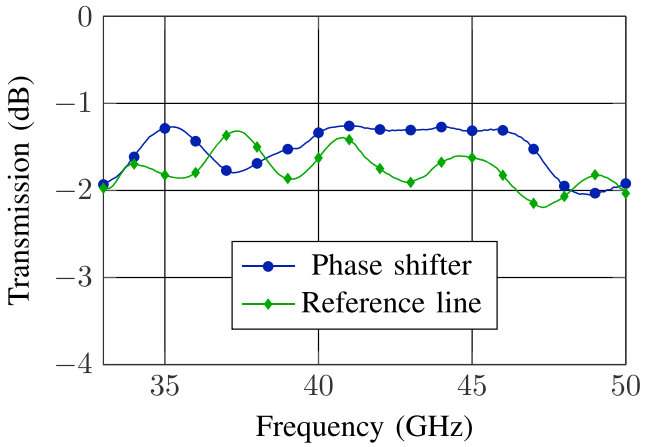


Figure 25. Measured transmissions of the ESIW-E phase shifter and the reference line.

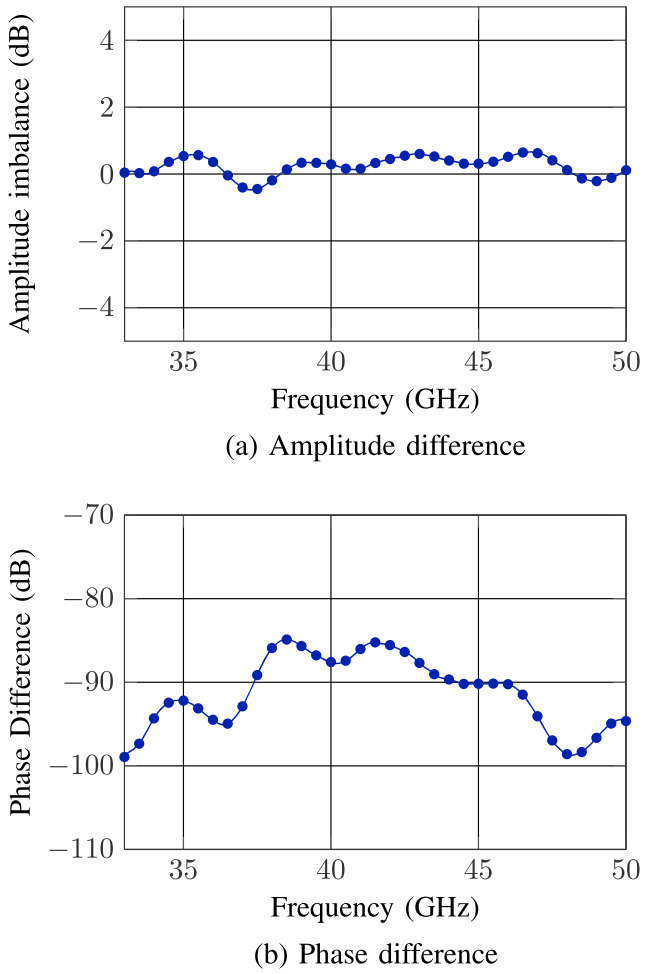


Figure 26. Measured amplitude and phase differences of the ESIW-E phase shifter and the reference line.

The simulated results of the CST model of Figure 20 are depicted in Figure 22. The return losses and the phase difference with respect to the reference line are shown. It can be observed that the design provides, at simulation level, good matching (return loss over 30 dB) and quite stable phase difference in the desired frequency band.

When the design in the classic rectangular waveguide is finished, it is mapped to an ESIW-E splitting the width of the WR-22 into several PCB. Table 3 shows the characteristics of the PCB used for the manufacturing of the phase shifter and its reference line. As it can be observed, the width of the ESIW-E with this choice of PCB is $a = 5.634$ mm, which is slightly lower than the width of the standard WR-22 ($a = 5.6896$ mm). However, it is worth noting that the tin soldering paste used for assembling the PCB slightly increases the width of the ESIW-E. T3

Figure 23 shows a schematic view of the ESIW-E phase shifter. It can be observed that the two central PCB form the ridge of the phase shifter. The reference line is similar but without the ridge steps.

The phase shifter and the reference line were measured in the coplanar probe station of Figure 17, with the J microTechnology adapters from coplanar to microstrip line, plus the golden tapers. The measured reflections of the phase shifter and the reference line are depicted in Figure 24. The return losses for both the phase shifter and the reference line are greater than 10 dB in the frequency band of interest (from 35 to 47 GHz). If the effect of the golden taper would be de-embeded from the measurements, the return losses would be higher. Figure 25 shows the transmission of both circuits. The insertion losses are lower than 2 dB. The amplitude and phase differences are depicted in Figure 26. The mean phase difference in the desired band is −89.1° with a maximum variation of ±5°. And the mean amplitude imbalance is 0.28 dB with a maximum variation of ±0.6 dB.

These results prove that the ESIW-E is a promising alternative for mapping *E* plane waveguide solutions in a low cost substrate integrated device. The *E* plane solutions cannot be mapped to SIW or ESIW. The performance is degraded when compared to the same device implemented in a classical rectangular waveguide, but the ESIW-E is low cost, integrated in a substrate and connected to planar microstrip ports, and its performance is much better than the performance of equivalent planar devices.

5. Conclusion

A new *E* plane empty substrate integrated waveguide (ESIW-E) has been presented. This new type of waveguide has the same advantages of other empty substrate integrated circuits (low cost, easy manufacturing, low losses compared to other SIC filled with substrate, higher-quality factor, and integration in a PCB), and it can easily map classical *E* plane solutions in rectangular waveguide, at the expense of needing more layers than the *H* plane ESIW.

A transition from microstrip to ESIW-E operating in a high-frequency band has been successfully designed, manufactured, and measured. A broadband high-frequency phase shifter has been implemented, and results prove the validity of this new type of circuit. The presence of a tapered transition from microstrip to coplanar waveguide (required for performing measurements at high frequencies with a probe station) increases the insertion losses and reduces the return losses, but it has been demonstrated with simulation that this effect is caused by this transition that has not been de-embeded from the measurements.

Acknowledgments
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