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From specialized to core course in Telecommunications degree: Experiences from digital electronic design and verification

Antonio Martinez-Millana[a,b], Alejandro Liberos[a,b], Jose M. Monzo[a,c], Marcos Martinez[a,c], Jorge Daniel Martinez[a,c] and Rafael Gadea[a,c]

[a]Dept. d'Enginyeria Electrònica. Universitat Politècnica de València. [b]ITACA.Universitat Politècnica de València. [c]I3M. Universitat Politècnica de València.

Abstract

The European Higher Education Area (EHEA) defines the competences for professional practice of a Telecommunications Engineer. The School of Telecommunication Engineering of the Universitat Politècnica de València (Valencia, Spain) provides an integrated education program consisting of a Graduate (GITST) + Master (MUIT). The GITST course offers four specialization tracks: Electronics, Telematics, Communication Systems and Multimedia for the proper acquisition of knowledge and competences of the future Telecommunications Engineers. In 2018, the graduate program has implemented a structural change in the organization of subjects for reinforcing important skills, in which a course on digital electronics design and verification (Integration of Digital Systems, ISDIGI) has been transformed into a core subject of the study plan. In this paper, we describe the methodology and adaptation of ISDIGI (i.e. a project-based learning intermediate HDL course that includes design and verification abilities) to the new GITST Curriculum. In addition, this paper describes the process of moving from specialized to core subject.

Keywords: *Telecommunications, Digital Electronics, EHEA, study plan*

1. Introduction

Moore's Law states that approximately every two years the number of transistors in a microprocessor is doubled. This means that today's a regular computer has a similar computational capacity as the NASA had when Neil Armstrong step on the moon, and that by 2025 a personal computer will have the computational capacity of a human brain. The advent of digital signal processing (DSP) systems, 32-bit microprocessors with internal DSP capabilities, Application Specific Integrated Circuits (ASICs) and Field Programmable

Gate Arrays (FPGAs) progressively replaced analog technologies by improving the maximum frequency range, stability and digital computing power with increasingly lower costs due to mass production manufacturing technologies. A FPGA is a programmable device that contains logic blocks whose interconnection and functionality can be electronically reconfigured. The FPGA design flow is based on specialized description languages, enabling hardware reuse for developing, testing and deploying digital systems. FPGA-based systems can be found in a wide range of applications, from aero-spatial systems to medical signal acquisition systems, including consumer electronics, power electronics and hardware acceleration. Hardware and software development environments have progressively included Hardware Description Verification Language (HDVL) as an integrated feature. HDVLs are languages that allow us to describe digital circuits together with their verification testbenches.

In 2009, the Spanish Ministry of Science and Innovation established the requirements of the official higher education that qualify for the profession of Telecommunications Engineering (Educación & Deporte, 2014). The current legislation defines the profession of Telecommunications Engineer as a regulated profession whose exercise requires the corresponding official degree, that complies with the new Bologna Plan promoted by the European Higher Education Area (EHEA). This ministerial disposition established the requirements that qualify for the exercise of the Telecommunications Engineer profession and specifically included: "*Knowledge and application of the fundamentals of hardware device description languages*" in the common study branch of the degree. In 2018, the graduate program for Telecommunications Systems Engineering of the U*niversitat Politècnica de València* has implemented a structural change in the organization of subjects for meeting the ministerial disposition, in which the subject of Integration of Digital Systems (ISDIGI) has been transformed from specialized branch into a core subject of the study plan.

This update has posed an interesting challenge for both the faculties and students, as it required to change the teaching methodology and syllabus structure to cover a course demand of more than 120 students, when formerly it was prepared for up to 30 students in the Electronics specialized branch. In this paper we describe the rationale and methods for transforming a branch subject into a common subject, the new proposed course structure and the evaluation results after the first year of set up.

2. Theoretical framework

Bowden and Marton defined the characteristics that a quality learning environment should provide (Bowden & Marton, 2003). These characteristics included varied set of teaching methods comprising concepts, theories, abilities and competencies which should be embedded into an interactive process between teachers and students, and among students themselves. Another important point was the introduction of realistic activities, in such a way that students can recognise them as socially valued and thus motivate and stimulate their interest towards the course. More recently, the Tuning Educational Structures defined the learning outcomes as "*statements of what a student is expected to know, understand and / or be able to demonstrate after completing a learning process"*. Learning outcomes are a fundamental pillar of the Bologna process and it requires to adapt the objective learning strategy to a more practical educational scenario (Bologna Working Group, 2005). Learning outcomes stand as a very useful tool for the planning and organization of higher education courses. On the one hand, they support teachers on the preparation of their lectures to the achievement of specific objectives defined as knowledge, abilities and competences (ANECA, 2012). Furthermore, they allow the student to meet beforehand the requirements needed to achieve during the course of the subject and, specifically, at the evaluation points.

2.1. Multimedia based support

New technologies in the classroom and those elsewhere located, known as virtual classrooms, have changed the way in which higher education is structured, paving the way to evolve from a teacher-directed method to a student-directed one (Abrami, 2005). We aim at including screen-casts and video and audio objects embedded into the educational program so they can be used by students anywhere and at any time they need to reinforce theoretical concepts, put in practice technical concepts and practice the skills of the subject.

2.2. Course assessment and evaluation

The increase of students enrolled in the subject (which accounts for a +300%) after the conversion from specialized to core course made necessary to adapt the number of teachers, adding three more lecturers to a course that was initially lectured by three professors. This change posed interesting challenges in the way each lecturer was implementing the course for his respective group of students, but also a risk in the way the tasks and the learning outcomes should be assessed in an objective and fair base. To this end, rubrics have been previously proposed to evaluate very different kinds of technical projects and skills

(Mergendoller, Markham, Ravitz, & Larmer, 2006). Analytical rubrics are useful to split a learning product into several sub-components and evaluate them independently with objective and clearly defined metrics and scores. In this subject, we aimed at defining a standard rubric for the major evaluation assignments students had to develop. The evaluation of this task was carried out by means of iRubric, from RCampus (Rcampus, 2019).

3. Case description

3.1. Structure of the subject and methodology

The subject is dedicated to the advanced verification and design of digital systems through the extensive use of System Verilog as verification and hardware description language. The presented program (topics, methodology and evaluation) are intended to provide an outcome-based subject for ensuring the following learning outcomes: 1) To analyse and design complex digital circuits architectures (i.e.: digital signal processing modules, microprocessor, etc.). 2) To use hardware description languages for the modelling and synthesis of combinational and sequential circuits. 3) To develop simple applications in assembly language 4) To implement advanced System Verilog-based automated verification methodologies and 5) To design testbenches that allow the functional validation of a module through hardware description languages. Table 1 depicts the course structure in chapters and the distribution of classroom lectures and the laboratory sessions.

Table 1. Course structure and distribution

Chapter	**Classroom sessions (hours)**	**Laboratory sessions (hours)**
System Verilog and Verification	10	8
Architectural design and partitions	8	4
High-level synthesis and temporal considerations	8	6
Data processing architectures	10	6

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As presented before, the main objective of the proposed methodology was the acquisition of competences by encouraging a growing autonomy of the students throughout the course. Accordingly, 75% of the percentage in the evaluation was dedicated to practical activities developed in teams from 3 to 6 students, while the theoretical part accounted for 25% and

was evaluated with two multiple-choice tests that had to be done individually. The contents of the course were introduced by means of an expository methodology in classrooms sessions, in addition, teachers motivated the participation of students through open questions or linking with the practical part of the subject. For the practical part, laboratory sessions were dedicated for team work. The teacher acted as a guide or mentor throughout the learning process. Tasks were also completed at home and individual or team tutorials and multimedia based support were also available. Even though the laboratory team was the same through the entire course, the roles of the members had to be swapped on each practical assignment. For instance, in the first project, half of the team should be devoted to design tasks, whereas the other half should be on verification task. In the subsequent projects, the team members who had done the design should move to the verification and so on.

3.2. Practical assignments

Laboratory sessions were aimed at developing two tasks (sections 3.2.1 and 3.2.2) and a project (section 3.2.3). Students were gathered into groups from 3-6 members, in which a half of them should focus on hardware design and the other half on the verification. Tasks had an atomic structure with clear and well defined objectives. The project consisted of a pipelined set of tasks (some of which could be developed sequentially or in parallel) with a clear definition of the control points (deliverables and progress reports), mandatory objectives and voluntary developments.

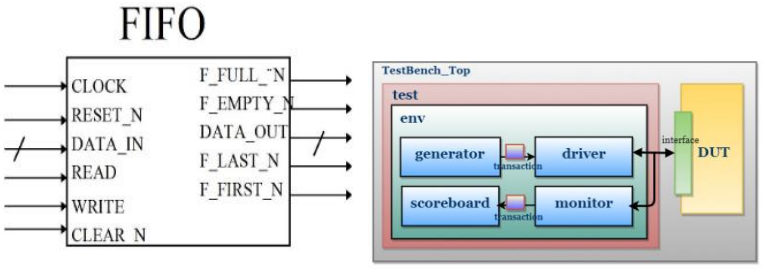

Fig. 1 Materials for task 1
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3.2.1. Design and Verification of a FIFO stack

Previous digital electronics courses are more focused on developing students design capabilities rather than verification. In this first task, students had to focus on verification and to get used to describe full test-benches with Verilog and learn new advanced

verification methodologies in System Verilog. During this task the student should gradually change their verification methodology from a Verilog based classical one to a System Verilog based self-checking methodology. In addition to functional simulations, developed as in the previous courses, students were provided with a much more powerful and complex testbench based on System Verilog, with the intention, that they understand a modern testbench architecture. During this task, students should add incrementally new verification functionalities sucha as the RCSG ("random constrained stimuli generation"), assertions, behavioural models or the functional coverage. In this way, students progressively learn the most typical System Verilog verification structures, as well as the types of necessary data for these tasks (Fig. 1).

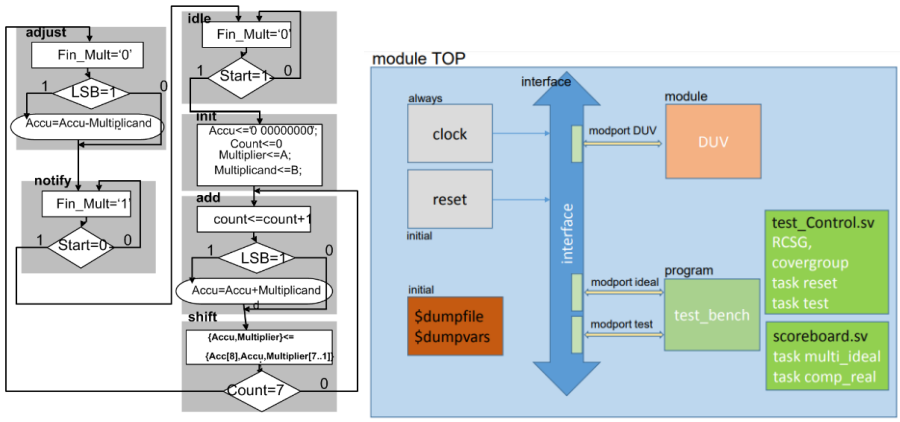

Fig.2 Materials for task 2
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3.2.2. Add and shift multiplier

In the second course task, students had to design and verify a parameterized two's complement binary multiplier. The proposed multiplier architecture is based on sums and shifts. The proposed design should be fully described in System Verilog with two hierarchical levels already introduced in the theoretical lessons dedicated to the “control-path” and “data-path” of a digital system and its architectural design (Fig. 2). A System Verilog automated tesbench should be developed to verify the described hardware. Finally, students had to implement their desings on the FPGA-based evaluation boards available in the laboratory.. However, at this stage, students started to miss classroom sessions and attended the practical sessions without the sufficient knowledge to extract the task requirements and draft the FSM (Fig. 2).

3.2.3. RISC-V micro-processor

The final task is focused on the design, functional verification and experimental validation of a simple microcontroller based on an instruction subset of the RISC-V architecture. The microcontroller had to be described in System Verilog so that it is synthesizable and can be implemented in the FPGAs in the laboratory. The experimental validation should be carried out in the laboratory through a simple application proposed by each team of students that makes use of the hardware resources available in the test module (Fig. 3). The project therefore covers the aspects of functional verification, microprocessor architecture, hardware segmentation, hardware description using System Verilog, implementation of a complex digital system integrated in a programmable device and assembly language programming of the RISC-V. The microcontroller was developed in four different phases. Phase 1 was focused on the design and validation of the functional units of the processor: instructions and data memories, register bank and arithmetic-logic unit (ALU). In addition, the programming model of the RISC-V architecture was introduced and put into practice by students through a series of simple assembler programs. Phase 2 consisted on the implementation of a single-cycle model of the processor. The priority was to deliver a fully functional model, which had to be validated exhaustively. Phase 2 model was then defined as the golden-model, which then allowed carrying out the verification of the segmented implementation.

Phase 3 was aimed at the hardware segmentation of the processor developed in the previous phase, as well as to the extent possible to carry out the introduction of mechanisms for the detection and control of risks that allow the execution of the instructions implemented without the need to introduce delay gaps or make segmentation stops. Finally, in Phase 4 students had to implement and validate the designed microprocessor in the Cyclone IV FPGA based board available in the laboratory. The objective was then to test simple programs that runs on the microcontroller and, using the elements available in the DE-2 module, carry out a simple application (e.g. control of LEDs, timing, use of the 7-segment displays, etc.). The program had to allow interaction with the user (i.e. students had to use both the output pins and the input pins of the GPIO module). The final task was presented at the end of the course to a panel formed by the teachers of the subject, this final evaluation was useful to identify those students that contributed differently to the task.

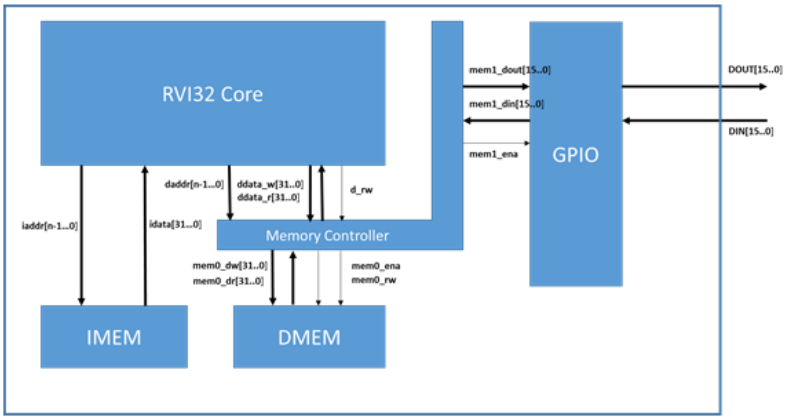

Fig.3 Materials for task 3.
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3.2.4. Evaluation and scores

Practical assignments were evaluated using an electronic rubric edited in iRubrics. We implemented three different analytic rubrics which defined three performance levels (indicators), each of them representing a factor for each of the assessed categories: Not implemented (0.0), Implemented (0.7) and Excellent Implementation (1.0). The assessment categories depended on the type of assignment, but the common structure contained Hardware Design (use of parametrization, comments in the code, proper use of System Verilog rules, coding style), Verification (implementation of a testbench, randomization, stimulus generator, cover-groups, timers and interfaces). The mark was in general shared for the whole team presenting the activity. Exceptionally, the grade was differentiated for those students who contributed differently to the task (abandoning team etc).

4. Discussion

In this paper we have described the process of converting a specialization course into a common branch course for the curricula of Telecommunication Engineer Degree under the EHEA. The approach presented hereby was successful in the way it enabled a collaboration with new lecturers in the team of professors and provided objective metrics and measurement methods to evaluate the attainment of learning outcomes. The evaluation with rubrics was different categories and objective indicators, a fact that allowed us to have an homogeneous criteria among the six teachers and helped students to know beforehand what

were the evaluating points and the scoring criteria (Martínez, Herrero, & De Pablo, 2011). The proposed approach for laboratory sessions was also satisfactory in the way team members switched on their roles, and tasks (form hardware design to software verification). Nevertheless, we should point out that in two of the assignments, students were provided with basic units of software so hardware designers and verifications could work in parallel. Multimedia based support were mainly viedos that helped students in the development of tasks and project. They made compatible the different work rhythms of the teams and avoided team work interruptions. A major limitation was the low attendance rates to the classroom sessions, as it affected the normal development of laboratory. A significant part of the students did not had the knowledge that should be put into practice in the tasks with the consequent delay in the implementation. A secondary limitation was the imbalance in the achievement of the competences detected in some students in comparison with other members in their teams. To face these limitations, forthcomming courses will integrate attendance controls and more multimedia and flipped teaching resources (mini-videos, materials and tests) to mitigate the negative impact of students un-attendance. Self-evaluation, continuous and peer assessment tools will be evaluated in the upcoming courses to avoid imbalances in the teams.

In summary, the case presented describes the year of growth of a subject in which the practical part predominates. Despite the significant increase in the number of both teachers and students, the course has been completed satisfactorily, limitations were detected and improvements are proposed for the upcoming courses.

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