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KM3NeT front-end and readout electronics system: hardware, firmware, and software

Sebastiano Aiello,[a] Fabrizio Ameli,[b] Michel Andre,[c] Giorgos Androulakis,[d] Marco Anghinolfi,[e] Gisela Anton,[f] Miquel Ardid,[g] Julien Aublin,[h] Christos Bagatelas,[d] Giancarlo Barbarino,[i,j] Bruny Baret,[h] Suzan Basegmez du Pree,[k] Anastasios Belias,[d] Meriem Bendahman,[l] Edward Berbee,[k] Ad M. van den Berg,[m] Vincent Bertin,[n] Vincent van Beveren,[k,*] Simone Biagi,[o] Andrea Biagioni,[b] Matthias Bissinger,[f] Pascal Bos,[k] Jihad Boumaaza,[l] Simon Bourret,[h] Mohammed Bouta,[p] Gilles Bouvet,[q] Mieke Bouwhuis,[k] Cristiano Bozza,[r] Horea Brânzaş,[s] Max M. Briel,[k,t] Marc Bruchner,[f] Ronald Bruijn,[k,t] Jurgen Brunner,[n] Ernst-Jan Buis,[u] Raffaele Buompane,[i,v] Jose Busto,[n] David Calvo,[w,*] Antonio Capone,[x,b] Silvia Celli,[b,x,y] Mohamed Chabab,[z] Nhan Chau,[h] Silvio Cherubini,[o,aa] Vitaliano Chiarella,[ab] Tommaso Chiarusi,[ac] Marco Circella,[ad] Rosanna Cocimano,[o] Joao A. B. Coelho,[h] Alexis Coleiro,[w] Marta C. Molla,[h,w] Stephane Colonges,[h] Rosa Coniglione,[o] Paschal Coyle,[n] Alexandre Creusot,[h] Giacomo Cuttone,[o] Antonio D'Amico,[k] Antonio D'Onofrio,[i,v] Richard Dallier,[q] Mauro De Palma,[ad,ae] Irene Di Palma,[b,x] Antonio F. Díaz,[af] Didac Diego-Tortosa,[g] Carla Distefano,[o] Alba Domi,[e,n,ag] Roberto Donà,[ac,ah] Corinne Donzaud,[h] Damien Dornic,[n] Manuel Dörr,[ai] Mora Durocher,[o,y] Thomas Eberl,[f] Thijs van Eeden,[k] Imad El Bojaddaini,[p] Hassnae Eljarrari,[l] Dominik Elsaesser,[ai] Alexander Enzenhöfer,[n] Paolo Fermani,[b,x] Giovanna Ferrara,[o,aa] Miroslav D. Filipović,[aj] Luigi A. Fusco,[h] Deepak Gajanana,[k] Tamas Gal,[f] Alfonso Garcia Soto,[k] Fabio Garufi,[i,j] Lucio Gialanella,[i,v] Emidio Giorgio,[o] Sara R. Gozzini,[w] Rodrigo Gracia,[f] Kay Graf,[f] Dario Grasso,[ak] Timothee Grégoire,[h] Giuseppe Grella,[r] Daniel Guderian,[al] Carlo Guidi,[e,ag] Steffen Hallmann,[f] Hassane Hamdaoui,[l] Hans van Haren,[am] Aart Heijboer,[k] Amar Hekalo,[ai] Juan J. Hernández-Rey,[w] Jannik Hofestädt,[f] Feifei Huang,[an] Enrique H. Santiago,[k] Giulia Illuminati,[w] Clancy W. James,[ao] Peter Jansweijer,[k] Martijn Jongen,[k] Maarten de Jong,[k] Paul de Jong,[k,t] Matthias Kadler,[ai] Piotr Kalaczyński,[ap] Oleg Kalekin,[f] Uli F. Katz,[f] Nafis R. Khan Chowdhury,[w] Frits van der Knaap,[u] Els N. Koffeman,[k,t] Paul Kooijman,[t,aq] Antoine Kouchner,[h,ar] Michael Kreter,[as] Vladimir Kulikovskiy,[e] Robert Lahmann,[f] Giuseppina Larosa,[o] Remy Le Breton,[h] Francesco Leone,[o,z] Emanuele Leonora,[a] Giuseppe Levi,[ac,ah] Massimiliano Lincetto,[n] Miles Lindsey Clark,[h] Alessandro Lonardo,[b] Fabio Longhitano,[a] Daniel Lopez-Coto,[at] Giuliano Maggi,[n] Jerzy Mańczak,[w] Karl Mannheim,[ai] Annarita Margiotta,[ac,ah] Antonio Marinelli,[ak,au] Christos Markou,[d] Gregory Martignac,[q] Lilian Martin,[q] Juan A. Martínez-Mora,[g] Agnese Martini,[ab] Fabio Marzaioli,[i,v] Safaa Mazzou,[y] Rosa Mele,[i,j] Karel W. Melis,[k] Pasquale Migliozzi,[i] Emilio Migneco,[o] Piotr Mijakowski,[ap] Luis S. Miranda,[av] Carlos M. Mollo,[i] Mauro Morganti,[ak,aw] Michael Moser,[f] Abdelilah Moussa,[p] Rasa Muller,[k] Paolo Musico,[e] Mario Musumeci,[o] Lodewijk Nauta,[k] Sergio Navas,[at] Carlo A. Nicolau,[b] Christine Nielsen,[h] Brian Ó Fearraigh,[k,t] Mukharbek Organokov,[an] Angelo Orlando,[o] Vasilis Panagopoulos,[d] Gogita Papalashvili,[ax] Riccardo Papaleo,[o] Cosimo Pastore,[ad] Gabriela E. P v laş,[s] Giuliano Pellegrini,[ac] Carmelo Pellegrino,[ah,ay] Mathieu Perrin-Terrin,[n] Paolo Piattelli,[o] Camiel Pieterse,[w] Konstantinos Pikounis,[d] Ofelia Pisanti,[i,j] Chiara Poirè,[g] Georgia Polydefki,[d] Vlad Popa,[s] Maarten Post,[t] Thierry Pradier,[an] Gerd Pühlhofer,[az] Sara Pulvirenti,[o] Liam Quinn,[n] Fabrizio Raffaelli,[ak] Nunzio Randazzo,[a] Antonio Rapicavoli,[z] Soebur Razzaque,[av] Diego Real,[w,*] Stefan Reck,[f] Jonas Reubelt,[f] Giorgio Riccobene,[o] Marc Richer,[an] Louis Rigalleau,[q] Alberto Rovelli,[o] Ilenia Salvadori,[n] Dorothea F. E. Samtleben,[k,ba] Agustin Sánchez Losa,[ad] Matteo Sanguineti,[e,ag] Andrea Santangelo,[az] Domenico Santonocito,[o] Piera Sapienza,[o] Jan-Willem Schmelling,[k] Jutta Schnabel,[f] Virginia Sciacca,[o] Jordan Seneca,[k] Irene Sgura,[ad] Rezo Shanidze,[ax] Ankur Sharma,[au] Francesco Simeone,[b] Anna Sinopoulou,[d] Bernardino Spisso,[r,i] Maurizio Spurio,[ac,ah] Dimitris Stavropoulos,[d] Jos Steijger,[k] Simona M. Stellacci,[i,r] Bruno Strandberg,[k] Dominik Stransky,[f] Mauro Taiuti,[e,ag] Yahya Tayalati,[l] Enrique Tenllado,[at] Tarak Thakore,[w] Paul Timmer,[k] Steven Tingay,[ao] Ekaterini Tzamariudaki,[d] Dimitrios Tzanetatos,[d] Veronique Van Elewyck,[h,ar] Federico Versari,[ac,ah] Salvo Viola,[o] Daniele Vivolo,[i,j] Gwenhael de Wasseige,[h] Joern Wilms,[bb] Rafał Wojaczyński,[ap] Els de Wolf,[k,t] Dmitry Zaborov,[n,bc] Angela Zegarelli,[b,x] Juan D. Zornoza,[w] and Juan Zúñiga[w]

[a]INFN, Sezione di Catania, Catania, Italy
[b]INFN, Sezione di Roma, Roma, Italy
[c]Universitat Politècnica de Catalunya, Centre Tecnològic de Vilanova i la Geltrú, Laboratori d'Aplicacions Bioacústiques, Vilanova i la Geltrú, Spain
[d]NCSR Demokritos, Institute of Nuclear and Particle Physics, Athens, Greece
[e]INFN, Sezione di Genova, Genova, Italy
[f]Friedrich-Alexander-Universität Erlangen-Nürnberg, Erlangen Centre for Astroparticle Physics, Erlangen, Germany
[g]Universitat Politècnica de València, Instituto de Investigación para la Gestión Integrada de las Zonas Costeras, Gandia, Spain
[h]APC, Université Paris Diderot, CNRS/IN2P3, CEA/IRFU, Observatoire de Paris, Sorbonne Paris Cité, Paris, France
[i]Complesso Universitario di Monte S. Angelo, INFN, Sezione di Napoli, Napoli, Italy
[j]Università di Napoli "Federico II," Complesso Universitario di Monte S. Angelo, Dipartimento Scienze Fisiche "E. Pancini," Napoli, Italy
[k]Nikhef, National Institute for Subatomic Physics, Amsterdam, The Netherlands
[l]University Mohammed V, Faculty of Sciences, Rabat, Morocco
[m]KVI-CART University of Groningen, Groningen, The Netherlands
[n]Aix Marseille University, CNRS/IN2P3, CPPM, Marseille, France
[o]INFN, Laboratori Nazionali del Sud, Catania, Italy
[p]University Mohammed I, Faculty of Sciences, Oujda, Morocco
[q]Université de Nantes, Subatech, IMT Atlantique, IN2P3-CNRS, Nantes, France
[r]Università di Salerno e INFN Gruppo Collegato di Salerno, Dipartimento di Fisica, Fisciano, Italy
[s]ISS, Măgurele, Romania
[t]University of Amsterdam, Institute of Physics/IHEF, Amsterdam, The Netherlands
[u]TNO, Technical Sciences, Delft, The Netherlands

[v]Università degli Studi della Campania "Luigi Vanvitelli," Dipartimento di Matematica e Fisica, Caserta, Italy
[w]IFIC - Instituto de Física Corpuscular (CSIC - Universitat de València), Valencia, Spain
[x]Università La Sapienza, Dipartimento di Fisica, Roma, Italy
[y]Gran Sasso Science Institute, GSSI, L'Aquila, Italy
[z]Cadi Ayyad University, Department of Physics, Faculty of Science Semlalia, Marrakech, Morocco
[aa]Università di Catania, Dipartimento di Fisica e Astronomia, Catania, Italy
[ab]INFN, LNF, Frascati, Italy
[ac]INFN, Sezione di Bologna, Bologna, Italy
[ad]INFN, Sezione di Bari, Bari, Italy
[ae]University of Bari, Bari, Italy
[af]University of Granada, Department of Computer Architecture and Technology/CITIC, Granada, Spain
[ag]Università di Genova, Genova, Italy
[ah]Università di Bologna, Dipartimento di Fisica e Astronomia, Bologna, Italy
[ai]University Würzburg, Würzburg, Germany
[aj]Western Sydney University, School of Computing, Engineering and Mathematics, Penrith, New South Wales, Australia
[ak]INFN, Sezione di Pisa, Pisa, Italy
[al]University of Münster, Institut für Kernphysik, Münster, Germany
[am]Utrecht University, NIOZ (Royal Netherlands Institute for Sea Research), Texel, The Netherlands
[an]Université de Strasbourg, CNRS, IPHC, Strasbourg, France
[ao]Curtin University, Curtin Institute of Radio Astronomy, Perth, Western Australia, Australia
[ap]National Centre for Nuclear Research, Warsaw, Poland
[aq]Utrecht University, Department of Physics and Astronomy, Utrecht, The Netherlands
[ar]Institut Universitaire de France, Paris, France
[as]North-West University, Centre for Space Research, Potchefstroom, South Africa
[at]University of Granada, Dipartimento de Física Teórica y del Cosmos & C.A.F.P.E., Granada, Spain
[au]Università di Pisa, Dipartimento di Fisica, Pisa, Italy
[av]University of Johannesburg, Department Physics, Auckland Park, South Africa
[aw]Accademia Navale di Livorno, Livorno, Italy
[ax]Tbilisi State University, Department of Physics, Tbilisi, Georgia
[ay]INFN, CNAF, Bologna, Italy
[az]Eberhard Karls Universität Tübingen, Institut für Astronomie und Astrophysik, Tübingen, Germany
[ba]Leiden University, Leiden Institute of Physics, Leiden, The Netherlands
[bb]Friedrich-Alexander-Universität Erlangen-Nürnberg, Remeis Sternwarte, Bamberg, Germany
[bc]NRC "Kurchatov Institute," A.I. Alikhanov Institute for Theoretical and Experimental Physics, Moscow, Russia

Abstract. The KM3NeT research infrastructure being built at the bottom of the Mediterranean Sea will host water-Cherenkov telescopes for the detection of cosmic neutrinos. The neutrino telescopes will consist of large volume three-dimensional grids of optical modules to detect the Cherenkov light from charged particles produced by neutrino-induced interactions. Each optical module houses 31 3-in. photomultiplier tubes, instrumentation for calibration of the photomultiplier signal and positioning of the optical module, and all associated electronics boards. By design, the total electrical power consumption of an optical module has been capped at seven Watts. We present an overview of the front-end and readout electronics system inside the optical module, which has been designed for a 1-ns synchronization between the clocks of all optical modules in the grid during a life time of at least 20 years. [DOI: 10.1117/1.JATIS.5.4.046001]

Keywords: front-end electronics; readout electronics; neutrino telescope; KM3NeT.

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1 Introduction

KM3NeT is a European research facility being built at the bottom of the Mediterranean Sea. It will host the future large volume ORCA[1] and ARCA[2] neutrino telescopes. The ARCA telescope (Astroparticle Research with Cosmics in the Abyss), a cubic kilometer-scale detector mainly dedicated to the detection of high energy neutrinos of astrophysical origin, is being installed at a site located offshore from the coast of Sicily, Italy, at an approximate depth of 3500 m. The detector of the Oscillation Research with Cosmics in the Abyss telescope (ORCA), located at a depth of about 2400-m offshore of Toulon, France, will be optimized for the detection of lower energy neutrinos to allow for the study of fundamental properties of neutrinos. ARCA and ORCA share the same detector technologies.[3] Cherenkov light produced by neutrino-induced charged particles will be detected by a regular array of optical modules in the water volume of the telescope [Fig. 1(a)]. Each module [Fig. 1(b)] is a high-pressure resistant, 17-in.-diameter glass sphere containing 31 3-in. photomultiplier tubes (PMTs), instrumentation for calibration and positioning, and all associated electronics boards. The modules are called digital optical modules (DOMs).[4–6] Eighteen DOMs, uniformly distributed along a vertical slender structure, form a detection unit (DU). The DOMs are held in place by means of two thin ropes. The DU is anchored on the seabed and kept in a close to vertical position by a submerged buoy at its top. An electro-optical backbone cable, with breakouts at each DOM, runs along the full DU length, providing connection for power feeding with one DU common line of 400 V, and data transmission with one single fiber per DOM.

*Address all correspondence to Diego Real, E-mail: real@ific.uv.es; David Calvo, E-mail: dacalcia@ific.uv.es; Vincent van Beveren, E-mail: v.van.beveren@nikhef.nl

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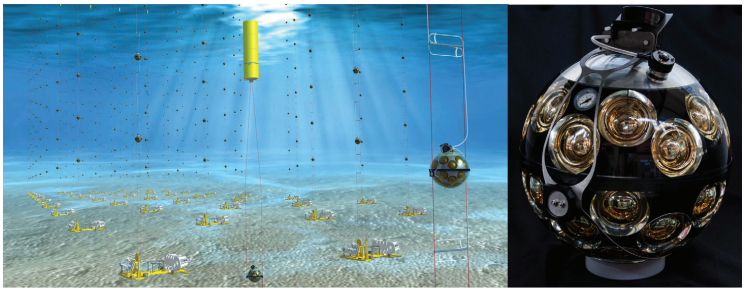

Fig. 1 (a) Artistic illustration of the KM3NeT detector. Note that the illustration is not to scale and that sunlight will not actually reach the depths at which the KM3NeT detector is deployed. (b) A picture of the KM3NeT optical module with the fly's eye organization of the PMTs and the cap of the aluminum cooling "mushroom" visible. The titanium collar around the module supports the connection to the ropes of the DU.

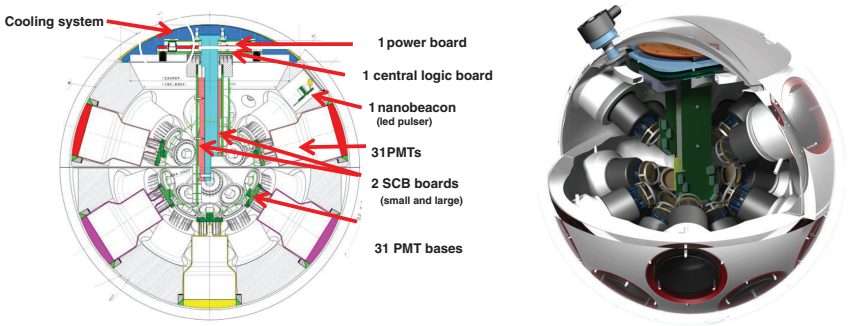

Fig. 2 Two- and three-dimensional drawings of the DOM showing the positions of the different devices.

In each DOM, the 31 PMTs are organized in five rings of six PMTs, plus a single one at the bottom pointing downward (Fig. 2). The PMTs are kept in place by a three-dimensional printed support structure. The lower and the upper hemispheres of the module contain 19 and 12 PMTs, respectively. In the upper hemisphere, a mushroom-shape aluminum structure provides support to the electronic boards of the DOM. The top surface of the mushroom cap is glued to the glass sphere in order to provide heat dissipation to the seawater. The measured temperature (oC) inside the DOM is about 22 deg with a sea temperature around 13 deg. Fixed to the mushroom cap is the power board, which provides all the dc voltages needed by the electronics. This board will be described in Sec. 3. The central logic board (CLB), which contains a field programmable gate array (FPGA), is directly connected to the power board. In the FPGA, the intellectual property (IP) cores that capture the PMT-generated signals are embedded. Also embedded in the FPGA is an implementation of the White Rabbit (WR),[7] a fully deterministic Ethernet-based timing protocol that provides both data transmission and accurate timing. The WR technology allows for a synchronization of the clocks of all CLBs in the telescope at nanosecond precision.

The description of the CLB is presented in Sec. 2. In Sec. 4, the PMT base board, which generates and adjusts the high voltage (HV) supply of the PMT and converts the analog signals generated by the PMTs to low voltage differential signaling (LVDS) is described. Two signal collection boards (SCBs), one for each DOM hemisphere, connect the CLB with the PMTs allowing for command and data signal transfer. The SCB is described in Sec. 5.

The light detected by a PMT is converted into an electrical pulse. When this electrical pulse surpasses a predetermined threshold, the PMT base board sets its LVDS output. This output is reset when the electrical pulse goes below the threshold. The first crossing of the threshold and the time over threshold (ToT) will be measured by the time-to-digital converters (TDCs) implemented in the CLB. The ToT gives an estimate of the pulse amplitude and its charge. The calibration of the PMT HV, using the DOM acquisition electronics system, provides an average ToT value of 26.4 ns when a single photoelectron (spe) impinges on a PMT with a threshold set at 30% of the spe.[8]

The CLB organizes the acquisition of the LVDS signals in frames, or timeslices, of fixed length in time, typically 100 ms. The data acquired and organized in timeslices are sent to a computer farm onshore via an optical network integrated in the submarine cables and junction boxes. The DU anchor hosts a base module equipped with a wet-mateable jumper to connect the DU to the seafloor network. The full chain of readout electronics was successfully qualified in a prototype DU of three DOMs deployed at the Italian KM3NeT site in May 2014 and operated

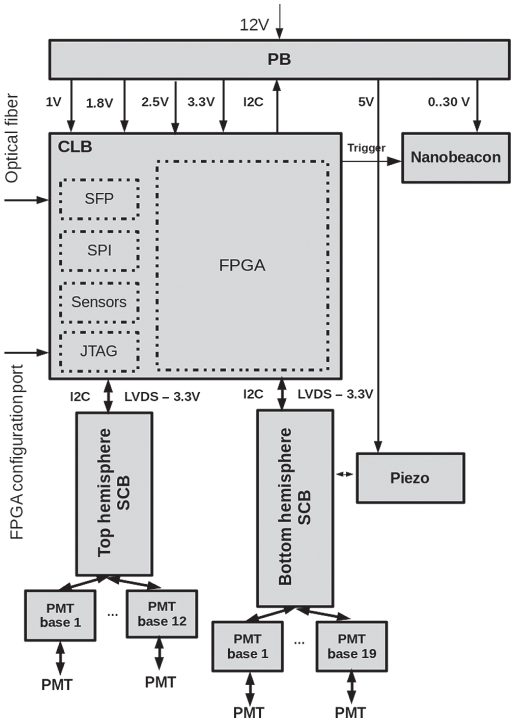

Fig. 3 Block diagram of the DOM electronics boards and their interconnections. The power board receives the 12-V input and generates all the voltages needed by the rest of electronics board. The CLB, the main electronics board, includes an FPGA where the data acquisition firmware runs, as well as different sensors and for communication via an optical fiber. The SCBs transfer the PMT signals to the CLB, while the PMT base digitizes the PMT signals. The CLB FPGA configuration port is not used in a closed DOM.

for more than 1 year.[9] Mass-produced electronics are operational in full-size deployed DUs with 18 DOMs,[10] thus demonstrating their functionality.

Figure 3 shows a block diagram of the different DOM electronics boards and their interconnections. The power consumption of the DOM is discussed in Sec. 6 and the reliability studies performed on the DOM electronics boards are presented in Sec. 7. Finally, a conclusion is given about the front-end and readout electronics system in light of the design goals set out by the KM3NeT Collaboration.

2 Central Logic Board

The DOM CLB[11,12] (Fig. 4) is the main electronics board in the readout chain of KM3NeT. The PMT bases generate LVDS signals from the PMT electrical pulses. The corresponding SCB receives and distributes these signals to the CLB, where they are digitized with a resolution of 1 ns by TDCs running in the FPGA programmable logic. After being organized and time stamped in the CLB, the TDC data are transferred to the onshore station for further processing and storage. The CLB board also houses a compass/tiltmeter, three temperature sensors, and a humidity sensor. In addition, it provides a connection for an

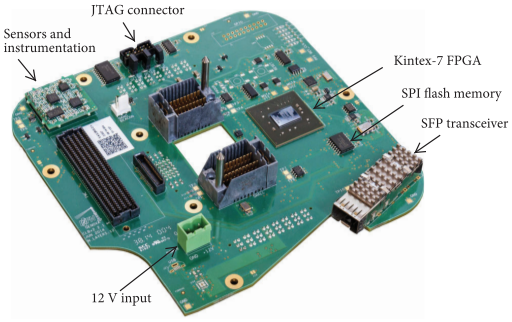

Fig. 4 The DOM CLB. The dimensions of the board are 150 mm × 150 mm.

LED flasher, called a nanobeacon.[13] In addition, a piezo sensor is connected to the CLB via the SCB that serves the lower hemisphere.

The control of the CLB is achieved by means of custom software, which runs in a LatticeMico32 (LM32)[14] soft-processor operating in the programmable logic of the CLB FPGA.

In the next sections, the hardware, firmware, and software of the CLB are described.

2.1 *Central Logic Board Hardware*

The CLB printed circuit board (PCB) comprises 12 layers: six of them are dedicated to signals, two of them to power planes, while the remaining four layers are ground. The ground layers surround the power planes in order to reduce the electromagnetic interference from the power layers on the signal layers and to improve the signal integrity.[15] For the same reasons, the number of vias in these layers has also been minimized wherever possible. Special care has been taken in routing the LVDS signals generated by the PMT base boards. The difference in length between any of the differential pairs has been kept below 100 ps. Moreover, in the case of the clock signals, this difference has been reduced to below 20 ps.

The central coordinating component of the CLB is a Xilinx Kintex-7 FPGA (XC160-T), chosen for its relatively low power consumption. Other relevant components are the serial peripheral interface (SPI) flash memory, which stores four images of the FPGA and the configuration parameters of the CLB; the programmable oscillators, which provide the appropriate clock signals needed by the WR protocol; two press fit connectors that provide a solid mechanical and electrical connection between the CLB and the SCB. The CLB board includes a 25-MHz crystal oscillator. The oscillator signal is first transferred from a clock pin to a buffer in the FPGA, and then fanned out to the inner phase locked loop (PLL) to provide two high frequency clocks of 250 MHz but with a 90-deg phase shift needed by the TDC core. The main component used for the communications with the onshore station is the small form-factor pluggable (SFP) transceiver, which interfaces the electronics with the optics system.

2.2 *CLB Firmware*

The readout logic of the DOM runs in the programmable fabric of the FPGA. A block diagram of the readout logic is shown in Fig. 5. Its main blocks are:

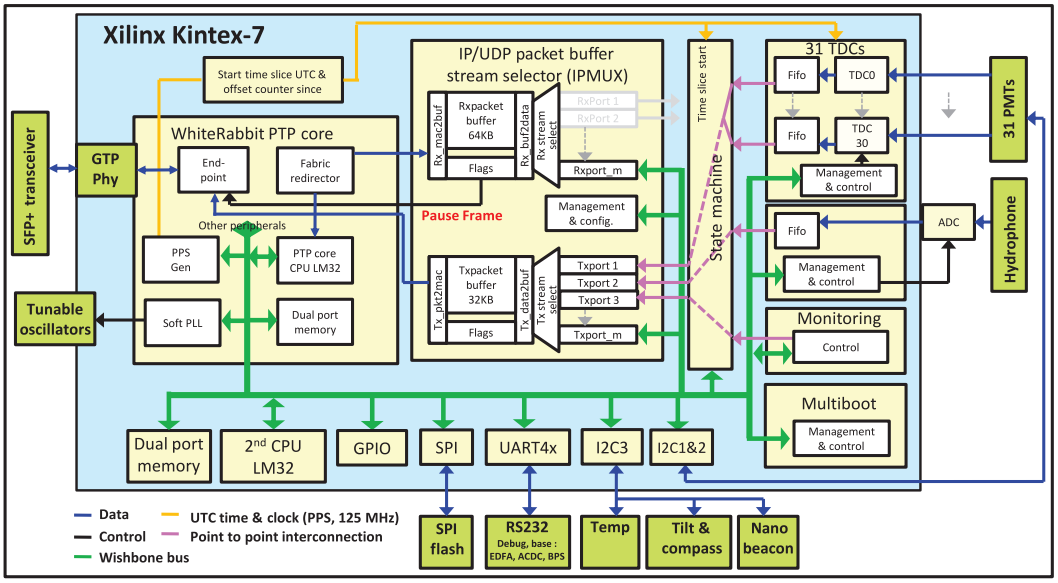

Fig. 5 Block diagram of the CLB FPGA firmware.

- The LM32 soft-processor running the control and monitoring software for the CLB.
- The White Rabbit PTP Core (WRPC) [precision time protocol (PTP)], which implements the WR protocol.
- The TDCs, which digitize and time-stamp the PMT signals arriving at the CLB.
- The state machine and IPMux cores, which collect the TDC data from the PMTs, Audio Engineering Society version 3 (AES3) data from the piezo sensor, and the monitoring data from the LM32, and dispatch them over Ethernet to the onshore station.[16]
- The multiboot core, which allows safe remote reconfiguration of the FPGA firmware.
- The different control cores for the instrumentation.

2.2.1 *Soft-microcontroller*

Central to the control and monitoring of the CLB is the LM32, a section of the FPGA fabric consisting of a central processing unit (CPU), random access memory (RAM), and peripherals for timing and communication [universal asynchronous receiver/transmitter, SPI, and inter integrated circuit (I^2C)]. The LM32 was chosen because it uses less FPGA resources than other CPUs[17] and has a wishbone bus[18] master interface. For the wishbone bus, many open-source programmable logic peripherals exist, such as SPI/I^2C controllers, coprocessors, timers, and counters. In addition, the LM32 CPU is also used in the WRPC, easing the integration and reducing the design complexity. The CPU runs at 62.5 MHz and has 128 KB of combined program and data RAM. Moreover, the wishbone bus also connects to the KM3NeT-specific programmable logic cores, such that the LM32 can control and monitor the peripherals, which are discussed in the next sections.

2.2.2 *White Rabbit PTP core*

The WRPC is an enhanced Ethernet media access controller (MAC), embedded in the CLB FPGA programmable logic. Apart from transferring data as a regular Ethernet MAC does, the WR protocol synchronizes all CLB clocks in the detector. The protocol is based on the synchronous Ethernet (SyncE) and PTP standards.[19] The WRPC synchronizes the CLB through the same optical link that is used for data transmission. The global time of the network is provided by the WR master switch located onshore, which is synchronized to a global positioning system receiver. The WRPC IP core synchronizes with the WR master switch and provides a register with the coordinated universal time (UTC), which is used by the rest of the CLB firmware. It also outputs a pulse per second (PPS) signal, whose rising edge occurs precisely at the second transition of the global CLB UTC. In order to qualify the stability of the synchronization at the CLB, the skew between the PPS of the CLB and the PPS of a WR switch has been measured at the laboratory using a 50-km optical fiber connection. The skew has a Gaussian distribution with a 22-ps standard deviation (Fig. 6). On the other hand, the time synchronization between DOMs in a deployed

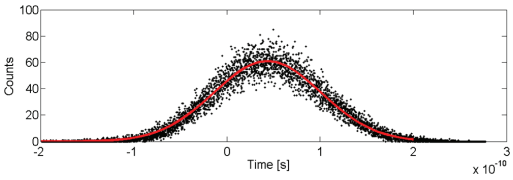

Fig. 6 Skew, measured at the laboratory, of the PPS of the CLB with respect to the PPS of the master WR switch. The red line is a Gaussian fit to the data with 22-ps standard deviation.

DU of ARCA, which takes into account the transit-time spread of the PMT and other types of jitters, has been measured *in situ* using down-going muons and a nanobeacon showing to be of the order of one ns.[20]

2.2.3 *State machine*

The data acquisition is organized in consecutive frames with a period of typically 100 ms, called timeslices. The state machine core orchestrates the data acquisition for the CLB. First, it is responsible for generating the periodic start of the timeslice signal. This signal is synchronized to the start of a UTC second and repeats at the start of every period. All data acquiring IP cores synchronize their acquisition to this start timeslice signal, and all acquired data are sectioned and time stamped relative to it. Second, the state machine is responsible for gathering the acquired data and merging the UTC time of the timeslice start signal, called the super time, to the acquired data. By combining the relative timeslice time and the super time, the UTC time for all acquired data can be resolved by the onshore data acquisition system. Once the acquired data are ready, the last responsibility of the state machine is to package the data to be dispatched toward the user datagram protocol (UDP) packet generator (IPMux). The data are portioned into frames such that they will fit within the payload of a UDP jumbo packet. A frame header containing metadata, such as the stream identifier or the run number, is also prepared.

2.2.4 *Time-to-digital converter*

The TDCs sample the signals from the PMT bases. They are implemented in the CLB FPGA programmable logic with one TDC channel per PMT, totaling 31 IP cores. The cores measure both the pulse arrival time and the duration of the pulse (ToT) using the 1-ns precision UTC WRPC time. The distribution of the ToT data readout as measured by one DOM is shown in Fig. 7. The TDC core produces 48 bits per event, where the first eight most significant bits are used for the PMT identifier and to store the status of the high rate veto (HRV) and first-in first-out (FIFO) full condition, the next 32 bits code the arrival time of the event with respect to the timeslice start time, and the last eight bits code the duration. The events are then dispatched to the state machine, which also organizes the TDC acquisition in timeslices.

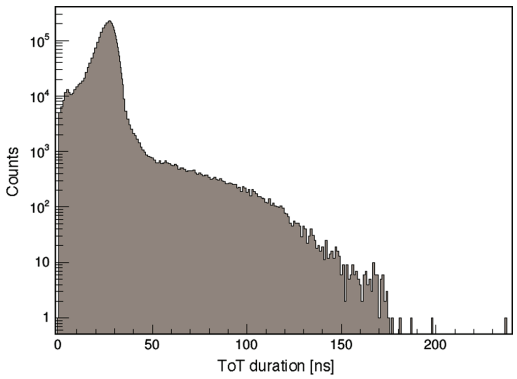

Fig. 7 ToT distribution from one DOM of a deployed KM3NeT DU. All the channels have been calibrated in order to harmonize the ToT data arriving from different PMTs. The represented data correspond to both background and muons. The calibration process consists of tuning the HV until an spe provides a ToT between 26 and 27 ns. This ToT corresponds, on average, to a gain of 3×10^6.

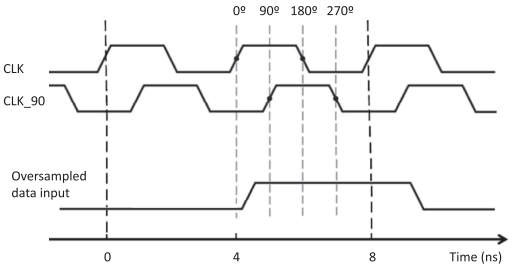

Fig. 8 Oversampling technique using two phase-shifted clocks. Technique implemented in the CLB TDCs.

The system clock of the FPGA firmware is derived from the 25-MHz hardware quartz oscillator in the PCB. This clock signal is first transferred to a digital PLL to generate the system frequency of 62.5 MHz. The WR protocol adjusts the phase and frequency of the FPGA system clock to the reference master clock. Finally, the adjusted system clock is fanned out to the inner PLLs within the FPGA to provide two high frequency clocks of 250 MHz with a phase shift of 90 deg. The TDC input signals are oversampled at a 1-ns rate using the rising and falling edges of the two clocks of 250 MHz as shown in Fig. 8.

The information of the sampling is organized by the TDCs, where the arrival time and the pulse length are coded. As with all other CLB IP cores connected to the LM32 soft CPU, the TDC core is controlled by the LM32 itself, allowing for enabling/disabling any of the 31 TDC channels.

The TDCs implement the HRV and multihit features. The HRV limits the total number of acquired hits in a timeslice. If the number of events in a TDC channel surpasses a predetermined threshold, the acquisition is stopped in that channel until the start of the next timeslice. In this way, it is possible to limit the amount of data sent onshore, preventing blockage of the data acquisition. The multihit option allows to expand the range of the TDCs, limited by the ToT codification of eight bits. If this option is active, then the hits with a ToT longer than 255 ns are coded as two or more consecutive events.

2.2.5 *Acoustic readout*

The CLB also includes a core for the readout of the acoustic piezo sensor,[21] one of the positioning instrumentation devices installed in the DOM. This core reads out the acoustic piezo channel data and time stamps it with respect to the WRPC time. In addition, it generates from the raw acoustic data an AES3 formatted stream, which is dispatched to the state machine.

2.2.6 *IPMux*

The packets created by the state machine are sent to one of the input ports of the IPMux, an IP/UDP packet buffer stream selector. The IPMux has different input ports for each data source. For each packet received from the state machine, a UDP header is added. By using the Ethernet jumbo frames, a maximum transfer unit of 9014 bytes per frame is possible, consequently

reducing protocol overhead significantly when the channel is fully occupied.

The IPMux receives also data from TDCs, the acoustic readout, the monitoring, and the slow control LM32 channels. All of them are aggregated on the IPMux and transferred to the WRPC endpoint, where they are routed through the WR core and sent onshore. Once they arrive on shore, it is possible to discriminate any of the sources of the IPMux (optical, acoustic, and monitoring channel) by the port number.

2.2.7 *Monitoring channel*

The monitoring channel enables transmission of metadata synchronous with the TDC and AES3 channels. However, unlike the TDC and AES3, the monitoring channel is not data driven and produces only one packet of content at the timeslice start signal. The header of the packet provides information regarding the TDC FIFO buffer. The monitoring packet consists of two parts. The first part is delivered by programmable logic, containing additional summary information concerning the TDC channel, such as the actual number of hits per channel. The content of the second part is software defined. At initialization, the programmable logic is provided with a pointer to a software-defined structure. For each timeslice, the content of this structure is combined before dispatching to the state machine.

The software provides additional information such as the latest reading from the compass and tilt sensor. Information about the state of the buffers and other system information is also inserted into this packet.

2.2.8 *Multiboot core*

On startup, the FPGA configures itself by loading the first valid image it finds while scanning the SPI flash memory. Up to four images can be stored in the flash memory at subsequent memory locations, reserving the memory regions above those images for storage of settings and logging. The multiboot gives access to the internal Xilinx specific ICAP2 hard-IP block, which allows software-initiated reconfiguration of the FPGA at any memory offset. The multiboot is an essential part of the two-stage startup sequence used for fail-safe startup of the CLB. The multiboot mechanism is described in Sec. 2.3.3.

2.3 *CLB-Embedded Software*

The FPGA contains two LM32 processors, the WRPC LM32 and the second LM32. Both run a separate software stack. The WRPC LM32 software was developed by the WR Collaboration,[22] but it has been adapted to the KM3NeT network topology. The second LM32 controls the DOM. The software has been developed by the KM3NeT collaboration and designed as control software for the KM3NeT detector. The latter software is discussed in the following sections.

2.3.1 *Main tasks*

The KM3NeT-embedded software handles the following tasks:

- Initializing, controlling, and monitoring hardware.
- Executing commands issued from the onshore station.
- Sending diagnostic information back to shore.
- Applying firmware updates.

A representation of the hardware directly coupled to the second LM32 is shown in Fig. 9. Most of the components inside the dashed line are programmable logic cores, including the CPUs. The hardware devices lie outside the dashed line boundary. Almost all cores are mapped into the memory space of the LM32. The embedded software reads from or writes to specific memory locations, depending on the device addressed. Outside the dashed lines in Fig. 9, the hardware is controlled through external integrated circuit (IC) buses such as I^2C or SPI. The interfaces require an additional layer of drivers to communicate with these devices.

2.3.2 *Software generalities*

The software running in the CPU is primarily coded in C, but some bootstrap and interrupt handling code has been written in LM32 assembly. There is no preemptive embedded operating system, but just a simple kernel capable of executing different tasks in a collaborative fashion. The layered structure of the main modules of the software stack is shown in Fig. 10.

The common layer contains functions and objects used throughout the software. They are not specific to the LM32 platform and could be compiled for any architecture. For example, the logging facilities are placed in this layer. The platform layer

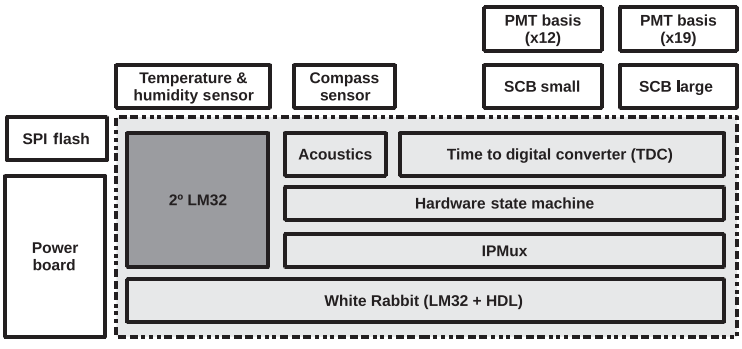

Fig. 9 Embedded software location with respect to the main components of the CLB, shown in gray. The dashed line shows the boundaries of the FPGA.

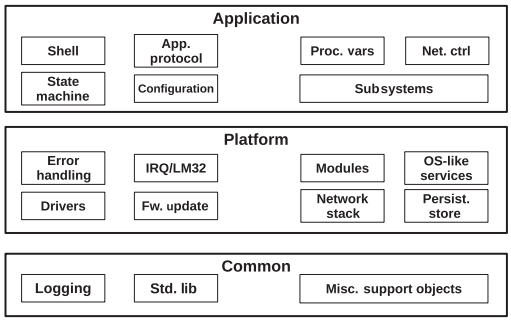

Fig. 10 Layers and modules of the CLB embedded software.

contains all the code required to control the LM32 and all the connected hardware. It consists of hardware control, operating system like services, and the network stack. It does not contain application functionality, but it provides convenient functions for the application layer to control and monitor the hardware. Finally, the application layer contains the high-level functionality of the software. It interprets and executes remote commands, configures and monitors the hardware, and implements the software state machine.

2.3.3 *Firmware update and multiboot*

As explained in Sec. 2.2.8, the embedded software has, through the multiboot core, the capability of configuring the FPGA from any image located in the serial flash. For the CLB, the flash may contain up to four separate configuration images, starting at address 0 with the startup image, also known as the golden image. The subsequent image is the runtime image, then two possible backup images or test images follow. After this, the space is reserved for settings and persistent logging. The remaining area of the flash is reserved for storing custom debug and diagnostic information. The complete flash layout is shown in Fig. 11.

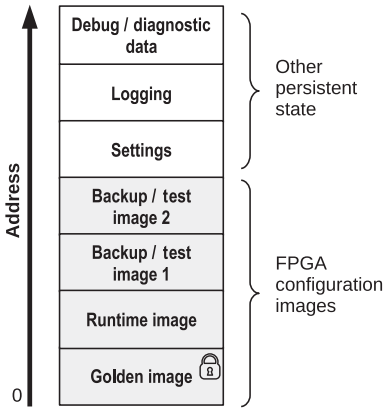

Fig. 11 Content of the serial flash memory. The golden startup image starts at address 0, followed by the primary runtime image, and two backup images. The remainder of the memory contains various types of persistent states.

The golden image is a special image with minimal hardware initialization. The memory region occupied by the golden image is protected from accidental overwrite by the write protection feature part of the flash controller. The golden image will start by default a preselected image, usually the runtime image, 30 s after a network connection has been established. In exceptional conditions, the startup procedure can be aborted from shore in the 30-s window. The golden image also provides access to diagnostic and recovery features. Each image on the flash can be updated by remote, including the golden image. However, the latter is an exceptional case and should be avoided. To deal with such cases, a precise and safe procedure has been prepared, which safeguards against accidental loss of CLB due to lack of valid images in the flash. The procedure requires that at least one valid image is always present in the serial flash, even during update.

3 Power Board

The power board,[23] shown in Fig. 12, provides power to the CLB and the full DOM. The schematic view of the power board functionality is shown in Fig. 13. The input supply to the power board is 12 V. Six regulated voltages (1, 1.8, 2.5, 3.3, 3.3 V PMT, and 5 V) are generated from the 12-V using dc/dc converters. The 1, 1.8, 2.5, and 3.3 V outputs are used by the CLB to supply the FPGA. The 3.3-V PMT output supplies the 31 PMT base boards and the 5-V voltage is used to supply the acoustic piezo sensor. Moreover, the power board provides another output, settable via an I^2C digital-to-analog converter (DAC), which results in a configurable voltage ranging from 0 to 30 V. The settable channel is used by the nanobeacon. The power board uses high-efficiency dc/dc converters in order to minimize the power consumption in the DOM. The efficiencies of these dc/dc converters are listed in Table 1.

In order to protect the sensitive electronics inside the DOM from the interferences by the high frequency noise produced by the dc/dc converters, the power board is located in the shielded part of the cooling mushroom. The chosen location also provides a better cooling of the power board. The location of the power board in the DOM is shown in Fig. 2.

3.1 *Power Startup*

One of the functions of the power board is to provide a proper voltage startup sequence to the FPGA. For this purpose, a sequencer has been implemented in the power board in order to provide the needed sequence of voltages.[24] The sequence of voltages generated by the power board is shown in Fig. 14. Two

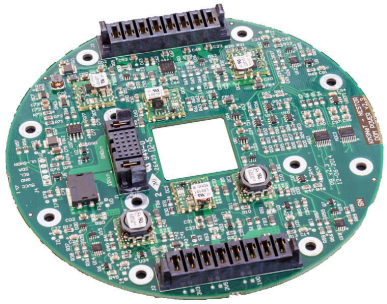

Fig. 12 The DOM power board, having a diameter of 130 mm.

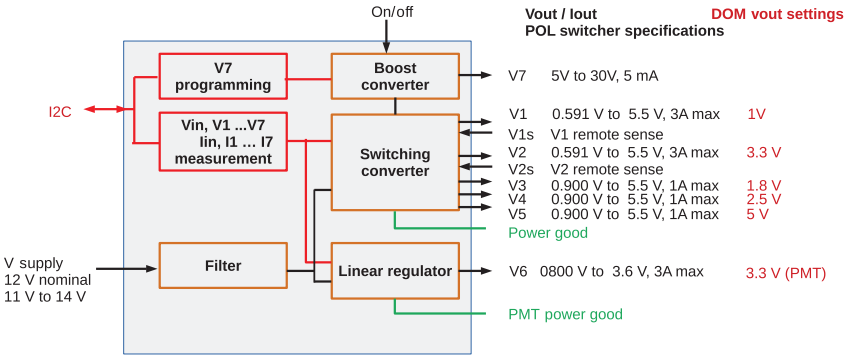

Fig. 13 Block diagram of the power board functionality. The specification of the dc/dc converters is presented for each power rail. The linear regulator included in the power board is used to provide a stable voltage to the PMTs.

Table 1 Power board efficiency for each output voltage.

V (V)	*I* (A)	Type of dc/dc	Efficiency (%)
2.5	0.13	OKL-1	60
3.3	0.33	OKL-3	65
3.3	0.34	OKL-1	90
1.0	0.80	OKL-3	80
1.8	0.46	OKL-1	80
5.0	0.10	OKL-1	60

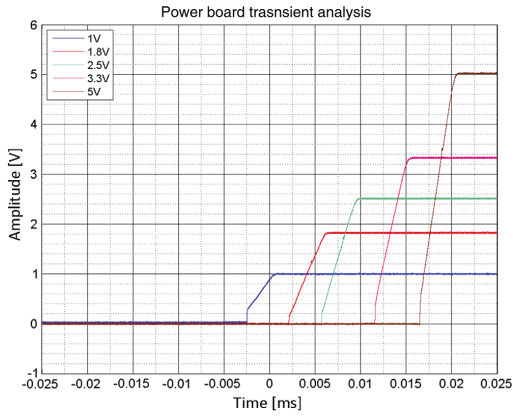

Fig. 14 Power up sequence. The picture corresponds to an oscilloscope capture. The oscilloscope trigger, set to 0.9 V, fixes the time reference.

power-good signals are generated by the power board. The first one indicates that the 3.3-V PMT output has been successfully started (power-good PMT). The second one indicates the successful completion of the power up sequence. The final function

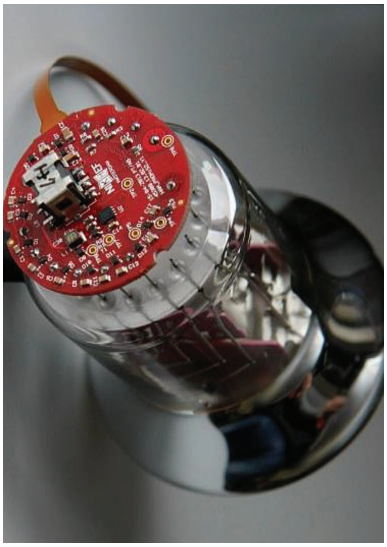

Fig. 15 The PMT base board mounted on a 3-in. PMT.

implemented in the power board is a hysteresis loop to avoid instabilities at the startup. The regulators of the power board are enabled only when the input voltage exceeds 11 V, whereas they are disabled when the input value drops below 9.5 V. In this way, fluctuations in the power board regulators are avoided at the start point of the input voltage.

4 Photomultiplier Base

The PMT base board[25] (see Fig. 15) takes care of both the generation of the HV supplied to the PMT and the digitization of the PMT signal. Before being digitized, the PMT signal is amplified by a preamplifier built in the PMT base. One of the main components of the PMT base is a comparator, which provides a logical high signal when the PMT output is over the comparator threshold—set through I^2C. The duration of the primary signal

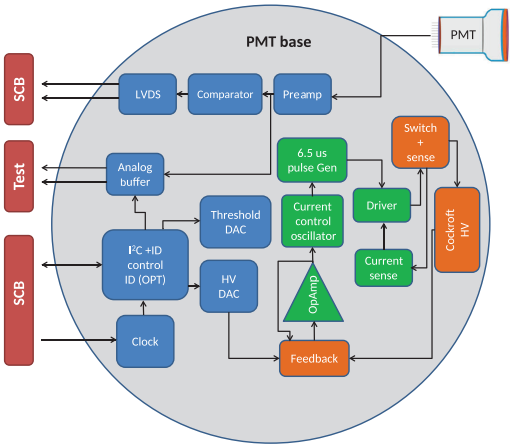

Fig. 16 Block diagram of the PMT base. CoCo subsystems are represented in green, front-end mixed signal ASIC (PROMiS) subsystems are represented in blue, while discrete components are represented in orange.

(ToT) provided by the PMT bases is accurately measured by the CLB TDCs. In addition to the logical signal, the PMT base also outputs the amplified analog PMT signal, which is only used for testing. The 31 PMT base boards are connected to the SCB by a flexible PCB. The HV, which is remotely configurable through I^2C, is independently generated in each PMT base. This allows for tuning the gain of individual PMTs in order to equalize cross-PMT photon response to provide a ToT range of 26 to 27 ns for single detected photons. The HV value can be adjusted remotely, from −800 to −1400 V. The PMTs are directly coupled to an external circuit, therefore, a negative HV is used.[26] The HV is generated by a Cockroft Walton (CW) voltage multiplier circuit driven by a flyback converter. The output of the voltage multiplier circuit is used to drive the dynodes of the PMT. A diagram of the PMT base board with its main components is shown in Fig. 16.

4.1 *Photomultiplier Base ASICs*

In order to reduce the space occupied by the PMT base, as well as its cost and power consumption, two application-specific integrated circuits (ASICs) have been developed.[27] As the DOM is tightly packed with the 31 PMTs and the electronics, compactification is crucial. The first ASIC is the so-called PROMiS ASIC, which performs the readout of the PMT signals and has two different parts, one digital and one analog. The second chip is the CoCo ASIC, which controls the Cockroft–Walton HV power supply providing a target gain in the 10^6 range. The main characteristics of both ASICs are listed in Tables 2 and 3.

4.1.1 *PROMiS analog block*

The analog section of the PROMiS ASIC includes a preamplifier, which can increase the amplitude signal of the PMT; a two-stage charge amplifier biased at 1 V (feedback: $R_f = 15$ kΩ, $C_f = 300$ fF); and a discriminator that compares the input signal with a predefined threshold level configured by I^2C. The PROMiS ASIC generates the LVDS signal. The signal is

Table 2 Specifications of the PROMiS chip.

Time resolution (for a single photon, photomultiplier + electronics)	<2 ns
Two-hit time separation	≥25 ns
Power consumption	35 mW
Supply voltage, technology	3.3 V, 0.35 μm CMOS AustriaMicro Systems (AMS)
Comparator threshold adjustment	8 bits (0.8 to 2.4 V)
HV feedback control	8 bits (0.8 to 2.4 V)
Slow-control communication, digital and analog output	I^2C, LVDS, and analog buffer, respectively

Table 3 Specifications of the CoCo chip.

Pulse output frequency	<50 kHz (max.)
Pulse width	<6.5 μs (max.)
Power consumption	<1 mW
Supply voltage, technology	3.3 V, 0.35 μm CMOS AMS
Current sense	100 mV over 1.5 Ω
Operational amplifier reference (internal)	1.2 V

transmitted via the SCB to the CLB where it is digitized by the corresponding TDC. The LVDS driver, with common mode feedback, feeds the 100 Ω kapton-insulated transmission line. The 1.2-V reference voltage is produced by a band-gap voltage reference. From this reference voltage, all the remaining voltages and currents used in the ASIC are generated. Figure 17 shows the block diagram of the ASIC.

4.1.2 *PROMiS digital block*

The PROMiS ASIC includes, in its digital block, an I^2C slave and one-time programmable memory block where a unique identifier of the chip is stored. In Fig. 17, the block diagram of the PROMiS ASIC, including its digital part, is shown. In order to save power, it is possible to shut off the clock via an enable/disable signal. The ASIC provides both the possibility to test the analog chain via I^2C and to switch on and off the HV circuit. In addition, it includes a clock generator that produces a 10-MHz clock signal with possible fluctuations due to temperature and voltage up to 30%. The clock accuracy is not critical as it is used by the I^2C interface, whose bus operates at 250 kHz.

4.1.3 *CoCo: Cockroft Walton multiplier feedback control ASIC*

The CoCo ASIC (see block diagram in Fig. 18) controls the autotransformer of the PMT base. The autotransformer, which has a ratio of 1:12, couples the 3.3-V power supply provided by the SCB to the CW multiplier circuit. The CW multiplier circuit generates the stable HV needed by the PMT. The logarithm of

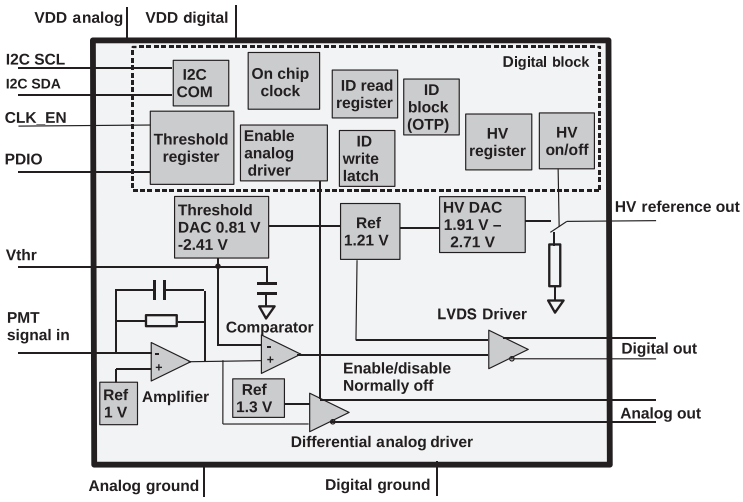

Fig. 17 Diagram of the PROMiS chip.

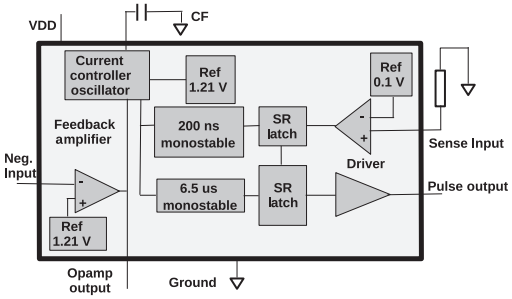

Fig. 18 Block diagram of the CoCo chip.

the PMT gain has a linear response to the HV. The ASIC receives feedback from the CW multiplier circuit in order to accurately control the HV. The control is performed by a series of pulses to the switch that is managing the autotransformer. The characteristic pulse width is 6.5 μs and its frequency, which determines the HV, changes according to the HV feedback. The HV feedback voltage is used for charging (or discharging) a capacitor. The value of the capacitor, loaded by the current of the HV feedback, sets the frequency. The triangular wave created by the charge and discharge of the capacitor is also used for generating internal clocks. Another function of the HV feedback is to avoid the autotransformer saturation in case of short circuit.

The relation between the PMT DAC value and the actual produced HV is shown in Fig. 19. The relation between the DAC value and the output voltage can be derived from the PMT base HV circuit and is given as

$$V_{\mathrm{HV}} = -F\left(V_{\min} - V_{\mathrm{ref}} + D\frac{V_{\max} - V_{\min}}{255}\right) + V_{\mathrm{ref}}, \qquad (1)$$

where D is the DAC value (0 to 255), V_{ref} is the reference voltage generated by the Cockroft Walton multiplier feedback control ASIC (1.21 V), $V_{\min}$ and $V_{\max}$ are the minimum and maximum output voltages of the DAC (1.91 and 2.71 V, respectively), and F is the feedback path voltage divider factor, which has been set to 1000. V_{HV} is the HV generated by the circuit. From this, it follows a range variation of the design output between -698.8 and -1498.8 V for DAC values 0 and 255, respectively. The observed variation among a sample of PMT bases in Fig. 19 is due to resistor tolerances present in the feedback loop, which total to a maximum of $\pm 6\%$. The nonlinearity and general offset with respect to the design voltage in the plot is due to the inherent error of the measurement method.

5 Signal Collection Board

The PMT base-generated LVDS signals are collected on a hub board, called the SCB. The main function of the SCB is to transfer the signals from the PMT base to the TDCs embedded in the CLB. The SCB also transfers the I^2C command signals from the CLB to the PMT bases in order to monitor and control the PMTs. Each DOM comprises two SCBs, one large and one small [Fig. 20(a)]. Figure 20(b) shows one SCB connected to the PMT bases in half a DOM. The architecture of the SCB consists of the following parts:

- Backplane connector to the CLB.
- Xilinx Coolrunner complex programmable logic device (CPLD).
- I^2C multiplexer.
- Current limit switches.
- PMT channels: 19 in the large SCB and 12 in the small SCB.
- One piezo connector (only in the large SCB).

LVDS signaling, as used between the PMT base and the CLB, is less susceptible to cross-talk due to the fact that the two

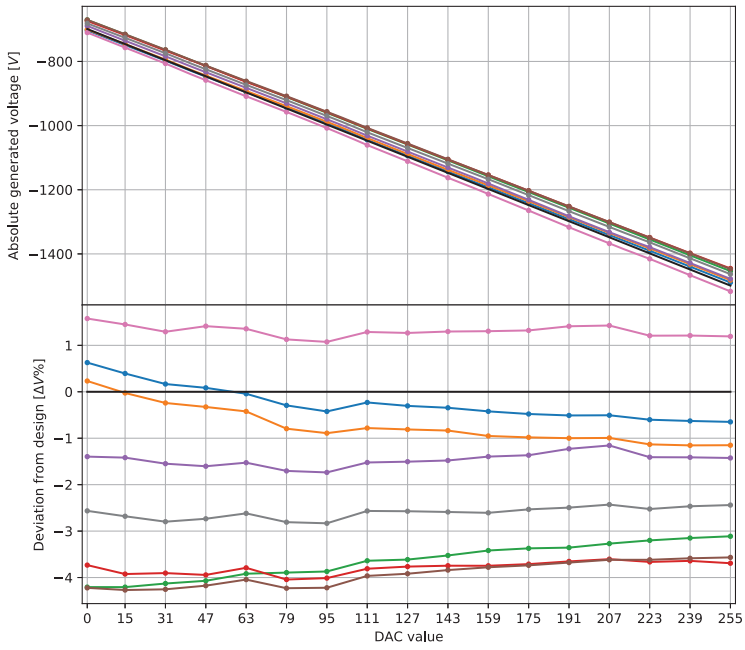

Fig. 19 HV produced by a sample of PMT bases against a set PROMiS DAC value. The top plot shows the absolute voltage for eight selected bases, while bottom plot shows the relative deviation from the design voltage, where $\Delta V\% = (V_{\mathrm{DAC}} - V_{\mathrm{design}})/V_{\mathrm{DAC}} \times 100$. The black line represents the design value.

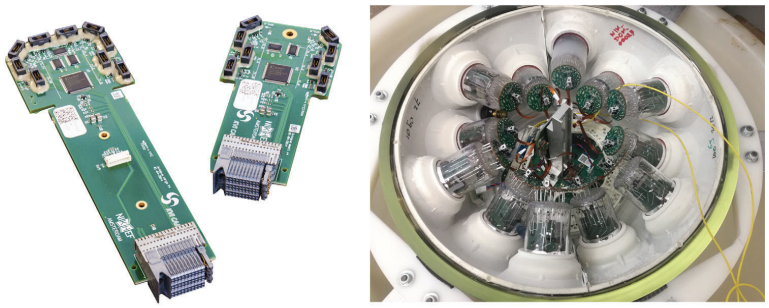

Fig. 20 (a) Small and large signal collection boards. (b) Small SCB mounted next to the cooling stem, connected to 12 PMTs inside the top half of a DOM.

signal lines of the LVDS are electrically tightly coupled with matched impedance throughout the complete route from the PMT base to the CLB. The signal that can be coupled into the LVDS line will be coupled into both signal lines at the same time. Because of this, the distortion becomes common mode and will not affect the signal integrity. For each PMT, a resettable fuse IC, integrated on the SCB, protects individual PMTs and the CLB from short circuit or excessive current draw. For control and monitoring of the SCB, a CPLD, accessible through I^2C, has been added. The CPLD allows for reading and resetting the current sensors and disabling the PMT base digital clock to eliminate possible interferences from this clock on the PMT signals. The acoustic piezo sensor is also connected to the CLB via the large SCB. As in the case of the PMTs, the SCB supplies the piezo with the needed voltage and transfers the acquired data from the piezo sensor to the CLB. The piezo does not feature a control interface.

The large SCB has 19 equal channels (see Fig. 21). The LVDS signals and the 5 V needed to supply the acoustic piezo sensor are connected from the backplane connector to the piezo connector.

The 5-V power is not measured and cannot be switched by the SCB. The small SCB has 12 PMT channels and three spare channels.

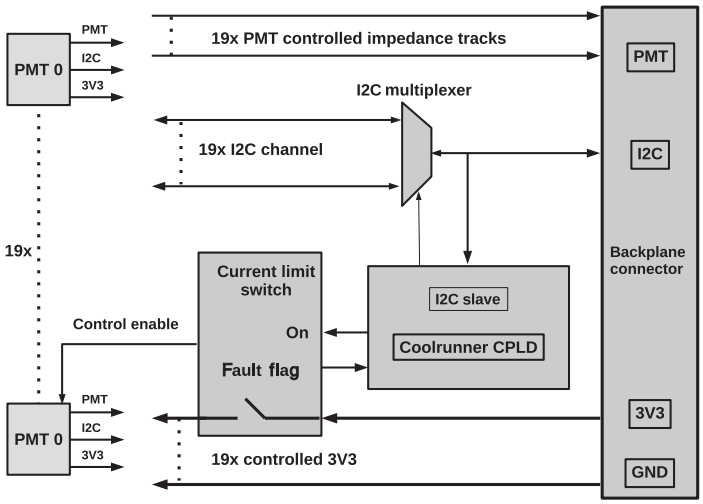

Fig. 21 Block diagram of the 19 PMT channel interface of the large SCB. The small SCB is analogous with only 12 channels.

6 DOM Power Breakdown

The power consumption breakdown of the most consuming DOM electronics boards is shown in Table 4. The component of the DOM with the highest power consumption is the CLB. Inside the CLB, the FPGA and the SFP are the main power consumers, followed by the clock conditioner and the nanobeacon. The nanobeacon is only operated when a calibration run is performed, typically a few minutes once a week.

The SCB consumption is negligible and the 31 PMT bases add up to a total of 1 W. The power board, mainly because of the dc/dc converter losses, accounts for 10.2% of the total DOM power consumption. In total, the power consumption of the DOM is around 7 W when fully operational. Keeping the power drain low is important both for keeping the overall consumption of the detector low and minimizing the heat production.

Table 4 DOM measured power breakdown.

Power breakdown		
Board	Subcomponent	Power (W)
Power board		0.72
CLB		4.45
	FPGA	*2.25*
	SFP	*1.50*
	Clock conditioner	*0.50*
	Tilt and compass	*0.20*
Small SCB		0.02
Large SCB		0.02
PMT 31×		1.05
Digital Piezo		0.50
Total power consumption		6.76

7 Reliability

Maintenance of DU operated in deep seawater is difficult. In order to quantify the reliability of the electronics boards used in the detector, the FIDES[28] method is used. The FIDES methodology provides two main engineering tools. The first one consists of a handbook for predicting the reliability of the electronic boards analyzed. The second one is a guide to estimate the impact of the design and manufacturing processes on the reliability of the produced boards. FIDES provides a spreadsheet tool to calculate the failure in time (FIT) and the mean time to failure (MTTF) of an electronics board. Given a board, each of its components is assigned an FIT, which is either provided by the manufacturer or obtained from the FIDES handbook. The final FIT of a board is the sum of the FITs of each single component and estimates the failure rate per 10^9 hours. Once the FIT is obtained, it is possible to calculate the probability of failure in a given time as $F(t) = 1 - R(t)$, with $R(t)$ the probability of a system to still be operational over a time period t. $R(t) = e^{-\lambda t}$, where λ is the board FIT value and t the time period duration in hours.

The results obtained for the DOM electronics boards are presented in Table 5. To fully quantify the reliability of the boards, it is necessary to evaluate each subsystem included in order to exclude, from the total FIT, those subsystems that are not critical or do not affect the overall performance of the detector in case of failure. The evaluation is called the failure mode, effects, and criticality analysis (FMECA). In the case of the power board, FMECA analysis has shown that the failure of the nanobeacon and piezo power supplies has no impact in the overall physics performances of the KM3NeT detector, because there is enough redundancy. Once adjusted, the power board FIT reduces to 947. The results obtained by the FIDES method show that the

Table 5 FIT and MTTF of the DOM electronics boards of KM3NeT. FIT is defined as the number of failures per 10^9 h.

Product	FIT	MTTF (years)
PMT base	1218	94
Large SCB	157	727
Small SCB	156	731
Power board	1424	80
CLB	417	273

electronics boards in the DOM comply with the quality levels required by the KM3NeT collaboration.

8 Conclusions

In this paper, the electronics front-end and readout system of the KM3NeT telescopes has been presented. The main electronics boards inside the optical modules: the CLB, the power board, the PMT bases, and the SCBs—have been described in detail, including a description of the readout architecture of the front-end electronics. A challenging requirement of the readout system is the 1-ns accuracy of the synchronization of the clocks inside the individual optical modules deployed in a water volume of about one-cubic kilometer scale. An additional challenge is the power budget of maximal 7 W, including the HV of the 31 3-in. PMTs. The full chain of the readout electronics has been successfully qualified *in situ* during a data-taking period from May 2014 to July 2015 at a depth of about 3500 m. The qualification has shown that a sustainable synchronization of 1-ns accuracy between the clocks in the individual optical modules has been achieved. Currently, the first deployed DUs, using the first batch of mass-produced DOM electronics, have been taking data successfully, thus demonstrating the functionality of the KM3NeT front-end and readout electronics system.

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Vincent van Beveren is a PhD candidate and embedded software engineer at the National Institute for Subatomic Physics Nikhef. He received his BS degree in computer science and information technology from the Hogeschool Utrecht in 2004. He has collaborated on multiple publications on various topics. His areas of expertise are ultralower power embedded systems, digital signal processing, and internet of things.

David Calvo is a PhD candidate and research engineer at the Instituto de Física Corpuscular of Valencia. He received his MS degree in computing from the University Jaume I in 2006, his MS degree in electronics from the University of Valencia in 2009, and his MS degree in electronic systems design from the Polytechnic University of Valencia in 2012. His research interests are focused on digital electronics, synchronization, and readout acquisition systems. He is the author of several publications on electronics.

Diego Real is a PhD candidate and research engineer at the Instituto de Física Corpuscular. He received his BS degree in electronics in 1996 and his MS degree in control and electronics in 2000, both from the Polytechnic University of Valencia. He is the author of several publications on electronics. His current research interests include acquisition and synchronization systems for particle physics. He has been the electronics project leader of the KM3NeT telescope and a member of the technical advisory board of the GVD-Baikal telescope since 2013.

Biographies of the other authors are not available.