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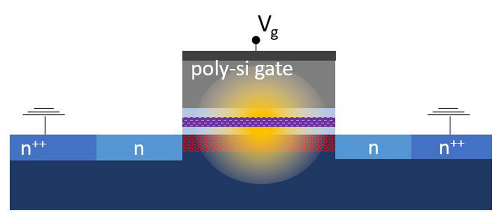

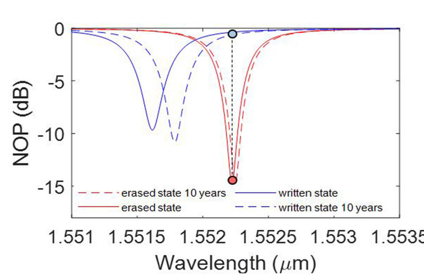

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Abstract: The non-volatile memory is a crucial functionality for a wide range of applications in photonic integrated circuits, however, it still poses a challenge in silicon photonic technology. This problem has been overcome in the microelectronic industry by using SONOS (silicon-oxide-nitride-oxide-silicon) memory cells, in which the non-volatility is enabled by a dielectric trapping layer such as silicon nitride. Analogously, in this work, a similar approach in which the nitride has been replaced by a hafnium oxide layer, named as SAHAS configuration, is proposed for enabling a programmable erasable photonic memory fully compatible with the silicon platform. The structure features an efficient performance with writing and erasing times of 100 μs, retention times over 10 years and energy consumption in the pJ range, which improve the current SONOS or floating gate based photonic approaches that exploit the plasma dispersion effect in silicon. The proposed non-volatile photonic memory device shows an extinction ratio above 12 dB and insertion losses below 1 dB in a compact footprint. In addition, because the memory is optically read, ultrafast access times in the picosecond range are also achieved.

Index Terms: Silicon photonics, photonic memory, non-volatile, integrated photonics, plasma dispersion effect.

1. Introduction

Silicon technology has gradually emerged as the platform of choice when it comes to developing photonic integrated circuits (PICs) due to its potential integration with electronic circuits in the same chip and the possibility of reusing the mature and cost-effective manufacturing infrastructure of the microelectronic industry. In addition, silicon has excellent properties for the development of photonic devices such as high thermal conductivity, high optical damage threshold and the presence of third-order non-linearities [1]. Furthermore, the large index contrast between silicon and silica makes the SOI (silicon-on-insulator) technology a great candidate for developing compact devices. The presence of Raman and Kerr effects joined to the high optical density coming from the large index contrast has made possible optical amplification [2]–[4], lasing [4]–[6] and wavelength conversion [7]–[9] in the silicon platform. However, non-volatile electro-optical memories, which is a crucial functionality demanded by a wide range of applications such as efficient data storage, are still a challenge in this platform. Several solutions have been proposed to overcome this issue, some of

TABLE 1
Comparison With the State-of-the Art in Silicon Non-Volatile Photonic Memory Devices Based on the Plasma Dispersion Effect

TECHNOLOGY	V_{WRITE}	V_{ERASE}	T_{WRITE}	T_{ERASE}	SIM/EXP	Ref.
SONOS	10V	100 V	1s	2s	Simulation	[20]
SONOS	120V	N/A	~ms	N/A	Experimental	[21]
Floating gate	20V	6V	600 ms	225 ms	Experimental	[16],[17]
SAHAS	**21.5V**	**-30V**	**100 μs**	**100 μs**	**Simulation**	**This work**

those relying on the integration of new materials [10]–[15], however, they come with the drawback of not using the standard fabrication process flow of the CMOS industry. On the other hand, a solution for a programmable erasable memory that exploits plasma dispersion effect has been proposed based on a floating gate scheme [16], [17]. Despite the good outcomes of the device, it has some limitations coming from the chosen technology and the complexity of the structure. In fact, the scaling of the tunneling layer is a key issue in floating gate memories: as a consequence of the conductive nature of the polysilicon floating gate, complete memory discharge is caused whenever there is a fabrication defect in the thin tunnel oxide [18], [19]. This issue has been overcome in the microelectronic industry by replacing the floating gate by a charge trapping dielectric such as silicon nitride [18], [19]. In photonics, two works have been reported to date following this approach [20], [21], however, the voltages needed for discharging the device exceed 100 V and the operation speed was in the millisecond range and above. In fact, the most recent one [21] is oriented to ring-resonator trimming instead of memory applications due to the need of UV (ultraviolet) light in order to charge the device.

In this work, we propose a solution for a charge trapping based photonic memory in which hafnium oxide (HfO_2) has been chosen as the charge storage layer due to its higher trap density and aluminum oxide (Al_2O_3) as the blocking and tunnel oxides. The designed structure, named as SAHAS (silicon-aluminum oxide-hafnium aluminum oxide), shows improved writing and erasing capabilities down to the μs regime, which is a crucial point for a practical device, and outperforms in about three orders of magnitude the current state-of-the art of silicon non-volatile devices based on the plasma dispersion effect, as shown Table 1. The writing and erasing processes are carried out by applying voltages of 21.5 V and -30 V, respectively, achieving retention times over 10 years. By embedding the waveguide structure into a ring resonator, a photonic memory device can be achieved. Our simulation results predict extinction ratios above 12 dB and insertion losses well below 1 dB for such device. The design of the charge trapping photonic structure and non-volatile memory device are described in next section. Main results and conclusions are then summarized.

2. A Programmable Erasable Photonic Memory

Conventional SONOS memories are essentially a MOS (metal-oxide-silicon) transistor where the metal has been replaced by a highly doped ($\sim 10^{20}$ cm^{-3}) polysilicon gate and the gate oxide by a ONO (oxide-nitride-oxide) dielectric stack, as shown in Fig. 1(a). The dielectric placed in the middle of the stack, usually silicon nitride, is used to capture the carriers injected from the silicon channel. When trying to reuse this concept for a photonic memory, the ONO stack is placed over the silicon waveguide. Once the silicon nitride is charged by applying a positive voltage to the gate, carriers will accumulate in the waveguide border to screen the stored charge and will change the effective index of the guided photonic mode due to the plasma dispersion effect in silicon. A sketch of the concept is depicted in Fig. 1(b). However, this configuration comes with several limitations. Usually, the metal or highly doped gate is placed relatively far from the photonic guiding structure to avoid high optical losses, leading to an increase in the writing/erasing voltages and a decrease in speed. Furthermore, the low overlap between the guided photonic mode and the accumulated charges limits the effective index change achieved for a given carrier accumulation. To overcome

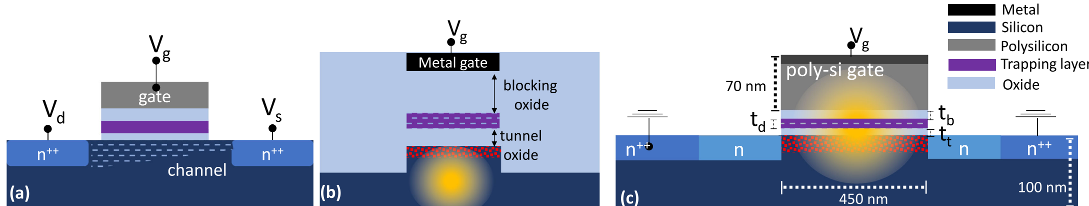

Fig. 1. Sketch of (a) a conventional SONOS memory, (b) SONOS photonic structure used in [21], [20] and (c) proposed SAHAS structure. Sketches are shown not to scale.

these restrictions, the configuration shown in Fig. 1(c) is proposed. In this structure, the mode is partially guided by a relatively low doped polysilicon gate, placing the core of the optical mode right on top of the charge accumulation. In addition, this configuration allows for a more direct voltage application because the gate is placed next to the thin ONO stack.

2.1 Charge Trapping Waveguide Design

The dimensions of the proposed SAHAS trapping structure (Fig. 1(c)) have been designed to optimize the TE polarized optical mode overlap with the carrier accumulation layer. Consequently, gate and slab thicknesses of 70 nm and 100 nm, respectively, have been selected together with a polysilicon width of 450 nm. Moreover, Al_2O_3 has been chosen as the tunnel and blocking oxides due to its higher dielectric constant (ε_r~9 [22]) compared to silica and HfO_2 as the charge storage layer due to its high trap density ranging between 10^{20} cm^{-3} and 10^{21} cm^{-3} [23]. Both materials ensure CMOS compatibility. Drain and source have been heavily doped (n^{++}-type 10^{20} cm^{-3}) to avoid the creation of a Schottky contact and placed 300 nm away from the poly-silicon waveguide to minimize optical losses. A more lightly doped area (n-type $5{\cdot}10^{18}$ cm^{-3}) is extended right next to the polysilicon, as shown in Fig. 1(c). Analogously, the gate has also a highly doped thickness of 20 nm on the top (10^{19} cm^{-3}). Soref equations have been used to obtain the index (Δn) and absorption ($\Delta\alpha$) changes due to the plasma dispersion effect in silicon and polysilicon at $\lambda = 1.55$ μm [24]:

$$\Delta n = -8.88 \cdot 10^{-22} \Delta N - 8.5 \cdot 10^{-18} \, (\Delta P)^{0.8} \tag{1}$$

$$\Delta\alpha = 8.5 \cdot 10^{-18} \Delta N - 6.0 \cdot 10^{-18} \, \Delta P \tag{2}$$

where ΔN and ΔP are, respectively, the electron and hole concentrations. In addition, optical losses of 20 dB/cm have been considered for the polysilicon material [25].

A 2-D simulation software, SILVACO [26], has been used to analyze and design the electrical and optical performance of the structure. SILVACO calculates the tunneling currents through the dielectric stack self consistently and obtains the structure behavior by solving Poisson's and charge continuity equations numerically. The dielectric stack has been modeled as a wide band gap semiconductor and direct and Fowler-Nordheim tunneling currents have been considered to compute the solution. The Poole-Frenkel effect as well as trap-assisted tunneling are known to control the retention behavior of this kind of structures [27]–[31] and have also been included to simulate this process. Nevertheless, it is important to stress that the retention characteristics are also influenced by the creation of extrinsic defects in the tunnel oxide, which cannot be considered through simulation models and makes specially important to control the oxide quality during the fabrication process. In addition, the MOS parameter, which enables Shockley-Read-Hall (SRH), Fermi Statistics (FERMI), and the Lombardi Mobility model (CVT) for transverse field and concentration mobility dependence has been used. All these mechanisms and models are included in the ATLAS package from SILVACO [32]. The values for the parameters involved in the simulations are specified in Table 2.

TABLE 2
Main Parameters Used for the Electrical Simulations

	Symbol	Quantity	Value	Ref.
HfO_2	N_T (cm^{-3})	trap density	$5\cdot10^{20}$	[23]
	ϕ_d (eV)	trap depth	1.5	[33]
	ε_r	dielectric constant	22	[33]
	χ (eV)	electron affinity	2.0	[34]
	E_{gap} (eV)	gap energy	5.8	[33]
Al_2O_3	m*	electron effective mass	0.4	[35]
	ε_r	dielectric constant	9	[22]
	χ (eV)	electron affinity	1	[36]
	E_{gap} (eV)	gap energy	8.8	[36]

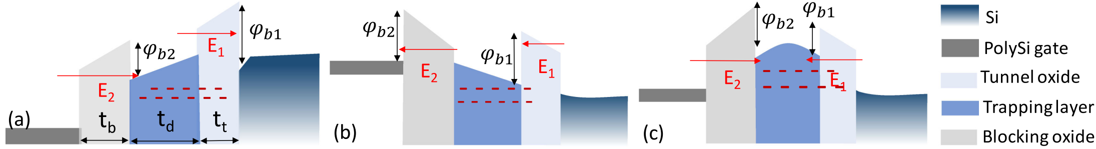

Fig. 2. Band diagram of the (a) writing, (b) erasing and (c) retention processes.

TABLE 3
Design Parameters for the Proposed SAHAS Structure

Symbol	Quantity	Value
t_b (nm)	blocking oxide thickness	6
t_t (nm)	tunnel oxide thickness	6
t_d (nm)	trapping diel. thickness	4

The main variables that will influence tunneling currents, i.e., electric fields E_1 and E_2, blocking (t_b) and tunnel (t_t) oxide thicknesses and tunnel barriers φ_{b1} and φ_{b2} seen by the electrons, are depicted in the band diagram of Fig. 2 for the (a) writing, (b) erasing and (c) retention processes. When a voltage is applied to the gate, an electric field will be created along the dielectric stack. Consequently, there will be two tunneling currents: the desired one through the tunnel oxide to charge and discharge the HfO_2 layer and an unwanted current through the blocking oxide that will inject carriers from and to the gate. Another current, governed by the Poole-Frenkel effect and trap assisted tunneling, will be in charge of moving the electrons across this layer hopping from trap to trap. All dielectric thicknesses must be chosen such that they facilitate the writing process through the tunnel oxide but thick enough to avoid currents through the blocking material and through both oxides during the retention period. The designed parameters of the proposed SAHAS structure are summarized in Table 3. A thickness of 6 nm has been designed for the tunneling oxide, which enables the writing process but, at the same time, avoids excessive charge loss during the retention period. Regarding the charge trapping layer, a thickness HfO_2 of 4 nm has been obtained together with a blocking oxide of 6 nm, which prevents the back tunneling of the trapped carriers.

On the other hand, the writing/erasing speed and stored charge will heavily depend on the doping levels of the silicon slab and polysilicon gate. To better illustrate the situation, Figs 3 (a) and (c) show, respectively, the potential across the structure for the writing ($V_g = 21.5$ V) and erasing (V_g

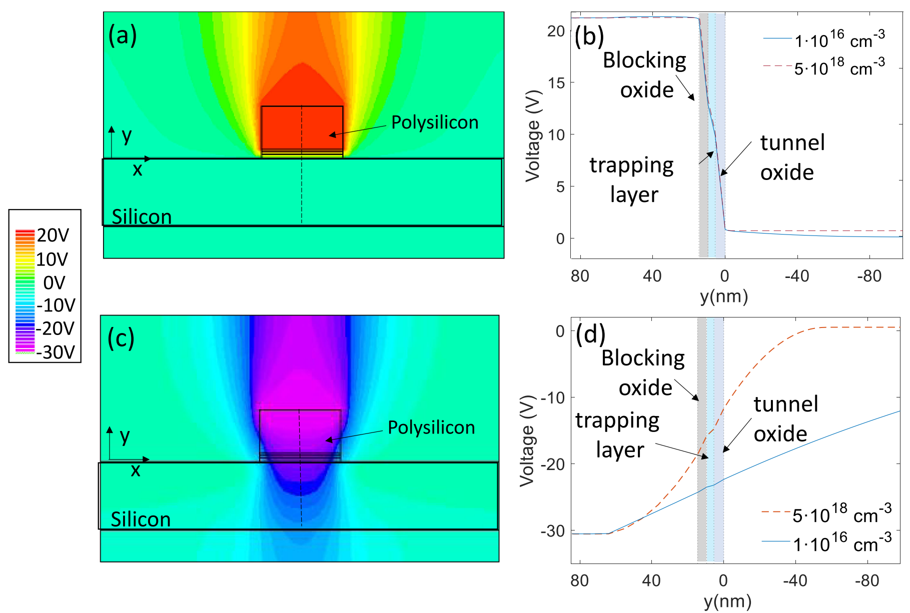

Fig. 3. Contour plot of the potential across the device for (a) the writing state at $V_g = 21.5$ V and (c) the erasing state at $V_g =$ -30 V considering a low doped structure (10^{16} cm^{-3}). Voltage drop along the vertical line depicted in the contour plots for (b) the writing state at $V_g = 21.5$ V and (d) the erasing state at $V_g =$ -30 V for a low ($1{\cdot}10^{16}$ cm^{-3}) and highly ($5{\cdot}10^{18}$ cm^{-3}) doped structure.

= -30 V) processes for a p-type slab and gate with doping concentrations of 10^{16} cm^{-3}. Fig. 3 (b) and (d) show the voltage across a vertical line at the center of the structure during writing and erasing, respectively, for doping levels of 10^{16} cm^{-3} and $5{\cdot}10^{18}$ cm^{-3}. For the writing state, majority carriers easily accumulate on both sides of the dielectric stack and all the applied voltage drops along the dielectrics. However, at the erasing process, minority carriers are not enough to screen the required voltage and a resistive path appears between gate and source/drain. As a consequence, the voltage falls in the semiconductor materials instead of falling in the oxide stack and strongly hinders the discharge process, especially for the low doped structure. By using a higher doping concentration for gate and slab ($5{\cdot}10^{18}$ cm^{-3}), we can improve the performance and a drop of 4 V is achieved inside the tunnel oxide.

Once the carrier and voltage distribution are known, the writing and erasing processes of the HfO_2 layer are calculated and, by using Soref (1) and (2), the effect of the stored charge is translated to the effective index change of the optical mode. In fact, a key feature is the amount of stored charge needed to achieve a given effective index change. This result is shown in Fig. 4 for different gate and slab doping concentrations, demonstrating an approximately linear relationship between both parameters. Moreover, the lower are the doping concentrations of the structure, less charge is needed to achieve the same effective index change and optical losses will also decrease. Thereby, a trade-off must be achieved between the low doping approach and a faster and more efficient programing/erase processes of a highly doped structure.

Using a doping concentration of $5{\cdot}10^{18}$ cm^{-3} for the gate and slightly adjusting it to $3{\cdot}10^{18}$ cm^{-3} at the slab, the writing process can be completed by applying a voltage of 21.5 V to the gate. A maximum stored charge of $7{\cdot}10^{-15}$ C/μm is achieved, as shown in Fig. 5 (a), which is equivalent to an effective index change of $1.5{\cdot}10^{-3}$. The erasing state is accomplished by applying -30 V. Both, the writing and erasing processes, are achieved within a 100 μs time range, however, a small residual charge of around $0.6{\cdot}10^{-15}$ C/μm is left after the erasing process is completed, although it will not significantly affect the device performance. On the other hand, optical losses of 11.28 dB/mm and 8.24 dB/mm are obtained at the two non-volatile states after the writing and

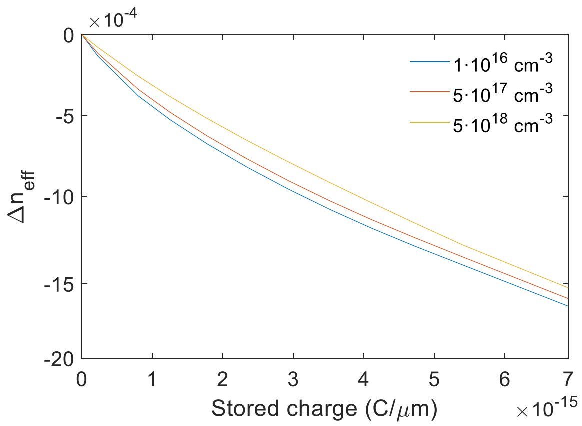

Fig. 4. Effective index change as a function of the stored charge for different gate and slab doping concentrations.

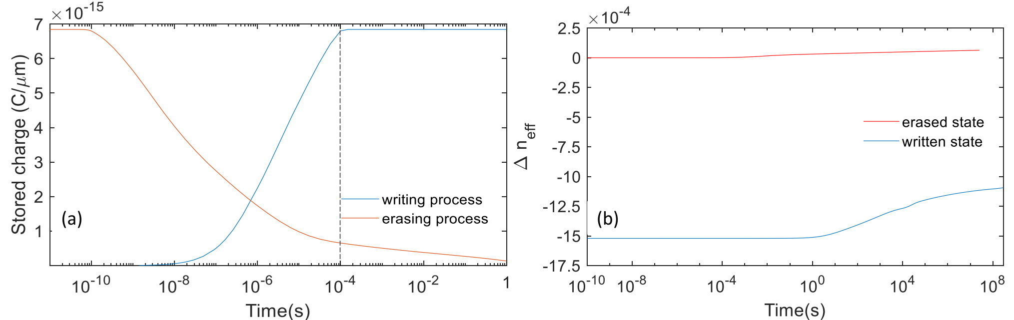

Fig. 5. (a) Evolution of stored charge with time at the writing and erasing processes and (b) retention characteristics of the effective index variation for 10 years.

erasing processes, respectively, which are accomplished with an energy consumption of 1.25 pJ and 5.7 pJ. In addition, the memory structure is also able to work at multiple intermediate stages by decreasing either the time or the voltage applied to the gate. Finally, the retention characteristics have also been analyzed to ensure the endurance of the stored data. As shown in Fig. 5(b), a value for the effective index change above $1.1{\cdot}10^{-3}$ is ensured over a time period of 10 years. A small variability in the erased state is observed during the retention time due to the partial loss of the residual charge, however, the maximum shift corresponds to an effective index change as small as $6{\cdot}10^{-5}$. On the other hand, a more significant variation happens at the written state. Its potential impact on the device performance will be managed through a careful device design to ensure the stability of the optical signal, as it will be explained in the following section.

2.2 Non-Volatile Photonic Memory Device

A functional non-volatile photonic memory device is achieved by making use of the designed charge trapping waveguide structure. Ring resonators are highly versatile devices able to transform the index change to intensity variation in a compact footprint, which makes them the perfect candidate for high density data storage and low energy consumption. Thereby, the proposed SAHAS waveguide structure can be embedded in a ring resonator as depicted in Fig. 6(a). A ring radius of $R = 20$ μm has been chosen with a gap between the bus waveguide and ring to achieve a power coupling ratio of $|k| = 0.15$. In addition, the written state has been chosen to be out-of-the

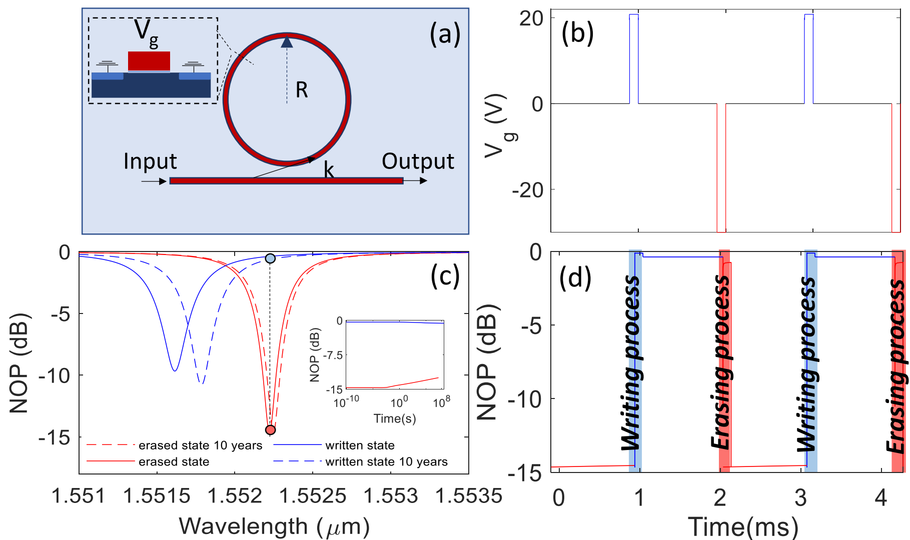

Fig. 6. (a) Sketch of the non-volatile photonic memory device based on a ring resonator, (b) applied voltage vs. time to change the state of the memory, (c) normalized optical power (NOP) showing photonic resonances at written and erased states and (d) corresponding NOP variation with time at the output port.

resonance so that the output power is stable during the retention period. Under these conditions, the resonator device will switch between the written and erased points marked in Fig. 6(c), which shows the resonances for both states at the beginning and at the end of a retention period of 10 years thus demonstrating how the impact of the charge loss in the optical signal is almost completely mitigated. Furthermore, the output power during the retention time is also depicted in the inset, showing a small variation around 2 dB and extinction ratios above 12 dB during the whole period. Finally, the temporal behavior through repetitive cycles is depicted in Fig. 6 (d), which is obtained as a result of applying the voltage pattern shown in Fig. 6 (b). As it can be observed, insertion losses below 1 dB at the written state and extinction ratios near to 15 dB are achieved. Furthermore, the photonic memory device is designed to be electrically written but optically read, therefore, the reading process will be only limited by photon lifetime and would enable reading times in the picosecond range, which outperforms current electronic memories and offers ultra-fast access data storage.

3. Conclusion

A novel configuration has been proposed for a programmable erasable photonic memory that can be electrically written and optically read in the micro and picosecond ranges, respectively. Writing and erasing times, which are a crucial point for practical devices, are improved in three orders of magnitude with respect to current floating gate CMOS compatible approaches for photonic memory applications based on the plasma dispersion effect in silicon [16], [17]. The proposed device is based on exploiting the plasma dispersion effect inside a charge trapping configuration memory cell, which is a well-known building block of the microelectronic industry and widely used for data storage. The HfO_2 has been chosen to work as trapping layer due to its higher trap density. The waveguide memory structure has been embedded into a micro-ring resonator to translate the effective index change into a non-volatile intensity modulation, achieving insertion losses below 1 dB and extinction ratios above 12 dB. The experimental validation of the structure remains as a future work, however, the similarities with the electronic flash memory would ensure maximum CMOS compatibility and therefore the potential for large scale integration at low cost.

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