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Switching Pattern Improvement for One-Cycle Zero-Integral-Error Current Controller

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ABSTRACT The one-cycle current control is a non-linear technique based on the cycle-by-cycle calculation of the ON time of the power converter switches. Its application is not common in tracking fast-changing reference currents, due to the necessity of fast and accurate measurements, and high-speed computing. In a previous study, a one-cycle digital current controller based on the minimization of the integral error of the current was developed and applied to the control of a three-phase shunt active power filter. In the present work, the one-cycle controller has been improved by proposing a new switching pattern. It allows an easy implementation that reduces the critical computational cost and avoids the main drawbacks of the previous implementation. The controller has been applied in a three-leg four-wire shunt active power filter, including a stability analysis considering the proposed switching pattern. Simulated and experimental results are presented to validate the proposed controller.

INDEX TERMS Current control, power converters, one-cycle controller, active filters, power quality.

I. INTRODUCTION

Shunt active power filters (SAPFs) improve the power quality and energy efficiency of electrical systems by compensating the non-efficient current components demanded by loads, represented by unbalanced, reactive and distortion powers [1]–[3]. The SAPF measures the load currents and power network voltages at the point of common coupling (PCC) and generates the non-efficient currents required by the load, as shown in Figure 1. In this way, the power network provides only useful power, improving the power quality and energy efficiency of the electrical system [4]–[6]. SAPF current control methods can be classified into two groups: (i) linear designs based on small-signal SAPF models [7]–[10], and (ii) non-linear designs based on large-signal SAPF models [11]–[23]. Non-linear designs are widely accepted because they avoid performance level degradation when the SAPF does not work close to the linearization point. In [19], a new one-cycle zero-integral-error (OCZIE) current control for SAPFs was designed using the one-cycle control (OCC) approach [13]–[17]. The OCC guarantees that

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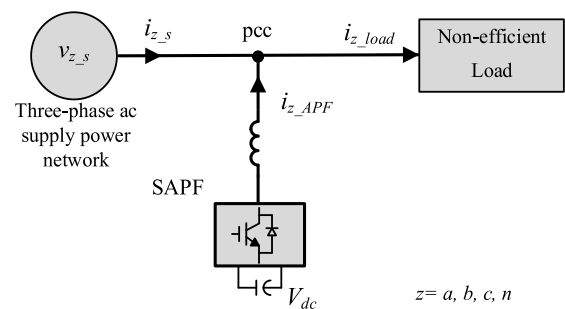


FIGURE 1. Block diagram of the SAPF connection.

the duty cycle is adjusted for each switching cycle to achieve a control objective.

The OCZIE presented in [19] is based on the minimization of the integral error of the current in each switching period. Hence, the proposed control provides, with a fixed switching frequency, a constant performance level of zero current integral error for each switching cycle. As a result, the control provides, in one cycle, the same power as that defined by the current reference.

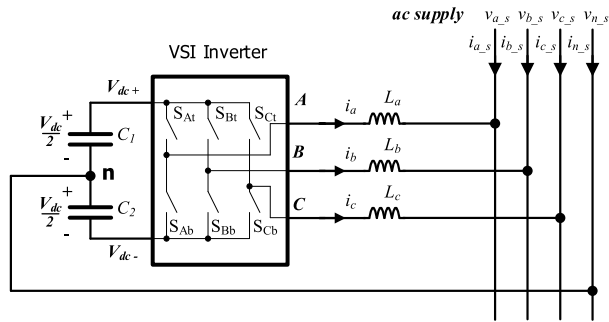


FIGURE 2. Block diagram of a three-leg four-wire grid-tied converter.

However, although the controller presented in [19] was proven to be technologically feasible, an alternating switching pattern strategy was used to achieve a stable behavior. The alternating switching pattern added some technological implementation complexity, as it required not only to detect the zero-voltage crossovers but also to change the switching pattern in real-time, which caused a current surge and transient at the zero-voltage crossovers.

In this article a new OCZIE current control for SAPFs is proposed. The new control avoids the fundamental and technological complexities previously discussed. The controller achieves stable zero-integral-error current control with a single (non-alternating) symmetrical switching pattern. Thus, avoiding the necessity of using two distinct switching patterns in the controller, simplifying the implementation, and mitigating the current surge and the transient instability at the zero-voltage crossovers, improving the overall performance. Conceptualization, design, analysis, and implementation, along with simulated and experimental results, are presented.

The paper is structured as follows. In Section II, the current control problem is presented. In Section III, the proposed controller is derived, and a stability analysis is presented, showing that the control loop is critically stable. Thus, in Section IV the control loop is stabilized by adding a proportional action to the controller. In Section V, the control algorithm is simulated. Section VI shows the experimental setup and obtained results. Finally, Section VII presents the conclusions of this study.

II. PROBLEM STATEMENT

Consider the three-leg four-wire grid-tied power converter presented in Figure 2. The converter operates as a three-phase voltage source inverter (VSI) connected to the AC power network through inductances $L_{(a,b,c)}$. The equivalent series resistance (ESR) of the DC bus capacitors and the resistive part of the inductances are neglected for clarity. The fourth wire connects the neutral wire of the power network to the DC bus midpoint. This power stage configuration is commonly used in SAPFs connected to electrical distribution lines and can be treated as three independent single-phase converters that share a unique DC bus. The VSI switches should be an IGBT–diode association that allows bidirectional current flow. The switches of a branch are controlled

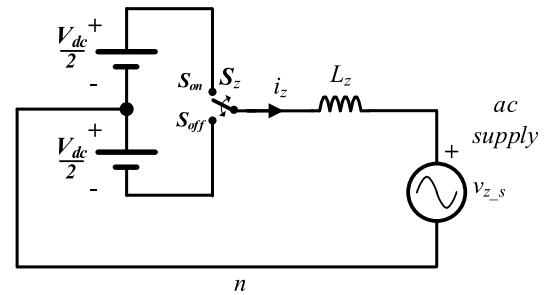


FIGURE 3. Per-phase equivalent circuit of the grid-tied converter.

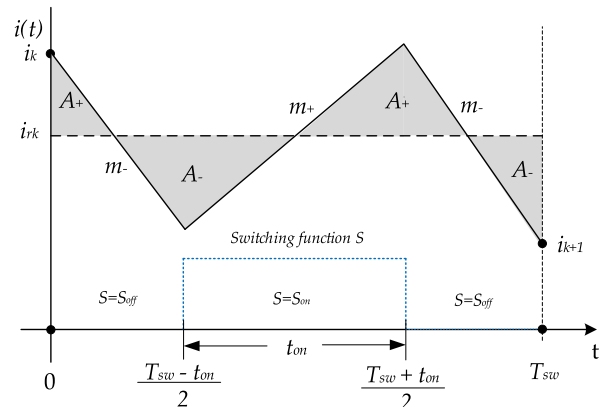


FIGURE 4. Time evolution of phase current $i(t)$ with respect to t_{on} in a switching period.

in a complementary fashion, meaning that at any time, only one switch per branch is in the ON state. Neglecting switching times, also for simplicity, only two states are possible, and the per-phase equivalent circuit of Figure 3 is obtained. The control system should include DC bus voltage regulation, DC bus midpoint voltage-balancing, and AC-side current control.

Consider now the application of one-cycle current control, with a fixed switching period T_{sw} to the circuit shown in Figure 3. The one-cycle control paradigm presented in [17] and [20] is based on computing the control in one switching cycle, as shown in Figure 4. As a result, given an initial current through the inductance (i_k in Figure 4), and a constant current reference value to be tracked (i_{rk}), the problem is to find the ON time (t_{on}) that allows an optimal reference tracking. The subscript z , which refers to the converter phases, is hereafter omitted for clarity.

This work proposes a one-cycle control method that seeks to minimize the absolute value of the current error integral in a switching cycle:

$$\min_{t_{on} \in [0, T_{sw}]} \left| \int_0^{T_{sw}} e(t) dt \right| \quad (1)$$

where $e(t) = i_{rk} - i(t)$. Graphically, the above optimization problem is equivalent to the minimization of the sum of the gray areas in Figure 4. The minimum value of the optimization problem is zero, which is achieved when the positive areas A_+ are equal to the negative ones A_- . If the optimal value is greater than zero, it provides the optimal ON time (t_{on}^*) that minimizes the integral error.

The rationale behind this figure of merit lies in the fact that when the minimum value of the current error integral $e(t)$ is achieved, the mean value of the phase current $i(t)$ over a switching cycle k can be made equal to the reference current (i_{rk}). Note that, given the switching nature of the converter, it is not possible to perfectly track the reference at every instant within a switching cycle.

In the rest of the article, the following assumptions are considered:

1. The reference current i_{rk} is constant during the switching period.
2. For a switching cycle k , when $S = S_{on}$, the phase current $i(t)$ increases with slope m_+ defined as $m_{+,k} = \frac{V_{dc} - v_{s,k}}{L_z}$, which is always positive because $\frac{V_{dc}}{2}$ is always greater than v_s . On the other hand, when $S = S_{off}$ the phase current decreases with slope m_- defined as $m_{-,k} = -\frac{V_{dc} - v_{s,k}}{L_z}$, which is always negative.
3. The slopes m_+ and m_- are assumed to be constant during the switching cycle. For high switching frequencies (in the range of kHz), v_s and V_{dc} are nearly constant for a switching period. Then, slopes m_+ and m_- can be considered constant for the entire switching cycle.

III. ONE-CYCLE ZERO-INTEGRAL

The optimal ON time t_{on}^* is obtained by solving the constrained optimization problem presented in (1), with the current error $e(t)$ defined as follows, (2), as shown at the bottom of the next page, with $e_k = i_{rk} - i_k$ the current error at the beginning of the cycle, (3) as shown at the bottom of the next page.

The optimization problem (1) can be solved analytically by first computing the one-cycle integral error as:

$$\int_0^{T_{sw}} e(t) dt = \int_0^{\frac{T_{sw}-t_{on}}{2}} e_1(t) dt + \int_{\frac{T_{sw}-t_{on}}{2}}^{\frac{T_{sw}+t_{on}}{2}} e_2(t) dt + \int_{\frac{T_{sw}+t_{on}}{2}}^{T_{sw}} e_3(t) dt \quad (4)$$

The integral of the error when the switch is OFF is:

$$\int_0^{\frac{T_{sw}-t_{on}}{2}} e_1(t) dt = e_k \frac{(T_{sw} - t_{on})}{2} - \frac{m_-}{2} \left(\frac{T_{sw} - t_{on}}{2} \right)^2 \quad (5)$$

The integral of the error when the switch is ON is:

$$\int_{\frac{T_{sw}-t_{on}}{2}}^{\frac{T_{sw}+t_{on}}{2}} e_2(t) dt = e_k t_{on} - (m_- - m_+) \frac{(T_{sw} - t_{on})}{2} t_{on} - \frac{m_+}{2} T_{sw} t_{on} \quad (6)$$

The integral of the error when the switch is again OFF is, (7), as shown at the bottom of the next page.

Finally, adding the three integrals yields the following expression:

$$\int_0^{T_{sw}} e(t) dt = \left(\frac{(m_- - m_+) T_{sw}}{2} \right) t_{on} + \left(e_k - \frac{m_-}{2} T_{sw} \right) T_{sw} \quad (8)$$

As a result, the integral of the error is a linear polynomial in t_{on} , defined as $p(t_{on}) = \int_0^{T_{sw}} e(t) dt$, and is given by

$$p(t_{on}) = t_{on} + \underbrace{\left(\frac{(m_- - m_+) T_{sw}}{2} \right)}_m t_{on} + \underbrace{\left(e_k - \frac{m_-}{2} T_{sw} \right) T_{sw}}_n \quad (9)$$

The linear equation $p(t_{on})$ has the following properties:

1. The slope m of the linear equation is negative ($m < 0$) because $m_- - m_+ < 0$.
2. The minimum absolute value of the linear polynomial is $p(t_{on}) = 0$.

The (t_{on}^*) that minimizes $p(t_{on})$ can be obtained by the following procedure:

1. Compute $p(T_{sw})$. If $p(T_{sw}) \geq 0$, the optimizer is $t_{on}^* = T_{sw}$, and the optimal value is $p(T_{sw})$.
2. Compute $p(0)$. If $p(0) \leq 0$, the optimizer is $t_{on}^* = 0$, and the optimal value is $|p(0)|$.
3. Finally, if $\frac{m_-}{2} T_{sw} \leq e_k \leq \frac{m_+}{2} T_{sw}$, the optimal t_{on}^* is obtained by the solution of $p(t_{on}) = 0$, which is given by

$$t_{on}^* = \frac{(2e_k - m_- T_{sw})}{m_+ - m_-} \quad (10)$$

A. CONTROL ALGORITHM

The control algorithm requires the measurement of i_k to compute the current error $e_k = i_{rk} - i_k$. Depending on e_k , the optimal control action to be applied is:

1. If $e_k \geq \frac{m_+}{2} T_{sw}$, then $t_{on}^* = T_{sw}$.
2. If $e_k \leq \frac{m_-}{2} T_{sw}$, then $t_{on}^* = 0$.
3. If $\frac{m_-}{2} T_{sw} \leq e_k \leq \frac{m_+}{2} T_{sw}$, then $t_{on}^* = \frac{(2e_k - m_- T_{sw})}{m_+ - m_-}$.

The following remarks are in order:

4. The optimization problem achieves the minimum value of 0 when $\frac{m_-}{2} T_{sw} \leq e_k \leq \frac{m_+}{2} T_{sw}$. In this case, the control provides the one-cycle zero-integral-error.
5. In the case where $e_k \geq \frac{m_+}{2} T_{sw}$ or $e_k \leq \frac{m_-}{2} T_{sw}$, the minimum value achieved is greater than zero and the one-cycle zero-integral-error property is no longer achieved, although the algorithm still minimizes its value. These cases arise when the value of the error is so large that it saturates the control action (i.e., $t_{on}^* = T_{sw}$ or $t_{on}^* = 0$).
6. In general, the slopes m_+ and m_- are not constant but vary over time in each switching cycle. Hence, the slopes must be updated accordingly in each cycle.

B. STABILITY ANALYSIS

Once t_{on}^* is obtained, a stability analysis is performed. The phase current at the end of a switching cycle i_{k+1} is related to the current at the beginning i_k by:

$$i_{k+1} = i_k + m_+ t_{on} + m_- (T_{sw} - t_{on}) \quad (11)$$

By subtracting (11) from the reference current in one cycle i_{rk} , the evolution of the error is obtained as in (12).

$$\begin{aligned} e_{k+1} &= i_{rk} - i_{k+1} = \underbrace{i_{rk} - i_{ik}}_{e_k} - m_+ t_{on} - m_- (T_{sw} - t_{on}) \\ &= e_k - m_- T_{sw} + (m_- - m_+) t_{on} \end{aligned} \quad (12)$$

The objective is to analyze the error evolution of (12) when the optimal ON time (10) is applied. Substituting (10) into (12) and arranging the terms, the following iterated map is obtained:

$$e_{k+1} = -e_k \quad (13)$$

Equation (13) has a single fixed point equal to zero and it is critically stable.

IV. STABILIZATION OF THE OPTIMAL SWITCHING PATTERN

The evolution of the error as $e_{k+1} = -e_k$ is not stable because the error does not decay to zero but oscillates between positive and negative values of the magnitude of the initial error. If the initial error is small, it may lead to a good behavior; however, for arbitrary initial values of the error, the optimal control does not provide error convergence towards zero. As a result, the following control action is considered to be applied:

$$t_{on} = t_{on}^* + \Delta t_{on} \quad (14)$$

where t_{on}^* is the optimal control action that makes the error integral equal to zero and given by (10), and Δt_{on} is a new control action taken to stabilize the system. Substituting the new control action (14) into the evolution error (12) yields (15).

$$e_{k+1} = -e_k + (m_- - m_+) \Delta t_{on} \quad (15)$$

The design of Δt_{on} is made by pole placement, assuming that the desired behavior of the error is given by

$$e_{k+1} = a e_k \quad (16)$$

with a being the tuning parameter that, for stability, must have a positive value within the range $0 < a < 1$. As a result, Δt_{on} is chosen as a proportional control action with gain K , that is

$$\Delta t_{on} = K e_k \quad (17)$$

The evolution of the error with the new control action is:

$$\begin{aligned} e_{k+1} &= -e_k + (m_- - m_+) K e_k \\ e_{k+1} &= e_k \underbrace{(-1 + (m_- - m_+) K)}_a \end{aligned} \quad (18)$$

Henceforth, given the desired closed-loop behavior a for the error, the gain is given by

$$K = \frac{1 - a}{m_+ - m_-} \quad (19)$$

In summary, by augmenting the optimal control action for one-cycle zero-integral-error with a proportional control action, the stable closed-loop behavior guarantees the convergence of the error to zero. Furthermore, the parameter a can be freely selected to tune the closed-loop response. It is true that with this extended stabilizing control the one-cycle zero-integral-error is no longer fulfilled when $e_k \neq 0$, but this compromise solution asymptotically achieves the one-cycle zero-integral-error as $\lim e_k \rightarrow 0$.

Finally, the control algorithm implementation is resumed in the flowchart of Figure 5.

V. SIMULATION RESULTS

The power system presented in Figure 6 is formed by a three-phase four-wire SAPF connected in parallel with a

$$e(t) = \begin{cases} e_1(t) = e_k - m_- t, & \text{if } 0 \leq t < \frac{T_{sw} - t_{on}}{2} \\ e_2(t) = e_k - (m_- - m_+) \frac{T_{sw} - t_{on}}{2} - m_+ t, & \text{if } \frac{T_{sw} - t_{on}}{2} \leq t < \frac{T_{sw} + t_{on}}{2} \\ e_3(t) = e_k - m_- \frac{T_{sw} - t_{on}}{2} - m_+ t_{on} + m_- \frac{T_{sw} + t_{on}}{2} - m_- t, & \text{if } \frac{T_{sw} + t_{on}}{2} \leq t \leq T_{sw} \end{cases} \quad (2)$$

$$e(t) = \begin{cases} e_1(t) = i_{rk} - (i_k + m_- t), & \text{if } 0 \leq t < \frac{T_{sw} - t_{on}}{2} \\ e_2(t) = i_{rk} - i_k - (m_- - m_+) \frac{T_{sw} - t_{on}}{2} - m_+ t, & \text{if } \frac{T_{sw} - t_{on}}{2} \leq t < \frac{T_{sw} + t_{on}}{2} \\ e_3(t) = i_{rk} - i_k - m_- \frac{T_{sw} - t_{on}}{2} - m_+ t_{on} + m_- \frac{T_{sw} + t_{on}}{2} - m_- t, & \text{if } \frac{T_{sw} + t_{on}}{2} \leq t \leq T_{sw} \end{cases} \quad (3)$$

$$\int_{\frac{T_{sw} + t_{on}}{2}}^{T_{sw}} e_3(t) dt = e_k \frac{(T_{sw} - t_{on})}{2} - m_- \left(\frac{T_{sw} - t_{on}}{2} \right)^2 - m_+ \frac{(T_{sw} - t_{on})}{2} t_{on} + m_- \left(\frac{T_{sw}^2 - t_{on}^2}{2} \right) - \frac{m_-}{2} \left(\frac{T_{sw}^2 + 2T_{sw}t_{on} - t_{on}^2}{2} \right) \quad (7)$$

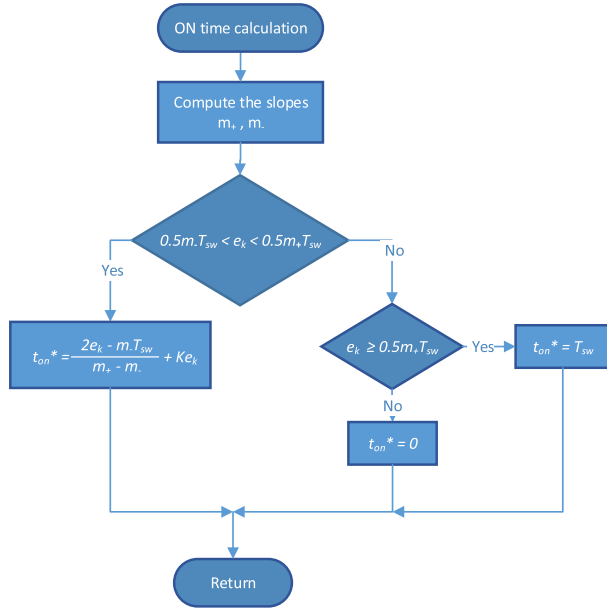


FIGURE 5. Flowchart of the digital control algorithm.

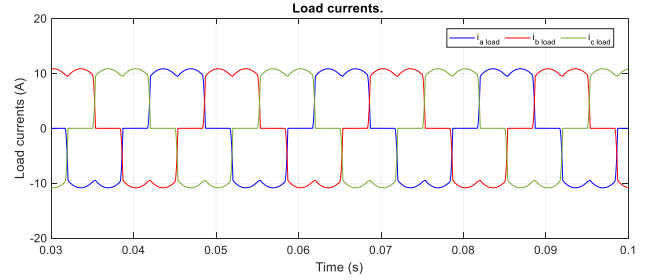


FIGURE 7. Load current waveforms.

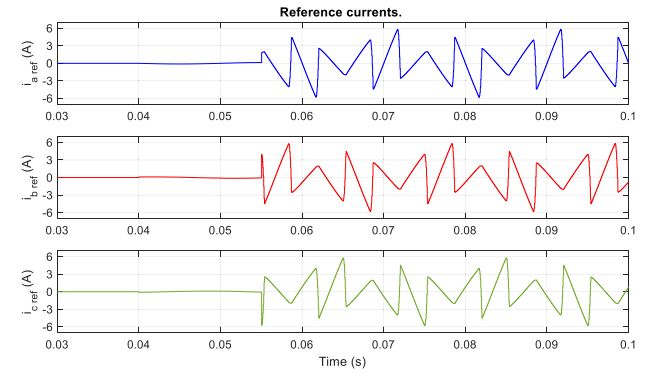


FIGURE 8. SAPF reference currents.

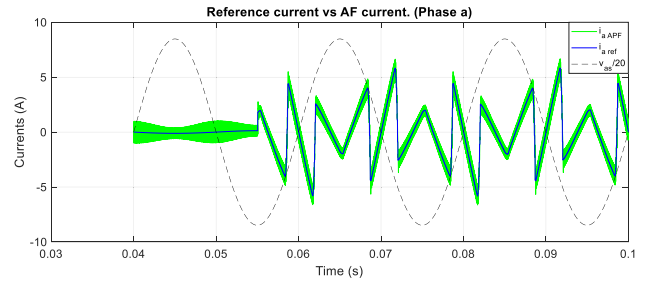


FIGURE 9. Current tracking performance for phase a.

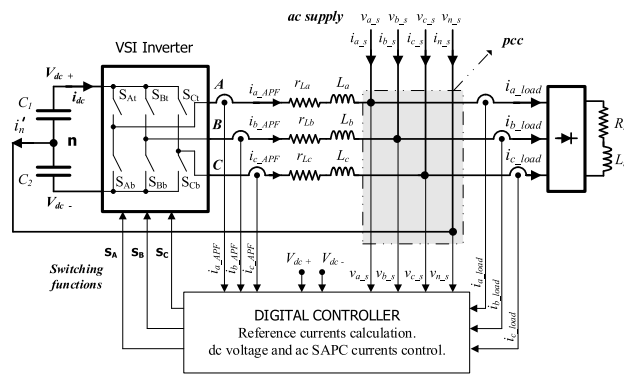


FIGURE 6. Block diagram of the power system under consideration.

non-linear load that demands reactive and distortion powers. The SAPF reduces the current total harmonic distortion (THD_i) and achieves near unity power factor (PF) upstream from the PCC.

The values used in the circuit are: $L_z = 3$ mH; $r_{Lz} = 0.1 \Omega$; $C_1 = C_2 = 4.7$ mF. The supply voltages (v_{a_s} , v_{b_s} and v_{c_s}) are symmetrical with RMS values equal to 120 V, and a fundamental frequency of 50 Hz. The DC bus voltage is $V_{dc} = 475$ V. The SAPF switching frequency is 20 kHz. Connected to the PCC, a diode-based three-phase rectifier feeds a series load with values $R_r = 27 \Omega$ and $L_r = 6$ mH.

Current slopes for each phase are given by:

$$m_{+z} = \frac{\frac{V_{dc}}{2} - V_{z_s} \sin(\omega t + \varphi_z)}{L}$$

$$m_{-z} = \frac{-\frac{V_{dc}}{2} - V_{z_s} \sin(\omega t + \varphi_z)}{L}$$

where φ_z are the corresponding phase shifts $\varphi_a = 0$, $\varphi_b = -\frac{2\pi}{3}$, and $\varphi_c = -\frac{4\pi}{3}$.

The power system was simulated using Matlab/Simulink®. The proposed control was programmed using a user function (s-function). Compared with the previous controller proposed in [19], the implementation is simpler because the switching pattern does not change. Figure 7 shows the load currents. The SAPF reference currents are presented in Figure 8. These currents are obtained by subtracting the fundamental positive-sequence active component from the load currents. Hence, by using these reference currents, the SAPF reduces the reactive and distortion powers to near-zero values. It must be noted that the selected value for the tuning parameter a of (19) is 0.9, because, as discussed below, it presents the lowest current THD_i value and a good compromise between settling time and tracking error.

Figure 9 presents the current tracking performance of the controller proposed in Section IV, while two details of this figure are presented in Figure 10 and Figure 11. The quality

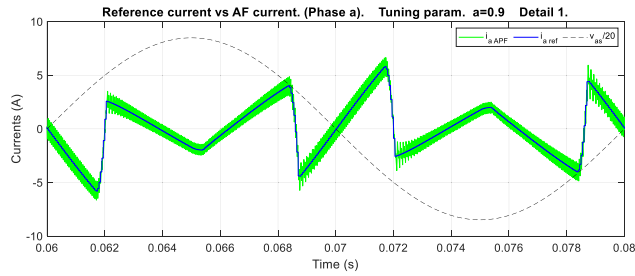


FIGURE 10. Current tracking performance for phase a. Detail 1 (0.06s < t < 0.08s).

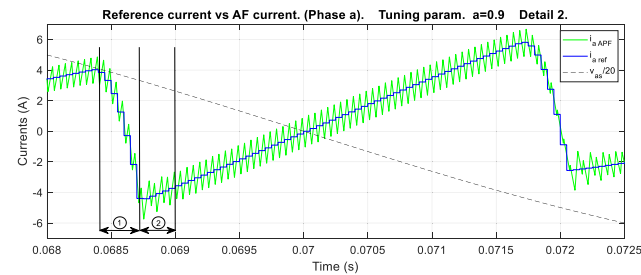


FIGURE 11. Current tracking performance for phase a. Detail 2 (0.08s < t < 0.0725s).

of the proposed control is demonstrated by the improved current tracking achieved compared with that obtained in [19]. In order to perform that comparison and, to demonstrate the effect of the tuning parameter a in the closed-loop behavior, Figure 12a, Figure 12b, and Figure 12c show the current tracking error corresponding to the time range of Figure 11 for values of a equal to 0.4, 0.75 and 0.9 respectively. Figure 12d also shows the current tracking error, but in this case, obtained by applying the alternating switching pattern presented in [19].

Comparing Figure 12a, Figure 12b and Figure 12c with Figure 12d, it can be seen that the surge and the small transient, showed at the zero-crossing of the phase voltage (at $t = 0.07$ s) in Figure 12d, have been avoided with the proposed switching pattern. Current tracking has been evaluated during the high derivative in the reference current that occurred from $t = 0.0684$ s to $t = 0.0687$ s (interval 1 in Figure 11 and Figure 12). To quantify the tracking performance, the maximum current error (E_{i_max}) and the current error average over this interval (E_{i_AV}) are computed for every case in Figure 12. On the other hand, settling time (t_s) has been measured as the transient time after the slope change at $t = 0.0687$ s (interval 2 in Figure 11 and Figure 12). Table 1 presents the obtained results.

As expected, settling time increases for values of a approaching 1, which is the value for the critically stable condition. On the contrary, the current tracking error is reduced as well. At this point, to establish the best value of the tuning parameter, the effect on the power factor PF and THD_i of the supply currents after SAPF activation is considered in the analysis.

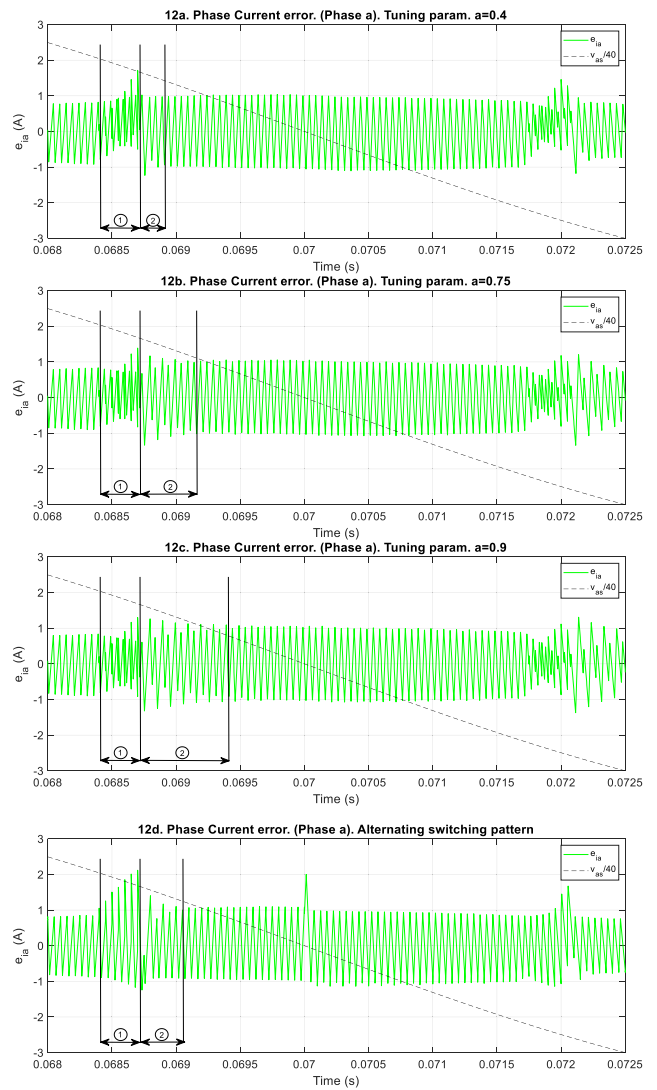


FIGURE 12. Current tracking error comparison during detail 2 time interval for tuning parameter: 12a) 0.4; 12b) 0.75; 12c) 0.95 and 12d) alternating pattern.

TABLE 1. Tracking current performance.

Pattern	Symmetrical (proposed)			Alternating
a	0.4	0.75	0.9	-
E_{i_max} (A)	1.71	1.39	1.29	2.12
E_{i_AV} (A)	0.271	0.092	0.031	0.008
t_s (μ s)	181.4	445	676	335

Figure 13 shows the supply currents for $a = 0.9$ before and after the SAPF activation in $t = 0.055$ s. The supply current waveforms become a set of fundamental balanced sinusoidal currents, as corresponds to an ideal power supply. The rest of the case waveforms studied for the different tuning parameters are not included since the signals present small differences that are better quantified by the THD_i and PF

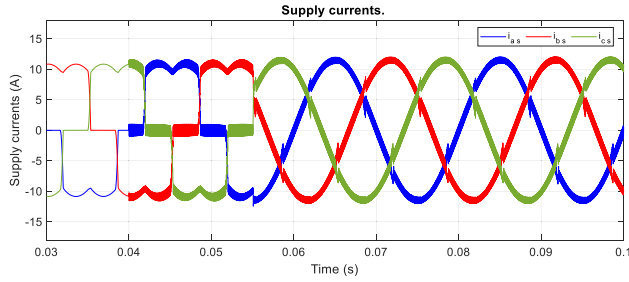


FIGURE 13. Supply currents before and during SAPF compensation for $a = 0.9$.

TABLE 2. THD and PF values.

Pattern	Symmetrical (proposed)			Alternating
	0.4	0.75	0.9	
a	0.4	0.75	0.9	-
$THD_{i(50)}$ (%)	3.09	2.48	2.27	2.48
$THD_{i(25)}$ (%)	2.55	2.04	1.86	2.02
PF	0.99805	0.99821	0.99820	0.99820

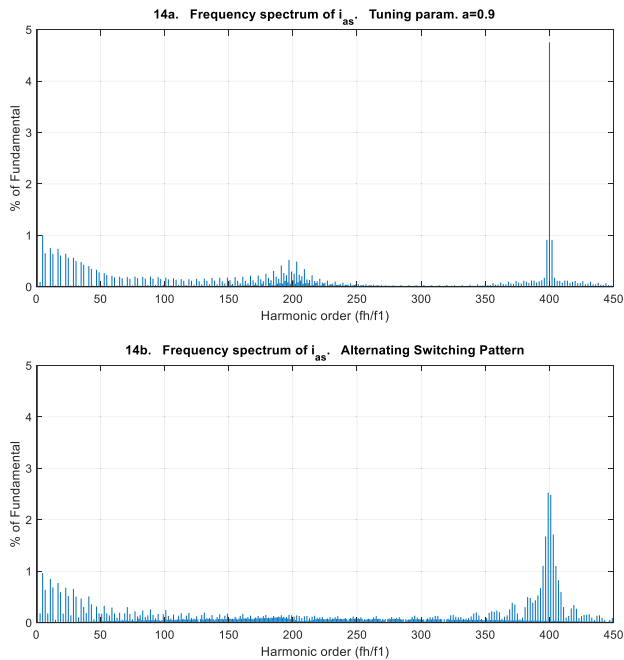


FIGURE 14. Supply current harmonic components during SAPF compensation for $a = 0.9$ (top) and for alternating switching pattern (bottom).

values included in Table 2. $THD_{i(50)}$ and $THD_{i(25)}$ are the current THD_i computed with the first 50 and first 25 harmonic components, respectively.

The analysis shows that no significant differences can be found in terms of PF ; however, in terms of THD_i , the best results are obtained for $a = 0.9$, which is the value finally selected for the implementation.

To complete the analysis, Figure 14 presents a comparison of the harmonic spectrum of the supply currents obtained during compensation. Figure 14a shows the harmonic spectrum corresponding to the proposed symmetrical pattern with tuning factor $a = 0.9$, while Figure 14b corresponds to

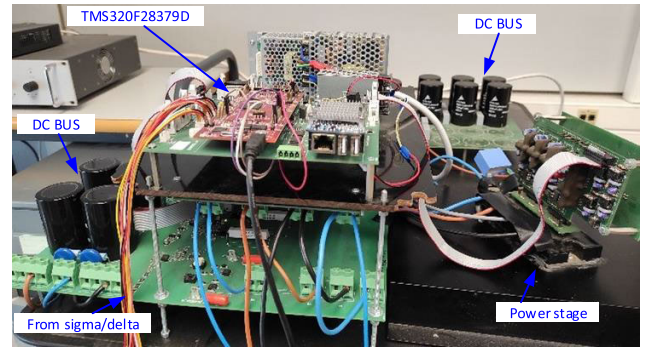


FIGURE 15. Experimental setup.

the alternating switching pattern presented in [19]. Both harmonic spectrums are quite similar. However, the one corresponding to the symmetrical pattern concentrates the harmonic distortion around the switching frequency (order 400 for 20 kHz). In the case of the alternating pattern, the high-frequency distortion is spread around the frequencies near the switching frequency. In both cases, the low-order harmonic components are small compared with the fundamental component, as indicated by the resulting THD_i values presented in Table 2.

VI. EXPERIMENTAL RESULTS

The prototype shown in Figure 15 is the same as the one used in [19]. SAPF was implemented by means of a Toshiba PM75CG1B120 (75 A, 1200 V) three-phase power stage switching at 20 kHz. The scheme of the power system matches the one shown in Figure 6. The SAPF component values (DC bus capacitors and phase inductances), as well as the load components are the same as those presented for the simulation example in Section V. A Pacific Power A-360MX three-phase power supply generates the 120 V RMS supply voltages. A DC bus voltage controller assures $V_{dc} = 475V$ and a capacitor voltage-balancing controller keeps the voltage equally distributed between the capacitors [1]. A LeCroy waveJet 324 oscilloscope (200 MHz-2 GS/s) is used to carry all measurements and to obtain the voltage and current waveforms presented in this section.

As it was explained in [19], the one-cycle control requires high-speed computing, because it has to calculate the reference currents and the ON times of the next switching period in a few microseconds at the beginning of the switching period, as shown in Figure 4. However, the proposed controller avoids the need for a switching pattern change, which means that the implementation becomes simpler, and the computational cost is reduced by 4.2%. The SAPF currents and load currents are measured using six AMC1303E2520 sigma-delta modulators featuring 20 mega samples per second (MSPS) to obtain 40 high-precision samples per switching cycle. This allows the digital signal controller (DSC) to precompute the slope of each one of the six currents and their values at the end of the switching period. Considering the power stage dead-band restrictions, the minimum and maximum values for t_{on} are limited to 5% and 95% of the

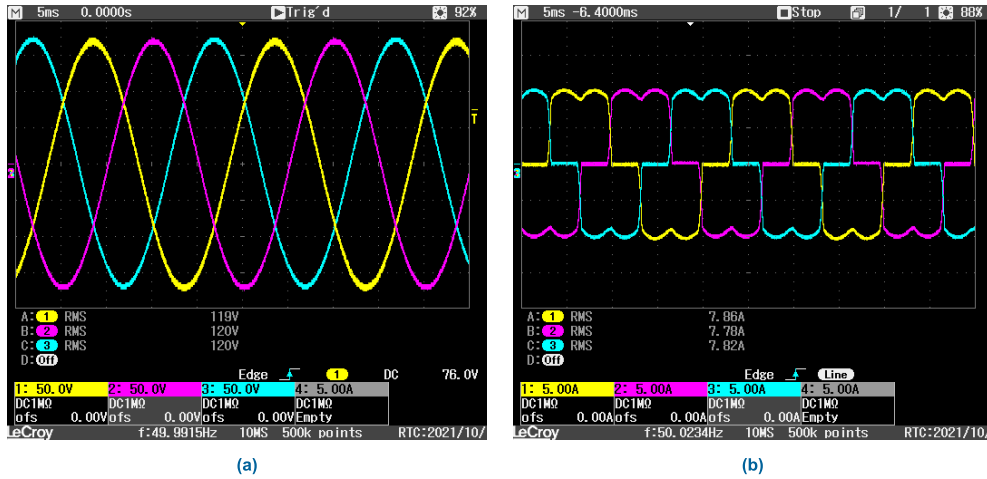


FIGURE 16. Supply voltages (a) and load current waveforms (b).

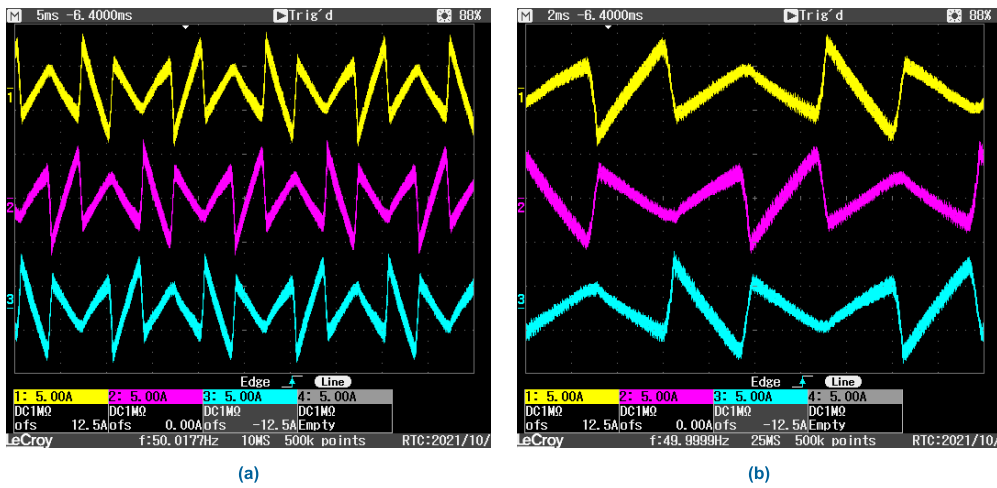


FIGURE 17. SAPF phase current waveforms (a) and a detail at 2ms/div (b).

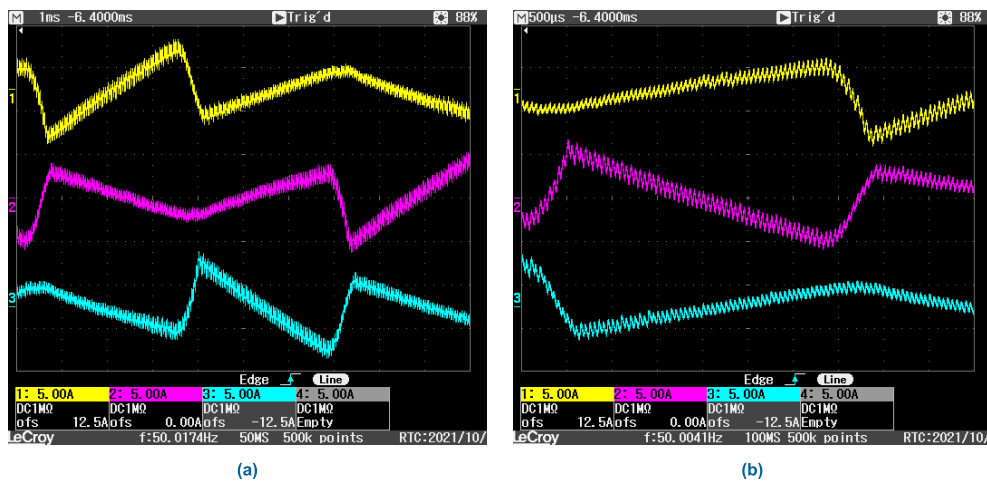


FIGURE 18. Detail of SAPF phase current waveforms at 1ms/div (a) and 500µs/div (b).

switching period, respectively. A Texas Instruments dual-core DSC TMS320F28379D is used to implement the proposed

control. The experimental results are shown in the following figures.

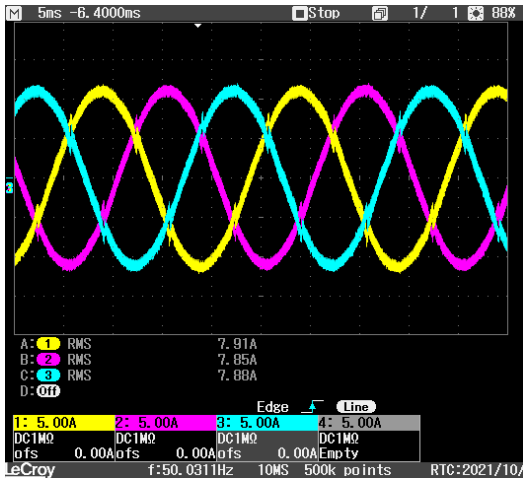


FIGURE 19. Supply during SAPF compensation.

Figure 16-a shows the supply voltages, a set of three-phase balanced voltages of 120 V RMS. The load currents are shown in Figure 16-b and correspond to the non-linear load presented in Section V. The currents delivered by the SAPF to achieve global compensation are presented in Figure 17-a and details of the SAPF phase currents are presented in Figures 17-b and 18. These detailed waveforms show the good shape of the currents. Compared with the ones obtained in [19], zero-crossing issues are avoided. The excellent current tracking is demonstrated by the high quality of the supply current waveforms obtained during compensation. Figure 19 shows how the supply currents become a set of balanced sinusoidal currents. The small surges remaining in the waveforms are due to the normal error produced in tracking the sudden slope changes in the reference currents. The supply current $THD_{i(50)}$ is 3.01% and PF reaches a value of 0.992. A slight increment in the current THD_i value compared with the one obtained in the simulation can be observed. This is caused by the non-ideal characteristics of the semiconductors and the tolerances of the passive components used in the experimental setup.

VII. CONCLUSION

A first version of the one-cycle current controller was implemented in a previous work, featuring minimization of the current integral error. However, an alternating switching pattern was used in the implementation presenting, as main drawbacks, a current surge and transient instability at the zero-voltage crossovers, and some technical implementation complexity. In this work, an improved version of the one-cycle digital current controller, using a single symmetrical switching pattern, has been proposed. Due to its simpler implementation, it reduces the computational cost by 4.2 %, which is crucial in this kind of controllers. It also solves the problems associated with the switching pattern changes at zero-voltage crossovers. However, the stability analysis of the proposed controller indicates that it is critically stable for any grid voltage sign. This problem was solved by adding a control action with a proportional term that forces the current

error to be reduced, guaranteeing the stable behavior of the control. In order to select the tuning parameter, the performance in current tracking has been studied via simulation considering THD_i and PF in the supply currents for several tuning parameters. Finally, the controller has been implemented in an experimental shunt active power filter setup. The results demonstrate the excellent current tracking of the proposed controller that achieves fundamental balanced supply currents with a low THD_i and a high PF .

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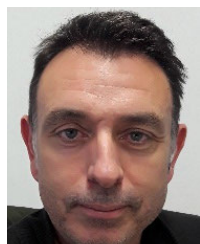
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