Received 6 April 2022; accepted 5 May 2022. Date of publication 23 May 2022; date of current version 15 June 2022. The review of this paper was arranged by Associate Editor Thomas I. Strasser. Digital Object Identifier 10.1109/OJIES.2022.3174218

# A Cross-Disciplinary Outlook of Directions and **Challenges in Industrial Electronics**

JINHUA SHE <sup>1</sup> (Fellow, IEEE), HIPÓLITO GUZMÁN-MIRANDA <sup>2</sup> (Senior Member, IEEE), VICTOR HUANG <sup>103</sup> (Life Fellow, IEEE), ALLEN C. CHEN<sup>4</sup> (Life Senior Member, IEEE), STAMATIS KARNOUSKOS <sup>105</sup> (Fellow, IEEE), LARISA DUNAI <sup>106</sup> (Member, IEEE), CHENGBIN MA<sup>D7</sup> (Senior Member, IEEE), ALIN TISAN<sup>D8</sup> (Member, IEEE), AND SHO YOKOTA <sup>[]</sup> (Member, IEEE)

> <sup>1</sup>Tokyo University of Technology, Hachioji, Japan <sup>2</sup>Universidad de Sevilla, Sevilla, Spain <sup>3</sup>Sage Technology Resources, Cupertino, California 95014 USA <sup>4</sup>Innovatech Solutions Inc, New Jersey, NJ USA 5 SAP, Walldorf, Germany <sup>6</sup>Universitat Politècnica de València, Valencia, Spain <sup>7</sup>Shanghai Jiao Tong University, Shanghai, China <sup>8</sup>Royal Holloway, University of London, Egham, United Kingdom 9 Toyo University, Bunkyo-ku, Japan

CORRESPONDING AUTHOR: JINHUA SHE (e-mail: she@stf.teu.ac.jp)

The work of Jinhua Sh was supported by JSPS Grant-in-Aid for Scientific Research B under Grant 22H03998 (Japan).

ABSTRACT How to build a sustainable society in view of industrial electronics has been discussed from energy, information and communication technologies, cyber-physical systems (CPSs), and other viewpoints. This paper presents a cross-disciplinary view that integrates the fields of human factors, professional education, electronic systems on chip, resilience and security for industrial applications, technology ethics and society, and standards. After explaining the efforts and challenges in these fields, this paper shows a methodology for cross-disciplinary technology that integrates the technical committees in Cluster 4, Industrial Electronics Society. A project, which was launched in March 2022, implements a 'Proof of Concept' trial of the methodology.

**INDEX TERMS** Cross-disciplinary technology, electronic systems on chip, human factors, resilience and security for industrial applications, professional education, technology ethics, standards, sustainable society.

#### I. INTRODUCTION

The UN (United Nations) General Assembly set up seventeen Sustainable Development Goals (SDGs) in 2015 to achieve a better and more sustainable future. Those interlinked global goals were intended to be achieved by 2030 [1]. Many of the goals are exactly what the IEEE (Institute of Electrical and Electronics Engineers) strategies aim for overall.

The Industrial Electronics Society (IES) in IEEE is active at the forefront of achieving these goals. For example, IES has been working with IEEE Honduras Section to perform IEEE Smart Village. The installation of solar PV panels not only illuminated the hallways of kitchen areas but also brought smiles to women and children in a village [2]. IEEE published the first issue of IEEE Women in Engineering Magazine in

2007 [3]. IES has been contributing significantly to women's activities in engineering and since the IES Women in Engineering Forum was arranged at the 43 rd IECON (the Annual Conference of IES) in 2017 in Beijing, it has become a regular event not only at IES-organized conferences but also at the seminars of IES local charters in the world. The IES Technical Committee on Standards has been carrying out INTEROP (Standards and Interoperability) Plugfest activities since 2018 to investigate and develop evolving standards or promote and describe established standards [4]. In addition, the Industry Forums organized by the IES Industry Activities Committee have often focused on sessions and talks that make evident how technology can be used towards enabling society and sustainability objectives. Furthermore, IES brought to life another Technical Committee in 2020 [5], with the goal to investigate the interplay of IES technologies, ethics, and society overall to address interdisciplinary aspects which are also underpinning the SGDs. Strategically, IES is eager to contribute to the fulfillment of the SDGs by acting as an enabler in all aspects of industrial electronics. New technologies, such as Big Data and machine learning, may further enable to tangibly monitor, measure, and develop innovative ways to achieve the 17 SGDs [6].

Changes in the economy, society, and environment can have a huge impact on how the aforementioned issues can be tackled. These changes are also opportunities for innovation. Adapting to these changes from the viewpoint of industrial electronics is a colossal challenge. While a large number of investigations have been carried out from the viewpoints of energy [7], [8], information and communication technologies (ICT) [9]–[11], and Cyber-Physical Systems (CPSs) [12], few have been reported from cross-disciplinary technology integrating the fields of human factors, professional education, electronic systems on chip, technology ethics and society, and standards. To call for attention and discuss breakthroughs in this situation, we have presented two reviews from the crossdisciplinary viewpoint [13], [14].

This paper elaborates on the concepts and ideas of these reviews, as not only the information and insights in each domain are discussed systematically, but also a methodology for the integration of cross-disciplinary technologies is presented. In this paper, we review the efforts of several Technical Committees, that is, Education in Engineering and Industrial Technologies, Electronic Systems on Chip, Human Factors, Resilience and Security for Industrial Applications, Standards, and Technology Ethics and Society, all of which are for Cluster 4 within IES, and explain how, within the scope of those committees, the posed challenges can be addressed.

## **II. HUMAN FACTORS**

Human factors is a practical engineering discipline that is an important part of designing tools and systems that are safe and easy to use, as well as creating environments that are easy to work and live in. The history of human factors has its origins in Europe in the 1850 s. Modern research on human factors started with human error research after World War II in the United States and has developed with applied psychology as its background. Currently, as the International Organization for Standardization (ISO) defines the principle of human-centered design as ISO11064-1, human factors considers human and system elements to be equidistant, and attempts to optimize the interactions among tasks, tools/equipment, design of objects/workplaces, physical environment, organizations/management, and culture/laws.

## A. TRENDS

Human factors makes an important contribution to solving the problems of modern society related to the 17 SDGs. In particular, findings of human factors are used in designing various systems that contribute to our society. After understanding human characteristics, it is necessary to design a system and related interfaces that are suitable for humans.

The members of the IES Technical Committee on Human Factors have been devoting themselves to the solution to this problem. For example, Suzuki et al. developed a system using artificial intelligence (AI) to automatically identify children's gross motor skills and reduce the burden of childcare in kindergartens [15]. They classified children's movements to understand human characteristics. Chugo et al. designed a standing support system that utilized a model of human dynamics to ease the movement of an elderly's standing-up motion [16]. The system integrated the knowledge of kinematics, mechanics, and bio-mechanics to produce a suitable movement for the elderly. Yokota et al. devised a low-profile omnidirectional personal-mobility system that was operated by a natural movement of human beings [17]. They modeled the standing posture of humans and used the model to successfully control mobility. She et al. applied control theory to assistive technology and developed an electric cart to improve walking ability [18]. A pedal unit was mounted on the cart to provide some exercise to train a driver's lower limbs. The cart system integrates bio-information, mechatronics, information technology, human factors, AI, and control theory to automatically select a suitable pedal load that fits the driver's physical condition. Makino et al. created an AI-based system to assist doctors in the early detection of pinched nails [19]. A neural network categorized gait patterns and diagnosed pincer nails based on the patterns. Other systems were also investigated based on the principles of human-centered design in the fields of social systems, transportation, daily life, manufacturing, and so on.

#### **B. FUTURE CHALLENGES**

Modern human factors are composed of a variety of elements, including cognition, mentality, and social characteristics. This allows us to address a wide range of issues, for example, problems in health care, quality of communication, and physical, psychological, and spiritual handicaps. In general, the challenge of human factors is how to optimize the relationship between systems and people, or the relationship among people. In addition to the facts that human perceptual, cognitive, and behavioral characteristics are complex and vary among individuals, the social environment changes rapidly. This poses a big challenge. Not only new perceptual, cognitive, and communicative features (for example, [20], [21]) need to be integrated into the area of human factors, but also interdisciplinary cooperation with other specialized committees in the IES is required to find solutions from a variety of perspectives.

A large number of human-factors-related standards have been established to ease the design of products and systems. An example is shown in Table 1. These standards ensure the safety of systems and products, guarantee that they are tailor-made for the purposes, and improve the operability and services. Some of the standards are summarized in [22], [23]. The related standards should be incorporated in system design

TABLE 1 Structure of ISO 9241 Series: Ergonomics of Human-System Interaction

Part	Title
1	Introduction
2	Job design
11	Hardware and software usability
20	Accessibility and human-system interaction
21-99	Reserved numbers
100s	Software ergonomics
200s	Human-system interaction processes
300s	Displays and display-related hardware
400s	Physical input devices, Ergonomics principles
500s	Workplace ergonomics
600s	Environment ergonomics
700s	Control rooms
900s	Tactile and haptic interactions



**FIGURE 1.** Educational interaction between University and Industry.

from the first stage to guarantee the safety and usability of a designed system because such a system is directly involved with humans.

#### **III. EDUCATIONAL PERSPECTIVE**

The continuous evolution of technologies pushes universities to update their course contents yearly, as well as to adapt their teaching methodologies and platforms. This update is possible thanks to the interconnection between universities, industry, and other partners through regional, national, and international projects that develop new theories and tools. This process shows that a higher education system is always interconnected with the industry and the research Fig. 1. That is, on one hand, the need and demand of a society for new products encourage the development of new knowledge, and on the other hand, the industrial demand for engineers prepared with the latest technologies and development processes leads higher education to promote (i) professional lecturers coming from industry, (ii) project-based learning (PBL) methodologies, (iii) internships in industry, and (iv) industrial seminars/courses.

A common trend is that professionals coming from industry are involved in the learning processes of a higher education system. The objective of those theoretical and practical courses is to convey to students the methods and practical contents that are routinely used in specific industrial areas. Experts from industry are often invited to teach students specific topics. This improves the quality of the course content and gives students a practical perspective of the taught concepts, while at the same time motivating them to take the subject. These professionals often utilize practical cases and examples that reinforce this practical and professional vision of the course [24].

## A. FUTURE TRENDS

The PBL methodology developed by John Dewey is based on the 'learning by doing' concept [25]. This method, which has been used since ancient Egypt, enhances practical learning and increases student motivation and collaboration. During PBL, groups of students under the supervision of an instructor are involved in the development of specific projects, following all the stages of project development from the idea to the actual initial prototype. Logically, this method requires a higher level of multidisciplinary knowledge. As a result, students gain experiences in aspects, such as project planning, acquisition of raw materials, product design and development, work management, logistics, and commercialization. As part of the learning process, students also improve their communication skills. In many universities, the PBL methodology involves the collaboration between universities and research institutions and between the industry and universities [26]. Since PBL is oriented toward solving real-world problems, students are in contact with stakeholders, end-users, and developers. Industry involvement in these projects has proven to have a positive impact on student motivation to learn and to help them develop analytical and critical thinking, technical management skills, and business management skills [27], [28].

The importance of work experience in the industry, the need for reference, and the need for employability encourage students to look for short-term internships in the industry. This practice allows them to work on specific projects or topics directly in the industry, and there is the possibility of using some of the research and development results for a final bachelor's or master's thesis [29]. This practice is usually well coordinated between universities and the industry and students are assigned two tutors, one from each part. Many universities have different collaborative programs between the university and industrial partners in different disciplines. Some of the existing programs, such as Erasmus+, EURES, and European Project Semester, also include the internationalization of work experience in the industry. Participation in such programs may enhance students' abilities in teamwork, decision-making, ability to work in a multicultural environment, knowledge of practical issues, management in a foreign environment, and professional experience and financial rewards. This activity involves academics that are often related to a particular field of research that is of great interest to a particular industry. This facilitates that these instructors are hired or invited to teach different seminars or courses to industrial users in their area of expertise. The benefits of this dissemination effort are enormous, as it facilitates the transfer of recently developed technologies and knowledge to industry.

It is also beneficial to instructors who can obtain industrial feedback that can be enhanced to optimize these developments. It also enables further collaboration that is very interesting for future testing of new methods and technologies. From an educational perspective, improving educational methodologies and content, and engaging education in the development of industrial projects are key to success. Finally, education requires the integration of the ethical and social aspects to manage societal impacts. In standards, the educational perspective serves as the definition of law and standards for safe and reliable online learning. One of the best practices of the committee for student motivation from an educational perspective is to provide them access to research IEEE platforms such as IEEE Xplore and IEEE ILN Learning Network, as a part of their educational resources additional to the books and professor notes. These platforms will allow students to be involved in research-related educational strategies, such as Project-Based Learning and tutorials.

#### **IV. ELECTRONICS SYSTEMS ON CHIP APPROACHES**

From an Electronic Systems-on-Chip point of view, the constant technological evolution has reduced the size of individual components and greatly increased the capacity of individual silicon chips, while the economies of scale have allowed huge price reductions for many electronic devices of small to medium capacity. This has allowed system-onchip solutions to appear across many different fields and industries [13]. These solutions allow programmable logic solutions to be used in fields that previously could not benefit from those approaches. Some examples of this could be adding programmable logic fabric (such as those used in FPGAs, Field Programmable Gate Arrays) to achieve higher parallelism and performance in previously microprocessoronly implementations, adding a microprocessor to ease the management of sequential tasks in previously FPGA-only projects, or even introducing new complex electronics where there were previously none.

## A. EMERGENCE OF FREE AND OPEN-SOURCE TOOLS FOR DIGITAL DESIGN

Another emerging trend is the appearance of free and opensource (FOSS) tools for digital design and verification. While some of these tools have been around for many years (for example, the first version of the GHDL simulator is now about 18 years old), it has only been in the latest years that they have reached significant milestones, such as support for modern verification methodologies [30], and a completely open-source design flow for the ICE40 and ECP5 families of Lattice FPGAs that covers all the steps from synthesis to bitstream generation and FPGA configuration [31].

The emergence of these free and open-source tools is also a push for vendors to release parts of their flows as open-source tools, or at least provide some way for the users to customize their tool flows, such as Xilinx's Rapidwright [32].

The status of the free and open-source tool ecosystem is very healthy, with multiple tools to choose from for each step of the design and verification process. There are simulators such as GHDL [33] for the VHDL language and Icarus Verilog [34] or Verilator [35] for the Verilog language. But there are also HDL (Hardware Description Languages) unit testing frameworks such as VUnit [36]. CoCoTb (Coroutine Cosimulation Testbench) is a specially interesting software since it allows to easily cosimulate HDL code interacting with a python testbench, greatly reducing the effort to create complex, structured testbenches [37]. For synthesis, the main tool is the Yosys Open Synthesis Suite [38], which can synthesize Verilog but also VHDL through the open-source GHDL synthesis front-end [39], although other front-ends may be used, for example, the proprietary front-end Verific (when a license is available). For place and route, nextpnr [31] is a timing-driven place and route tool, which is also portable and vendor-neutral, so it can support different FPGA families if their architecture is documented. For bitstream generation, project icestorm [40] can generate bitstreams for the iCE40 family of Lattice FPGAs, but there are multiple efforts to document other FPGA families, such as project Trellis and project X-ray, for the Lattice ECP5 and Xilinx 7-Series respectively [41], [42]. For interfacing with different EDA tools, both open source and proprietary, Edalize provides a common interface to abstract the operation of multiple tools, so users do not have to learn to script every tool independently [43]. An interesting text editor to operate with all these tools is the TerosHDL editor [44], which is an integrated IDE that is distributed as a Visual Studio Code extension.

FOSS tools may enable unexpected ways of using the tools, as they are not subject to usage, licensing, or modification restrictions. For example, without even modifying the tools, a user can launch any number of instances of the GHDL simulator, limited only by available computing power, and not the number of available license seats [45]. Furthermore, since the tools allow studying and modifying their source code, this can be a further enabler for innovation. Depending on the application, the usage of multiple economical chips configured with open source tools can position itself as an alternative to solutions based on monolithic programmable System-on-Chip devices, configured with proprietary toolchains.

The availability of these tools is also especially interesting from an educational standpoint, since they allow for lifelong learning both inside and outside higher education institutions, while also allowing institutions with fewer economic resources to perform PBL with real devices and applications. Furthermore, FOSS tools may make the difference between being able to use and implement FPGA solutions or not in developing countries, especially those with reduced or nonexistent R+D budgets and those subject to export control restrictions, contributing to technology democratization and reducing inequality. Additionally, FOSS tools can be subjected to security audits, to avoid almost-undetectable supply chain attacks like [46].

An important difference that open-source FPGA implementation and bitstream generation tools have with respect to open-source software compilers is that the internal chip details needed for bitstream generation are not public, while the ISA (instruction set architectures) of the microprocessors supported by open source compilers (such as GCC) have been published by device manufacturers. Thus, the developers of open-source FPGA implementation tools must use probing techniques to determine which bits in the FPGA bitstream configure the primitive attribute of each specific device. This is not different from what many researchers already do for academic and research projects [47], [48]. Probing is performed by using tools that already exist, for example, the ones provided by the FPGA vendors. The probing process uses the tool as a black box, where known inputs are stimulated and the outputs are observed.

The main advantage of probing versus other methods is that it allows acquiring the needed information without reverseengineering any software, which is forbidden by the majority of software end-user license agreements (EULAs). As of today, even if the method used to obtain this information does not violate any license agreements, the fact that it is not supported or intended by the manufacturers, coupled with the diversity of Intellectual Property law particularities across the globe, creates a legal gray area where companies currently do not know if they could hit any legal issue if using these tools for production.

A desirable step forward would be the standardization of the minimal information that chip manufacturers would have to provide to allow implementation and bitstream generation. This future standard would need to balance this interoperability needs with the need to preserve the confidentiality of the internal chip implementation details. Concerns about what information can be provided without inadvertently leaking internal information to competitors have been historically the main reason chip manufacturers are reluctant to share the information needed to create bitstreams using third-party tools.

Nevertheless, free and open-source tools for digital design and verification can be used as of today, with good performance and implementation efficiency results, in both research and educational contexts, and it is expected that their importance will grow in the future.

#### **B. IMPLEMENTATION CHALLENGES OF AI ON SOC**

The increase in the compute capability of the hardware platforms has facilitated AI to advance to a new level. Hence, meta-heuristic methods (MHM), fuzzy logic (FL), expert systems (ES), or complex machine learning (ML) algorithms can now be run close to signal source (sensors) on edge devices (embedded systems/cyber-physical devices), on the "cloud" in data centers, or in-between, on what is called "fog" computational systems made of a collection of edge devices. All these systems can be made now flexible enough to enable the software to efficiently be defined to benefit of the task customized compute hardware and the hardware to reconfigure for a specific software application to maximize the processing speed/energy consumption ratio. There is now an increased hardware-software symbiosis, in which, the heterogeneous systems on programmable chips (SoPC) have an even more growing role to play. It is a fact that today, deep learning (DL) on deep neural networks (DNNs) and spiking neural networks (SNNs) are used in everyday consuming electronics due to this fantastic paradigm shift in the software-hardware relationship. This symbiosis is discussed in the following.

The SNN is implemented on digital CMOS or analog/mixed-signal technologies, memristive device technologies, or a combination of CMOS-memristive device neuromorphic chips (hardware architectures that mimic the biological neuron functionality). The neuromorphic hardware implementations have been crystallized in a few prominent state-of-the-art designs capable to simulate neural networks with several hundreds of thousands of neurons, such as SpiNNaker [49] (array of one million ARM9 cores and 7 Tbytes of distributed memory, all interconnected by a bespoke multicast router), IBM TrueNorth (1 million neurons and 256 million synapses) [50], Neurogrid (1 million neurons and 6 billion synapses) [51] or Intel Loihi (128 neuromorphic cores that simulate 130 k neurons and 130 M synapses in real-time) [52].

The DNNs are mostly deployed in general-purpose platforms, such as CPUs and GPUs (graphics processing units). Large-scale image classification models, best represented by the convolutional neural networks (CNN), have boomed in the last years, revealing high accuracy, multimillion parameter networks with high computational demands such as GoogLeNet [53], ResNet [54], DenseNet [55] or NAS-Net [56]. The above-mentioned networks were successfully implemented due to the capability of the (neural) CPUs to process multiple data using the single-instruction-multiple-data (SIMD) technique or implementing neural-specific instructions set such as Intel AVX-512 or custom floating-point data format (such as the brain floating point: bfloat16). These advantages have been many times multiplied when implemented in GPUs, for which manufacturers have developed highly optimized hardware and software framework support, such as Tensorflow, Pytorch, or Caffe. Taking data processing concurrency even further by adding the FPGAs design flexibility, successful DNN accelerators, composed of many processing elements (PE) and on/off chip memory such as NPU (Project Brainwave) [57], MAERI [58], Cambricon-X [59], Swallow [60], Eyeriss [61] or Xilinx Versal AI core [62], have been reported.

Moreover, when combining CPUs, GPUs, and FPGAs, obtaining heterogeneous computing platforms, the true computing potential is released, increasing, even more, the system performances when deploying complex/heavy computational tasks, bringing the development of integrated solutions such as system on chip (SoC), multi-chip module (MCM), systemin-package (SIP), single-board computer (SBC), or systemon-module (SOM) to a new level. Being able to take advantage of each compute platform paradigm's strong points has conferred high design flexibility and proven very performance rewarding. However, each of the platforms comes with drawbacks as well, and being able to 'pick and mix' the right data size and algorithm on the desired platform is not yet easily achieved.

To address these problems, a few methods have been developed such as data reuse, efficient memory access, algorithm compression, or workload partition strategies, which are used together to improve the data throughput and power efficiency [61], [63]–[66]. However, being able to address the diverse computing requirements for AI algorithms found in 5G, network, cloud, or edge applications is not an easy task.

The developed methods explore manual or automatic data partitioning and task-processing scheduling. The schedulers dynamically distribute the processing tasks among all the resources to fully exploit all computing devices while minimizing load unbalance [67]. Amdahl's Law aims at maximizing power-normalized performance by considering the dynamic workload variations and its classification [68], [69], deploying data partitioning algorithms to minimize the parallel execution time of data-parallel applications on clusters of identical nodes of heterogeneous processors [70] or scheduling strategies and task decomposition to accelerate the training process of large-scale CNNs by minimizing the waiting time for critical paths [71].

Partitioning methods for CPU and FPGA-based heterogeneous platforms targeted high-throughput sparse convolution accelerators, such YOLOv2, where algorithm-level optimization schemes (hardware-aware neural network pruning, clustering, and quantization) and hardware/software tasks allocation with non-performance-critical layers (pooling, reorganization, concatenation) running on CPUs and the convolution layers accelerated on FPGAs, have resulted in a maximized overall system performance [72]. Predictive frameworks for optimum partitioning of a workload between hardware and software have been also explored [73].

The scheduling goes even further, and questions about the best places to run the algorithm (edge, fog, or cloud computing) are ever more emerging. The level of proximity to the data source of the calculus platform is dictated by the application constraints such as the data bandwidth, communication latency in real-time applications, computing resources, or power consumption. It is mainly applied in Internet of Things (IoT) scenarios. To achieve high performance, various novel edge-cloud, edge-fog, fog-cloud solutions have been developed. Task allocation algorithms such as the weighted cost model to minimize the execution time and energy consumption in fog-cloud platforms [74], computation offloading method by dynamic scheduling of data/control-constrained computing tasks for IoT-enabled cloud-edge computing [75], or context-aware application placement policy for Fog environments [76] have been recently developed.

The superiority of flexible software running on reconfigurable hardware has now been demonstrated, with a multitude of methods capable to schedule processing loads across variate hardware systems being reported in the literature in a greater number. However, they mostly look at specific cases and cannot transcend into a unified divide and allocate methodology without a further understanding of the application-software-hardware relationship.

## C. FUTURE CHALLENGES

An open issue for vendors is how to improve the ease of use and configuration of programmable System-on-chip devices, so all the steps of the design and verification processes are made easier. The motivation behind this is to make FPGA and System-on-chip design accessible to more people, in particular software developers who may not have a strong background in electronics or digital design, with the intention of greatly increasing market size for these solutions.

One promising driver for this greater adoption is the arrival of higher-level languages and synthesis tools, which constitutes a push towards the higher adoption of these devices. In particular, these higher-level languages and tools open the field of FPGA and programmable System-on-Chip design to computer programmers who already have expertise in programming languages such as C, C++, or Python. A couple of examples of these higher-level synthesis tools are Vivado HLS [77], which is based on C and C++, and Amaranth-HDL [78], which is based on python. The first tool is provided by Xilinx and the second one is open-source. It must be noted that these higher-level synthesis tools do not support all the functionalities of the original languages they are based on, but must instead make some compromise and define what subset of the language they can work on, since not all high-level functionality provided by a programming language may be synthesized into logic gates.

As is typically the case when moving from lower-level descriptions to higher-level descriptions (such as when using software compilers instead of assemblers), the trade-off of this ease of use is an impact on the efficiency of the generated implementations, both in terms of area consumption and maximum working frequency for the implemented designs [79]. This means that, depending on the application, the most efficient strategies in terms of a trade-off between development time, area consumption, and performance may be a mix of both typical HDL descriptions and higher-level synthesis, where traditional HDLs are used for the design elements where area or performance is most critical.

The trend of moving the electronics, including signal processing and data handling, towards the very phenomena that need to be measured may result in systems with a high number of devices, where distributed computing may happen, and in which designers may find multiple synchronization and communication challenges (as explored in [80], [81] or [82]).

With respect to the accountability of AI decisions, the electronic implementations should include accountability mechanisms that can give the operators the possibility of extracting the information about decision-making so these decisions can be reviewed. This remains an open problem both at the machine learning and electronic implementation levels.

Finally, while functional safety of the designs has always had an important role to play in aerospace, automotive, biomedical, and other fields where critical systems take major roles and where failures are expensive in personal and/or economic terms, it is expected that due to the increase in complexity of the average design, higher verification efforts will be required for industrial designs in other, non-critical areas, increasing the required knowledge and efforts needed to successfully finalize a design [83].

## V. RESILIENCE AND SECURITY FOR INDUSTRIAL APPLICATIONS

As the complexity of today's products and systems increases, it is becoming more and more important to develop various aspects and technologies to assess and/or enhance the resilience and security of industrial applications. For example, how to reconfigure cyber or physical networks to ensure resilience vulnerable to failures and attacks, how to design distributed algorithms to manage systems to avoid single points of failure and reduce congestion, and how to improve the design of devices to improve their resilience and security. Applications range from national critical infrastructures such as power/energy systems and transportation systems, microgrids, nanogrids (e.g., household energy management), picogrids to devices, such as energy storage, smart sensors, smart actuators, and smart controller.

#### A. TRENDS

With the widespread adoption of cyber-physical systems of all kinds, resilience and security are now a central issue in many industrial applications, such as in critical infrastructures (e.g., smart grids, computing systems, factories, and supply chains) and in emerging autonomous systems [84], [85]. Strategies for achieving resilience and security are usually comprehensive and require a systematic approach to risk analysis, vulnerability identification, decision making, testing and evaluation, etc. [86]. For example, it is critical to ensure the resilience of a power grid to extreme weather events.

Probabilistic metrics have been proposed to quantify the operational resilience of the power grid to high impact low probability (HILP) events, including extreme weathers [87]. Two metrics, value-at-risk and conditional value-at-risk, were defined to measure resilience as the maximum loss of energy and conditional loss expectation of a loss of energy for events that exceed a predefined risk threshold, i.e., to quantify the worst possible outcome of a HILP event. Vulnerabilities are usually identified by worst-case events. In the resilient management of microgrids against storms (i.e., extreme weather events, overhead distribution lines, poles, and wind turbines are components that are vulnerable to damage [88]. Using the relevant fragility curves as model inputs, it is possible to find the failure probability of each vulnerable component under the forecasted maximum wind speed.

A complex system usually takes the form of a network containing nodes, edges, and connections. The failure probabilities of those components, which depend on the worst-case events, and various characteristic profiles of recovery in time can be utilized to find the least expensive solution to achieve the resilience of the system [89]. Meanwhile, game theory is a well-known tool for representing trade-offs between heterogeneous components and predicting their choices. The real-time interaction in the game-theory-based decision allows a complex system to autonomously adapt to reconfiguration when failures occur [90].

## **B. FUTURE CHALLENGES**

As the integration of information technologies and physical systems continues to expand, future industrial applications, including important infrastructures such as the power grids, will become more complicated and interdisciplinary, including numerous heterogeneous components and stakeholders. Those highly heterogeneous actors usually have their own preferences and goals. And they have to operate under a large degree of uncertainty, which will become more unpredictable and controllable [91]. The next generation of complex and inter-connected CPS does bring new challenges and also opportunities to ensure resilience and security. Intelligent, autonomous, and self-healing solutions are key [92].

Fully automated and resilient systems require monitoring and controlling all major components, ensuring the bidirectional flow of information and/or power supply such as in the form of electricity [93]. Distributed intelligence, especially with the help of a seamless interface with users, enables automated control and adaptability to a variety of uncertainties, both at a component level and a system level. Systematic approaches are expected to address 1) detection, 2) prediction, 3) analysis, 4) isolation, and 5) self-healing of failures in hardware, software, and communication. Cost economics and standardization are also important aspects for the feasibility of final solutions.

## **VI. TECHNOLOGY ETHICS AND SOCIETY**

Over the last years, modern ICT has been spread to critical parts of the business and personal life [94]. Nowadays, increasingly intelligent systems are embedded in everyday objects and assist humans in their tasks and decision-making processes, while there are clear visions of symbiosis with intelligent autonomous systems in the future [95]. Because technology is no longer a mere tool but is capable of autonomously making decisions that affect humans directly, several concerns and challenges are raised that pertain to machine ethics and the societal impact of technology that need to be investigated from multiple angles [96].

AI is one technology that exemplifies ethical and societal concerns. Although AI is not new, as it is in the making for over 50 years now, its practical applications at mass have been made possible only in the last decade due to the availability of hardware, computing resources, and Big Data to train upon. AI can be found today in consumer electronics, industrial processes, autonomous and intelligent systems, chatbots, decision-making software in police, banks, courts, etc. While before such intelligent and autonomous systems could be operated in controlled environments, e.g., a production line within a factory, nowadays such systems are envisioned and

realized within non-deterministic and highly dynamic environments, e.g., smart cities.

The trend is to integrate AI into a wide range of products and services to enhance their functionalities and provide a better interaction with the users. The reliance on AI also implies the relaxing of control from the user side and its delegation to AI to take care of trivial aspects or assist the users with their decisions. The efforts that are common in all industries and can be seen in their products raise significant concerns as most AI inclusion is considered by experts as mostly a black box that lacks explainability on how it derives decisions.

The interplay of AI and ethics can be highlighted via the example case of self-driving cars. Such intelligent AIempowered cars will make a multitude of decisions on behalf of their users, and some of them, e.g., in the case of unavoidable accidents, will be literally life and death decisions. Therefore, a key question is on which ethical frameworks and assumptions such decisions should be made upon, as well as how they can be implemented in the car. That ethics may influence the acceptance of self-driving cars [96] points out the need to consider it for the lifecycle of other AI-empowered products also. It is therefore pertinent to properly investigate how ethical frameworks can be engineered and how decisions taken by autonomous systems can properly consider them.

While new technologies can be utilized for the good of humanity, there have also been several pitfalls that raise alarms and can not be ignored not only by society but also by the engineers that develop such technologies and products. For instance, technology has been misused, e.g., unlawfully monitoring citizens, to (even unknowingly) derive biased decisions and discriminate against people, etc. Because this is an interdisciplinary grand challenge, it must be approached from different angles, i.e., go beyond the consideration of technical aspects only, towards a more holistic consideration of sociotechnical considerations that accompanies all aspects of the lifecycle of the technology and its derived products. This is easier said than done, but evidence suggests that for new industrial technologies to be accepted [97], they must strive for a balance of characteristics that include technological, business, standards, sustainability, criteria, etc. In addition, while the pursuit of engineering machine ethics can enhance the alignment between humans and machines, it also bears some risks [96], [98].

Beyond ethics, the developed solutions should also be lawful in the sense that the actions of the intelligent and autonomous systems should be in compliance with the applicable laws and regulations when they operate [96]. This implies that such constraints must be understood, embedded in the decision-making of the systems, and sufficiently linked with the context of the operating environment of the system. In addition, any developed solution must be trustworthy. In that sense, it should be fair and gain the trust of the users that it adheres to the expectations posed upon it, e.g. to perform well, lawfully, and for the benefit from the user and society at large. However, because what is lawful is not always ethical, this means that additional aspects need to be considered, modeled, and included in the decision-making processes of such systems [96]. As it can be seen, the engineering of intelligent autonomous systems that can operate in society has several challenges associated with them that go well beyond technology.

Engineering systems that integrate into an explainable form of intelligence are considered to be a grant challenge. For instance, to engineer autonomous systems that take into consideration ethical aspects, these must be included early enough at the design phase of it and potentially be fine-tuned, e.g., via simulations of the operations the systems are destined for. Therefore, the engineer of the future needs to possess inter-disciplinary knowledge that excels in technical depth and is broad enough to identify and comprehend the limitations and impacts the technology has, as well as how to realistically build such intelligent and autonomous systems that adhere to societal norms and regulations [96].

Standards are indispensable for engineering to be successful, considering the large spectrum of AI-enabled products envisioned. These would lead to the development of technologies that can be assessed on the basis of their qualities, as well as outcomes, and that are interoperable. Today there are several standards available for system integration, but the addressing of ethical and other aspects that are strongly linked to AI systems is limited, especially when they are in conjunction with physical forms such as intelligent robots or self-driving cars. Recent efforts in this area, e.g. by IEEE [99] as well as standardization bodies such as ISO/IEC/JTC1 aim to address such issues by developing new AI-relevant standards.

Education is seen as critical, especially considering the broad aspects engineers of such intelligent autonomous systems have to deal with. Academic curricula have to be expanded to combine deep technical knowledge with a more broad approach towards ethical and societal implications, as well as how to consider the different phases of product creation. Beyond academic curricula, though, what is needed are lifelong learning and especially industry training programs that enable engineers to expand their knowledge and expertise and keep up with a rapidly developing area. Thankfully with the advances of ICT, such learning and training can be done online and at a mass scale, e.g., via a massive open online course (MOOC), which has positive effects on the industry. To conclude, the knowledge and expertise requested by future engineers are increasingly demanding and multi-faceted. To exemplify this, one needs to consider that s/he should be capable of interacting with involved stakeholders, identifying and comprehending their needs, and considering societal impacts, and be capable of addressing the technical and societal needs in intelligent systems that can be deployed in real-world environments and be societally acceptable.

#### **VII. STANDARDS VIEW**

Several discussions on cross-disciplinary industrial electronics technology clusters covering trends, perspectives, changes, and challenges have been presented, focusing on the vertical clusters of IES fields of interest for building a sustainable society [13], [14]. This section extends these perspectives focusing on the inclusion of IES standards in the integration of such cross-disciplinary cluster technologies.

## A. PERSPECTIVES

To further explore the IES vertical fields of interest, the collaboration of cross-disciplinary technologies is considered. Examining the sampling of the numerous industrial applications continues to indicate the importance and needs of standards. A proposed methodology using cross-disciplinary concepts to these industrial electronics verticals is investigated, inspiring advances into further cross technological integration for society's benefit.

Feature articles from the March 2020 - September 2021 series of the IEEE Industrial Electronics Magazine (IEM) highlight the latest trends in industrial electronics technologies ranging from transportation electrification and autonomous vehicles, smart micro-grids and industrial power generation, and industrial automation and advances in automated mining. Of the 56 articles surveyed, approximately half of the articles cite or discuss standards in their applications, while eleven papers indicated the need for standards in application development. Several other articles described reference architecture frameworks in the application scenarios that could lead to standardization opportunities. In the next three sections below, a quick survey of the feature articles from the seven issues of the Industrial Electronics Magazine show trends in standards usage, industrial applications citing the need for standards, and applications with standards possibilities. The reader is invited to peruse these magazine issues for further details. These are the four quarterly IEM issues for 2020 (Vol. 14, nos. 1, 2, 3, 4) and next three issues of 2021 (Vol. 15, nos. 1, 2, 3). In addition, lack of standards adoption and inadequate co-development of standards with the communities that use it, have been identified as barriers that hinder the growth in specific domains e.g. manufacturing [100].

#### **B. TRENDS**

Within Industry4.0, standards are needed in automation models in a wide range of applications. Complex automation infrastructure modeling requires structural approaches and development discipline, and standards already adopted by industry are widely used. Industrial Cyber-Physical Systems, Industrial IoT, and industrial automation technology sectors all prefer standardized approaches to integration and conformity.

Trends, where industrial standards have an impact, include electric vehicles (EVs) and e-mobility, energy management frameworks (EMF), AI in edge computing, and topics in wireless networks utilized in the industrial Internet of Things framework and the automated mining industry. EV charging infrastructures are accelerating at a rapid pace with the aggressive push of electric vehicles in transportation applications and e-mobility. All aspects of the EV ecosystem have been improved, due to the collaborative development of EV charging standards enabling interoperability and ease-of-use in charging for a wide assortment of EVs, by the joint efforts of the infrastructure stakeholders (governments, automotive industry). In the charging infrastructure consisting of physical charging and the communications layer component for EVs, standards play a critical role in allowing the rapid deployment and acceptance of EVs in society. These standards include the International Electrochemical Commission (IEC) 61850, the common CCS standard (Combined Charging System) IEC 61851-22/23, SAE J1772 (Society of Automotive Engineers), and CHAdeMO from Japan. China and India EV manufacturers follow the China Electricity Council's Guobiao (GB/T) 20234.2/.3 standards for fast chargers.

As the world moves increasingly towards transportation electrification, the main design objectives for the efficiency and reliability, and safety of systems components for electrical machines (EM) become important, such as lifetime degradation on such components as insulation systems. Today, the safety and reliability for such systems are guaranteed due to established procedures on reliability and certification of EMs via extremely robust designs and compliance to standards such as military or avionics standards.

The emerging importance of energy management systems (EMS) in today's growth of renewable energy systems and smart grids introduced the need for energy management agents (EMA). These EMAs are integrated into energy management frameworks (EMF) utilized in homes, factories, and the grid. The EMAs are used for energy data collection and management by home electronic system gateways (HES), distributed energy resources (DER), EVs, and smart appliances. These EMAs are governed by IEC Joint Technical Committee 1 (JTC1), specifying the ISO/IEC 15067.3 and 15067.3-3 standards. An article from the 2021 March issue of the IEM (Vol. 15, no, 1) provides a comprehensive overview of EMA standards and frameworks deployed in conjunction with 5G vertical industries.

Trending in the energy smart grids and storage systems area, standards have been cited in the applications and implementation of these systems. In the review on cyber-physical microgrids, standards have been shown to play prominent roles in the monitoring, control, and resilient sections of microgrid designs, necessitated by the needs for better control, design ease, stability, reliability, and safety. Multiple standards were cited in the critical monitoring and control functions of the cyber-physical microgrids and in particular, it concluded with the need for standards in the resilience for microgrids.

On the topic of new trends in utility-scale energy storage systems, heavy emphasis was given to the importance of standards and regulations to the power electronic converter applications (PEC), and the needs for new standards in its digitalization and grid communications network areas for the ESSs. It covered international standards related to PEC, batteries, battery management systems, and addressed future challenges and trends of PECs in the ESS industry. These standards are usually created by a national or international level organization, such as IEC, UL, and the European Committee on Standardization. Future trends in the digitalization of the Energy industry require communications and control protocol standards for the ESS industry. This includes new standards needed for cybersecurity features for the PEC and ESS communications networks. In the concluding statements, it is noted the wide deployment of ESSs is limited by the lack of standards, especially so on safety regulatory and standardization issues for battery-based ESSs (BESSs).

In the report by the IES Energy Cluster of TCs, standardization approaches are highly recommended to enable the highest possible degree of interoperability when transforming electrical energy systems to smart grids. This is especially important when using an ICT and automated smart grid architecture integrating hardware and software components from multiple suppliers. For renewable energy systems, standards are being frequently reviewed and revised due to the variability of renewable energy sources affecting grid stability.

AI and Edge computing, and IIoT are currently hot topics in emerging technologies and relevant to industrial electronics. To address the three important challenges identified by research studies of edge AI for IIoT, a federated active transfer model (FATL) application is proposed. The three challenges are personalization, responsiveness, and privacy preservation. The FATL model can be deployed using industrial edge computing standards, citing IEEE P2805 standard. Here it shows an explicit example of the use of standards to address edge AI performance in IIoT solutions.

In wireless IIoT networks, the issue of cross wireless technology interference over unlicensed bands was investigated. Due to the popularity of unlicensed bands, the following popular wireless standards are used worldwide-IEEE 802.11 (wireless local area networks: WLANs), IEEE 802.15.1, IEEE 802.15.4 networks. For the two leading wireless standards in the automation field, ISA 100. 11a and WirelessHart, where cross-interference is common, another paper from the March 2021 IEM described the work on this issue by analyzing the interfering aspects of the different technologies and mitigating cross-interference to allow for enhanced co-existence on the network protocol stack layers, or for co-existence through interference aware routing. This work illustrates the need for possibly more standards to solve cross-interference issues to provide interference-free wireless IIoT networks using heterogeneous devices.

A key article covering the industrial revolution since the 1950 s, industrial electronics and industrial informatics provided solid foundations in the design and development of industrial ICT over the lifecycle of products, processes, and systems and adhering to the IEC 62890 standards. Following this, in new emerging technologies such as industrial CPSs (ICPS), Industrial Agents (IA) are seen as key enablers for the realization of ICPS, and multiple standards have been established in the IA domain. Here, the article shows the evident need to address IA integration and communications with low-level real-time control systems integration. It is evidently clear standards are needed to effectively embed IA into the ICPS domain.

The special issue on advances in mining automation presented in the September 2021 issue of the Industrial Electronics Magazine (Vol. 15, no. 3) was especially relevant in standards, where almost all the five articles devoted to mining automation cited standards are essential in the industry. The lead article in this special issue provides a good overview of industrial electronics technologies used in practice in the present and future trends in mining automation. One clear example of standards used in the industrial academia collaboration is knowledge sharing of the Open Process Automation Standards testbeds. Safety is a paramount factor in the mining industry, which is a high-risk industry. A paper discussing 'progress toward zero entry mining' advocates truly autonomous mining operations without humans entering the mining areas. Numerous examples of safety issues were covered under safety standards guidelines governed by the Commonwealth Scientific and Industrial Research Organization (CSIRO) and various industry consortia.

A comprehensive view on the use of emerging digitization and industrial electronics to modernize and assist the mining industry provided great insights into the use of interoperability and digital twins. Standards were liberally cited as essential in the mining operations as well as needs where it is not available. A two-part series of articles introduced companies engaged in the deployment of digital technologies, and discusses the use of integration platforms and digital twins interoperability technologies for the mining operations. In particular, detailed integration platforms and digital twins techniques advocate heavy innovation and adoption in the mining industry. The article cited the Common Mine Model, a digital twins concept first introduced to the mining industry by CSIRO in 2009. In South Africa, where mining is the secondlargest employer, the industry has introduced mechanization and automation (mechanized mining) as improvements to the traditional labor-intensive drill-and-blast approach. Moreover, mechanized mining provides improved productivity and safety. With this approach, the use of wireless positioning in underground mines provides context awareness of machinery in tunnels and other critical pathways. Wireless techniques considered include Wi-Fi, Ultrawideband, Bluetooth, 5G, and long-range approaches. However, since there is no single technology that is suitable for all use cases, the wireless approach requires quite a lot of effort. Therefore, the lack of sustained interoperability and standardization efforts presently hampers the widespread use of wireless in underground mines. This makes a very strong case for the need for standards in the wireless applications approaches in the mining industry.

#### C. NEED FOR STANDARDS

As new technological trends evolve, generating new developments and applications, standards will not be introduced or considered until trends come into focus and stabilization. This section reviews the common theme that new technologies and their applications look to standards for stability. Eleven brief examples here cite the strong need for standards, as culled from the survey articles mentioned earlier.

New solid-state transformers (SST) introduced into existing electrical systems brought challenges in the interfaces, stabilization, and costs during the integration process. These challenging situations caused the industry to call for SST standards for better product integration processes and usage. This was cited as a necessary requisite for the commercial acceptance of SSTs.

Another emerging technology coming to maturity calls for the need for standardized substitute fault diagnosis tests for Lithium-Ion Battery Systems (LIBS). The challenging issues here are there are no standardized evaluation methods for LIBS fault diagnosis and calls for the immediate need for standardized substitute tests for LIBS faults.

In multiterminal (MT) high-voltage dc (HVdc) (MTdc) grid technology applications, the test procedures for the operation and implementation of protection solutions strongly emphasized the need for standardized procedures and developing standards. These procedures contribute to the dc protection system design and testing standards [101]. IEEE and IEC standards such as *IEEE Guide for Power System Protection Testing*, (IEEE C37.233, 2009) and *IEC 60255-1, 2009* series of standards (*Generic Requirements for Measuring Relays and Protection Equipment*) are the present methods used.

The most common weakness in the design and development of wind turbines (WT) is the lack of common guidelines, best practices, and standards [102]. This is especially focused on the lack of standards in the LIDAR (light detection and ranging) technologies used in performance enhancements of WT controllers. It is quoted that "...the opinions of wind industry experts reveal the main issues for LIDAR technologies relate to providing common guidelines and standards as well as risk evaluation and reliability concerns...".

Future research into real-time-based testing of modern energy systems will entail more complex cyber-physical and multi-domain processes that transform the energy grid to a complex ecosystem of heterogeneous (cooperating) entities that interact in order to provide the envisioned functionality. In an article summarizing real-time simulation and hardwarein-the-loop (HIL) based validation and testing, the conclusion was that future work requires more harmonization and standardization, citing the need for such standards as IEEE P2004. This standard is a recommended practice standard for realtime system/HIL tools.

In investigating concepts, advantages, and applications of hybrid energy storage systems (HESS), researchers highlighted the advantages of HESS specifically for attaining the distributed smart energy paradigm and zero-emissions transportation systems. In its discussion on trends and perspectives, one of the main barriers and challenges that the HESS market needs to overcome is in developing specific regulations for HESSs, in other words, some form of standardization under regulatory control.

One interesting application that looks promising in the need for standards is in noise mapping procedures to combat the issues of noise pollution in industrial environments [103]. Here an entire architecture reference model has been described, where research is carried out to contain this pollution issue, especially with the rapid deployment of IIoT. While the reference architecture framework provides a collaborative computing layer including computing networks in sensing, fog, and cloud, wireless standards have already been used, such as proprietary 2.4 GHz protocol stacks, Bluetooth, and IEEE 802.15.4. This indicates the universal use of standards where available, and for this application, in the communications layer. However, suffice to say that as the reference architecture gets more developed and refined, there will be more opportunities in the different architecture layers for standards development.

In the *Trends* section above, five areas actually strongly cited the needs for standards in the various applications of technologies, notably the use of industrial agents, Utility Scale ESSs, and wireless positioning of underground mines. Additionally, strong safety standards are advocated for the mining industry, and the need for standards in the interoperability, integration, and digital twins applications in automated mining. This section shows the importance of standards and their necessity in new technologies that are exploding in today's high technology society. Highly reliable standards and standardization contributes to society's safety, lowered costs both in consumer and manufacturing prices, and ease of use of products. The examples given above emphasize that new technology trends need and benefit from standardization once it achieves stabilization.

#### **D. STANDARDS POSSIBILITIES**

While standards may not be necessary at this time, it is notable that the following industrial electronics trends might one day require standards for industrial and commercial widespread usage and safety considerations, cost reduction, and ease of use. These trends include intelligent industrial informatics, the application of AI in wireless networks for IIoT, and methods for harvesting vibration energy as an alternate power source. Then there is a specialized application area trending in the deployment of industrial electronics technologies in closed ecosystems (CES) applications for outer space missions.

With the resurgence of AI, machine and deep learning, industrial informatics practitioners embrace this by developing intelligent information informatics. Future directions and current development of AI in industrial informatics are focused on five primary domains in factories, CPSs, industrial processes, transport, and energy. Here, a reference architecture framework was presented with AI applications integrated with industrial informatics. Noting the detailed description of the architecture covering several layers of the reference framework designed for intelligent industrial informatics, it leads to speculation that once the reference framework matures and is developed into various industrial applications usage, these reference framework components can become standards on their own in whole or in part, with the backing of its practitioners and stakeholders from the aforementioned domains.

Continuing on this trend on AI, overcoming the challenges of incorporating AI in wireless networks for IIoT was investigated by focusing on areas of AI in the IIoT generic network architecture. The three levels in the architecture covered IoT networks, the backhaul networks, and the operator network cloud, with corresponding challenges identified such as communications overhead, latency, security caching and routing, and increased complexity, to name a few. After listing the challenges of AI in the wireless network infrastructure, a roadmap for a generalized global AI architecture is proposed. Again, as stated earlier, once the reference architecture matures, these framework components and its protocols can become standards standardizing AI into wireless networks and improve on the legacy networks it represents, such as WLANs or cellular networks (e.g., 5G/6G). Earlier, a few other wireless network research trends can also be tied with this example into an overall future IIoT wireless network and its standards.

Another novel example of an application in need of standards is the vibration energy harvester product and its usage. Alternate power sources in low power applications looked to vibrational energy harvesters (VEHs), with such advantages over batteries in that it does not require replacement and reinstallation, and more importantly, when used in IoT environments, battery-powered devices can number in the hundreds. It is often inaccessible for power source replacement or costly in battery replacement due to its large numbers. However, at the moment, VEHs are a niche market, and questionable in terms of long-term marketability and profitability. Moreover, VEHs are often not standardized, and it is concluded that for profitability and market acceptance, standardization of VEHs is necessary, to reduce costs and simplify the installation process. The above two examples on AI in wireless networks and VEHs were illustrated from the March 2021 issue of IEM (Vol. 15, no. 1) Lastly, one interesting application with the use of standards is in a specialized area of outer space systems, for the implementation and operation of closed ecological systems (CESs) which are self-sustaining life support systems (LSSs) for long-duration human space missions. An article in the June 2021 issue of IEM (Vol. 15, no. 2) describes the hierarchical control of space CES, where it is simply put as likened to islanded microgrids (MGs). Several standards govern the operation and control of MGs, such as IEC 62898-1, IEC/TS 62898-2, IEC 62898-1-3, and IEEE 2030.7-2017. Additionally, ANSI/ISA-95, an automation system design and implementation international standard for all industries, is applied to the hierarchical control structure of the MG for CES.

## VIII. METHODOLOGY FOR CROSS-DISCIPLINARY TECHNOLOGY INTEGRATION AND ITS IMPLEMENTATION

As explained earlier in this paper, cross-disciplinary considerations of the industrial electronics technologies are important for the industry, where standards and business play key roles in the adoption of solutions in addition to technical results [97]. Requirements beyond pure technological factors should be considered to enable the adoption of new innovative technologies. With that, a suggested methodology of how collaboration and integration of cross-disciplinary cluster technologies can benefit IES vertical cluster technologies was originally proposed in the conference paper [14]. Fig. 2 [14] illustrates the interoperability and integration of the cluster technologies in expanded details of the presented methodology.

Starting by applying the cross-disciplinary intra-cluster methodology to a robotic walker with standing/sitting assistance capabilities [13], each cross-disciplinary technology contributes its respective solution to the problem at hand. The first cross-disciplinary technology of note is human factors, where its principles are applied impacting the design and application of the robotic walker, providing ease of use and comfort for the disabled or assisted elderly user. To aid in the comfort and mobility of the water, many supportive and wearable components are designed in the product, requiring electronic chips to be integrated into the design due to space and weight constraints.

With the increasing deployment of technologies in user applications in today's society, miniaturized electronic systems on a chip are most likely incorporated into assistive devices for the elderly and disabled, wearables, and light-weight robotic walkers. Following closely on these technologies, design considerations for resilience and safety are embedded into such assistive devices and systems, where such factors as self-healing, device resiliency, and 'fail-safe' modes must be built-in to both hardware and software ensuring the ease of use and safety to the elderly or disabled user, as well as 'peace of mind' in device usage. Together with human factors, electronic systems on chip, and resilience and security for industrial applications, heavy emphasis and thought must be placed on technology ethics and societal aspects (TES) of the design of the product in terms of considerations for race, ethnicity, gender, language, age bias, and any other discriminatory effects.

Following the acceptance and stabilization of the designs, the design requirements and implementation practices can be standardized for mass production, ensuring fast implementation and deployment of products, with lowered costs, to the consumer. The education on the concepts, requirements, and the use of the product, both for the user and the training of production personnel will be the focus of the Education cluster (EDU). These last two cross-disciplinary technical components are represented as 'full rings' around the intra-cluster methodology as it 'pervades' all aspects of the other technology clusters. This is also true for the TES, where ethics and societal impact encompasses the lifecycle of the developed products from concept to engineering to eventual disposition.

Technical committees in Cluster 4 are committed to a 'Proof of Concept' (PoC) trial implementation of the proposed

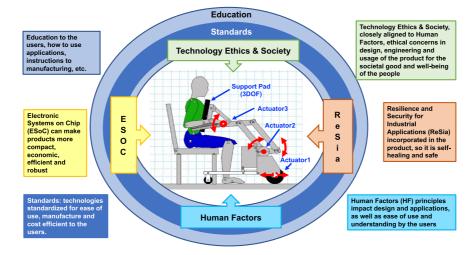


FIGURE 2. A suggested cross-disciplinary intra-cluster methodology.

Step	Description	Output
Discussion of	All stakeholders	Main system
objectives	discuss system	objectives
	objectives	
Definition of	Define objectives	Discipline-specific
discipline-specific	inside each TC's	objectives (human
objectives	field of expertise	factors, education,
	•	etc.)
Constraint	Identify constraints	Physical,
identification	in the project	physiological, and
	1 0	other constraints
Definition of	Derive requirements	Hardware and
requirements	from the objectives	software
*	and constraints	requirements,
		minimum
		requirements, and
		recommended
		requirements
Definition of	Group requirements	Subsystem list and
subsystems	into subsystems.	requirements
Subsystem	Each team	Hardware and
implementation	implements	software of
implementation	subsystems in	subsystems of the
	parallel	project
Subsystem	Confirm the	Acceptability, cost,
verification	implementation of	sustainability, etc. of
vermeation	assigned	sub-systems
	requirements for	sub-systems
	each subsystem	
Sustam integration	Integrate subsystems	Hardware and
System integration	to form the whole	
		software of the
Sustam varificati	system Convert	System Quality control
System verification		~ /
	requirements into	measures,
	test cases and	acceptability, cost,
	perform functional	sustainability, etc.
	and interconnection	
	tests	
System validation	Review and collect	Project review,
	performance	report, and users'
	information and	manual
	complete project	
	report	

methodology with a selected vertical within the IES community. Preliminary development stages consist of a requirement stage, an implementation stage, a testing-and-validation stage, and concluding with a successful trial complete with instruction documentation and manuals developed by an education group. Relevant standards will be utilized, and new interoperable technologies or solutions will be studied to assess its needs for standardization, based on its generic applications or focused applications needs.

A project to define and implement a robotic walker with assistance capabilities was launched in March 2022 by Cluster 4. The project has ten steps from the discussion of the objectives to system validation (Table 2). The items in each step will be modified during the project based on collaboration results between technical committees. In the beginning, each technical committee inputs requirements, considerations, constraints, and others from the viewpoint of the committee. Then, teams are formed to work on subsystems in parallel. Such a team does not need to have expertise in all the different disciplines inside the cluster and is involved in a collaboration between two or more TCs. At the final validation step, All TCs review and modify the items again, and check the achievement of both the main system objectives and all the discipline-specific objectives. At the requirement stage, technical requirements for each cluster member group are clearly laid out and described guiding the development and validation stages. Within each development stage, the principles from each technology of the cluster will be evaluated, embedded, and validated. The success of the project will be determined by showing clear identification of each expert technology in the PoC. This project will contribute to SDGs 3 (ensure healthy lives and promote well-being for all at all ages) and 9 (build resilient infrastructure, promote inclusive and sustainable industrialization, and foster innovation). The achievements of this project are also considered to build project-based learning materials for engineers. This will contribute to SDG 4 (quality education).

## **IX. CONCLUSION**

This paper explained efforts, new trends, and challenges to create a sustainable society from the viewpoints of human factors, education, electronics systems-on-chip approaches, resilience and security for industrial applications, technology ethics and society, and standards. Since the seventeen SDGs [1] are multiple cross-cutting issues, it is impossible to attain these goals without interdisciplinary studies and cooperation with and among different fields. Awaking to the importance and urgency of these points, the technical committees in Cluster 4 of IES have been making a constant effort and working together to meet these challenges and achieve these goals. A near-term task is the development of a PoC trial for the methodology demonstration of the cross-disciplinary technology integration. A future task is to attract young generations of professionals from both industrial and academic sectors to the activities of Cluster 4 to contribute to the sustainable growth of society.

#### ACKNOWLEDGMENT

All authors would like to thank the countless members that work within the Technical Committees of IEEE IES in Cluster 4. Hipólito Guzmán-Miranda wants to thank Claire Xenia Wolf and Matt Venn from YosysHQ for the fruitful discussions about the legal challenges in the development and usage of a free and open-source toolchain for FPGAs.

#### REFERENCES

- United Nations, "Transforming our world: The 2030 agenda for sustainable development," A/RES/70/1, Dec. 2015. [Online]. Available: https://sdgs.un.org/2030agenda
- "Industrial electronics society, latin america working group and IEEE Honduras section precedent setting project completed," Jun. 2021.
  [Online]. Available: https://smartvillage.ieee.org/news/empower-vol-2-issue-5-june-2021/
- [3] K. Panetta, "Welcome to IEEE women in engineering magazine [letter from the editor]," *IEEE Women Eng. Mag.*, vol. 1, no. 1, pp. 2–3, Winter 2007, doi: 10.1109/wie-m.2007.4510827.
- [4] V. Huang, A. Chen, and D. Bruckner, "The standards and interoperability plugfest at IECON 2020 [society news]," *IEEE Ind. Electron. Mag.*, vol. 15, no. 1, pp. 95–98, Mar. 2021, doi: 10.1109/mie.2021.3054456.
- "IEEE IES Technical Committee on Technology Ethics and Society," [Online]. Available: https://tes.ieee-ies.org
- [6] C. Yeh *et al.*, "SustainBench: Benchmarks for monitoring the sustainable development goals with machine learning," 2021, *arXiv:2111.04724*.
- [7] M. R. Cruz, D. Z. Fitiwi, S. F. Santos, and J. P. Catalão, "A comprehensive survey of flexibility options for supporting the low-carbon energy future," *Renewable Sustain. Energy Rev.*, vol. 97, pp. 338–353, Dec. 2018, doi: 10.1016/j.rser.2018.08.028.
- [8] N. Kishor, A. Srivastava, and H. Pota, "Guest editorial: Special section on "deep learning and data analytics to support the smart grid operation with renewable energy"," *IEEE Trans. Ind. Informat.*, vol. 17, no. 10, pp. 6935–6938, Oct. 2021, doi: 10.1109/tii.2021. 3072770.
- [9] IEEE Sustainable ICT, "IEEE sustainable ICT initiative white paper: A smart and sustainable world through ICT," Institute of Electrical and Electronics Engineers, Tech. Rep., 2020. [Online]. Available: https: //sustainableict.ieee.org
- [10] E. Chang, K. Y. Chan, P. Clark, and V. Potdar, "Guest editorial: Blockchain and AI enabled 5G mobile edge computing," *IEEE Trans. Ind. Informat.*, vol. 16, no. 11, pp. 7067–7069, Nov. 2020, doi: 10.1109/tii.2020.2983764.
- [11] S. Karnouskos, "Blockchain for development in the era of the COVID-19 pandemic," *IEEE Open J. Ind. Electron. Soc.*, vol. 2, pp. 556–567, Oct. 2021, doi: 10.1109/ojies.2021.3121549.
- [12] A. W. Colombo, S. Karnouskos, O. Kaynak, Y. Shi, and S. Yin, "Industrial cyberphysical systems: A backbone of the fourth industrial revolution," *IEEE Ind. Electron. Mag.*, vol. 11, no. 1, pp. 6–16, Mar. 2017, doi: 10.1109/mie.2017.2648857.

- [13] O. Lucia *et al.*, "Emerging trends in industrial electronics: A cross-disciplinary view," *IEEE Ind. Electron. Mag.*, vol. 15, no. 1, pp. 127–139, Mar. 2021, doi: 10.1109/mie.2020.3032942.
- [14] J. She *et al.*, "A cross-disciplinary view of industrial electronics: Change, chance, and challenge," in *Proc. IECON* 47th Annu. Conf. IEEE Ind. Electron. Soc., 2021, pp. 1–7, doi: 10.1109/iecon48115.2021.9589742.
- [15] H. Ono and S. Suzuki, "Data augmentation for grossmotor-activity recognition using DCGAN," in *Proc. IEEE/SICE Int. Symp. Syst. Integration*, 2020, pp. 440–443, doi: 10.1109/sii46433.2020.9026252.
- [16] D. Chugo *et al.*, "Standing assistance control based on voluntary body movement within safety tolerance," in *Proc. IEEE 16th Int. Workshop Adv. Motion Control*, 2020, pp. 177–182, doi: 10.1109/amc44022.2020.9244314.
- [17] M. Suzuki, S. Yokota, A. Matsumoto, D. Chugo, and H. Hashimoto, "Simulation of omni-directional low-floor mobility controlled by inverted pendulum and human postural control model in forward-backward direction," in *Proc. IECON 46th Annu. Conf. IEEE Ind. Electron. Soc.*, 2020, pp. 2668–2674, doi: 10.1109/iecon43393.2020.9254558.
- [18] J. She, Y. Ohyama, M. Wu, and H. Hashimoto, "Development of electric cart for improving walking ability — application of control theory to assistive technology," *Sci. China Inf. Sci.*, vol. 60, no. 12, Nov. 2017, doi: 10.1007/s11432-017-9261-1.
- [19] K. Makino *et al.*, "Classification of a pincer nail using a recurrentbased neural network," in *Proc. IEEE Int. Symp. System Integration*, 2020, pp. 249–252, doi: 10.1109/sii46433.2020.9025990.
- [20] L. M. Contreras-Somoza *et al.*, "Study on the acceptability of an ICT platform for older adults with mild cognitive impairment," *J. Med. Syst.*, vol. 44, no. 7, pp. 1–12, May 2020, doi: 10.1007/s10916-020-01566-x.
- [21] H. Wang *et al.*, "Driving fatigue recognition with functional connectivity based on phase synchronization," *IEEE Trans. Cogn. Devel. Syst.*, vol. 13, no. 3, pp. 668–678, Sep. 2021, doi: 10.1109/tcds.2020.2985539.
- [22] W. Karwowski, A. Szopa, and M. M. Soares, Eds., Handbook of Standards and Guidelines in Human Factors and Ergonomics, 2nd ed. Boca Raton, FL, USA: CRC Press, 2021.
- [23] G. Salvendy and W. Karwowski, Eds., Handbook of Human Factors and Ergonomics, 5th ed. Hoboken, NJ, USA: Wiley, 2021.
- [24] Z. Kemény, R. J. Beregi, G. Erdös, and J. Nacsa, "The MTA SZTAKI smart factory: Platform for research and project-oriented skill development in higher education," *Procedia CIRP*, vol. 54, pp. 53–58, 2016, doi: 10.1016/j.procir.2016.05.060.
- [25] C. A. Maida, "Project-based learning: A critical pedagogy for the twenty-first century," *Policy Futures Educ.*, vol. 9, no. 6, pp. 759–768, Jan. 2011, doi: 10.2304/pfie.2011.9.6.759.
- [26] E. Abele *et al.*, "Learning factories for research, education, and training," *Procedia CIRP*, vol. 32, pp. 1–6, 2015, doi: 10.1016/j.procir.2015.02.187.
- [27] L. Abeysekera and P. Dawson, "Motivation and cognitive load in the flipped classroom: Definition, rationale and a call for research," *Higher Educ. Res. Develop.*, vol. 34, no. 1, pp. 1–14, Aug. 2014, doi: 10.1080/07294360.2014.934336.
- [28] D. Ktoridou, E. Doukanari, E. Epaminonda, and A. Karayiannis, "Case-based learning: Offering a premier targeted learning experience for technology management students," in *Proc. IEEE Glob. Eng. Educ. Conf.*, 2018, pp. 1781–1786, doi: 10.1109/educon.2018.8363450.
- [29] R. Bekkers and I. M. Bodas Freitas, "Analysing knowledge transfer channels between universities and industry: To what degree do sectors also matter?," *Res. Policy*, vol. 37, no. 10, pp. 1837–1853, Dec. 2008, doi: 10.1016/j.respol.2008.07.007.
- [30] B. Marshall, "Hardware verification in an open source context," in Proc. 1st Worshop on Open Source Des. Automat. Workshop 10 Des., Automat. Test Europe conf., Florence, Italy, pp. 1–6, 2019. [Online]. Available: https://osda.gitlab.io/19/1.2.pdf
- [31] D. Shah, E. Hung, C. Wolf, S. Bazanski, D. Gisselquist, and M. Milanovic, "Yosys+nextpnr: An open source framework from verilog to bitstream for commercial FPGAS," in *Proc. IEEE 27th Annu. Int. Symp. Field-Programmable Custom Comput. Machines*, 2019, pp. 1–4, doi: 10.1109/fccm.2019.00010.
- [32] C. Lavin and A. Kaviani, "RapidWright: Enabling custom crafted implementations for FPGAS," in *Proc. IEEE 26th Annu. Int. Symp. Field-Programmable Custom Comput. Machines*, 2018, pp. 133–140, doi: 10.1109/fccm.2018.00030.

- [33] T. Gingold *et al.*, "GHDL: Free and open-source analyzer, compiler, simulator and (experimental) synthesizer," [Online]. Available: https: //ghdl.github.io/ghdl/
- [34] S. Williams, "Icarus Verilog," [Online]. Available: https://http:// iverilog.icarus.com/
- [35] Veripool, "Verilator," [Online]. Available: https://www.veripool.org/ verilator/
- "VUnit, a test framework for HDL," [Online]. Available: https://vunit. github.io/
- [37] "Cocotb, a coroutine based cosimulation library for writing VHDL and verilog testbenches in Python," [Online]. Available: https://docs. cocotb.org
- [38] C. Wolf, "Yosys open synthesis suite," [Online]. Available: https: //yosyshq.net/yosys/
- [39] T. Gingold, "GHDL-yosys-plugin: VHDL synthesis (based on GHDL)," [Online]. Available: https://github.com/ghdl/ghdl-yosysplugin
- [40] C. Wolf and M. Lasser, "Project icestorm," [Online]. Available: http: //bygone.clairexen.net/icestorm/
- [41] "Project trellis: Documenting the lattice ECP5 bit-stream format," [Online]. Available: https://prjtrellis.readthedocs.io
- [42] "Project X-ray: Documenting the Xilinx 7-series ECP5 bit-stream format," [Online]. Available: https://prjxray.readthedocs.io
- [43] O. Kindgren *et al.*, "Edalize: An abstraction library for interfacing EDA tools," [Online]. Available: https://github.com/olofk/edalize
- [44] C. A. R. Naranjo and I. P. Rojo, "TerosHDL, an open source IDE for FPGA/ASIC," [Online]. Available: https://terostechnology.github. io/terosHDLdoc/
- [45] M. Muñoz-Quijada, L. Sanz, and H. Guzman-Miranda, "A virtual device for simulation-based fault injection," *Electronics*, vol. 9, no. 12, Nov. 2020, Art. no. 1989, doi: 10.3390/electronics9121989.
- [46] C. Krieg, C. Wolf, and A. Jantsch, "Malicious lut: A stealthy FPGA Trojan injected and triggered by the design flow," in *Proc. 35th Int. Conf. Comput.-Aided Des.*, 2016, pp. 1–8, doi: 10.1145/2966986.2967054.
- [47] N. Steiner and P. Athanas, "An alternate wire database for xilinx FP-GAs," in *Proc. 12th Annu. IEEE Symp. Field-Programmable Custom Comput. Machines*, 2004, pp. 336–337, doi: 10.1109/fccm.2004.13.
- [48] S. Raaijmakers and S. Wong, "Run-time partial reconfiguration for removal, placement and routing on the virtex-II pro," in *Proc. Int. Conf. Field Programmable Log. Appl.*, 2007, pp. 679–683, doi: 10.1109/fpl.2007.4380744.
- [49] S. Furber and P. Bogdan, Eds., SpiNNaker: A Spiking Neural Network Architecture. Boston, MA, USA: Now Publishers, Mar. 2020.
- [50] P. A. Merolla *et al.*, "A million spiking-neuron integrated circuit with a scalable communication network and interface," *Science*, vol. 345, no. 6197, pp. 668–673, Aug. 2014, doi: 10.1126/science.1254642.
- [51] K. Boahen, "Neurogrid: Emulating a million neurons in the cortex," in *Proc. Int. Conf. IEEE Eng. Med. Biol. Soc.* 2006, pp. 6702–6702, doi 10.1109/iembs.2006.260925.
- [52] M. Davies *et al.*, "Loihi: A neuromorphic manycore processor with on-chip learning," *IEEE Micro*, vol. 38, no. 1, pp. 82–99, Jan. 2018, doi: 10.1109/mm.2018.112130359.
- [53] C. Szegedy et al., "Going deeper with convolutions," in Proc. IEEE Conf. Comput. Vis. Pattern Recognit., 2015, pp. 1–9, doi: 10.1109/cvpr.2015.7298594.
- [54] K. He, X. Zhang, S. Ren, and J. Sun, "Deep residual learning for image recognition," in *Proc. IEEE Conf. Comput. Vis. Pattern Recognit.*, 2016, pp. 770–778, doi: 10.1109/cvpr.2016.90.
- [55] G. Huang, Z. Liu, L. Van Der Maaten, and K. Q. Weinberger, "Densely connected convolutional networks," in *Proc. IEEE Conf. Comput. Vis. Pattern Recognit.*, 2017, pp. 4700–4708, doi: 10.1109/cvpr. 2017.243.
- [56] B. Zoph, V. Vasudevan, J. Shlens, and Q. V. Le, "Learning transferable architectures for scalable image recognition," in *Proc. IEEE/CVF Conf. Comput. Vis. Pattern Recognit.*, 2018, pp. 8697–8710, doi: 10.1109/cvpr.2018.00907.
- [57] J. Fowers et al., "A configurable cloud-scale DNN processor for real-time AI," in Proc. ACM/IEEE 45th Annu. Int. Symp. Comput. Architecture, 2018, pp. 1–14, doi: 10.1109/isca.2018.00012.
- [58] H. Kwon, A. Samajdar, and T. Krishna, "Maeri," in Proc. 23rd Int. Conf. Architectural Support Program. Lang. Operating Syst., 2018, doi: 10.1145/3173162.3173176.

- [59] S. Zhang *et al.*, "Cambricon-X: An accelerator for sparse neural networks," in *Proc. 49th Annu. IEEE/ACM Int. Symp. Microarchitecture*, 2016, pp. 1–12, doi: 10.1109/micro.2016.7783723.
- [60] B. Liu, X. Chen, Y. Han, and H. Xu, "Swallow: A versatile accelerator for sparse neural networks," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 39, no. 12, pp. 4881–4893, Dec. 2020, doi: 10.1109/tcad.2020.2978836.
- [61] Y.-H. Chen, T. Krishna, J. S. Emer, and V. Sze, "Eyeriss: An energyefficient reconfigurable accelerator for deep convolutional neural networks," *IEEE J. Solid-State Circuits*, vol. 52, no. 1, pp. 127–138, Jan. 2017, doi: 10.1109/jssc.2016.2616357.
- [62] Xilinx, "Versal: The first adaptive compute acceleration platform (ACAP)" Xilinx, Tech. Rep., Sep. 2020, white paper. [Online]. Available: https://www.xilinx.com/support/documentation/ white\_papers/wp505-versal-acap.pdf
- [63] D. T. Nguyen, T. N. Nguyen, H. Kim, and H.-J. Lee, "A highthroughput and power-efficient FPGA implementation of YOLO CNN for object detection," *IEEE Trans. Very Large Scale Integration Syst.*, vol. 27, no. 8, pp. 1861–1873, Aug. 2019, doi: 10.1109/tvlsi.2019.2905242.
- [64] X. Chen and Z. Yu, "A flexible and energy-efficient convolutional neural network acceleration with dedicated ISA and accelerator," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 26, no. 7, pp. 1408–1412, Jul. 2018, doi: 10.1109/tvlsi.2018.2810831.
- [65] S. Choi, J. Sim, M. Kang, Y. Choi, H. Kim, and L.-S. Kim, "An energy-efficient deep convolutional neural network training accelerator for in Situ personalization on smart devices," *IEEE J. Solid-State Circuits*, vol. 55, no. 10, pp. 2691–2702, Oct. 2020, doi: 10.1109/jssc.2020.3005786.
- [66] F. Zhang, J. Zhai, B. Wu, B. He, W. Chen, and X. Du, "Automatic irregularity-aware fine-grained workload partitioning on integrated architectures," *IEEE Trans. Knowl. Data Eng.*, vol. 33, no. 3, pp. 867–881, Mar. 2021, doi: 10.1109/tkde.2019.2940184.
- [67] J. Nunez-Yanez et al., "Parallelizing workload execution in embedded and high-performance heterogeneous systems," CoRR, 2018, arXiv:1802.03316.
- [68] A.-h. M. A. Noaman, A. Rafiev, F. Xia, R. Shafik, A. Romanovsky, and A. Yakovlev, "PARMA: Parallelization-aware runtime management for energy-efficient many-core systems," *IEEE Trans. Comput.*, vol. 69, no. 10, pp. 1507–1518, Oct. 2020, doi: 10.1109/tc.2020.2975787.
- [69] H. Khaleghzadeh, M. Fahad, A. Shahid, R. R. Manumachu, and A. Lastovetsky, "Bi-objective optimization of data-parallel applications on heterogeneous HPC platforms for performance and energy through workload distribution," *IEEE Trans. Parallel Distrib. Syst.*, vol. 32, no. 3, pp. 543–560, Mar. 2021, doi: 10.1109/tpds.2020.3027338.
- [70] H. Khaleghzadeh, R. R. Manumachu, and A. Lastovetsky, "A hierarchical data-partitioning algorithm for performance optimization of data-parallel applications on heterogeneous multi-accelerator NUMA nodes," *IEEE Access*, vol. 8, pp. 7861–7876, 2020, doi: 10.1109/access.2019.2959905.
- [71] J. Chen, K. Li, K. Bilal, X. Zhou, K. Li, and P. S. Yu, "A bilayered parallel training architecture for large-scale convolutional neural networks," *IEEE Trans. Parallel Distrib. Syst.*, vol. 30, no. 5, pp. 965–976, May 2019, doi: 10.1109/tpds.2018.2877359.
- [72] Z. Wang, K. Xu, S. Wu, L. Liu, L. Liu, and D. Wang, "Sparse-YOLO: Hardware/software co-design of an FPGA accelerator for YOLOV2," *IEEE Access*, vol. 8, pp. 116569–116585, 2020, doi: 10.1109/access.2020.3004198.
- [73] A. Kroh and O. Diessel, "A short-transfer model for tightly-coupled CPU-FPGA platforms," in *Proc. Int. Conf. Field-Programmable Tech*nol., 2018, pp. 366–369, doi: 10.1109/fpt.2018.00075.
- [74] M. Goudarzi, H. Wu, M. Palaniswami, and R. Buyya, "An application placement technique for concurrent IoT applications in edge and fog computing environments," *IEEE Trans. Mobile Comput.*, vol. 20, no. 4, pp. 1298–1311, Apr. 2021, doi: 10.1109/tmc.2020.2967041.
- [75] X. Xu *et al.*, "A computation offloading method over Big Data for IoTenabled cloud-edge computing," *Future Gener. Comput. Syst.*, vol. 95, pp. 522–533, Jun. 2019, doi: 10.1016/j.future.2018.12.055.
- [76] R. Mahmud, A. N. Toosi, K. Ramamohanarao, and R. Buyya, "Context-aware placement of industry 4.0 applications in fog computing environments," *IEEE Trans. Ind. Informat.*, vol. 16, no. 11, pp. 7004–7013, Nov. 2020, doi: 10.1109/tii.2019.2952412.

- [77] D. O'Loughlin, A. Coffey, F. Callaly, D. Lyons, and F. Morgan, "Xilinx vivado high level synthesis: Case studies," in *Proc. 25th IET Ir: Signals Syst. Conf. China-Ireland Int. Conf. Inf. Communities Technol.*, Institution of Engineering and Technology, 2014, pp. 352–356, doi: 10.1049/cp.2014.0713.
- [78] "Amaranth: A modern hardware definition language and toolchain based on python," [Online]. Available: https://github.com/amaranthlang/amaranth
- [79] M. Pelcat, C. Bourrasset, L. Maggiani, and F. Berry, "Design productivity of a high level synthesis compiler versus HDL," in *Proc. Int. Conf. Embedded Comput. Syst.: Architectures, Model. Simul.*, 2016, pp. 140–147, doi: 10.1109/samos.2016.7818341.
- [80] R. Krishnamoorthy *et al.*, "Systematic approach for state-of-theart architectures and system-on-chip selection for heterogeneous IoT applications," *IEEE Access*, vol. 9, pp. 25594–25622, 2021, doi: 10.1109/access.2021.3055650.
- [81] A. Al-Ali, I. A. Zualkernan, M. Rashid, R. Gupta, and M. Alikarar, "A smart home energy management system using IoT and Big Data analytics approach," *IEEE Trans. Consum. Electron.*, vol. 63, no. 4, pp. 426–434, Nov. 2017, doi: 10.1109/tce.2017.015014.
- [82] G. Fedrecheski, L. C. C. De Biase, P. C. Calcina-Ccori, and M. K. Zuffo, "Attribute-based access control for the swarm with distributed policy management," *IEEE Trans. Consum. Electron.*, vol. 65, no. 1, pp. 90–98, Feb. 2019, doi: 10.1109/tce.2018.2883382.
- [83] H. D. Foster, "2018 FPGA functional verification trends," in *Proc. 19th Int. Workshop Microprocessor SOC Test Verification*, 2018, pp. 40–45, doi: 10.1109/mtv.2018.00018.
- [84] C. Ji, Y. Wei, and H. V. Poor, "Resilience of energy infrastructure and services: Modeling, data analytics, and metrics," *Proc. IEEE*, vol. 105, no. 7, pp. 1354–1366, Jul. 2017, doi: 10.1109/jproc.2017.2698262.
- [85] S. O. Johnsen and S. S. Kilskar, "A review of resilience in autonomous transport to improve safety and security," in *Proc. 30th Eur. Saf. Rel. Conf., 15th Probabilistic Saf. Assessment Manage. Conf.*, Nov. 2020, pp. 5059–5066, doi: 10.3850/978-981-14-8593-0.
- [86] D. Gritzalis, M. Theocharidou, and G. Stergiopoulos, Eds., *Critical Infrastructure Security and Resilience*. Berlin, Germany: Springer, 2019.
- [87] S. Poudel, A. Dubey, and A. Bose, "Risk-based probabilistic quantification of power distribution system operational resilience," *IEEE Syst. J.*, vol. 14, no. 3, pp. 3506–3517, Sep. 2020, doi: 10.1109/jsyst.2019.2940939.
- [88] M. H. Amirioun, F. Aminifar, and H. Lesani, "Resilience-oriented proactive management of microgrids against windstorms," *IEEE Trans. Power Syst.*, vol. 33, no. 4, pp. 4275–4284, Jul. 2018, doi: 10.1109/tpwrs.2017.2765600.
- [89] J. Salomon, M. Broggi, S. Kruse, S. Weber, and M. Beer, "Resilience decision-making for complex systems," ASCE-ASME J. Risk Uncertainity Eng. Sys. Part B. Mech. Eng., vol. 6, no. 2, Mar. 2020, Art. no. 20901, doi: 10.1115/1.4044907.
- [90] H. Yin, C. Zhao, and C. Ma, "Decentralized real-time energy management for a reconfigurable multiple-source energy system," *IEEE Trans. Ind. Informat.*, vol. 14, no. 9, pp. 4128–4137, Sep. 2018, doi: 10.1109/tii.2018.2827466.
- [91] S. D. Ramchurn, P. Vytelingum, A. Rogers, and N. R. Jennings, "Putting the smarts into the smart grid," *Commun. ACM*, vol. 55, no. 4, pp. 86–97, Apr. 2012, doi: 10.1145/2133806.2133825.
- [92] M. Eriksson, M. Armendariz, O. O. Vasilenko, A. Saleem, and L. Nordstrom, "Multiagent-based distribution automation solution for self-healing grids," *IEEE Trans. Ind. Electron.*, vol. 62, no. 4, pp. 2620–2628, Apr. 2015, doi: 10.1109/tie.2014.2387098.
- [93] US DoE, "Grid 2030: A national vision for electricity's second 100 years," US Department-Of-Energy, Tech. Rep., 2003. [Online]. Available: https://www.energy.gov/sites/default/files/oeprod/ DocumentsandMedia/Electric\_Vision\_Document.pdf
- [94] V. Tsiatsis, S. Karnouskos, J. Höller, D. Boyle, and C. Mulligan, Internet of Things: Technologies and Applications for a New Age of Intelligence. London U.K.: Elsevier Academic Press, Nov. 2018.
- [95] O. Kaynak, W. He, F. Flammini, and Z. Liu, "Towards symbiotic autonomous systems," *Philos. Trans. Roy. Soc. A: Mathematical, Phys. Eng. Sci.*, vol. 379, no. 2207, Aug. 2021, Art. no. 20200359, doi: 10.1098/rsta.2020.0359.
- [96] S. Karnouskos, "Symbiosis with artificial intelligence via the prism of law, robots, and society," *Artif. Intell. Law*, vol. 30, pp. 93–115, May 2021, doi: 10.1007/s10506-021-09289-1.

- [97] S. Karnouskos and P. Leitao, "Key contributing factors to the acceptance of agents in industrial environments," *IEEE Trans. Ind. Informat.*, vol. 13, no. 2, pp. 696–703, Apr. 2017, doi: 10.1109/tii.2016.2607148.
- [98] S. Cave, R. Nyrup, K. Vold, and A. Weller, "Motivations and risks of machine ethics," *Proc. IEEE*, vol. 107, no. 3, pp. 562–574, Mar. 2019, doi: 10.1109/jproc.2018.2865996.
- [99] IEEE, "Ethically aligned design: A vision for prioritizing human wellbeing with autonomous and intelligent systems," The IEEE Global Initiative on Ethics of Autonomous and Intelligent Systems, Res. Report, 2018. [Online]. Available: https://standards.ieee.org/content/ dam/ieee-standards/standards/web/documents/other/ead1e.pdf
- [100] Y. Lu, X. Xu, and L. Wang, "Smart manufacturing process and system automation - A critical review of the standards and envisioned scenarios," *J. Manuf. Syst.*, vol. 56, pp. 312–325, Jul. 2020, doi: 10.1016/j.jmsy.2020.06.010.
- [101] Z. Liu *et al.*, "Protection testing for multiterminal high-voltage dc grid: Procedures and procedures and assessment," *IEEE Ind. Electron. Mag.*, vol. 14, no. 3, pp. 46–64, Sep. 2020, doi: 10.1109/mie.2020.2977150.
- [102] A. Shourangiz-Haghighi *et al.*, "Developing more efficient wind turbines: A survey of control challenges and opportunities," *IEEE Ind. Electron. Mag.*, vol. 14, no. 4, pp. 53–64, Dec. 2020, doi: 10.1109/mie.2020.2990353.
- [103] Y. Liu, L. Shu, Z. Huo, K. F. Tsang, and G. P. Hancke, "Collaborative industrial Internet of Things for noise mapping: Prospects and research opportunities," *IEEE Ind. Electron. Mag.*, vol. 15, no. 2, pp. 52–64, Jun. 2021, doi: 10.1109/mie.2020.3040162.



JINHUA SHE (Fellow, IEEE) received the B.S. degree in engineering from Central South University, Changsha, China, in 1983, and the M.S. and Ph.D. degrees in engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 1990 and 1993, respectively. In 1993, he joined the School of Engineering, Tokyo University of Technology, Hachioji, Japan, where he is currently a Professor. His research interests include the application of control theory, repetitive control, process control, mobile education, and assistive robotics. Dr. She

is a member of the Society of Instrument and Control Engineers, Institute of Electrical Engineers of Japan, Japan Society of Mechanical Engineers, Chinese Association of Automation, and Asian Control Association. He is the Delegate of IES TC Cluster four (Cross-disciplinary, during 2020–2021) and the Chair of IES TC on Human Factors (during 2018–2021). He was the recipient of the IFAC (International Federation of Automatic Control) Control Engineering Practice Prize Paper Award in 1999 (jointly with M. Wu and M. Nakano).



HIPÓLITO GUZMÁN-MIRANDA (Senior Member, IEEE) received the degree in telecommunications engineering in 2006, with a specialization in electronics, and the Ph.D. degree (with Hons. and European mention) from the Department of Electronics Engineering, Universidad de Sevilla, Seville, Spain, in 2010. In 2006, he joined the Electronics Engineering Department, Universidad de Sevilla. He is currently a Professor with Universidad de Sevilla, where he mainly teaches subjects related to microelectronics, programmable logic

design, and verification, and project management applied to electronics. He has authored or coauthroed more than 15 JCR journal papers and more than 40 conference contributions. His research interests include design and verification of programmable logic applications, high-throughput visual classification systems, and emulation and mitigation of radiation effects in digital devices. He has been the Chair of the IEEE IES Technical Committee on Electronic Systems on Chip (during 2020–2021), and is currently a Cluster Delegate for IEEE IES Cluster 4 (Cross-Disciplinary), for the term 2021–2022.





VICTOR HUANG (Life Fellow, IEEE) received the Ph.D. degree in electrical engineering. He is currently a partner in Sage Technology Resources, a technology and business consulting services firm, where he specializes in the IT-Automotive sector – Electric Vehicles and infrastructure industry (EV), and in connected and autonomous vehicles. He holds four international patents. and a Life Administrative Committee (AdCom) member of the IEEE IES, the Vice-Chair of IES Technical Committee on Standards, IES representative to the IEEE

Standards Board. He was the recipient of the IEEE Standards Association (IEEE-SA) Standards Medallion for exceptional contributions to standards development.



ALLEN C. CHEN (Life Senior Member, IEEE) received the M.S. degree in electrical and computer engineering from the University of North Dakota, Grand Forks, ND, USA., and the Ph.D. degree in electrical and computer engineering from the University of Wisconsin, Madison, WI, USA. He is currently a Professional Engineer. He has more than 30 years of technical and managerial experience in computer, VLSI, and wireless communication industries. He is an IEEE Industrial Electronics Society Life AdCom Member and the

Chair of the IES Technical Committee on Standards. Allen has served for IES in various capacities including General Chair, Program Chair, Track Chair, and Session Chair of many IES conferences and was an IES Officer. He was the recipient of the IEEE Third Millennium Medal Award and IES Anthony Hornfeck Award.



**STAMATIS KARNOUSKOS** (Fellow, IEEE) is currently with SAP in Germany, dealing with technology foresight, especially in the scope of industrial technologies and enterprise systems. He has extensive experience in industrial research and technology management. He has coauthored/edited several books relevant to the Industrial Internet of Things and cyber-physical systems.



LARISA DUNAI (Member, IEEE) received the B.S. and master's degrees in electronic engineering from the Technical University of Moldova, Chisinau, Moldova, in 2003 and 2004, respectively, and the Ph.D. degree from the Universitat Politécnica de Valéncia, Valencia, Spain, in 2010. She is currently an Associate Professor with the Universidad Politecnica de Valencia (UPV), Valencia, Spain. After receiving the M.Sc. degree, she joined the Technical University of Moldova, as an Assistant Professor with the Radio Electronics and

Telecommunications Department. In 2007, she was a Researcher with the Research Center in Graphic Technology, Universidad Politécnica de Valencia, Valencia, Spain. In November 2008, she joined the UPV, as an Assistant Professor with the Graphic Design Department.

In 2013 she was the recipient of the MIT Innovators Award for Spain and in 2014 the Michael Richey Medal from the Royal Institute of Navigation. From 2020 to 2022, she was the Chair of the Technical Committee of Education in Engineering and Industrial Technologies.



**CHENGBIN MA** (Senior Member, IEEE) received the B.S. degree from the East China University of Science and Technology, Shanghai, China, in 1997, and the M.S. and Ph.D. degrees in electrical engineering from the University of Tokyo, Tokyo, Japan, in 2001 and 2004, respectively. From 2004 to 2006, he was an R&D Researcher with FANUC Limited, Japan. Between 2006 and 2008, he was a Postdoctoral Researcher with the Department of Mechanical and Aeronautical Engineering, University of California, Davis, CA, USA. In 2008, he

joined the University of Michigan-Shanghai Jiao Tong University Joint Institute, Shanghai Jiao Tong University, Shanghai, China, where he is currently a Professor of electrical and computer engineering. His research interests include battery and energy management, wireless power transfer, dynamics and motion control, and wide applications in electronic devices, electric vehicles, microgrids, and smart grids.



ALIN TISAN (Member, IEEE) received the B.Eng. and M.Sc. degrees in physics from Babeş-Bolyai University, Cluj-Napoca, Romania, in 1997 and 1998, respectively, and the Ph.D. degree in neuromorphic systems for olfaction applications from the Technical University of Cluj Napoca, Cluj-Napoca, Romania, in 2008. He is currently a Lecturer with the Electronic Engineering Department, Royal Holloway University of London, Egham, U.K. His research interests include AI on system on chip (neuromorphic software/hardware sys-

tems), machine learning for neuronal data, data processing in olfaction, signal processing for gas sensors, IoT with applications in pervasive, unobstructive healthcare, and smart homes. He has authored or coauthored more than 50 papers and Co-Chaired several Electronic Systems-on-Chip and Embedded Systems related Technical Tracks and Special Sessions.



SHO YOKOTA (Member, IEEE) received the B.E. degree in electrical engineering, the M.E. degree, and the Ph.D. degree from Hosei University, Tokyo, Japan, in 2001, 2003, and 2006, respectively, and Docteur en Robotique from the Université de Versailles Saint-Quentin-en-Yvelines, Versailles, France, in 2009. From 2006 to 2009, he was an Assistant Professor with the School of Computer Science, Tokyo University of Technology, Hachioji, Japan. From 2009 to 2014, he was a Lecturer with the Department of Mechanical En-

gineering, Setsunan University, Osaka, Japan. He is currently an Associate Professor with the Department of Mechanical Engineering, Toyo University, Saitama, Japan. His research interests include robotics, human support systems, and human-system interaction. Dr. Yokota is a member of the Institute of Electrical Engineers of Japan, Robotics Society of Japan, and Japan Society of Mechanical Engineers.