Analysis and Design of Electrostatic Discharge Protection Devices and Circuits

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Abstract

An electrostatic discharge (ESD) is a spontaneous electrical current that flows between two objects at different electrical potentials. ESD currents can reach several amps and are typically in the order of tens of nanoseconds.

Concerning microelectronics, on-chip protection against ESD events has become a main concern on the reliability of IC as dimensions continue to shrink. ESD currents could lead to on-chip voltages that are high enough to cause MOS gate oxide breakdown. ICs can thus be damaged by human handling, contact with machinery, packaging, board assembling, etc.

The main goal of this study was to analyze the effectiveness of two-stage ESD protection circuits by means of mixed mode TCAD simulations. Two-dimensional device simulations were carried out using T-Suprem4 and Taurus-Medici software from Synopsis. Also, a TCAD input deck calibration for an NXP Semiconductors' proprietary 0.14 μm CMOS technology was realized.

In addition, two aspects on the transparency of ESD protections were studied. An excessive leakage problem found in a real product was analyzed in TCAD. Furthermore, a new approach for distributed ESD protection design for broadband applications is also discussed, resulting in improved RF performance.

Acknowledgments

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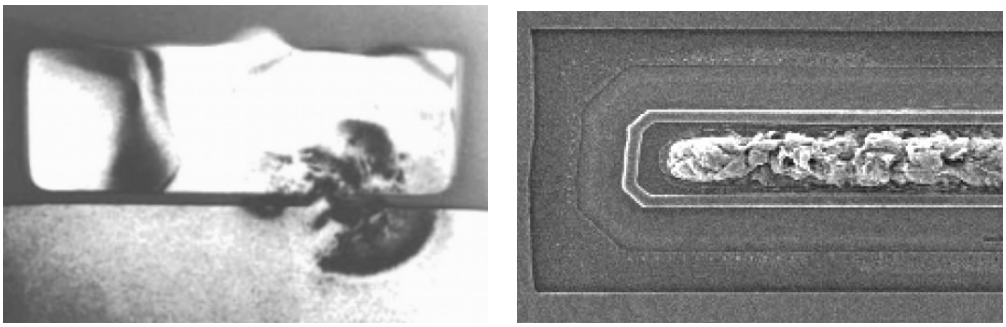
1 Introduction

1.1 ESD phenomena and IC reliability

An electrostatic discharge (ESD) is a spontaneous electrical current that flows between two objects at different electrical potentials. For example, everyday actions such as walking across the carpet or wearing a woolen jumper produce charge accumulation in the human body. As a result of this, an ESD (typically felt as a spark) occurs when having contact with another object.

Although harmless for humans, ESD is one of the main causes of IC failure. ESD currents in IC can be in the order of amperes and as fast as tens of nanoseconds. Figure 1 shows examples of IC damage due to ESD.

An object can be charged by various reasons such as triboelectric charging [ESDAD112], ionization during IC fabrication process, external electric field or contact with another charged object [Amerase86]. Therefore, there are many ways ICs can be damaged by ESD: human handling, contact with machinery, packaging, board assembling, etc. In addition, ESD is more probable in certain environments, for example when there is low air humidity during a dry winter.



(a) (b)

Figure 1. Examples of IC damage due to ESD. (a) A damaged MOST gate oxide (picture taken from [Semenov08]) (b) Damage at the drain of a donut shape ESD protection device (picture from [Smedes07] taken in an NXP Semiconductors ESD lab).

ESD phenomena are a subcategory of a more general type of events called electrical overstress (EOS). Examples of electrical overstresses are lightings and electromagnetic pulses (EMP). EOS events time scale is typically in the order of microseconds or milliseconds. ESD, with EOS, are one of the most important causes of IC failure. Figure 2 shows that around 10% of the IC failures are caused by ESD [Amerase86]. This entails an expense of millions for IC companies. In addition, on-chip protection against ESD events has become a main concern on the IC reliability since ESD failure susceptibility increases because of IC dimensions shrinking.

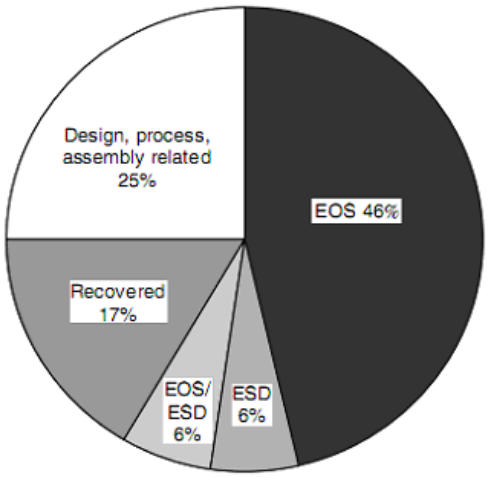


Figure 2. Estimation of failure percentage in silicon ICs [Amerase86]

The features of an ESD protection can be categorized in four different approaches:

- **Robustness**. It refers to the amount of current that an ESD protection can handle without getting damaged. Typical robustness values can be as high as several amperes.

- **Effectiveness**. ESD currents could lead to on-chip voltages that are high enough to cause MOS gate oxide breakdown. Effectiveness is the capability of an ESD protection to clamp the voltage low enough to protect the internal circuitry. Figure 3 illustrate a simplified scenario of ESD protection from the point of view of the effectiveness.

- **Speed**. Even if an on-chip ESD protection is robust and effective, the voltage at the bondpad may be temporarily too high for circuits connected to it. The concept of speed here refers to the capability of the protection circuit to be fast enough so that the pad voltage will not damage external circuitry.

- **Transparency**. ESD protections might affect to the normal performance of functionality of system. For example, aspects such as leakage current and load capacitance should have a low impact to the system performance. This is of added importance in RF or high speed applications.

Electrical engineering associations develop standards that provide manufacturers with models to reproduce ESD events like in real life. Stress test procedures such as ESD excitation circuits, discharge current waveforms, etc. are thus defined and used by industry as qualification methods to define ESD stress tolerance levels.

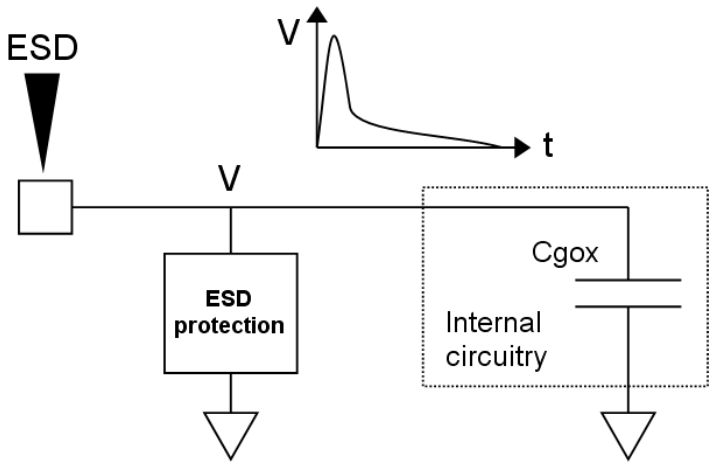


Figure 3. Simplified schematic of an ESD protection circuit from the point of view of the effectiveness.

It is also important to point out that there has always been a lack of understanding in terms of reproducing the behavior of the devices used in ESD due to the complexity of the physics involved. Typically, a trial-and-error approach has been followed in ESD protection development. This methodology requires time and an expense in fabrication and testing. This issue is becoming more important as life cycles of new technologies are shorter. Using semiconductor device simulators such as Technology Computer Aided Design (TCAD) [TCAD] software can help to accelerate this process.

1.2 ESD test methods

1.2.1 Introduction

ESD test methods are intended to measure the ESD protection performance of an IC. The reproducibility of the results and the correlation between tests is crucial. ESD test methods can be classified into two types: qualification tests and characterization tests.

1.2.2 ESD qualification tests

Different environments produce ESD events with different features. ESD qualification tests are intended to mimic the different ESD events typically found in all the hostile scenarios. They inform about failure thresholds (usually in kilovolts) for certain ESD model. The most common models used for ESD qualification are now discussed.

1.2.2.1 Human Body Model (HBM)

The Human Body Model (HBM) is the most widespread ESD qualification test. It was originally defined by a US military standard [HBM]. It reproduces the ESD event when the finger of a charged human being approaches a pin of an IC. When the air breaks down between the IC and the finger, the capacitance of the person starts to discharge and the current flows through the IC to ground. Figure 4 shows the current waveform as it is described in the standard for a discharge into a short circuit.

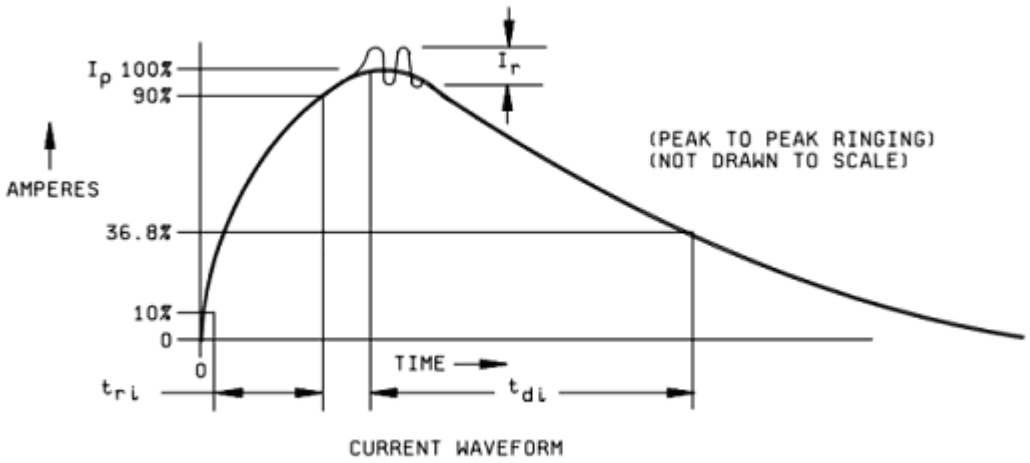


Figure 4. Human Body Model current waveform (taken from [HBM])

Parameter	Symbol	Value	Units
Rise time	tri	2-10	ns
Delay time	tdi	150 ± 20	ns
Peak current	Ip	$V_{HBM} / 1.5k\Omega$	A
Ringing	Ir	$\pm$ 10% of the Ip value	A

Table 1. List of parameters and its values of the HBM current waveform [HBM] The rise time is defined from 10% to 90% of the maximum amplitude. The delay time gives the duration of the exponential decay (1/e) after the peak.

According to the HBM standard, the equivalent lumped element circuit showed in Figure 5 is intended to reproduce the HBM current waveform. The circuit mainly consists of a capacitor C1 of 100pF (which represents the capacitance of the human body where the charge is stored) and a resistor R2 that limits the current and determines the rise time. Although not explicitly present in the circuit, it is deduced that some inductance has to be included in order to produce the current in Figure 4.

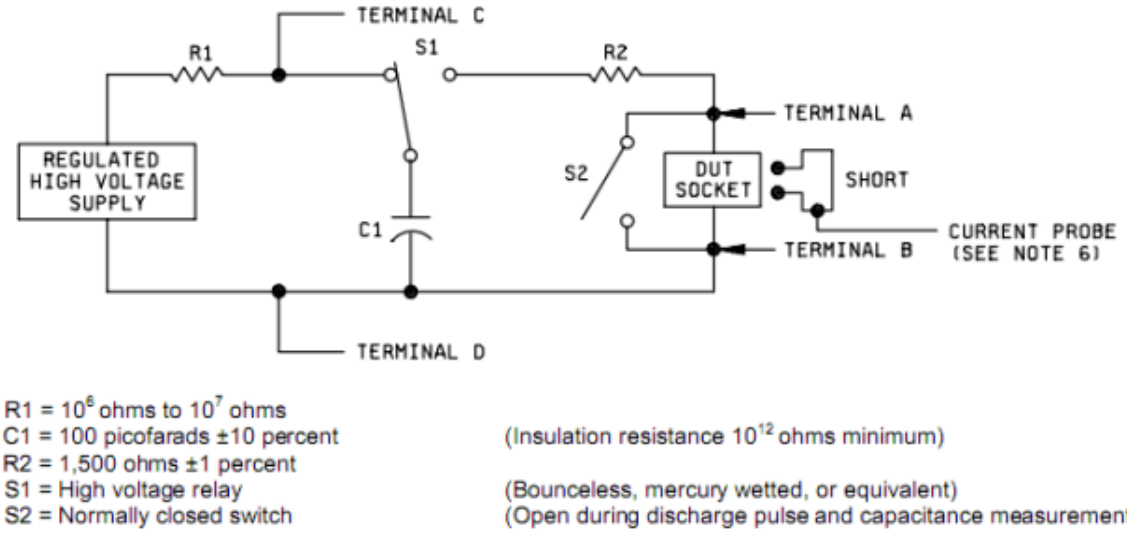


Figure 5. Human Body Model equivalent circuit (taken from [HBM])

1.2.2.2 Charged Device Model (CDM)

The Charged Device Model was originally created at AT&T in 1974 for simulating ESD produced by machinery in automated handling environments. Minor gate oxide leakage in transistors was found which could not be explained or produced by HBM testing only.

Figure 6 shows the setup for CDM testing described in [CDM09]. The IC is first charged by either direct contact or an inducing field. As Figure 6 illustrates, the IC is placed in “dead bug” position. Then the robotic arm (usually named pogo) probe is used to discharge each pin through to ground. The amount of charge stored depends on characteristics of the IC package (size, material, thickness, geometry, etc.). Hence, the failure thresholds depend strongly on the package.

Figure 7 depicts the CDM current waveform and Table 2 its parameters according to the CDM standard [CDM09]. The CDM is an oscillating current of much shorter duration and with less energy than HBM although the peak currents can be much higher. This yields in more relaxed requirements for the protection

circuits in terms of robustness and, as it will be shown in following chapters, harder requirements in terms of effectiveness.

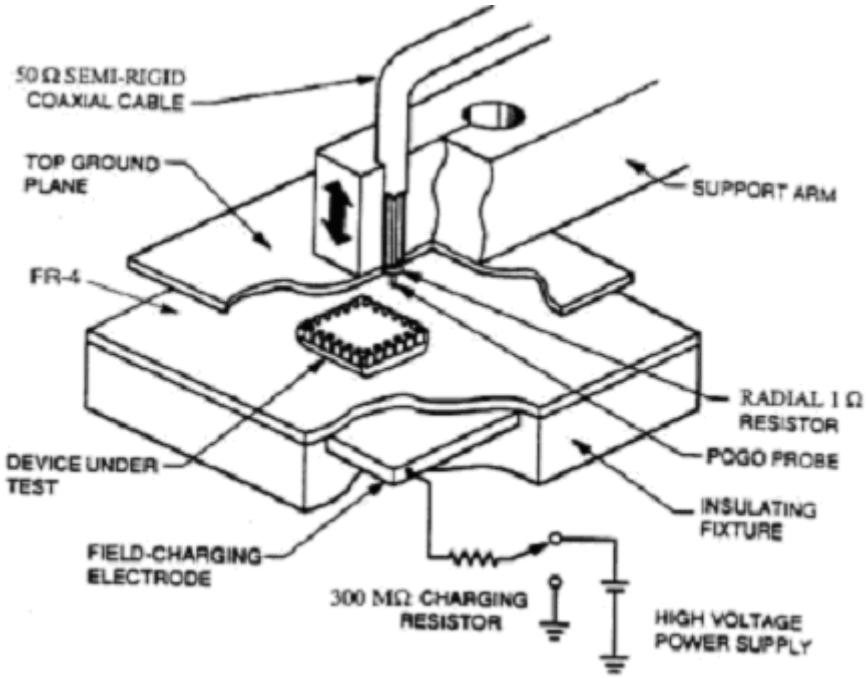


Figure 6. Field induced CDM simulator [CDM09]

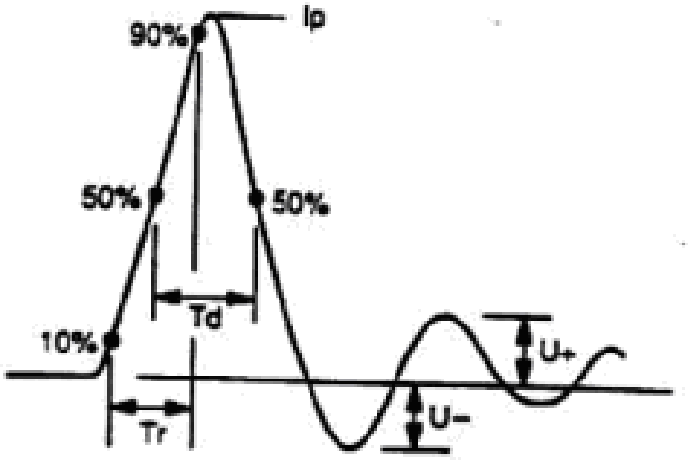


Figure 7. Charged Device Model current waveform [CDM09]

		Test Number			
		#1	#2	#3	#4
Standard test module		**Small**	**Small**	**Large**	**Large**
Test voltage (V)		500 (± 5%)	1000 (± 5%)	200 (± 5%)	500 (± 5%)
Peak current magnitude (A)	Ip	5.75 (± 15%)	11.5 (± 15%)	4.5 (± 15%)	11.5 (± 15%)
Rise time (ps)	tr	<400	<400	-	-
Full width at half height (ns)	Td	1.0 ± 0.5	1.0 ± 0.5	-	-
Undershoot (A, max.)	U-	<50% Ip	<50% Ip	<50% Ip	<50% Ip
Overshoot	U+	<25% Ip	<25% Ip	<25% Ip	<25% Ip

Table 2. Charged Device Model current waveform parameters [CDM09]

1.2.2.3 System level model

In daily life we use mobile phones, laptops, TV screens, etc. which are made of multiple ICs and have all kind of connectors (such as USB ports, antennas, etc.) that are frequently exposed to human manipulation and other systems. As the name suggests, system level model is intended to address the ESD problem in a whole system in which there are various IC, buses and connections to the outside world (Figure 8). This is a different situation from HBM and CDM, which are component level models. The most commonly used system level test is described in IEC 61000-4-2 [IEC].

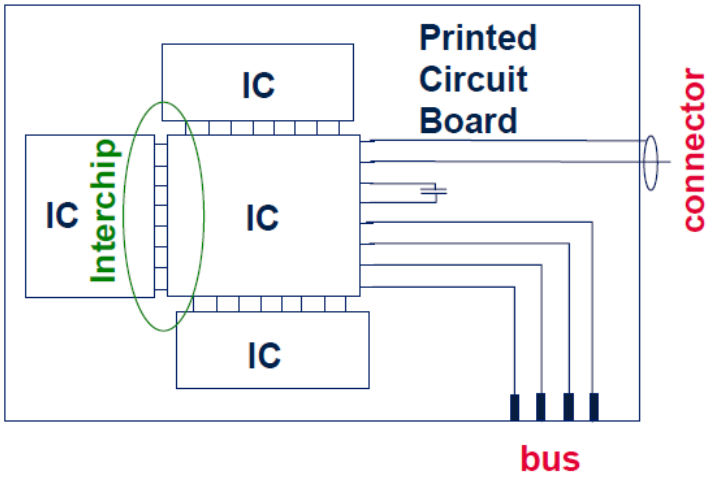


Figure 8. Example of whole system. There are two types of connection: IC-IC and IC-outside world/system.

In this study, a worse-case system level ESD is considered only, which is when the IEC 61000-4-2 current waveform (Figure 9) is applied directly to two pins of the IC, reproducing the contact discharge when a person with a metal tipped tool such as a screw driver touches a port on the system. This case is known as the Zwickau test or Human Metal Model [ESDSP56][HMM]. This test is therefore relevant for all pins of the IC that will be connected directly with the outside world in the system. The normal system level standard (IEC 61000-4-2) does not refer to this situation explicitly.

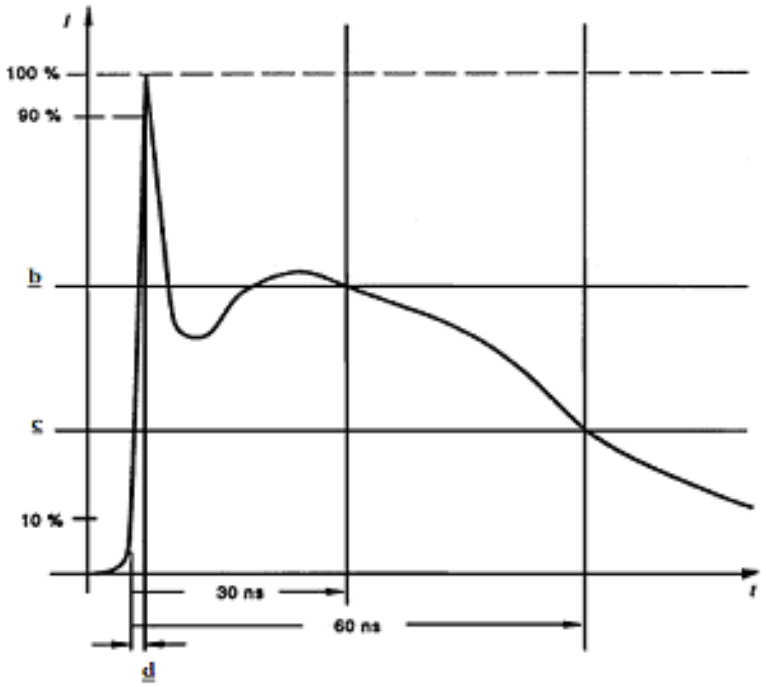


Figure 9. System level current waveform (figure taken from IEC 61000-4-2 standard [IEC]).

Level	Indicated voltage kV	First peak current of discharge ±10% A	Rise time t_r with discharge switch ns	Current (±30%) at 30 ns A	Current (±30%) at 60 ns A
1	2	7,5	da 0,7 a/*to* 1	4	2
2	4	15	da 0,7 a/*to* 1	8	4
3	6	22,5	da 0,7 a/*to* 1	12	6
4	8	30	da 0,7 a/*to* 1	16	8

Table 3. System level waveform parameters (table taken from IEC 61000-4-2 standard [IEC]).

Function	Device level ESD test	System level ESD Test (IEC)
Stressed pin group	All pin combinations	Few special pins
Supply	Unpowered	Powered & unpowered
Test methodology	Standardized	Application specific
Test set-up	Commercial tester & sockets	Application specific
Typical qualification goal	1 ...2 kV JEDEC HBM	8 kV Contact (IEC 61000-4-2) 15kV Air (IEC 61000-4-2)
Corresponding peak current	0.65 ... 1.3 A	> 20 A
Failure signature	Destructive	Functional or destructive

Table 4. Summary of main differences between device level and system level tests according to the Industry Council on ESD Target Levels [SYSLVL].

Table 4 summarizes the differences between device level and system level tests. It is important to point out that test methodology is application specific, which means that the stress method is different depending on the product and also the requirements that the protection must fulfill (for instance, a phone call must not be interrupted or the TV must never hang up during an ESD event).

1.2.2.4 Further considerations on ESD models

The normalized waveforms, that is, for peak current of 1A, and power spectrum of the explained ESD models are plotted in Figure 10. It is noticed that ESD occupy a wide frequency band and therefore it is not possible to filter them out in frequency domain in most of the applications [Semenov08].

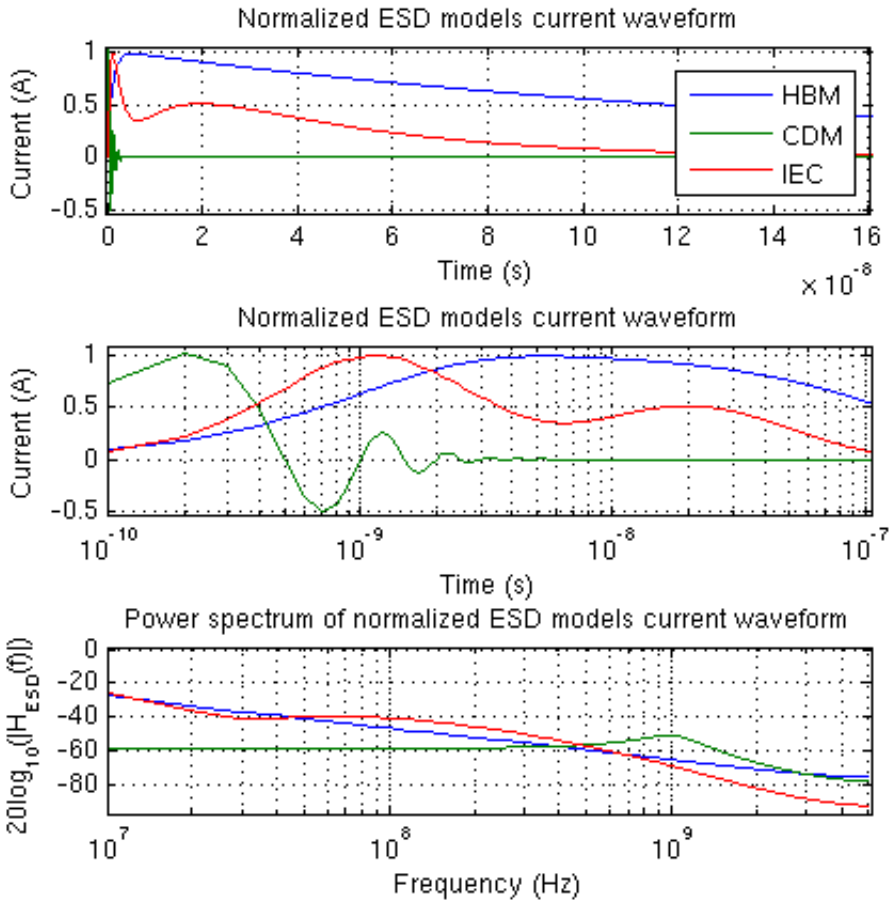


Figure 10. Comparison of the studied ESD models in time and frequency domains.

1.2.3 ESD characterization tests

Since ESD qualification test are intended to provide failure thresholds IC for reliability characterization, another type of test is needed to obtain more detailed information on the ESD protection behavior. It must be able to be well repeated and characterized. This is necessary for ESD protection study and development.

DC characterization of ESD protection devices is not the appropriate approach because of the strong self-heating. Furthermore, since ESD events are short

events of tens of nanoseconds, a proper characterization method should include the dynamic behavior of the devices against such short events.

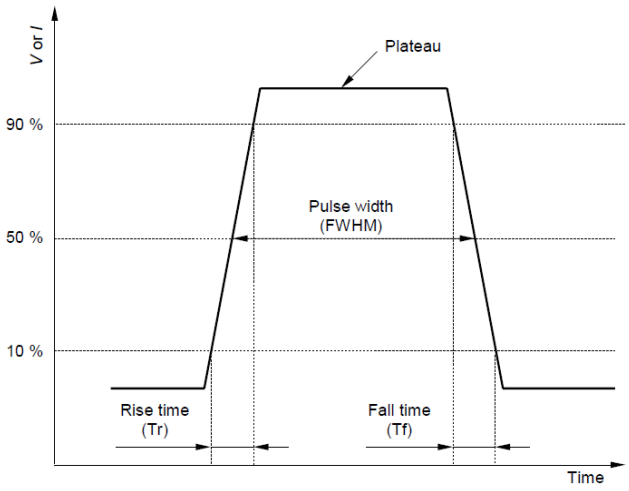
This section will focus on Transmission Line Pulsing (TLP) characterization test, which has always been used extensively.

1.2.3.1 Transmission Line Pulsing (TLP)

Basically, the TLP test consists of applying a series of short current pulses to the Device Under Test (DUT) and then measure the voltage. An IV plot is thus obtained by sweeping the maximum current value of the pulses. Figure 11 describes the procedure. Between two consecutive pulses, the leakage current of the DUT is measured. The leakage current increases when device failure has been produced. A practical example of this is shown in Figure 12.

The pulses rise time (T_r) and fall time (T_f) range from 0.2ns to 10ns and the pulse width (defined as the full width half maximum) is typically 100ns. After a current pulse is injected into the DUT, the voltage is measured and averaged from approximately 40ns until 80ns after the beginning of the pulse. TLP IV plots are often called quasi-static since they lay somewhere in between DC and dynamic transient measurements.

(a)



(b)

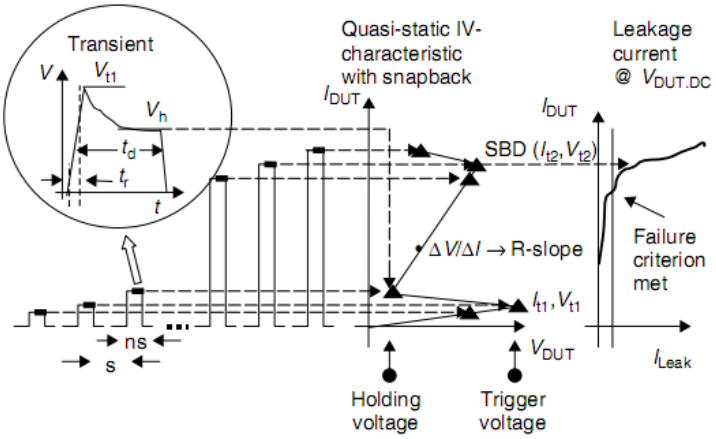


Figure 11. (a) Simple diagram of TLP pulse (taken from [ESDSP56]) (b) Description of TLP measurement (taken from [Amerase86]).

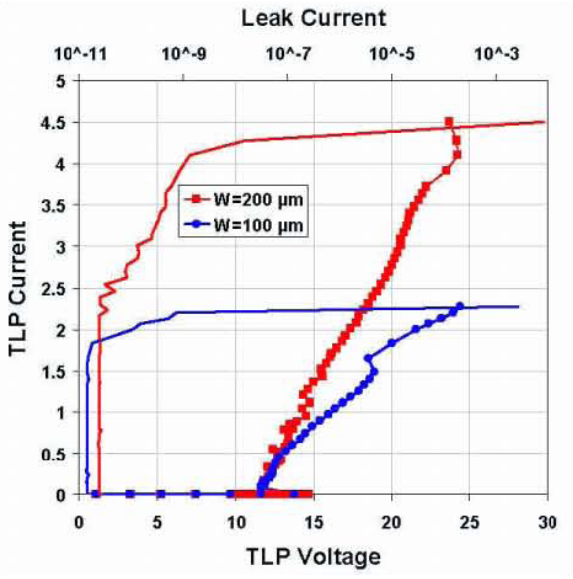


Figure 12. Example of real TLP IV plot for two snapback devices (red and blue) measured in an NXP Semiconductors ESD lab. Dotted lines are IV curves, solid lines are leakage current (figure taken from [Smedes06]).

The TLP measurements mentioned in this study were performed using laboratory equipment based on Time Domain Reflectometer (TDR) TLP [Barth].

Figure 13 depicts a diagram of a TDR TLP test. First, with switch S1 off, the transmission line TL1 is charged up to the high voltage V_{HV}. When S1 and S2 switches on, a voltage wave travels through TL2, TL3 (which is used as delay) and finally reaches the DUT. Because of the difference of impedance, a reflected wave is produced. The total wave amplitude and current is then measured between TL2 and TL3. Thus, the voltage and current that it has been transmitted to the DUT (V_{DUT} , I_{DUT}) can be calculated by Eq. 1.1 and Eq. 1.2.:

$$V_{DUT}(t) = V_3^+(t - t_{delay}) + V_3^-(t - 2t_{delay}) \quad \text{Eq. 1.1}$$

$$I_{DUT}(t) = \frac{V_3^+(t - t_{delay}) - V_3^-(t - 2t_{delay})}{Z_0} \quad \text{Eq. 1.2}$$

where V_3^+ and V_3^- are the incident and reflected waves measured between TL2 and TL3 and t_{delay} is the time that takes for the waves to pass through TL3.

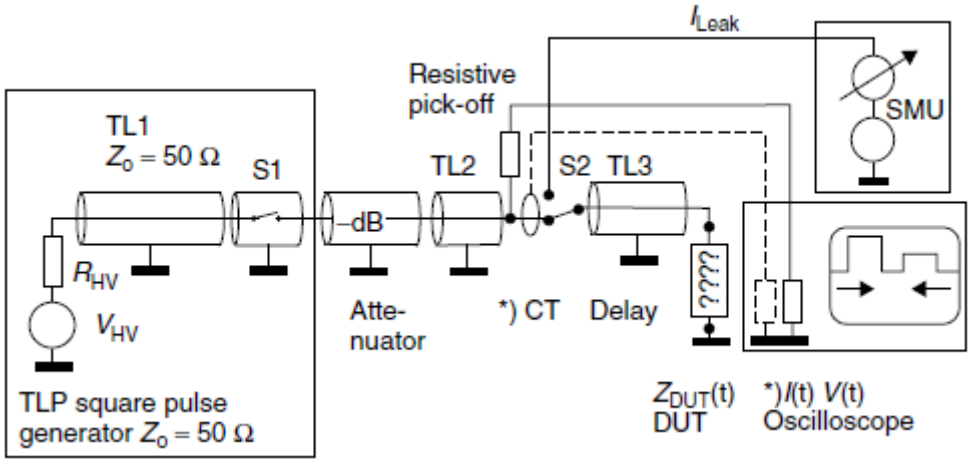


Figure 13. Time Domain Reflectometer TLP (figure taken from [Amerase86]).

1.3 ESD protection architectures

ESD can occur for any combination of two IC pins and therefore it entails to protect every pin and provide a path for the current to flow from one pin to another. There are two approaches to face this issue: pad based and rail based architectures. Figure 14 will be used to explain the features of both architectures. The blocks primary ESD, secondary ESD and power clamp are protection devices that ideally let only the ESD current flow through them so that it is steered from the input pin to the output pin. Notice that power rails (VDD and GND) are often used for carrying the ESD current from one place to another in the chip.

- Pad based

As the name suggests, the semiconductor devices involved in the primary protection are placed close to the bond pad. Usually they are snapback devices (see section 1.4). Figure 15 represents the pad based circuit that will be studied in following sections. It also describes the ESD current path: it enters the IC through the input pad, then it is directed to the VSS rail and finally it leaves the IC thought a diode.

- Rail based

The primary protection now consists of two diodes and a big clamp (see Figure 14), usually a bipolar transistor or a MOSFET. The clamp is activated by a trigger circuit that detects the ESD event. The ESD current is thus conducted by the first diode to a metal rail, passes through the clamp, then through another metal rail to the second diode and finally the output pin. Normally, VDDIO and VSSIO rails are used for carrying the ESD current. Notice that the big clamp can thus be used for protecting several pins.

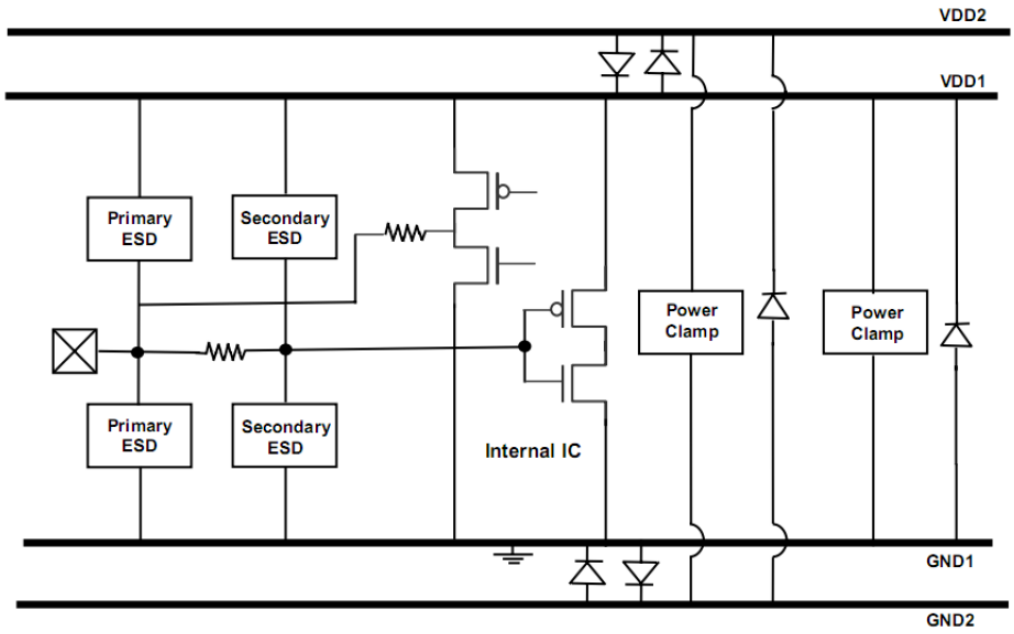


Figure 14. Simplified schematic of a generic ESD protection architecture (taken from [Amerase86])

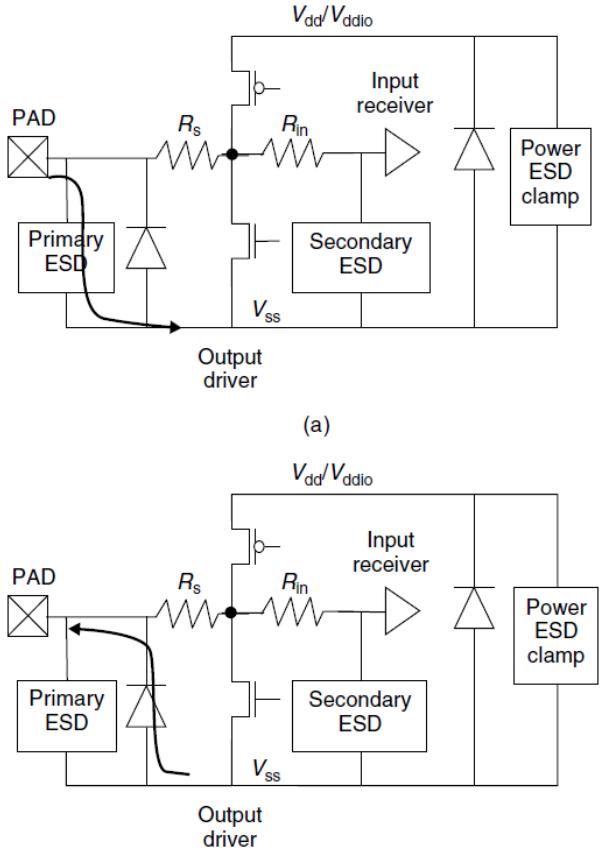


Figure 15. Example of pad based circuit (figure taken from [Amerase86]).

1.4 ESD protection devices

In ESD protection, it is common to use diodes, thyristors and MOSTs amongst other semiconductor devices. A frequently used type of protection devices, called snapback devices, should be studied separately. Figure 16 depicts a simplified curve of a generic snapback device. Table 5 describes the I-V plot parameters in Figure 16.

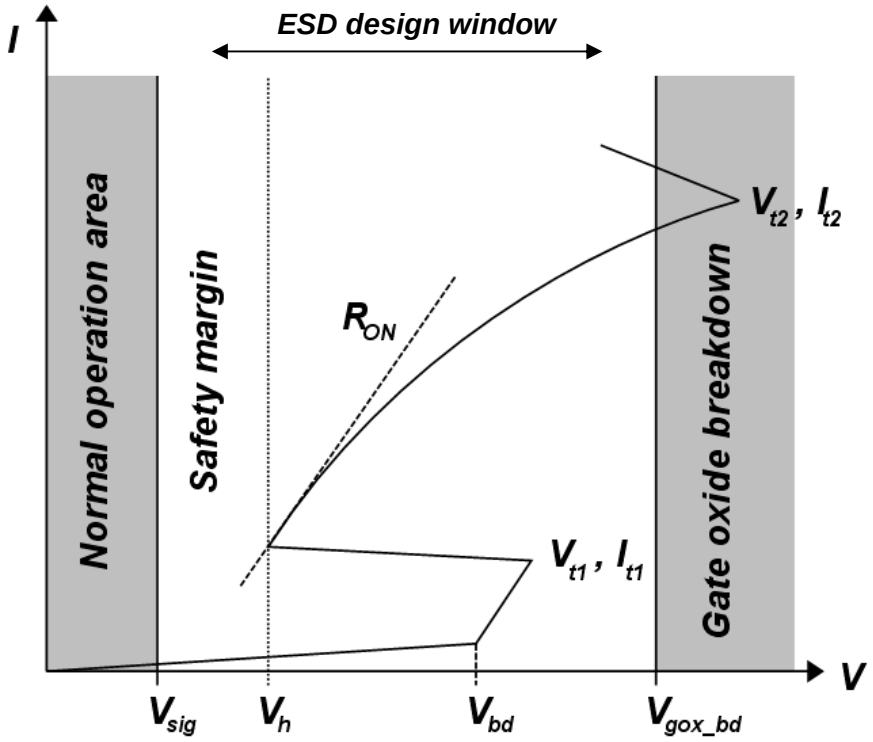


Figure 16. I-V plot for a snapback device. ESD design window and main parameters are also shown.

Table 5. Usual nomenclature for I-V plot parameters

Symbol	Meaning
V_{t1}, I_{t1}	Trigger voltage and current
V_h	Holding voltage
V_{t2}, I_{t2}	Failure voltage and current
R_{on}	Differential resistance after snapback zone.

Snapback devices have the property of decreasing the anode voltage when the trigger point (V_{t1}, I_{t1}) is reached. The device then enters into a special regime where one or various parasitic bipolar transistors, depending of the device, turn on and the voltage decreases abruptly down to a holding voltage V_h. This property is called snapback. At this point, the device behaves in an ohmic operation mode and further increase of the current yields an approximately linear increase of the voltage determined by R_{on}.

As far as the protection effectiveness is concerned, V_{t1} must be lower than the thin gate oxide breakdown voltage (V_{gox_bd} in Figure 16). For preventing latch-up issues, a safety margin is required between the maximum signal voltage level during normal operation, V_{sig}, and the holding voltage, V_h. Also notice that between (V_{t1}, I_{t1}) and (V_h, I_h) the device presents a negative differential resistance.

In next sections, we will focus on some aspects of the physical phenomena involved in snapback devices during ESD events.

1.4.1 PN junction

This chapter is intended to explain the physics in a PN junction during impact ionization avalanche. A one-dimensional abrupt p-n junction diode will be considered with the metallurgical junction between both p and n bulks.
Figure 17 depicts the energy band diagram of the device. Typical values of the doping concentration in submicron processes for the p and n materials, N_A and N_D respectively, are N_A=$10^{16}\ atoms/cm^3$ and N_D=$10^{15}\ atoms/cm^3$.

The diode is biased in reverse, that is, $V_A < 0$. As V_A becomes more negative, the electric field in the depletion region increases and so does the width of the depletion region. x_N and x_P, the depletion widths in n and p zones, are not equal since the junction depletes further where the doping concentration is lower, that is, the n zone. When the junction is starting to be reversed biased, the reverse current is defined by:

$$I_0 = \frac{qADN_C N_V}{L_d N_B}\exp\left(\frac{-E_g}{kT}\right) + \frac{qW}{\tau_e}\sqrt{N_C N_V}\exp\left(\frac{-E_g}{2kT}\right) \qquad \text{Eq. 1.3}$$

where N_C and N_V are the state density in the conduction and valence bands, respectively, W is the width of the depletion region and τ_e is the effective carrier lifetime. At this point, minority carriers are drifting down the potential hill and the only two contributions to these currents are the regular diffusion of minority carriers (left-hand side of Eq. 1.3) and the thermally generated carriers in the depletion region (right-hand side of Eq. 1.3). As V_A decreases, the E field becomes higher and so does the drift velocity of the carriers, increasing the reverse current.

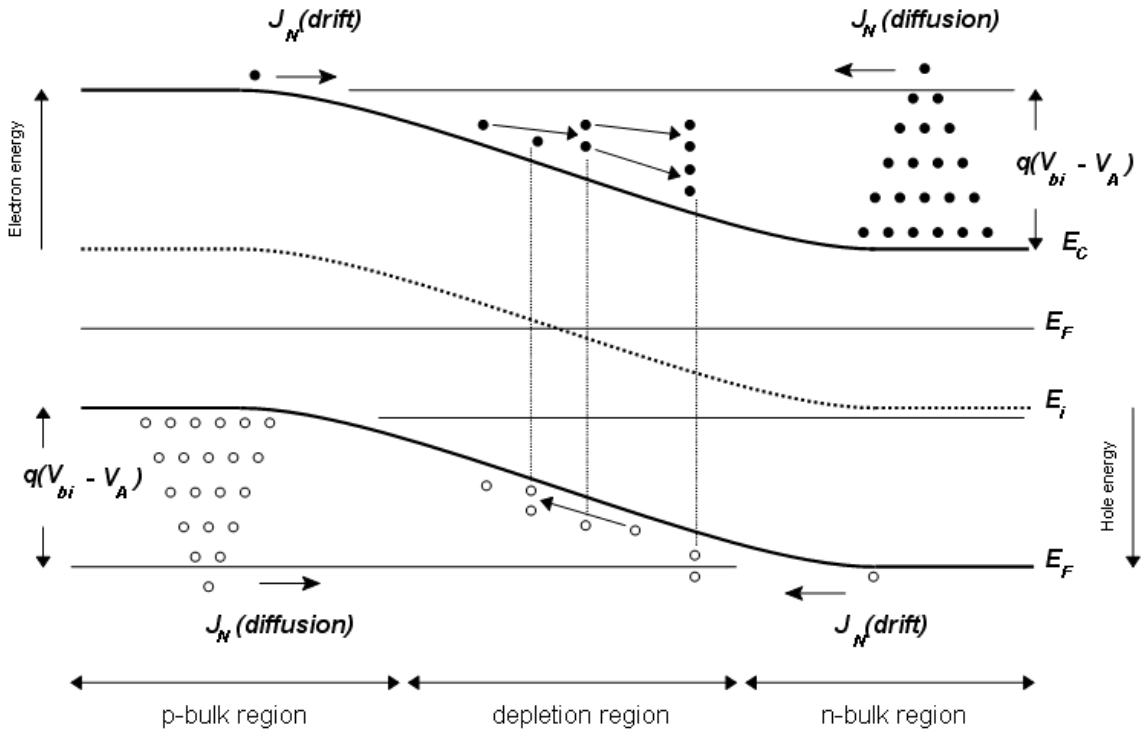


Figure 17. Energy band diagram and carrier flux at avalanche breakdown due to impact ionization

There is always certain probability that a minority carrier is accelerated to such velocity that when it collides to an atom of the crystal lattice an electron in the valence band is excited to the conduction band. This is called *impact ionization.* As a result of this collision, a single carrier (electron or hole) produces two carriers. Generated electrons will now flow towards the anode and holes towards the cathode.

If the electric field at the depletion region is relatively low, there is low probability that these new carriers are in turn accelerated enough to produce more carriers by impacting and ionizing another atom in the lattice. However, as the electric field is increased, this probability increases too. The new carriers gain energy enough to generate new electron-hole pairs by impact ionization. This phenomenon produces an avalanche effect and the total current increases dramatically. This process is called *avalanche breakdown by impact ionization.*
The electron and hole currents can thus defined as follows:

$$I_p = I_{p0} + \alpha_p I_{p0}$$
$$I_n = I_{n0} + \alpha_n I_{n0}$$

Eq. 1.4

where α_p and α_n are the impact ionization coefficients for holes and electrons, respectively. An empirically obtained equation for α_p and α_n is given in [Amerase86]. An important parameter, named multiplication factor M, is defined as by integrating the impact ionization coefficients across the width of the depletion region, x_d:

$$M_{n,p} = \frac{1}{1 - \int_0^{x_d} \alpha_{n,p} dx}$$

Eq. 1.5

It can be considered that $\alpha_n \approx \alpha_p \approx \alpha$ and therefore $M_n \approx M_p \approx M$. Hence, M represents the ratio between the total current entering the depletion region (I_{in}) and the total current leaving the depletion region (I_{out}).

$$M = \frac{I_{out}}{I_{in}} = \frac{|I|}{I_0}$$

Eq. 1.6

An equivalent expression for the multiplication factor but as a function of the applied voltage (V_A) and the avalanche breakdown voltage (V_{BR}) is usually given by [NeudeckPN][Amerase86]:

$$M = \frac{1}{1 - \left(|V_A| / V_{BR} \right)^n}$$

Eq. 1.7

where n is a fitting parameter. n ranges from 2 to 6, depending on the type of intrinsic semiconductor. Figure 18 qualitatively depicts the current and voltage at the anode as M increases. For deriving the expression of V_{BR} as a function of the doping concentrations, the maximum electric field at the depletion region must be

calculated, which happens at x=0, that is, just in the edge between the n and p materials. The equation of the electric field at the depletion region is

$$E(x)=\frac{-qN_D}{K_S\varepsilon_0}(x_n-x),\ 0\le x\le x_n \qquad \text{Eq. 1.8}$$

where the length of the depletion region at the n-material side, x_n, is formulated as:

$$x_n=\left[\frac{2K_S\varepsilon_0}{q}(V_{bi}-V_A)\frac{N_A}{N_D(N_A+N_D)}\right]^{\frac{1}{2}} \qquad \text{Eq. 1.9}$$

Taking x=0 in Eq. 1.9 and Eq. 1.8 using results in:

$$E_{CR}=E(0)=\frac{-qN_D}{K_S\varepsilon_0}(x_n-0)=-\left[\frac{2q}{K_S\varepsilon_0}(V_{bi}+V_{BR})\frac{N_AN_D}{N_A+N_D}\right]^{1/2} \qquad \text{Eq. 1.10}$$

Hence, the avalanche breakdown voltage can be approximated as:

$$V_{BR}\cong\left(\frac{E_{CR}^2K_S\varepsilon_0}{2q}\right)\left[\frac{N_A+N_D}{N_AN_D}\right] \qquad \text{Eq. 1.11}$$

E_{CR} is the critical electric field where avalanche breakdown starts to occur and it mainly depends on the semiconductor. For Si, E_{CR} varies from $2\cdot10^5V/cm$ to $8\cdot10^5V/cm$ depending on the doping [NeudeckPN]. This result implies that V_{BR} decreases for any increase in the doping concentrations.

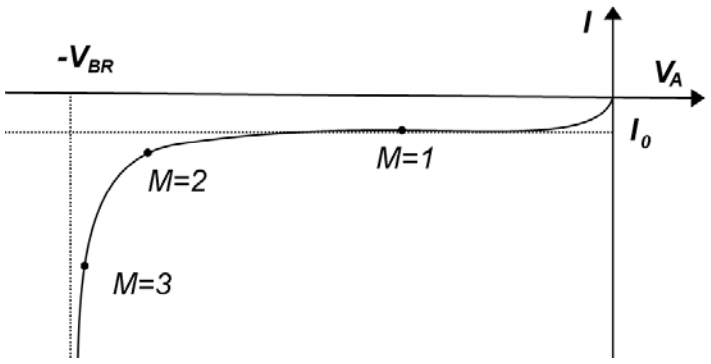


Figure 18. Approximation of avalanche breakdown approaching.

1.4.2 Grounded Gate NMOS Transistor (GGNMOST)

The Grounded Gate NMOS Transistor (GGNMOST) is one of the most widespread devices for ESD protection. When used for ESD protection purposes, gate, source and substrate are tied to ground and a positive ESD current is injected into the drain. Its snapback behavior relies on the activation of the parasitic bipolar junction transistor of the NMOST. Figure 19(b) depicts a NMOST with this parasitic bipolar transistor, where the path between the silicon area just under the channel and substrate contacts is represented by a ballast resistance. The snapback phenomenon is now described by explaining what is happening at different points in Figure 19(a):

1- Regular reverse current

Given an increasing positive current at the drain, the p-n junction is in reverse and only leakage current can flow. The potential at the drain increases, and so does the electric field at the junction. By the moment, the current due to impact ionization is negligible in comparison with the reverse current due to minority carriers drift and carriers thermal generation [Amerase86].

2- Avalanche breakdown by impact ionization

When the drain voltage is high enough, the drain pn junction gets into avalanche breakdown operation and a considerable increase of the current happens. More current starts to flow from the drain to the substrate contact. The substrate potential at the area just under the gate starts to rise locally.

3- Bipolar transistor activation

The voltage under the gate, mainly produced as a result of the avalanche current that is flowing, can raise high enough to turn on the source pn junction. At that moment, the parasitic bipolar transistor turns on and the current injected into the drain can now flow throw the NPN bipolar. The drain, source and the substrate

area where the voltage has increased locally become collector, emitter and base of the bipolar junction transistor, respectively.

4- Minimum voltage/current that sustains the bipolar

Now, the drain voltage abruptly decreases down to a holding voltage, V_H , as a consequence of the new low-resistive bipolar path.

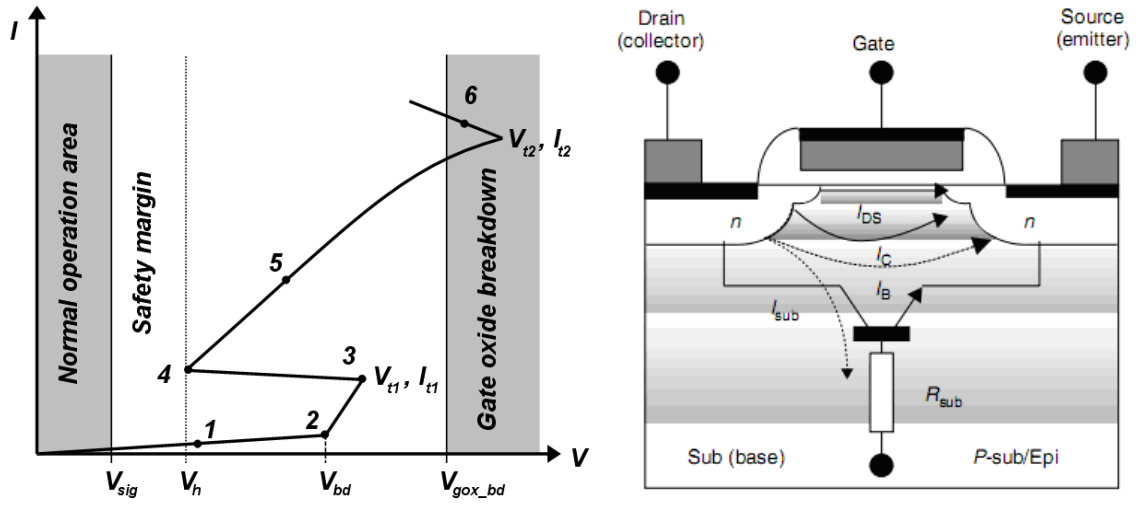
5- Linear zone

Further increase of the current yields in higher collector voltage as in a regular BJT. Now most of the current flows throw the bipolar transistor, that is, from collector to emitter, and not throw drain to substrate contact.

6- Thermal failure

The power dissipation is too high and the device starts to enter into thermal breakdown. The temperature is approaching the Si melting point.

In CMOS submicron processes, V_{t1} and V_h can range between 6-10V and 2-6V, respectively. Figure 20 shows the area of operation in which the NMOST operates as a snapback device. Table 6 shows the GGNMOST I-V curve parameters dependence on the most important process and layout parameters. Most of these relations were experienced and demonstrated qualitatively during the TCAD simulations in this study. Some of them will be explained along this study.



(a) (b)

Figure 19. (a) Cross section of an NMOST showing the different implants (b) Drain current as a function of the drain voltage and regions of operation. (Figure (b) taken from [Amerase86]).

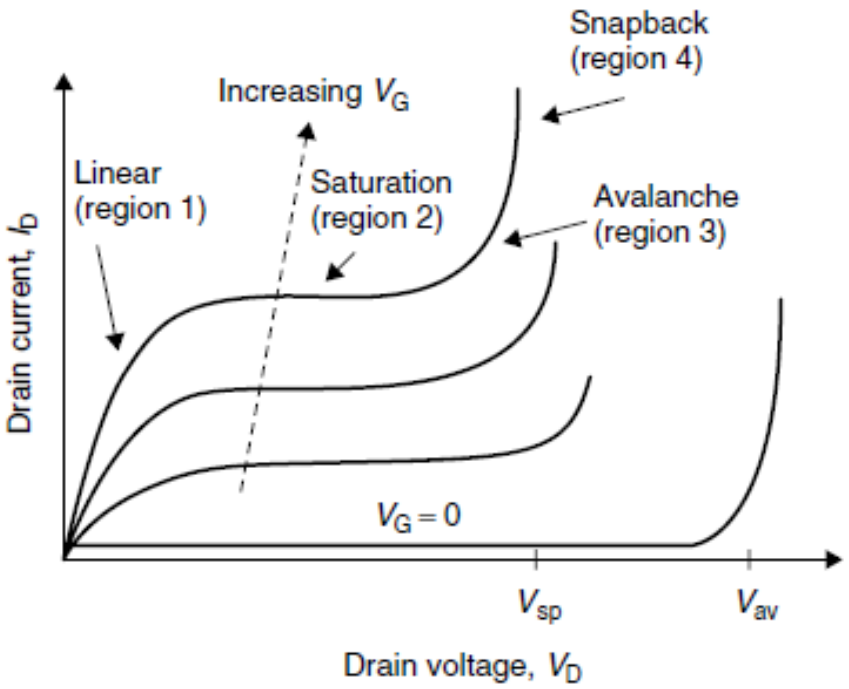


Figure 20. Drain current as a function of the drain voltage and regions of operation. (Figure taken from [Amerase86])

Table 6. GGNMOST I-V curve parameters dependence on process parameters and layout dimensions. Arrows represent direct or inverse relation. Single arrows mean weak dependence or side effect while double arrows mean strong dependence. ND means little or no dependence (taken from [Beebe98])

Parameter	V_{bd}	V_{t1}	I_{t1}	V_{sb}	R_{sb}	V_{t2}	I_{t2}
Gate length	ND	↑↑	↑	↑↑	↑	↑	↑↑
Gate width	ND	↓[a]	↑↑	ND	↓	ND	↑↑
S/D junction depth (1 / curvature)	↓↓	↓	ND	↓	↓	↑	↑↑
Contact-gate spacing	↑	↑	ND	↑↑	↑↑	↑	ND
Remove silicide	ND	↑	ND	↑↑	↑↑	↑	↑↑
Gate bias/bounce	↓↓	↓↓	↓↓	ND	ND	ND	ND
Block LDD implant	↑↑	↑	ND	↑	↑	↑	↑↑[b]
Substrate resistance	↓	↓	↓↓	ND	ND	ND	↓

a. If gate coupling is used.
b. If LDD junction is shallow compared to S/D junction.

1.4.3 Low Voltage Triggered Silicon Controlled Rectifier (LVTSCR)

In a regular Silicon Controlled Rectifier (SCR), shown Figure 21(a), V_{t1} is determined by the n-well/p-well avalanche breakdown voltage, which usually is around 20V in advanced CMOS process [Amerase86]. Since this voltage is often too high for most applications, an n+ implant is placed between the n-well edge with the p-well. By increasing the doping concentration the trigger voltage decreases in agreement with Eq. 1.11. For further V_{t1} decrease, a gate is placed between the n+ implants and connected to ground, forming a kind of GGNMOST. This configuration is called Low Voltage Triggered SCR (LVTSCR). The LVTSCR (Figure 21(b)) can thus be considered as an SCR that is helped to trigger by a GGNMOST.

For the LVTSCR snapback device, the shape of the I-V curve is very similar to the GGNMOST I-V curve and only quantitative aspects change. Also, the

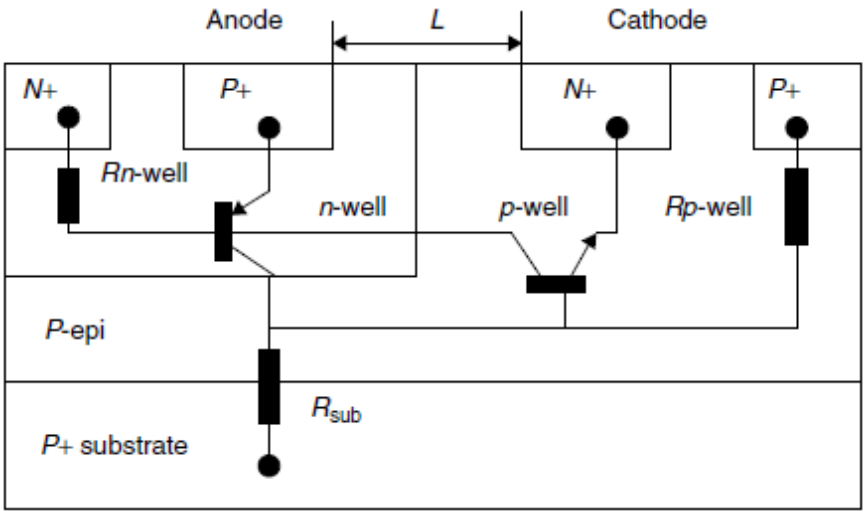
snapback process is in essence the same as in the GGNMOST. This is now described using Figure 19(a):

Point 2-3: GGNMOST triggers the latch-up structure

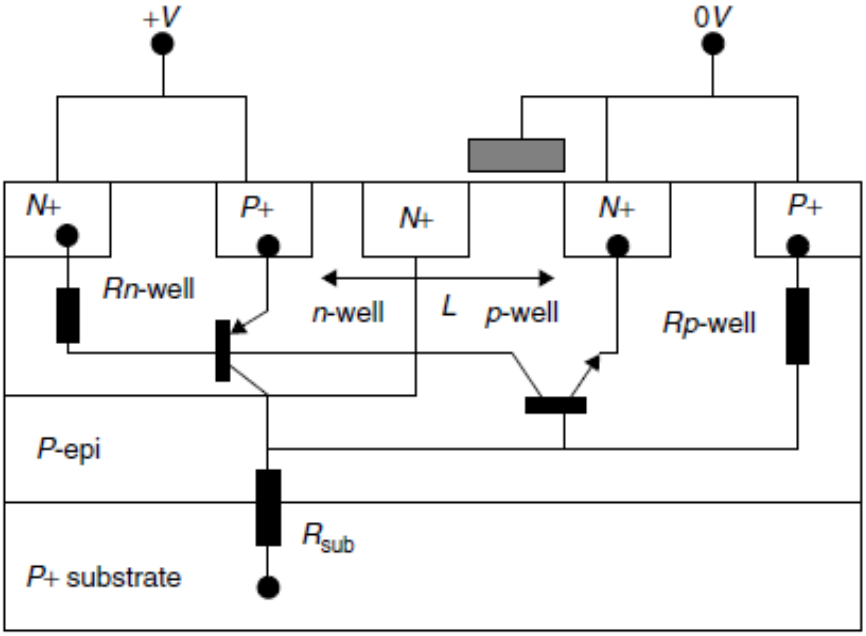
At this point the parasitic NPN bipolar transistor of the embedded GGNMOST turns on, which results in current flowing through the n-well, crossing the p-well and leaving out to the GGNMOST source.

Point 4-5: NPN and PNP latch up

The two parasitic bipolar latch-up and the anode voltage down to the holding voltage since a new low ohmic path has been produced. Current can now flow through both bipolar branches.



(a)



(b)

Figure 21. Cross sections of an SCR (a) and a LVTSCR (b) with parasitic latch-up structure (figures taken from [Amerase86]).

1. Introduction

2 ESD protection effectiveness study

2.1 TCAD input deck calibration

Despite the fact that TCAD simulations sometimes do not agree quantitatively as much as desired due to miscalibration or the use of not accurate enough models, the results can be meaningful from a qualitative point of view. Simulation experiments can be performed by, for instance, varying process and layout parameters of the devices. Simulations of snapback devices can be used to get an understanding of the physics involved in order to help to predict the performance of similar circuits in future or solve problems such as a leakage issue in following chapters.

In this study, two-dimensional numerical device simulations were carried out using T-Suprem4 [Tsuprem05] and Taurus-Medici [Medici09] software from Synopsys utilizing a $0.14\,\mu m$ CMOS technology. The most relevant features of this technology in terms on ESD protection design are described in Table 7. This technology is the result of a shrinking process of an older $0.18\,\mu m$ CMOS technology. T-Suprem4 simulates the fabrication process of integrated circuits as it is performed in the foundry. The device is represented by a mesh of points. Diffusion, implantation, deposition and other physical phenomena are

implemented by means of models. In modern CMOS process, all the MOST implants in Figure 22 (pocket or halo implant, Vt implant, ATP (Anti Punch Through) implant and Lightly Doped Drain (LDD)) play a role. Also the substrate resistance as a strong impact in the ESD protection performance [Smedes02]. The thickness of the epitaxial layer, the Shallow Trench Isolation (STI) properties, and the polysilicon doping are also implemented.

Silicidation requires especial consideration. In this study, non-silicided devices were always used. The reasoning behind this is for the improvement of the uniform finger activation of the ESD protection. For example, in multi-fingered snapback devices different fingers may have slightly different trigger voltages. By blocking the silicidation, the device R_{on} resistance is increased. It is thus assured that all the fingers will turn on before the thermal breakdown is reached. Figure 23 depicts an approximation of the multi-finger activation process. Typically, ESD performance is optimal for the minimum gate length due to the better activation of the parasitic bipolar transistors.

After model creation, the doping profiles in drain/source implants and channel were extracted from the model and compared successfully with Secondary Ion Mass Spectrometry (SIMS) measurements. Also voltage threshold of NMOS was extracted and compared with technology report data. Finally, the ESD protection performance of the devices was simulated and compared with real measurements (see section 2.1.2).

It is important to point out that in this study the design parameters (layout dimensions, doping profiles, substrate resistivity, etc.) were taken as close to the real values as possible when designing a model of an ESD protection device. Therefore, the results are presented *as it is,* without any further tuning for better fitting to the real measurements.

Starting material	Lightly doped p-wafer, 3.5 μm deep epitaxial layer
Wells	Retrograded n-well and p-well
Device isolation	Shallow Trench Isolation (STI)
Gate oxide (GO) thickness / operating voltage	GO1: 3nm / 1.8V GO2: 7nm / 3.3V
Silicidation	Titanium silicide. Silicide blocking layer available.
Lightly Doped Drain (LDD)	LDD blocking layer available.
Substrate resistivity	High ohmic (10 Ω cm)
Estimated gate oxide V_{BD} in ESD time scale (several nanoseconds)	GO1: $\approx$ 9V GO2: $\approx$ 14V
Diffusion sheet resistance (silicide blocked)	85 Ω / □
Contact resistance	25 Ω

Table 7. Summary of the most relevant process parameters for ESD protection design purposes in this study [C14DRM].
Some data is skipped due to confidentiality.

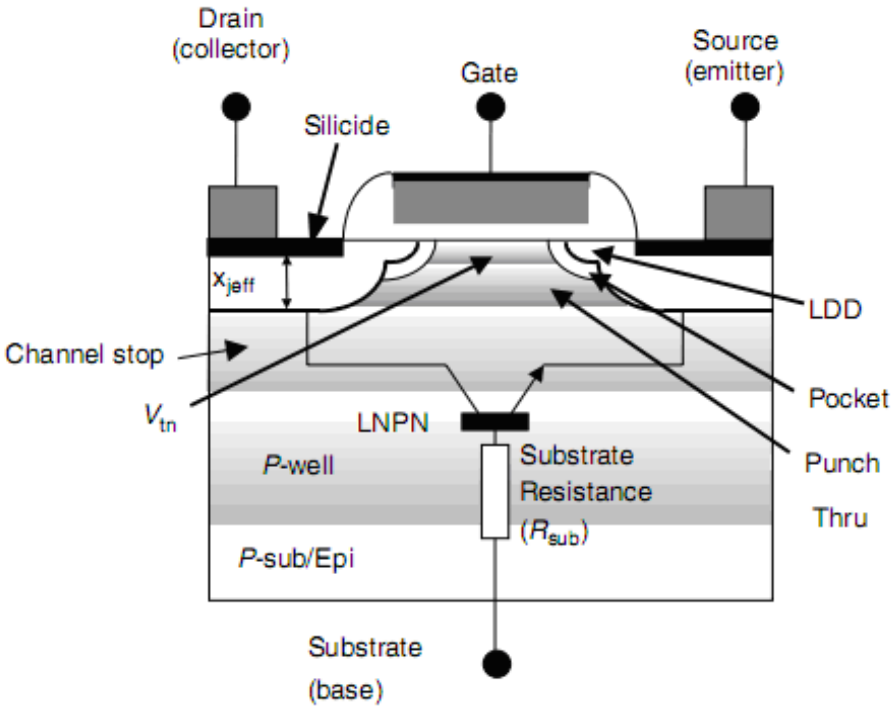


Figure 22. Cross section of an NMOST showing the different implants.

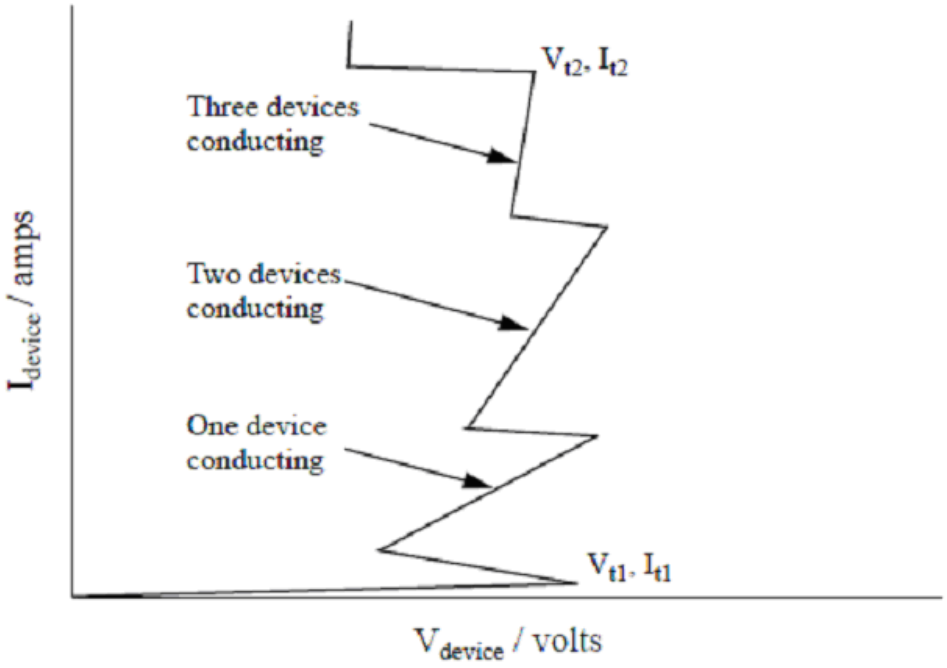


Figure 23. Approximation of the real snapback process of a multi-finger snapback device (taken from [Beebe98])

2.1.1 Double snapback due to Kirk effect

A TCAD input deck was given at the beginning of the internship. However, a double snapback behavior was observed in TLP simulations of a GGNMOST (see Figure 24). This does not agree with the observed device behavior. Further investigations showed that this input deck was partially wrong. Therefore, it was decided to start a new input deck for our 0.14 μm CMOS technology taking a calibrated input deck from a similar technology as a starting point, specifically a 0.18 μm CMOS technology. The phenomenon, however, was investigated for educational purposes.

The state of physical parameters of the device were captured at the most relevant points, which are I={1e-04, 5e-04, 2e-03, 1e-02} A (see Figure 24, blue dotted curve). The simulation was done for a 1 μm wide device, so all the currents in this chapter can be considered current densities in $A/\mu m$. Note that, in 2D simulations, the simulator interprets the width of the device as if all the

physical parameters where uniformly applied along the width. For instance, the current through a 10 μm wide device will be the 10 times higher than for the 1 μm wide device. Figure 26 depicts the impact ionization density in $cm^{-3}s^{-1}$ and total current density in Acm^{-2}. It can be observed how the area of maximum impact ionization spreads as the injected current increases. The maximum is located mainly in the diffusion area closer to the substrate contact, that is, just underneath the gate spacer. It is important to point out that at I=1E-02A (see Figure 26 (4)) a new maximum impact ionization density, one order of magnitude higher than in the cases with less current (Figure 26 (1,2,3)), appears just under the drain contact. In agreement with this, the total current density also changes its maximum position to where the new impact ionization density maximum takes place.

This behavior is due to the Kirk effect. The charge density at the collector area exceeds the charge density at the depletion region and, therefore, the depletion region at that area disappears (see Figure 26 (4)). At this point, there is a generation of majority carriers from the base in the base-collector depletion region. When there is full ionization, the Kirk effect takes place when the following condition happens:

$$J_C \geq qN_C v_{sat} \qquad \text{Eq. 2.1}$$

where J_C is the current density at the collector, q is the unitary charge, N_C is the doping concentration at the collector, v_{sat} is the saturation velocity in silicon. The displacement of the charge creates a new current path. Thus, for the GGNMOST to carry more current, a new bipolar transistor path turns on.

Figure 25 is intended to compare the shape of current density distribution. A vertical cut of the cross section was done from the gate down to 3 μm in the substrate. A comparison of the shape between Figure 25(1,2) and Figure 25 (3) supports that a deeper current path has been created. Notice the two relative

maximums in Figure 25 (3). The first peak, at 150nm depth has similar amplitude for both total currents I=2E-03A and I=1E-02A. A new deeper peak, nevertheless, is shown that carries most of the current.

Figure 27 shows the potential and total current in the substrate. The potential scale ranges from 0V to only 2V in order to focus on the area that corresponds to the base of the bipolar transistor. It is observed in Figure 27(1) that most of the current injected into the drain leaves to the substrate contact. At Figure 27(2), the shallow bipolar is starting to turn on and therefore the current now tends to leave through the source (emitter). On the other hand, Figure 27(3,4) show that the bipolar is fully on and almost all the current leaves to through the emitter. Furthermore, the largest arrows in Figure 27(4) indicate that most of the current now flows deeper into the substrate. Also, small arrows at higher depth are visible. It is also significant that the potential in the substrate across the current path is now much higher since it ranges from 2V to 0V.

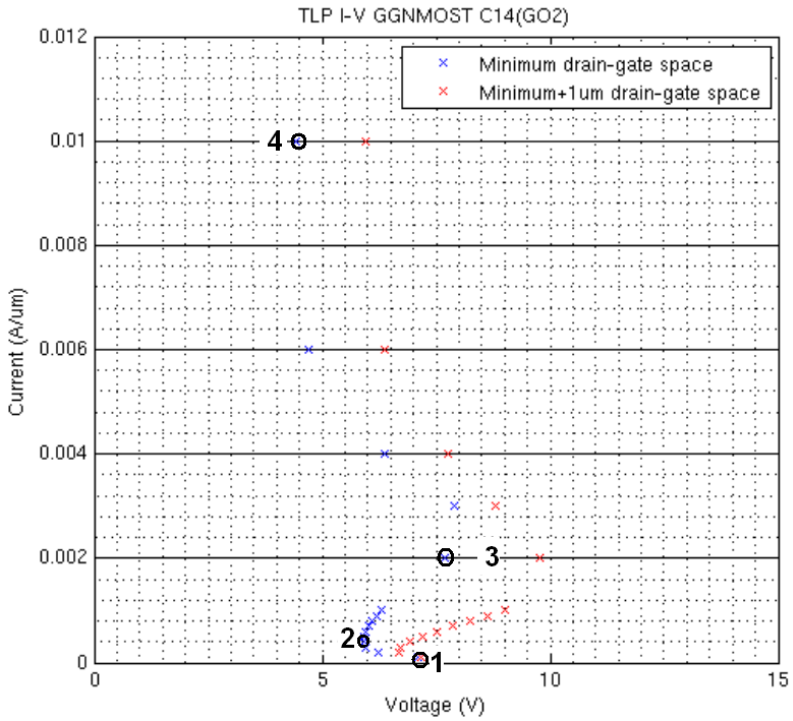
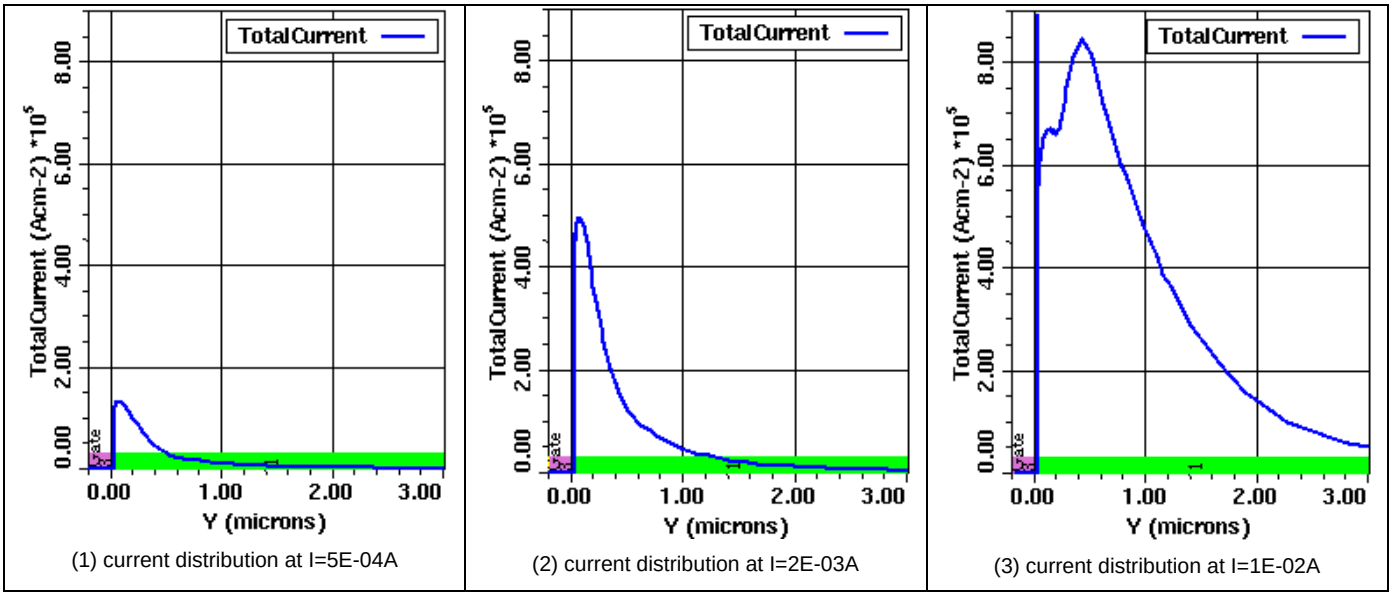


Figure 24. TLP simulation of two GGNMOST with different drain to gate distances using the wrong input deck. The device was studied at I={1e-04, 5e-04, 2e-03, 1e-02} A (blue line).

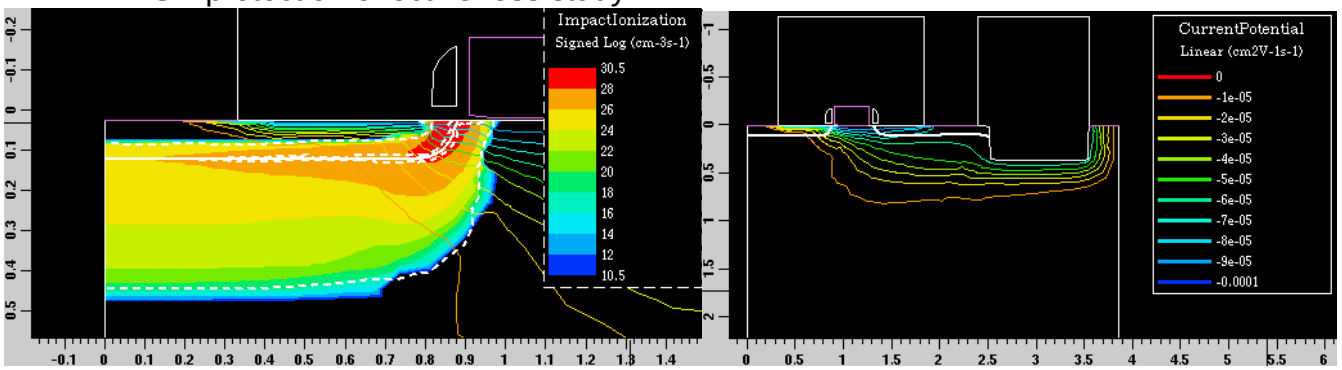


(1) current distribution at I=5E-04A

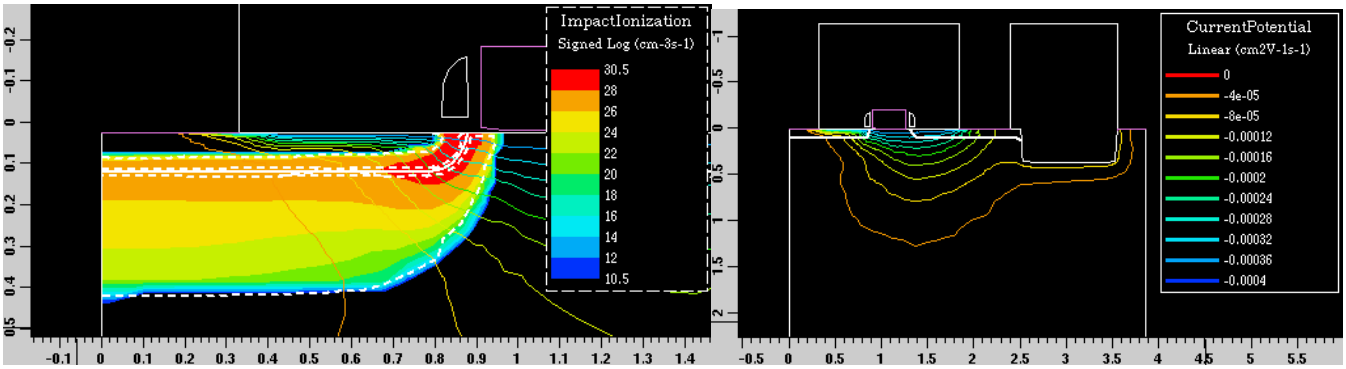
(2) current distribution at I=2E-03A

(3) current distribution at I=1E-02A

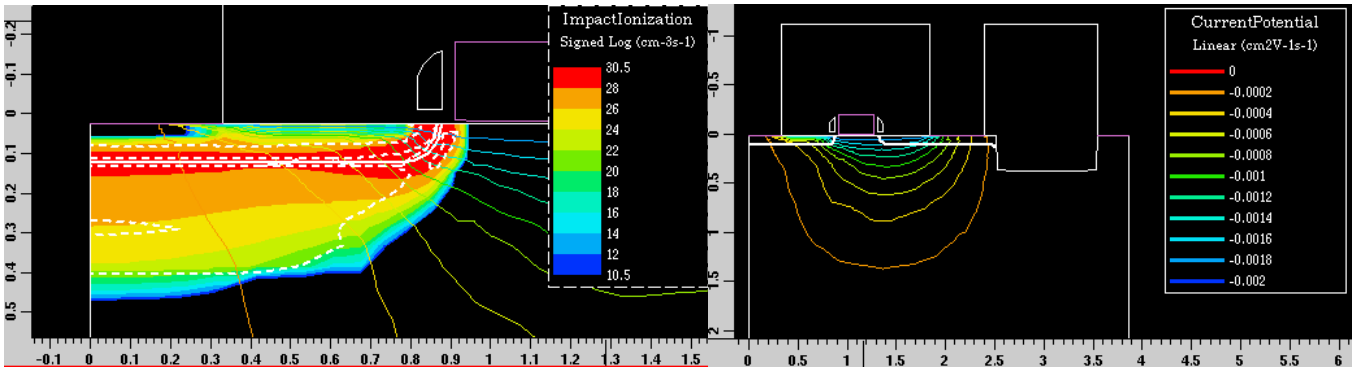
Figure 25. Current density distribution flowing throw a perpendicular plane from the center of the gate to 3 μm down the substrate. All plots have the same scale. Vertical scale magnitude not relevant. Notice the double relative peak in (3).



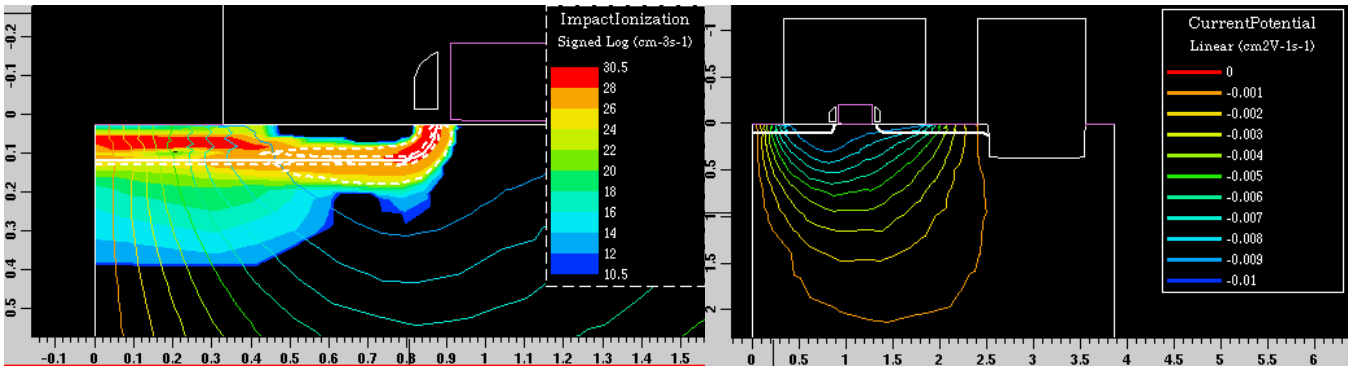
(1) Impact ionization density (left) and total current (right) at I=1E-04A



(2) Impact ionization density (left) and total current (right) at I=5E-04A

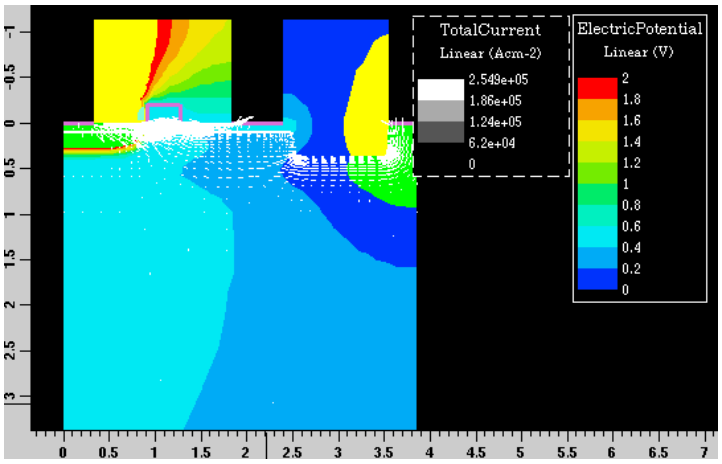


(3) Impact ionization density (left) and total current (right) at I=2E-03A

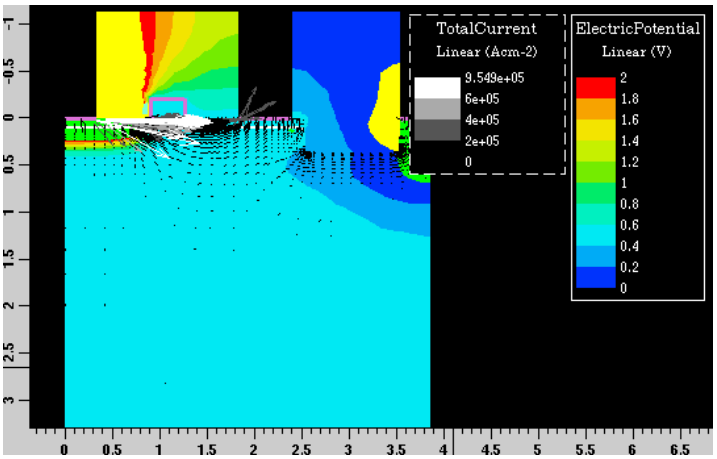


(4) Impact ionization density (left) and total current (right) at I=1E-02A

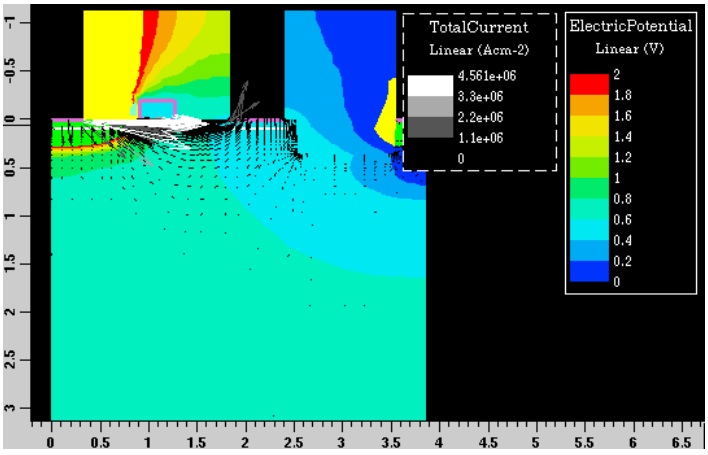
Figure 26. Impact ionization density and total current. Impact ionization ranges from 1E12 $cm^{-3}s^{-1}$ to 1E31 $cm^{-3}s^{-1}$ in logarithmic scale. The depletion region is delimited by the white dashed lines.



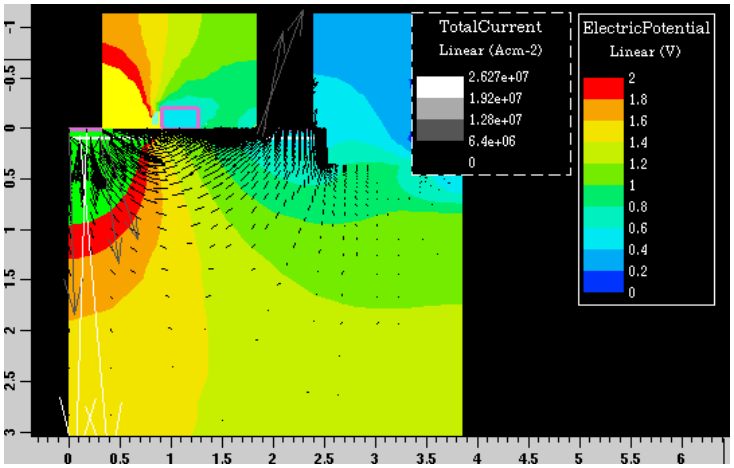
(1) Potential and total current at I=1E-04



(2) Potential and total current at I=5E-04



(3) Potential and total current at I=2E-03



(4) Potential and total current at I=1E-04

Figure 27. Electric potential and total current. Potential ranges from 0 to 2V, which yields in silicon areas out of scale which are in light green. Arrows have not the same scale. Notice the change in relative size and direction of the arrows at (4) in comparison with the rest of figures.

2.1.2 Single device simulations

TCAD 2D simulations were first carried out for single devices. Because the models are two-dimensional, Taurus-Medici does not take into consideration three-dimensional effects such as different currents through the fingers or the actual donut shape of the LVTSCR. Other considerations such as contact resistance were not taken into account either. For every device, DC and TLP simulations were performed and compared, when possible, with measurements.

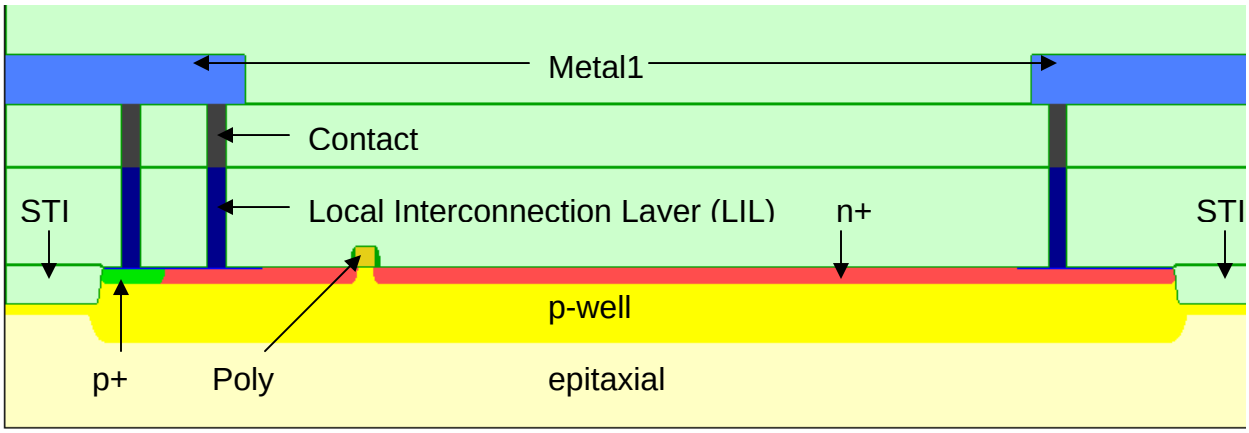
A summary of the characteristics of all the devices is in Table 8. Explanations on the simulation process are given in section 2 and source codes and transients are attached in appendices.

GGNMOST

Figure 28 depicts the layout view and cross section of the GGNMOST. Figure 29 shows the final device designed in T-Suprem4. Purple zones represent n-doped silicon material and blue p-doped silicon, gray with pink edge is aluminum and yellow represents oxide. Polysilicon and nitride are also present in the gate. The depth of the model (not shown in the figure) is 10um.

The results of the DC and TLP simulations are compared with real measurements in Figure 30. The trigger voltage of the simulated devices (7.4V for GO1 and for 8.4 for GO2) are very close, if not equal, to the measured ones (7.5V for GO1 and 8.4 for GO2). However, more little disagreement is found with the holding voltage, with 4.5V for both models and 5.0 and 5.8 for the GO1 and GO2 real devices.

(a)



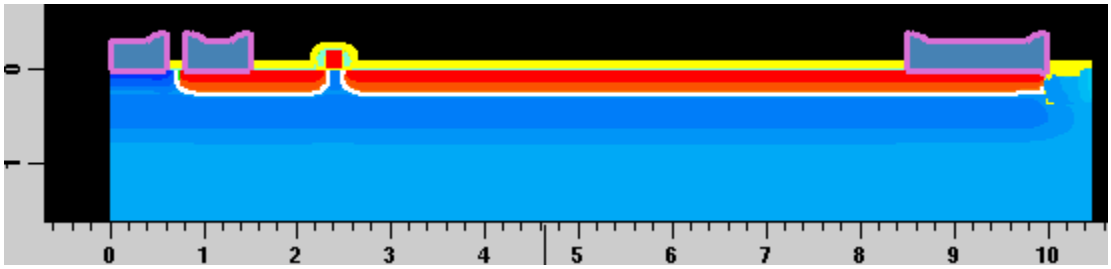
(b)

Figure 28. (a) Layout view and (b) cross section of the GGNMOST

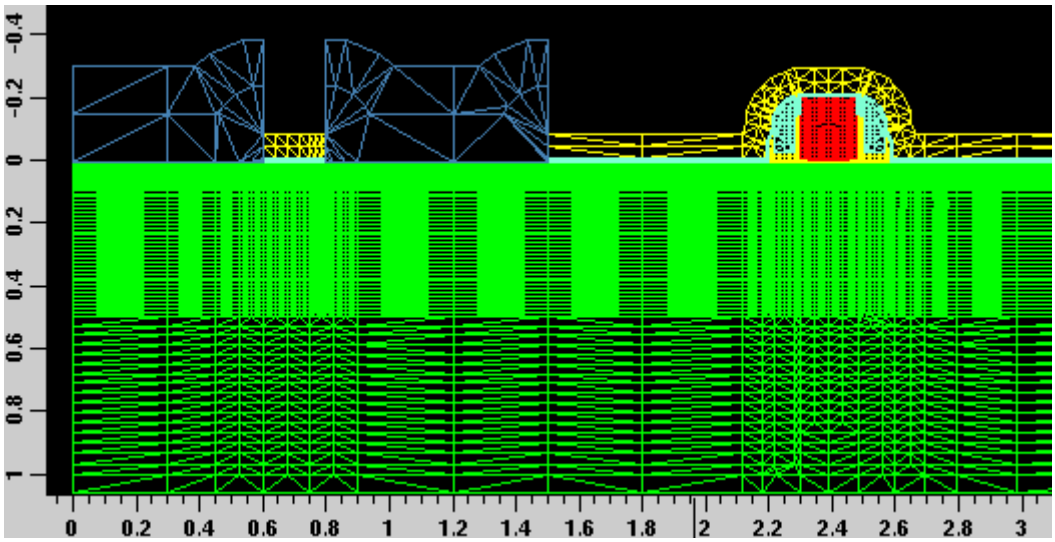
A special consideration must be taken on the slope of the curves after snapback. The R_{on} of the simulated device is lower than the measured one. The next section tries to explain why.

Parasitic resistance estimation

The probe needles used in TLP equipment have tips from 10 μm to 50 μm radius. Such a small area results in a contact resistance, which depends on the material of the needles, the pad material, the thickness of native oxides that coat the surfaces, the overdrive distance used, temperature, humidity, etc. It was reported that this parasitic resistance can range from 1 Ω to 4 Ω even after calibration [Grund05].



(a)



(b)

Figure 29. (a) Cross section view of the simulated GGNMOST taken from Taurus-Visual software.(b) Zoom of the source area to appreciate the grid density.

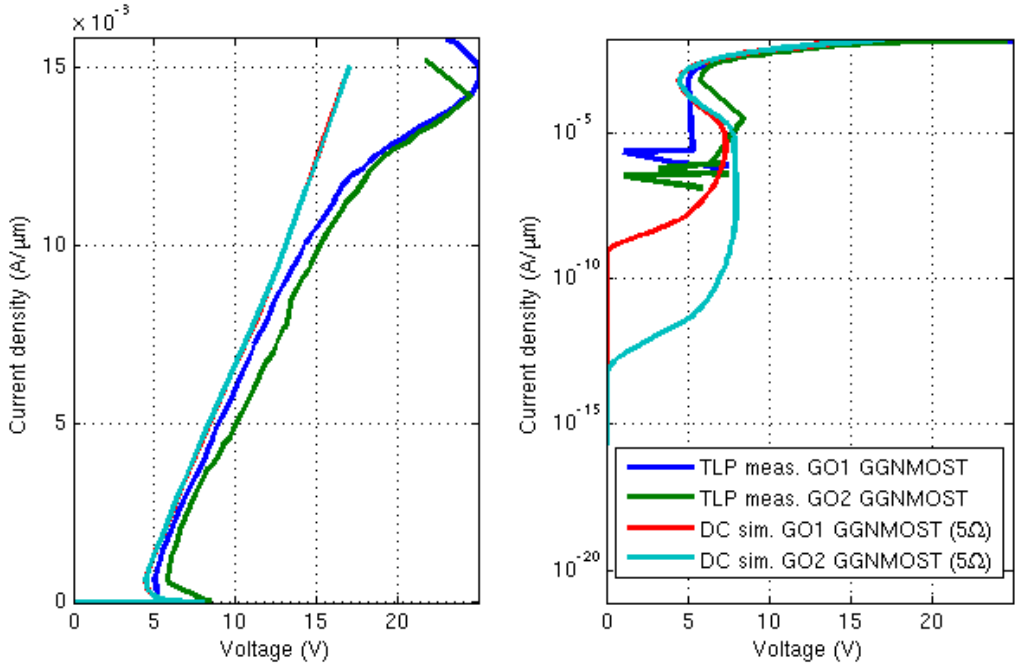


Figure 30. Comparison between TLP measurements and DC and TLP simulations of the GGNMOST. The results with (5Ω) mean that a parasitic 5Ω resistance was added in post processing for fitting purposes.

Unfortunately, the measurements were realized using regular probes. Therefore, it is reasonable to consider the contribution of the contact resistance to the total parasitic resistance in the abovementioned range.

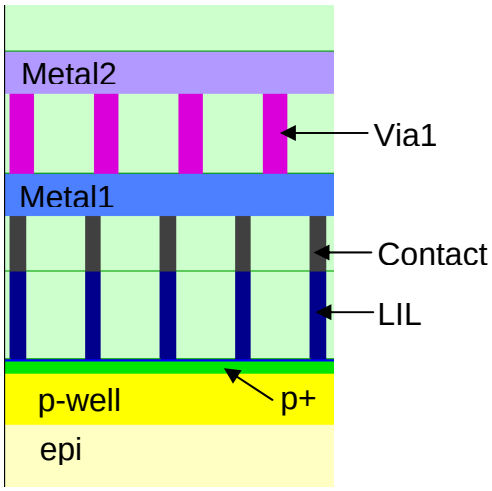


Figure 31. Cross section of cathode of the LVTSCR used for resistance estimation of the contacts and vias.

Another contributor to the parasitic resistance is all the metal layers and vias/contacts in the ESD current path from the bond pad to the ESD protection devices.

For this design, metal1 and metal2 rails were used from the bondpad to the device. The typical resistance value per contact ($R_{contact}$) in our technology is 25Ω [C14DRM]. The number of contacts placed in the layout and the space between them was measured to calculate the parallel contact resistance. Two rows of contacts in parallel are placed in the drain and one row in the source. The total resistance due to the contacts is calculated as follows:

$$R_{contacts} = \frac{1}{Wn\left(\frac{1}{R_{contact}/r}\right)} \qquad \text{Eq. 2.1}$$

where W is the width of the device, n the number of contacts per micron and r the number of rows in parallel. In our case W =100 μm, n =0.8 μm^{-1} and r =2,

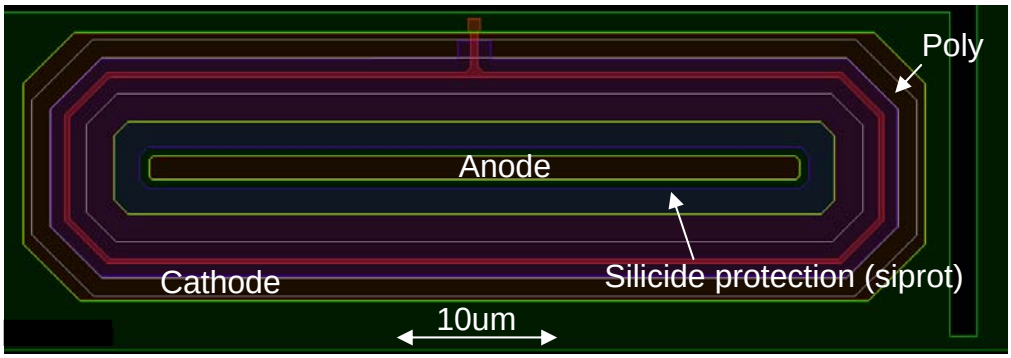
$R_{contacts}^{source} = R_{contacts}^{drain} / 2 =$ 0.2 Ω. Assuming that the ESD current uniformly distributed along the contacts, this makes a total voltage contribution of 0.45V at the maximum applied TLP current (1.5A).

Focusing on metal layers, the resistivity of melta1 and metal2 is 68 $m\Omega / square$ which both in parallel makes 34 $m\Omega / square$. A rough path dimensions measurement gives a L/W = 500 μm/25 μm = 20 squares. This gives a resistance of 0.7 Ω. Assuming the contribution of some other wider paths present in the layout it can be concluded that the resistance due to metal layers can well be 1 Ω. In addition, at high current densities, self-heating increases the resistance of metal rails and contacts [C14DRM].

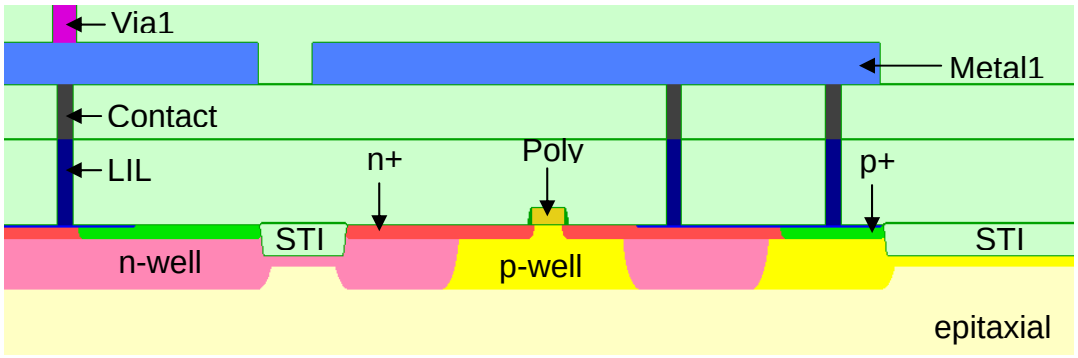
LVTSCR

The layout and cross section views of the LVTSCR are shown given (Figure 32). Figure 33 depicts the cross sectional view of the modeled LVTSCR. In this particular case, the LVTSCR was used in a pin for IIC protocol purposes.

In this case, differences between simulated GO1 and GO2 LVTSCR were found. However, the differences between the simulated devices and the real device were somewhat higher. The trigger voltage for the real device was 8.29V whereas for the simulated devices was 6.12 and 6.75 (GO1 and GO2, respectively). Holding voltages, however, are closer.



(a)



(b)

Figure 32. (a) Layout view and (b) cross section of the donut shape LVTSCR

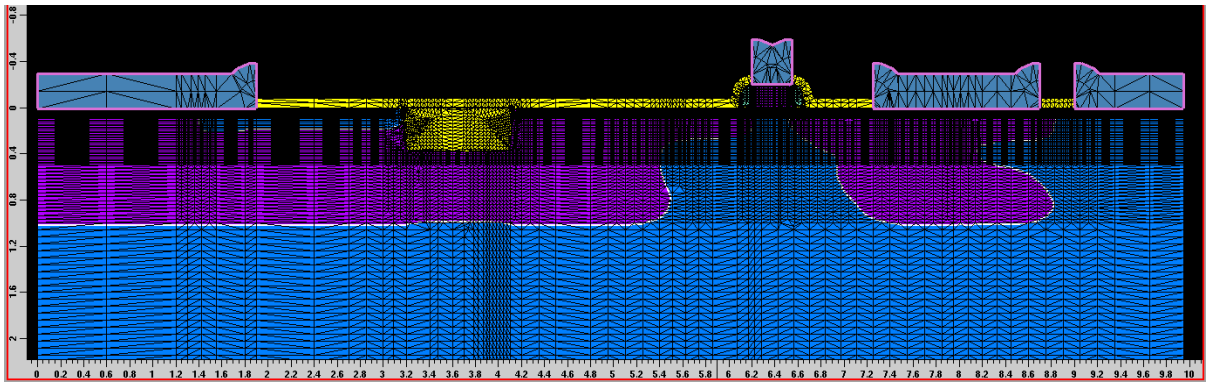


Figure 33. Cross section view of the simulated LVTSCR taken from Taurus-Visual software.

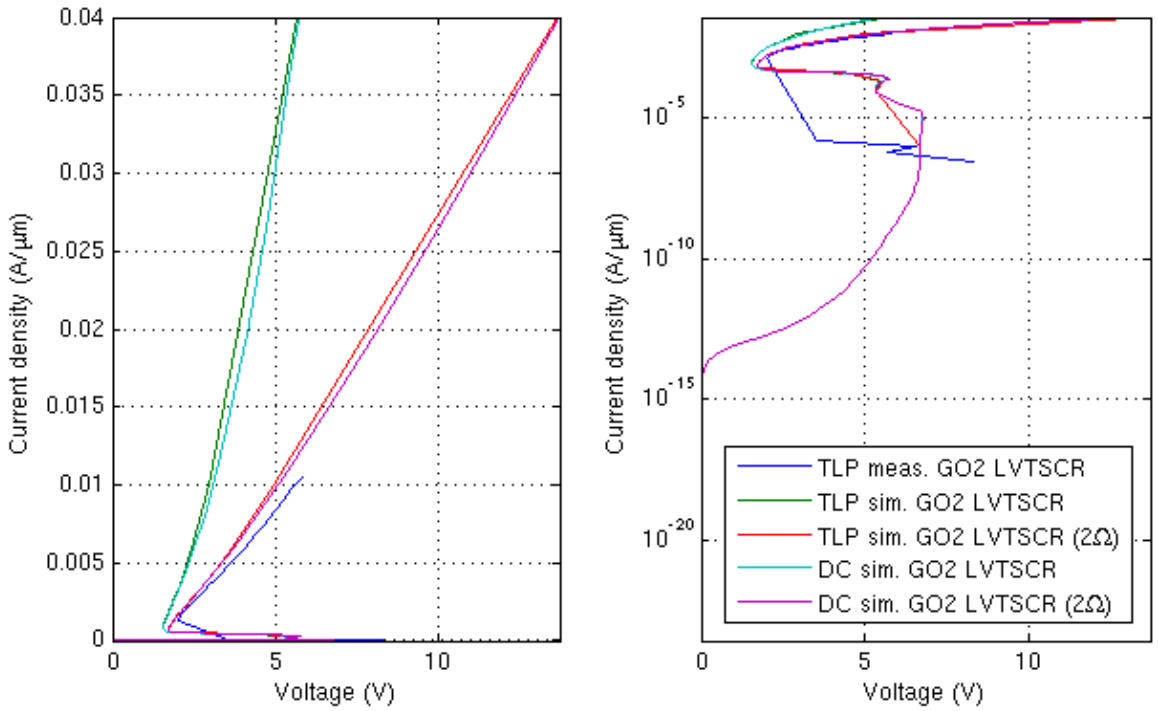


Figure 34. Comparison between TLP measurements and DC and TLP simulations of the LVTSCR. The results with (2Ω) mean that a parasitic 2Ω resistance was added in post processing for fitting purposes

Device	Trigger voltage, V_{t1} (V)	Trigger current, I_{t1} (A/ μm)	Holding voltage, V_h (V)	On-resistance, R_{on} (Ω)
GGNMOST GO1 (real)	7.5	7.25e-7	5.0	10
GGNMOST GO2 (real)	8.4	3.5E-05	5.8	10
GGNMOST GO1 (model)	7.4	4.8E-06	4.5	5(+5)
GGNMOST GO2 (model)	8.4	5E-06	4.5	5(+5)
LVTSCR GO2 (real)	8.29	3.02E-07	2.0	4.3
LVTSCR GO1 (model)	6.12	1.59E-05	1.7	2.3(+2)
LVTSCR GO2 (model)	6.75	1.66E-05	1.7	2.3(+2)

Table 8. Summary of parameters for the snapback devices under study.

STI DIODE

The simulated cross section and en Figure 35 and Figure 36. It consists of both n+ and p+ implants on p-well separated by an STI. Simulation results are depicted in Figure 36 and Figure 37. A bending due to thermal effects is seen for TLP simulations. The forward voltage V_d is around 0.7V, on-resistance R_{on} 2Ω and the reverse breakdown voltage V_r is around 40V.

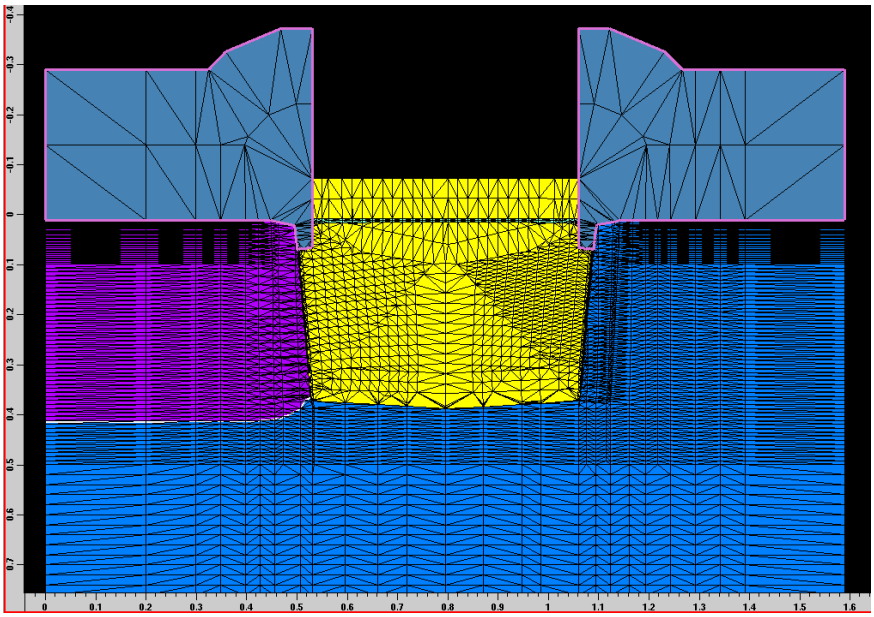


Figure 35. N+/P-well STI diode TCAD model cross section.

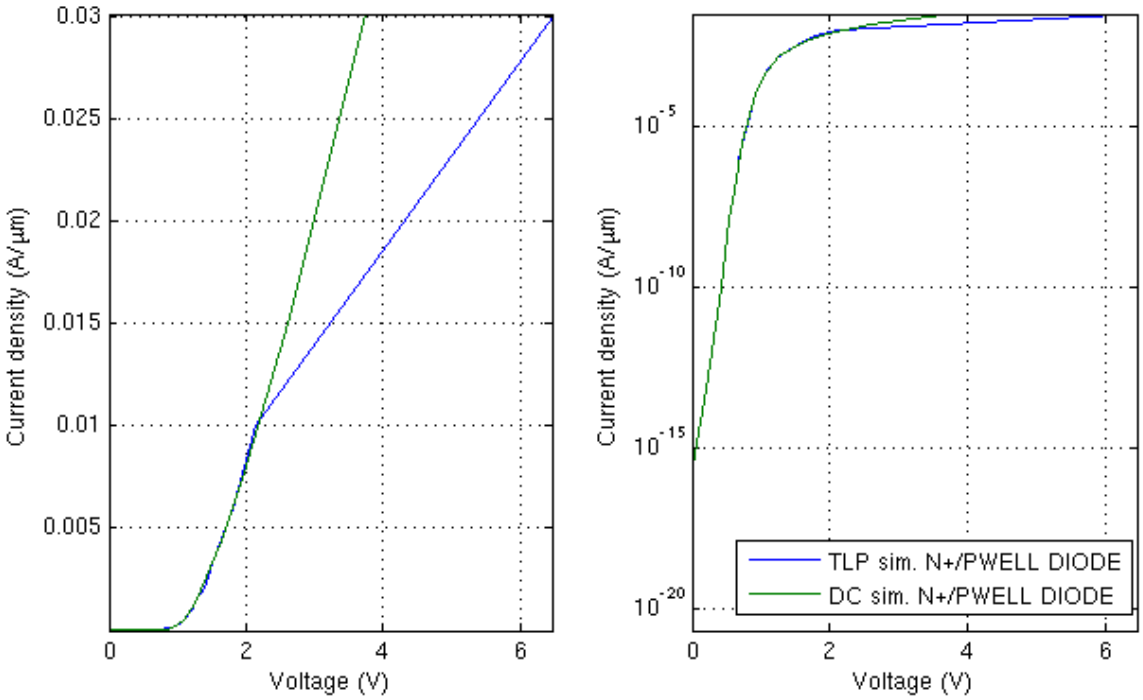


Figure 36. TLP and DC simulation results of the N+/P-well STI diode in forward mode.

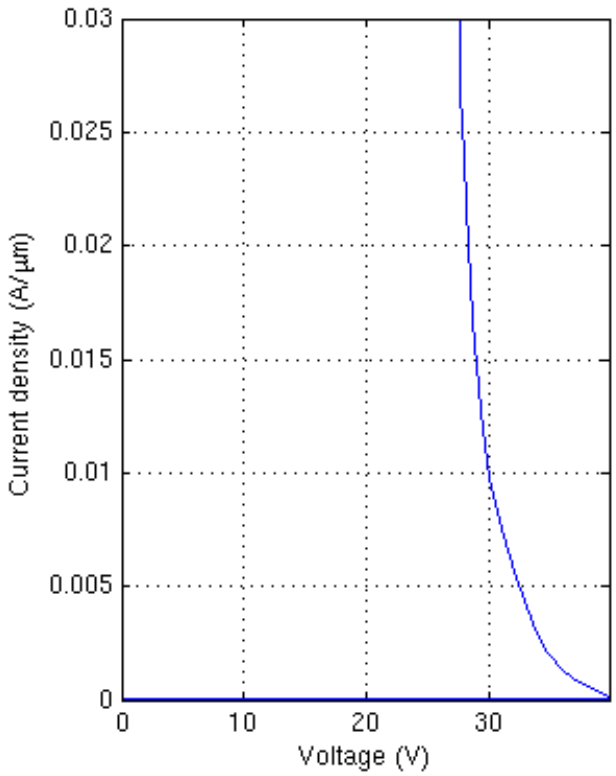


Figure 37. TLP and DC simulation results of the N+/P-well STI diode in reverse mode.

NMOS clamp

The cross section view of the NMOS clamp is shown in Figure 38. Figure 39 shows the Ids-Vgs and Ids-Vds curves for the modeled NMOST. The V_t was calculated by T-Suprem to be 0.9V, somewhat higher than in our technology (around 0.4-0.8V, depending on the size parameters).

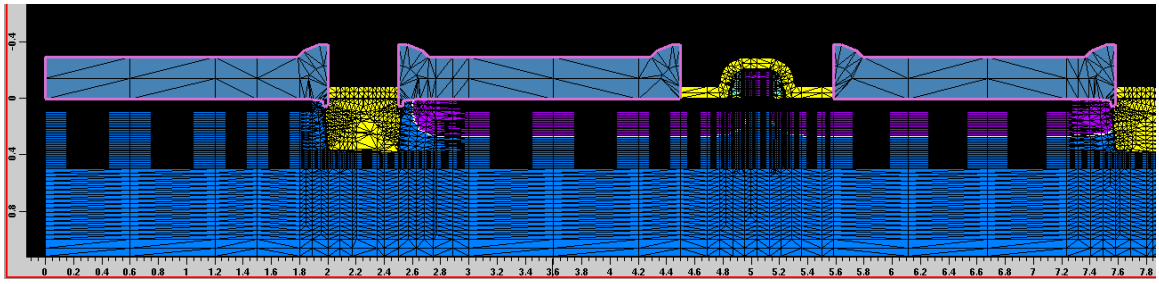


Figure 38. NMOS TCAD model cross section.

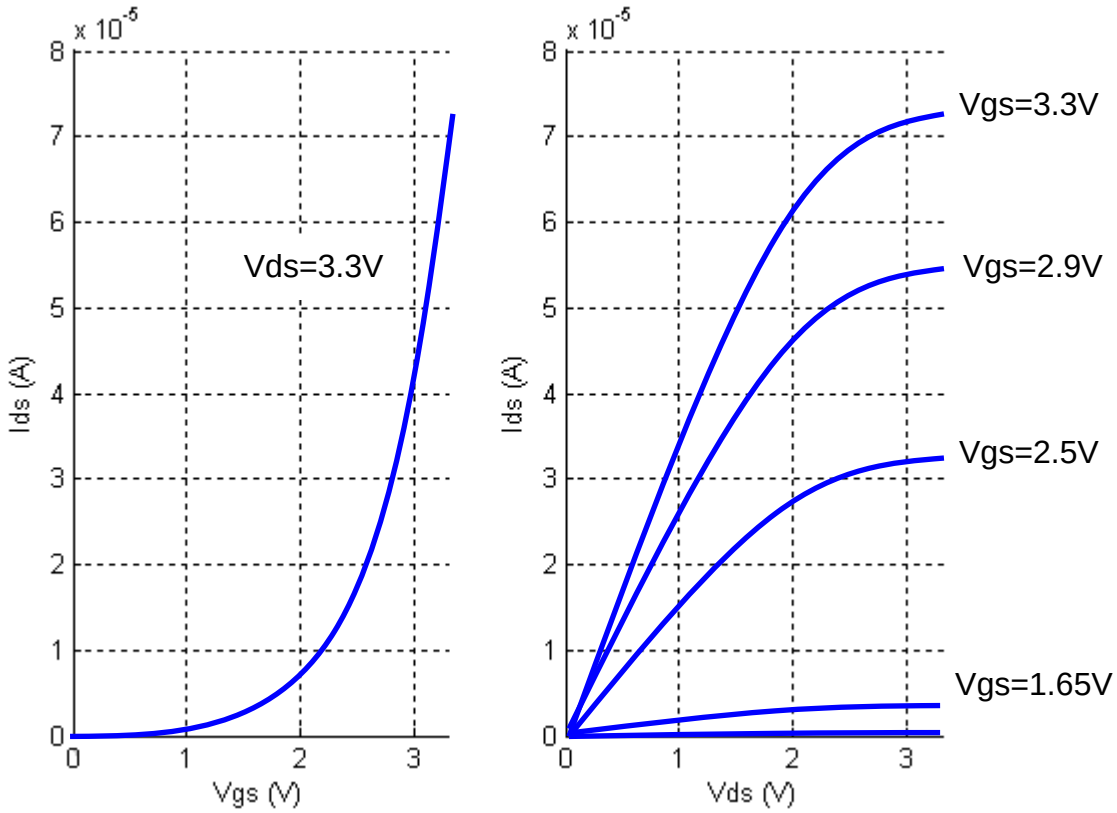


Figure 39. Ids-Vgs and Ids-Vds curves for the modeled NMOST.

2.2 Secondary protection analysis

2.2.1 Analysis methodology

The secondary protection analysis consisted of studying the effectiveness of two-staged ESD protection for different primary protections. A series of mixed mode TCAD simulations were performed for combinations of primary protections, ESD models and stress levels, and secondary protection design parameters. From the thin gate oxide protection point of view, the relevant part of a transient simulation is the first nanoseconds, when the maximum voltage is reached.

Figure 40 shows a simplified schematic of the protection circuit under study. In this section, the following nomenclature will be used:

V_1, V_2: voltage at the primary/secondary protection anode, respectively.

I_1, I_2: current through the primary/secondary protection anode.

W_1, W_2: width of the active device of the primary/secondary protection.

R: resistance value of the secondary protection

V_{GO}: voltage at the gate oxide to protect from the ESD stress.

The main objective of the simulations was, for a given maximum gate oxide breakdown voltage, to obtain a series of safe design areas for different values of R and W_2 and for any combination of ESD model, stress level and primary protection (see

Table 9). This provides the ESD protection designer with a range of W_2 - R values that assure the effectiveness of the whole ESD protection circuit.

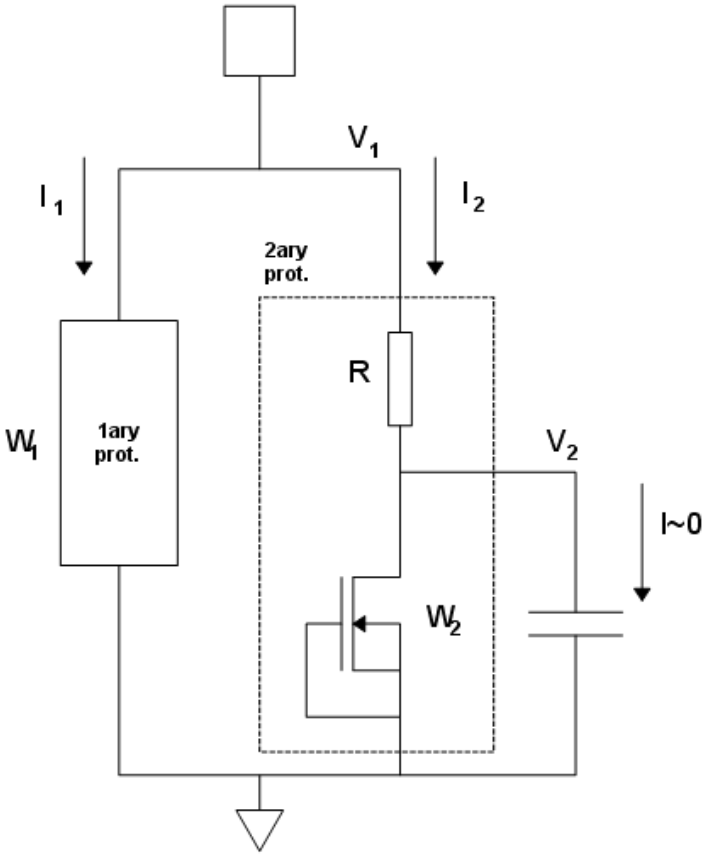


Figure 40. Diagram of a two-staged ESD protection circuit.

ESD model	ESD stress level	Primary protection
HBM	3KV, 5KV, 8KV	LVTSCR
CDM	1A, 3A, 5.75A	GGNMOST
IEC (system level)	2KV,4KV,6KV,8KV	Non-boosted rail based
		Boosted rail based

Table 9. Combinations of simulations for secondary protection analysis. Every ESD model and stress level combination was applied to each primary protection with a secondary protection.

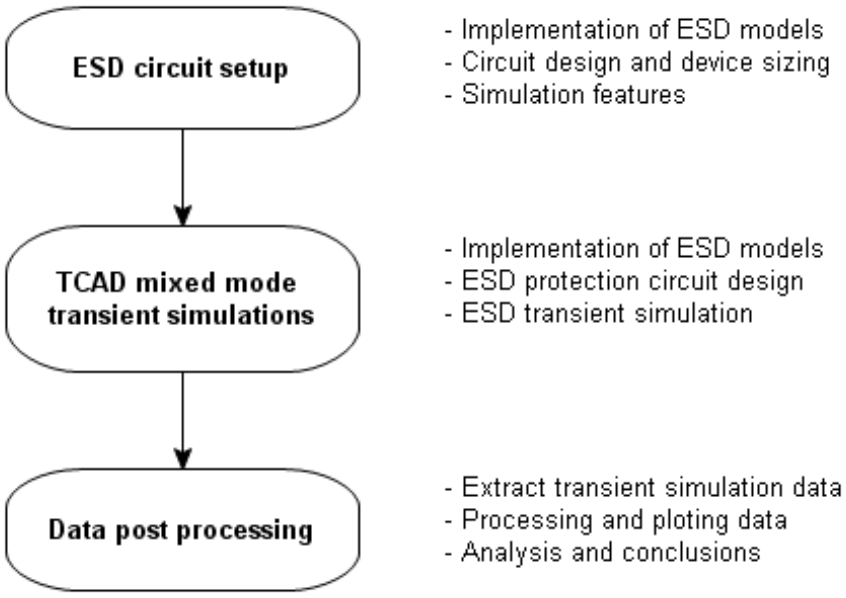


Figure 41. Diagram of the followed data analysis approach.

Figure 42 shows the four simulated circuits, using a resistor in series with a GGNMOST as secondary protection in all of them. Transient simulations in TCAD and data post processing were carried out. All the transient simulation results, source codes and other figures are attached in appendixes. Figure 41 summarizes the analysis flow.

For the sake of simplicity and simulation speed, only positive ESD pulses are injected and thus the corresponding primary protection device for negative pulses is not included in circuits, that is, GGPMOST or diodes. Also, it is important to notice that in real implementations of rail based circuits it is common to have a trigger circuit (also called crowbar) that when detects an ESD stress raises quickly the voltage at the gate of the NMOST. The case in Figure 42, however, the gate is shorted to the bondpad. This can be considered as a worse case with a slow trigger circuit.

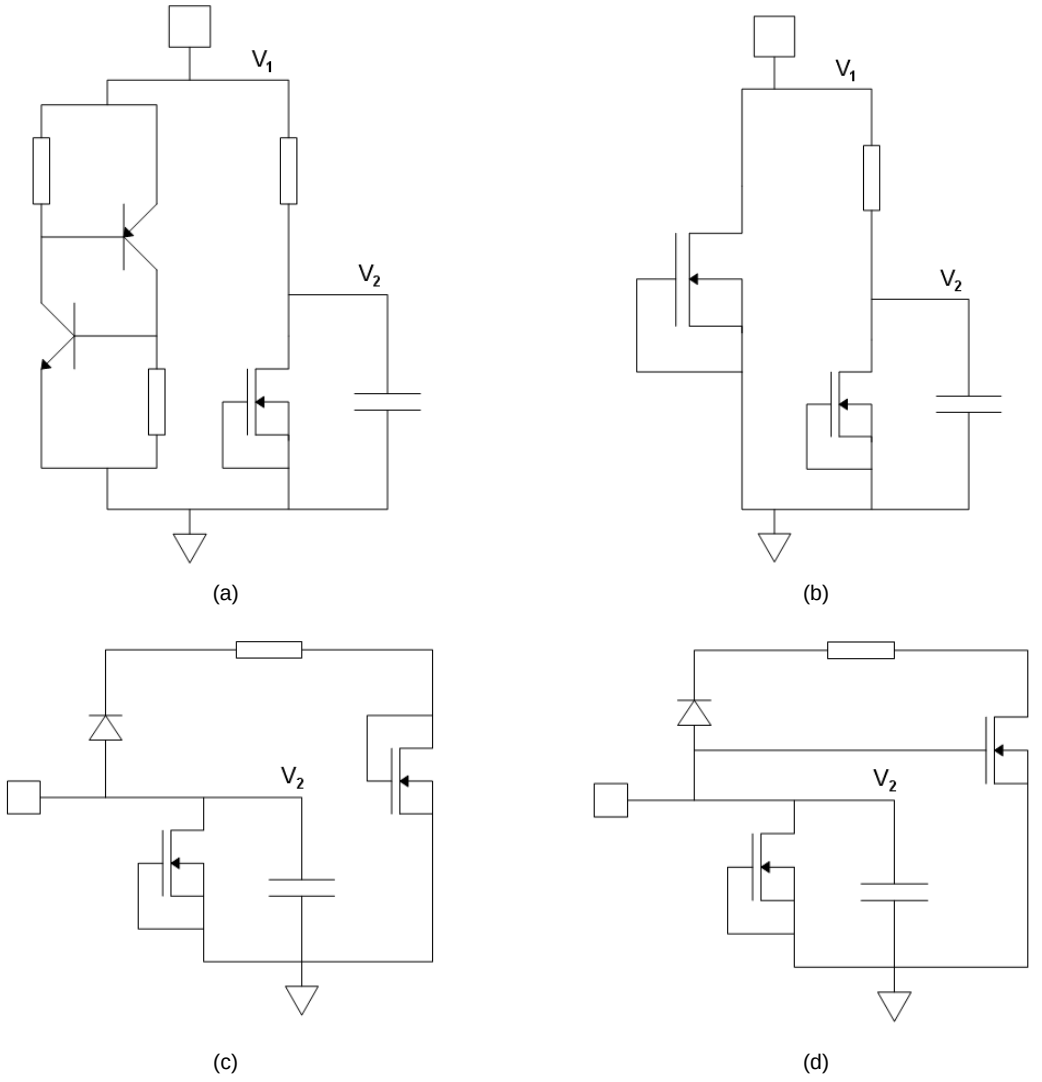


Figure 42. Diagram of the circuits simulated in the mixed mode simulation analysis: (a) LVTSCR + GGNMOST circuit (b) GGNMOST + GGNMOST circuit (c) Non-boosted rail based + GGNMOST circuit (d) Boosted rail based + GGNMOST

ESD models implementation

Since ESD model standards give some tolerance to amplitudes and times, the worse case was taken for each model in terms of effectiveness, that is higher amplitudes and shorter rise times.

HBM and CDM waveforms were implemented in Taurus-Medici by using built-in exponential current sources. For implementing IEC, the waveform was divided in

a number time chunks in which a pulse current source was enable at a time, thus emulating the IEC waveform shape.

- HBM. The HBM waveform can be mathematically expressed as a double exponential function:

$$I_{HBM} = I_{\max}\left(1-\exp\left(-\frac{t-t_{d1}}{\tau_1}\right)\right), \text{ when } t_{d1} < t < t_{d2} \quad \text{Eq. 2.2}$$

$$I_{HBM} = I_{\max}\left(\exp\left(-\frac{t-t_{d2}}{\tau_2}\right)-\exp\left(-\frac{t-t_{d1}}{\tau_1}\right)\right), \text{ when } t > t_{d2} \quad \text{Eq. 2.3}$$

Figure 43 shows the simulated waveform, which corresponds with t_{d1} = 0s, τ_1 = 1ns, t_{d2} = 5ns, τ_2 = 165ns.

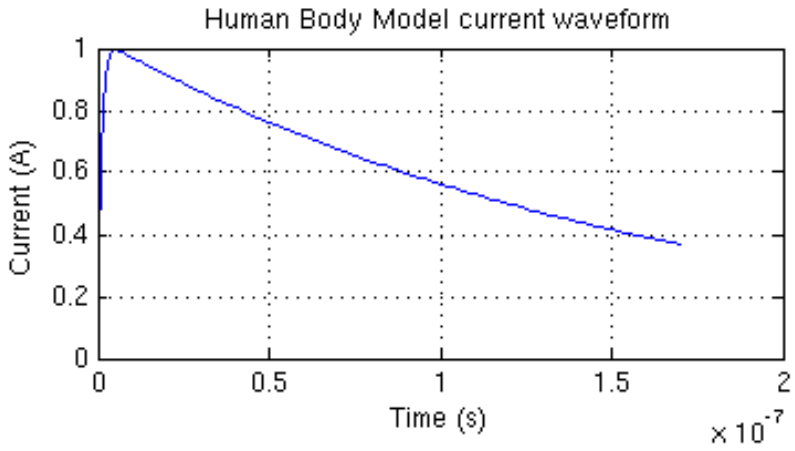


Figure 43. Simulated HBM waveform (normalized).

- CDM. The CDM waveform can be expressed as an exponentially attenuated sinusoid:

$$I_{CDM} = I_{\max} e^{r/4} \sin(2\pi f t) e^{-At}, \text{ when } t > t_{d2} \quad \text{Eq. 2.4}$$

with f=1GHz, r=1.4, A=f*r.

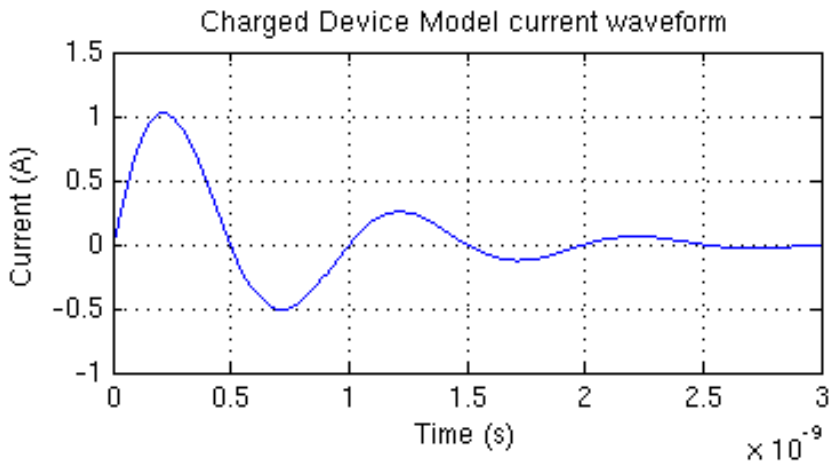


Figure 44. Simulated CDM waveform (normalized).

- System level. The system level waveform can be implemented by the following equations [Fotis06]:

$$I_A = I_1 \frac{\left(\frac{t}{\tau_1}\right)^n}{1+\left(\frac{t}{\tau_2}\right)^n} \exp\left(\frac{1}{\tau_2}\left(\tau_1\left(\frac{n\tau_2}{\tau_1}\right)^{1/n} - t\right)\right) \quad \text{Eq. 2.5}$$

$$I_B = I_2 \frac{\left(\frac{t}{\tau_3}\right)^n}{1+\left(\frac{t}{\tau_4}\right)^n} \exp\left(\frac{1}{\tau_4}\left(\tau_3\left(\frac{n\tau_4}{\tau_3}\right)^{1/n} - t\right)\right) \quad \text{Eq. 2.6}$$

$$I_{IEC} = I_A + I_B \quad \text{Eq. 2.7}$$

where τ_1=0.7ns, τ_2=2ns, τ_3=12ns, τ_4=37.8ns and n=1.8.

Since Medici-Taurus does not provide a way to implement such waveform, a script was programmed for obtaining the parameter values of a series (around 150) pulse type current sources. Because of the limit of instances in mixed mode simulator in Taurus-Medici, it was necessary to use different time steps to limit the number of current sources, as it is shown in Figure 45.

Table 10 and Table 11 collect the values of all the abovementioned ESD model waveform parameters used in this study.

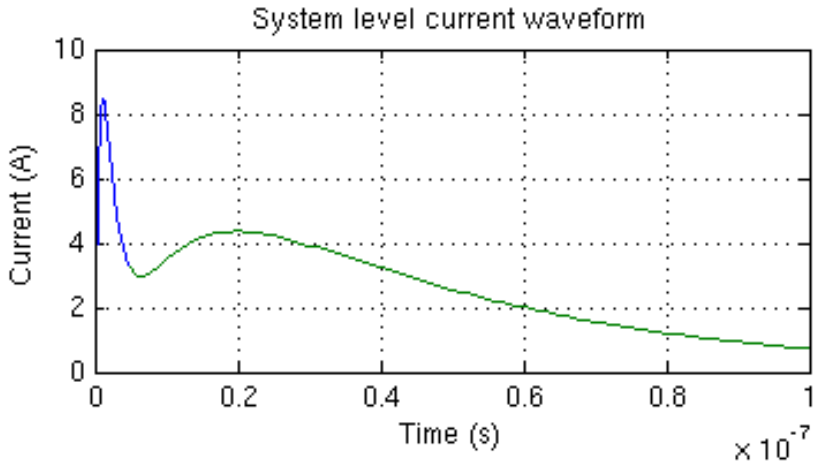
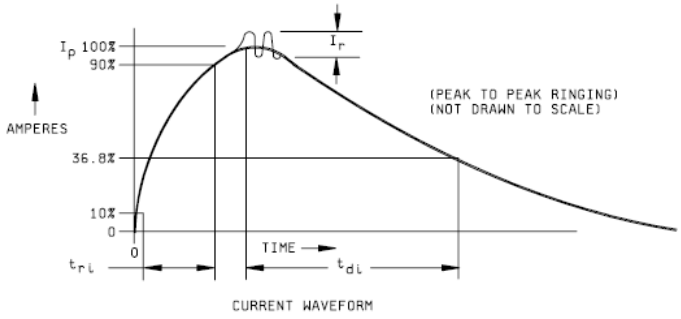
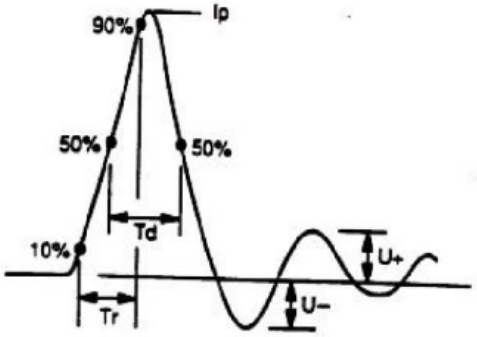
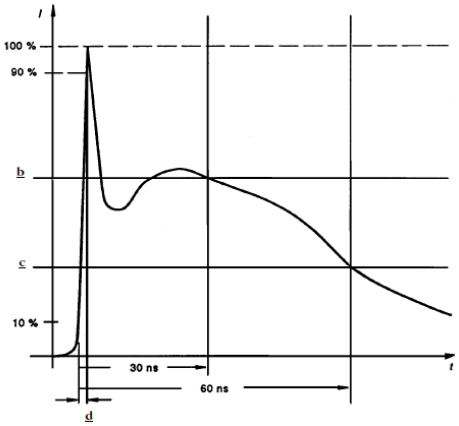


Figure 45. Example of simulated system level waveform for I_1=8.75A , I_2 =4.5A. Blue means shorter time steps.

Table 10. Summary of the ESD models and stresses of study. The simulated peak current is the result of applying the tolerance according each ESD model standard (10% for HBM, 15% for CDM and 20% for IEC)

Model	Stress level	Peak current (A)	Simulated peak current (A)
HBM	3KV	2	2.2
	5KV	3.33	3.67
	8KV	5.34	5.87
CDM	1A	1	1.15
	3A	3	3.45
	5.75A	5.75	6.613
IEC	2KV	7.5	9
	4KV	15	18
	6KV	22.5	27
	8KV	30	36

Table 11. Summary of the simulated ESD waveforms.

Model	Comments on simulated waveform	Figure
HBM	- t_r = 2ns - t_d = 70ns - No peak ripple.	
CDM	- t_r = 400ps - t_d = 470ps - U-=0.5*Ip U+=0.25*Ip	
IEC	- b=0.54* Ipeak (+30%) - c=0.27*Ipeak (+30%) - d=0.7ns	

Primary protection design criteria

Since the primary protection will carry most of the ESD current, it must be sized to be robust enough. The peak density current for HBM analysis was assumed equal to the measured TLP density currents just before failure breakdown. In [Smedes06] it was shown that 1A TLP is approximately equivalent to 0.5KV IEC

in terms of robustness. According to the IEC waveform peak currents (see Table 10), 0.5KV IEC corresponds to a peak current of 1.875A. It is thus assumed that the maximum current densities of a device for a IEC-like stress is 1.875 times the maximum current density of that device for TLP stress.

The reasoning behind this lays on the Wunsch-Bell equation [Wunsch68]. The power-to-failure, that is, the maximum power that a semiconductor device can withstand without thermal failure, is higher for shorter pulses. In the case of IEC waveform, the 2nd peak carries most of the energy and therefore is the most relevant part of the waveform concerning power dissipation. For the same maximum current amplitude, TLP pulses have more energy than the IEC 2nd peak because there are longer. The power-to-failure for IEC stresses is therefore higher.

Concerning CDM, since the current handled during a CDM stress is lower than for HBM/TLP stresses, the abovementioned criterion for IEC was also followed for CDM. Notice that the amount of transferred charge in CDM is much lower than in IEC and therefore this criterion is quite conservative. However, ESD protections are designed to protect against not only CDM stresses but also other models as for example HBM, which is the most commonly used. Therefore, it would not be realistic to size the primary protection for only CDM stresses. A summary of the primary protection sizing is shown in
Table 12 and Table 13.

Table 12. Summary of the device robustness criteria for different stresses. The values represent the maximum current density that the devices can carry and it will be considered as a safety limit in simulations.

Device	**TLP and HBM** ($mA/\mu m$)	**IEC and CDM** ($mA/\mu m$)
GGNMOST	10	18.75
LVTSCR	40	70
Diode (N+/P-well STI diode)	15	28.125
NMOST	1	1.875

Table 13. Summary of the sizes of the devices used in the simulations.

Pad based

Circuit	Model	Level	1ary prot. Size (um)	Maximum ESD current (A)	Maximum robustness current for corresponding ESD level (A)
LVTSCR + GGNMOST	HBM	3KV	150	2.2	6
		5KV	150	3.67	6
		8KV	150	5.87	6
	CDM	1A	80	1.15	6
		3A	80	3.45	6
		5.75A	80	6.613	6
	IEC	2KV	150	9	11.25
		4KV	250	18	18.75
		6KV	375	27	28.125
		8KV	500	36	37.5
GGNMOST + GGNMOST	HBM	3KV	600	2.2	6
		5KV	600	3.67	6
		8KV	600	5.87	6
	CDM	1A	350	1.15	6.56
		3A	350	3.45	6.56
		5.75A	350	6.613	6.56
	IEC	2KV	600	9	11.25
		4KV	1000	18	18.75
		6KV	1500	27	28.125
		8KV	2000	36	37.5

Rail based

Model	Level	Diode (um)	NMOST (um)	Maximum ESD current (A)	Maximum robustness current for corresponding ESD level (A)
HBM	3KV	400	6000	2.2	6
	5KV	400	6000	3.67	6
	8KV	400	6000	5.87	6
CDM	1A	210	3200	1.15	6
	3A	210	3200	3.45	6
	5.75A	210	3200	6.613	6
IEC	2KV	400	6000	9	11.25
	4KV	667	10000	18	18.75
	6KV	1000	15000	27	28.125
	8KV	1334	20000	36	37.5

Analysis process

The analysis is divided into three steps. First, transient simulations were performed for every combination depicted in Figure 46. The data was therefore stored in a kind of eight-dimensional matrix. This was realized by means of a script code in MATLAB that sweeps all the directory tree were the different files with simulation results are located. The code stores all data in an objected-oriented programming (OOP) approach for the subsequent analysis. Transient simulations can thus be plotted as shown in Figure 47(a).

Second, the maximum V_2 value is taken and plotted in a $V_2^{\max}$ - W_2 plot for every R value (see Figure 47, steps 1 and 2). By interpolating each one of these curves at a certain $V_{GO\_breakdown}$ (see Figure 47, step 3), a $W_2 - R$ plot or safe design area plot like the one in Figure 48 is obtained for every combination of protection circuit, ESD model, stress level. Thus, in order for the secondary protection to be effective (that is, assure a $V_2^{\max}$ below $V_{GO\_breakdown}$), the R and W_2 values must be somewhere inside the safe design area.

Figure 49 depicts a snapshot of the used script. As far as the functionality is concerned, the main options are #0 and #100, which load and save simulation data, respectively. Option #100 creates all the plots to be studied and exports them in a readable format for a graphical user interface that will be described in the next section.

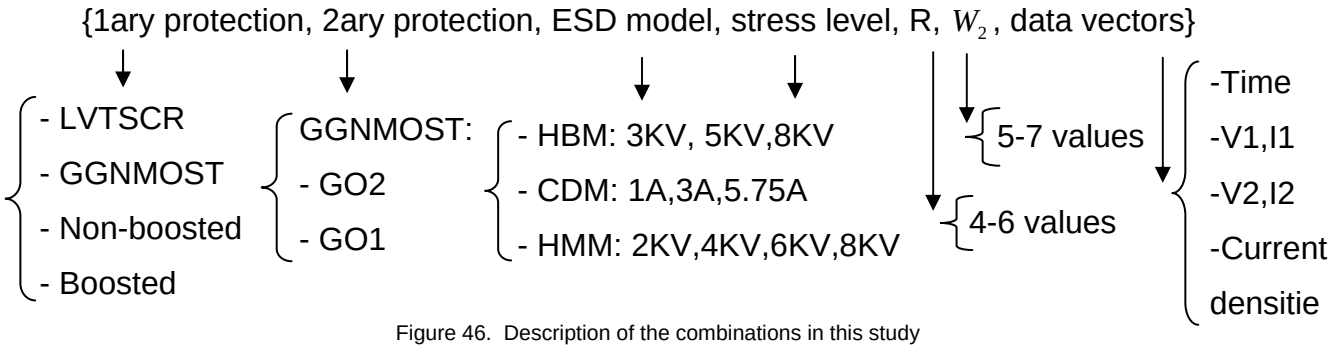
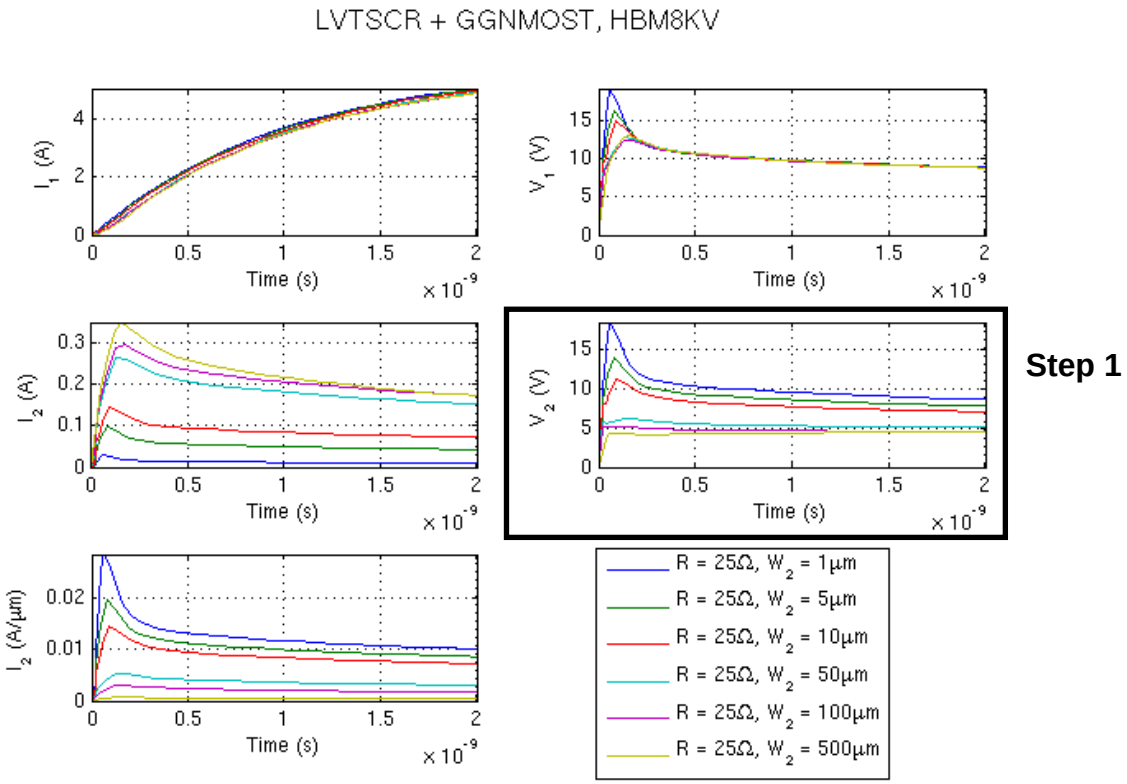
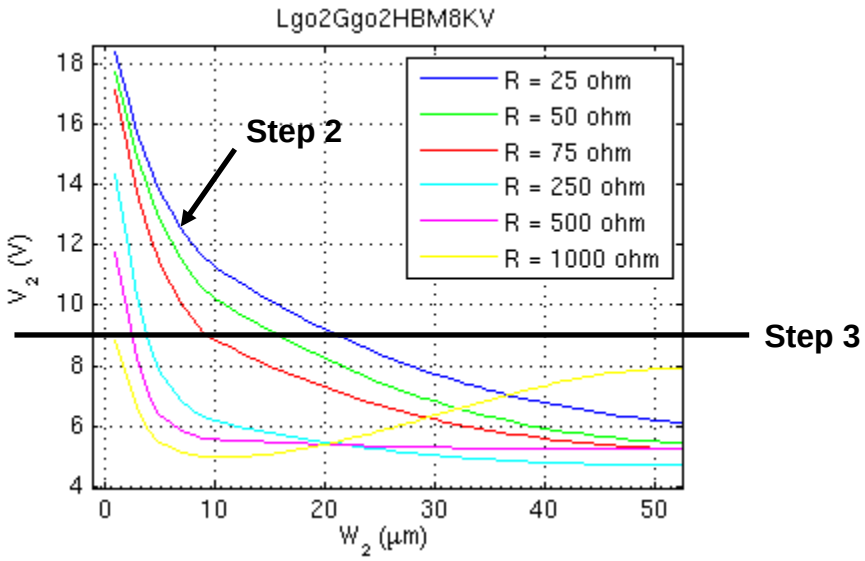


Figure 46. Description of the combinations in this study



(a)



(b)

Figure 47. Explanation of how the safe design areas were calculated. Step 1 represents the transient simulation for different R and W_2 values. Step 2 shows the values in step 1 plotted for interpolating at $V_{GO\_breakdown}$ in step 3.

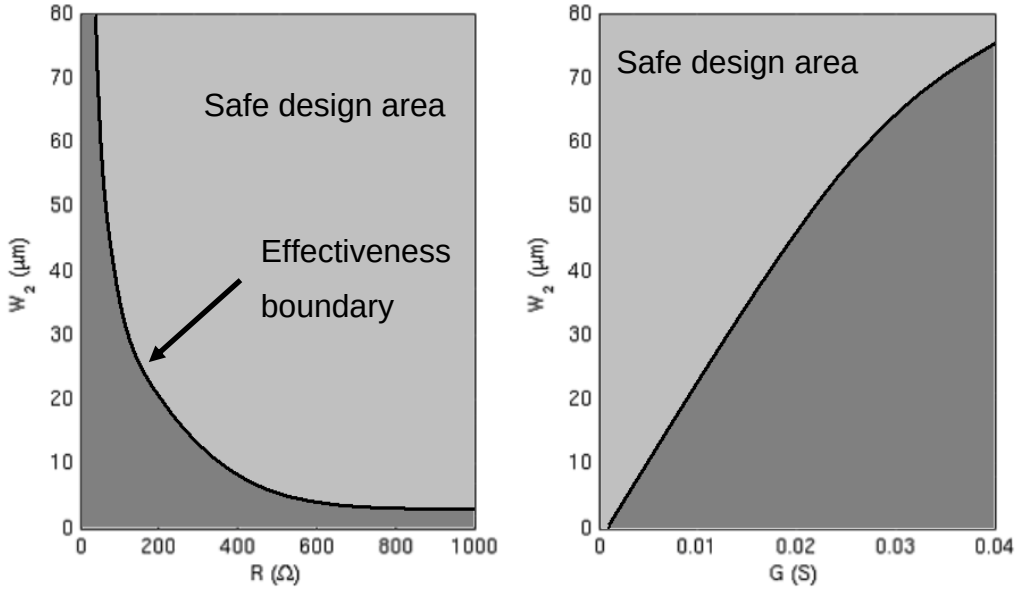


Figure 48. Example of safe design area plot.

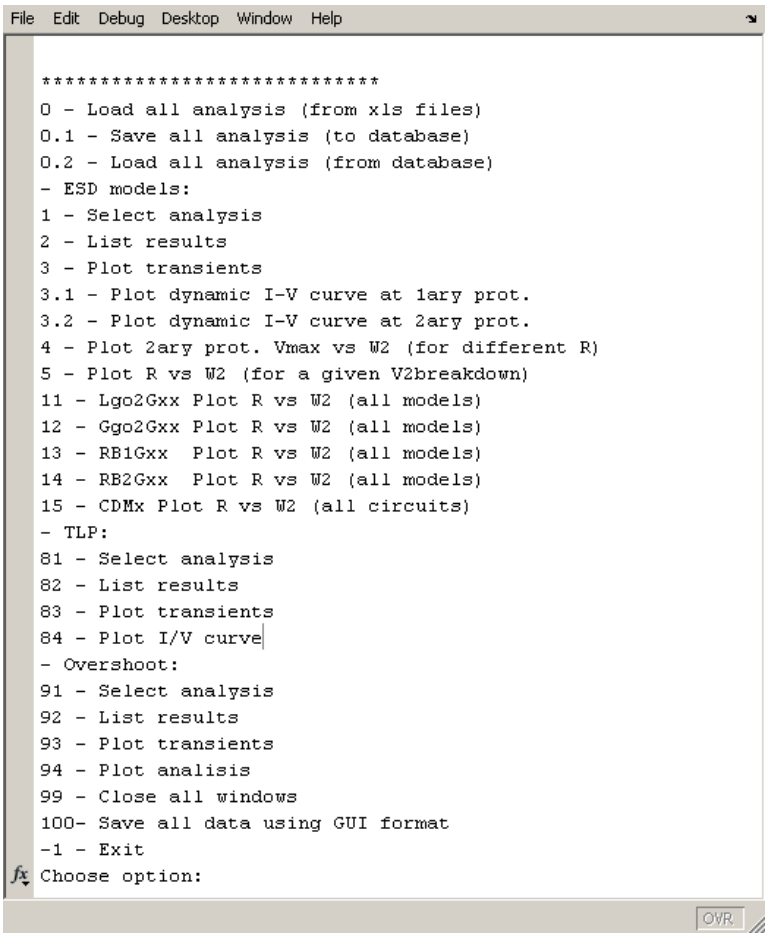


Figure 49. Snapshot of the loader program.

2.2.2 Data plotting tool (GUI)

It was found that, in order to extract information from the huge amount of data, that is, represent them in such a way that some conclusions can be achieved, a tool to handle the data in a straightforward fashion is necessary.

A Graphical User Interface (GUI) was programmed in MATLAB (see Figure 50). This GUI serves as parametric data loader and plotter, and easy enormously the task of plotting. All plots in this thesis were generated by using this tool. Emphasis on simplicity and documentation was done for further utilization by NXP employees.

It is important to point out that this tool is intended to be as flexible as possible, that is, to load and plot any type of data, not the one produced in this study. This and the usage of the tool are now described:

- The data samples to be plotted can be loaded either in MATLAB format (.mat extension files) or in plain text. An example of data file in plain text is shown in Figure 51.
- Plotting configurations are loaded from a separated file, in which the titles, labels, subplots layout and columns definition (that is, which columns of the data samples are x-axis and y-axis) is established. These files are in plain text format in a similar fashion to the data files. The plotting configurations are shown in *Plotting configurations* (see Figure 51).
- Due to the large amount of data that can be plotted (around 3000 different files with several columns representing time, voltages and currents) a filtering system is needed. An example is shown left-bottom corner of Figure 51. A logical AND function is implemented by the question mark. Only the data sample names in which name there is the words between question marks will be shown in the *Results list*.

- The data samples to be plotted can be selected individually or in groups by adding them to the Plotting cart.
- The type of plot to generate is selected in the *Plotting configurations* list. The corresponding plot will be created by clicking on the *Plot* button. A plain text file with the selected data is generated by clicking on the *Export to* button,

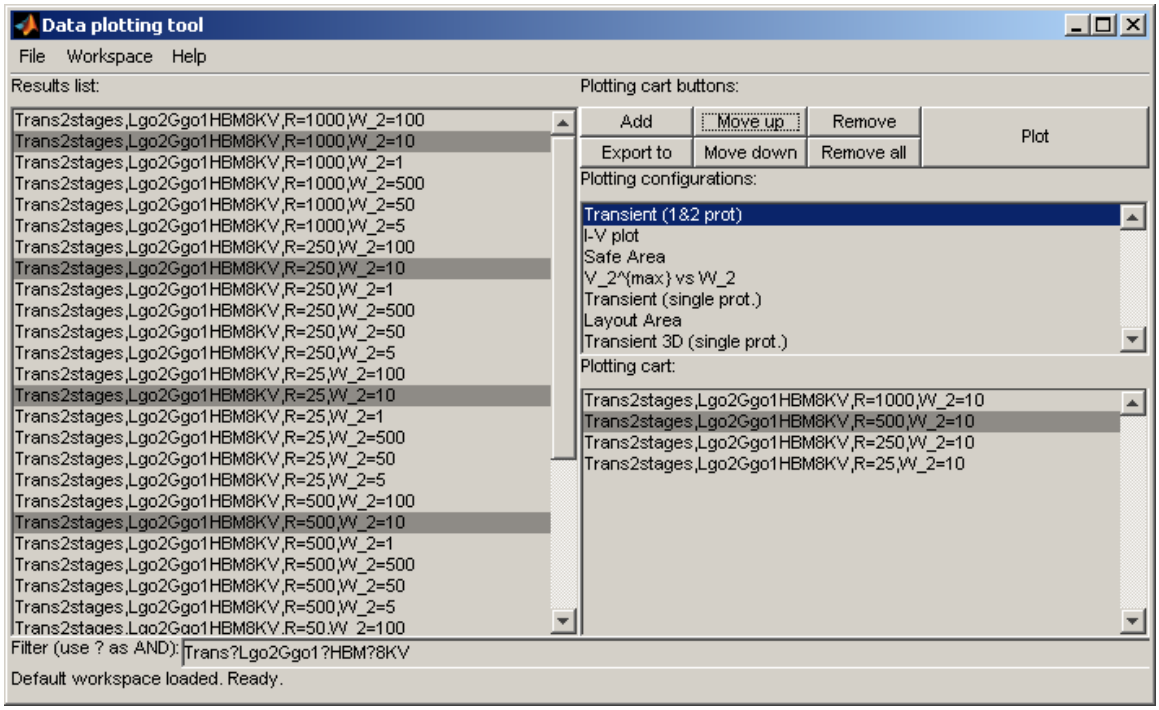


Figure 50. Snapshot of the Graphical User Interface (GUI).

```
1  Trans2stages,Lgo2Ggo1HBM3KV,R=1000,W_2=100
2  Lgo2Ggo1HBM3KV,R=1000,W_2=100
3  6
4  29
5  1.000000e-12    5.882944e-02    2.140916e-03    8.450284e-04    4.108384e-05
6  2.000000e-12    1.499583e-01    4.248416e-03    2.771592e-03    1.086554e-04
7  4.000000e-12    4.169622e-01    8.377212e-03    1.175057e-02    3.154218e-04
```

Figure 51. Example of data file. The data is structured in columns and

2.2.3 Results

Circuit 1: LVTSCR + GGNMOST

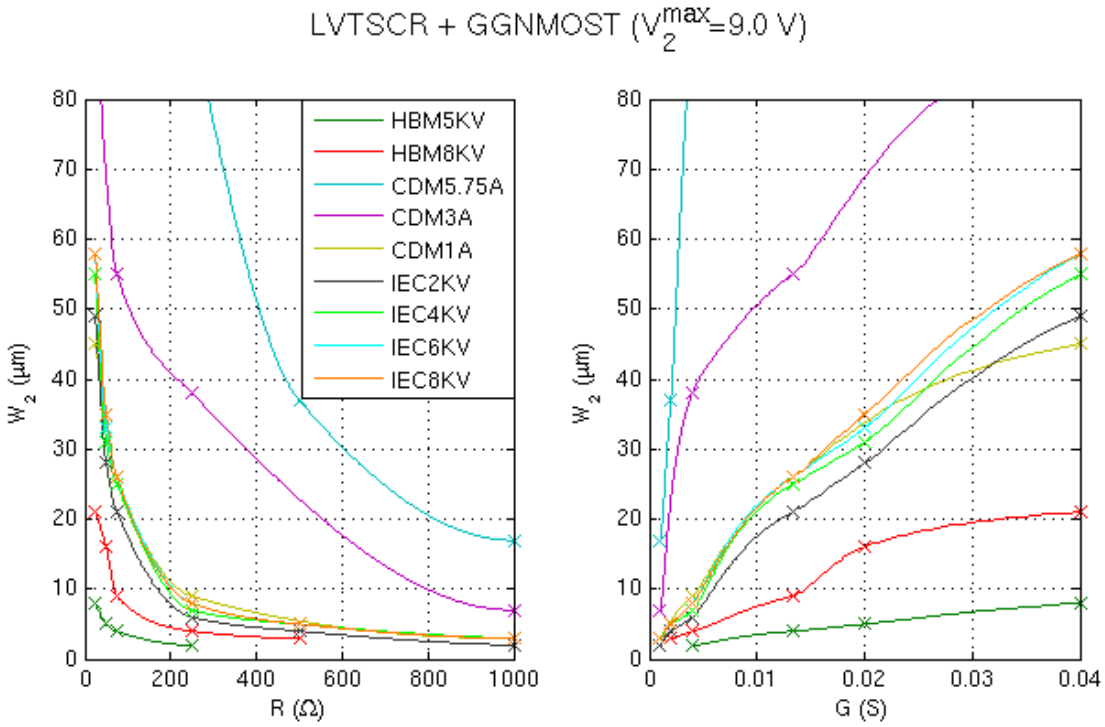


Figure 52. W_2 -R and W_2 -G curves for LVTSCR + GGNMOST circuit at V2max=9V (GO1).

The results for an LVTSCR as primary protection and a GGNMOST for secondary protection active device are shown in Figure 52. The safe design area curve for a particular ESD stress corresponds to the pair values of $W_2 - R$ that ensure the voltage at the gate oxide to protect is always below a certain voltage level (in this case, 9V).

It is noticed that, using a LVTSCR as primary protection, $V_{2_{max}}$ is found at the beginning of the transient in all cases as a result of a voltage overshoot. Then, the voltage decreases despite the fact that the current is still rising. Examples of this behavior are shown in Figure 53 and Figure 54.

This voltage overshoot is due to the slow turn on time of the LVTSCR. As explained at section 1.4, the LVTSCR requires time for turning on. Meanwhile the charge is accumulated at the anode and therefore the voltage increases. Once the device is on the anode voltage decreases slowly.

A consequence of the overshoot phenomenon is that most important aspect when designing an effective LVTSCR+GGNMOST circuit is the dI_{dens}/dt in the primary protection. Fast calculations give:

CDM 5.75A: $\frac{5.75A/80\mu m}{400\,ps}$ =1.8E-04 $\frac{A}{\mu mps}$

HBM 8KV: $\frac{5.33A/150\mu m}{2ns}$ =1.78E-05 $\frac{A}{\mu mps}$

IEC 8KV: $\frac{30A/2000\mu m}{0.7ns}$ =2.14E-05 $\frac{A}{\mu mps}$

The highest dI_{dens}/dt corresponds to CDM 5.75A, which agrees with the explanation in section 1.4 and the results in Figure 52.

It is also shown that for combinations of R-W_2 that sink more current (those with low values of R and high W_2 values) the voltage overshoot is lower. This happens because the overshoot takes place after few tens or hundreds of picoseconds, when the ESD current is still relatively low. For these R-W_2 combinations the current through the secondary protection is not negligible in comparison with the current through the primary protection. This also explains why, despite the fact the primary protection is equally sized in system level 4KV, 6KV and 8KV, the curves are slightly different. As the IEC current through the primary protection is higher, the bending is lower (curve more linear).

It is also important to notice that the maximum current density of the GGNMOST is reached for certain R-W_2 combinations. This must be taken into account when designing the secondary protection.

For W_2=500 μm the GGNMOST stays near the edge of the trigger point since there a balance between voltage and current occurs: When I_2 increases, the V_2 decreases as a result of the voltage drop in the resistance. This makes the GGNMOST to sink less current. The trigger point is thus never reached.

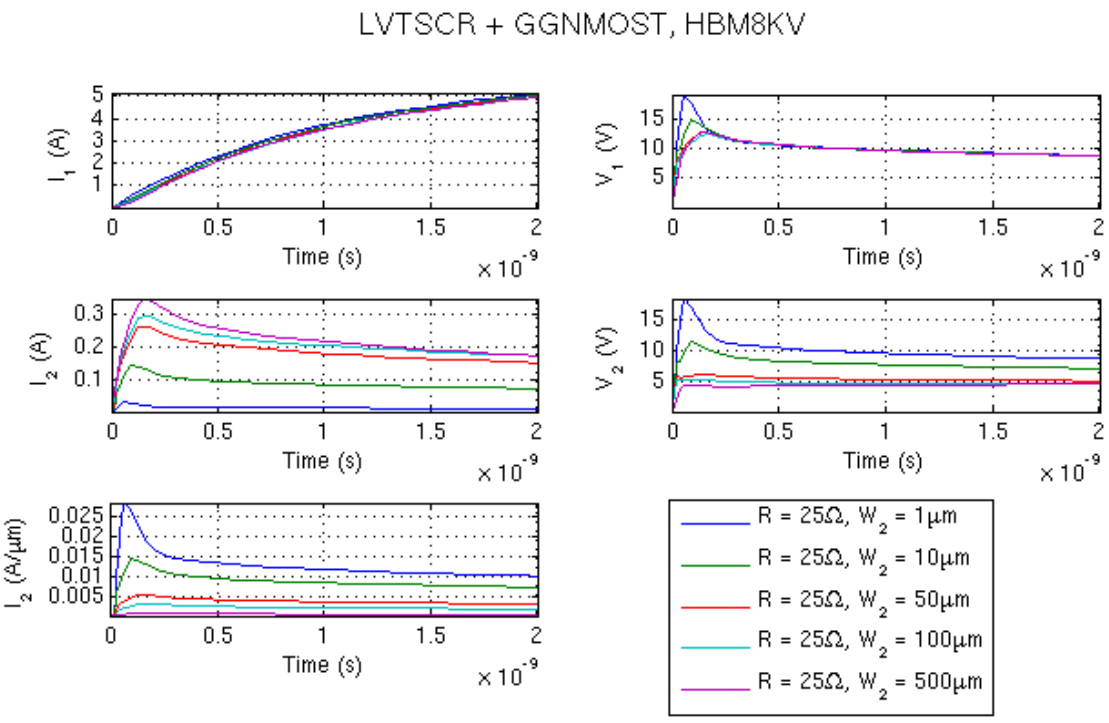


Figure 53. Transient analysis for LVTSCR+GGNMOST circuit protecting against HBM 8KV. Only results for R=25 Ω are shown to describe overshoot performance.

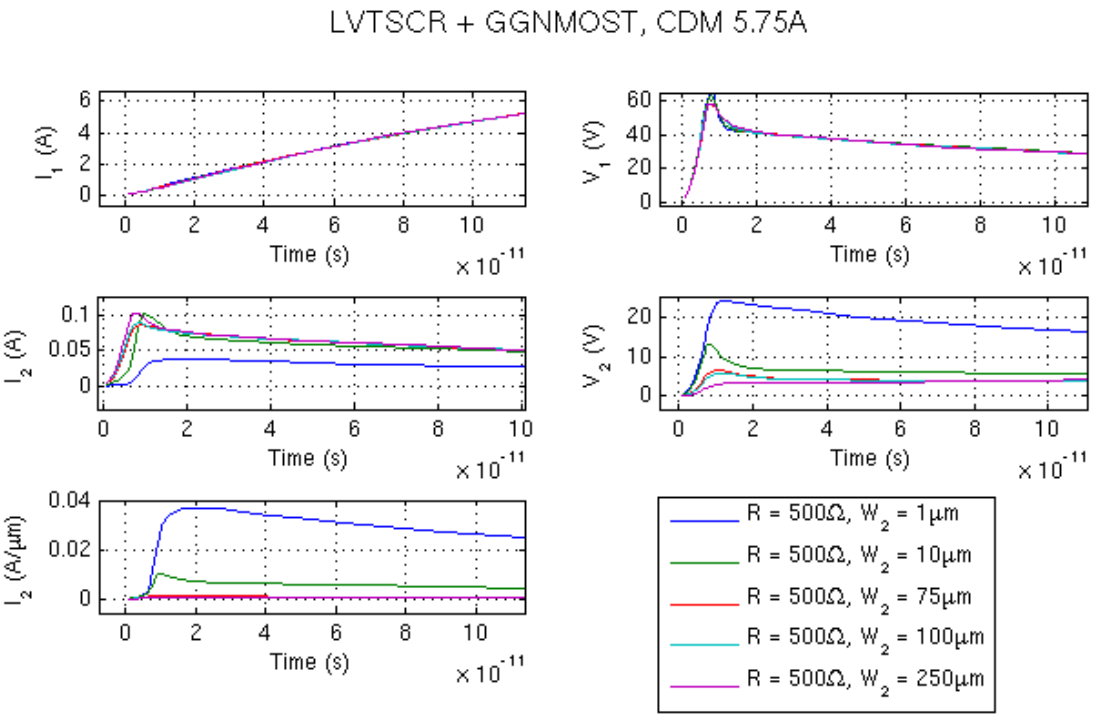


Figure 54. Transient analysis for LVTSCR+GGNMOST circuit protecting against CDM 5.75A. Only results for R=500 Ω are shown.

Circuit 2: GGNMOST + GGNMOST

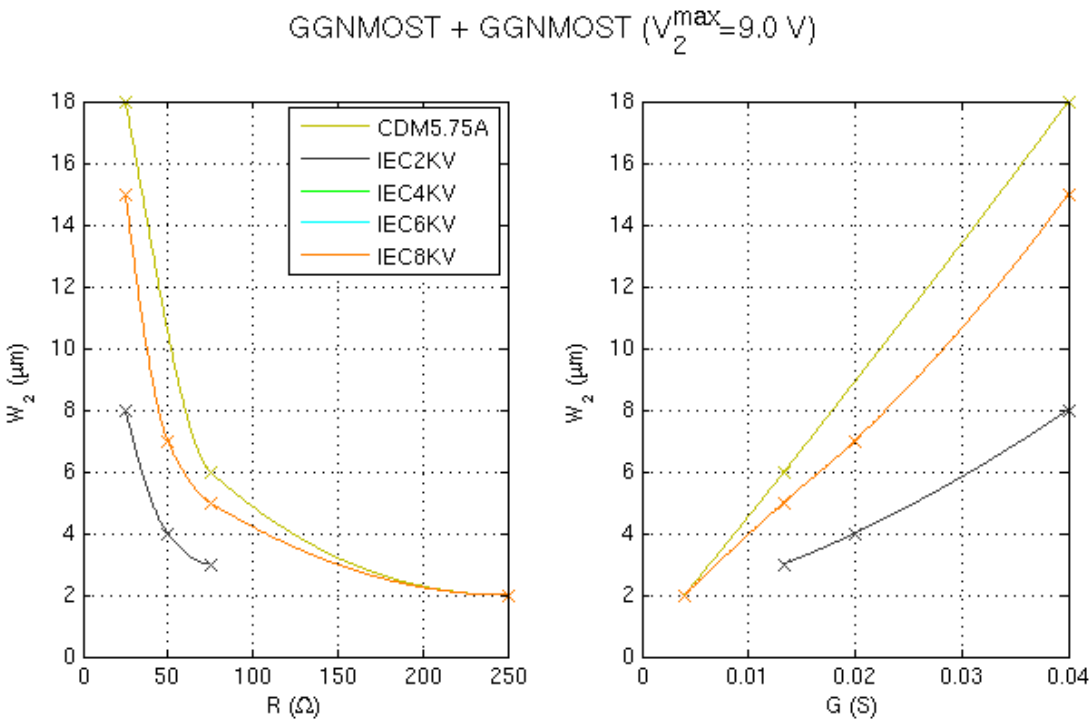


Figure 55. W_2 -R and W_2 -G curves for GGNMOST + GGNMOST circuit V2max=9V (GO1). Notice that IEC2KV, IEC4KV, IEC6KV and IEC8KV are overlapped.

The results for GGNMOST both as primary and secondary protection are depicted in Figure 55. In this case, only system-level stresses and the most demanding CDM stress cause V_2 to rise above 9V.

Together the high width of the primary GGNMOST due to robustness requirements and the high turn-on speed of the GGNMOST make this protection to have the best results in terms of effectiveness. The drawback, however, is that it requires more layout area.

It is found in Figure 55 that the W_2-G curves are very linear, especially when compared with the previous case for LVTSCR as primary protection (see Figure 52). This is because the primary protection GGNMOST sinks most of the ESD

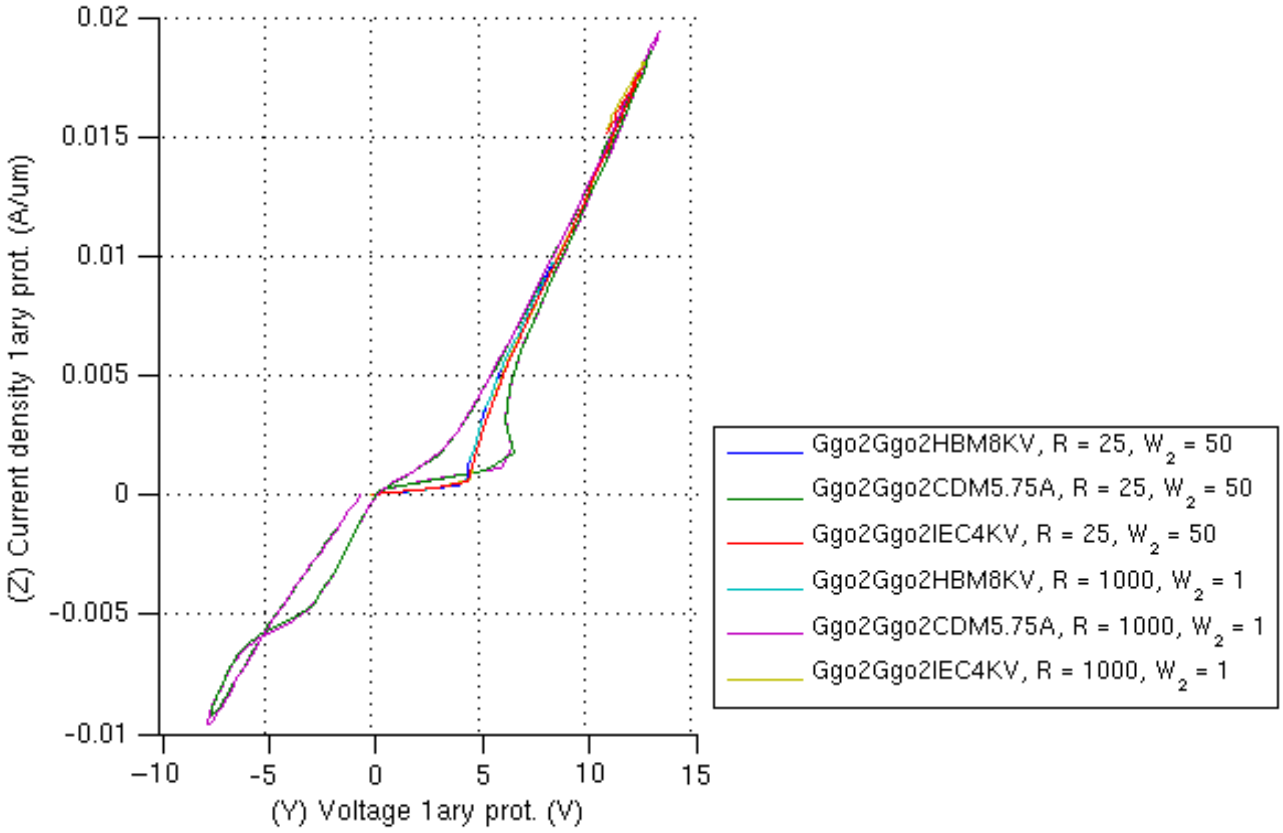


Figure 56. Plot intended to show that when using a GGNMOST as a primary protection, transients tend to the quasi-static TLP I-V curve for all combinations. Negative voltages and currents (CDM case) must be ignored since only the protection for positive ESD stresses was implemented.

current in all cases and it is not affected by the secondary protection parameter values.

Furthermore, Figure 56 shows that when using a GGNMOST as a primary protection, transients tend to the quasi-static TLP I-V curve for all combinations of the rest of the parameters. This is due to the fast response of the GGNMOST, which is the fastest device in this study.

Circuit 3: Non-boosted rail based circuit

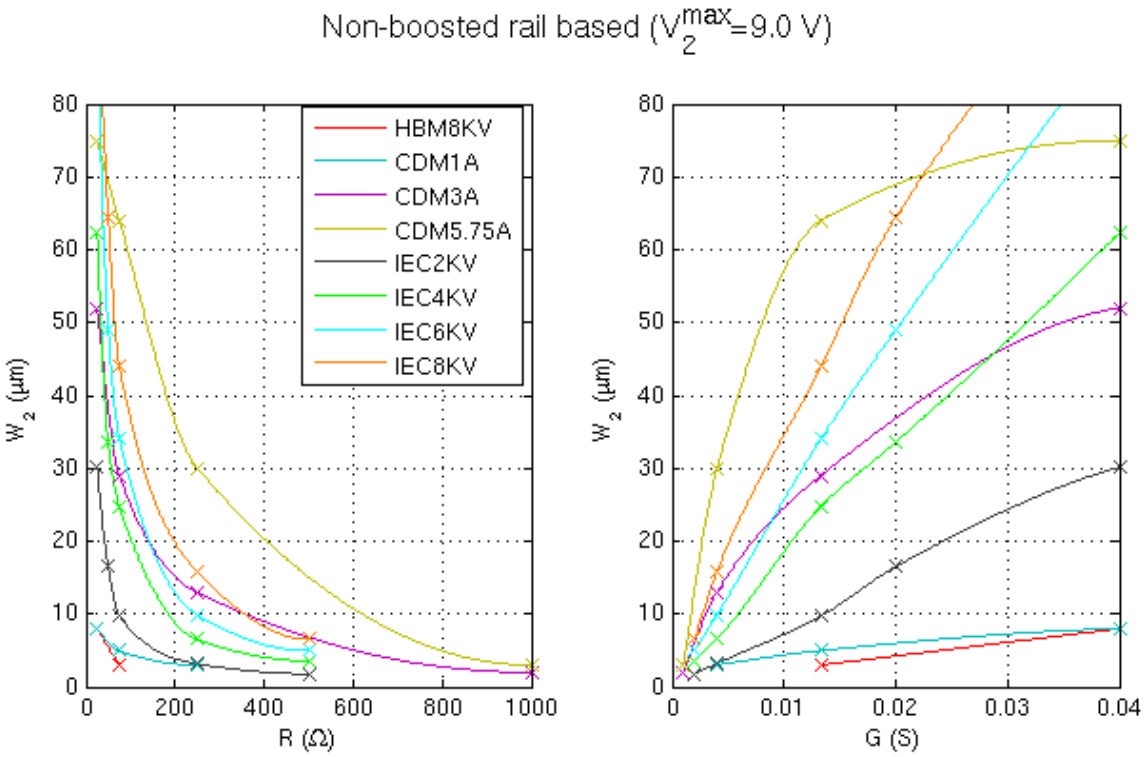


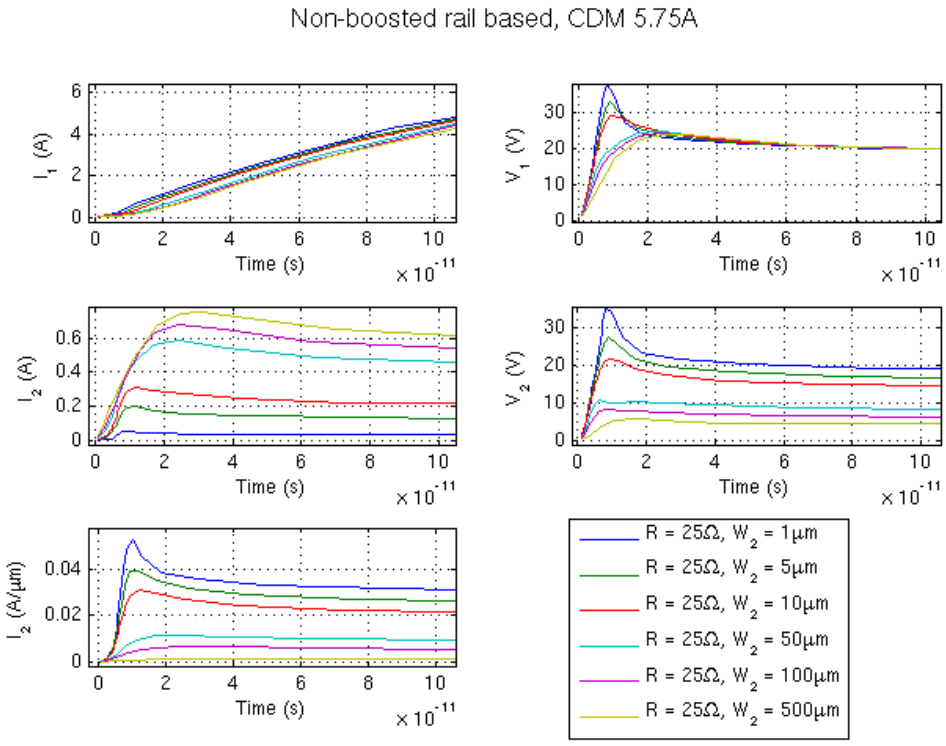
Figure 57. W_2-R and W_2-G curves for non-boosted rail based circuit V2max=9V (GO1)

Figure 57 shows the W_2-R and W_2-G plots for the non-boosted rail based circuit at GO1 breakdown voltage. The protection circuit protects the gate oxide below 9V for any combination of W_2-R for HBM 3KV and 5KV. The W_2-G curves behave in a linear fashion for IEC and HBM stresses. However, a bending is observed at low R values (25Ω = 0.04S) only for CDM.

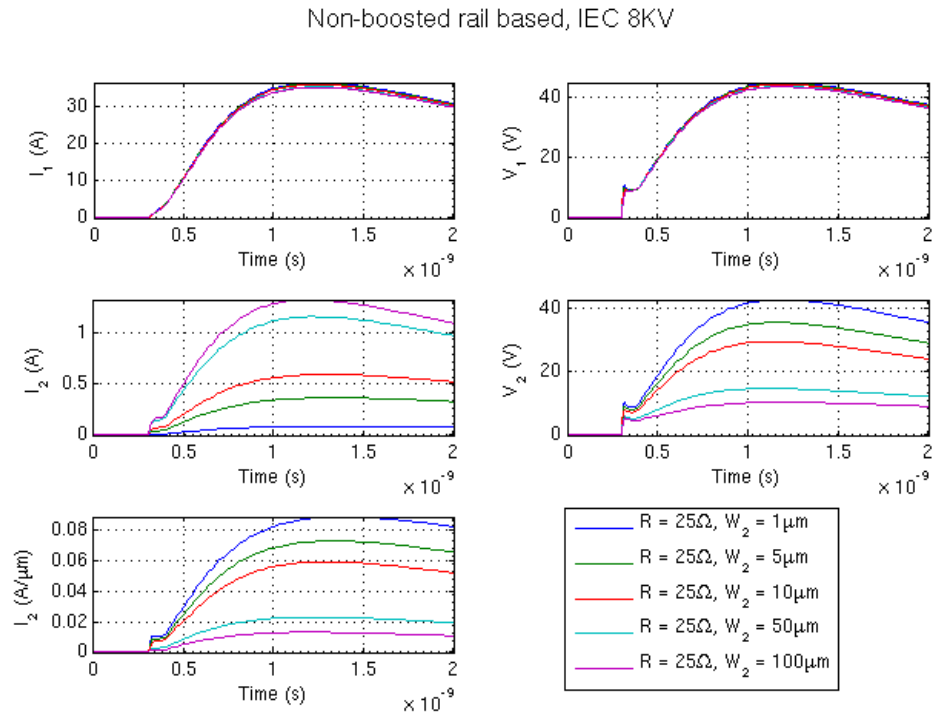
Figure 58(a) depicts a simulated transient until 100ps in order to investigate the reason of this bending. Although not shown, I_2 and both V_1 and V_2 continuously decrease down to zero until the first negative half cycle of the CDM waveform is reached. Notice that this happens despite the fact that the ESD current is still increasing.

In Figure 58, it can be appreciated how the non-boosted primary protection produces a voltage overshoot both for CDM 5.75A and IEC 8KV stresses. V_1 can reach about 40V for the worse W_2-R combination for CDM 5.75. Figure 58(b) shows that a smaller overshoot (V_1 gets up to 8.8V) is produced for IEC 8KV. It is concluded that the main factor for the overshoot is again the value dI_{dens}/dt at the primary protection. The higher this value, the higher voltage the overshoot.

As in previous cases, the reason non-linearity of the W_2-G lies in the fact that $I_{2_{\max}}$ is not negligible in comparison with $I_1(t_1^{crit})$. $I_1(t_1^{crit})$ is lower than in the linear cases since it occurs at the beginning of the transient, when the ESD current is starting to raise. In this case, $I_1(t^{crit})$ is around 1.5 A (t^{crit}=250ps, see Figure 58(a)) whereas $I_2(t^{crit})$ for V_2=9V is near 0.6A. Since both currents are comparable, a significant voltage drop (20V maximum) is produced.



(a)



(b)

Figure 58. CDM 5.75A (a) and IEC 8KV (b) transient analyses for non-boosted rail based circuit. Only results for R=25 Ω are shown to describe overshoot performance.

Circuit 4: Boosted rail based circuit

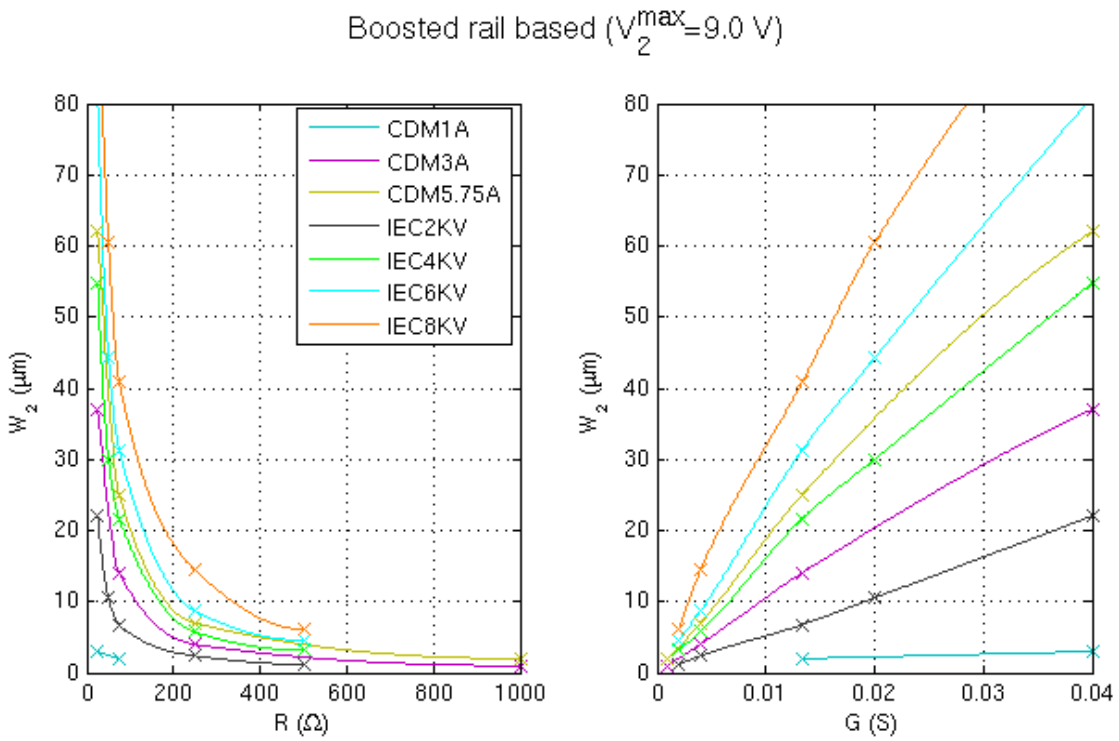


Figure 59. W_2-R and W_2-G curves for boosted rail based circuit V2max=9V (GO1)

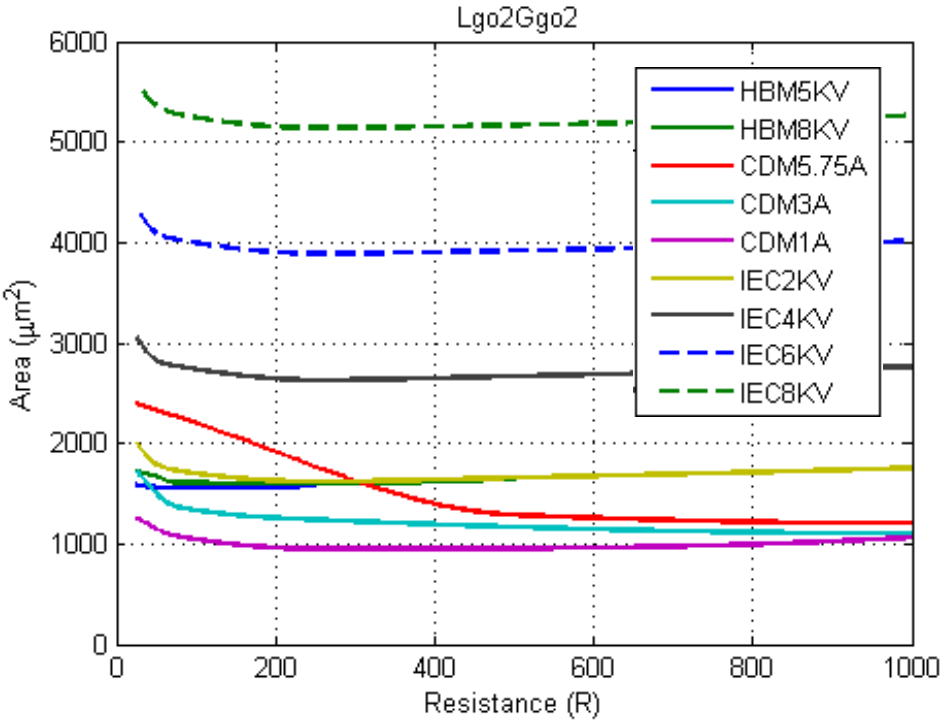
W_2-R and W_2-G curves for boosted rail based circuit are depicted in Figure 59. HBM 3KV, 5KV and 8KV are not shown since the maximum V_2 was below the GO1 breakdown voltage.

It is found that the curves are very linear for any W_2-G combination.

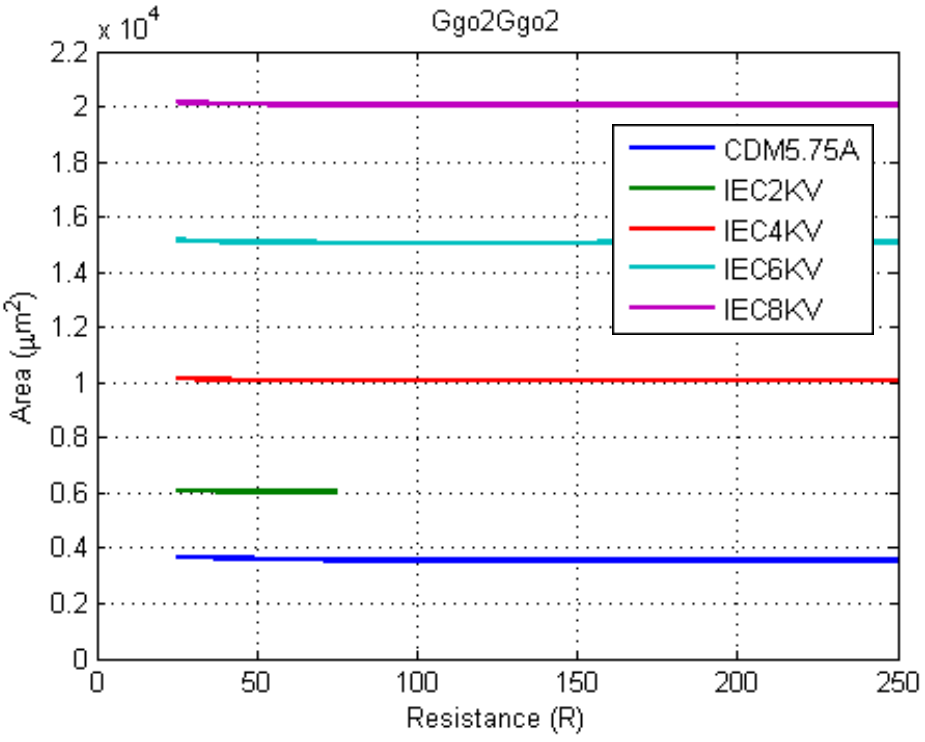
Layout area estimation

One obtained the safe design area plots, a layout area estimation using the secondary protection parameter values on the safe area boundaries was performed. For LVTSCR and GGNMOST devices, the area was calculated by multiplying the cross section length by the device width. In resistors, the calculation was done taking into consideration the unsilicided n+ polysilicon resistor sheet resistance [C14DRM] and the minimum poly resistor width for robustness (5 μm)[C14ESD]. This calculation was carried out only for pad based circuits (that is, circuits 1 and 2) because rail based circuits share clamps with a number of I/O cells, depending on several criteria, and therefore a direct comparison between both architectures would not be coherent.

Figure 60 shows the layout area estimation for circuit 2 and circuit 3 with GO2 secondary protection GGNMOST. As expected, using GGNMOST as a primary protection instead of a LVTSCR consumes more area due to its lower robustness. Also, most of the area is used by the primary GGNMOST and variations on the secondary protection are negligible. On the other hand, it is observed that, using a LVTSCR as a primary protection, a minimum area can be achieved for certain values of the secondary protection parameters.



(a)



(b)

Figure 60. Layout area estimation for Lgo2Ggo2 (a) and Ggo2Ggo2 (b) circuits.

2.2.4 Conclusions

The following conclusions can be reached by analyzing the simulation results:

- From the point of view of the ESD effectiveness, there are two scenarios:
  a) $V_2^{\max}$ is determined by a voltage overshoot, which occurs before the ESD current reaches its maximum value. This voltage depends on the primary protection turn-on speed characteristics and I_{dens}/dt.
  b) $V_2^{\max}$ is determined by the maximum ESD current which in turn determines $V_1^{\max}$. The circuit behaves in a quasi-static fashion which yields in simpler design calculations.

A simplified approach for secondary protection design is now exposed for case b.

As it has been demonstrated in this section, for case b the current flowing through the primary protection can be considered much higher than the current flowing through the secondary protection ($I_{1_{\max}} >> I_{2_{\max}}$). Hence, V_1 can be expressed as follows:

$$V_1 = RI_2 + V_2 = R\left(W_2 I_{2_{\max}}^{dens}\right) + V_{2_{\max}} = V_{1_{\max}} = V_1(t^{crit}) \quad \text{Eq. 2.8}$$

where $V_{1_{\max}}$ is the maximum voltage at the primary protection during the ESD stress transient, $V_{2_{\max}}$ is the wanted maximum voltage at the anode of the secondary protection and $I_{2_{\max}}^{dens}$ the corresponding current density to $V_{2_{\max}}$ according the device quasi-static (TLP) I-V curve. It has been also assumed that the current is uniform along the device width. It is thus concluded that:

$$\frac{V_{1_{\max}} - V_{2_{\max}}}{I_{2_{\max}}^{dens}} = RW_2 = const \qquad \text{Eq. 2.9}$$

RW_2 equals a constant which determines the voltage division given the design parameters $V_{1_{\max}}$, $V_{2_{\max}}$ and $I_{2_{\max}}^{dens}$. These parameters are in turn determined by the primary protection, the ESD model and stress level.

It has been demonstrated that this straightforward approach can be used as a rule of thumb when designing a two-stage ESD protection. Nevertheless, there are scenarios when the condition $I_{1_{\max}} >> I_{2_{\max}}$ cannot be applied without taken a too high approximation error (case a). This occurs when t^{crit} is at beginning of the ESD event (typically first hundreds of picoseconds) and therefore $I_{1_{\max}}$ has not reached the maximum value yet. In these cases, $I_{1_{\max}}$ is in the order of $I_{2_{\max}}$ and V_1 drops noticeably, depending on the secondary protection parameters R and W_2.

In this study, the effectiveness of the protection circuit has been the only design criterion. Other secondary criteria, such as matching or noise requirements, could be required in an ESD protection design. This secondary protection analysis provides the ESD designer with safe design areas and guidelines that serve as a starting point for effective two-stage protection circuit design.

3 ESD protection transparency study

This chapter will focus on two ESD protection transparency issues: leakage current during normal operation and capacitive load matching for broadband applications.

3.1 Leakage current

3.1.1 Introduction

During the course of this internship, urgent TCAD simulations were required by a department to analyze a leakage problem found in a product. More specifically, a GO2 LVTSCR of 150 μm wide in a 0.14 μm CMOS process, similar to the one studied in section 2.1.2, presented a too high leakage current when exposed to a voltage relatively far from the trigger voltage, in this case around 8V. The cross section and TCAD DC simulations of the device are shown in Figure 62 and Figure 63, respectively. In the working voltage range, which was below 5V, such a LVTSCR usually presents a leakage current as low as a few nanoamps, which agrees with Figure 63. In this product, however, the current was several orders of magnitude higher.

In order to understand the reasons of this problem and fix it, the following experiment was performed. A sinusoidal voltage at approximately 800MHz with a certain DC offset was applied to the device and DC leak current was measured, as it is depicted in Figure 61. The amplitude and DC offset was swept along a range of values. TCAD simulations were realized to compare them with the measurements. An analogous methodology was used in TCAD simulations. A transient simulation was performed for several pairs of the values of the sweeping parameters (V_{DC} and V_{amp}). The stop time was chosen so that the current reaches a stable state (beyond initial transient). The voltage sinusoid was applied at the anode and then the current was integrated along an integer number of cycles.

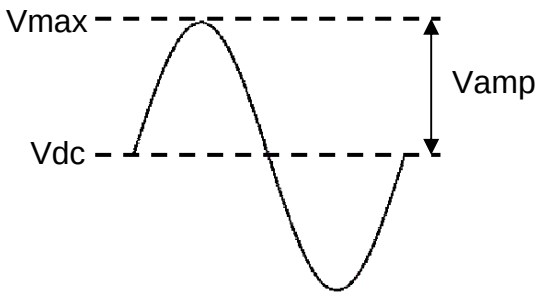


Figure 61. Sinusoid applied to the LVTSCR anode. Vmax = Vamp * sin(2 * pi * frequency * time) + Vdc

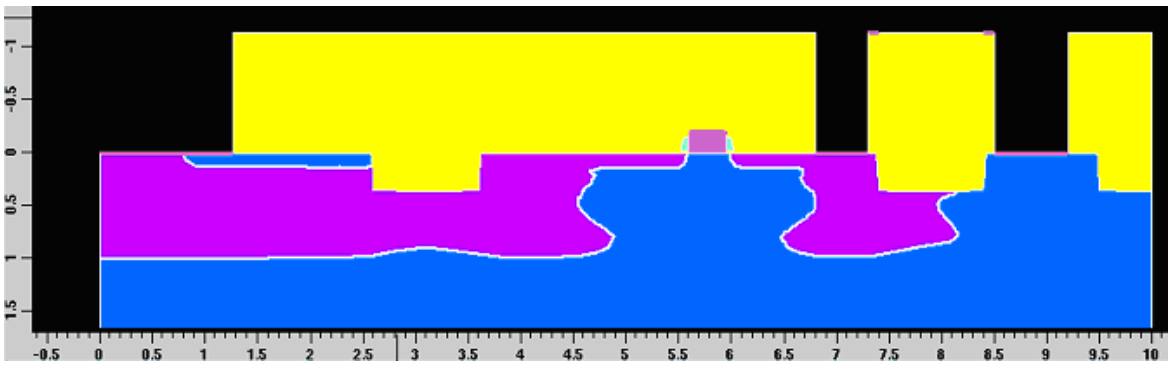


Figure 62. Cross section of the simulated LVTSCR.

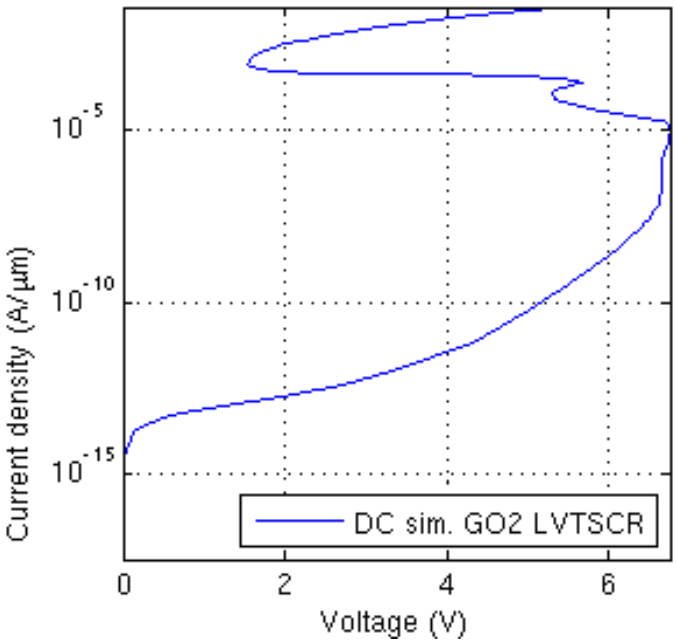


Figure 63. TCAD DC simulations of the device under study.

Figure 64 depicts the measurements (dotted curves) and simulation results (solid curves). It can be observed that simulation results qualitatively agree with measurements. The current through the device increases several orders of magnitude as $V_{\max}$ approaches the trigger voltage and it is much higher than for DC. This cannot be observed in TLP measurements because in TLP the voltage is measured 100ns after the initial overshoot approximately and therefore it can be considered quasi-static. It is also important to notice that the leakage current depends mainly on the amplitude of the sinusoid V_{amp} and in a lesser extent on the offset voltage V_{DC}.

The same experiment was repeated for real waveforms (see Figure 66) at two frequencies with similar results to the sinusoidal case. Figure 67 shows that higher leakage currents were found at higher frequencies. Figure 68 depict I-V plots for two cases near the trigger voltage, one right before the device gets unstable and one after. Figure 65 shows that, for V_{DC} below the trigger circuit, if V_{amp} is high enough, the device gets unstable and it eventually triggers and reach the ohmic (R-on) zone.

Possible factors that may contribute to this phenomenon are the leakage current of the reverse junction, a partial activation of the bipolar/latch-up structure, carriers generated by impact ionization and capacitive coupling between n+/n-well and p-well. In order to discover the reasons of this increase of the leakage current, another type of experiment in TCAD was carried out. A DC simulation at 1V and transient simulations for 1V ramps with rise times of 500ps and 50ns were realized in order to compare the state of the device.

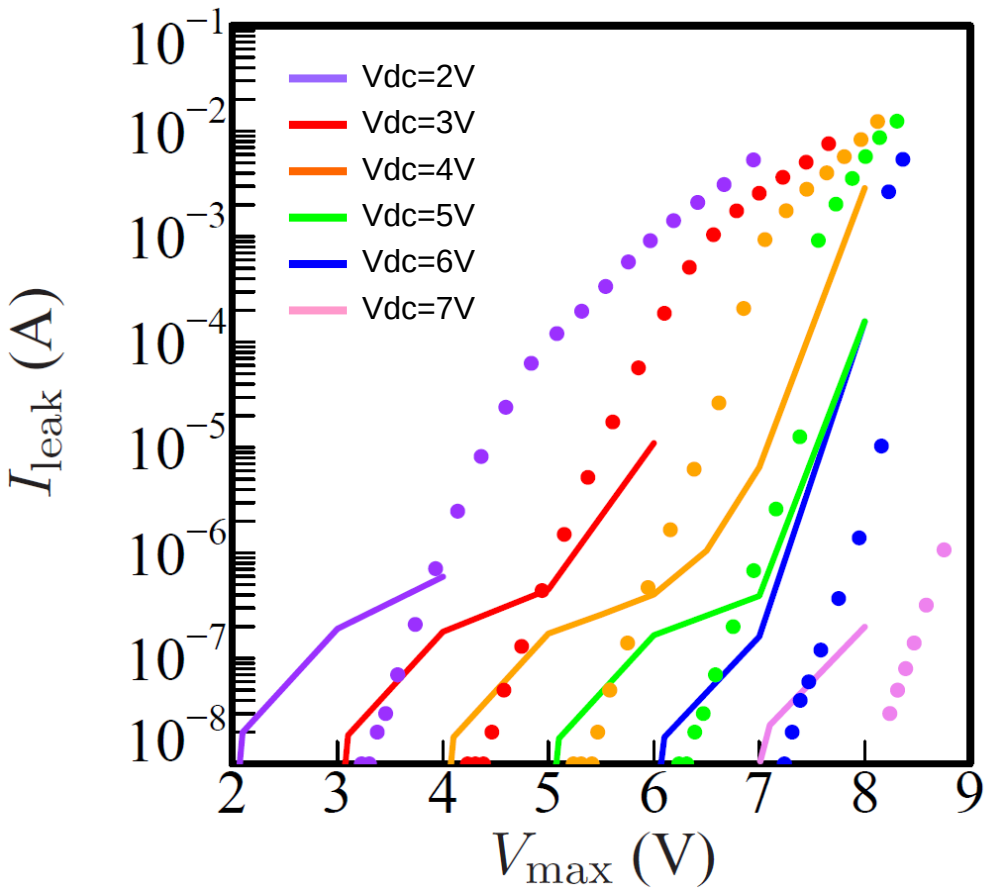


Figure 64. Leakage current results comparison between measurements (dotted curves) and simulations (solid curves). Different colors represent different offset voltage values (Vdc), e.g.: purple=2V, red=3V, and so on.

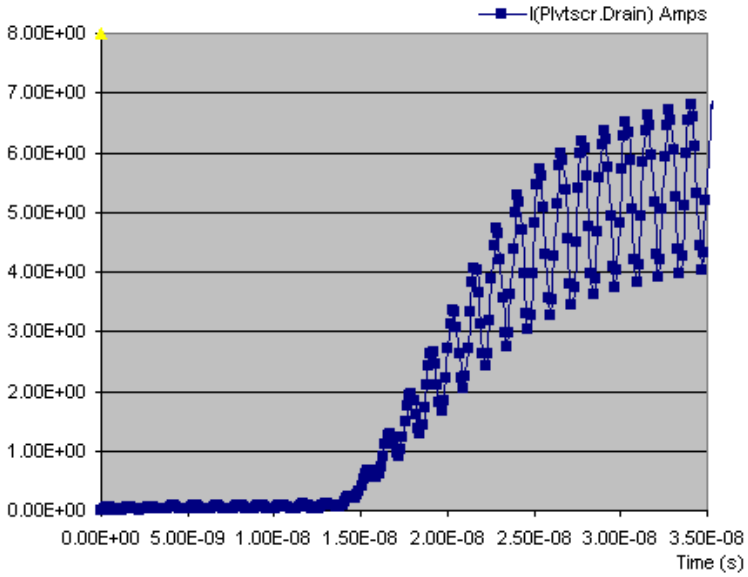


Figure 65. Exponential increase of current

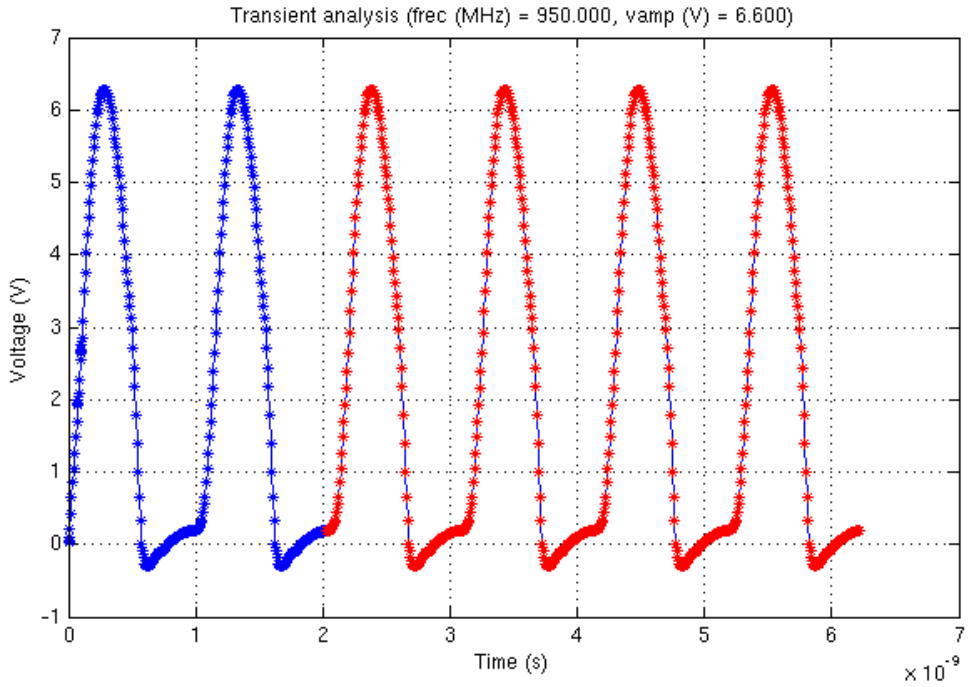


Figure 66. Example of transient simulation for real waveform. The cycles taken for DC leakage integration are in red color.

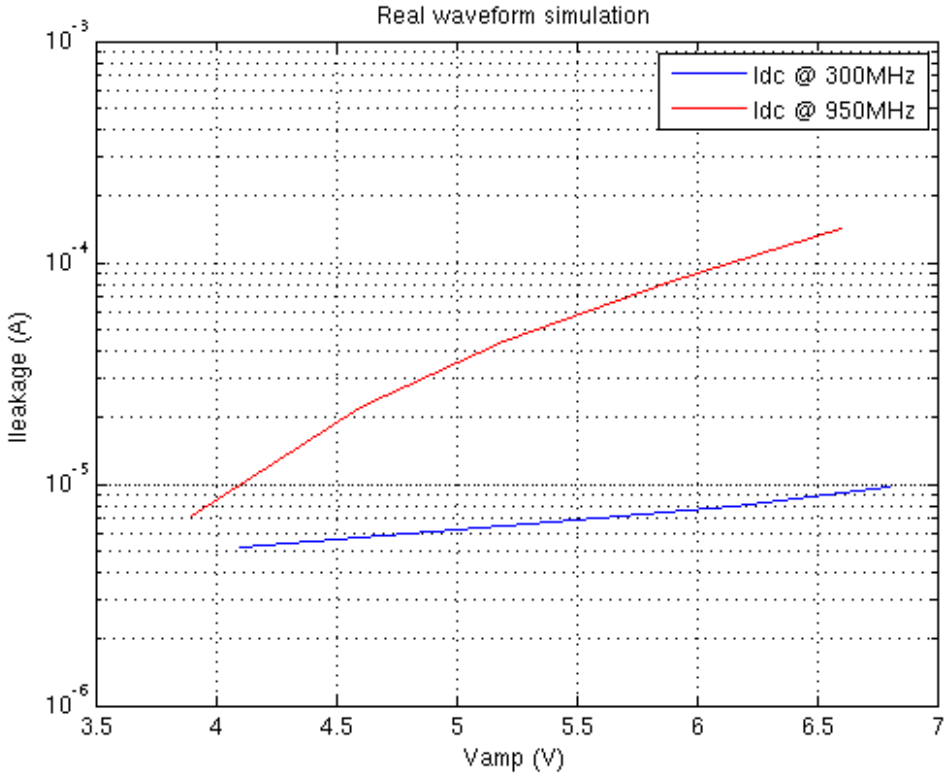
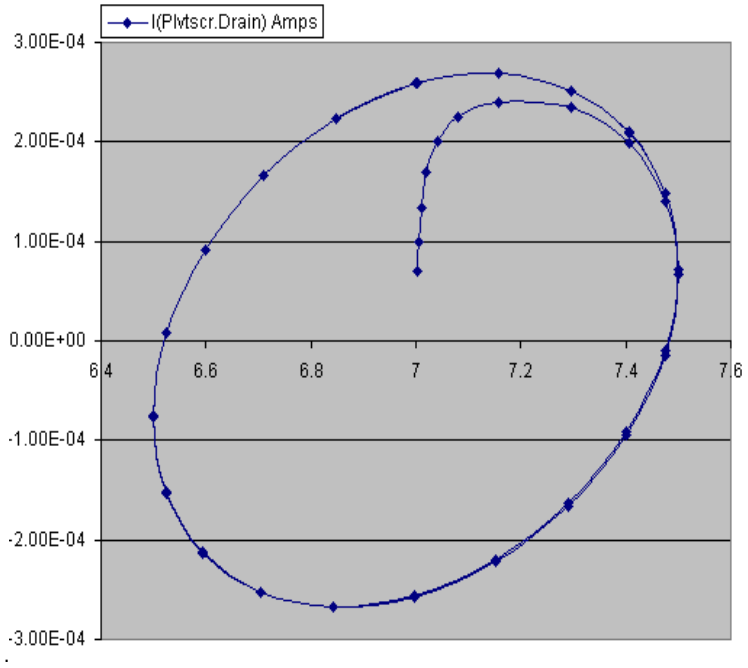
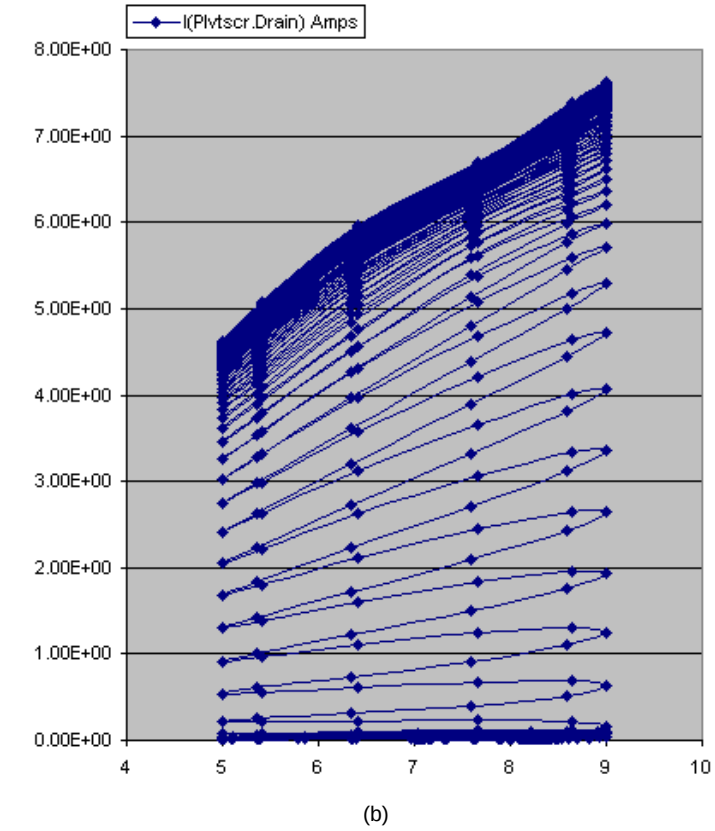


Figure 67. Comparison between leakage current for real waveforms at two different frequencies.



(a)



(b)

Figure 68. I-V plots curves for (a) 7Vdc+0.5Vamp and (b) 7Vdc+2Vamp . Horizontal axis represents voltage (V) and vertical axis represents current (A). In (a), the device behaves as a parasitic capacitor and a resistor that produces some leakage. In (b), the device turns on and after a transient it reaches the ohmic (R-on) region.

Figure 70 shows the current potential at the end of the ramp for both rise times. The space between lines represents 10% of the total current that flows through the structure. It is thus observed that more than 90% of the current flows directly from the anode to the substrate contact in both cases. This shows that neither the parasitic bipolar under the gate nor the latch-up structure are turned on and therefore the current cannot be attributed to a bipolar activation.

Figure 72 shows the impact ionization density, which mainly occurs at the drain/well junction of the NMOS embedded in the LVTSCR. The total current produced by impact ionization was extracted by integrating the impact ionization density along the entire device volume. Also, Figure 71 depicts the displacement current magnitude for both cases at the end of the ramp. The distribution is very similar in both cases and the maximum is two orders of magnitude higher for 500ps than for 50ns rise time.

Table 14 summarizes all the results. It was concluded that, for this particular case, most of the leakage current is due to capacitive coupling. The amount of current due to capacitive coupling was calculated by subtracting the impact ionization current from the total current. In all ramp cases, current due to impact ionization was two orders of magnitude lower than the one generated by capacitive coupling. Leakage current was found negligible for the ramp cases and bipolar activation was also rejected by observing current potential curves.

Figure 69 depicts the lumped element path along which the leakage current flows in the device. The current can be expressed as follows:

$$I_{leakage} = \frac{V}{\left[\left(R_n + R_p\right) - j\frac{1}{2\pi fC}\right]} \qquad \text{Eq. 3.1}$$

where C is the capacitance mainly formed by the n-well,n+/pwell junction and R_n and R_p are the resistance throw the n-well and p-well, respectively. Notice that there is a high pass filter for the current comprised of C, R_n and R_p.

Further simulation experiments to decrease the cut-off frequency of this filter were carried out by removing the n-well at the cathode. This shortened the current path between the n+/pwell to the substrate contact and therefore decreased the Rp resistance. However, no significant improvement was found.

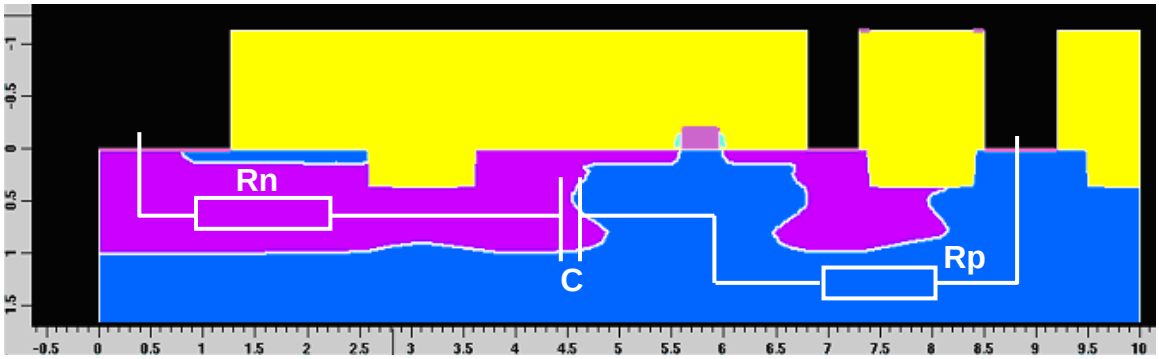


Figure 69. Cross section of the simulated LVTSCR with capacitive coupling circuit.

Table 14. Summary of TCAD simulation results.

	1V DC	1V ramp trise=50ns	1V ramp trise=500ps
Cap.Coupling (A/ μm)	**0**	**3E-08**	**5E-06**
Junc.Leakage (A/ μm)	8E-14	Negligible	Negligible
Impact Ionization (A/ μm)	6E-16	3E-10	5E-08
Total (A/ μm)	**8E-14**	**3E-08**	**5E-06**

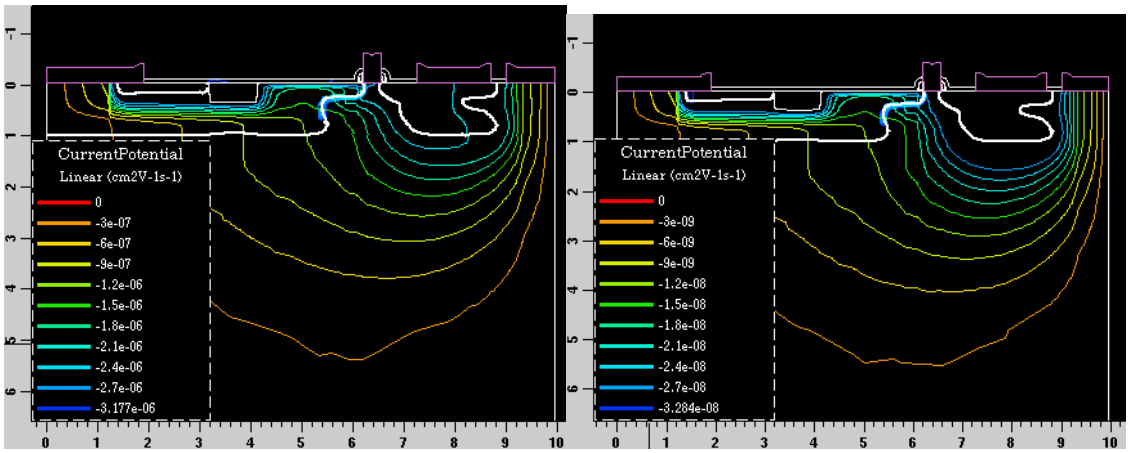


Figure 70. Current potential at 500ps (left side) and 50ns (right side). Space between lines represents 10% of the total amount of current. Figure intended to show qualitatively the current flow.

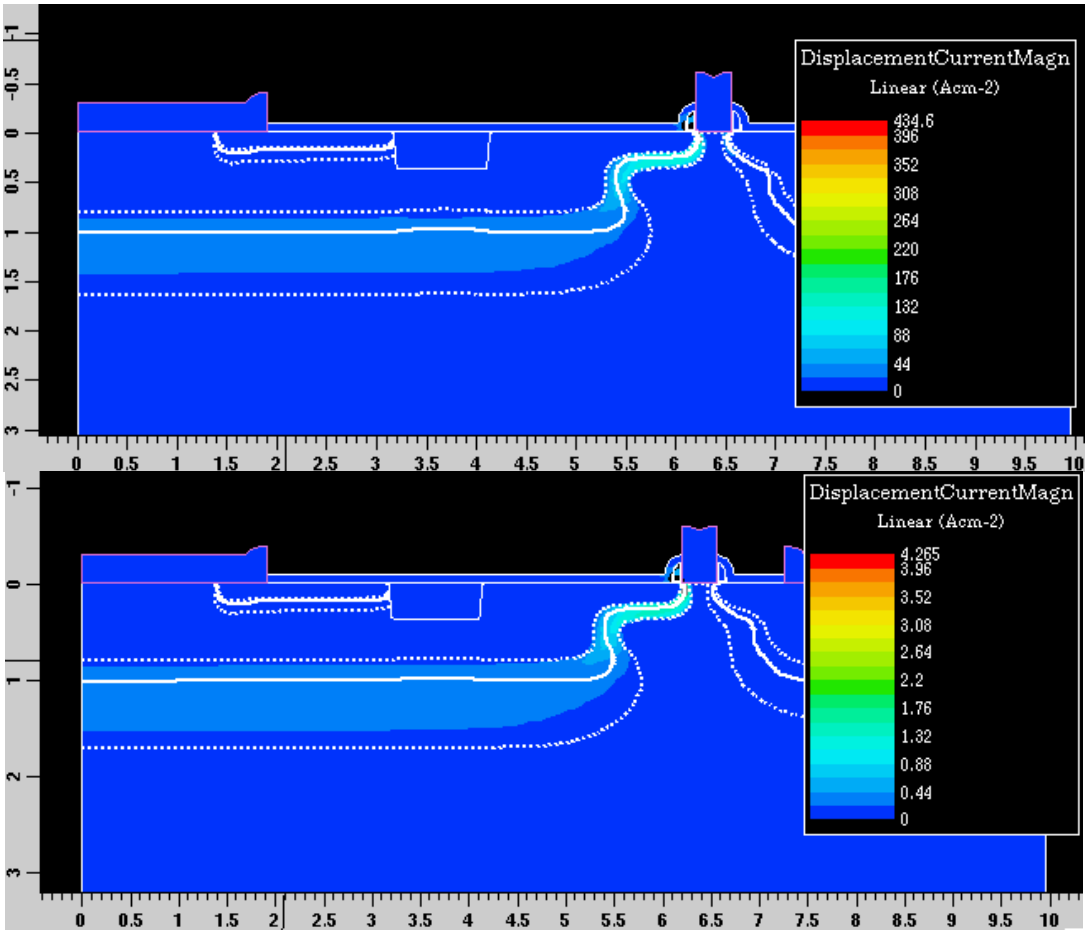


Figure 71. Displacement current magnitude at 500ps (top) and 50ns (bottom).

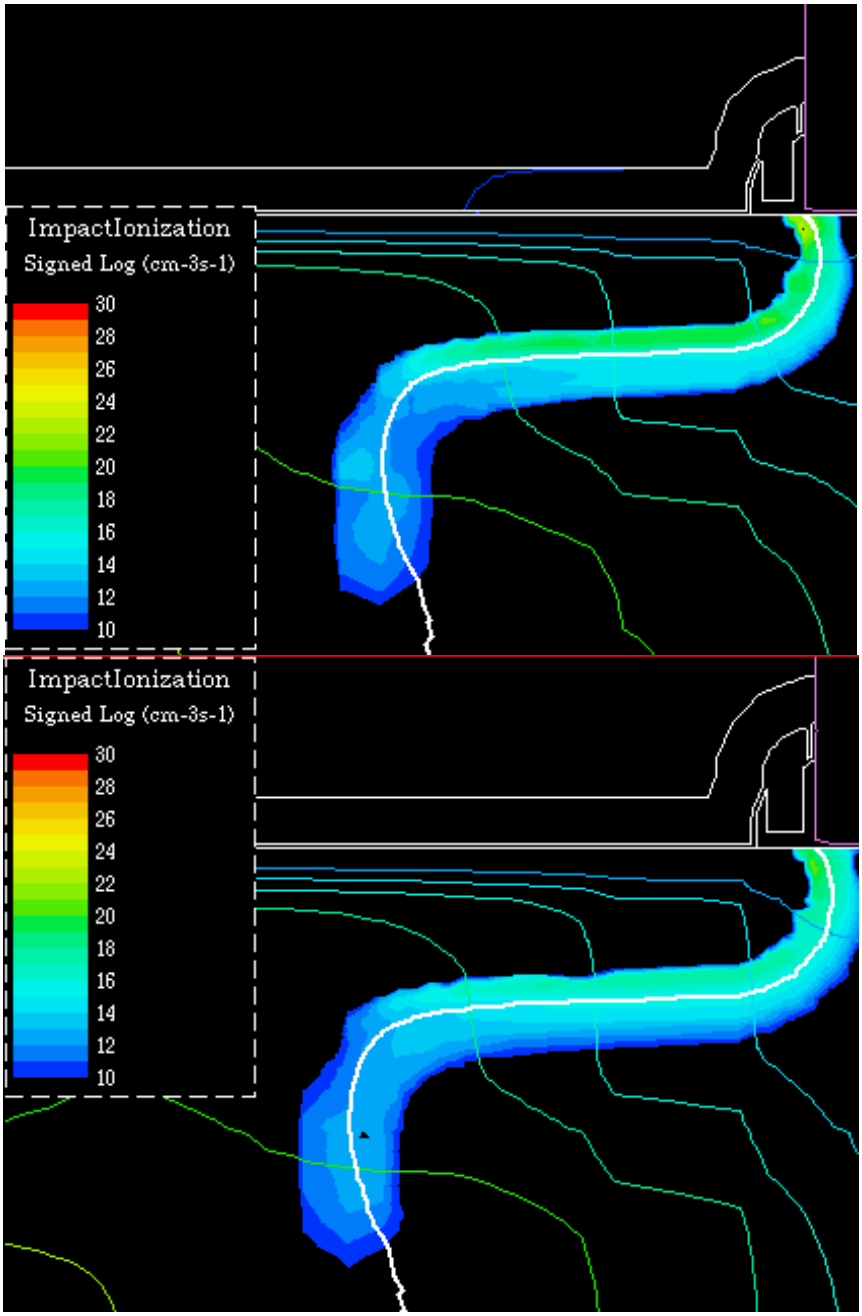


Figure 72. Impact ionization density at 500ps (top) and 50ns (bottom).

3.2 Distributed ESD protection circuit

It is unavoidable to take ESD protection issues into account when designing IC for high-speed applications. Tuning out of ESD protection parasitic capacitance is feasible for narrowband RF applications by resonant cancellation [Voldman04]. For broadband applications, however, this is not possible since ESD bandwidth falls just in the application bandwidth. Figure 73 describes the design criteria typically followed in different frequency bands.

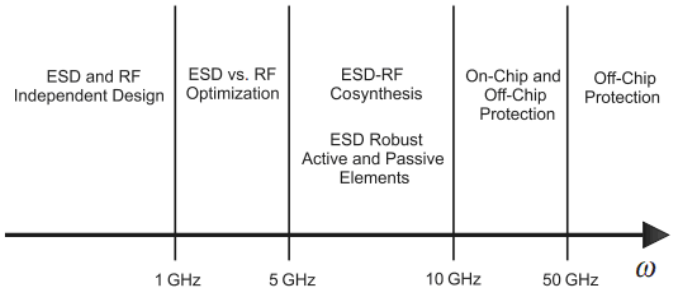


Figure 73. RF ESD design approach as a function of application frequency (figure taken from [Voldman04]).

Distributed networks approach can be applied to ESD protection to improve broadband response **[Ito02][Ker05][Kleveland00]**. This yields in a better impedance matching and improved linearity. The purpose of the distributed approach is hence twofold:

- Decrease the bandwidth limitation due to ESD protection in broadband applications.
- Decrease the distortion due to junction capacitance dependence on voltage when using wide ESD protections.

Figure 74 shows the simplified schematics of the traditional approach and a 4 stage distributed protection. It consists of dividing the parasitic capacitance of the ESD protection in several parts and connecting them by creating a matching

network. Notice that the same approach can be applied for another types of ESD protection devices and structures, not only for rail based protections.

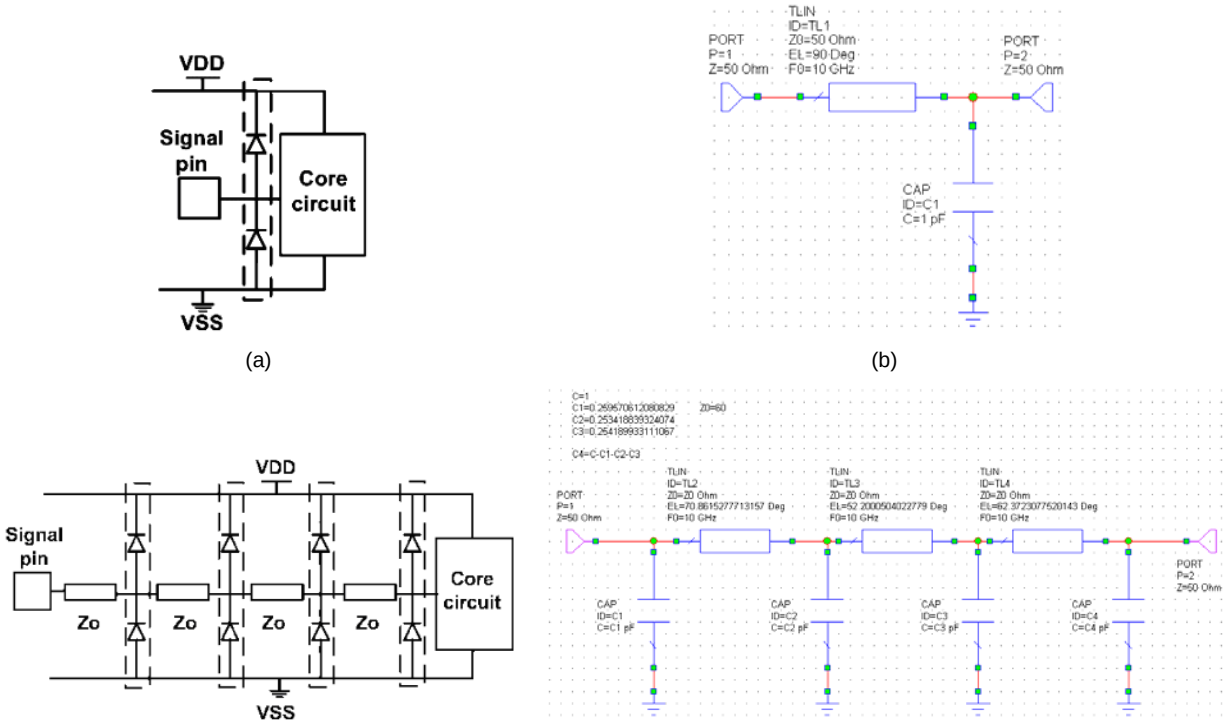


Figure 74. Examples of ESD protection. (a)(b) regular approach (c)(d) 4-staged distributed approach. (Figures (a) and (c) taken from **[Ito02]** and **[Ker05]**).

A common idea in distributed protections is using coplanar waveguides (CPW) to improve the power transfer and matching and to reduce the loading effect on the input nodes [Voldman06]. Also, it was proven in [Kleveland00] that the CPW signal path resistance was low enough to successfully turn on the distributed ESD protection, demonstrating the feasibility of this approach.

3.2.1 Diode characterization

TCAD simulations were performed to extract the parasitic capacitance of an N+/P-well STI diode (Figure 75). Since the model is two-dimensional, the simulations where only useful to check the results with JUNCAP data [C14DRM] and measurements [C16D] and to have an estimation of how much this capacitance can vary with voltage. Figure 76 shows TCAD simulation results. It can be seen that the capacitance can vary up to 10% of its value when sweeping the DC voltage in reverse. There is no dependence on the frequency until f=100GHz. These results were also compared with measurements of the same device in a similar technology in order to check their validity.

A similar diode with a total junction width of approximately 225 μm was measured to have a capacitance of 325fF at -2V [C16D]. According to Figure 76, for a 225 μm wide will have a capacitance of approximately 280fF at –2V. This value fits reasonably well, taking into account that the TCAD model is two-dimensional and therefore lateral capacitances are not considered.

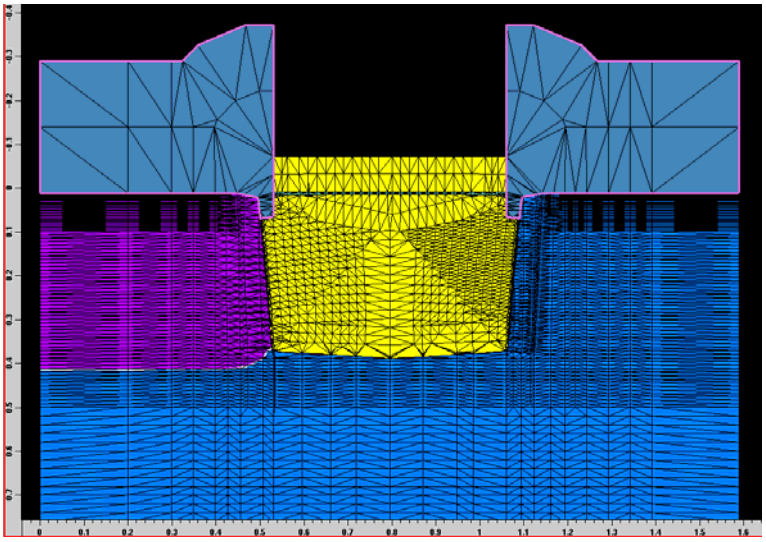


Figure 75. Cross section of the N+/P-well STI diode TCAD model.

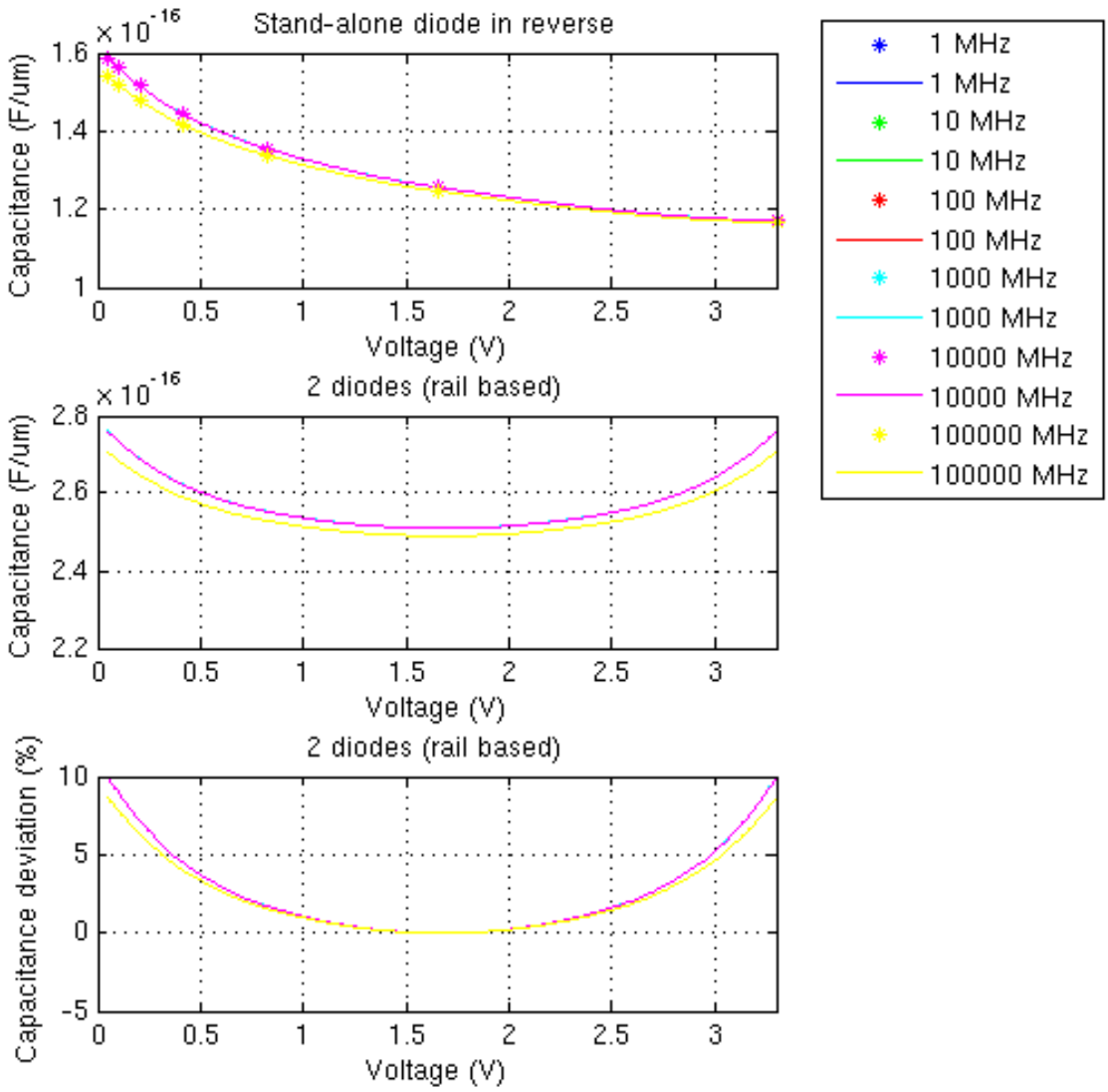


Figure 76. Parasitic capacitance simulation results a diode sweeping the voltage in reverse and frequency (2D model, no 3D effects on capacitance included). For frequencies from 1MHz to 10GHz the curves are overlapped so only 10GHz is visible. A slight decrease of the capacitance is shown at 100GHz.

It was decided to design a distributed ESD protection network with a total capacitance of 1pF, which yields in a total diode width of roughly 675 μm, capable to withstand 4KV system level stress and 8KV Human Body Model stress as it was studied in previous chapters.

3.2.2 Coplanar waveguide design

A proper design methodology requires the whole layout design of the waveguide structure and importing it into an electromagnetic simulator so as to obtain accurate results. However, it was considered that, for study purposes, this was not strictly necessary. Therefore, GDS views of CPW in QUBiC[4] technology were provided as a starting point for a CPW design in a 0.14 μm CMOS process for RF applications using a commercial finite element method solver for 3D electromagnetic structures [HFSS].

The process uses different dielectric materials with different thicknesses between metal layers and for passivation. These dielectric layers were included in the HFSS model for more accurate results. The wave port form electric field excitation was designed according to HFSS guidelines [Ansoft08]. Also, as it is suggested in [Ansoft08], the different calculation methods of characteristic impedance in HFSS were checked for the validity of the results. The wavelength can be directly measured from the electric field 3D view after simulation (see Figure 78).

The choice of appropriate CPW dimensions for distributed ESD protection is a trade-off between broadband RF performance, ESD robustness and layout area. Table 1 reflects RF performance, ESD robustness and layout area dependence on the CPW design parameters. Note that the characteristic impedance depends in turn on the dimensions of the CPW [Voldman06]. It was finally decided to size the CPW with W=10 μm, S=20 μm, G=50 μm as a trade-off (see Figure 77). The signal path is robust enough to withstand system level ESD up to 4KV due to the high last metal layer thickness. Figure 79 and Figure 80 show the characteristic impedance and s-parameters of a designed 1mm long CPW.

[4] QUBiC is a NXP's propietary high performance BiCMOS Si technology.

	RF performance	ESD robustness	Layout area
Higher characteristic impedance	+	x	-
Narrower signal path width (W)	-	-	+
Wider spaces (S)	+	x	-
Shorter CPW	-	-	+

Table 15. List of parameters that affect positively and negatively to the overall performance in terms of RF performance, ESD robustness and layout area. Symbols +, - and x mean improvement, worsening and no dependence, respectively.

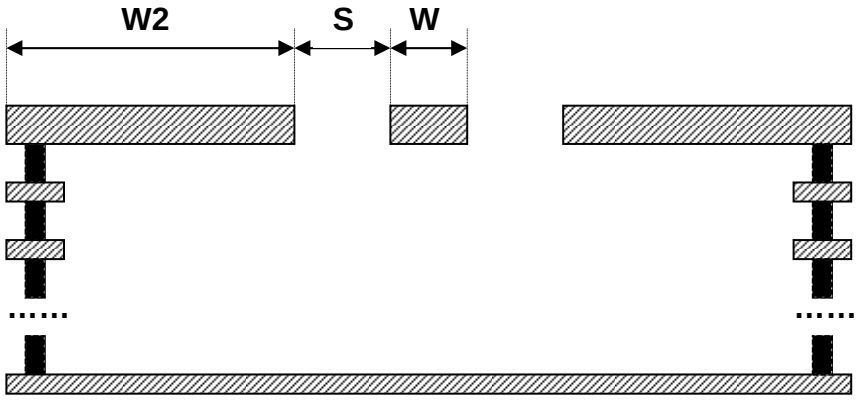


Figure 77. Cross section of a real on-chip implementation of a coplanar waveguide.

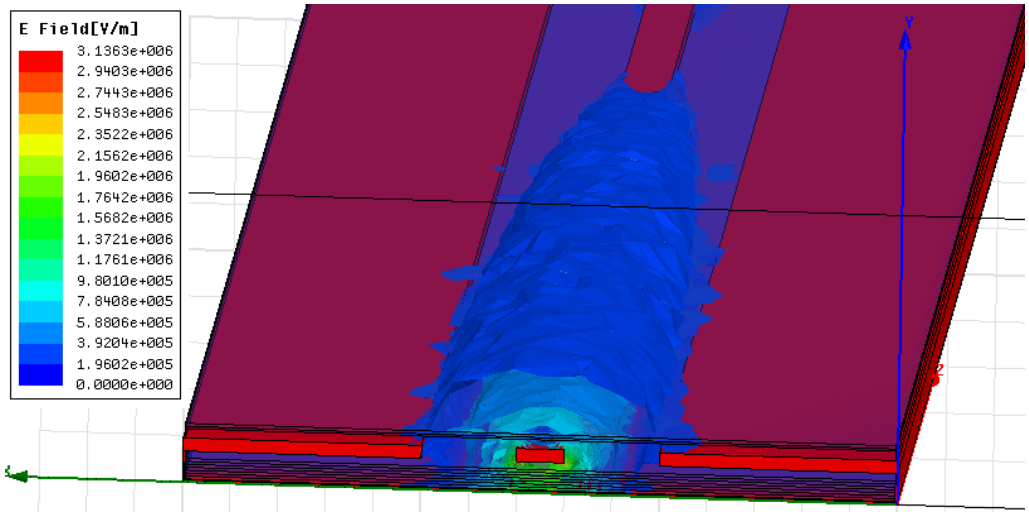


Figure 78. Electric field propagation (for f=100GHz) in CPW

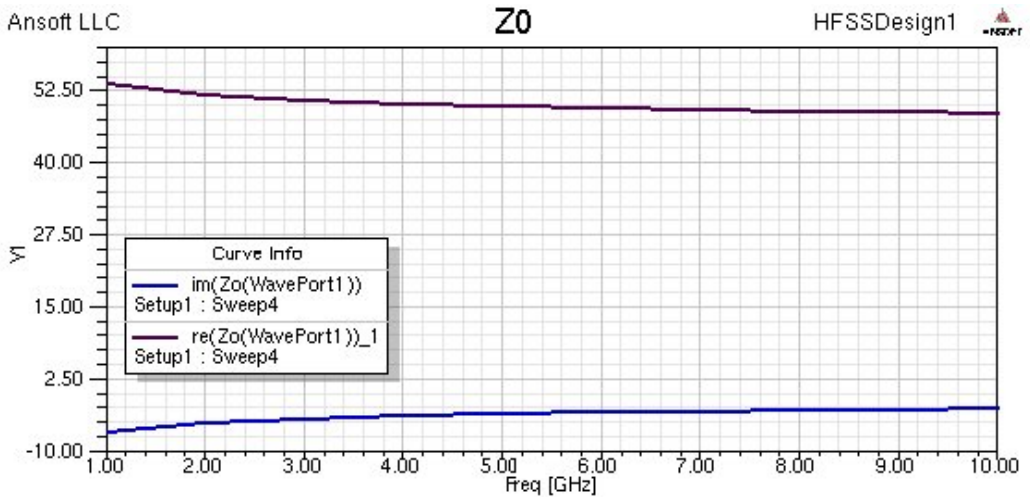


Figure 79. Characteristic impedance of the designed CPW

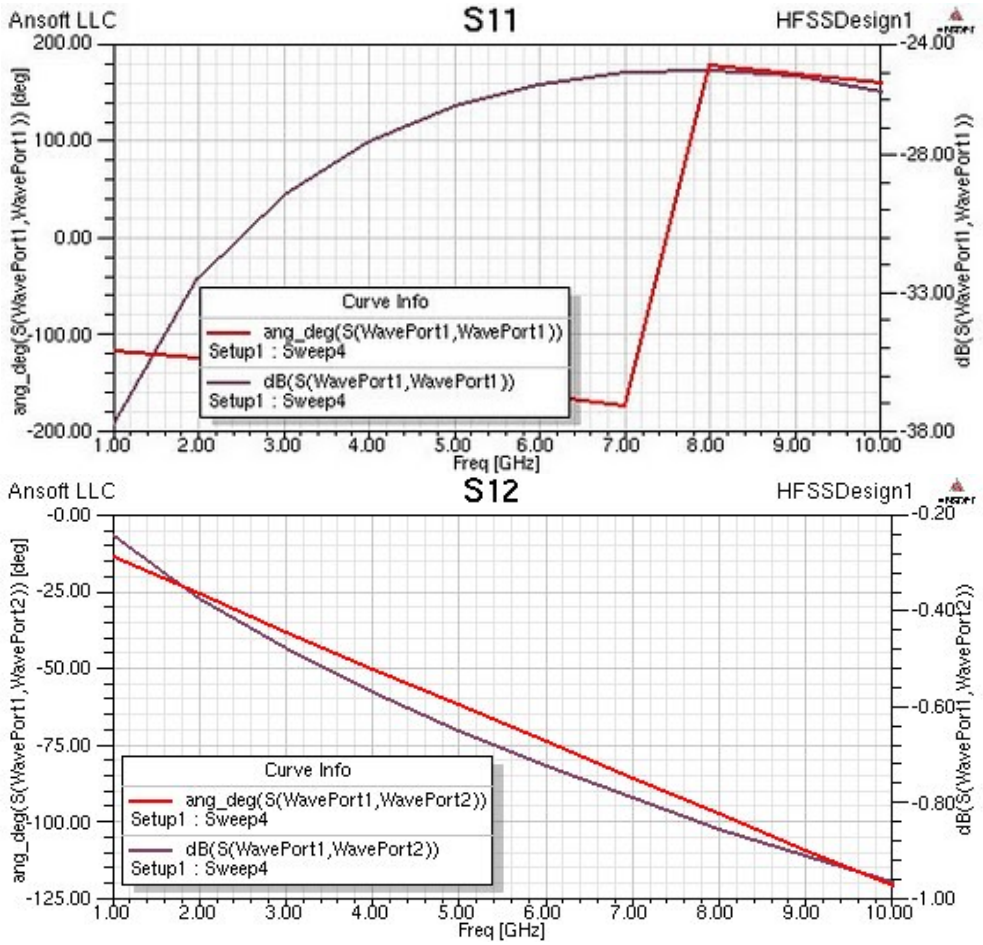


Figure 80. S-parameters of the designed CPW (for 1mm long)

3.2.3 Results

The design methodology was as follows:

1 - Parasitic capacitance extraction of the diode using TCAD simulations as a function of voltage and frequency. Comparison of simulation results with measurements.

2 – Study of distributed ESD protection RF performance improvement over traditional approach. Microwave Office software was used to find the optimum parameter values, which were transmission line electrical lengths for different number of stages and capacitor values.

3 - Design of CPW. Trade-off among signal path width for ESD robustness, losses and layout size. Extraction of touchstone data file.

4 – Simulation of whole circuit by replacing ideal transmission lines with the simulated CPW.

Notice that steps 2 to 4 were repeated several times in order to obtain an optimized design.

In comparison with previous works on distributed ESD protections **[Ito02][Ker05][Kleveland00]**, the methodology followed in this study incorporates the following aspects:

- Design of CPW by using a 3D electromagnetic simulator instead of models. More accurate characterization and incorporation to the matching network by using touchstone files.

- Optimization algorithms (available in Microwave Office software) were used, not only for calculating CPW lengths, but also the distribution of the capacitance. In previous works, the capacitance was established a priori.
- Study of distortion improvement due to capacitance variation on voltage. This is not mention in previous works.

Due to the high losses in the designed CPW, a one stage distributed ESD protection was found to have the best broadband performance (Figure 81). For the optimized electrical length of 67deg the total layout area of the CPW is 150 μm x 2814 μm = 422100 μm^2 .

Figure 82 shows the s-parameters of the regular approach, Figure 83 if the CPW were lossless and Figure 84 using the simulated CPW by importing the touchstone file generated in HFSS. A summary is in Table 16. Figure 85 shows the difference of S21 in dB when there is a variation of 10% of the capacitance value due to voltage sweeping. It can be appreciated that the distributed approach also yields better performance for signal distortion in this case.

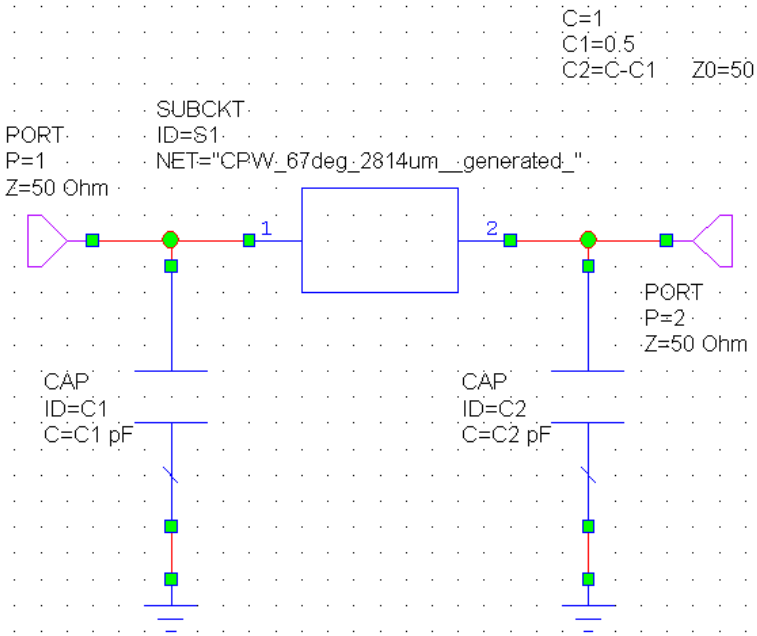


Figure 81. Schematic of the DESD protection circuit.

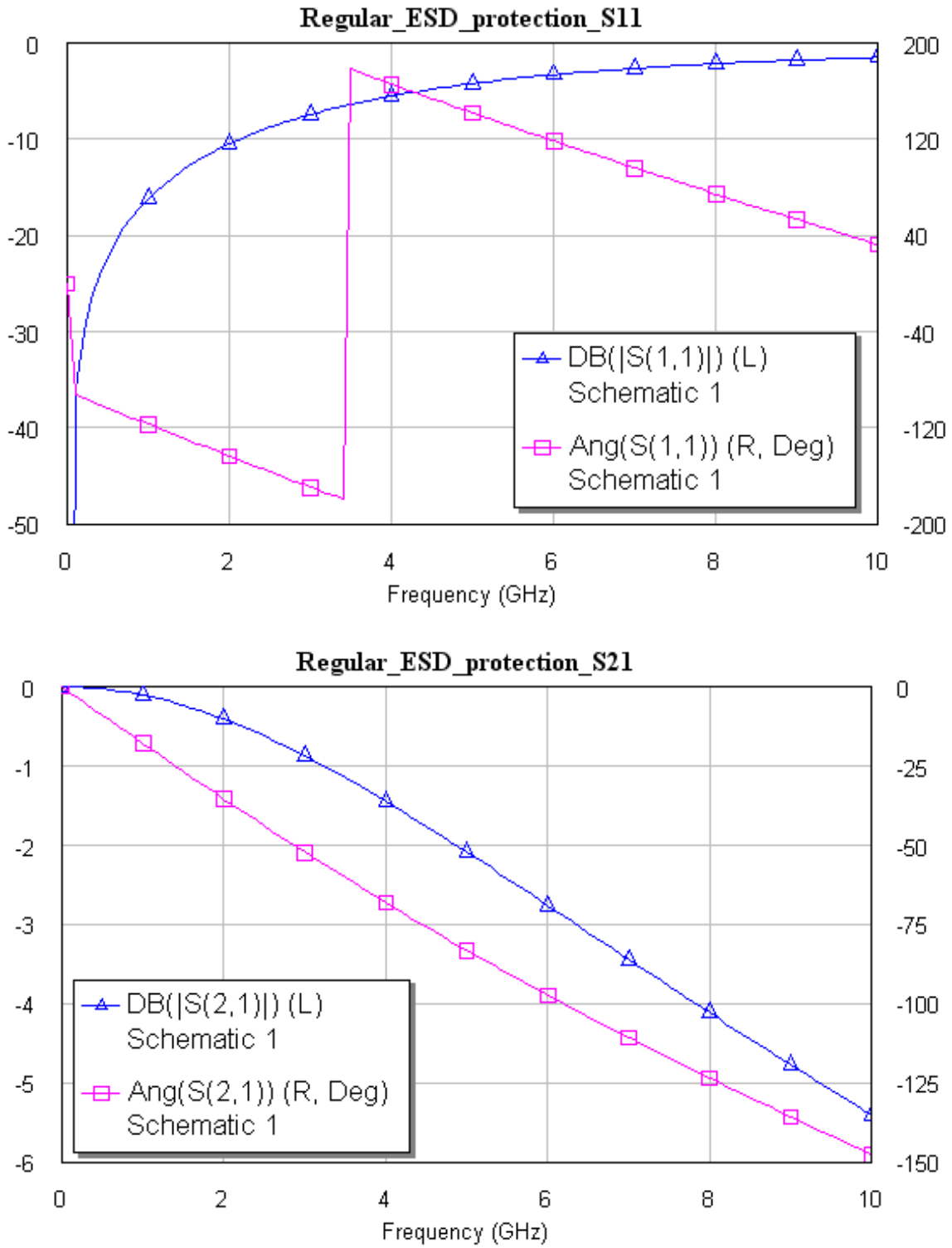


Figure 82. S11 and S21 parameters with a regular approach for 1pF ESD protection parasitic capacitance.

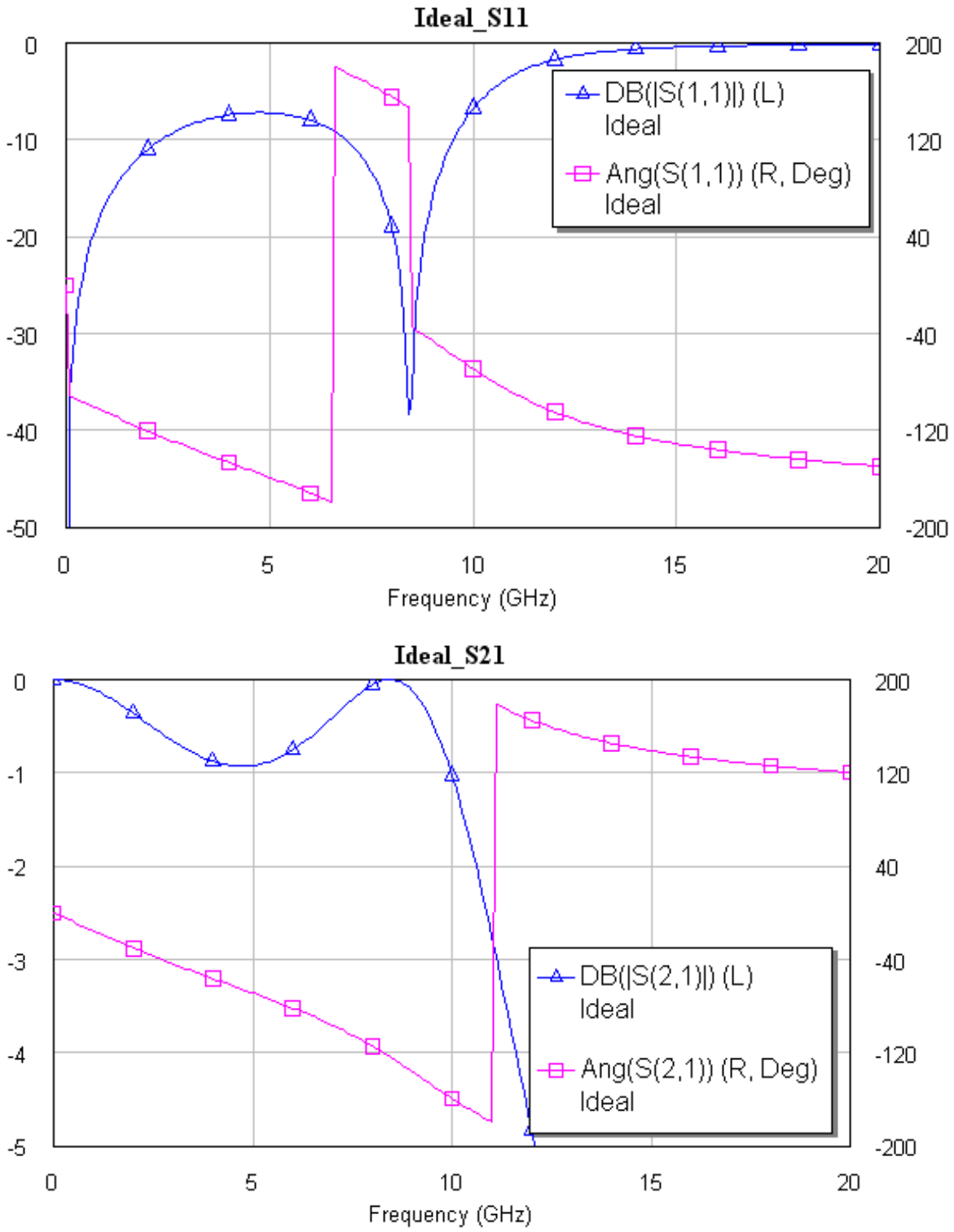


Figure 83. S11 and S21 parameters of DESD circuit (Figure 81) using a lossless transmission line.

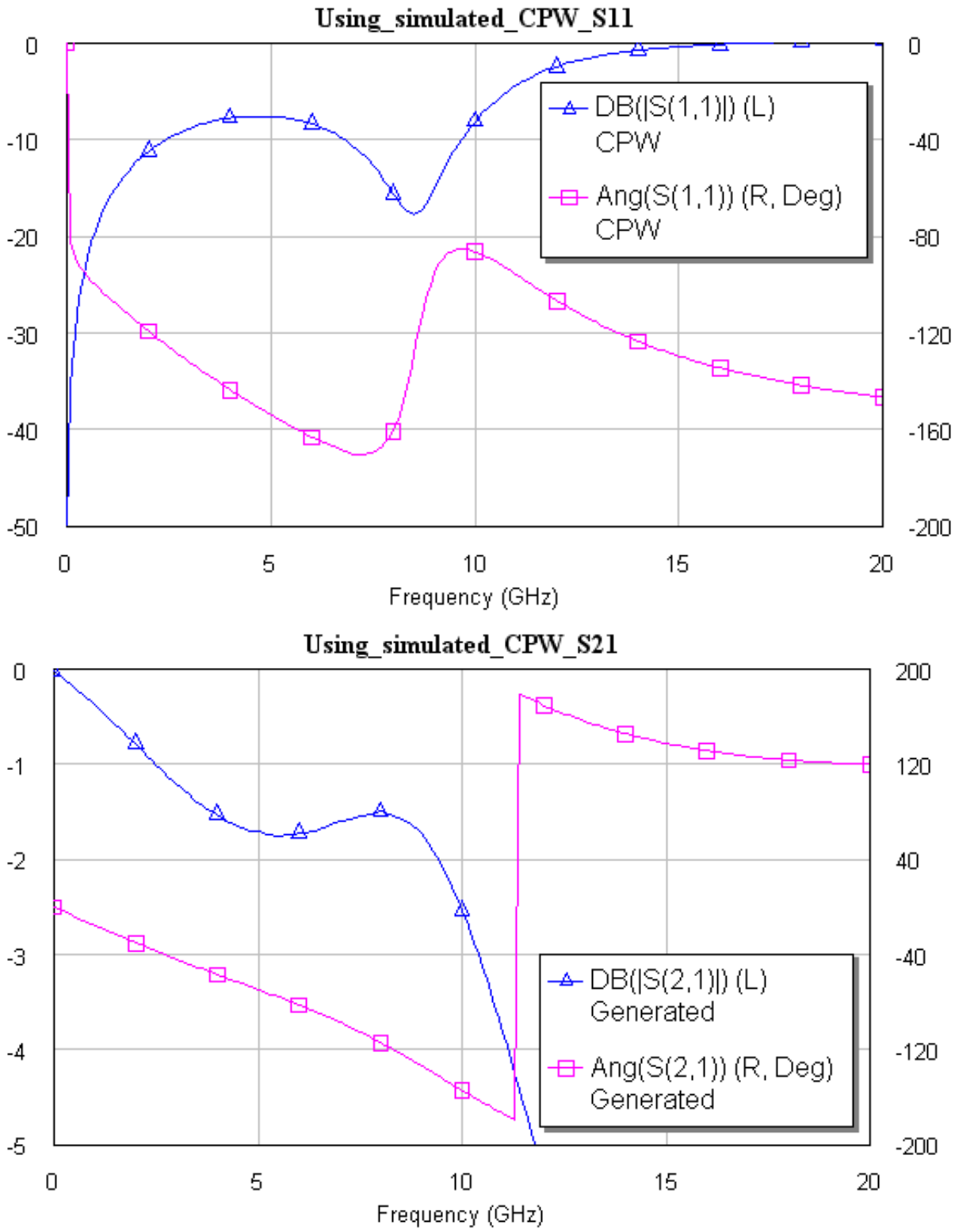
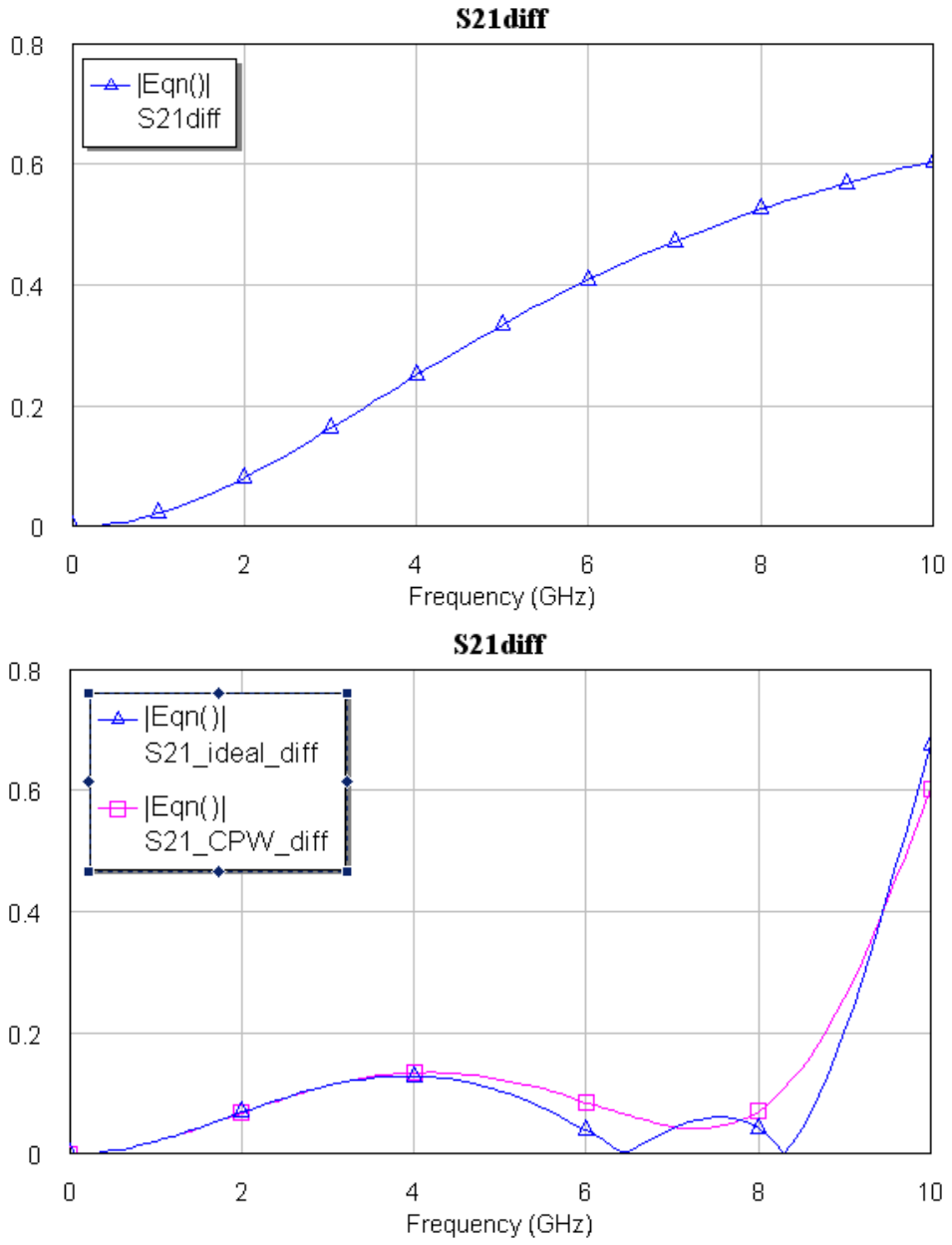


Figure 84. S11 and S21 parameters of DESD circuit (Figure 81) using the simulated CPW.



(a) (b)

Figure 85. Comparison of S21 difference (in dB) between C=1pF and C=1.1pF for regular approach (a) and the designed distributed approach (b).

	Traditional	1 stage distributed (lossless CPW)	1 stage distributed (0.14 μm CMOS CPW)
S21 decay @ 10GHz (dB)	5.5	1	2.5
S21 variation for 10% C variation @ 0-8 GHz (dB)	0.55	0.13	0.13

Table 16. Summary of the designed distributed ESD protection characteristics.

4 Conclusions

This study has reviewed several aspects on the effectiveness and transparency of current ESD protection circuits. Previously, a TCAD input deck for an NXP Semiconductors' proprietary 0.14 μm CMOS technology was calibrated. Simulation results were compared with SIMS measurements. Single device TLP simulations were realized and results were compared with real device measurements to check the validity of the models, finding a good agreement in general.

The effectiveness of two-stage ESD protection circuits has been analyzed by realizing mixed mode two-dimensional TCAD simulations. More specifically, transient simulations were performed for different ESD models, stress levels, primary protections and secondary GGNMOST gate oxide types, values of the resistor and widths of the GGNMOST in the secondary protection. Transient simulation results were computed and safe design area plots were calculated. Safe design area provides the ESD protection designer with a range of values of the resistor and the device width of the secondary protection that ensures the maximum voltage at the gate oxide to protect is below a certain voltage levels. A safe design area plot, therefore, was calculated for any combination of ESD

models, stress levels, primary protections and secondary GGNMOST gate oxide. Voltage levels of 9V and 14V were taken.

One conclusion derived from the safe design area analysis is that the effectiveness hazards can be divided into two cases, depending on whether an overshoot at the beginning of the transient simulation is found or not.

An overshoot voltage is shown for combinations of slow primary protections and fast ESD stresses. As a consequence of the slow turn-on time of the primary protection, the voltage at the primary protection, and hence the voltage at the gate oxide to protect, increases very quickly until the primary protection is fully on.

For the ESD stresses used in this study, the maximum voltage is found after some tens of picoseconds, even though the ESD current has not reached its maximum value yet. At this moment, the current throw the primary protection is still low. The overshoot voltage at the primary protection is thus affected by the smaller amount of current that flows throw the secondary protection. This means that both primary and secondary protection play a role in the maximum voltage at the primary protection.

On the other hand, for the non-overshoot case the effectiveness hazard happens at the maximum ESD current. In this case, the maximum voltage at the gate oxide can be estimated by the TLP plot of the primary protection and the voltage divider formed by the secondary protection at the maximum ESD current time.

Concerning the transparency of ESD protections, two aspects were studied. In the first one, urgent TCAD simulations were required to analyze a leakage problem found for a LVTSCR in a real product. Unexpected too high leakage current was measured when the LVTSCR was exposed to a voltage below from the trigger voltage. Measurements and simulations demonstrated that this current

strongly depends on the amplitude of the applied signal and, in a much lesser extent, on the DC component. Simulations also showed the main contributor to the increase of the leakage current might be the displacement currents due to capacitive coupling at n+/p-well junction.

The second transparency topic was on a novel approach in distributed ESD protection design for improved broadband performance. It consisted of a matching network in which parasitic capacitance of ESD protection devices was spitted. A coplanar waveguide was used as a transmission line. Novelties in this design are the characterization of coplanar waveguides using 3D electromagnetic simulations, optimization of network parameters and estimation of distortion improvement.

List of abbreviations

ESD	Electrostatic Discharge
HBM	Human Body Model
CDM	Charged Device Model
IEC	International Electrotechnical Commission (in this study, it usually refers to the Human Metal Model (HMM))
TLP	Transmission Line Pulsing
GGNMOST	Grounded Gate N-channel Metal Oxide Semiconductor Transistor
LVTSCR	Low Voltage Triggered Silicon Controlled Rectifier
TCAD	Technology Computer-Aided Design (for semiconductor manufacturing technology)
LDD	Lightly Doped Drain
STI	Shallow Trench Isolation
GDS	Graphic Data System (a format for integrated circuit layout data)
GO1,GO2	Gate oxide 1, 2
CPW	Coplanar Waveguide

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[Smedes02] T. Smedes, A. Heringa, J. van Zwol, P.C. de Jong, "The impact of substrate resistivity on ESD protection devices", EOS 2002.

[HMM] IEC TS 62228, "Integrated Circuits - EMC Evaluations of CAN Transceivers ".

[SYSLVL] Presentation of Industry Council on ESD Target Levels, “Aspects of System Level ESD”.

[Wunsch68] D. C. Wunsch, R. R. Bell, “Determination of Threshold Failure Levels of Semiconductor Diodes and Transistors Due to Pulse Voltages”, IEEE Transactions on Nuclear Science, 1968.

[QUBIC1] O. Hubert, “MPWQ4L04 documentation. Layout for Parasitic Extraction study”.

[QUBIC2] J.-P. Kouadio, “MPWQ4C05 documentation. Transmission lines test structures – QUBIC4plus”,2005.

[Estreich81] D.B.Estreich, “The Physics and Modeling of Latch-Up in CMOS Integrated Circuits”, Ph.D.Thesis, Stanford University,1981.

Appendix A: Secondary protection analysis plots

The most relevant plots concerning the secondary protection analysis in this study are attached in this appendix. As explained in section 2.2.2, source code in MATLAB language was programmed for employees at NXP Semiconductors to access all simulation data, including a graphical user interface.

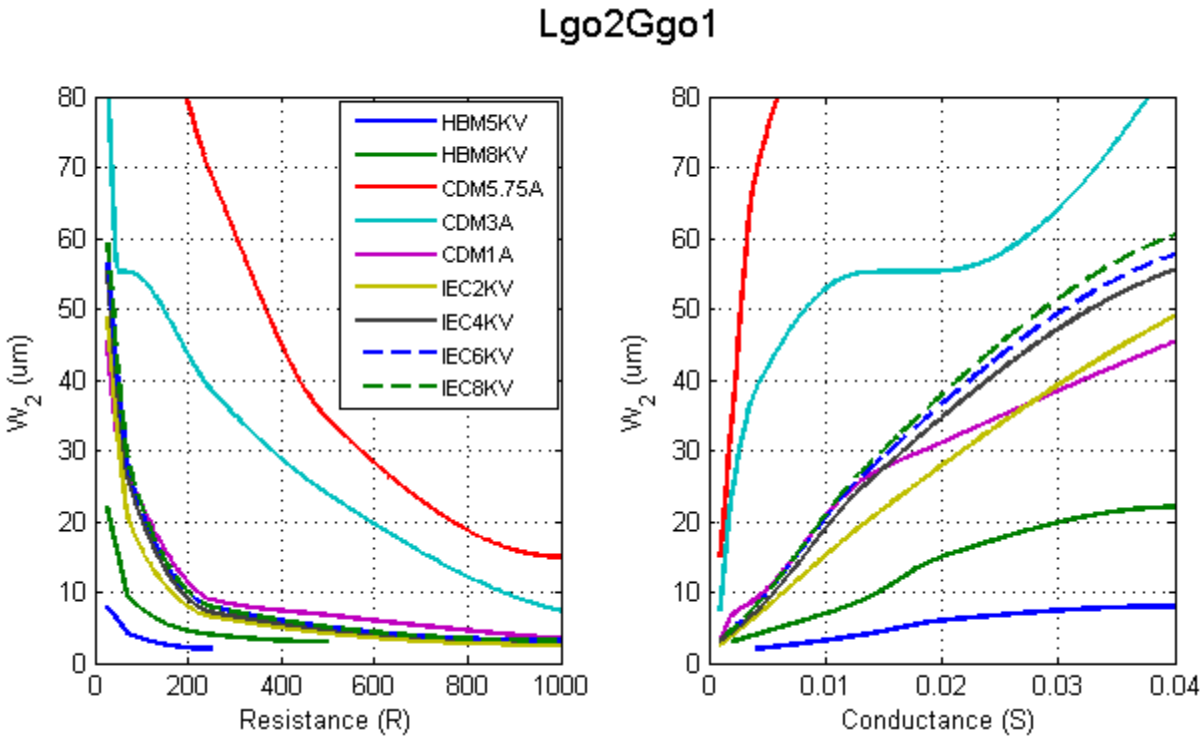
The following figures are divided into three types: safe design area plots, $V_2^{\max}$ versus R_2 plots and transient simulation plots.

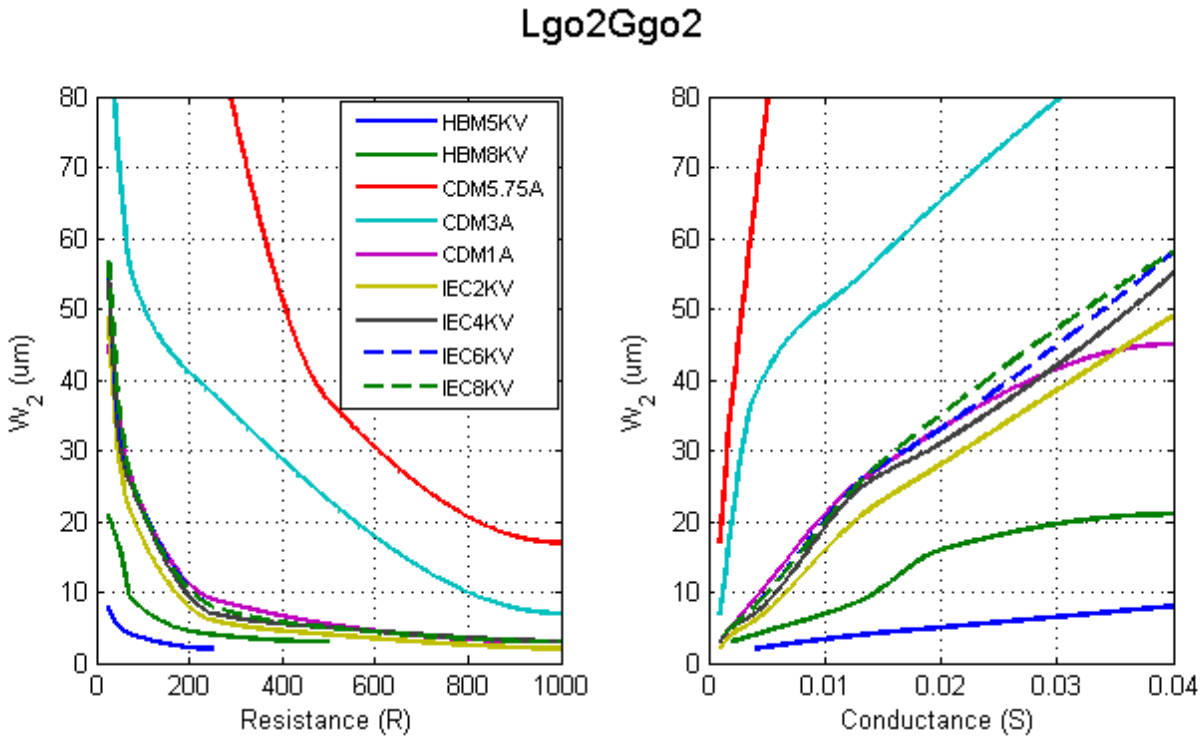
In safe design area plots, some ESD stresses are not shown in some cases because the voltage at the gate oxide did not reach $V_{GOX}^{\max}$. The cases for GGNMOST as primary protection for $V_{GOX}^{\max}$=14V (GO2) did not reach $V_{GOX}^{\max}$ and therefore are not shown.

In $V_2^{\max}$ versus R_2 plots and transient simulation plots, results using secondary protection GGNMOST with GO2 are shown only since it was found that for GO1 the performance is equal or better. Therefore, those figures can be considerer as worse case.

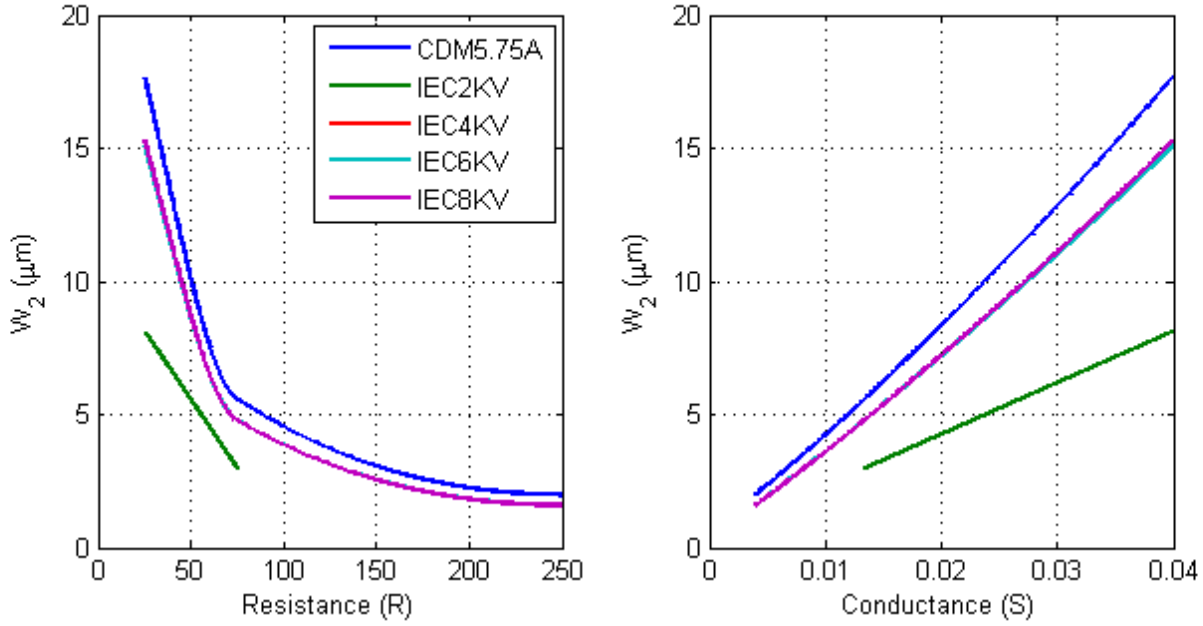
In transient simulations, only a combination of secondary protection parameters is shown as an example.

Safe design area plots ($V_{GOX}^{\max}$ =9V, GO1)



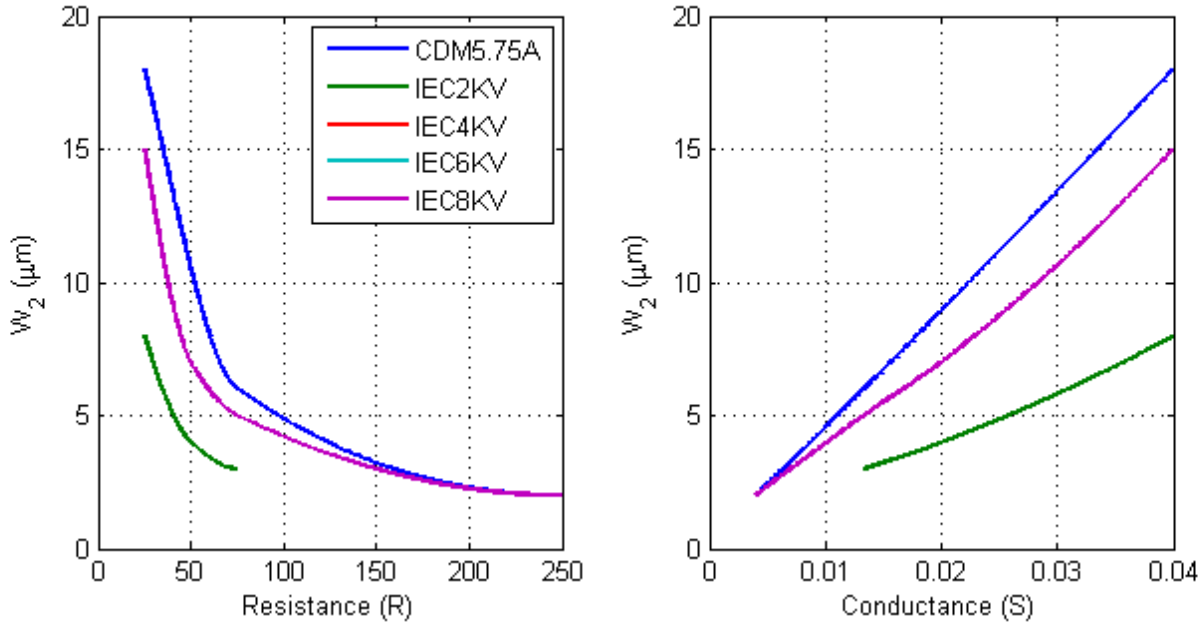


Ggo2Ggo1



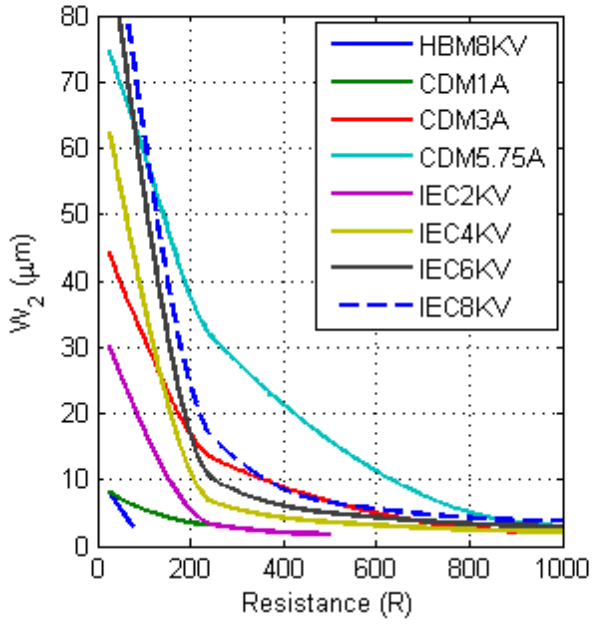
Note: IEC4KV, 6KV and 8KV are overlapped

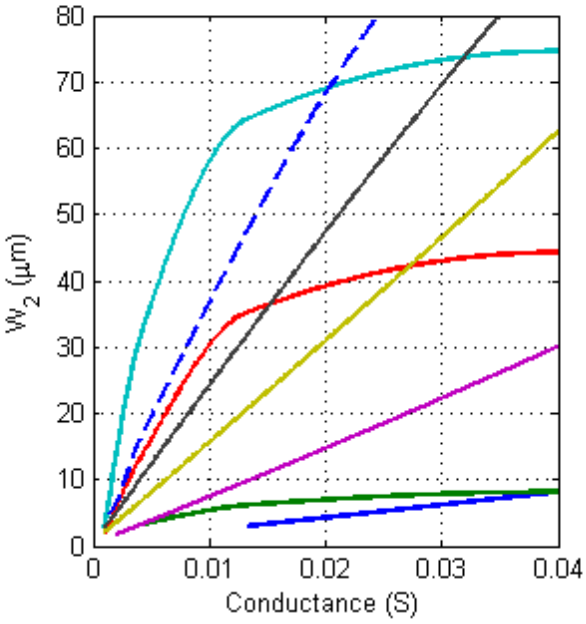
Ggo2Ggo2



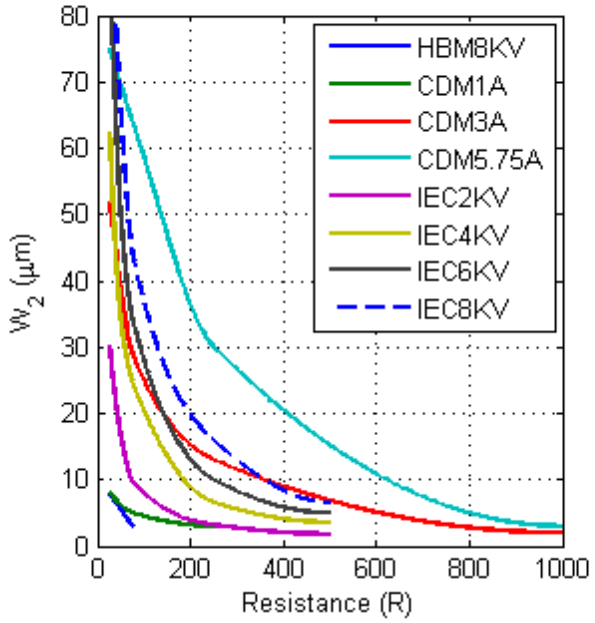
Note: IEC4KV, 6KV and 8KV are overlapped

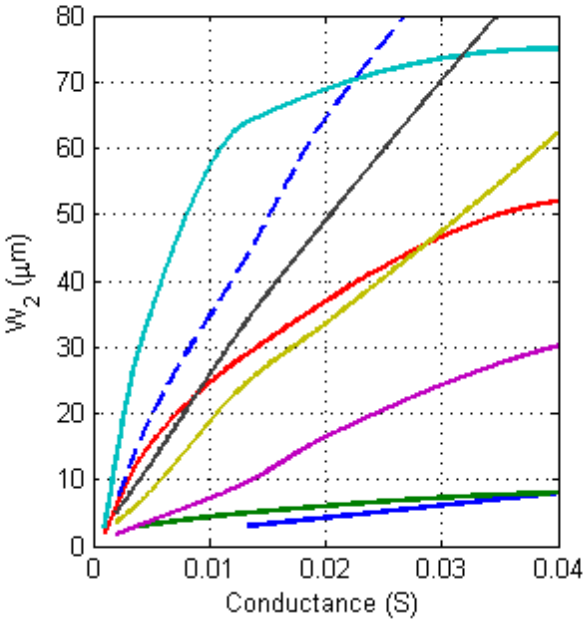
RB1Ggo1



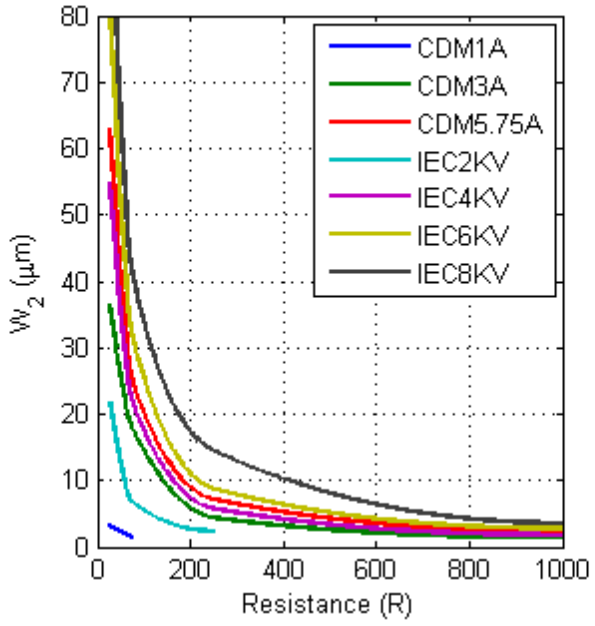


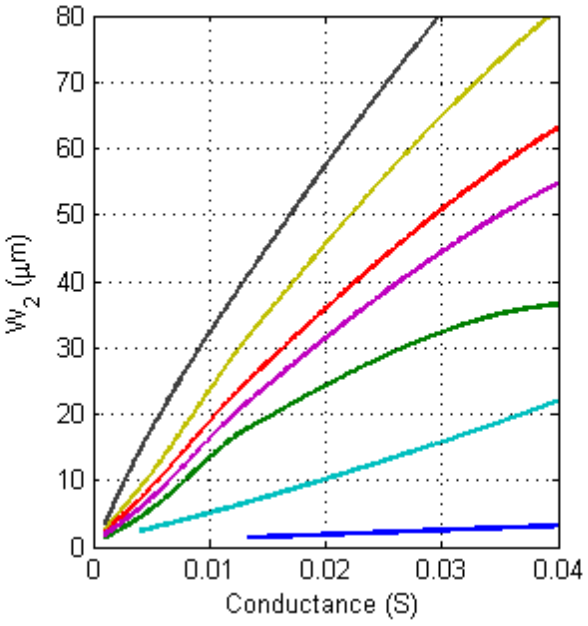
RB1Ggo2



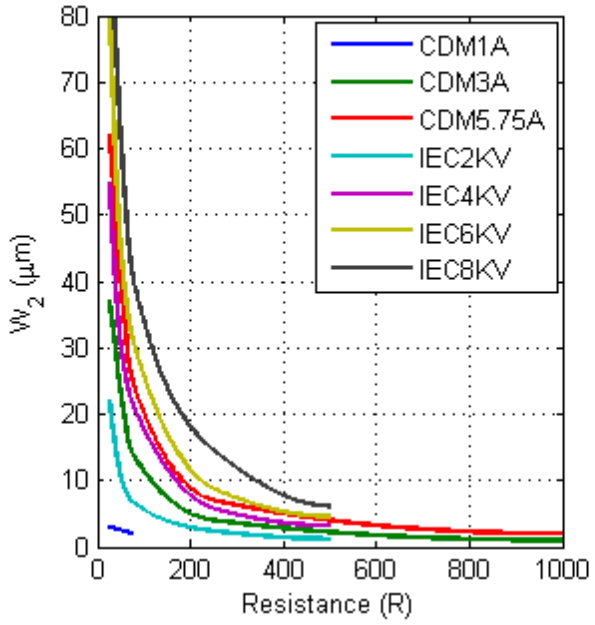


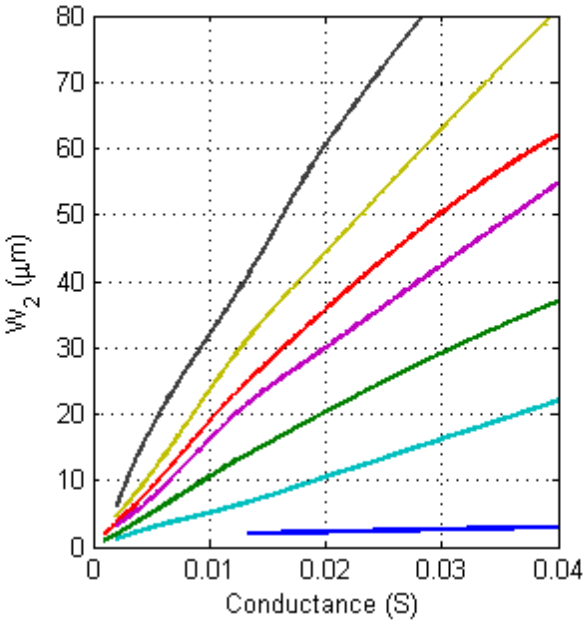
RB2Ggo1



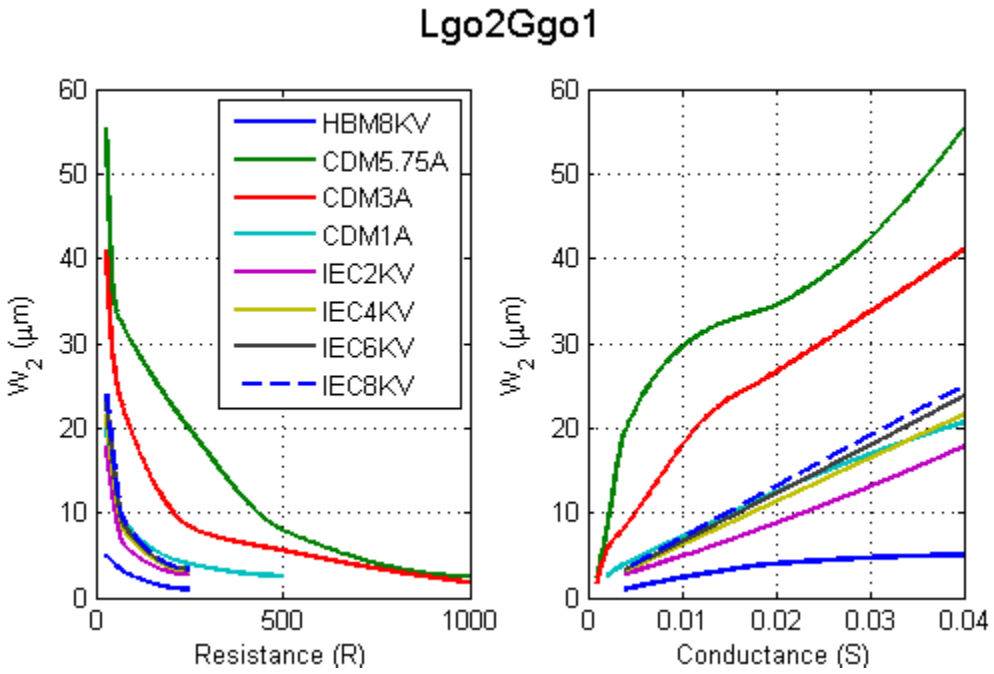


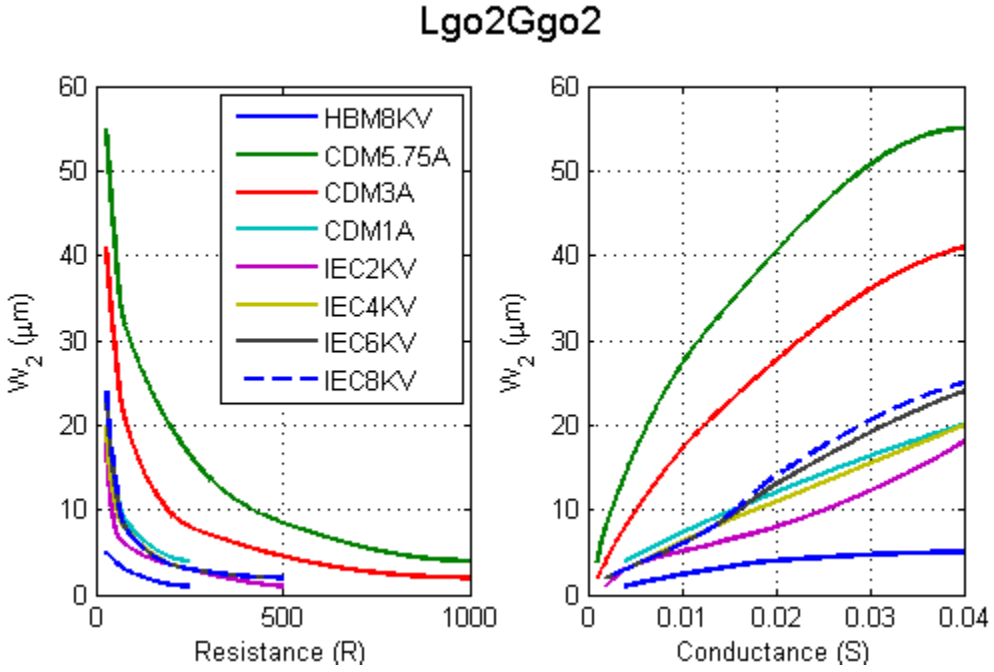
RB2Ggo2



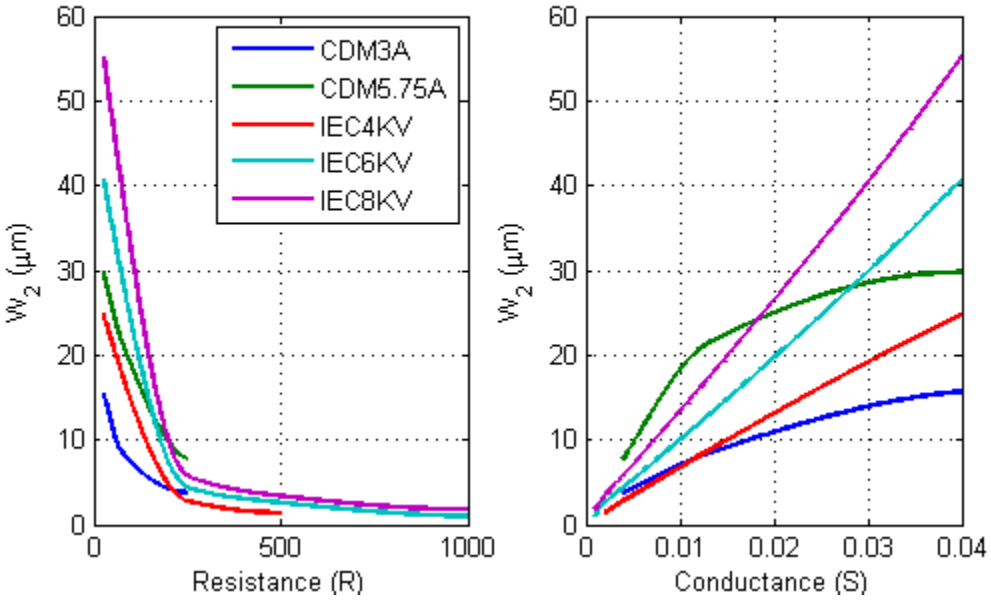


Safe design area plots ($V_{GOX}^{\max}$ =14V, GO2)

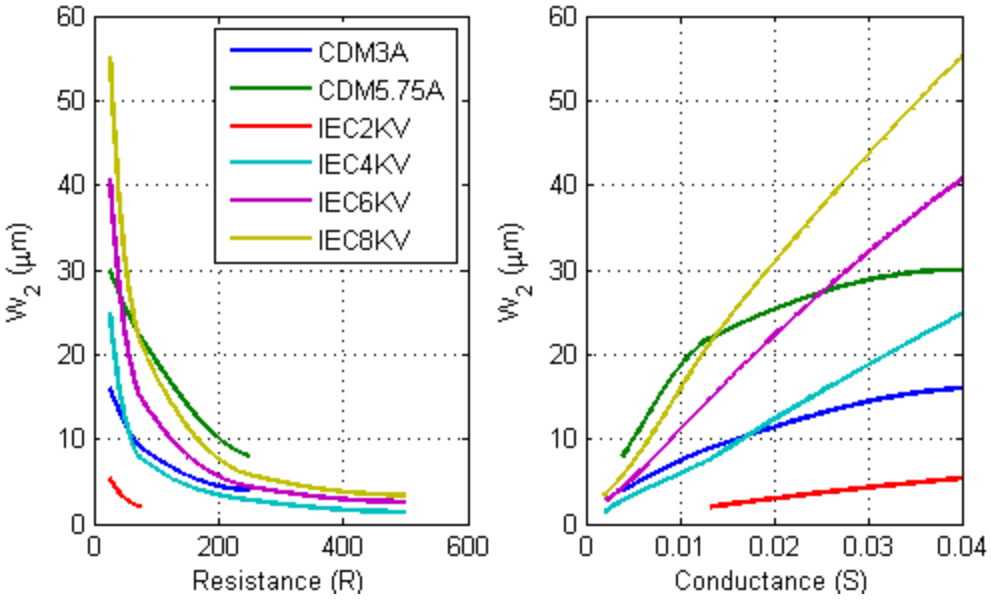




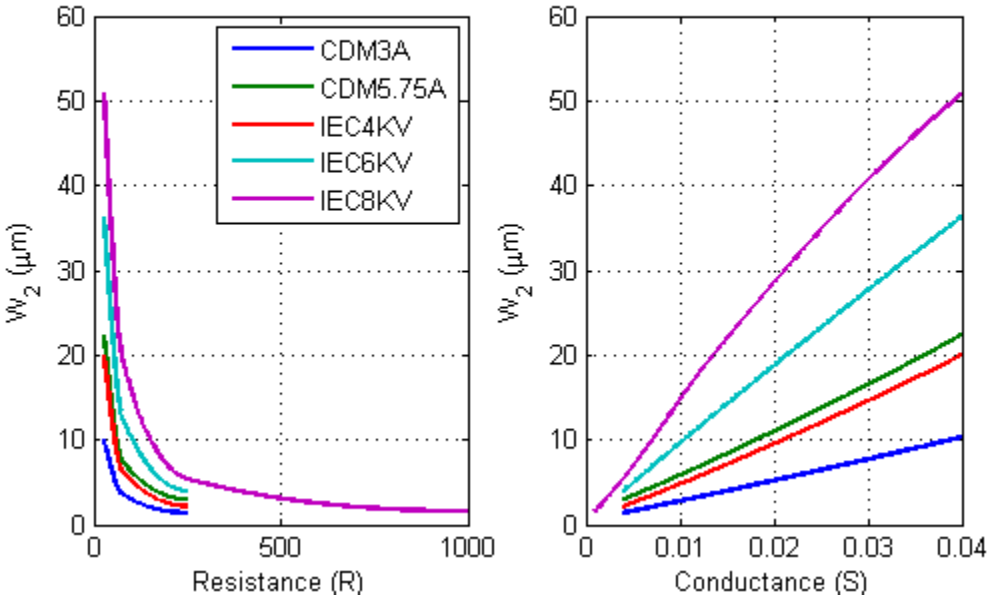
RB1Ggo1



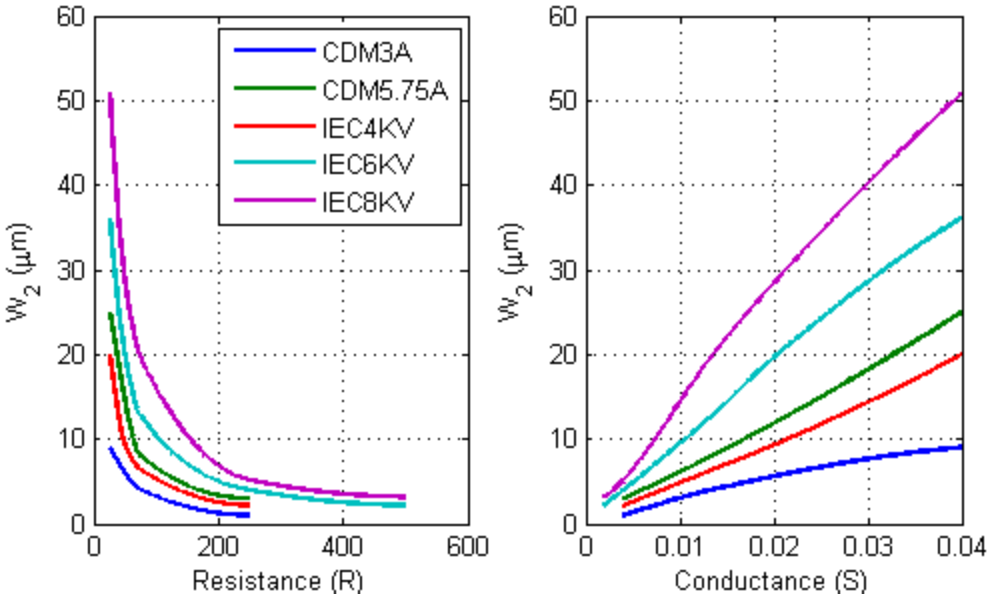
RB1Ggo2



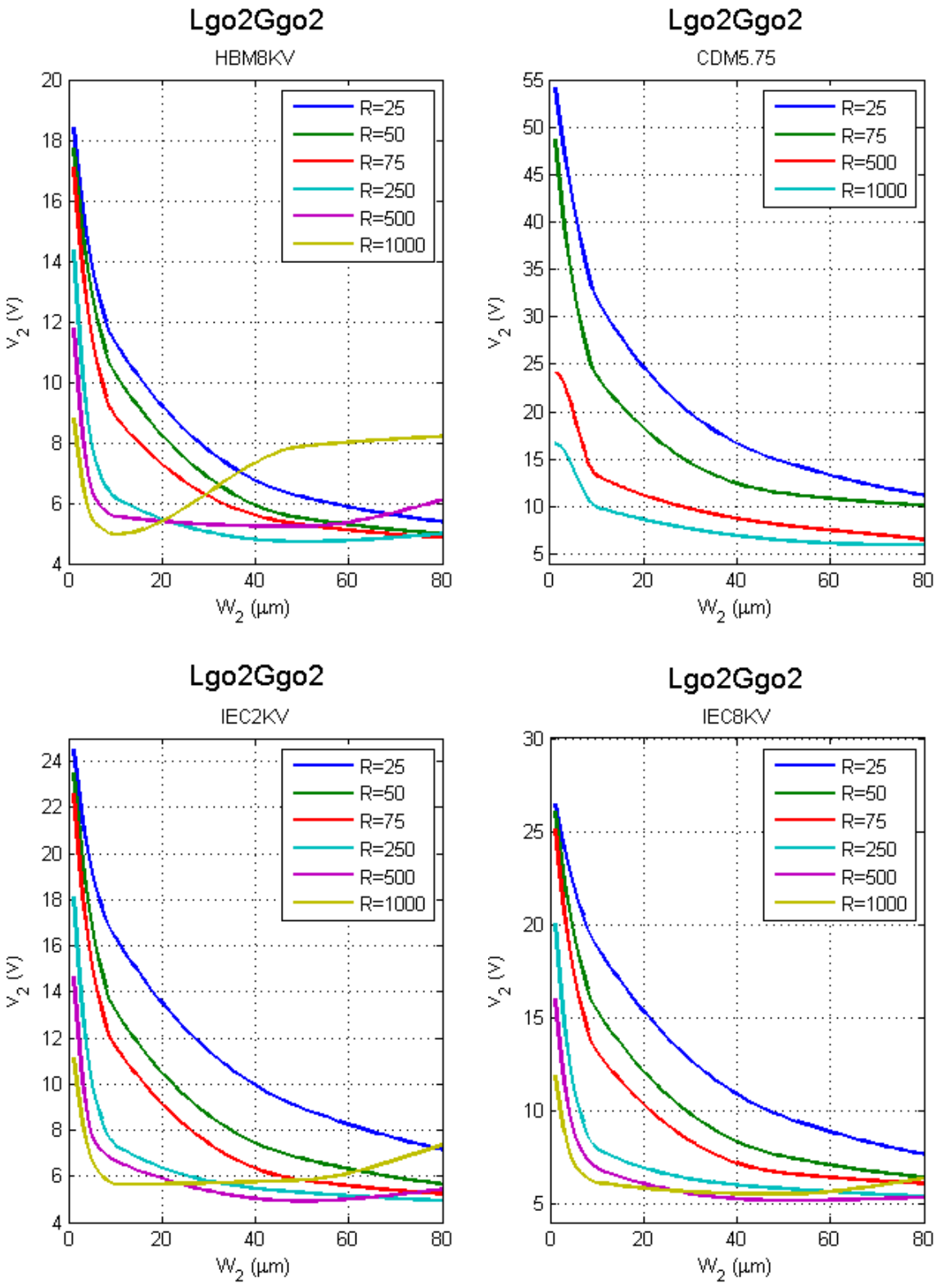
RB2Ggo1

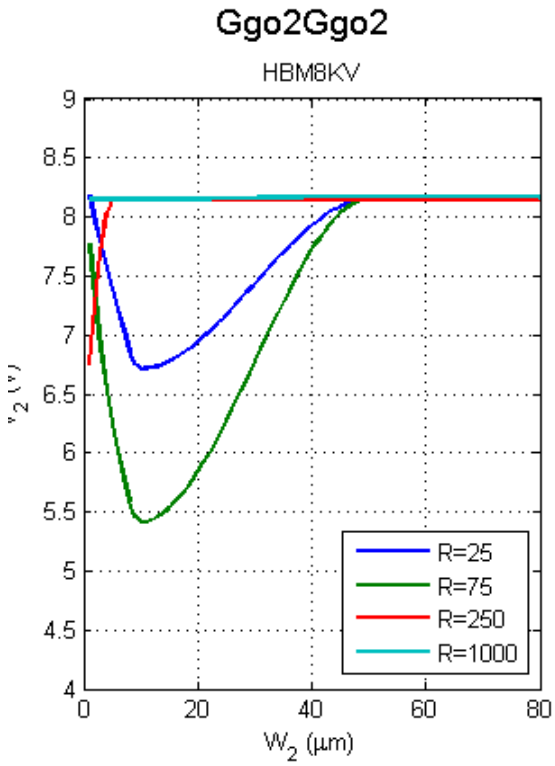


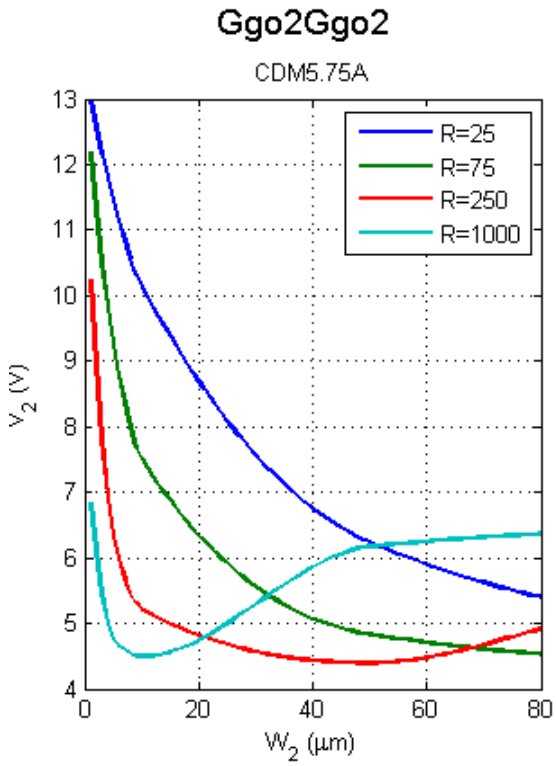
RB2Ggo2

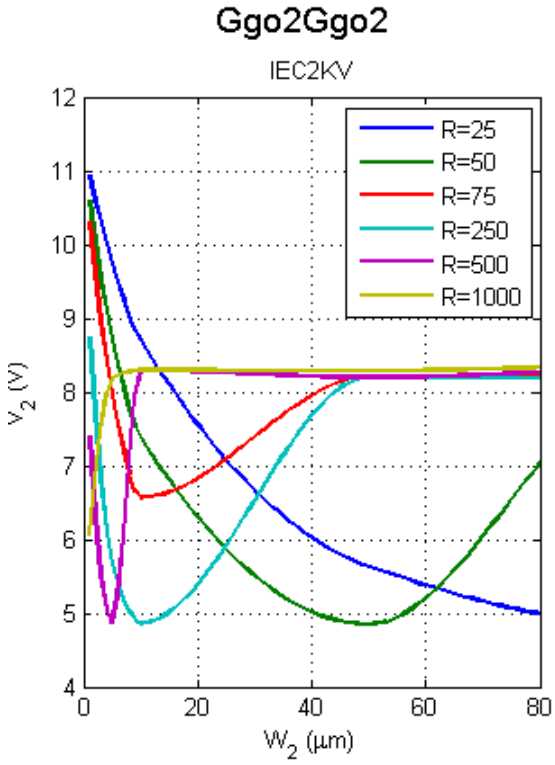


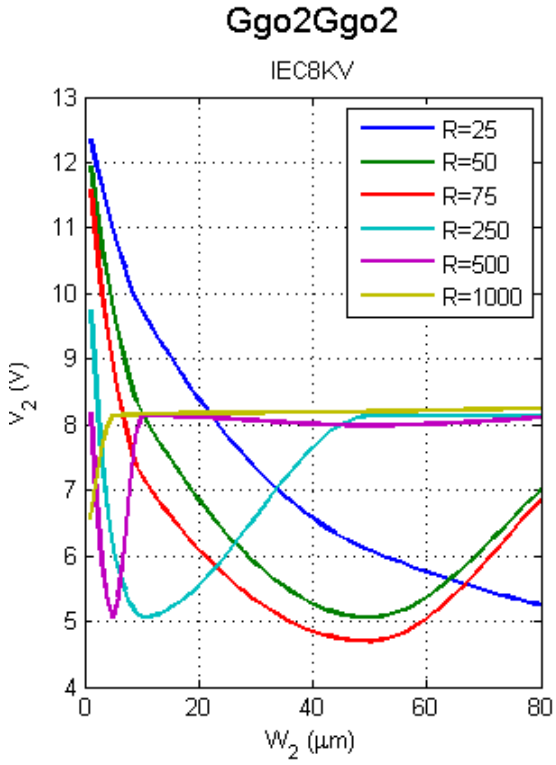
V_2^{max} **VS** R_2 **plots**

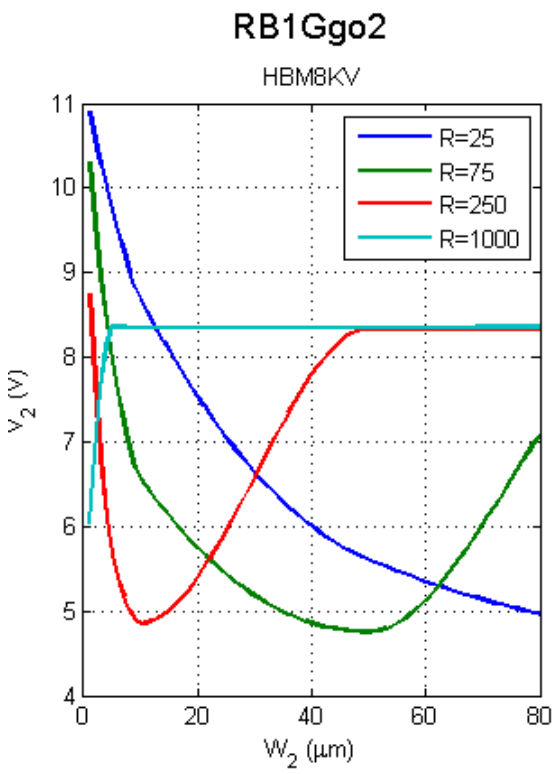


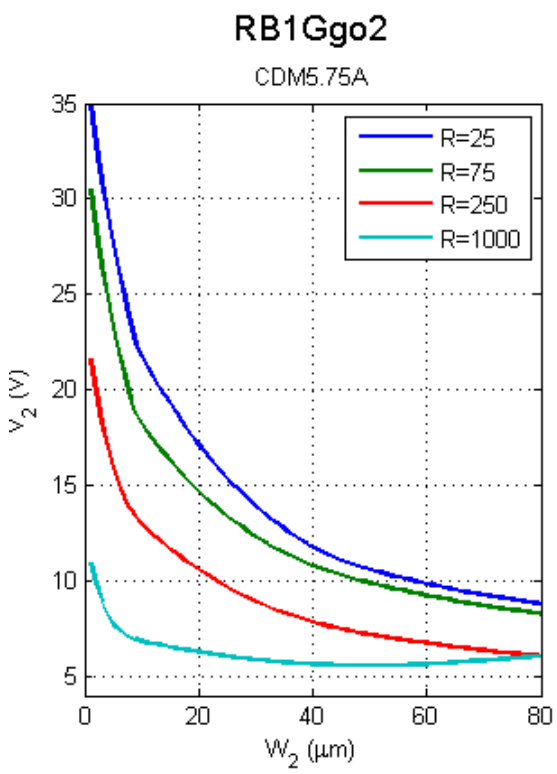

Ggo2Ggo2
HBM8KV
R=25
R=75
R=250
R=1000
V_2 (V)
W_2 (μm)

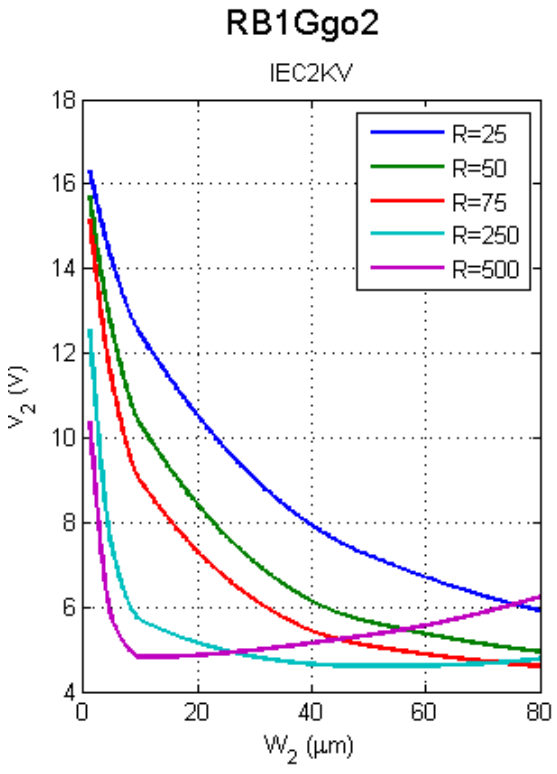

Ggo2Ggo2
CDM5.75A
R=25
R=75
R=250
R=1000
V_2 (V)
W_2 (μm)

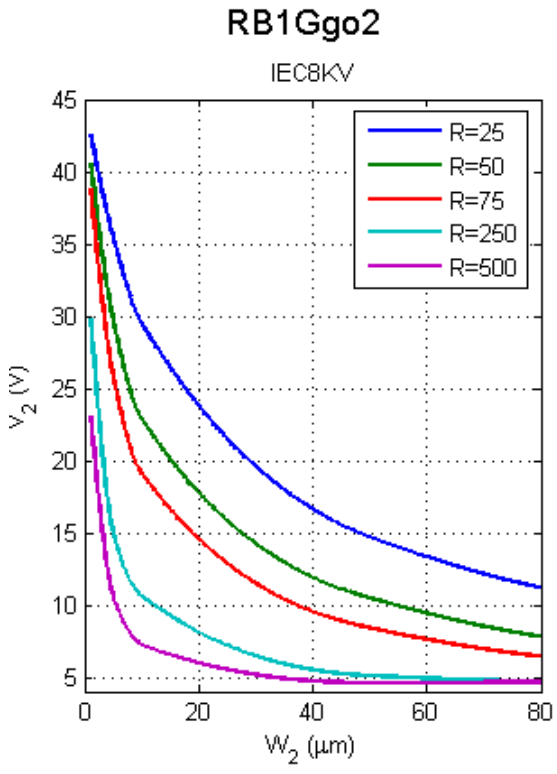

Ggo2Ggo2
IEC2KV
R=25
R=50
R=75
R=250
R=500
R=1000
V_2 (V)
W_2 (μm)

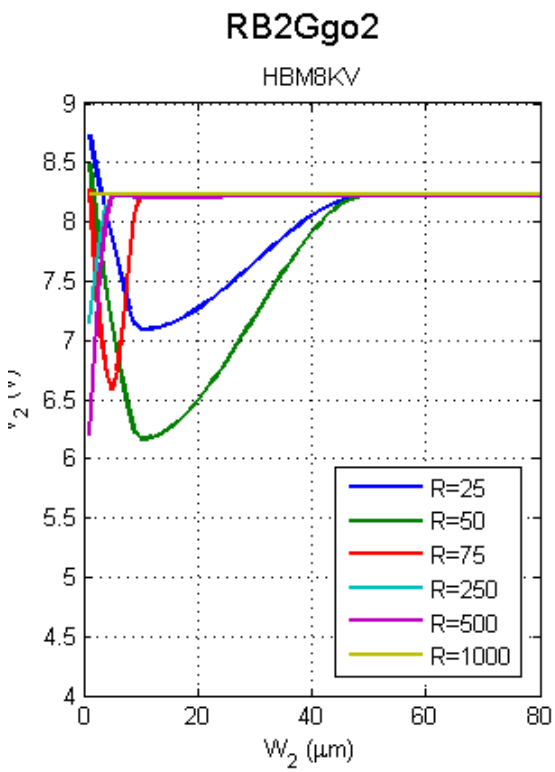

Ggo2Ggo2
IEC8KV
R=25
R=50
R=75
R=250
R=500
R=1000
V_2 (V)
W_2 (μm)

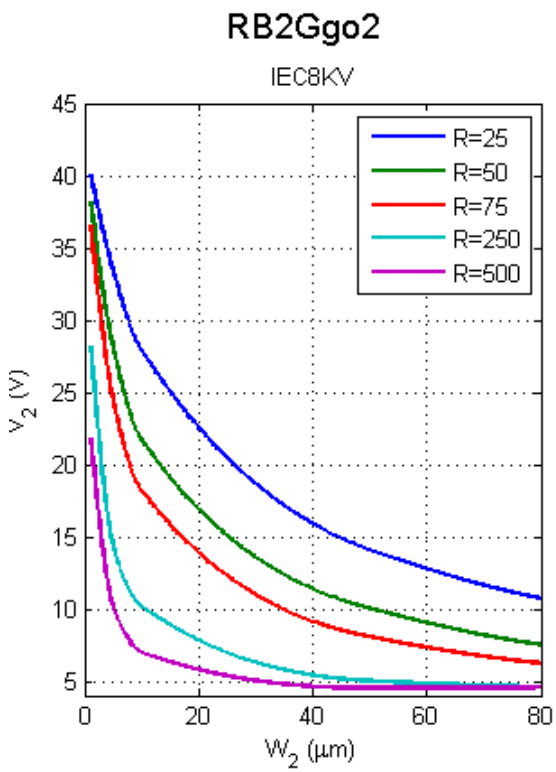

RB1Ggo2
HBM8KV
R=25
R=75
R=250
R=1000
V2 (V)
W2 (µm)

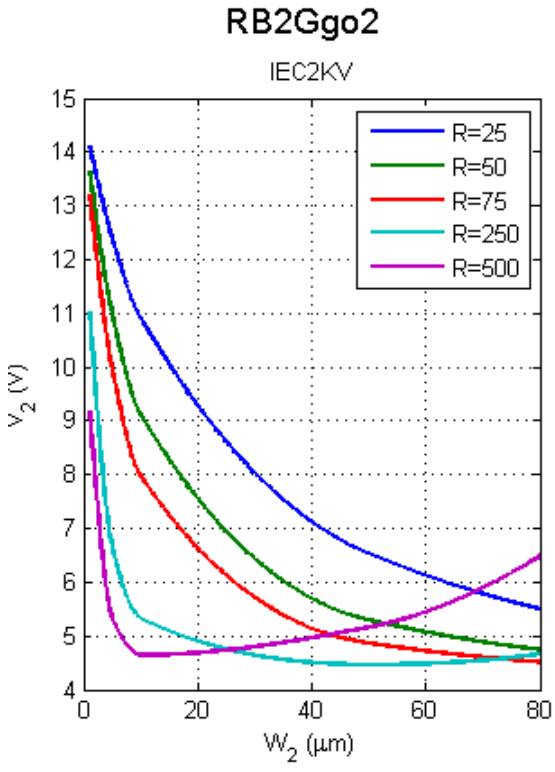

RB1Ggo2
CDM5.75A
R=25
R=75
R=250
R=1000
V2 (V)
W2 (µm)

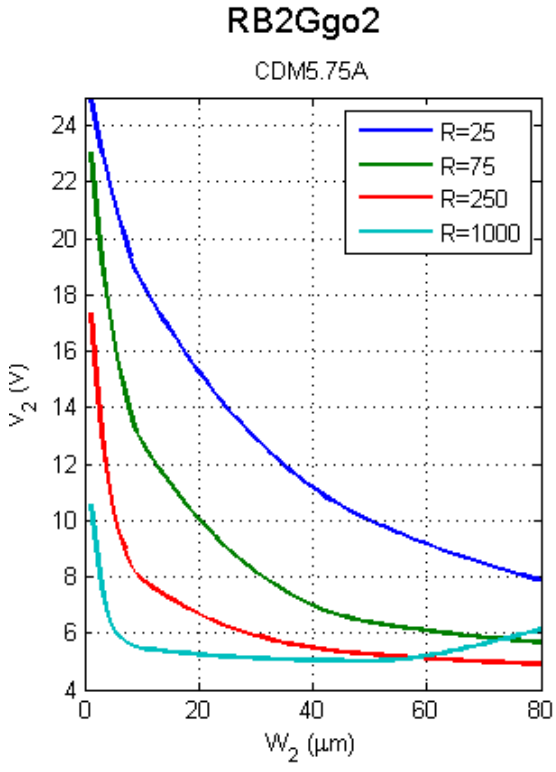

RB1Ggo2
IEC2KV
R=25
R=50
R=75
R=250
R=500
V2 (V)
W2 (µm)


RB1Ggo2
IEC8KV
R=25
R=50
R=75
R=250
R=500
V2 (V)
W2 (µm)

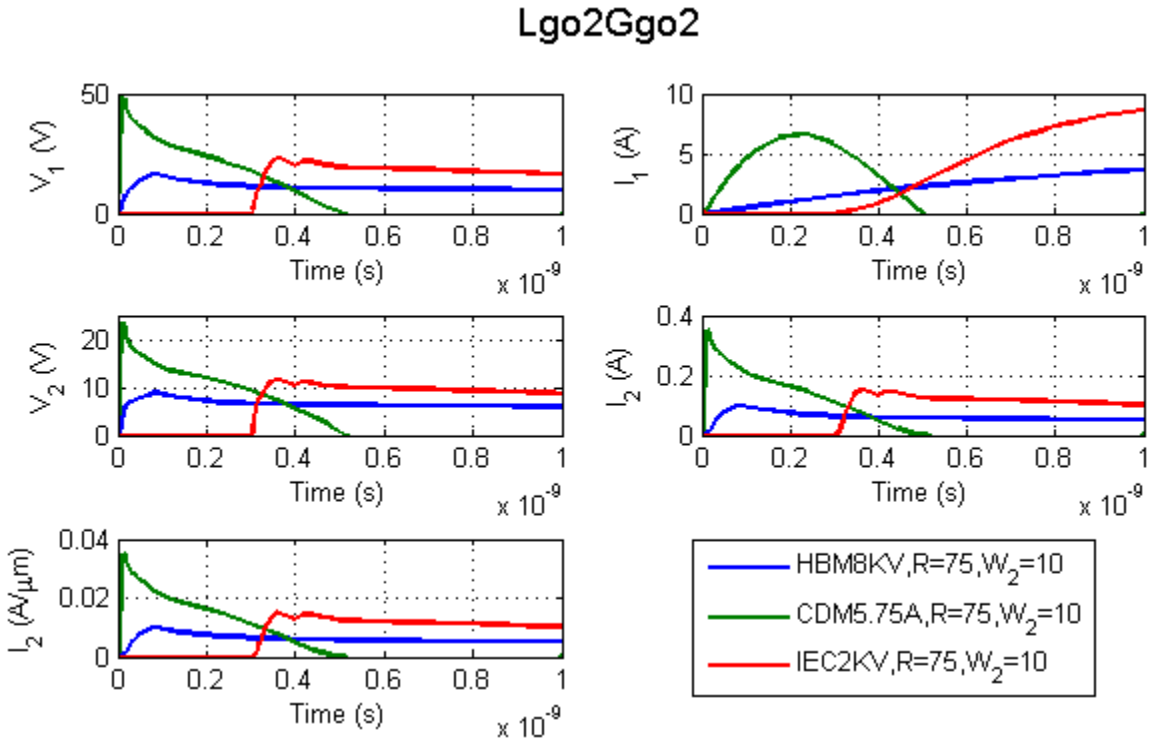

RB2Ggo2
HBM8KV
R=25
R=50
R=75
R=250
R=500
R=1000
W2 (µm)

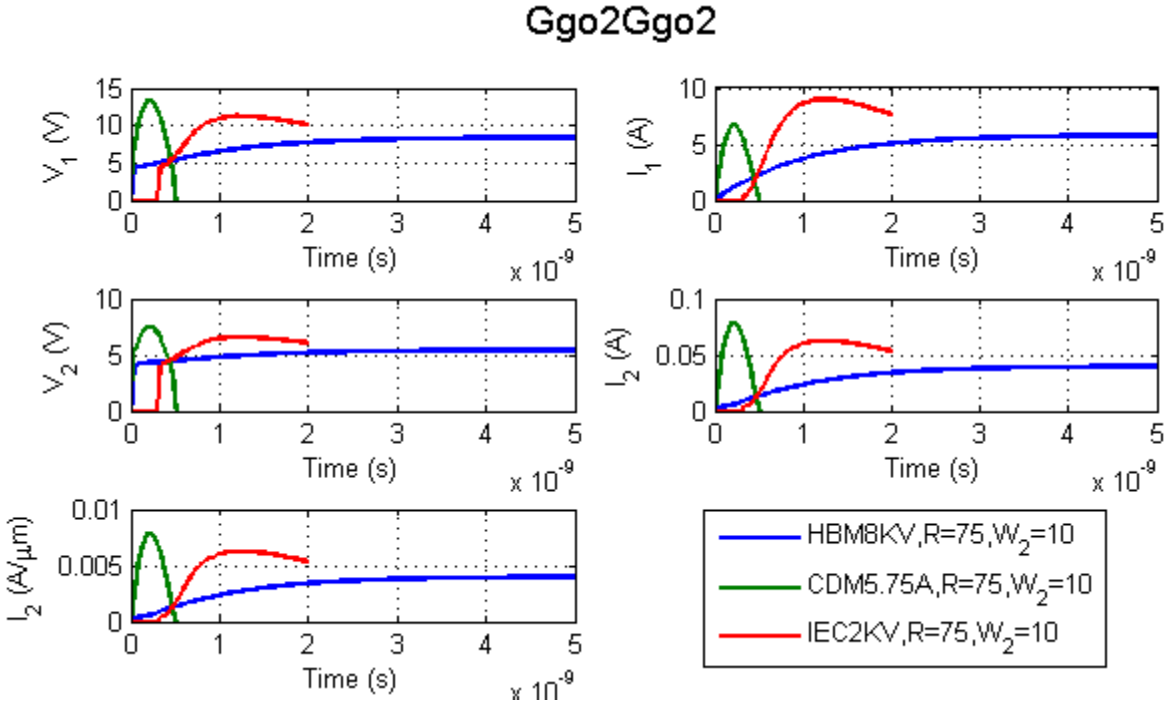

RB2Ggo2
IEC8KV
R=25
R=50
R=75
R=250
R=500
V2 (V)
W2 (µm)


RB2Ggo2
IEC2KV
R=25
R=50
R=75
R=250
R=500
V2 (V)
W2 (µm)

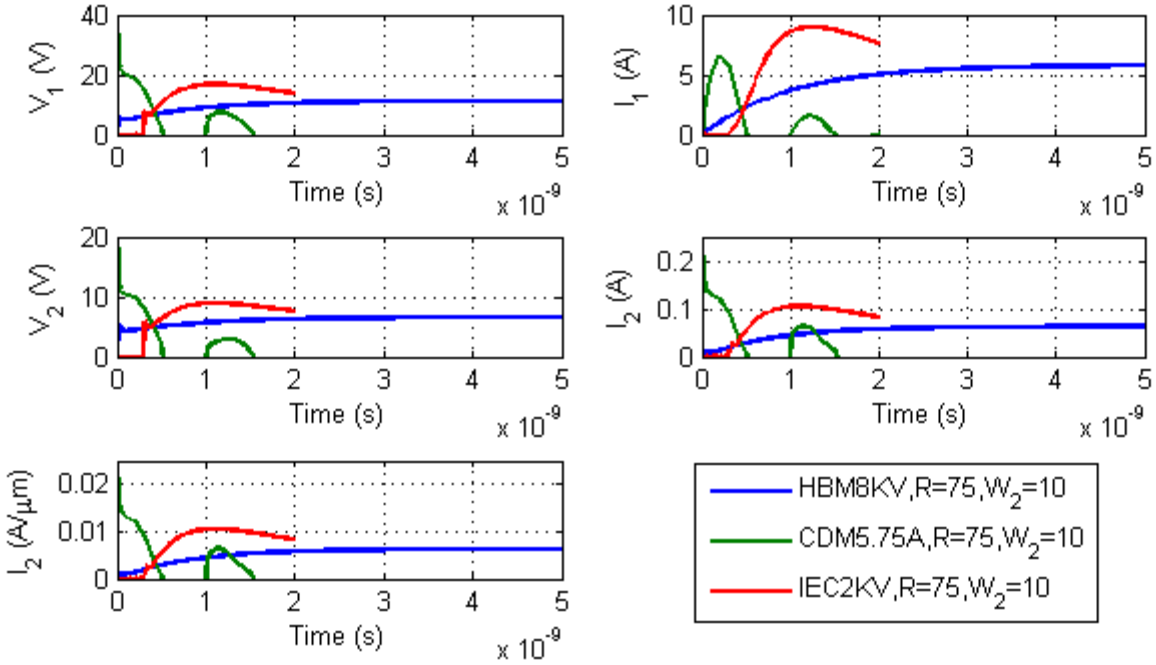

RB2Ggo2
CDM5.75A
R=25
R=75
R=250
R=1000
V2 (V)
W2 (µm)

Transients of two-stage ESD protection circuits

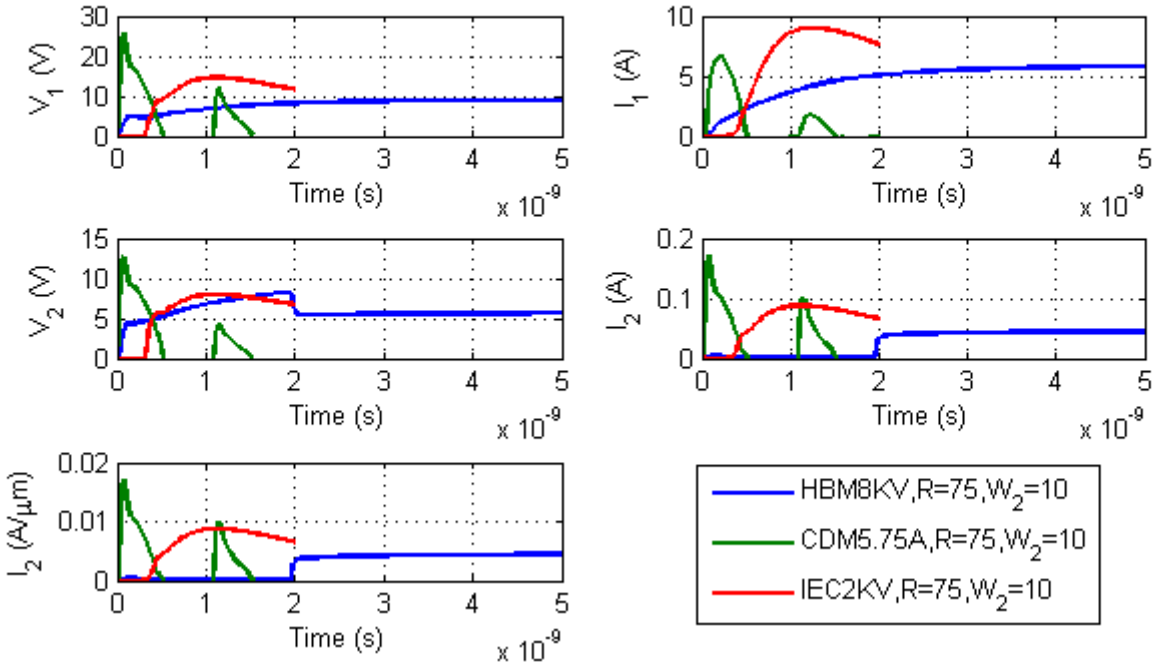




RB1Ggo2



RB2Ggo2



Appendix B: MATLAB source codes

The most relevant files and pieces of code related to MATLAB used in this work are now described.

ESD protection analysis

result.m	*result* class definition of generic data structure.
esd.m	*esd* class definition of an ESD analysis where a number of result objects are stored, analyzed and plotting data is calculated.
tlp.m	*tlp* class definition of a TLP analysis where a number of result objects are stored, analyzed and plotting data is calculated.
launcher.m	Loads all simulation data by navigating along the directory tree. Creates *esd* and *tlp* objects, among others. Plotting data is calculated.
GUI.m	GUI definition and implementation.
GUI_result.m	Class definition of plotting data.
GUI_plotdef.m	Class definition of plotting definition.
GUI_saved_workspace.mat	Stores all data and plotting configurations in one single file.
Plotting_data_(plain_text).txt	All data to plot (from all TCAD simulations).
Plotting_conf_(plain_text).txt	Definitions of plotting styles and configurations.

Leakage problem

lvtscr_leakage.m	*lvtscr_leakage* class definition that stores and computes data from the leakage TCAD simulations.
lvtscr_leakage_launcher.m	Creates *lvtscr_leakage* objects and plots results.

Others

Medici_waveform_generator.m	Script code to generate Medici source code for a given current waveform.

Fragment of code in GUI.m showing parametric plotting

```
[...]
for i=1:length(list2)

nc=list2(i);
legends(end+1)=cellstr(g(nc).curve_title);

    [...]
    for ns=1:num_subplots

        nx=g2(nf).axis_column(ns,1);
        ny=g2(nf).axis_column(ns,2);
        x=g(nc).data(:,nx);
        y=g(nc).data(:,ny);

        typex=char(g2(nf).axis_type(ns,1));
        typey=char(g2(nf).axis_type(ns,2));

        subplot(g2(nf).subplot_config(1),g2(nf).subplot_config(2),ns);

        % interpolation by means of pchip method in interp1 command
        if sum(size(strfind(typex,'pchip'))) | sum(size(strfind(typey,'pchip')))
            xx=linspace(min(x),max(x),500); yy=interp1(x,y,xx,'pchip')';
            x=xx; y=yy;
        end

        % linear/logarithmic scales
        if strfind(typex,'lin') & strfind(typey,'lin')
            p=plot(x,y);
        end
        if strfind(typex,'lin') & strfind(typey,'log')
            p=semilogy(x,y);
        end
        if strfind(typex,'log') & strfind(typey,'lin')
            p=semilogx(x,y);
        end
        if strfind(typex,'log') & strfind(typey,'log')
            p=loglog(x,y);
        end
        grid on; hold on;

        color_num=mod(i-1,length(pcolor))+1;
        set(p,'LineWidth',1.5,'MarkerSize',10,'Color',pcolor(color_num,:), ...
            'LineStyle',char(pstyle(color_num)));

        xlabel(char(g2(nf).axis_title(ns,1)));
        ylabel(char(g2(nf).axis_title(ns,2)));
        title(char(g2(nf).subplot_title(ns)));

        [...]
    end

end

[...]
suptitle(char(g2(nf).super_title));
legend(char(legends));
[...]
```