Abstract

This thesis studies the design of non-binary error-correction decoders for high-speed modern communication systems. The objective is to propose low complexity decoding algorithms for non-binary low-density parity-check (NB-LDPC) and Reed-Solomon codes, to implement efficient hardware architectures.

In the first part of the thesis, we analyze the bottlenecks of the existing algorithms and architectures for NB-LDPC decoders and we propose low-complexity high-speed solutions based on symbol-flipping algorithms. First, flooding schedule solutions are designed with the aim of obtaining the highest-throughput possible without considering coding gain. Two different decoders based on clipping and blocking techniques are proposed; however, the maximum frequency is limited due to an excessive wiring. For this reason, we explore some methods to reduce the routing problems in NB-LDPC. A half-broadcasting architecture for symbol-flipping algorithms that mitigates the routing congestion is proposed. As the flooding schedule solutions with higher throughput are sub-optimal from a frame error rate performance point of view, we decide to design solutions for the serial schedule, with the objective of reaching higher throughput but keeping the coding gain of the original symbol flipping algorithms. Two serial schedule algorithms and architectures are introduced, reducing the required area resources of the decoders and increasing the maximum speed achievable. Finally, we generalize symbol-flipping algorithms and we show that some particular cases can achieve a coding gain close to Extended Min-sum and Min-max algorithms with lower complexity. An efficient architecture is proposed, showing that area resources are reduced to half compared to a direct mapping solution.

In the second part of the thesis, soft-decision decoding Reed-Solomon algorithms are compared, concluding that low complexity Chase (LCC) algorithm is the most efficient solution if high-speed is the main objective. However, LCC schemes are based on interpolation, which introduces some hardware limitations due to its complexity. In order to reduce complexity without modifying performance, we propose a soft-decision LCC scheme based on hard-decision algorithms. An efficient architecture is designed for this new scheme.