

Contents

List of Figures	vii
List of Tables	ix
Abstract	xi
<i>Resumen</i>	xiii
<i>Resum</i>	xv
1 Introduction	1
1.1 Current cache design and motivation	2
1.2 RAM technologies	2
1.3 Manufacturing imperfections	4
1.4 Working under the threshold voltage	5
1.5 Objectives of the thesis	6
1.6 Contributions of the thesis	6
1.7 Thesis outline	7
2 Related work	9
2.1 Leakage reduction in SRAM caches	10
2.2 Fault-tolerant caches	11
3 Experimental Framework	13
3.1 General view of the simulation environment	14
3.2 HSPICE	15
3.3 CACTI	15
3.4 SimpleScalar	16
3.5 Workload	16
4 Heterogeneous Caches	19
4.1 Macrocell-based caches (M-Caches)	20
4.1.1 Macrocell internals	20
4.1.2 Accessing the M-Cache	23
4.2 Timing and area details	25
4.2.1 Retention time	25
4.2.2 Access time	26
4.2.3 Area	27
4.3 Experimental evaluation	28

4.3.1	Performance analysis varying capacitance & processor frequency	28
4.3.2	Energy distribution analysis	31
4.3.3	Impact of capacitance & processor frequency on energy	34
4.3.4	Trade-off between energy consumption and performance	35
4.4	Implementation constraints and alternative implementation	37
4.5	Summary	38
5	Fault-Tolerant Heterogeneous Caches	39
5.1	Motivation	40
5.2	Bank-based HER cache	41
5.2.1	High-performance mode	42
5.2.2	Design issues: manufacturability and low voltages	44
5.2.3	Low-power working behavior	45
5.2.3.1	Read hit in the SRAM way	45
5.2.3.2	Write hit in the SRAM way	47
5.2.3.3	Read/Write hit in an eDRAM way	47
5.2.3.4	Cache miss	48
5.2.4	Mode changes	48
5.3	Timing details	49
5.4	Experimental results	50
5.4.1	Performance evaluation	50
5.4.1.1	Performance and retention time analysis	51
5.4.1.2	Hit rate evaluation	53
5.4.2	Power and energy consumption	53
5.4.3	Area	55
5.5	Summary	57
6	Trade-offs between SRAM Failures and Operation Modes	59
6.1	Background on SRAM cell failures	60
6.1.1	Hold failure	61
6.1.2	Read failure	61
6.1.3	Write failure	61
6.1.4	Access failure	62
6.2	SRAM cell failure characterization	62
6.2.1	Impact of the power supply on the failure probabilities	63
6.2.2	Impact of the WL pulse length on write and access failures	63
6.3	Optimal voltage/frequency pairs in fault-tolerant caches	66
6.3.1	Operation modes	67
6.3.2	Experimental evaluation	68
6.3.2.1	Performance	69
6.3.2.2	Energy Consumption	70
6.4	Summary	72
7	Conclusions	75
7.1	Contributions	76
7.2	Future Directions	77

7.3 Publications	77
References	79