Contents

Acknowledgements **i**

Abstract **v**

Resumen **ix**

Resum **xiii**

Contents **xvii**

List of Figures **xxvii**

List of Tables **xxxv**

1 Introduction **1**
- 1.1 Motivation 1
- 1.2 From Landell to Digital Television in a Glance 2
  - 1.2.1 DTV First Efforts and Tests 2
  - 1.2.2 The R&D Efforts 3
  - 1.2.3 The Decision and Some Numbers 3
  - 1.2.4 How DTV Influenced the Brazilian Industry of Broadcasting . 4
- 1.3 The National Program on Microelectronics and the Ambitions of the Brazilian Government 5
- 1.4 Thesis Objectives 6
- 1.5 Outline of the Thesis and Survey of the Contributions 7
- 1.6 Summary of my Main Roles and Responsibilities on ISDB-T and DVB-S2 Receivers Projects 10

2 Wireless Communications Basics **13**
- 2.1 OFDM - Orthogonal Frequency Division Multiplex 14
  - 2.1.1 OFDM Advantages and Drawbacks 19
    - 2.1.1.1 Advantages of OFDM 20
      - 2.1.1.1.1 High Spectral Efficiency 20
      - 2.1.1.1.2 One Tap Equalization 20

2.1.1.1.3 Robust Against ISI 21
2.1.1.1.4 Resistance Against Fading and Narrowband Interference 21
2.1.1.1.5 Efficient Implementation Using FFT 21
2.1.1.1.6 Low Sensitivity to Time Synchronization Errors 22
2.1.1.1.7 SFN and Macrodiversity 22
2.1.1.2 Disadvantages of OFDM 22
2.1.1.2.1 Sensitivity to Doppler Shift 22
2.1.1.2.2 Sensitive to Frequency Synchronization Errors 22
2.1.1.2.3 Sensitive to Phase Noise 23
2.1.1.2.4 Loss of Efficiency Due to GI 23
2.1.1.2.5 High PAPR 23
2.2 Wireless Channels 24
2.2.1 Small-Scale Fading 25
2.2.1.1 Power Delay Profile 27
2.2.1.2 Excess Delay 27
2.2.1.2.1 Maximum Excess Delay 27
2.2.1.3 Mean Delay 28
2.2.1.4 RMS Delay Spread 28
2.2.1.5 Coherence Bandwidth 29
2.2.1.6 Doppler Shift 30
2.2.1.7 Doppler Spread 31
2.2.1.8 Coherence Time 31
2.2.1.9 Types of Small-Scaling Fadings 32
2.2.1.9.1 Fadings Due to Multipath Time Delay Spread 32
2.2.1.9.1.1 Flat Fading 33
2.2.1.9.1.2 Frequency Selective Fading 33
2.2.1.9.2 Fadings Due to Doppler Spread 33
2.2.1.9.2.1 Fast Varying Fading 34
2.2.1.9.2.2 Slow Varying Fading 34
2.2.1.10 Large-Scale Fading 34
2.2.1.10.1 Shadowing 36
2.2.1.10.1.1 Log-Normal Distribution 36
2.2.1.10.2 Path Loss 36
2.2.1.10.2.1 Typical Urban 36
2.2.1.10.2.2 Typical Suburban 37
2.2.1.10.2.3 Rural 37
2.2.1.10.3 Small Scaling Fading 38
2.2.1.10.3.1 Rice Distribution 38
2.2.1.10.3.2 Rayleigh Distribution 38
2.2.1.10.3.3 Nakagami Distribution 39
2.2.1.10.3.4 Other Distributions 39
2.2.1.11 Reception Scenarios for Wireless Channels 39
2.2.2 Main RF Analog Front-End Impairments 41

2.2.2.1 Radio Conversion Architectures Impairments 42
2.2.2.2 A Second Look at RF Analog Front-End and Wireless Chanel Impairments 42
2.2.2.2.1 Non-Linearity 44
2.2.2.2.2 Power Amplifier Distortion 45
2.2.2.2.3 Phase Noise 45
2.2.2.2.4 Carrier Frequency Offset 46
2.2.2.2.5 Sampling Clock Offset 47
2.2.2.2.6 Timing Synchronization Errors 47
2.2.2.2.7 I&Q Imbalance or I&Q Mismatch 48
2.2.2.2.8 DC Offset 48
2.2.2.2.9 Additive Noise 49
2.2.2.2.9.1 Noise Figure and Sensitivity 49
2.2.2.2.10 Multipath 50
2.2.2.2.11 Quantization Noise and Limited Bit Length . 50
2.2.2.2.12 Quantization Clipping (Saturation) 51

3 ISDB-T and DVB-S2 Standards 53
3.1 ISDB-T Standard Basics 54
3.1.1 ISDB-T a First Look 54
3.1.2 ISDB-T a Detailed View 57
3.1.2.1 Transport Stream Re-multiplexer (Remux) 57
3.1.2.2 Reed Solomon Encoder 58
3.1.2.3 Hierarchical Layer Divider 58
3.1.2.4 Bytes to Bit 59
3.1.2.5 Energy Dispersal 59
3.1.2.6 Delay Adjustment 59
3.1.2.7 Bits to Byte 59
3.1.2.8 Byte Interleaving 59
3.1.2.9 Byte to Bits 61
3.1.2.10 Convolutional Coding 61
3.1.2.11 Carrier Modulation 62
3.1.2.11.1 DQPSK 63
3.1.2.11.2 QPSK 63
3.1.2.11.3 16-QAM 65
3.1.2.11.4 64-QAM 66
3.1.2.11.5 NORMALIZATION FACTOR 66
3.1.2.11.6 Data Segment 68
3.1.2.12 Hierarchical Layer Combining 69
3.1.2.13 Time Interleaving 70
3.1.2.14 Frequency Interleaving 73
3.1.2.14.1 Intersegment Time Interleaving 74
3.1.2.14.2 Intrasegment Interleaver 74
3.1.2.14.2.1 Intrasegment Carrier Rotation 78
3.1.2.14.3 Intrasegment Carrier Randomizer 78

3.1.2.15 OFDM Frame Structure 82
    3.1.2.15.1 OFDM Segment for Differential Modulation 82
    3.1.2.15.2 OFDM Segment for Coherent Modulation . . 82
3.1.2.16 Pilot and Control Signals 84
    3.1.2.16.1 Scattered Pilot (SP) 84
    3.1.2.16.2 Continual Pilot (CP) 87
    3.1.2.16.3 TMCC 87
    3.1.2.16.4 AC 88
    3.1.2.16.5 Transmission Spectrum 88
    3.1.2.16.6 IFFT and GI 89
3.1.2.17 TMCC Fields 89
    3.1.2.17.1 Synchronization Word 90
    3.1.2.17.2 Segment Type Identification 90
    3.1.2.17.3 TMCC Information 90
        3.1.2.17.3.1 System Identification 91
        3.1.2.17.3.2 Transmission Parameter Switching . . 91
        3.1.2.17.3.3 Emergency Alarm Broadcast Flag . . 91
        3.1.2.17.3.4 Current and Next Information 92
        3.1.2.17.3.5 Phase-Shift Correction for Terrestrial Audio Broadcasting 92
        3.1.2.17.3.6 Parity Bits 92
3.2 DVB-S2 Standard Basics 92
  3.2.1 DVB-S2 a Detailed View 93
    3.2.1.1 Mode Adaptation 93
        3.2.1.1.1 Input Interface 93
        3.2.1.1.2 Input Stream Synchronizer 95
        3.2.1.1.3 Null Packets Deletion 95
        3.2.1.1.4 CRC-8 Encoder 95
        3.2.1.1.5 Merger/Slicer 96
        3.2.1.1.6 Base Band Header (BBHEADER) 96
    3.2.1.2 Stream Adaptation 97
        3.2.1.2.1 Base Band (BB) Scrambling 97
    3.2.1.3 FEC Encoding Subsystem 97
        3.2.1.3.1 BCH Encoder 97
        3.2.1.3.2 Low Density Parity Check (LDPC) Encoder 98
        3.2.1.3.3 Bit Interleaver 102
    3.2.1.4 Bit Mapping 102
        3.2.1.4.1 16APSK 104
        3.2.1.4.2 32APSK 104
    3.2.1.5 Physical Layer (PL) Framing 105
        3.2.1.5.1 Dummy PLFRAME Insertion 107
        3.2.1.5.2 PL Signaling 108
            3.2.1.5.2.1 Start-Of-Frame (SOF) Field 108
            3.2.1.5.2.2 MODCOD Field 108
            3.2.1.5.2.3 TYPE Field 109

3.2.1.5.2.4 PLS Code 109
3.2.1.5.3 Pilots Insertion 109
3.2.1.5.4 Physical Layer Scrambling 111
3.2.1.6 Base Band Shaping 111
3.2.2 DVB-S2X: the Future of DVB-S2 113

4 The ISDB-T Receiver Design Methodology 115
4.1 Overview of the Methodology 115
4.2 Receiver Design Steps 116
4.2.1 Transmitter Model and Impairments Generation 118
4.2.1.1 ISDB-T Transmitter Model 118
4.2.1.2 Impairments Generation 118
4.2.2 Receiver Architecture and Model 119
4.2.2.1 System Level Architecture Specification 119
4.2.2.2 Algorithm and Block Design In Octave and Matlab . 120
4.2.3 Digital Front-End Design and FPGA Prototyping 121
4.2.3.1 Block Specification 121
4.2.3.2 Block Design 121
4.2.3.3 Block Verification 122
4.2.3.4 FPGA Physical Verification of Blocks 122
4.2.3.5 Receiver Integration 123
4.2.3.6 FPGA Physical Verification of the Receiver 123
4.2.3.7 Real data generation and capturing 124
4.2.4 ASIC Design Flow 124
4.2.4.1 Synthesis 124
4.2.4.2 Gate level post-synthesis verification 125
4.2.4.3 Physical design 125
4.2.4.4 Gate level post-physical design verification 125
4.2.4.5 Physical IC in 65 nm 126
4.2.5 System Test and IC Characterization 126

5 The Proposed ISDB-T Receiver Architecture and Algorithms 127
5.1 Introduction 127
5.2 An Architecture for an IF Digital Receiver for ISDB-T Signal Reception 129
5.3 The Digital Receiver Algorithms in Details 133
5.3.1 CORDIC Algorithm 133
5.3.1.1 The CORDIC Algorithm 133
5.3.2 Time Synchronization 137
5.3.2.1 Effects of Timing Offset 137
5.3.2.2 Symbol Boundary Detection, Coarse Fractional Carrier Frequency Offset Estimation and, Mode and GI Detection Algorithm 141
5.3.2.2.1 Detection of Coarse and Fine Symbol Boundaries, Mode and GI 141
5.3.2.2.2 Coarse Fractional CFO Estimation 144

- 5.3.3 Fine and Integer Carrier Frequency Offset . . . 146
  - 5.3.3.1 The Effects of ICFO and RCFO . . . 146
  - 5.3.3.2 ICFO Estimation . . . 149
- 5.3.4 Joint RCFO and SCO Estimator . . . 151
  - 5.3.4.1 Estimation of RCFO and SCO . . . 153
  - 5.3.4.2 Correction of RCFO and SCO . . . 159
    - 5.3.4.2.1 Farrow Interpolation Advantages and Disadvantages . . . 164
- 5.3.5 Frequency Domain Equalizer . . . 165
  - 5.3.5.1 The Channel Estimator and the Equalization . . . 165
- 5.3.6 Soft-Demapper With CSI . . . 171
  - 5.3.6.1 The Soft Bits Computation . . . 173
    - 5.3.6.1.1 QPSK . . . 173
    - 5.3.6.1.2 16-QAM . . . 173
    - 5.3.6.1.3 64-QAM . . . 173
    - 5.3.6.1.4 QPSK . . . 174
    - 5.3.6.1.5 16-QAM . . . 174
    - 5.3.6.1.6 64-QAM . . . 174
- 5.3.7 Joint TMCC Detection and Frame Synchronization . . . 175
- 5.3.8 SNR Estimator . . . 177
- 5.3.9 Soft Time Deinterleaver . . . 177
- 5.3.10 BER Estimator . . . 178
  - 5.3.10.1 Post Viterbi Decoder Bit Error Rate (BER) . . . 178
  - 5.3.10.2 Post Reed-Solomon BER . . . 178
- 5.4 Simulation Results . . . 179
  - 5.4.1 Performance Over Brazil-A and Brazil-B Wireless Channels . . 180
  - 5.4.2 Performance Under Impulsive Noise . . . 184
  - 5.4.3 ADC Quantization Effects in the Performance . . . 185
  - 5.4.4 SCO, RCFO and Fine Boundary Convergence . . . 186
- 5.5 Conclusions . . . 186

6 ISDB-T Receiver: VLSI Implementation, FPGA Prototype and Test Results **189**
- 6.1 Introduction . . . 189
- 6.2 VLSI Implementation in 65 nm CMOS . . . 191
  - 6.2.1 Physical Synthesis . . . 191
  - 6.2.2 Physical Design . . . 191
  - 6.2.3 Memory Area . . . 193
  - 6.2.4 DTV01 Demo Board . . . 194
  - 6.2.5 Mini PCI Based DTV01 Demo Board and Multi-Chip-Module(MCM) 194
- 6.3 FPGA Prototype . . . 196
- 6.4 Test Environment . . . 199
- 6.5 Experimental Results . . . 202
- 6.6 Conclusions . . . 205

7 The Proposed DVB-S2 Receiver Architecture and Algorithms 207
7.1 Introduction . . . 207
7.2 Architecture for an IF Digital Receiver for DVB-S2 Signal Reception . 208
7.2.1 The Current Implemented Architecture . . . 208
7.2.1.1 Signal Processing . . . 211
7.2.1.2 Data Processing . . . 212
7.2.2 The Final Architecture . . . 213
7.3 The Digital Receiver Algorithms in Details . . . 215
7.3.1 Timing Recovery . . . 215
7.3.2 Frame Synchronization and PLS Decoding . . . 216
7.3.2.1 Frame Synchronization and PLS Decoding . . . 217
7.3.2.1.1 Acquisition . . . 217
7.3.2.1.2 Peak Search . . . 219
7.3.2.2 PLS Decoding . . . 221
7.3.2.3 The Proposed Implementation Architecture . . . 224
7.3.3 Coarse and Fine Frequency Estimation (CFE and FFE) and Correction . . . 224
7.3.3.1 Coarse Frequency Estimation and Correction . . . 225
7.3.3.2 Fine Frequency Estimation and Correction . . . 226
7.3.3.2.1 The Proposed Architecture . . . 229
7.3.3.2.2 Simulations . . . 231
7.3.4 Coarse Phase Estimation and Correction . . . 233
7.3.5 Digital Automatic Gain Control (AGC) . . . 234
7.3.6 Physical Layer Descrambler - PL Descrambler . . . 235
7.3.7 Adaptive Equalizer . . . 236
7.3.7.1 Proposed Equalizer Architecture . . . 238
7.3.7.1.1 FIR-LMS Core . . . 240
7.3.7.1.2 Error Tracking . . . 241
7.3.7.1.3 CMA . . . 242
7.3.7.1.4 Decision Device . . . 242
7.3.7.2 Simulation Results . . . 243
7.3.7.2.1 Inter Symbol Interference - ISI . . . 243
7.3.7.2.2 TWTA Nonlinear Effect . . . 247
7.3.8 SNR Estimator . . . 250
7.3.9 Soft and Hard-Decision Demappers . . . 252
7.3.9.1 Hard-Decision Demapper . . . 253
7.3.9.2 Soft Demapper (SD) . . . 254
7.3.9.3 Proposed Architecture . . . 255
7.3.9.3.1 Hard Demapper . . . 255
7.3.9.3.2 Soft Demapper . . . 257
7.3.10 FEC Subsystem and BER Measurement Platform . . . 258
7.3.10.1 Deinterleaver . . . 260
7.3.10.2 LDPC Decoder . . . 261
7.3.10.3 BCH Decoder . . . 264
7.3.10.4 Platform for FEC Subsystem BER Measurement . . 266

7.4 Conclusions 268

8 DVB-S2 Receiver: The Methodology, VLSI Implementation, FPGA Prototype and Test Results 271

8.1 Introduction 271
8.2 The Methodology 273
8.3 Prototype in FPGA and VLSI Implementation in 65nm CMOS 275
  8.3.1 Full Receiver FPGA Prototyping 275
  8.3.2 Receiver VLSI Physical Synthesis 279
8.4 FEC FRAME Decoder: FPGA Prototype 280
8.5 Soft and Hard Demappers: FPGA Prototype and VLSI Physical Synthesis 282
8.6 Adaptive Equalizer: FPGA Prototype Results 284
8.7 Optimized Fine Frequency Estimator: FPGA Prototype Results . . . 284
8.8 Conclusions 285

9 Conclusions and Future Work 287

9.1 Fundamental Understanding on the Wireless Radio Impairments . . . 289
9.2 Proposal of a ISDB-T Receiver Architecture and Algorithms Exploration 290
9.3 ISDB-T Receiver: VLSI Implementation , FPGA Prototype and Test Results 291
9.4 Proposal of a DVB-S2 Receiver Architecture and Algorithms Exploration 291
9.5 DVB-S2 Receiver: FPGA Prototype, Early VLSI Design Exploration and Test Results 292
9.6 Creating and Proving the Competences for ASIC Implementation in Brazil 293
9.7 Future Works Directions 294

A List of Publications 297

B Digital Terrestrial Television Around The World 301

B.1 Digital Terrestrial Television Around The World 301
  B.1.1 First Generation of Digital Television 302
    B.1.1.1 Digital Video Broadcasting - Terrestrial (DVB-T) . . 302
      B.1.1.1.1 Mux Adaptation and PRBS Scrambling . . . 302
      B.1.1.1.2 Reed Solomon Encoding 302
      B.1.1.1.3 Byte-Wise Interleaving 303
      B.1.1.1.4 Convolutional Encoding 304
      B.1.1.1.5 Bit and Symbol Interleaving 304
      B.1.1.1.6 Constellation Mapping 308
      B.1.1.1.7 OFDM Frame Structure 311
    B.1.1.2 ATSC - Advanced Television Systems Committee Standards 316
      B.1.1.2.1 Transmission Data Organization 316
      B.1.1.2.2 Data Randomizing 317

B.1.1.2.3 Reed-Solomon Enconding 318
B.1.1.2.4 Convolutional Byte Interleaving 318
B.1.1.2.5 Trellis Coding and Intrasegment Symbol Interleaving 318
B.1.1.2.6 Data Segment Sync 322
B.1.1.2.7 Data Field Sync 322
B.1.1.2.8 VSB Modulation 323
B.2 Dedicated Mobile Digital Television Standards 324
B.2.1 DVB Transmission System for Handheld Devices (DVB-H) . . 324
B.2.1.1 Time-Slicing 325
B.2.1.2 MPE-FEC 325
B.2.1.3 4K mode and in-depth interleavers 325
B.2.1.4 DVB-H signaling 326
B.2.2 ISDB-T(1-SEG) 326
B.2.3 Terrestrial Digital Multimedia Broadcasting (T-DMB) 326
B.2.4 Chinese Mobile Multimedia Broadcasting - CMMB 327
B.3 Second Generation Digital Television and a Little About the Future of DTV 327
B.3.1 DVB-T2 327
B.3.2 The Future of Terrestrial DTV 329

C Semiconductor Area in Brazil **331**
C.1 An Historical View of Semiconductor Area in Brazil 331
C.1.1 The National Program on Microelectronics - PNM 332
C.1.1.1 Design Houses 334
C.1.1.2 Foundries 334
C.1.1.3 Package and Test 335
C.1.2 What PNM Has Achieved So Far 335

Bibliography **337**