A new Low Complexity Time Synchronization Algorithm for Optical OFDM PON System using a Directly Modulated DFB Laser

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***Abstract*—In this paper a low complexity time synchronization algorithm for Optical Orthogonal Frequency Division Multiplexing (OOFDM) is proposed. The algorithm is based on a repetitive preamble which allows the use of a short cross-correlator with a exponential average filter for post-processing before a threshold detection. The signals in the correlation have been quantized with 1 bit and the correlation have been implemented as a hard-wired tree adder to reduce the hardware cost. This solution has been verified in an optical communication test-bed achieving an excellent performance with low computing processing complexity even in low signal to noise ratio scenarios. Finally, a parallel hardware architecture has been proposed for this time synchronization algorithm and it has been implemented in a FPGA device reaching a sample rate throughput up to 7.4 Gs/s.**

***Index Terms*—Time synchronization; OOFDM: PON; FPGA implementation; Real-time signal processing.**

I. Introduction

The fast growing bandwidth demand in the access network market will not be supported by the current wired and wireless access techniques. Therefore, passive optical networks (PONs) are being widely adopted and implemented as a high-speed strategy for broad-band access due to their low cost, high reliability and easy maintenance. Orthogonal Frequency Division Multiplexing (OFDM) has been recently introduced into fiber communications due to its flexible dynamic bandwidth allocation, high spectral efficiency and strong resistance to chromatic dispersion (CD) [1, 2]. OFDM is a multicarrier modulation technique where each symbol is composed of N samples which are generated by performing an N-point inverse fast Fourier transform (IFFT) on N complex data symbols. OFDM systems are very sensitive to errors in time and frequency synchronization. A time synchronization algorithm (TSA) must estimate where the fast Fourier transform (FFT) window begins to cover only N samples belonging to the same OFDM symbol, avoiding in this way inter symbol interference (ISI) and inter-carrier interference (ICI).

In the last years, much research effort has been dedicated to develop time synchronization algorithms for OFDM systems for wireless environment [3–6] and references therein. However, these algorithms cannot be directly applied to optical OFDM (OOFDM) systems due to their high hardware computational complexity as OOFDM systems operate with throughputs of several Giga samples per second (Gs/s). To achieve such throughputs the algorithms must be implemented in hardware using highly parallelized architectures like Field Programmable Gate Arrays (FPGA) or Application-Specific Integrated Circuits (ASICs). So, the design of tailored high-speed, low-complexity OOFDM synchronization solutions with good accuracy is important for real time implementation of the OOFDM technique in next-generation, cost-effective, high-capacity transmission systems. Therefore, to make feasible the implementation of OOFDM systems using current technologies, it is mandatory to reduce as much as possible the computing complexity of the digital signal processing algorithms.

A simple symbol synchronization technique utilizing subtraction and Gaussian windowing has been proposed and implemented for OOFDM systems in [7, 8], where authors exploit the periodic structure of the cyclic prefix (CP) of OFDM symbols. Although they were originally designed for general OFDM systems, they can be adapted to be used in preamble-based OFDM systems where a known preamble is transmitted before the OFDM data symbols for synchronization and channel estimation purposes; nevertheless, a better performance can be obtained by using algorithms that take advantage of the known preamble structure as in [9–12]. In [9] authors make use of an autocorrelation of the incoming signal scaled by the signal power to detect the beginning of the training sequence. Another approach is to replace the autocorrelation by a cross-correlation and eliminate the division by the received signal power [10–12].

In this paper we have developed a time synchronization algorithm for real-time intensity modulation and direct-detection (IM/DD) preamble-based OOFDM reception system. In order to achieve a hardware efficient implementation of this algorithm, we propose a novel N_p-parallel symbol synchronization method based on a designed preamble with a repetitive structure in time domain, this TSA performs a cross-correlation between the known preamble and the received data without using multipliers. The use of a repetitive preamble allows us to employ a shorter cross-correlator than the one used in works cited above, which results in a lower hardware complexity implementation. To test our algorithm we implemented an experimental setup over 100 km standard single-mode fiber (SSMF) using a digital analog converter (DAC) operating at 4 Gs/s to generate the test signals and the photoreceiver output is captured with a digital oscilloscope working at 20 Gs/s and stored for offline processing. Thanks to the parallel pipelined architecture and its low hardware cost, the proposed algorithm has been successfully implemented in a Xilinx Virtex-7 FPGA device working at more than 7 Gs/s.

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The paper is organized as follows. In Section II the proposed time synchronization algorithm is described. Section III presents the experimental setup used to evaluate our TSA and the obtained results. Section IV describes the hardware implementation and comparisons with other algorithms from the literature. Finally, conclusions are given in Section V.

II. Proposed Algorithm

In a previous work we proposed a synchronization technique for wireless OFDM systems using cross-correlation with a repetitive preamble [6]. The main problem of the solutions designed for wireless systems is the difficulty to work at sample rates of Gs/s which are usual in IM/DD OOFDM systems. Thus, we take the idea of employing a repetitive preamble from [6] to reduce the cross-correlation complexity, but we have developed a new solution for the post-processing of the cross-correlator output to reduce the hardware cost maintaining a good performance. The block diagram of the proposed time synchronization algorithm is shown in Fig. 1. After quantization, the input signal is cross-correlated with the known preamble and the result is processed by an exponential average filter. Finally, there is a threshold detection block to find the peak of the filter output.

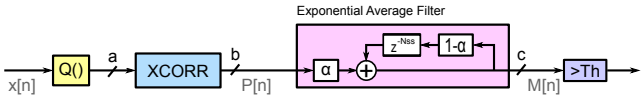

Fig. 1. Implementation for the proposed TSA.

The preamble structure used in this work for OOFDM is shown in Fig. 2. It consists of 8 identical short symbols (SS) of N_{ss} samples and 2 identical long symbols (LS) of N samples each one preceded by a guard interval (GI) composed of $2N_{cp}$ samples from last samples of the LS. Where N_{cp} is the size of the cyclic prefix, N_{ss} is the size of a SS and is equal to $N/8$, and N is the size of the IFFT. The length of the cyclic prefix must be at least equal to the length of the channel dispersion and this value does not affect the proposed TSA. In this work we have worked with an FFT size of 256 and a CP of 32 samples long. This structure is similar to the one used by WLAN standard IEEE 802.11 a/g [13, 14]. The first part of the preamble composed of 8 SS can be used to detect the presence of the signal, to estimate the beginning of the OFDM data symbols, to manage the distortion in the early samples of the preamble during the settling time of the automatic gain control (AGC) stage, and to estimate the carrier frequency offset (CFO). Although in IM-DD optical systems a real valued baseband OFDM signal is usually employed and CFO is not present, the use of a repetitive preamble makes it feasible to use radiofrequency (RF) modulated OOFDM signals, where the RF sections in transmission and reception may introduce CFO. This transmission scheme, where the OFDM signal is generated by using quadrature and in-phase branches modulating an RF sin/cos carrier, can double the data rate by using another couple of ADC/DAC without doubling the sampling rate specifications of the converters. Finally, channel estimation can be accurately achieved using the long symbols.

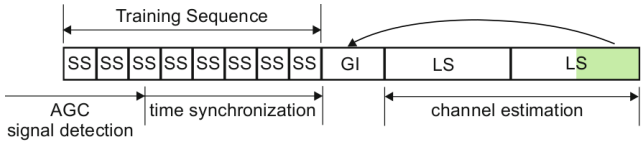

Fig. 2. Proposed preamble structure with 8 short symbols and 2 long symbols.

The repetitive part of the preamble with 8 SS, also called training sequence (TS) along the paper, is generated by modulating one of every 8 subcarriers (from subcarrier 1 to $N/2-1$) with quadrature phase shift keying (QPSK) symbols, while the remaining subcarriers are filled with zeros before using the IFFT. As the generated signal must be composed of real valued samples, it is necessary that subcarriers from -1 to $-N/2+1$ have Hermitian symmetry around direct current (DC) subcarrier: it implies that only $N/8$ of N total subcarriers are not zero, and DC carrier is used to bias the laser. The length of the training sequence N_{ts} is equal to the FFT length N. In the experimental measurements we have used the values $N = 256$ and $N_{ss} = 32$ because they facilitate the parallel implementation of the algorithm, as will be discussed below.

From an implementation point of view a cross-correlator is a block with high complexity in optical communications, as it requires a large number of multipliers to process several Gs/s. To avoid this high computational cost it is possible to simplify its implementation with a scheme without multipliers [6] by means of a hard-wired tree adder, where the TS values are represented by their sign bit and the input signal $x[n]$ is quantized (Q()) with as less bits as possible. Then, the cross-correlation can be expressed as in Eq. (1), where sgn() is the sign function. This solution, i.e., the replacement of adders and multipliers by a hard-wired tree adder, is possible because the TS values are known and they determine the structure of the tree adder. We will show that it is also possible to quantize the input signal with one bit. A similar approach has also been employed in [11, 15] where the full multipliers have been substituted by XNOR multipliers and a tree adder, but that solution does not take into account that the TS is known by the receiver and more hardware resources are needed.

$$P[n] = \sum_{m=0}^{N_{ss}-1} \mathrm{Q}(x[n+m]) \cdot \mathrm{sgn}(SS[m]) \quad (1)$$

Only $N_{ss}-1$ real adders are needed to implement a cross-correlator as a hard-wired tree adder, whereas the traditional implementation requires N_{ss} real multipliers and $N_{ss}-1$ real adders. For example, if we use a $N_{ss} = 32$ and a SS with these signs $\{+1, +1, +1, +1, +1, -1, -1, +1, +1, +1, +1, -1, -1, -1, -1, -1, -1, -1, -1, -1, -1, -1, +1, +1, +1, -1, -1, -1, +1, -1, -1, -1\}$ the cross-correlator is implemented as shown in Fig. 3, where the box represents the last 4 terms of the cross-correlator calculated as Eq. (2). If we regroup these 4 terms to implement 2 steps hard-wired tree adders, we obtain Eq. (3).

$$\mathrm{Q}(x[n+28]) - \mathrm{Q}(x[n+29]) - \mathrm{Q}(x[n+30]) - \mathrm{Q}(x[n+31]) \quad (2)$$

$$\{\mathrm{Q}(x[n+28]) - \mathrm{Q}(x[n+29])\} - \{\mathrm{Q}(x[n+30]) + \mathrm{Q}(x[n+31])\} \quad (3)$$

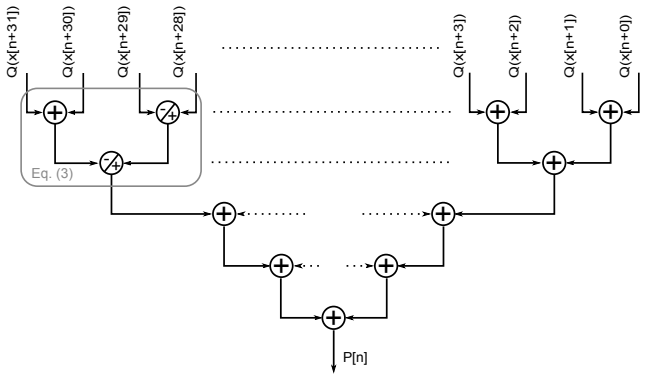

Fig. 3. Block diagram of cross-correlator.

The cross-correlator generates a periodic peak at its output when the TS is at its input, then, we make use of the exponential average filter in Eq. (4) to enhance these peaks and reduce the background noise: the amplitude of peaks generated when SS is present grows and the amplitude of other spurious peaks decreases because the filter averages the actual cross-correlator output ($P[n]$) with the filter output delayed N_{ss} samples ($M[n-N_{ss}]$). The average filter also avoids false detections when the input is not the TS and the background noise is high. Moreover, thanks to this average filter the peaks at the output vanish quickly once the TS ends, because now in $P[n]$ there is no periodic peak. So, the implementation of a threshold detector to find the last peak is simplified as the difference between the periodic peak and the spurious peaks is high. By using $\alpha = 0.5$ both products in the average filter can be implemented by a bit shift operation, and the hardware cost is reduced.

$$M[n] = \alpha \cdot P[n] + (1-\alpha) \cdot M[n-N_{ss}] \tag{4}$$

The output of this averaged cross-correlation has 8 major peaks, each one coinciding with the presence of the last SS sample at the cross-correlator input, as can be seen in Fig. 4. The last peak is used as a reference for time synchronization: once the TS has entered the cross-correlator it is expected a peak every N_{ss} samples, when it disappears it means the GI has started and therefore the last peak has been found. Once its location is found, it is used to select the incoming $2(N_{cp}+N)$ samples from $x[n]$ that correspond to the LS part of the preamble, then the LS is employed to estimate the channel response. The reference peak can be detected by setting a threshold value at the output of the filter and using a small control logic; this threshold is selected in the same way as in [6].

A. Finite Precision Analysis

We have developed a fixed-point model of the TSA where signals are quantized with the following number of bits: a for correlation input data, b for filter input data and c for filter output data, as shown in Fig. 1. As the filter is an exponential recursive one, c can have the same width as b. However, b depends on the input width a and the growth of the N_{ss} terms to be added in the correlator: $b = a + \log_2(N_{ss})$. The performance of the time synchronization algorithm with different quantization values has been evaluated by simulation, and later these results have been validated in a real experiment. Thus, 10^4 preambles have been generated and transmitted through an additive white Gaussian noise

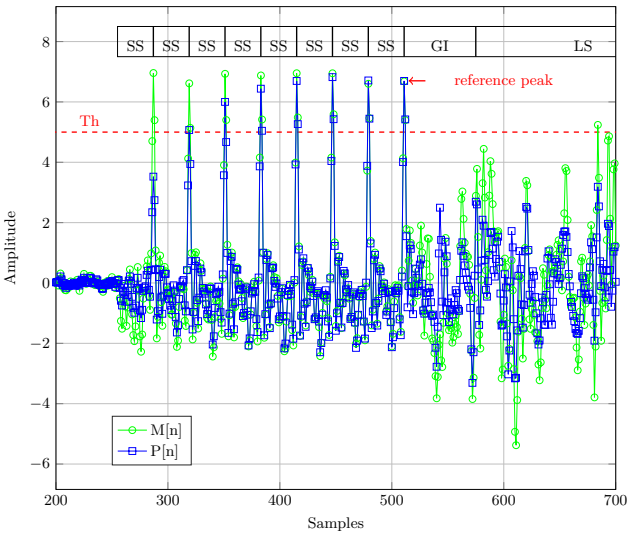

Fig. 4. Magnitude of the cross-correlator ($P[n]$) and filter ($M[n]$) output during the repetitive part of the preamble and at the beginning of the guard interval. TS with 8 SS and $N_{ss} = 32$.

(AWGN) channel. At the receiver side, the probability of correct time detection (PCTD) has been computed as:

$$\text{PCTD} = \frac{\text{Number of correct timing offset acquisitions}}{\text{Number of total timing offset acquisitions}} \tag{5}$$

where correct time detection is considered when the TSA detects a peak at the last sample of the TS, or one sample before or one sample after.

Simulation results for $N_{ss} = 32$ are shown in Fig. 5. It is clearly observed that the PCTD of the proposed method does not depend on a for SNR > 3 dB; for example, as a reference, it is necessary a channel with a SNR of 3.6 dB to obtain a BER value of 10^{-2} if a QPSK modulation scheme is employed. So, we can expect a good performance ($PCTD \approx 1$) of the TSA using an input signal quantized with 1 bit ($a = 1$, that is using the sign bit of the received signal) in practical scenarios where the SNR would be higher, then the growth in the number of quantization bits in the cross-correlator would give $b = c = 6$ for $N_{ss} = 32$. As the hardware cost of digital signal processing has a strong dependence with the number of quantization bits, these low values allow us to obtain a low cost hardware implementation. We have taken the BER value of 10^{-2} as a reference because it is commonly considered a forward error correction (FEC) threshold to obtain an error free transmission when a soft decision FEC coding with 20% redundancy is employed [16]; on the other hand, in case a hard decision FEC coding with 7% redundancy were employed, the FEC threshold would be 3.8×10^{-3} [17], which corresponds with a SNR of 4.9 dB.

III. Experimental Setup and Results

A. Experimental setup

In this experiment the number of OFDM subcarriers is set to $N = 256$, but due to the Hermitian symmetry only 128 are defined: 112 transport data, 15 are used for frequency guard interval and DC is used to bias the laser. The CP length is $1/8$ of an OFDM period, *i.e.*, 32 samples in every OFDM symbol. Data subcarriers are modulated with QPSK symbols. The OFDM samples are generated offline using

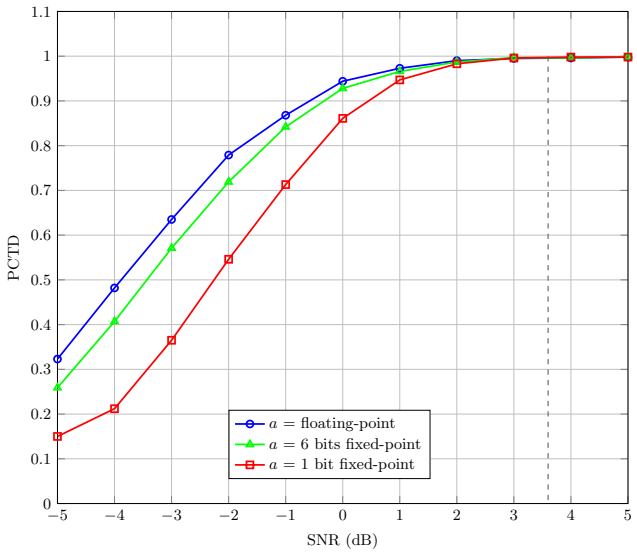

Fig. 5. Curves of probability of correct time detection of our TSA ($N_{ss} = 32$) versus SNR for different received data quantification schemes and the marker for 10^{-2} BER.

MATLAB and they are sent to a Maxim DAC MAX19693 (12 bits) operating at 4.0 Gs/s to produce the required analog electrical signal. As a result of these settings the bit rate in our experiment is 3.11 Gb/s. First, the electrical OFDM signal is low pass filtered (LPF) and then passes through an electrical amplifier (EA) before optical conversion. A single-mode 1550 nm directly modulated linear optically isolated distributed feedback (DFB) laser is driven by the amplified electrical OFDM signal with a +3 dBm optical output power. Before the photoelectric conversion, the power of the detected optical OFDM signal can be changed by a variable optical attenuator (VOA). The received base-band OFDM signal is obtained via a high performance InGaAs photodiode (PD) with a bandwith of 3.0 GHz. The converted electrical OFDM signal is preamplified by an EA and is sampled at 20 Gs/s by a Tektronix DPO TDS7154B (8 bits) and stored for offline processing in MATLAB. Fig. 6 shows the experimental setup for the IM/DD OOFDM transmission system over 100 km SSMF.

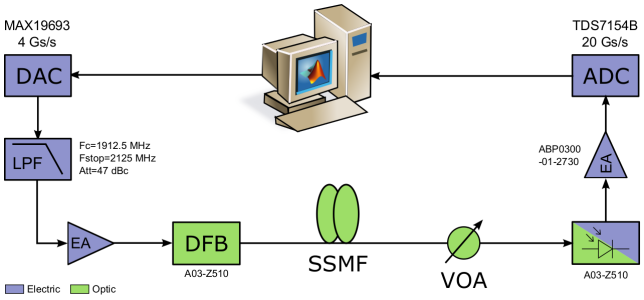

Fig. 6. Experimental setup for the IM/DD OOFDM transmission system.

B. Results

The proposed time synchronization algorithm with a preamble composed of 8 SS of $N_{ss} = 32$ samples has been evaluated in the setup shown in Fig. 6 and its performance has been compared with the ones obtained by other two time synchronization algorithms: the first one was proposed by Park [5] for wireless channels and it is based on the autocorrelation of the received signal; and the second one was proposed in [12] for OOFDM and it is based on a cross-correlation. Fig. 7 and Fig. 8 show the probability of obtaining a correct time detection versus the received optical power for a back-to-back (BTB) connection and after transmission through 100 km SSMF, respectively. These results have been obtained transmitting 1200 OFDM test frames for each algorithm and for each received power. Fig. 9 shows the curves of BER versus received optical power for back-to-back and after 100 km SSMF, in both curves the received optical power needed to obtain a FEC threshold BER of 10^{-2} have been highlighted. The BER results have been calculated for correctly detected frames, in this case all the time synchronization algorithms give the same results and the figure characterizes the behavior of the complete system after synchronization.

It can be seen that all three synchronization algorithms can accurately synchronize in time for the BER value of reference, although Park's method has a poorer performance for low values of received optical power. Both methods using cross-correlation have better performance, but Chen's one is a bit better thanks to its larger correlation size. Nevertheless, the difference between both algorithms in the 100 km experiment appears only for received optical power levels below -23 dBm, corresponding to BER values poorer than 10^{-1}; that is to say, corresponding to optical power levels which are not useful in a real scenario. Same behavior can be noticed in the BTB case.

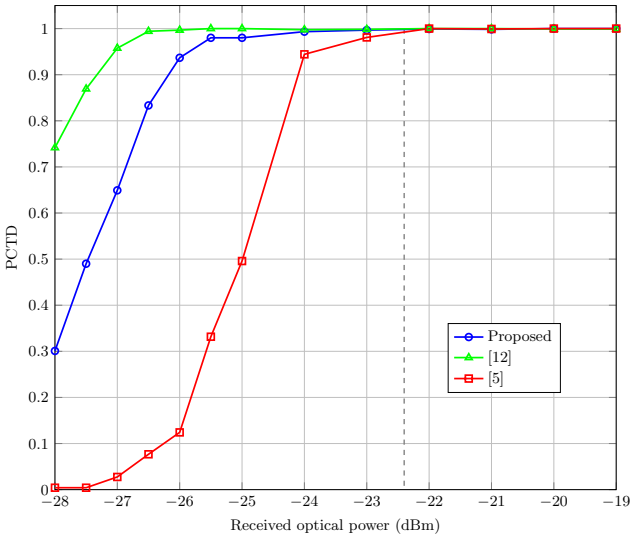

Fig. 7. Curves of probability of correct time detection versus the received power for the back-to-back case and the marker for 10^{-2} BER.

IV. Hardware Implementation

The real time OFDM receiver has been implemented on a Xilinx Virtex-7 VC707 evaluation board and a 4DSP FMC126 ADC card. The first board is equipped with a XC7VX485T-2 FPGA chip (with a maximum clock frequency of 650 MHz) and the second board is equipped with an E2V 10-bit EV10AQ190 ADC chip allowing a maximum sampling rate of

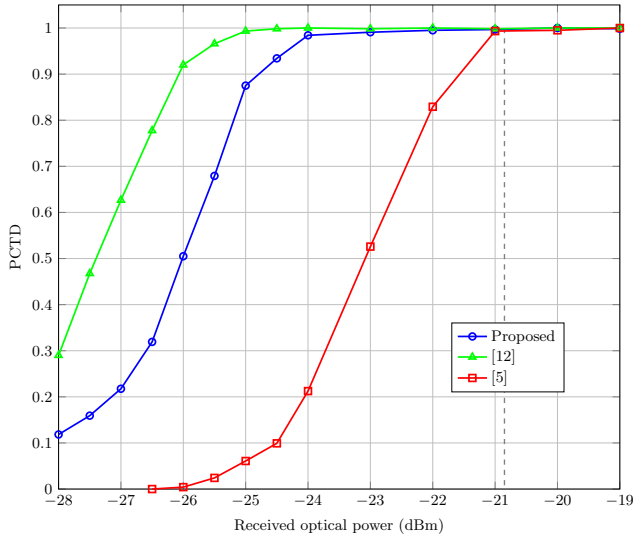

Fig. 8. Curves of probability of correct time detection versus the received power after transmission over 100 km SSMF and the marker for 10^{-2} BER.

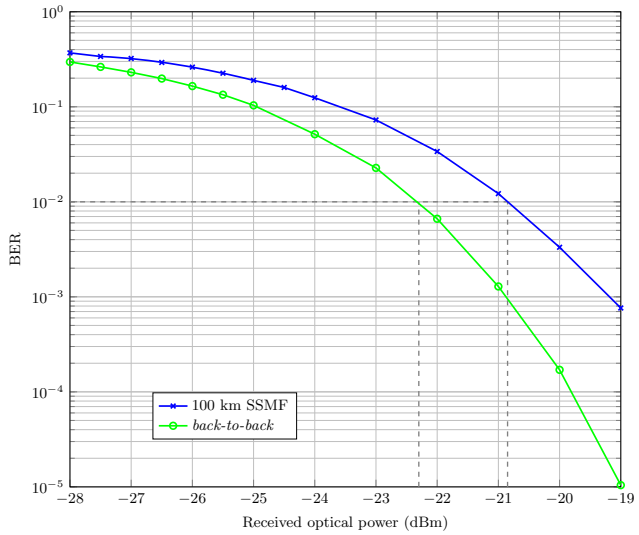

Fig. 9. Curves of BER versus the received power for the back-to-back case and after transmission over 100 km SSMF.

5 Gs/s. The EV10AQ190 ADC sends to the FPGA 4 sampled data at the same time in dual data rate (DDR) mode via 40 low-voltage differential signaling (LVDS). The FPGA has a dedicated serial-to-parallel converter (ISERDES) which can create a 4-, 6-, 8- or 10-bit-wide parallel word. If the smallest bit-wide parallel word (4) is selected, 16 sampled data per clock cycle are obtained. Therefore to achieve a throughput of 5 Gs/s we need to process 16 channels in parallel using a clock frequency of 312.5 MHz.

The performance and the hardware cost of the TSA is affected by finite-precision issues in the representation of inner variables and the input signal. The finite precision analysis of our algorithm was presented in Sec. II-A. In the following sections we present its parallel implementation and compare the resources used by this implementation with other algorithms. Finally, we presented the implementation results for Virtex-7 XC7VX485T-2 FPGA.

A. Parallel TSA

The algorithm described in Eq. (1) and Eq. (4) is a single-input single-output (SISO) system. To obtain a parallel processing structure, the SISO system must be converted into a multiple-input multiple-output (MIMO) system using the *look-ahead* technique described in [18]. The Eq. (6) describes a parallel cross-correlation system with N_p inputs per clock cycle, where k denotes the clock cycle.

$$\begin{aligned} P[kN_p+0] &= \sum_{m=0}^{N_{ss}-1} \mathrm{Q}(x[kN_p+0+m]) \cdot \mathrm{sgn}(SS[m]) \\ P[kN_p+1] &= \sum_{m=0}^{N_{ss}-1} \mathrm{Q}(x[kN_p+1+m]) \cdot \mathrm{sgn}(SS[m]) \\ &\vdots \qquad\quad \vdots \qquad\qquad \vdots \qquad\quad \vdots \\ P[kN_p+N_p-1] &= \sum_{m=0}^{N_{ss}-1} \mathrm{Q}(x[kN_p+N_p-1+m]) \cdot \mathrm{sgn}(SS[m]) \end{aligned} \tag{6}$$

The N_p-parallel exponential average filter is described as:

$$\begin{aligned} M[kN_p+0] &= \alpha \cdot P[kN_p+0] + (1-\alpha) \cdot M[kN_p+0-N_{ss}] \\ M[kN_p+1] &= \alpha \cdot P[kN_p+1] + (1-\alpha) \cdot M[kN_p+1-N_{ss}] \\ &\vdots \qquad\quad \vdots \qquad\qquad\qquad\qquad \vdots \\ M[kN_p+N_p-1] &= \alpha \cdot P[kN_p+N_p-1] \\ &\quad + (1-\alpha) \cdot M[kN_p+N_p-1-N_{ss}] \end{aligned} \tag{7}$$

$N_p(N_{ss}-1)$ and N_p adders are needed to implement Eq. (6) and Eq. (7), respectively. For our purpose it is necessary to detect the last peak by setting a threshold value at the output of the N_p exponential average filters. The correct timing location is determined by the position of the last peak. To implement this task N_p comparators and one priority decoder are needed.

The parallel implementation of the TSA and the detailed signal processing flow is shown in Fig. 10 with $N_p = 16$ and $N_{ss} = 32$. This value of the N_{ss} parameter has been chosen as a trade-off between algorithm's performance and hardware complexity to simplify the N_p-parallel hardware architecture of the exponential average filter. If $N_{ss} < N_p$, there exists long feedback loops in the parallel recursive filter. In this case, the filter output depends on a previous output that is being computed in parallel; so, combinational paths are generated among outputs. These combinational paths exhibit long delays and usually are the critical paths that limit the maximum operating frequency in the algorithm implementation. On the other hand, if $N_{ss} > N_p$ but N_{ss} is not an integer multiple of N_p, an irregular hardware structure is obtained introducing routing delays and limiting the operating frequency. However, these problems are avoided if N_{ss} is chosen as an integer multiple of N_p. In such a case, each parallel output only depends on itself delayed by N_{ss}/N_p samples; so, the critical path is not increased and the hardware structure is regular as the N_p-parallel average filters can be implemented as N_p independent filters. For example, as in our case $N_p = 16$ this means that one delay in a branch gives a total delay of 16 samples. Therefore, to obtain the term $M[16k-32]$ in Eq. (7) we need to delay $M[16k]$ two times instead of 32 times. Samples $M[16k-32]$ and $M[16k]$ are outputs from the same filter, avoiding dependences among the 16 parallelized branches of the filter.

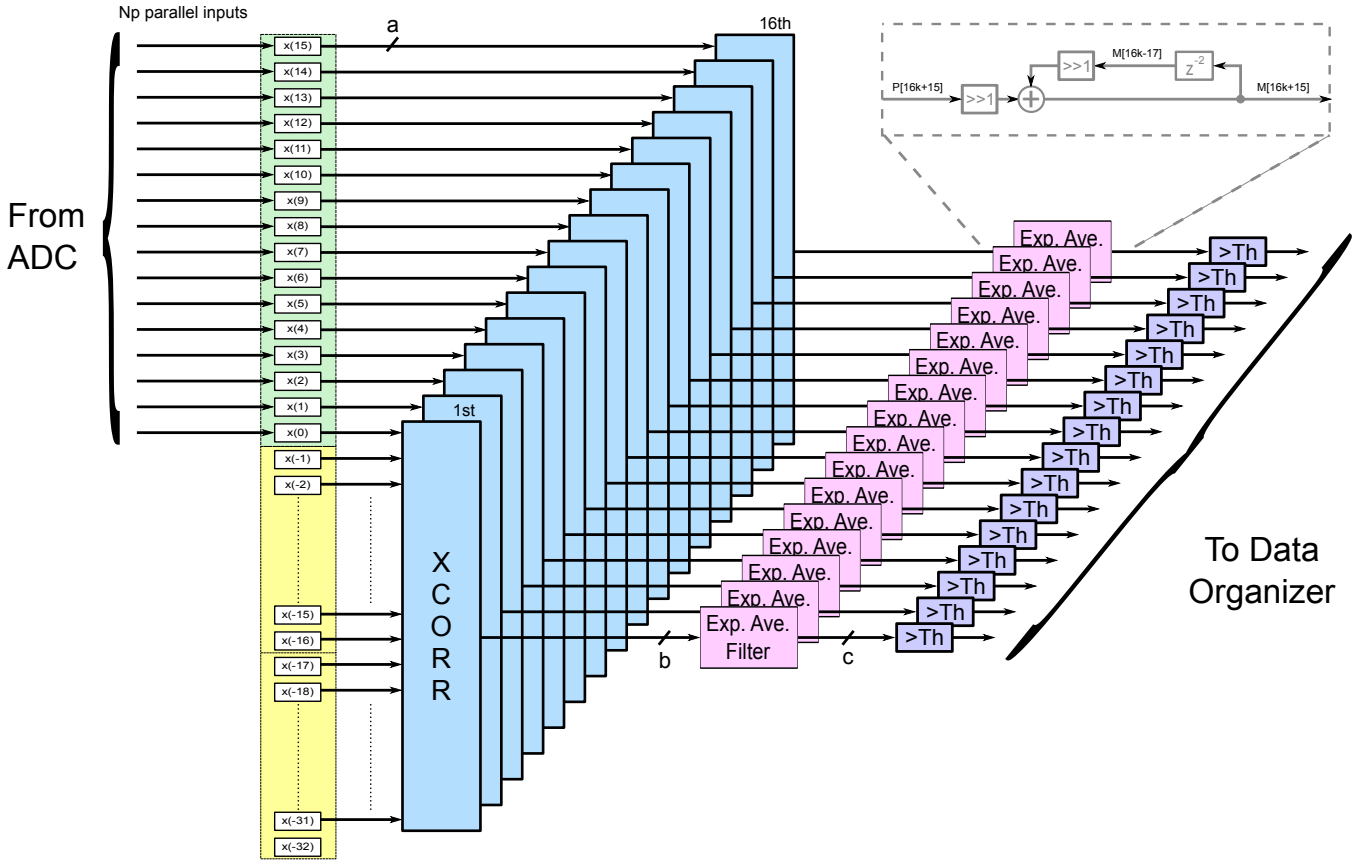

Fig. 10. Digital signal processing block diagram of parallel TSA with $N_p = 16$ and $N_{ss} = 32$.

B. Complexity Comparisons

The complexity of six hardware implementations of time synchronization algorithms is presented next. References [7, 8] are based on subtraction and Gaussian windowing of the CP, [9] is based on autocorrelation of the TS and [10–12] are based on cross-correlation of the TS. These implementations are used for high-speed OOFDM receiver systems and all algorithms process N_p samples in parallel. For a fair comparison of various time synchronization techniques, they are evaluated in an IM/DD OOFDM system with real valued OFDM signal generation and detection, in which only the symbol synchronization is considered. The algorithms presented in [9, 10] were designed for complex valued OFDM signals in coherent optical communications. We have estimated their computational cost when they are used with real valued OFDM signals to be able to compare them with the rest.

The algorithm proposed in [9] makes use of a repetitive preamble based on autocorrelation, it needs a special demultiplexed channel to reduce its computational cost. The size of the training sequence is equal to $8N$. In [10] a training sequence is generated with values randomly selected from the set of $\{-1, 1\}$. At the receiver side, the received data is cross-correlated with the training sequence. This correlation operation is implemented using additions and subtractions, so multiplication is removed and large area is saved. In [11, 12] the sign of the received data is cross-correlated with the sign of the training sequence, so multiplications are replaced by XNOR multipliers. In these algorithms the size of the TS is equal to $N_{cp} + N$.

The generation of the training sequence used by the proposed TSA has been described in section II. At the receiver side, the quantized received data are cross-correlated with the sign of the training sequence, this correlation is implemented using only additions and subtractions. It was shown in section II-A that using only 1-bit for quantizing the received signal preamble is enough to obtain a good performance for a BER value of 10^{-2}; this reduction in the number of bits dramatically reduces the computational cost.

In Table I the complexity of these time synchronization algorithms is shown, they can be classified in two groups depending on the use or not of multipliers. Moreover, those that use multipliers ([7–9]) also need to find a maximum (Max) to determine the correct timing position of the start of the data symbol, which is more computationally expensive than using a threshold detection (Th). The algorithms based on cross-correlation have been implemented without multipliers. In [11] and [12] the average bit-width of pipelined adders is smaller than those in [10]. It is due to the fact that whereas [11] and [12] work with 1 bit quantization for input and reference signals, in [10] the input signal is quantized with 7 bits, as shown in Table I. Our algorithm has a lower complexity than the rest because it only needs N_{ss} adders, where $N_{ss} << N_{ts}$, to determine the correct timing location. It also benefits from using a hard-wired tree adder instead of using XNOR multipliers. For example, with $N = 256$, $N_{cp} = 32$ and $N_p = 16$, the TSA described in [12] need 4624 real adders, 4608 XNORs and 2 threshold detectors while our algorithm need 512 real adders and 1 threshold detector; which implies 9 times less adders, 0 XNORs and

TABLE I
COMPLEXITY COMPARISONS

Algorithm	CP/TS-based	Auto/Cross-correlation	Input/TS bit-width	Multipliers	Adders	XNORs	Max/Th
[7] , [8]	CP	-	8/-	$2N_p + N_{cp} + N$	$2(N_p + N_{cp} + N)$	0	Max, Th
[9]	TS	Auto	5/-	2	2	0	Max
[10]	TS	Cross	7/1	0	$N_p(N_{ts} - 1)$	0	Th
[11]	TS	Cross	1/1	0	$N_p(N_{ts} - 1)$	$N_p(N_{ts})$	Th
[12]	TS	Cross	1/1	0	$N_p(N_{ts} + 1)$	$N_p(N_{ts})$	2Th
Proposed	TS	Cross	1/1	0	$N_p(N_{ss})$	0	Th

half hardware cost to detect the peak of the correlation. The small number and size of the adders in our TSA makes the system latency lower than in the other algorithms.

C. FPGA implementation

The time synchronization architecture has been modelled using the VHDL hardware description language and verified using the MATLAB finite precision model. It has been implemented on a Xilinx Virtex-7 XC7VX485T-2 FPGA using the Xilinx ISE 14.7 software tool. The number of Slice Registers and Slice LUTs used in our design is 1,690 and 1,773, respectively. The achieved maximum operating frequency is 464.253 MHz, which would allow it to work in real-time at a sampling rate up to 7.4 Gs/s.

V. CONCLUSION

In this work, a new time synchronization algorithm has been proposed for IM/DD optical systems using OFDM modulation. This synchronization algorithm makes use of a repetitive preamble, where the receiver cross-correlates the received signal with the repetitive part of the preamble using only one bit to quantize both signals. The use of a repetitive preamble allows us to reduce the length of the cross-correlation and the computational complexity with respect to the rest of the studied algorithms. A hardware architecture and its implementation in FPGA has been presented and experimentally validated in an optical communication testbed, showing the feasibility of our proposal and its good performance in low SNR scenarios.

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