

Contents

Abstract	iii
Resumen	v
Resum	vii
Contents	ix
List of Figures	xiii
List of Tables	xix
Acronyms	xxi
Preface	1
1 State of the art of non-binary low-density parity-check codes	9
1.1 LDPC codes and decoding process.	9
1.2 Nomenclature	11
1.3 Decoding schedules.	12
1.4 Decoding architectures	15
1.5 NB-LDPC decoding algorithms and architectures.	18
1.5.1 Trellis Extended Min-Sum Algorithm	23
1.6 Frame Error Rate (FER) Performance	26

1.7 Conclusions of the state of the art	30
2 Simplified Trellis Min-Max Decoder Architecture for NB-LDPC Codes	31
2.1 Introduction	32
2.2 Trellis Extended Min-Sum Algorithm.	34
2.3 Simplified Trellis Min-Max Algorithm	36
2.3.1 Algorithm Description	36
2.3.2 Frame Error Rate Performance	39
2.4 Check Node Architecture	39
2.5 Architecture for the Complete Decoder	44
2.5.1 Decoder Schedule	44
2.5.2 Decoder Architecture	45
2.5.3 Decoder Timing	47
2.5.4 Decoder Complexity and Implementation Results	48
2.6 Comparisons With Other NB-LDPC Decoders.	49
2.7 Conclusions	51
3 One Minimum Only Trellis Decoder for NB-LDPC Codes	53
3.1 Introduction	54
3.2 Trellis - Extended Min-Sum algorithm	56
3.3 One Minimum Only Trellis Decoder.	58
3.3.1 Estimators for the second minimum value	58
3.3.2 Statistical analysis of the different estimators.	60
3.3.3 Frame Error Rate Performance	62
3.4 OMO T-EMS and OMO T-MM Hardware Architectures.	63
3.4.1 Check Node Architecture	64
3.4.2 Complete decoder architecture.	68
3.5 Conclusions	70
4 Reduction of complexity for NB-LDPC decoders with compressed messages	71
4.1 Introduction	72
4.2 Non-binary LDPC message passing	73

4.3 Compressed Non-Binary Message-Passing (CNBMP)	76
4.4 Hardware impact of CNBMP	77
4.5 Conclusions	80
5 A 630 Mbps Non-Binary LDPC Decoder for FPGA	81
5.1 Introduction	82
5.2 Basis on NB-LDPC codes and T-MM decoding algorithm	83
5.3 Proposed Decoder Architecture.	85
5.3.1 Check-node architecture.	85
5.3.2 Top-level decoder architecture	87
5.4 Conclusions	91
6 High-performance NB-LDPC decoder with reduction of message exchange	93
6.1 Introduction	94
6.2 Trellis Min-Max decoding algorithm	96
6.3 Modified Trellis Min-Max Algorithm	98
6.3.1 Reformulation of Trellis Min-Max Algorithm	99
6.3.2 Reduction of replicated information in check-to-variable exchanged messages	99
6.3.3 Modified Trellis Min-Max algorithm	102
6.4 NB-LDPC Decoder Implementation.	107
6.4.1 CN architecture for mT-MM algorithm	109
6.4.2 Top-level decoder architecture	110
6.4.3 Decoder implementation results and comparisons	115
6.5 Conclusions	117
7 Reduced-complexity NB-LDPC decoder for high-order GF based on T-MM algorithm	119
7.1 Introduction	120
7.2 T-MM decoding algorithm with compressed messages.	123
7.3 T-MM algorithm with reduced set of messages	125
7.3.1 Reduction of the CN-to-VN messages	126
7.3.2 Performance Analysis	127
7.3.3 Generation of the set $I^*(a')$	129

7.4 Check Node architecture	132
7.5 Top-level decoder architecture and complexity comparison.	138
7.5.1 Decoder implementation results and comparisons	139
7.6 Conclusions	141
8 Discussion and conclusions	143
8.1 Summary of the main contributions.	143
8.2 Analysis of results.	146
8.3 Comparison with other works from literature	153
8.4 Conclusions	156
8.4.1 Objective 1: reduction of area and latency of Check Node (CN) processors	156
8.4.2 Objective 2: reduction of the number of messages exchanged between pro-	
cessors in NB-LDPC decoders.	157
8.4.3 Objective 3: implementation of high-performance decoders for Galois fields	
larger than 32.	158
8.4.4 Final Comments	159
8.5 Future Research Lines	160